

Favalon

AN762S-GL Module

Hardware Design Guide

Version: 1.1

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Shenzhen Favalon Technology Co., Ltd.

Applicable Model

No.	Product Model	Software Baseline	Applicable Customer	Description
1	AN762S-GL-HG70	-	-	LPDDR5X 16GB, UFS 128GB 5G version
2	AN762S-GL-HH70	-	-	LPDDR5X 24GB, UFS 128GB 5G version

Change History

Version	Date	Author	Reviewed by	Approved by	Change Description
1.0	2024-12-02	Zhang Conghui	Ma Baihui	Li Gao	Initial version
1.1	2023-02-24	Zhang Conghui	Ma Baihui	Li Gao	1) Update pin definition. 2) Update interface capability. 3) Update the process document name. 4) RF PCB Layout design guide. 5) Add CA_n2A-n29A. 6) Change GNSS CEP to 1.5. 7) Update WLAN TX/RX indicator. 8) Update cellular sensitivity and TX power. 9) Add safety instructions.

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1 About This Document

1.1 Description

This document describes the electrical characteristics, RF performance, structural dimensions, and application environment information of the Favalon AN762S-GL series modules. With the help of this document and other related documents, application developers can quickly understand the hardware functions of AN762S-GL series modules and carry out hardware development of their products.

1.2 Safety Instruction

Please observe the following safety instructions to ensure personal safety and protect the product and work environment from potential damages. The product manufacturer should communicate the following safety instructions to end users and incorporate the safety instructions into the User Manuals of end products. Favalon Auto Inc. will not take any responsibility for the consequences made by users who do not follow the safety rules or use the product improperly.

	Road safety first! When you are driving, do not use a handheld mobile terminal, even if it has a hands-free function. Stop the car before making a call.
	Please turn off the mobile terminal before boarding. It is prohibited to turn on the wireless function of the mobile terminal on the aircraft to prevent interference with the communication system of the aircraft. Failure to follow this prompt may affect flight safety or even violate the law.
	When you are in a hospital or health care facility, please be aware of restrictions on the use of mobile terminals. RF interference may cause abnormal operation of medical devices. Therefore, it may be required to turn off the mobile terminals.
	The mobile terminal does not guarantee a valid connection under any circumstances, for example, when the mobile terminal is in arrears or the (U)SIM is invalid. In case of emergency in above situations, remember to use the emergency call, and make sure your device is turned on and in an area with enough signal strength.
	Your mobile terminal will receive and transmit RF signals when it is turned on. When it is close to TV, radio, computer or other electronic equipment, RF interference will be generated.
	Keep the mobile terminal away from flammable gases. Please turn off the mobile terminal when it is near gas stations, oil depots, chemical plants or explosive workplaces. There are potential safety hazards caused by the operation of electronic devices in any area with potential explosion hazards.

2 Product Overview

2.1 Product Introduction

The AN762S-GL module is an automotive front-loading 5G communication module packaged based on MediaTek's MT8676 platform, which features rich functionality, high integration, small size, low power consumption, excellent performance, and stable quality, and can meet the front-loading needs of automotive intelligence and networking, helping customers to shorten the project development cycle, reduce R&D investment, and lower the quality risk.

- Integrated 2G/3G/4G/5G, Audio, GNSS, WIFI, BT (cellular version).
- Suitable for 360 panoramic reversing, multi-screen heterodyne display, DMS, T-BOX, AR navigation, driving record and other scenes.
- The main controller chip is an 8-core processor: 4 Arm Makalu cores and 4 Arm Klein cores with 4MB of L3 cache.
- Six 4-Lane MIPI CSI interfaces with CSI-2 support.
- Two 4-Lane MIPI DSI interfaces.
- Supporting LPDDR5X SDRAM and UFS3.1, Rel.16 NR, BT5.3 equipped with Android OS, it is powerful and feature-rich, which fully meets the requirements of smart car phone and automotive smart cockpit front-loading.

Table 2-1 Bands supported by **AN762S-GL**

Mode	Band
5G NR	n1, n2, n3, n5, n7, n8, n12, n14, n20, n25, n28, n29, n38, n40, n41, n48, n66, n71, n75, n77, n78
LTE FDD	B1, B2, B3, B4, B5, B7, B8, B12, B13, B14, B17, B20, B25, B26, B28, B29, B32, B66, B71
LTE TDD	B38, B40, B41, B42, B48
WCDMA	B1, B2, B4, B5, B8
GSM	GSM850, GSM900, DCS1800, PCS1900
WIFI 802.11a/b/g/n/ac/ax	2.4G/5G/6G
BT5.3 BLE	2.4G
GNSS	L1/L5

2.2 Main Performance

The AN762S-GL module is packaged in a SIP with 1032 pins and measures 63.0 mm x 60.0 mm x 5.2 mm.

Table 2-2 Performance specifications

Performance	Description
Power supply	Supply voltage: 3.8V to 4.2V, Typical voltage: 4.0V, transient peaks need to meet at least 10A
Application processor	8-core processor: 4 Arm Makalu cores and 4 Arm Klein cores, L3 cache 4MB
Memory	Supporting LPDDR5X SDRAM and UFS3.1
Power level	Class 4 (33dBm±2dB) for GSM850 Class 4 (33dBm±2dB) for GSM900 Class 1 (30dBm±2dB) for DCS1800 Class 1 (30dBm±2dB) for DCS1900 Class E2 (27dBm±3dB) for GSM850 8-PSK Class E2 (27dBm±3dB) for GSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800 8-PSK Class E2 (26dBm±3dB) for DCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (24dBm+1/-3dB) for LTE FDD bands Class 3 (24dBm+1/-3dB) for LTE TDD bands Class 2 (26dBm+2/-3dB) for 5G N41/N77/N78 bands Class 3 (24dBm+1/-3dB) for 5G others bands
GSM/GPRS/EDGE	GPRS: Supporting GPRS multi-slot class 12 Coding format: CS-1/CS-2/CS-3 and CS-4 Maximum downlink rate 107Kbps / Maximum uplink rate 85.6Kbps EDGE: Supporting EDGE multi-slot class 12 Supporting GMSK and 8-PSK Uplink coding format: CS 1-4 and MCS 1-9 Downlink coding format: CS 1-4 and MCS 1-9 Maximum downlink rate 296Kbps / Maximum uplink rate 236.8Kbps
WCDMA	Supporting 3GPP R99 DC-HSPA+ Supporting 16-QAM, 64-QAM and QPSK modem HSUPA: Maximum uplink rate 11.5Mbps DC-HSPA+: Maximum downlink rate 42.2Mbps
LTE	Supporting FDD/TDD R15 CAT18 Supporting 1.4M to 20M RF bandwidth Supporting downlink 4 x 4 MIMO Maximum uplink rate 200Mbps, maximum downlink rate 1.2Gbps
5G	Supporting FDD/TDD R16 Supporting 5-100M RF bandwidth Supporting downlink 4 x 4 MIMO Maximum uplink rate 500Mbps, maximum downlink rate 4Gbps
WLAN	Supporting 2.4G 及 5G/6G WLAN wireless communication

Performance	Description
	Supporting 802.11a/b/g/n/ac/ax standards, up to 2.8Gbps
Bluetooth	BT5.3 (BR/EDR+BLE)
GPS	GPS/Beidou/Glonass/Galileo/QZSS
LCD interface	Two sets of MIPI_DSI interfaces, support up to 3360 x 1600@120 Hz
DP interface	One set of DP, supporting DP1.4 compatible USB Type-C interface
USB interface	One set of USB 2.0 High Speed (HS) interface, supporting OTG mode One set of USB 3.0 Super Speed (SS) interface, supporting master/slave mode
Camera interface	6 sets of 4-Lane MIPI CSI interfaces, supporting 4Lane D-PHY
SIM interface	2 sets of SIM card interfaces, dual cards dual standby by default, supporting hot plug
UART interface	4 sets of UART serial ports: One set of two-wire DEBUG serial port; Two sets of two-wire high-speed serial ports; One set of four-wire high-speed serial port
SDIO interface /SDC2	One set of SD/SDIO 3.0, supporting hot plug
PCIe interface	One set of 1-lane Gen3.0 PCIe
SPI interface	Three sets of SPI interfaces with a maximum rate of 52MHz
I2S interface	6 sets of I2S interfaces, the maximum support for the sampling frequency of 384KHz in the main mode, I2S4 can be multiplexed to TDM, Bit clock up to support 12.288MHz
I2C interface	14 sets of I2C interfaces, which can be used for TP, Camera and Sensor
ADC interface	General ADC x 5
Antenna interface	TX+PRX antenna, DRX antenna, PRXM antenna, DRXM antenna, GNSS antenna, WIFI0(BT)/WIFI1 antenna
Physical property	Size: 63.0mm×60.0mm×5.2mm Package: 1032-Pin SIP
Temperature range	Operating temperature: -40°C to 85°C Storage temperature: -40°C to 95°C
RoHS	RoHS compliant
IP protection class	00

2.3 CA Combinations

2.3.1 CA Combinations Supported by AN762S-GL

LTE UL 2CA			
CA_1C	CA_3C	CA_38C	CA_40C
CA_42C	CA_48C	CA_66C	--
LTE DL 2CA			
CA_12A-66A	CA_4A-12A	CA_20A-32A	CA_3A-8A

CA_25A-25A	CA_4A-29A	CA_1A-1A	CA_3C
CA_2A-12A	CA_4A-4A	CA_1A-20A	CA_40C
CA_2A-2A	CA_4A-5A	CA_1A-28A	CA_5A-7A
CA_2A-48A	CA_4A-71A	CA_1A-3A	CA_7A-20A
CA_2A-66A	CA_5A-66A	CA_1A-5A	CA_7A-28A
CA_2A-4A	CA_5B	CA_1A-8A	CA_7A-8A
CA_2A-5A	CA_66A-66A	CA_1C	CA_7C
CA_2A-66A	CA_66A-71A	CA_20A-38A	CA_8A-32A
CA_2A-71A	CA_66C	CA_28A-32A	CA_8A-38A
CA_2C	CA_7A-7A	CA_3A-20A	CA_8A-41A
CA_41C	CA_7A-12A	CA_3A-28A	CA_38C
CA_48A-66A	CA_2A-13A	CA_3A-3A	CA_42C
CA_48C	CA_2A-14A	CA_3A-5A	CA_28A-40A
LTE DL 3CA			
CA_12A-66A-66A	CA_2A-4A-5A	CA_4A-4A-71A	CA_1A-3C
CA_2A-12A-66A	CA_2A-4A-71A	CA_5A-66A-66A	CA_28A-40C
CA_2A-2A-12A	CA_2A-5A-66A	CA_66A-66A-71A	CA_3A-3A-20A
CA_2A-2A-4A	CA_2A-66A-66A	CA_66A-66C	CA_3C-20A
CA_2A-2A-5A	CA_2A-66A-71A	CA_2A-2A-13A	CA_3C-28A
CA_2A-2A-66A	CA_2A-66C	CA_2A-2A-14A	CA_3C-8A
CA_2A-2A-71A	CA_41D	CA_1A-3A-20A	CA_5A-7A-7A
CA_2A-48A-66A	CA_48C-66A	CA_1A-3A-28A	CA_5A-7C
CA_2A-48C	CA_48D	CA_1A-3A-3A	CA_7C-20A
CA_2A-4A-12A	CA_4A-4A-12A	CA_1A-3A-5A	CA_7C-28A
CA_2A-4A-4A	CA_4A-4A-5A	CA_1A-3A-8A	CA_1A-1A-3A
LTE DL 4CA			
CA_2A-12A-66A-66A	CA_2A-2A-4A-71A	CA_2A-66A-66A-71A	CA_1A-3C-20A
CA_2A-2A-12A-66A	CA_2A-2A-5A-66A	CA_48D-66A	CA_1A-3C-28A
CA_2A-2A-4A-12A	CA_2A-2A-66A-66A	CA_48E	CA_1A-3C-8A
CA_2A-2A-4A-4A	CA_2A-2A-66A-71A	CA_1A-1A-3C	CA_41E
CA_2A-2A-4A-5A	CA_2A-5A-66A-66A	CA_1A-3A-3A-20A	--
NR DL 2CA			
CA_n12A-n66A	CA_n2A-n78A	CA_n66A-n71A	CA_n28A-n75A
CA_n12A-n77A	CA_n41A-n41A	CA_n66A-n77A	CA_n28A-n78A
CA_n25A-n25A	CA_n41A-n71A	CA_n66A-n78A	CA_n3A-n28A
CA_n25A-n66A	CA_n41A-n77A	CA_n71A-n77A	CA_n3A-n78A
CA_n25A-n71A	CA_n48A-n48A	CA_n71B	CA_n40A-n78A
CA_n25A-n77A	CA_n48A-n66A	CA_n77A-n77A	CA_n5A-n7A

CA_n25A-n78A	CA_n48C	CA_n1A-n28A	CA_n75A-n78A
CA_n2A-n12A	CA_n5A-n66A	CA_n1A-n3A	CA_n78C
CA_n2A-n2A	CA_n5A-n77A	CA_n1A-n78A	CA_n7A-n28A
CA_n2A-n5A	CA_n5A-n78A	CA_n1A-n8A	CA_n7A-n78A
CA_n2A-n66A	CA_n5B	CA_n20A-n78A	CA_n8A-n40A
CA_n2A-n77A	CA_n66a-n66a	CA_n28A-n40A	CA_n8A-n78A
CA_n2A-n29A	--	--	--

2.4 EN-DC Combinations

2.4.1 EN-DC Combinations Supported by AN762S-GL

5G-NR	Combination Type	EN-DC Combination	4G DL 4 × 4 MIMO	5G-NR DL 4 × 4 MIMO	4G UL	5G-NR UL
TDD	1DL + FR1	DC_25A_n77A	25A	n77A	25A	n77A
TDD	1DL + FR1	DC_26A_n77A	--	n77A	26A	n77A
TDD	1DL + FR1	DC_2A_n77A	2A	n77A	2A	n77A
TDD	1DL + FR1	DC_12A_n77A	--	n77A	12A	n77A
TDD	1DL + FR1	DC_2A_n78A	2A	n78A	2A	n78A
TDD	1DL + FR1	DC_12A_n78A	--	n78A	12A	n78A
TDD	1DL + FR1	DC_13A_n77A	--	n77A	13A	n77A
TDD	1DL + FR1	DC_14A_n77A	--	n77A	14A	n77A
TDD	1DL + FR1	DC_71A_n78A	--	n78A	71A	n78A
TDD	1DL + FR1	DC_4A_n78A	4A	n78A	4A	n78A
TDD	1DL + FR1	DC_5A_n77A	--	n77A	5A	n77A
TDD	1DL + FR1	DC_5A_n78A	--	n78A	5A	n78A
TDD	1DL + FR1	DC_66A_n77A	66A	n77A	66A	n77A
TDD	1DL + FR1	DC_7A_n77A	7A	n77A	7A	n77A
TDD	1DL + FR1	DC_7A_n78A	7A	n78A	7A	n78A
TDD	1DL + FR1	DC_1A_n77A	1A	n77A	1A	n77A
TDD	1DL + FR1	DC_1A_n78A	1A	n78A	1A	n78A
TDD	1DL + FR1	DC_20A_n77A	--	n77A	20A	n77A
TDD	1DL + FR1	DC_20A_n78A	--	n78A	20A	n78A
TDD	1DL + FR1	DC_28A_n77A	--	n77A	28A	n77A
TDD	1DL + FR1	DC_28A_n78A	--	n78A	28A	n78A
TDD	1DL + FR1	DC_38A_n78A	38A	n78A	38A	n78A
TDD	1DL + FR1	DC_3A_n77A	3A	n77A	3A	n77A

5G-NR	Combination Type	EN-DC Combination	4G DL 4 × 4 MIMO	5G-NR DL 4 × 4 MIMO	4G UL	5G-NR UL
TDD	1DL + FR1	DC_3A_n78A	3A	n78A	3A	n78A
TDD	1DL + FR1	DC_40A_n77A	--	n77A	40A	n77A
TDD	1DL + FR1	DC_40A_n78A	--	n78A	40A	n78A
TDD	1DL + FR1	DC_41A_n77A	41A	n77A	41A	n77A
TDD	1DL + FR1	DC_41A_n78A	41A	n78A	41A	n78A
TDD	1DL + FR1	DC_8A_n77A	--	n77A	8A	n77A
TDD	1DL + FR1	DC_8A_n78A	--	n78A	8A	n78A
TDD	2DL + FR1	DC_25A-25A_n77A	25A	n77A	25A	n77A
TDD	2DL + FR1	DC_2A-2A_n77A	2A	n77A	2A	n77A
TDD	2DL + FR1	DC_2A-12A_n77A	2A	n77A	2A,12A	n77A
TDD	2DL + FR1	DC_2A-2A_n78A	2A	n78A	2A	n78A
TDD	2DL + FR1	DC_2A-12A_n78	2A	n78A	2A,12A	n78A
TDD	2DL + FR1	DC_2A-13A_n77A	2A	n77A	2A,13A	n77A
TDD	2DL + FR1	DC_2A-14A_n77A	2A	n77A	2A,14A	n77A
TDD	2DL + FR1	DC_2A-5A_n77A	2A	n77A	2A,5A	n77A
TDD	2DL + FR1	DC_2A-71A_n78A	2A	n78A	2A,71A	n78A
TDD	2DL + FR1	DC_2A-5A_n78A	2A	n78A	2A,5A	n78A
TDD	2DL + FR1	DC_5A-66A_n77A	66A	n77A	66A,5A	n77A
TDD	2DL + FR1	DC_66A-66A_n77A	66A	n77A	66A	n77A
TDD	2DL + FR1	DC_7A-12A_n78A	7A	n78A	7A,12A	n78A
TDD	2DL + FR1	DC_7A-7A_n77A	7A	n77A	7A	n77A
TDD	2DL + FR1	DC_1A-20A_n78A	1A	n78A	1A,20A	n78A
TDD	2DL + FR1	DC_1A-28A_n78A	1A	n78A	1A,28A	n78A
TDD	2DL + FR1	DC_1A-3A_n78A	1A	n78A	1A,3A	n78A
TDD	2DL + FR1	DC_1A-5A_n78A	1A	n78A	1A,5A	n78A
TDD	2DL + FR1	DC_1A-8A_n78A	1A	n78A	1A,8A	n78A
TDD	2DL + FR1	DC_20A-32A_n78A	--	n78A	20A	n78A
TDD	2DL + FR1	DC_3A-20A_n78A	3A	n78A	3A,20A	n78A
TDD	2DL + FR1	DC_3A-28A_n78A	3A	n78A	3A,28A	n78A
TDD	2DL + FR1	DC_3A-3A_n77A	3A	n77A	3A	n77A
TDD	2DL + FR1	DC_3A-3A_n78A	3A	n78A	3A	n78A
TDD	2DL + FR1	DC_3A-5A_n78A	3A	n78A	3A,5A	n78A
TDD	2DL + FR1	DC_3A-8A_n78A	3A	n78A	3A,8A	n78A
TDD	2DL + FR1	DC_3C_n78A	3A	n78A	3A	n78A
TDD	2DL + FR1	DC_7C_n78A	7A	n78A	7A	n78A
TDD	3DL + FR1	DC_2A-2A-12A_n77A	2A	n77A	2A,12A	n77A

5G-NR	Combination Type	EN-DC Combination	4G DL 4 × 4 MIMO	5G-NR DL 4 × 4 MIMO	4G UL	5G-NR UL
TDD	3DL + FR1	DC_2A-2A-12A_n78A	2A	n78A	2A,12A	n78A
TDD	3DL + FR1	DC_2A-2A-13A_n77A	2A	n77A	2A,13A	n77A
TDD	3DL + FR1	DC_2A-2A-14A_n77A	2A	n77A	2A,14A	n77A
TDD	3DL + FR1	DC_2A-2A-5A_n77A	2A	n77A	2A,5A	n77A
TDD	3DL + FR1	DC_2A-2A-71A_n78A	2A	n78A	2A,71A	n78A
TDD	3DL + FR1	DC_1A-3C_n78A	1A	n78A	1A,3A	n78A
TDD	3DL + FR1	DC_3C-20A_n78A	3A	n78A	3A,20A	n78A
TDD	3DL + FR1	DC_3C-28A_n78A	3A	n78A	3A,28A	n78A
TDD	3DL + FR1	DC_3C-8A_n78A	3A	n78A	3A,8A	n78A



Note

The 4G bands not listed in the 4G DL 4 x 4 MIMO do not support DL 4 x 4 MIMO, but DL 2 x 2 MIMO is supported by default.

2.5 Hardware Block Diagram

The following hardware block diagram shows the main hardware features of the AN762S-GL modules, including:

- Baseband
- Wireless transceiver
- PMU
- Storage
- External interfaces
 - Communication extension interface (USB/UART/I2C/SDIO/SPI/I2S/PCIe)
 - SIM card interface
 - MIPI DSI interface
 - MIPI CSI interface
 - Audio interface

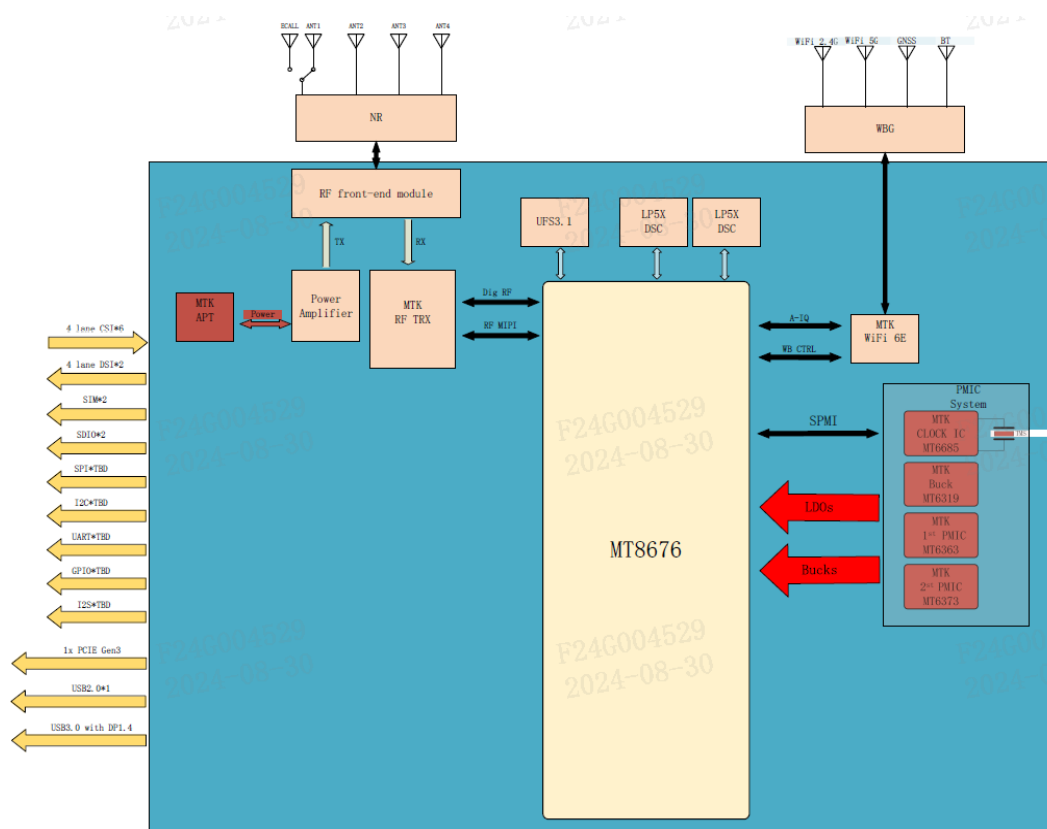


Figure 2-1 Hardware block diagram

2.6 Pin Definition

2.6.1 Pin Distribution



2.6.2 Pin Description

Table 2-3 I/O parameter description

Type
IO

Table 2-3 I/O parameter description

Type	Description
IO	Input/Output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Type	Description
PD	Pull-down
PU	Pull-up
G	Ground
NP	No-pull
Hi-Z	High resistance

Table 2-4 Pin description

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
Power Supply					
VBAT1	CA31	PI	Module 4V power input		Typical 4.0V, transient peaks need to meet at least 10A
VBAT2	CA32	PI	Module 4V power input		
VBAT3	CA33	PI	Module 4V power input		
VBAT4	CB31	PI	Module 4V power input		
VBAT5	CB32	PI	Module 4V power input		
VBAT6	CB33	PI	Module 4V power input		
VIO18_PMU	DD18	PO	Module 1.8V power output		1.8V, 50mA, for pull-up/down configuration applications only
VMC_PMU	DD9	PO	SD card IO power supply		1.8V/3.0V, 160mA
VMCH_PMU	DC9	PO	SD card main power supply		1.8V/3.0V, 500mA
SIM1_PWR	DD6	PO	SIM1 power output		1.8V/3.0V, 160mA
SIM2_PWR	DD10	PO	SIM2 power output		1.8V/3.0V, 160mA
VUSB_PMU	DD7	PO	USB level output		3.0V, 160mA
GND	AA1, AA2, AA5, AA11, AA17, AA21, AA27, AA31, AA34, AA35, AB2, AB5, AB11, AB17, AB21, AB27, AB31, AB34, AC3~AC18, AC21~ AC31, AJ9~ AJ27, BA1, BA2, BA4, BA5, BA7~BA9, BA11~BA13, BA15~BA17, BA19, BA20, BA21, BA23, BA24, BA25, BA27, BA28, BA29, BA31, BA32, BA33, BA35, BB2~ BB34, BC3~BC33, BE9, BF9, BJ9~BJ27, CA1, CA2, CA12, CA18, CA25, CA29, CA30, CA34, CA35, CB2, CB12, CB18, CB25, CB29, CB30, CB34, CC3, CC5~CC23, CC29~CC33, CD10, CD16, CD32, CE10, CE16, CF6~CF15, CJ9~CJ27, DA1, DA2, DA9, DA12, DA18, DA24, DA30, DA34, DA35, DB2, DB9, DB12, DB18, DB24, DB30, DB34, DC12~DC29, DC31~DC33, DE19, DG16, DG20, DG24, DH19, DH24, DJ9~DJ27, E166~E225				
Control Interface					
USB_VBUS_DET	DD31	DI	VBUS detection signal	5.0V	● USB insertion detection ● The pin level is pulled high, and the module will power on by default after powering up.

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
PWRKEY_N	DD30	DI	Power-on signal	4.0V	Module default internal pull-up, active low, pull-down time > 500ms
RESET_N	AF6	DI	Module reset signal	1.8V	Module default internal pull-up, active low, prohibit the addition of external pull-ups
FORCE_BOOT	CE24	DI	Force download signal	1.8V	The module defaults to internal pull-up, and enters the FORCE_BOOT mode when it detects the pin is low before powering on
BOOT_STATUS	DE26	DO	Module normal boot signal	1.8V	High level indicates that the module boots normally
SUSPEND_STATUS	BF15	DO	Module status output signal	1.8V	● High level indicates that the module is in the wake-up state ● Low level indicates that the module is in sleep state
WAKEUP_N	BF16	DI	Module wake-up input signal	1.8V	Input high to wake up, input low to sleep
RECOVERY_N	DE28	DI	RECOVERY function pin	1.8V	● The module detects the pin as low during the boot phase, and the system enters Recovery mode, at which time it can be upgraded or restored in Recovery mode. The pin can be reused as a GPIO after the module boots and enters the Kernel, and external pull-downs is prohibited. ● Pull up the pin before booting, and the module boots normally
RAMDUMP_N	BD29	DI	RAMDUMP function pin	1.8V	● For module crash log, supporting AEE mechanism real-time dump log capture ● After the module is booted, the pin is pulled down and the module enters RAMDUMP mode
FASTBOOT_N	DF26	DI	FASTBOOT function pin	1.8V	● When the module detects that the pin is low during startup, the system enters FASTBOOT mode. At this time, the external processor can directly perform image burning on the specified partition of the module through the USB interface. After the module enters Kernel, the pin can be multiplexed into GPIO. External pull-down is prohibited. ● Pull up the pin, and the system

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
					starts normally
SIM card interface					
SIM1_CLK	BE5	DO	SIM1 clock	1.8V	--
SIM1_DATA	BF7	DI/DO	SIM1 data	1.8V	--
SIM1_RESET	BF8	DO	SIM1 reset	1.8V	--
SIM1_DETECT	DG15	DI	SIM1 insertion detection signal	1.8V	--
SIM2_CLK	BE6	DO	SIM2 clock	1.8V	--
SIM2_DATA	BE7	DI/DO	SIM2 data	1.8V	--
SIM2_RESET	BF6	DO	SIM2 reset	1.8V	--
SIM2_DETECT	DH15	DI	SIM2 insertion detection signal	1.8V	--
MSDC interface					
MSDC_CLK	AB32	DO	SD card clock	1.8V	--
MSDC_CMD	AA32	DI/DO	SD card command signal	1.8V	--
MSDC_DAT0	AA33	DI/DO	SD card data signal 0	1.8V	--
MSDC_DAT1	AC32	DI/DO	SD card data signal 1	1.8V	--
MSDC_DAT2	AC33	DI/DO	SD card data signal 2	1.8V	--
MSDC_DAT3	AB33	DI/DO	SD card data signal 3	1.8V	--
MSDC_DETECT	DD5	DI	SD card insertion detection	1.8V	--
PCIe interface					
PCIE0_CLKREQ	CF30	DI/DO	PCIe clock request signal	1.8V	--
PCIE0_RST	DG8	DI/DO	PCIe reset signal	1.8V	--
PCIE0_WAKE	DG7	DI/DO	PCIe wake-up signal	1.8V	--
PCIE0_CLK_M	AA24	AO	PCIe clock signal -	--	--
PCIE0_CLK_P	AB24	AO	PCIe clock signal +	--	--
PCIE0_RX0_M	AA23	AI	PCIe data receiving -	--	--
PCIE0_RX0_P	AB23	AI	PCIe data receiving +	--	--
PCIE0_TX0_M	AA22	AO	PCIe data transmitting -	--	--
PCIE0_TX0_P	AB22	AO	PCIe data transmitting +	--	--
I2C interface					
I2C0_SCL	AD31	OD	I2C0 serial clock	1.8V	No pull-up by default inside the module
I2C0_SDA	AD30	OD	I2C0 serial data	1.8V	No pull-up by default inside the module
I2C1_SCL	BD5	OD	I2C1 serial clock	1.8V	No pull-up by default inside the module
I2C1_SDA	BD6	OD	I2C1 serial data	1.8V	No pull-up by default inside the module

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
I2C2_SCL	DG13	OD	I2C2 serial clock	1.8V	No pull-up by default inside the module
I2C2_SDA	DH13	OD	I2C2 serial data	1.8V	No pull-up by default inside the module
I2C3_SCL	CH15	OD	I2C3 serial clock	1.8V	No pull-up by default inside the module
I2C3_SDA	CH16	OD	I2C3 serial data	1.8V	No pull-up by default inside the module
I2C4_SCL	DF15	OD	I2C4 serial clock	1.8V	No pull-up by default inside the module
I2C4_SDA	DF16	OD	I2C4 serial data	1.8V	No pull-up by default inside the module
I2C5_SCL	CG18	OD	I2C5 serial clock	1.8V	No pull-up by default inside the module
I2C5_SDA	CF18	OD	I2C5 serial data	1.8V	No pull-up by default inside the module
I2C6_SCL	AD27	OD	I2C6 serial clock	1.8V	No pull-up by default inside the module
I2C6_SDA	AE27	OD	I2C6 serial data	1.8V	No pull-up by default inside the module
I2C7_SCL	AD28	OD	I2C7 serial clock	1.8V	No pull-up by default inside the module
I2C7_SDA	AD29	OD	I2C7 serial data	1.8V	No pull-up by default inside the module
I2C8_SCL	AE16	OD	I2C8 serial clock	1.8V	No pull-up by default inside the module
I2C8_SDA	AE15	OD	I2C8 serial data	1.8V	No pull-up by default inside the module
I2C9_SCL	AB18	OD	I2C9 serial clock	1.8V	No pull-up by default inside the module
I2C9_SDA	AA18	OD	I2C9 serial data	1.8V	No pull-up by default inside the module
I2C10_SCL	BH26	OD	I2C10 serial clock	1.8V	No pull-up by default inside the module
I2C10_SDA	BG26	OD	I2C10 serial data	1.8V	No pull-up by default inside the module
I2C11_SCL	DF9	OD	I2C11 serial clock	1.8V	No pull-up by default inside the module
I2C11_SDA	DF10	OD	I2C11 serial data	1.8V	No pull-up by default inside the module
I2C12_SCL	CE29	OD	I2C12 serial clock	1.8V	IMU dedicated No pull-up by default inside the module
I2C12_SDA	CF29	OD	I2C12 serial data	1.8V	
I2C13_SCL	AF14	OD	I2C13 serial clock	1.8V	No pull-up by default inside the module
I2C13_SDA	AF13	OD	I2C13 serial data	1.8V	No pull-up by default inside the module
USB2.0 interface					

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
USB0_DM	CA4	AI/AO	USB2.0 differential data signal +	--	--
USB0_DP	CB4	AI/AO	USB2.0 differential data signal -	--	--
USB0_ID	AG13	AI	USB ID signal	1.8V	--
USB0_VBUS_DET	DD31	AI	VBUS detection signal	5.0V	● USB insertion detection ● When the pin level is pulled high, the module will be powered on by default
USB3.0 interface					
USB0_SS_RX_M	CD5	AI	USB3.0 differential data reception -	--	● Multiplexing DP_LN3_TX_M ● Adaptive switching is not supported
USB0_SS_RX_P	CE5	AI	USB3.0 differential data reception +	--	● Multiplexing DP_LN3_TX_P ● Adaptive switching is not supported
USB0_SS_TX_M	CA6	AO	USB3.0 differential data transmission -	--	● Multiplexing DP_LN2_TX_M ● Adaptive switching is not supported
USB0_SS_TX_P	CB6	AO	USB3.0 differential data transmission +	--	● Multiplexing DP_LN2_TX_P ● Adaptive switching is not supported
UART interface					
UART0_TX	AE19	DO	Serial port 0 data transmission	1.8V	DEBUG serial port The default baud rate is 921600
UART0_RX	AE18	DI	Serial port 0 data 0 data reception	1.8V	DEBUG serial port The default baud rate is 921600
UART1_TX	AE26	DO	Serial port 1 data transmission	1.8V	--
UART1_RX	AD26	DI	Serial port 1 data 0 data reception	1.8V	--
UART2_TX	AF11	DO	Serial port 2 data transmission	1.8V	--
UART2_RX	AF12	DI	Serial port 2 data 0 data reception	1.8V	--
UART2_CTS	AG11	DI	Serial port 2 clear to send	1.8V	--
UART2_RTS	AG12	DO	Serial port 2 request to send	1.8V	--
UART3_TX	DH12	DO	Serial port 3 data transmission	1.8V	--
UART3_RX	DH11	DI	Serial port 3 data reception	1.8V	--
SPI interface					
SPI0_CLK	BF21	DO	SPI0 clock signal	1.8V	--
SPI0_CS	BF22	DO	SPI0 chip selection signal	1.8V	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
SPI0_MI	BG22	DI	SPI0 data input	1.8V	--
SPI0_MO	BG21	DO	SPI0 data output	1.8V	--
SPI1_CLK	BE18	DO	SPI1 clock signal	1.8V	--
SPI1_CS	BD18	DO	SPI1 chip selection signal	1.8V	--
SPI1_MI	BE17	DI	SPI1 data input	1.8V	--
SPI1_MO	BD17	DO	SPI1 data output	1.8V	--
SPI2_CLK	BF19	DO	SPI2 clock signal	1.8V	--
SPI2_CS	BF20	DO	SPI2 chip selection signal	1.8V	--
SPI2_MI	BG19	DI	SPI2 data input	1.8V	--
SPI2_MO	BG20	DO	SPI2 data output	1.8V	--
SPI2_IRQ	AG9	DI	SPI2 data reception request	1.8V	Active at high level
SPI2_ASK	CG24	DO	SPI2 data transmission request	1.8V	Active at high level
DSI interface					
DSI0_CK0_M	CD13	AI/AO	DSI0 MIPI clock -	--	--
DSI0_CK0_P	CE13	AI/AO	DSI0 MIPI clock +	--	--
DSI0_D0_M	CD12	AI/AO	DSI0 MIPI data line 0 -	--	--
DSI0_D0_P	CE12	AI/AO	DSI0 MIPI data line 0+	--	--
DSI0_D1_M	CD14	AI/AO	DSI0 MIPI data line 1-	--	--
DSI0_D1_P	CE14	AI/AO	DSI0 MIPI data line 1+	--	--
DSI0_D2_M	CD11	AI/AO	DSI0 MIPI data line 2-	--	--
DSI0_D2_P	CE11	AI/AO	DSI0 MIPI data line 2+	--	--
DSI0_D3_M	CD15	AI/AO	DSI0 MIPI data line 3-	--	--
DSI0_D3_P	CE15	AI/AO	DSI0 MIPI data line 3+	--	--
DSI1_CK0_M	CB20	AI/AO	DSI1 MIPI clock -	--	--
DSI1_CK0_P	CA20	AI/AO	DSI1 MIPI clock +	--	--
DSI1_D0_M	CB24	AI/AO	DSI1 MIPI data line 0-	--	--
DSI1_D0_P	CA24	AI/AO	DSI1 MIPI data line 0+	--	--
DSI1_D1_M	CB21	AI/AO	DSI1 MIPI data line 1-	--	--
DSI1_D1_P	CA21	AI/AO	DSI1 MIPI data line 1+	--	--
DSI1_D2_M	CB23	AI/AO	DSI1 MIPI data line 2-	--	--
DSI1_D2_P	CA23	AI/AO	DSI1 MIPI data line 2+	--	--
DSI1_D3_M	CB22	AI/AO	DSI1 MIPI data line 3-	--	--
DSI1_D3_P	CA22	AI/AO	DSI1 MIPI data line 3+	--	--
DP interface					
DP_AUX_M	CB3	AI/AO	DP auxiliary channel -	--	--
DP_AUX_P	CA3	AI/AO	DP auxiliary channel +	--	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
DP_LN0_TX_M	CA5	AI/AO	DP transmission link LN0-	--	--
DP_LN0_TX_P	CB5	AI/AO	DP transmission link LN0+	--	--
DP_LN1_TX_M	CC4	AI/AO	DP transmission link LN1-	--	--
DP_LN1_TX_P	CD4	AI/AO	DP transmission link LN1+	--	--
DP_HPD	AH22	DI	DP hot-plug signal	1.8V	Can be multiplexed as SPI3_CLK
Camera 0 interface					
MIPI_CSI0_CLK_M	AB14	AO	Camera 0 MIPI clock -	--	--
MIPI_CSI0_CLK_P	AA14	AO	Camera 0 MIPI clock +	--	--
MIPI_CSI0_L0_M	AB13	AI/AO	Camera 0 MIPI data line 0 -	--	--
MIPI_CSI0_L0_P	AA13	AI/AO	Camera 0 MIPI data line 0 +	--	--
MIPI_CSI0_L1_M	AB15	AI/AO	Camera 0 MIPI data line 1 -	--	--
MIPI_CSI0_L1_P	AA15	AI/AO	Camera 0 MIPI data line 1 +	--	--
MIPI_CSI0_L2_M	AB12	AI/AO	Camera 0 MIPI data line 2 -	--	--
MIPI_CSI0_L2_P	AA12	AI/AO	Camera 0 MIPI data line 2 +	--	--
MIPI_CSI0_L3_M	AB16	AI/AO	Camera 0 MIPI data line 3 -	--	--
MIPI_CSI0_L3_P	AA16	AI/AO	Camera 0 MIPI data line 3 +	--	--
Camera 1 interface					
MIPI_CSI1_CLK_M	DA27	AO	Camera 1 MIPI clock -	--	--
MIPI_CSI1_CLK_P	DB27	AO	Camera 1 MIPI clock +	--	--
MIPI_CSI1_L0_M	DA26	AI/AO	Camera 1 MIPI data line 0-	--	--
MIPI_CSI1_L0_P	DB26	AI/AO	Camera 1 MIPI data line 0+	--	--
MIPI_CSI1_L1_M	DA28	AI/AO	Camera 1 MIPI data line 1-	--	--
MIPI_CSI1_L1_P	DB28	AI/AO	Camera 1 MIPI data line 1+	--	--
MIPI_CSI1_L2_M	DA25	AI/AO	Camera 1 MIPI data line 2-	--	--
MIPI_CSI1_L2_P	DB25	AI/AO	Camera 1 MIPI data line 2+	--	--
MIPI_CSI1_L3_M	DA29	AI/AO	Camera 1 MIPI data line 3-	--	--
MIPI_CSI1_L3_P	DB29	AI/AO	Camera 1 MIPI data line 3+	--	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
			3+		
Camera 2 interface					
MIPI_CSI2_CLK_M	DA21	AO	Camera 2 MIPI clock -	--	--
MIPI_CSI2_CLK_P	DB21	AO	Camera 2 MIPI clock +	--	--
MIPI_CSI2_L0_M	DA20	AI/AO	Camera 2 MIPI data line 0-	--	--
MIPI_CSI2_L0_P	DB20	AI/AO	Camera 2 MIPI data line 0+	--	--
MIPI_CSI2_L1_M	DA22	AI/AO	Camera 2 MIPI data line 1-	--	--
MIPI_CSI2_L1_P	DB22	AI/AO	Camera 2 MIPI data line 1+	--	--
MIPI_CSI2_L2_M	DA19	AI/AO	Camera 2 MIPI data line 2-	--	--
MIPI_CSI2_L2_P	DB19	AI/AO	Camera 2 MIPI data line 2+	--	--
MIPI_CSI2_L3_M	DA23	AI/AO	Camera 2 MIPI data line 3-	--	--
MIPI_CSI2_L3_P	DB23	AI/AO	Camera 2 MIPI data line 3+	--	--
Camera 3 interface					
MIPI_CSI3_CLK_M	AB8	AO	Camera 3 MIPI clock -	--	--
MIPI_CSI3_CLK_P	AA8	AO	Camera 3 MIPI clock +	--	--
MIPI_CSI3_L0_M	AB7	AI/AO	Camera 3 MIPI data line 0-	--	--
MIPI_CSI3_L0_P	AA7	AI/AO	Camera 3 MIPI data line 0+	--	--
MIPI_CSI3_L1_M	AB9	AI/AO	Camera 3 MIPI data line 1-	--	--
MIPI_CSI3_L1_P	AA9	AI/AO	Camera 3 MIPI data line 1+	--	--
MIPI_CSI3_L2_M	AB6	AI/AO	Camera 3 MIPI data line 2-	--	--
MIPI_CSI3_L2_P	AA6	AI/AO	Camera 3 MIPI data line 2+	--	--
MIPI_CSI3_L3_M	AB10	AI/AO	Camera 3 MIPI data line 3-	--	--
MIPI_CSI3_L3_P	AA10	AI/AO	Camera 3 MIPI data line 3+	--	--
Camera 4 interface					
MIPI_CSI4_CLK_M	DA15	AO	Camera 4 MIPI clock -	--	--
MIPI_CSI4_CLK_P	DB15	AO	Camera 4 MIPI clock +	--	--
MIPI_CSI4_L0_M	DA14	AI/AO	Camera 4 MIPI data line 0-	--	--
MIPI_CSI4_L0_P	DB14	AI/AO	Camera 4 MIPI data line 0+	--	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
MIPI_CSI4_L1_M	DA16	AI/AO	Camera 4 MIPI data line 1-	--	--
MIPI_CSI4_L1_P	DB16	AI/AO	Camera 4 MIPI data line 1+	--	--
MIPI_CSI4_L2_M	DA13	AI/AO	Camera 4 MIPI data line 2-	--	--
MIPI_CSI4_L2_P	DB13	AI/AO	Camera 4 MIPI data line 2+	--	--
MIPI_CSI4_L3_M	DA17	AI/AO	Camera 4 MIPI data line 3-	--	--
MIPI_CSI4_L3_P	DB17	AI/AO	Camera 4 MIPI data line 3+	--	--
Camera 5 interface					
MIPI_CSI5_CLK_M	DB33	AO	Camera 5 MIPI clock -	--	--
MIPI_CSI5_CLK_P	DA33	AO	Camera 5 MIPI clock +	--	--
MIPI_CSI5_L0_M	DB32	AI/AO	Camera 5 MIPI data line 0-	--	--
MIPI_CSI5_L0_P	DA32	AI/AO	Camera 5 MIPI data line 0+	--	--
MIPI_CSI5_L1_M	AB3	AI/AO	Camera 5 MIPI data line 1-	--	--
MIPI_CSI5_L1_P	AA3	AI/AO	Camera 5 MIPI data line 1+	--	--
MIPI_CSI5_L2_M	DB31	AI/AO	Camera 5 MIPI data line 2-	--	--
MIPI_CSI5_L2_P	DA31	AI/AO	Camera 5 MIPI data line 2+	--	--
MIPI_CSI5_L3_M	AB4	AI/AO	Camera 5 MIPI data line 3-	--	--
MIPI_CSI5_L3_P	AA4	AI/AO	Camera 5 MIPI data line 3+	--	--
I2S					
I2S0_MCLK	AA20	DO	I2S0 main clock	1.8V	--
I2S0_BCK	CD30	DO	I2S0 bit clock	1.8V	--
I2S0_LRCK	CD29	DO	I2S0 frame synchronization signal	1.8V	--
I2S0_DI	CE28	DI	I2S0 serial data input	1.8V	--
I2S0_DO	CE27	DO	I2S0 serial data output	1.8V	--
I2S1_MCLK	AB20	DO	I2S1 main clock	1.8V	--
I2S1_BCK	CC25	DO	I2S1 bit clock	1.8V	--
I2S1_LRCK	CD25	DO	I2S1 frame synchronization signal	1.8V	--
I2S1_DI	CD24	DI	I2S1 serial data input	1.8V	--
I2S1_DO	CD23	DO	I2S1 serial data output	1.8V	--
I2S2_BCK	BF10	DO	I2S2 bit clock	1.8V	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
I2S2_LRCK	BH12	DO	I2S2 frame synchronization signal	1.8V	--
I2S2_DI	BH11	DI	I2S2 serial data input	1.8V	--
I2S2_DO	BF11	DO	I2S2 serial data output	1.8V	--
I2S3_MCLK	CF27	DO	I2S3 main clock	1.8V	--
I2S3_BCK	CF28	DO	I2S3 bit clock	1.8V	--
I2S3_LRCK	CH25	DO	I2S3 frame synchronization signal	1.8V	--
I2S3_DI	CG27	DI	I2S3 serial data input	1.8V	--
I2S4_BCK0	CA28	DI	I2S4 bit clock	1.8V	Supports I2S and TDM mode inputs, defaults to I2S mode
I2S4_LRCK0	CC28	DI	I2S4 frame synchronization signal	1.8V	Supports I2S and TDM mode inputs, defaults to I2S mode
I2S4_DO0	CC26	DO	I2S4 serial data output Data0	1.8V	Supports I2S and TDM mode inputs, defaults to I2S mode
I2S4_DO1	CE25	DO	I2S4 serial data output Data1	1.8V	Supports I2S and TDM mode inputs, defaults to I2S mode
I2S4_DI0	CD27	DI	I2S4 serial data input Data0	1.8V	I2S and TDM mode inputs are supported, and only I2S4_DI0 can be used as input in TDM mode
I2S4_DI1	CC27	DI	I2S4 serial data input Data1	1.8V	--
I2S5_BCK	BG27	DO	I2S5 bit clock	1.8V	--
I2S5_LRCK	BH27	DO	I2S5 frame synchronization signal	1.8V	--
I2S5_DI	BG28	DI	I2S5 serial data input	1.8V	--
I2S5_DO	BH28	DO	I2S5 serial data output	1.8V	--
JTAG interface					
JTAG_TCK	AE28	DI	Test clock	1.8V	--
JTAG_TDI	AE30	DI	Test data input	1.8V	--
JTAG_TDO	AE29	DO	Test data output	1.8V	--
JTAG_TMS	AF30	DI	Test mode selection	1.8V	--
JTAG_RESET	AF29	DI	Test reset	1.8V	--
ADC interface					
ADC1	DD8	AI	ADC input detection	--	Voltage range: 0.04V-1.78V
ADC2	DF7	AI	ADC input detection	--	Voltage range: 0.04V-1.78V
ADC3	DF8	AI	ADC input detection	--	Voltage range: 0.04V-1.78V
ADC4	DC8	AI	ADC input detection	--	Voltage range: 0.04V-1.78V
ADC5	DE7	AI	ADC input detection	--	Voltage range: 0.04V-1.78V
Antenna interface					
ANT1	BA6	I/O	Main antenna interface	--	Band: refer to Table 4-2 Band Antenna Assignments
ANT2	BA10	I/O	Diversity antenna	--	Band: refer to Table 4-2 Band

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
			interface		Antenna Assignments
ANT3	BA14	I/O	4 x 4 MIMO antenna interface	--	Band: refer to Table 4-2 Band Antenna Assignments
ANT4	BA18	I/O	4 x 4 MIMO antenna interface	--	Band: refer to Table 4-2 Band Antenna Assignments
ANT_WB0	BA30	I/O	WIFI_BT antenna interface	--	Band: refer to Table 4-5 Band Antenna Assignments
ANT_WB1	BA26	I/O	WIFI antenna interface	--	Band: refer to Table 4-5 Band Antenna Assignments
ANT_GNSS	BA34	I/O	GNSS antenna interface	--	Band: refer to Table 4-6 Band Antenna Assignments
GPIO interface					
GPS_PPS	BE10	DO	GPS_PPS synchronization signal	1.8V	--
GPIO_0	AE23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_1	AE24	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_2	AE25	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_3	AD25	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable as DP_HPD DP hot-plug signal
GPIO_4	AH23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_5	AG14	DO	General input/output interface	1.8V	--
GPIO_6	BG15	DI/DO	General input/output interface	1.8V	--
GPIO_7	DF13	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_8	DF14	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_9	AH19	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_10	BH20	DI/DO	General input/output interface	1.8V	--
GPIO_11	AH15	DI/DO	General input/output interface	1.8V	--
GPIO_12	AG15	DI/DO	General input/output interface	1.8V	--
GPIO_13	BG7	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_14	AA19	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to SPI3_CS

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
GPIO_15	DF18	DI/DO	General input/output interface	1.8V	--
GPIO_16	CF24	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to SPI3_MI
GPIO_17	CF23	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to SPI3_MO
GPIO_18	CE23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_19	CH9	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_20	DF12	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_21	AE20	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_22	CG28	DI/DO	General input/output interface	1.8V	--
GPIO_23	AG17	DI/DO	General input/output interface	1.8V	--
GPIO_24	CE30	DI/DO	General input/output interface	1.8V	--
GPIO_25	CE31	DI/DO	General input/output interface	1.8V	--
GPIO_26	AD22	DI/DO	General input/output interface	1.8V	--
GPIO_27	DF11	DI/DO	General input/output interface	1.8V	--
GPIO_28	CG29	DI/DO	General input/output interface	1.8V	--
GPIO_29	DE27	DI/DO	General input/output interface	1.8V	--
GPIO_30	BH23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_31	BG23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_32	AE13	DI/DO	General input/output interface	1.8V	--
GPIO_33	BE22	DI	General input interface	1.8V	● Interrupt input can be supported ● 100-ohm resistor in series is required
GPIO_34	BE23	DI	General input interface	1.8V	● Interrupt input can be supported ● 100-ohm resistor in series is required
GPIO_35	DF19	DI/DO	General input/output	1.8V	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
			interface		
GPIO_36	DH27	DI/DO	General input/output interface	1.8V	--
GPIO_37	CG23	DI/DO	General input/output interface	1.8V	--
GPIO_38	CG22	DI/DO	General input/output interface	1.8V	--
GPIO_39	DD27	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_40	DH9	DI/DO	General input/output interface	1.8V	--
GPIO_41	DG10	DI/DO	General input/output interface	1.8V	--
GPIO_42	DD28	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_43	DD26	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_44	BG18	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_45	DC11	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_46	DH26	DI/DO	General input/output interface	1.8V	--
GPIO_47	DF6	DI/DO	General input/output interface	1.8V	--
GPIO_48	CE19	DI/DO	General input/output interface	1.8V	--
GPIO_49	DC4	DO	General output interface	1.8V	--
GPIO_50	DD4	DO	General output interface	1.8V	--
GPIO_51	CH22	DO	General output interface	1.8V	--
GPIO_52	CD31	DO	General output interface	1.8V	--
GPIO_53	DC3	DO	General output interface	1.8V	--
GPIO_54	DA11	DO	General output interface	1.8V	--
GPIO_55	DB11	DO	General output interface	1.8V	--
GPIO_56	DA10	DO	General output interface	1.8V	--
GPIO_57	DH10	DI/DO	General input/output interface	1.8V	--
GPIO_58	CG25	DI/DO	General input/output interface	1.8V	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
GPIO_59	CE21	DI/DO	General input/output interface	1.8V	--
GPIO_60	AD24	DI/DO	General input/output interface	1.8V	--
GPIO_61	AG10	DI/DO	General input/output interface	1.8V	--
GPIO_62	DH22	DI/DO	General input/output interface	1.8V	--
GPIO_63	DH14	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_64	DG14	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_65	AF9	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_66	AE17	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_67	CG7	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_68	BH22	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_69	CH8	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_70	BD4	DO	General output interface	1.8V	Can be used for backup antenna switching control
GPIO_71	BH24	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_72	BG24	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_73	BG25	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_74	BH25	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_75	CD26	DI/DO	General input/output interface	1.8V	--
GPIO_76	CD28	DI/DO	General input/output interface	1.8V	--
GPIO_77	AD21	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to PWM0
GPIO_78	DH8	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to PWM1
GPIO_79	BH19	DI/DO	General input/output interface	1.8V	Multiplexable to PWM2
GPIO_80	DD17	DO	General output interface	1.8V	--
GPIO_81	DD15	DO	General output interface	1.8V	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
GPIO_100	AE5	DO	General output interface	1.8V	--
GPIO_101	AE6	DO	General output interface	1.8V	--
GPIO_102	AD4	DO	General output interface	1.8V	--
GPIO_103	DE29	DO	General output interface	1.8V	--
GPIO_104	DE18	DO	General output interface	1.8V	--
GPIO_105	DD14	DO	General output interface	1.8V	--
GPIO_106	DF22	DO	General output interface	1.8V	--
GPIO_107	DD16	DO	General output interface	1.8V	--
GPIO_108	DF21	DO	General output interface	1.8V	--
GPIO_109	DF23	DO	General output interface	1.8V	--
GPIO_110	CB28	DI/DO	General input/output interface	1.8V	--
GPIO_111	AF10	DI/DO	General input/output interface	1.8V	--
GPIO_112	CE26	DI/DO	General input/output interface	1.8V	--

Note: The default voltage level of normal GPIO is 1.8V.

NC Pin

RESERVED	AE14, BE30, BE31, AB19, AC19, AC20, AD5~AD9, AD14, AD17~AD20, AD23, AD32, AE7, AE8, AE21, AE22, AE31, AF7, AF8, AF15~AF28, AG7, AG8, AG16, AG18, AG19~AG29, AH8~AH14, AH16~AH18, AH24~AH28, BD7~BD16, BD19~BD28, BD30~BD32, BE8, BE11~BE16, BE19~BE21, BE24, BE25, BF12, BF14, BF17, BF18, BF23~BF30, BG8~BG10, BG12, BG13, BG14, BG16, BG17, BH8~BH10, BH13~BH18, CD6, CE6, CE17, CE18, CF19~CF22, CG8~CG17, CG19, CG20, CG26, CH10~CH14, CH17~CH20, CH24, CH26, DA3, DA6, DB3, DB6, DC30, DC10, DD12, DD13, DD29, DD32, DE5, DE6, DE8, DE9, DE15, DE16, DE17, DE30, DE31, DF17, DF25, DF27, DF28, DF30, DG9, DG17, DG25~DG29, DH16, DH17, DH18, DH21, DH23, DH25, DH28, CE22, CE20, CC24, DH20, CB19, CA19, DE10, CH27, CH28, CD17~CD22, CB27, CA27, CB26, CA26, DD11, DF29, CF17, CF16, CA13, CB13, CA17, CB17, CA16, CB16, CA15, CB15, CA14, CB14, BF13, CA9, CB9, CA10, CB10, CA8, CB8, CA11, CB11, CA7, CB7, CE7, CE8, CE9, CD7,	Suspended
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Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
			CD8, CD9, DE11, DE14, DE12, DE13, DF24, BG11, DG11, DG12, DG23, AH20, CH23, DG18, DG19, DF20, AH21, DA7, DB7, DA8, DB8, DA5, DB5, DA4, DB4, BG29, BH21, AE12, AD13, AD12, AD11, AE11, AE10, AE9, AD10, AB26, AA26, AB25, AA25, AB28, AA28, AB30, AA30, AB29, AA29, DD20~DD25, DE20~DE25, AD15, AD16, DG22, DG21, CF25, CF26, CG21, CH21, BE26~BE29, BA22, BA3, DB10, DC5, DC7, DC6, DD19		

3 Application Interfaces

3.1 Power Supply Characteristics

3.1.1 Power Supply

The AN762S-GL series module provides 6 VBAT pins for connecting an external power supply to power the module. The power supply input voltage range is 3.8V to 4.2V, and the typical value is 4.0V. The performance of the module input power supply, such as load capacity, ripple size, etc., will directly affect the performance and stability of the module during normal operation. In the limit case, the peak current of the module can reach 10A. If the power supply capacity is insufficient, the power supply voltage drops below 3.8V instantaneously, and the module may have abnormal phenomena such as power-off or restart. The power supply voltage drop diagram is as follows:

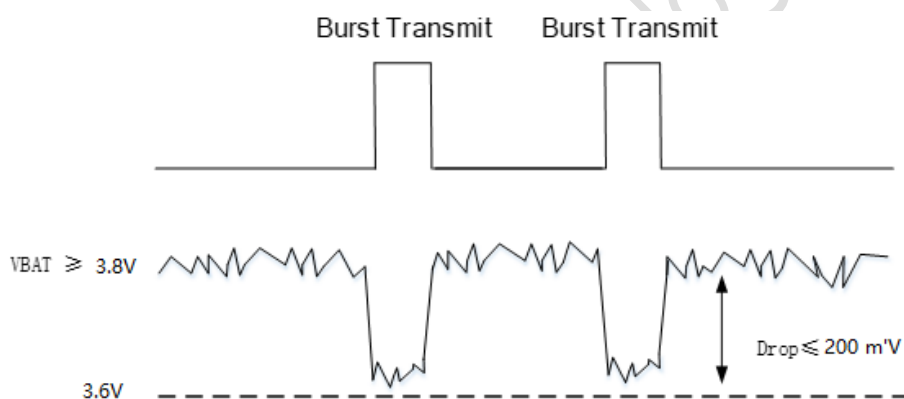


Figure 3-1 Voltage drop

3.1.2 Power Input

The external power supply supplies power to the AN762S-GL series module through the VBAT pin to ensure that the power supply voltage is not lower than 3.8V. Close to the VBAT input of the module, it is recommended to connect two tantalum capacitors with low ESR of 220uF and filter capacitors of 1uF, 100nF, 10nF, 1nF, 100pF in parallel, and it is recommended that the PCB traces of VBAT be as short as possible and wide enough (not less than 10mm) to meet at least 10A current. The ground plane of the power supply part is as complete as possible to reduce the equivalent impedance of the VBAT trace and ensure that there is not too much voltage drop under high current at maximum transmit power.

Table 3-1 Power supply

Parameter	Minimum Value	Typical Value	Maximum Value	Unit
VBAT (DC)	3.8	4.0	4.2	V



Note

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VBAT supply voltage must be guaranteed in the range of 3.8V to 4.2V, supply voltage below 3.8V may lead to system instability, supply voltage above 4.2V may lead to hardware damage, or even damage.

The power supply design is shown in figure:

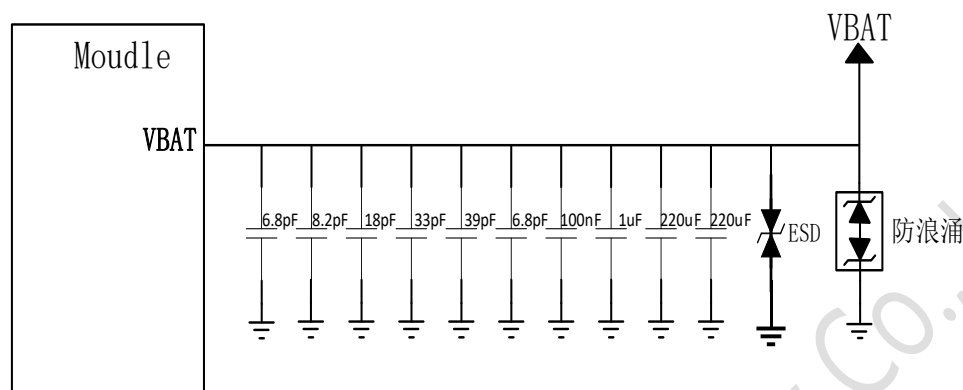


Figure 3-2 Power supply design diagram

The filter capacitors for the power supply are designed as shown in the following table:

Table 3-2 Filter capacitor design for power supply

Recommended Capacitance	Application	Description
220uF x 2	Voltage regulator capacitors	Reducing power fluctuations during module operation requires low ESR capacitors. LDO or DC-DC power supply requires no less than 440uF capacitance. Battery power supply can be appropriately reduced to 100uF to 220uF capacitance.
1uF, 100nF, 10nF	Filter capacitors	Filtering of clock and digital signal interference.
1nF, 100pF, 33pF, 6.8pF	Decoupling capacitors	Instantaneous power should be more than 2000W, clamping voltage should meet module VBAT working voltage.
TVS anti-surge tube x 1	Surge protection	The power reference is about 80W, and the parasitic capacitance is about 20pf.

3.1.3 Power Output

The AN762S-GL module has multiple sets of power outputs for powering peripheral circuits. When applied, 33pF and 10pF capacitors can be connected in parallel to effectively eliminate high-frequency interference.

Table 3-3 Power output

Pin Name	Programmable Voltage (V)	Default Voltage (V)	Drive current (mA)
VIO18_PMU	1.8	1.8	50

Pin Name	Programmable Voltage (V)	Default Voltage (V)	Drive current (mA)
VMC_PMU	1.8/1.86/2.9/3.0	3.0	160
VMCH_PMU	1.8/1.86/2.9/3.0	3.0	500
SIM1_PWR	1.8/2.9/3.0	1.8	160
SIM2_PWR	1.8/2.9/3.0	1.8	160
VUSB_PMU	3.0	3.0	160

3.2 Control Signals

3.2.1 Power-on

The AN762S-GL series module provides PWRKEY_N pin as the power-on signal interface.

Table 3-4 Power-on control signals

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
PWRKEY_N	DD30	DI	Power-on signal	4.0V	Be pulled up inside the module by default, active low, pull down time > 500ms
USB_VBUS_DET	DD31	DI	VBUS detection signal	5.0V	• USB insertion detection • When the pin level is pulled up, the module will boot after powering on.

After VBAT is powered on, the module is triggered to power on by pulling PWRKEY_N pin low for more than 500ms.

The circuit reference design is as follows:

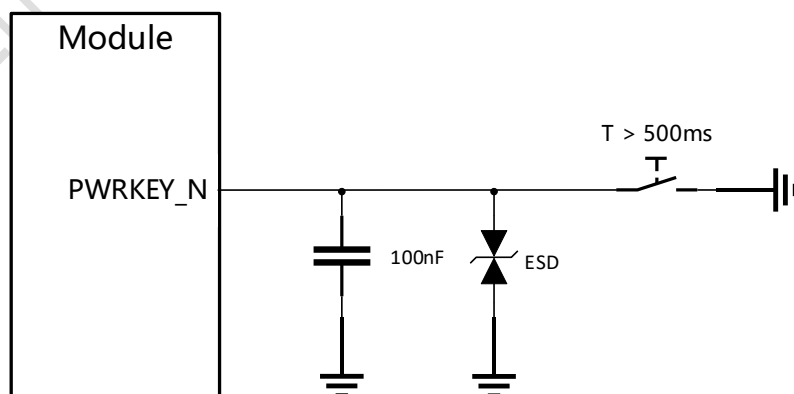


Figure 3-3 Key-powered circuit reference design

The power-on timing is as follows:

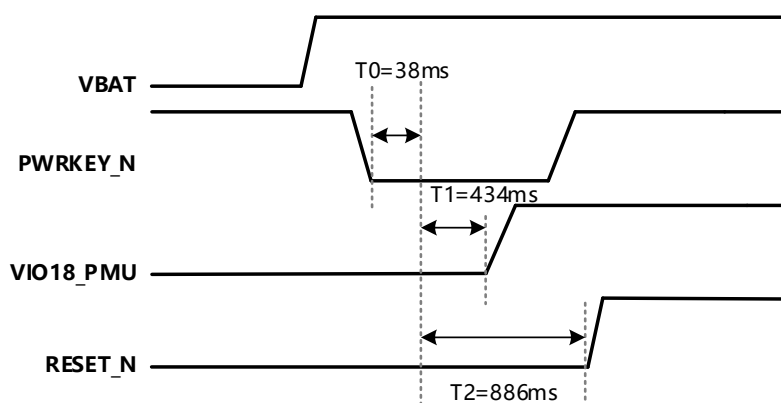


Figure 3-4 Power-on timing

Design considerations:

Reserve 22-ohm series resistance for PWRKEY_N interface and parallel TVS tube to prevent ESD damage.

3.2.2 Forced Download Interface

The AN762S-GL module provides the FORCE_BOOT pin as a forced download interface.

Table 3-5 Power-on control signal

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
FORCE_BOOT	CE24	DI	Forced download interface	1.8V	Be pulled up inside the module. When the pin is detected as low level before power-on, the module enters FORCE_BOOT mode.

Press the power-on key and short FORCE_BOOT and GND, the module can enter emergency download mode, which is used for the final processing mode when the product cannot start normally or run due to fault. Please reserve this pin for the convenience of subsequent software upgrade and debugging.

The circuit reference design is as follows:

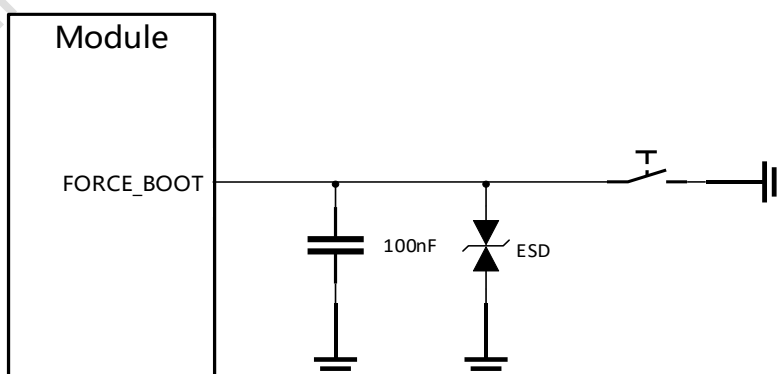


Figure 3-5 Key forced download circuit reference design

The FORCE_BOOT timing is as follows:

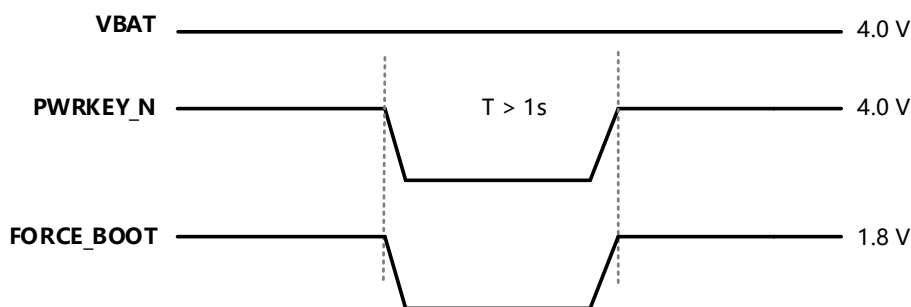


Figure 3-6 FORCE_BOOT timing

Design considerations:

FORCE_BOOT interface parallel TVS tube, to prevent ESD damage.

3.2.3 Sleep/Wake-up

The AN762S-GL module provides WAKEUP_N pin for module wake-up input signal and SUSPEND_STATUS pin for module status output signal.

Figure 3-6 Sleep/wake-up control signals

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
WAKEUP_N	BF16	DI	Module wake-up input signal	1.8V	Input high to wake up, input low to sleep
SUSPEND_STATUS	BF15	DO	Module status output signal	1.8V	- High level indicates that the module is in wake-up state - Low level indicates that the module is in sleep state

3.2.4 Reset

The AN762S-GL module provides the RESET_N pin to reset the module.

Table 3-7 Reset control signal

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
RESET_N	AF6	DI	Module reset signal	1.8V	Be pulled up inside the module by default, active at low level, and external pull-up is not allowed.

After the VBAT power-up is complete, the module is triggered to power on by pulling the RESET_N pin low for more than 200ms.

The reference circuit design is as follows:

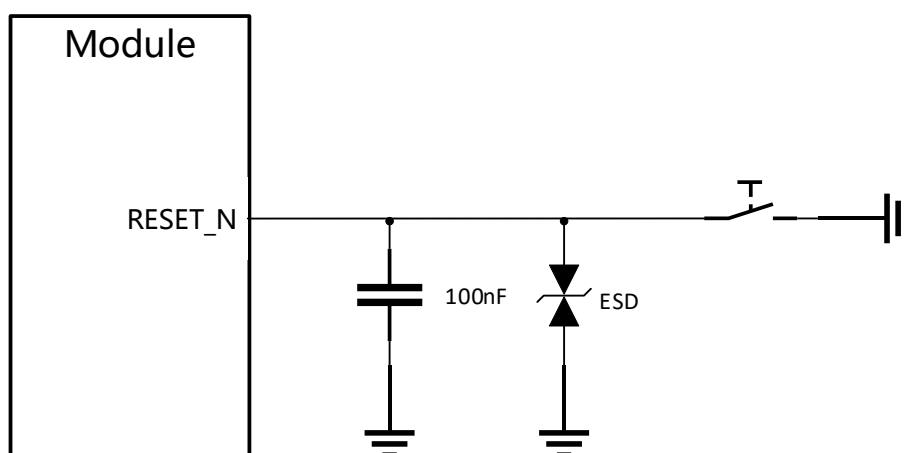


Figure 3-7 Key reset circuit reference design

The reset timing is as follows:

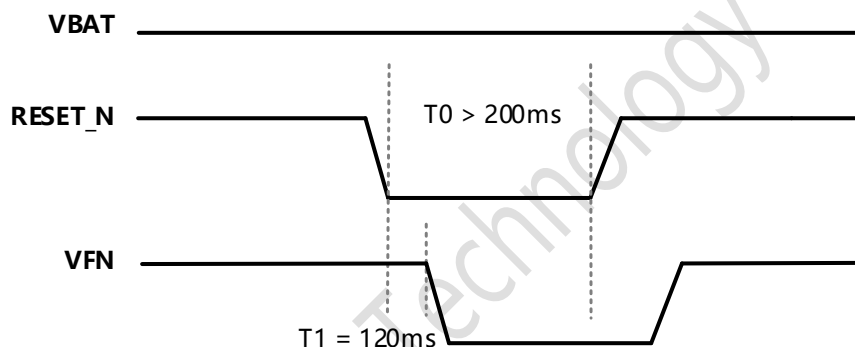


Figure 3-8 Reset timing

Design considerations:

- 1) The RESET_N interface is connected in parallel with a TVS tube to prevent ESD damage.
- 2) VFN outputs each voltage for the PMIC.

3.3 USB Interfaces

The AN762S-GL module supports a set of USB3.0 Gen1; USB2.0 supports OTG mode, backward compatible with USB 1.1 FS mode. USB interfaces support Host and Device modes. The following table defines the pins of the USB interfaces:

Table 3-8 USB 2.0 pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
USB0_DM	CA4	AI/AO	USB2.0 differential data signal +	--	--
USB0_DP	CB4	AI/AO	USB2.0 differential data signal -	--	--
USB0_ID	AG13	AI	USB ID signal	1.8V	--

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
USB0_VBUS_DET	DD31	AI	VB0US detection signal	5.0V	● USB insertion detection ● When the pin level is pulled high, the module will boot after powering on.

Table 3-9 USB 3.0 pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
USB0_SS_TX_M	CA6	AO	USB3.0 differential data transmission	--	● Multiplexing DP_LN2_TX_M ● Adaptive switching is not supported
USB0_SS_TX_P	CB6	AO	USB3.0 differential data transmission +	--	● Multiplexing DP_LN2_TX_P ● Adaptive switching is not supported
USB0_SS_RX_M	CD5	AI	USB3.0 differential data reception +	--	● Multiplexing DP_LN3_TX_M ● Adaptive switching is not supported
USB0_SS_RX_P	CE5	AI	USB3.0 differential data reception +	--	● Multiplexing DP_LN3_TX_P ● Adaptive switching is not supported

The USB 2.0 interface circuit reference design is as follows:

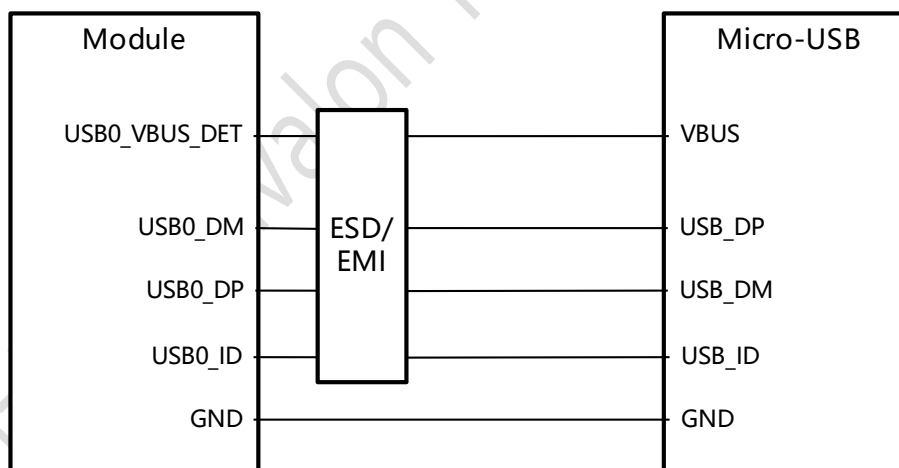


Figure 3-9 Micro-USB interface circuit reference design

The USB 3.0 interface circuit reference design is as follows:

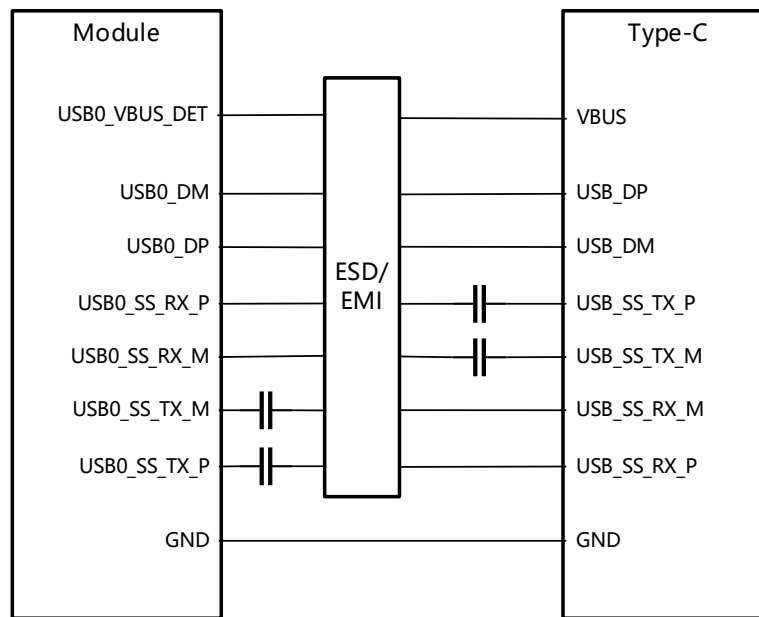


Figure 3-10 Type-C interface circuit reference design

Design considerations:

- 1) The parasitic capacitance of the ESD device on the USB3.0 signal must be less than 0.5pF, with an isolation capacitance tolerance of 0.22uF.
- 2) Since USB insertion triggers the module to power on when using the USB0_VBUS_DET signal, if the pin is suspended, it is necessary to add an interrupt IO detection on the USB VBUS signal to detect the USB insertion/removal signal.
- 3) The ESD protection device for USB0_DP/DM requires a junction capacitance of less than 2pF.
- 4) The highest transmission rate of USB0_DP and USB0_DM is 480Mbps. The routing requirements are equal length and three-dimensional grounding. Follow the principle of high-speed differential routing and do a good job of differential 90-ohm impedance control.
- 5) Please select output 5V specification for the reference circuit design DC-DC supporting OTG function.
- 6) USB3.0 is a high-speed signal line, and the routing requires equal length and three-dimensional grounding. Follow the principle of high-speed differential routing and do a good job of differential 90-ohm impedance control.
- 7) USB 2.0 maximum trace length should be less than 5000mil, internal difference less than 50mil and insertion loss < 2dB@240Mhz; USB 3.0 maximum trace length should be less than 2000mil, internal difference less than 5mil, internal difference less than 300mil and insertion loss < 5dB@4.05Ghz.

3.4 UART Interface

The AN762S-GL module has four UART interfaces, all in the 1.8V voltage domain. The pin definitions are listed in the table below:

Table 3-10 UART pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
UART0_TX	AE19	DO	Serial port 0 data transmission	1.8V	DEBUG serial port, and the default baud rate is 921600
UART0_RX	AE18	DI	Serial port 0 data reception	1.8V	DEBUG serial port, and the default baud rate is 921600
UART1_TX	AE26	DO	Serial port 1 data transmission	1.8V	--
UART1_RX	AD26	DI	Serial port 1 data reception	1.8V	--
UART2_TX	AF11	DO	Serial port 2 data transmission	1.8V	--
UART2_RX	AF12	DI	Serial port 2 data reception	1.8V	--
UART2_CTS	AG11	DI	Serial port 2 clear to send	1.8V	--
UART2_RTS	AG12	DO	Serial port 2 request to send	1.8V	--
UART3_TX	DH12	DO	Serial port 3 data transmission	1.8V	--
UART3_RX	DH11	DI	Serial port 3 data reception	1.8V	--

The voltage domain of each serial port is 1.8V; when communicating with serial ports in other voltage domains, it is necessary to add a level conversion chip. The reference circuit design is as follows:

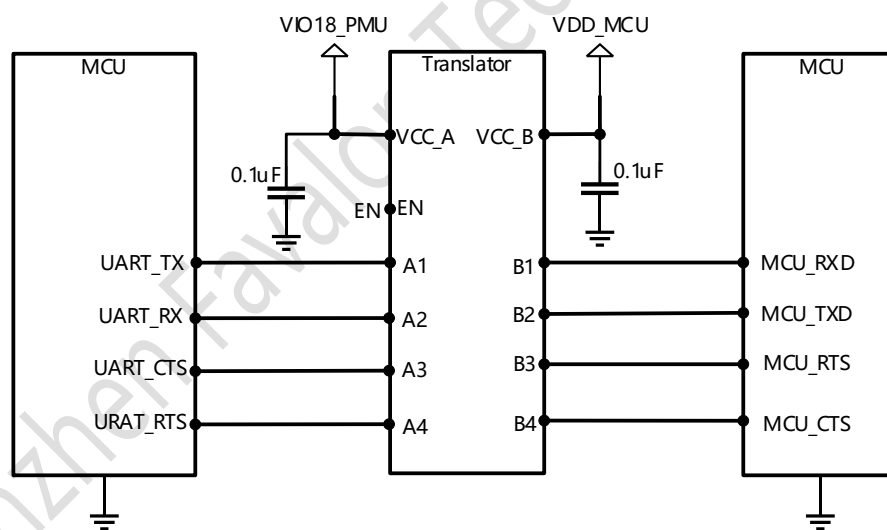


Figure 3-11 UART interface circuit reference design

Design considerations:

- 1) It is recommended to reserve 0-ohm series resistor to prevent waveform overshoot during debugging.
- 2) The highest speed of high-speed serial port supports 4MHz. When routing, it covers the ground left and right and is far away from interference sources.

3.5 SPI Interface

The AN762S-GL module provides three SPI interfaces with a maximum rate of 52MHz. Only master mode is supported. The pin definition is as follows:

Table 5-12 SPI interface pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
SPI0_CLK	BF21	DO	SPI0 clock signal	1.8V	--
SPI0_CS	BF22	DO	SPI0 chip selection signal	1.8V	--
SPI0_MI	BG22	DI	SPI0 data input	1.8V	--
SPI0_MO	BG21	DO	SPI0 data output	1.8V	--
SPI1_CLK	BE18	DO	SPI1 clock signal	1.8V	--
SPI1_CS	BD18	DO	SPI1 chip selection signal	1.8V	--
SPI1_MI	BE17	DI	SPI1 data input	1.8V	--
SPI1_MO	BD17	DO	SPI1 data output	1.8V	--
SPI2_CLK	BF19	DO	SPI2 clock signal	1.8V	--
SPI2_CS	BF20	DO	SPI2 chip selection signal	1.8V	--
SPI2_MI	BG19	DI	SPI2 data input	1.8V	--
SPI2_MO	BG20	DO	SPI2 data output	1.8V	--
SPI2_IRQ	AG9	DI	SPI2 data reception request	1.8V	Active high
SPI2_ASK	CG24	DO	SPI2 data transmission request	1.8V	Active high

The reference circuit design is as follows:

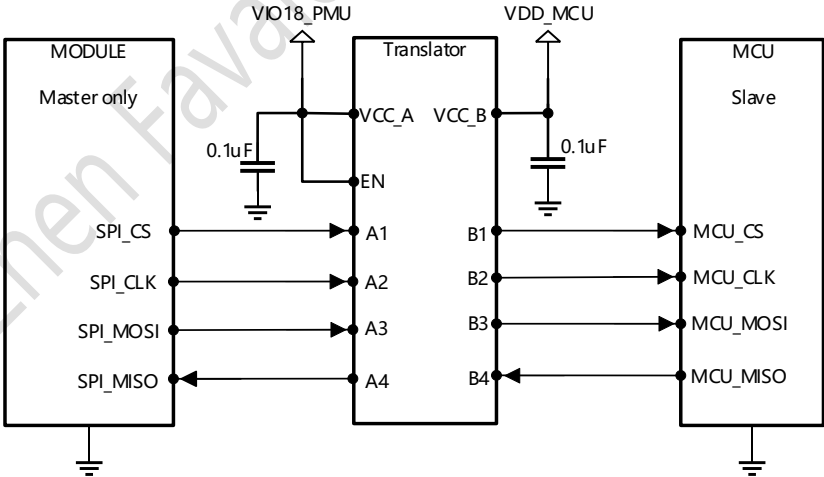


Figure 3-12 SPI interface circuit reference design

Design considerations:

- 1) It is recommended to reserve 0-ohm series resistor to prevent waveform overshoot during debugging.
- 2) SPI signal supports the highest frequency of 52Mbps, and when routing, it covers the ground left and right, away from interference sources.
- 3) All traces of the SPI bus shall be well shielded by nearby ground traces in the same layer, and ground traces

shall be wrapped in layers n-1 and n+1 and close to each other.

- 4) All traces of the SPI bus should be kept away from noise sources such as buck switching nodes.
- 5) SPI maximum trace length should be less than 5 inches (distance of module-to-peripheral).
- 6) SPI signal traces (CS, CK, MOSI, MISO) should have a gap of less than 2 mm.

3.6 SIM Card Interface

The AN762S-GL module reserves two sets of SIM cards with default dual card dual standby, and supports hot-plug.

Table 3-12 SIM pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
SIM1_CLK	BE5	DO	SIM1 clock	1.8V	--
SIM1_DATA	BF7	DI/DO	SIM1 data	1.8V	--
SIM1_RESET	BF8	DO	SIM1 reset	1.8V	--
SIM1_DETECT	DG15	DI	SIM1 insertion detection signal	1.8V	--
SIM2_CLK	BE6	DO	SIM2 clock	1.8V	--
SIM2_DATA	BE7	DI/DO	SIM2 data	1.8V	--
SIM2_RESET	BF6	DO	SIM2 reset	1.8V	--
SIM2_DETECT	DH15	DI	SIM2 insertion detection signal	1.8V	--

The SIM card interface circuit reference design is as follows:

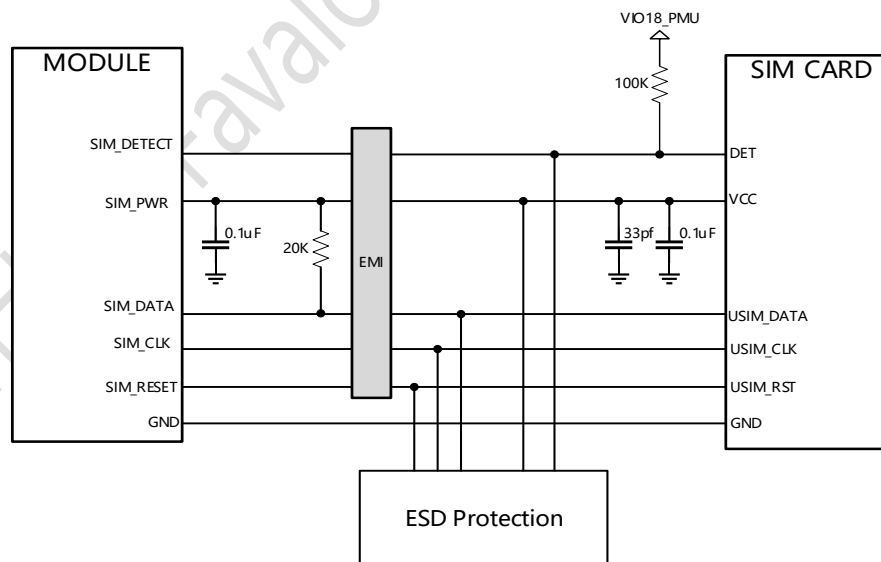


Figure 3-13 SIM interface circuit reference design

Design considerations:

- 1) SIM card layout and routing must be away from EMI interference sources such as RF antennas and digital switching power supplies.

- 2) SIM card signal filter capacitance, ESD devices should be placed close to the card slot, and the junction capacitance is not greater than 7pF.
- 3) The pull-up 10K ohm resistor for the hot plug detection signal uses the VIO18_PMU power supply.
- 4) The signal traces CLK, IO and RST are well protected.

3.7 MSDC Interface

The AN762S-GL module supports a set of SDIO interfaces, and supports version 3.0. The pin definition is as follows:

Table 3-13 MSDC interface pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
MSDC_CLK	AB32	DO	SD card clock	1.8V	--
MSDC_CMD	AA32	DI/DO	SD card command signal	1.8V	--
MSDC_DAT0	AA33	DI/DO	SD card data signal 0	1.8V	--
MSDC_DAT1	AC32	DI/DO	SD card data signal 1	1.8V	--
MSDC_DAT2	AC33	DI/DO	SD card data signal 2	1.8V	--
MSDC_DAT3	AB33	DI/DO	SD card data signal 3	1.8V	--
MSDC_DETECT	DD5	DI	SD card insertion detection	1.8V	--

The MSDC interface circuit reference design is as follows:

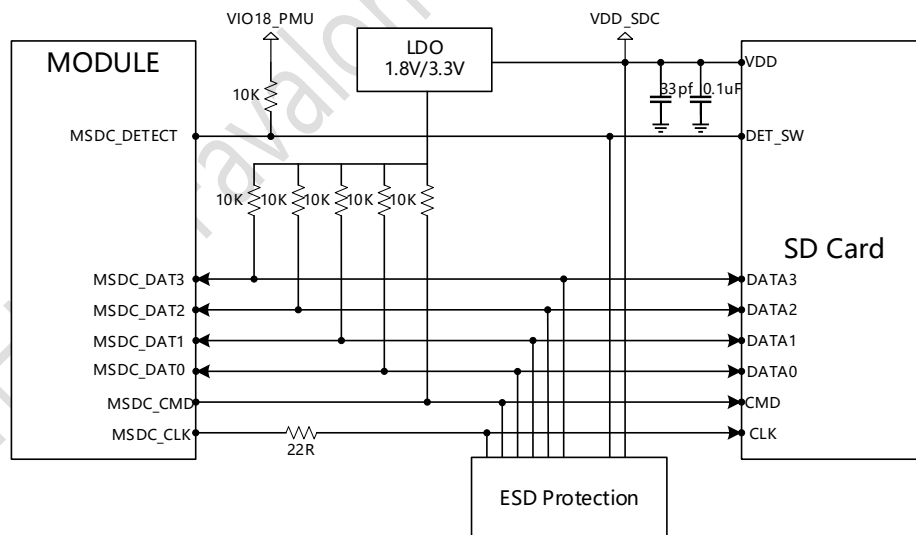


Figure 3-14 MSDC interface circuit reference design

Design considerations:

- 1) VDD_SDC is the SD card peripheral drive power supply, at least 800mA current flow capacity, trace width 1 mm.
- 2) Pull up hot plug detection signal to VIO18_PMU power supply.
- 3) MSDC is a high-speed digital signal line, which needs three-dimensional grounding and equal length

processing when routing.

- 4) When external SD card is connected, TVS tube shall be added to each interface of SDIO, and the junction capacitance shall not exceed 1pF.
- 5) When MSDC is not in use, MSDC_DETECT is pulled up to VIO18_PMU and DAT/CLK/CMD is suspended.
- 6) MSDC traces must be well protected and kept away from RF/WIFI/BT/GNSS or other RF functional signals on the previous layer, the same layer, or the next layer.
- 7) MSDC traces shall be separated by the real ground plane connected to the main ground plane. MSDC traces must be routed on the inner PCB layer to be shielded by completely connected to the ground.
- 8) The MSDC signal must be connected directly from the host to the device, and no trace branching on the MSDC signal trace is allowed.
- 9) MSDC VMCH may cause two voltage steps when slowly unplugging the device and quickly closing the VMCH.

3.8 I2S Interface

The AN762S-GL series module has 6 sets of I2S interfaces, one of which can be configured as master-slave mode. In master mode, the sampling frequency can support up to 384KHz, I2S4 can be multiplexed into TDM, and Bit clock can support up to 12.288MHz.

Table 3-14 I2S interface pin definition

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
I2S0_MCLK	AA20	DO	I2S0 main clock	1.8V	--
I2S0_BCK	CD30	DO	I2S0 bit clock	1.8V	--
I2S0_LRCK	CD29	DO	I2S0 frame synchronization signal	1.8V	--
I2S0_DI	CE28	DI	I2S0 serial data input	1.8V	--
I2S0_DO	CE27	DO	I2S0 serial data output	1.8V	--
I2S1_MCLK	AB20	DO	I2S1 main clock	1.8V	--
I2S1_BCK	CC25	DO	I2S1 bit clock	1.8V	--
I2S1_LRCK	CD25	DO	I2S1 frame synchronization signal	1.8V	--
I2S1_DI	CD24	DI	I2S1 serial data input	1.8V	--
I2S1_DO	CD23	DO	I2S1 serial data output	1.8V	--
I2S2_BCK	BF10	DO	I2S2 bit clock	1.8V	--
I2S2_LRCK	BH12	DO	I2S2 frame synchronization signal	1.8V	--
I2S2_DI	BH11	DI	I2S2 serial data input	1.8V	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
I2S2_DO	BF11	DO	I2S2 serial data output	1.8V	--
I2S3_MCLK	CF27	DO	I2S3 main clock	1.8V	--
I2S3_BCK	CF28	DO	I2S3 bit clock	1.8V	--
I2S3_LRCK	CH25	DO	I2S3 frame synchronization signal	1.8V	--
I2S3_DI	CG27	DI	I2S3 serial data input	1.8V	--
I2S4_BCK0	CA28	DI	I2S4 bit clock	1.8V	Supports I2S and TDM mode inputs, default I2S mode
I2S4_LRCK0	CC28	DI	I2S4 frame synchronization signal	1.8V	Supports I2S and TDM mode inputs, default I2S mode
I2S4_DO0	CC26	DO	I2S4 serial data output Data0	1.8V	Supports I2S and TDM mode inputs, default I2S mode
I2S4_DO1	CE25	DO	I2S4 serial data output Data1	1.8V	Supports I2S and TDM mode inputs, default I2S mode
I2S4_DI0	CD27	DI	I2S4 serial data input Data0	1.8V	Supports I2S and TDM mode inputs, default I2S mode
I2S4_DI1	CC27	DI	I2S4 serial data input Data1	1.8V	--
I2S5_BCK	BG27	DO	I2S5 bit clock	1.8V	--
I2S5_LRCK	BH27	DO	I2S5 frame synchronization signal	1.8V	--
I2S5_DI	BG28	DI	I2S5 serial data input	1.8V	--
I2S5_DO	BH28	DO	I2S5 serial data output	1.8V	--

The voltage domain of each serial port is 1.8V; when communicating with serial ports in other voltage domains, it is necessary to add a level conversion chip. The reference circuit design is as follows:

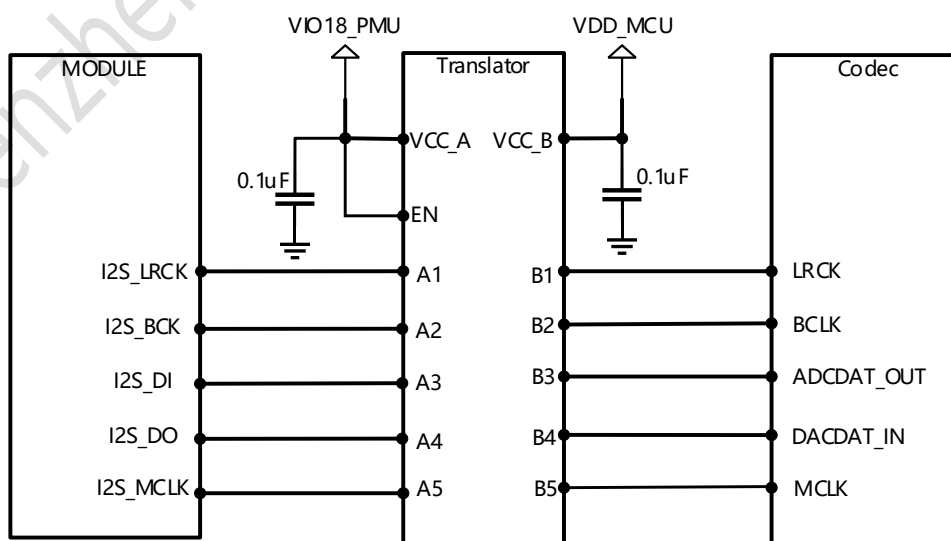


Figure 3-15 I2S interface circuit reference design

Design considerations:

- 1) Some CODEC chips do not need MCLK, they can be suspended.
- 2) It is recommended to reserve a series 0-ohm resistor to prevent the waveform from overshoot when debugging.
- 3) I2S signals are routed around the ground, away from sources of interference.

3.9 I2C Interface

The AN762S-GL module has fourteen I2C interfaces, which can be used for TP, camera, sensor, etc. Fourteen groups of I2C interfaces are all open-drain outputs, and need to be added with pull-up resistors to VIO18_PMU when in use. I2C interface pins are defined in the following table:

Table 3-15 I2C interface pin definition

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
I2C0_SCL	AD31	OD	I2C0 serial clock	1.8V	Do not pull up inside the module by default
I2C0_SDA	AD30	OD	I2C0 serial data	1.8V	Do not pull up inside the module by default
I2C1_SCL	BD5	OD	I2C1 serial clock	1.8V	Do not pull up inside the module by default
I2C1_SDA	BD6	OD	I2C1 serial data	1.8V	Do not pull up inside the module by default
I2C2_SCL	DG13	OD	I2C2 serial clock	1.8V	Do not pull up inside the module by default
I2C2_SDA	DH13	OD	I2C2 serial data	1.8V	Do not pull up inside the module by default
I2C3_SCL	CH15	OD	I2C3 serial clock	1.8V	Do not pull up inside the module by default
I2C3_SDA	CH16	OD	I2C3 serial data	1.8V	Do not pull up inside the module by default
I2C4_SCL	DF15	OD	I2C4 serial clock	1.8V	Do not pull up inside the module by default
I2C4_SDA	DF16	OD	I2C4 serial data	1.8V	Do not pull up inside the module by default
I2C5_SCL	CG18	OD	I2C5 serial clock	1.8V	Do not pull up inside the module by default
I2C5_SDA	CF18	OD	I2C5 serial data	1.8V	Do not pull up inside the module by default
I2C6_SCL	AD27	OD	I2C6 serial clock	1.8V	Do not pull up inside the module by default
I2C6_SDA	AE27	OD	I2C6 serial data	1.8V	Do not pull up inside the module by default
I2C7_SCL	AD28	OD	I2C7 serial clock	1.8V	Do not pull up inside the module by default

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
I2C7_SDA	AD29	OD	I2C7 serial data	1.8V	Do not pull up inside the module by default
I2C8_SCL	AE16	OD	I2C8 serial clock	1.8V	Do not pull up inside the module by default
I2C8_SDA	AE15	OD	I2C8 serial data	1.8V	Do not pull up inside the module by default
I2C9_SCL	AB18	OD	I2C9 serial clock	1.8V	Do not pull up inside the module by default
I2C9_SDA	AA18	OD	I2C9 serial data	1.8V	Do not pull up inside the module by default
I2C10_SCL	BH26	OD	I2C10 serial clock	1.8V	Do not pull up inside the module by default
I2C10_SDA	BG26	OD	I2C10 serial data	1.8V	Do not pull up inside the module by default
I2C11_SCL	DF9	OD	I2C11 serial clock	1.8V	Do not pull up inside the module by default
I2C11_SDA	DF10	OD	I2C11 serial data	1.8V	Do not pull up inside the module by default
I2C12_SCL	CE29	OD	I2C12 serial clock	1.8V	IMU dedicated
I2C12_SDA	CF29	OD	I2C12 serial data	1.8V	Do not pull up inside the module by default
I2C13_SCL	AF14	OD	I2C13 serial clock	1.8V	Do not pull up inside the module by default
I2C13_SDA	AF13	OD	I2C13 serial data	1.8V	

The circuit reference design is as follows:

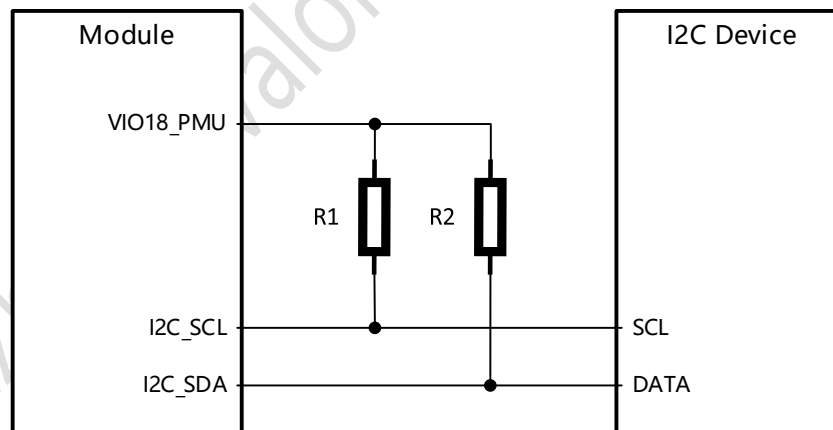


Figure 3-16 I2C interface circuit reference design

Design considerations:

- 1) Supports standard mode, fast mode, and high-speed mode.
- 2) When multiple groups of peripherals are mounted on an I2C group, ensure the uniqueness of each peripheral address. When mounting a peripheral with high real-time requirements, do not share I2C with other peripherals.
- 3) I2C requires external pull-up resistor to VIO18_PMU power network. As shown in Table 3-16, the

corresponding resistance value can be selected according to the speed.

Table 3-16 Pull-up resistance selection

Operating Mode	Maximum Transmission Rate	R1&R2	Parasitic Capacitance Limitation
Standard Mode (Sm)	100 kbps	4.7 k Ω	≤ 400 pF
Fast Mode (Fm)	400 kbps	2.2 k Ω	≤ 400 pF
High Speed Mode (Hs)	1.7 Mbps	2.2 k Ω	≤ 400 pF
High Speed Mode (Hs)	3.4 Mbps	2.2 k Ω	≤ 100 pF

3.10 ADC Interface

The AN762S-GL module has five ADC interfaces. The acquisition voltage ranges from 0.04V to 1.78V, step: 17.54mV. The pin definition is as follows:

Table 3-17 ADC pin definition

Pin Name	Pin No.	I/O	Pin Description	I/O Voltage	Remark
ADC1	DD8	AI	ADC input detection	--	Voltage range: 0.04V to 1.78V
ADC2	DF7	AI	ADC input detection	--	Voltage range: 0.04V to 1.78V
ADC3	DF8	AI	ADC input detection	--	Voltage range: 0.04V to 1.78V
ADC4	DC8	AI	ADC input detection	--	Voltage range: 0.04V to 1.78V
ADC5	DE7	AI	ADC input detection	--	Voltage range: 0.04V to 1.78V

The reference circuit design is as follows:

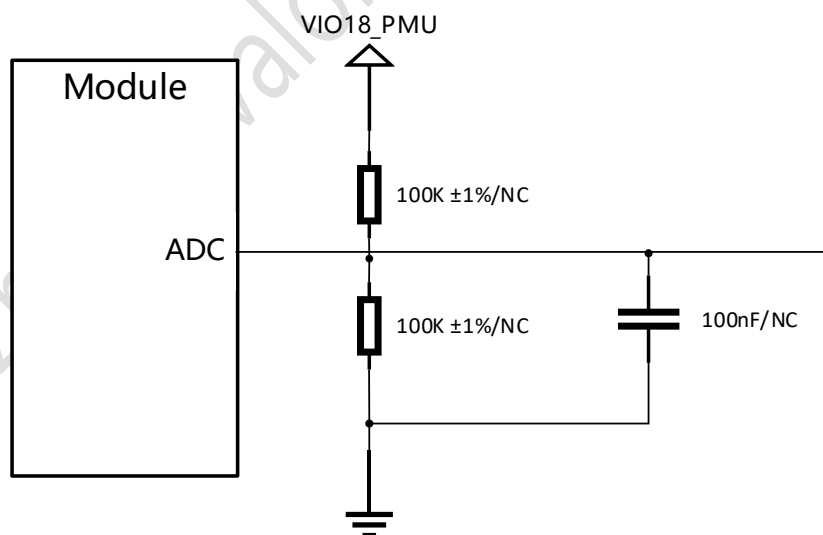


Figure 3-17 ADC interface circuit reference design

Design considerations:

- 1) Away from interference sources, and be routed around the ground.
- 2) It is recommended to reserve pull-up and pull-down resistors for ADC.

3.11 LCM Interface

The AN762S-GL module screen interface is based on the DSI D-PHY standard and supports two DSI D-PHY 4-Lane interfaces at speeds up to 2.5 Gbps/lane. DSI interface pins are defined in the following table:

Table 3-18 LCM pin definition

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
DSI0_CK0_M	CD13	AI/AO	DSI0 MIPI clock -	--	--
DSI0_CK0_P	CE13	AI/AO	DSI0 MIPI clock +	--	--
DSI0_D0_M	CD12	AI/AO	DSI0 MIPI data line 0-	--	--
DSI0_D0_P	CE12	AI/AO	DSI0 MIPI data line 0+	--	--
DSI0_D1_M	CD14	AI/AO	DSI0 MIPI data line 1-	--	--
DSI0_D1_P	CE14	AI/AO	DSI0 MIPI data line 1+	--	--
DSI0_D2_M	CD11	AI/AO	DSI0 MIPI data line 2-	--	--
DSI0_D2_P	CE11	AI/AO	DSI0 MIPI data line 2+	--	--
DSI0_D3_M	CD15	AI/AO	DSI0 MIPI data line 3-	--	--
DSI0_D3_P	CE15	AI/AO	DSI0 MIPI data line 3+	--	--
DSI1_CK0_M	CB20	AI/AO	DSI1 MIPI clock -	--	--
DSI1_CK0_P	CA20	AI/AO	DSI1 MIPI clock +	--	--
DSI1_D0_M	CB24	AI/AO	DSI1 MIPI data line 0-	--	--
DSI1_D0_P	CA24	AI/AO	DSI1 MIPI data line 0+	--	--
DSI1_D1_M	CB21	AI/AO	DSI1 MIPI data line 1-	--	--
DSI1_D1_P	CA21	AI/AO	DSI1 MIPI data line 1+	--	--
DSI1_D2_M	CB23	AI/AO	DSI1 MIPI data line 2-	--	--
DSI1_D2_P	CA23	AI/AO	DSI1 MIPI data line 2+	--	--
DSI1_D3_M	CB22	AI/AO	DSI1 MIPI data line 3-	--	--
DSI1_D3_P	CA22	AI/AO	DSI1 MIPI data line 3+	--	--

LCM interface circuit reference design is as follows:

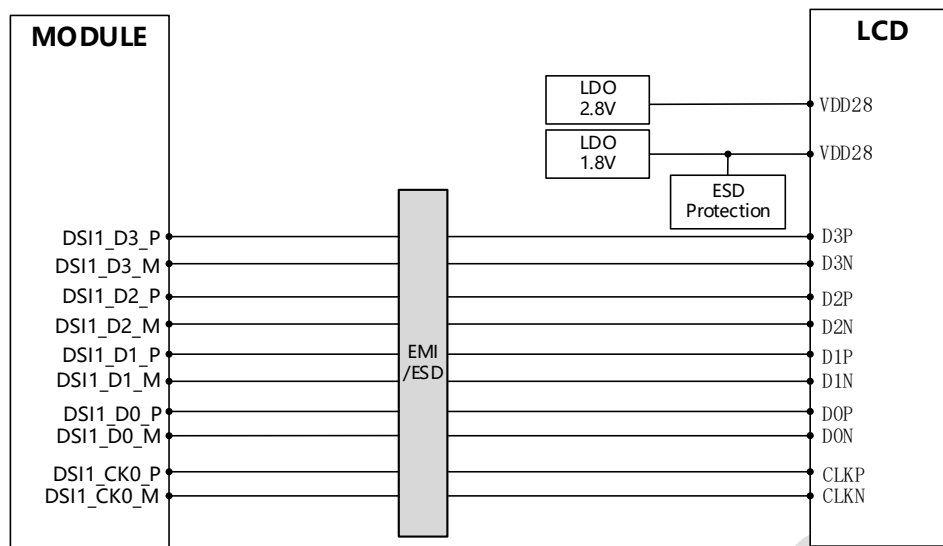


Figure 3-18 LCM interface circuit reference design

Design considerations:

- 1) MIPI is a high-speed signal line. It is recommended to connect a common-mode inductor in series near the LCD connector end to improve the electromagnetic radiation interference of the circuit.
- 2) MIPI routing is recommended to be placed in the inner layer, three-dimensional grounded, with differential impedance control of 100 ohms.
- 3) The total length of the wiring shall not exceed 4000 mils, the difference in the length of the differential line within the group shall be controlled within 25 mils, and the difference in the length between the groups shall be controlled within 100 mils.
- 4) It is recommended that the spacing within a group of differential lines be 1.5 times the line width, and that the spacing between differential lines and other traces be maintained at 3 times the line width.
- 5) The total device parasitic capacitance on the MIPI differential signal lines must not exceed 2pF.
- 6) Ground signals are inserted between differential pairs to improve cross coupling between groups.

3.12 Camera Interface

The AN762S-GL module video input interface is based on the MIPI_CSI standard and supports 6 CSI D-PHY 4-Lane interfaces at a maximum speed of 6.5 Gbps/lane. CSI interface pins are defined in the following table:

Table 3-19 Camera interface pin definition

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
MIPI_CSI0_CLK_M	AB14	AO	Camera 0 MIPI clock -	--	--
MIPI_CSI0_CLK_P	AA14	AO	Camera 0 MIPI clock +	--	--
MIPI_CSI0_L0_M	AB13	AI/AO	Camera 0 MIPI data line 0-	--	--
MIPI_CSI0_L0_P	AA13	AI/AO	Camera 0 MIPI data line 0 +	--	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
MIPI_CSI0_L1_M	AB15	AI/AO	Camera 0 MIPI data line 1-	--	--
MIPI_CSI0_L1_P	AA15	AI/AO	Camera 0 MIPI data line 1+	--	--
MIPI_CSI0_L2_M	AB12	AI/AO	Camera 0 MIPI data line 2-	--	--
MIPI_CSI0_L2_P	AA12	AI/AO	Camera 0 MIPI data line 2+	--	--
MIPI_CSI0_L3_M	AB16	AI/AO	Camera 0 MIPI data line 3-	--	--
MIPI_CSI0_L3_P	AA16	AI/AO	Camera 0 MIPI data line 3+	--	--
MIPI_CSI1_CLK_M	DA27	AO	Camera 1 MIPI clock -	--	--
MIPI_CSI1_CLK_P	DB27	AO	Camera 1 MIPI clock +	--	--
MIPI_CSI1_L0_M	DA26	AI/AO	Camera 1 MIPI data line 0-	--	--
MIPI_CSI1_L0_P	DB26	AI/AO	Camera 1 MIPI data line 0+	--	--
MIPI_CSI1_L1_M	DA28	AI/AO	Camera 1 MIPI data line 1-	--	--
MIPI_CSI1_L1_P	DB28	AI/AO	Camera 1 MIPI data line 1+	--	--
MIPI_CSI1_L2_M	DA25	AI/AO	Camera 1 MIPI data line 2-	--	--
MIPI_CSI1_L2_P	DB25	AI/AO	Camera 1 MIPI data line 2+	--	--
MIPI_CSI1_L3_M	DA29	AI/AO	Camera 1 MIPI data line 3-	--	--
MIPI_CSI1_L3_P	DB29	AI/AO	Camera 1 MIPI data line 3+	--	--
MIPI_CSI2_CLK_M	DA21	AO	Camera 2 MIPI clock -	--	--
MIPI_CSI2_CLK_P	DB21	AO	Camera 2 MIPI clock +	--	--
MIPI_CSI2_L0_M	DA20	AI/AO	Camera 2 MIPI data line 0-	--	--
MIPI_CSI2_L0_P	DB20	AI/AO	Camera 2 MIPI data line 0+	--	--
MIPI_CSI2_L1_M	DA22	AI/AO	Camera 2 MIPI data line 1-	--	--
MIPI_CSI2_L1_P	DB22	AI/AO	Camera 2 MIPI data line 1+	--	--
MIPI_CSI2_L2_M	DA19	AI/AO	Camera 2 MIPI data line 2-	--	--
MIPI_CSI2_L2_P	DB19	AI/AO	Camera 2 MIPI data line 2+	--	--
MIPI_CSI2_L3_M	DA23	AI/AO	Camera 2 MIPI data line 3-	--	--
MIPI_CSI2_L3_P	DB23	AI/AO	Camera 2 MIPI data line 3+	--	--
MIPI_CSI3_CLK_M	AB8	AO	Camera 3 MIPI clock -	--	--
MIPI_CSI3_CLK_P	AA8	AO	Camera 3 MIPI clock +	--	--
MIPI_CSI3_L0_M	AB7	AI/AO	Camera 3 MIPI data line 0-	--	--
MIPI_CSI3_L0_P	AA7	AI/AO	Camera 3 MIPI data line 0+	--	--
MIPI_CSI3_L1_M	AB9	AI/AO	Camera 3 MIPI data line 1-	--	--
MIPI_CSI3_L1_P	AA9	AI/AO	Camera 3 MIPI data line 1+	--	--
MIPI_CSI3_L2_M	AB6	AI/AO	Camera 3 MIPI data line 2-	--	--
MIPI_CSI3_L2_P	AA6	AI/AO	Camera 3 MIPI data line 2+	--	--
MIPI_CSI3_L3_M	AB10	AI/AO	Camera 3 MIPI data line 3-	--	--
MIPI_CSI3_L3_P	AA10	AI/AO	Camera 3 MIPI data line 3+	--	--
MIPI_CSI4_CLK_M	DA15	AO	Camera 4 MIPI clock -	--	--
MIPI_CSI4_CLK_P	DB15	AO	Camera 4 MIPI clock +	--	--
MIPI_CSI4_L0_M	DA14	AI/AO	Camera 4 MIPI data line 0-	--	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
MIPI_CSI4_L0_P	DB14	AI/AO	Camera 4 MIPI data line 0+	--	--
MIPI_CSI4_L1_M	DA16	AI/AO	Camera 4 MIPI data line 1-	--	--
MIPI_CSI4_L1_P	DB16	AI/AO	Camera 4 MIPI data line 1+	--	--
MIPI_CSI4_L2_M	DA13	AI/AO	Camera 4 MIPI data line 2-	--	--
MIPI_CSI4_L2_P	DB13	AI/AO	Camera 4 MIPI data line 2+	--	--
MIPI_CSI4_L3_M	DA17	AI/AO	Camera 4 MIPI data line 3-	--	--
MIPI_CSI4_L3_P	DB17	AI/AO	Camera 4 MIPI data line 3+	--	--
MIPI_CSI5_CLK_M	DB33	AO	Camera 5 MIPI clock -	--	--
MIPI_CSI5_CLK_P	DA33	AO	Camera 5 MIPI clock +	--	--
MIPI_CSI5_L0_M	DB32	AI/AO	Camera 5 MIPI data line 0-	--	--
MIPI_CSI5_L0_P	DA32	AI/AO	Camera 5 MIPI data line 0+	--	--
MIPI_CSI5_L1_M	AB3	AI/AO	Camera 5 MIPI data line 1-	--	--
MIPI_CSI5_L1_P	AA3	AI/AO	Camera 5 MIPI data line 1+	--	--
MIPI_CSI5_L2_M	DB31	AI/AO	Camera 5 MIPI data line 2-	--	--
MIPI_CSI5_L2_P	DA31	AI/AO	Camera 5 MIPI data line 2+	--	--
MIPI_CSI5_L3_M	AB4	AI/AO	Camera 5 MIPI data line 3-	--	--
MIPI_CSI5_L3_P	AA4	AI/AO	Camera 5 MIPI data line 3+	--	--

The camera circuit reference design is as follows:

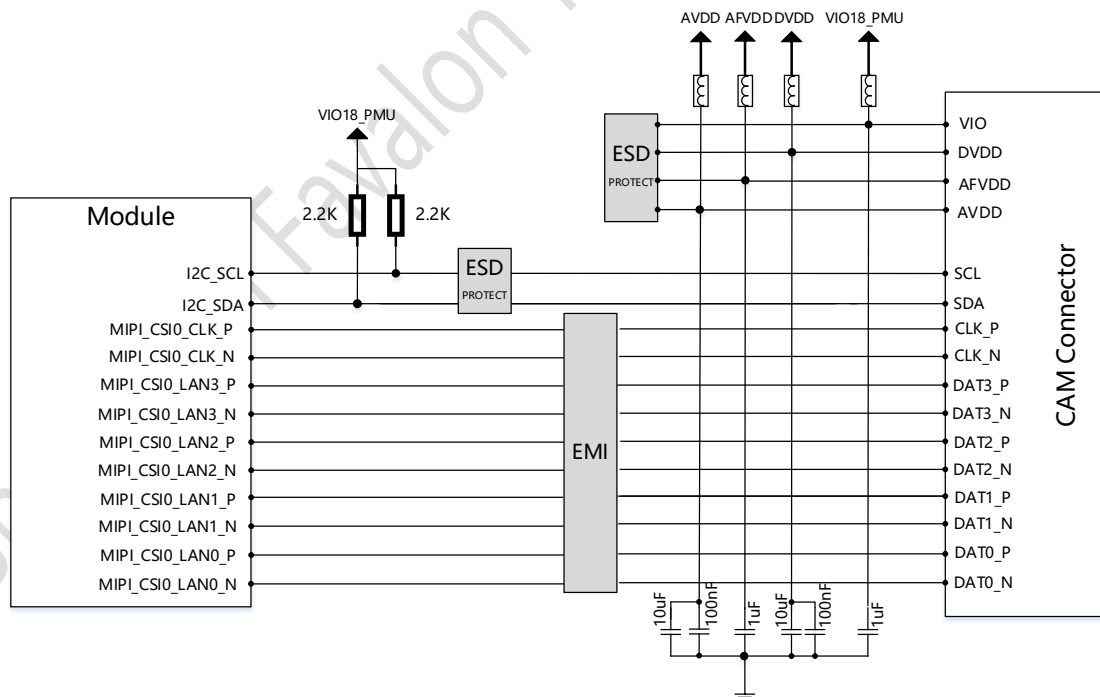


Figure 3-19 Camera interface circuit reference design

Design considerations:

- 1) MIPI is a high-speed signal line, it is recommended to connect a common mode inductor in series near the

camera connector end to reduce EMI.

- 2) MIPI wiring is recommended to be placed in the inner layer, three-dimensional grounded. MIPI signal line requires differential impedance control of 100 ohms.
- 3) The total length of traces shall not exceed 2300 mils, the length difference of differential lines within a group shall be controlled within 6 mils, and the length difference between groups shall be controlled within 100 mils.
- 4) It is recommended that the spacing within the differential line group be 1.5 times the line width, and the spacing between the differential line and other traces be 3 times the line width.
- 5) Total device parasitic capacitance on the MIPI differential signal lines must not exceed 0.5pF.
- 6) If the front and rear cameras share I2C, it is necessary to confirm that the I2C addresses of the two cameras do not conflict.
- 7) Analog voltage AVDD is recommended with LDOs with high PSRR and routed away from interference sources to avoid introducing power supply noise.
- 8) TVS tubes are added to the power supply and control signals to prevent ESD damage.

3.13 PCIe Interface

The module provides a set of 1-lane Gen3.0 PCIe interface. The pin definition is as follows.

Table 3-20 PCIe interface pin definition

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
PCIE0_CLKREQ	CF30	DI/DO	PCIe clock request signal	1.8V	--
PCIE0_RST	DG8	DI/DO	PCIe reset signal	1.8V	--
PCIE0_WAKE	DG7	DI/DO	PCIe wakeup signal	1.8V	--
PCIE0_CLK_M	AA24	AO	PCIe clock signal -	--	--
PCIE0_CLK_P	AB24	AO	PCIe clock signal +	--	--
PCIE0_RX0_M	AA23	AI	PCIe data reception -	--	--
PCIE0_RX0_P	AB23	AI	PCIe data reception +	--	--
PCIE0_TX0_M	AA22	AO	PCIe data transmission -	--	--
PCIE0_TX0_P	AB22	AO	PCIe data transmission +	--	--

The circuit reference design is as follows:

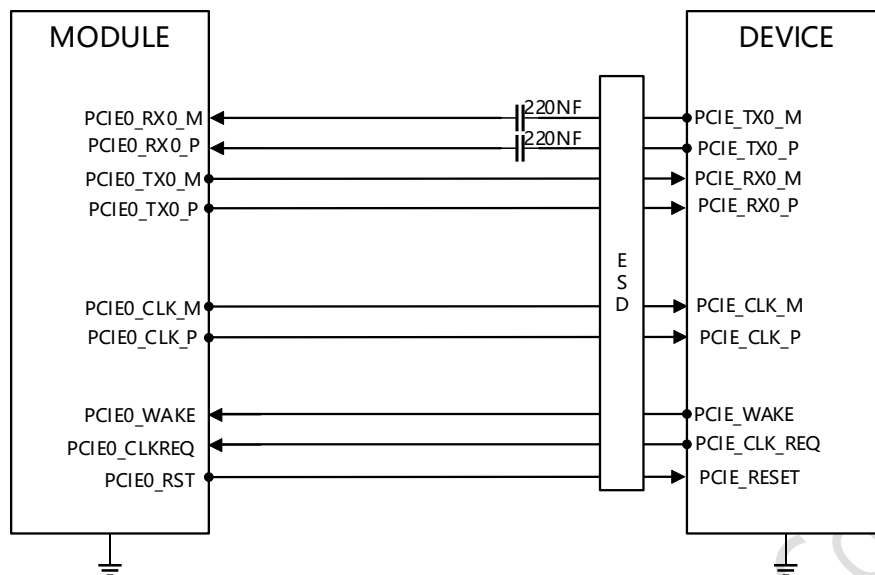


Figure 3-20 PCIe interface circuit reference design

Design considerations:

- 1) PCIe is a high-speed signal line, three-dimensional grounded when routing, equal length, follow the principle of high-speed differential routing principles, with differential impedance control of 85 ohms.
- 2) A 42.5-ohm impedance matching to ground needs to be reserved for the PCIE_CLK signal.
- 3) The total length of the routing shall not exceed 10000 mils, the difference in the length of the differential line within the group shall be controlled within 5 mils, and the difference in the length between the groups shall be controlled within 40 mils.
- 4) The parasitic capacitance of the TVS device must be less than 0.5pF.
- 5) The DC-blocking capacitor needs to be placed close to the transmitting end.

3.14 GPIO

The AN762S-GL module has rich GPIO resources, the interface level is 1.8V, and the pin definition is as follows:

Table 3-21 GPIO list

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
GPS_PPS	BE10	DO	GPS_PPS synchronization signal	1.8V	--
GPIO_0	AE23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_1	AE24	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_2	AE25	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_3	AD25	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to DP_HPD DP

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
					hot-plugging signal
GPIO_4	AH23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_5	AG14	DO	General input/output interface	1.8V	--
GPIO_6	BG15	DI/DO	General input/output interface	1.8V	--
GPIO_7	DF13	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_8	DF14	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_9	AH19	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_10	BH20	DI/DO	General input/output interface	1.8V	--
GPIO_11	AH15	DI/DO	General input/output interface	1.8V	--
GPIO_12	AG15	DI/DO	General input/output interface	1.8V	--
GPIO_13	BG7	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_14	AA19	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to SPI3_CS
GPIO_15	DF18	DI/DO	General input/output interface	1.8V	--
GPIO_16	CF24	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to SPI3_MI
GPIO_17	CF23	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to SPI3_MO
GPIO_18	CE23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_19	CH9	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_20	DF12	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_21	AE20	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_22	CG28	DI/DO	General input/output interface	1.8V	--
GPIO_23	AG17	DI/DO	General input/output interface	1.8V	--
GPIO_24	CE30	DI/DO	General input/output interface	1.8V	--
GPIO_25	CE31	DI/DO	General input/output interface	1.8V	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
GPIO_26	AD22	DI/DO	General input/output interface	1.8V	--
GPIO_27	DF11	DI/DO	General input/output interface	1.8V	--
GPIO_28	CG29	DI/DO	General input/output interface	1.8V	--
GPIO_29	DE27	DI/DO	General input/output interface	1.8V	--
GPIO_30	BH23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_31	BG23	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_32	AE13	DI/DO	General input/output interface	1.8V	--
GPIO_33	BE22	DI	General input/output interface	1.8V	● Interrupt input can be supported ● 100-ohm resistor in series is required
GPIO_34	BE23	DI	General input/output interface	1.8V	● Interrupt input can be supported ● 100-ohm resistor in series is required
GPIO_35	DF19	DI/DO	General input/output interface	1.8V	--
GPIO_36	DH27	DI/DO	General input/output interface	1.8V	--
GPIO_37	CG23	DI/DO	General input/output interface	1.8V	--
GPIO_38	CG22	DI/DO	General input/output interface	1.8V	--
GPIO_39	DD27	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_40	DH9	DI/DO	General input/output interface	1.8V	--
GPIO_41	DG10	DI/DO	General input/output interface	1.8V	--
GPIO_42	DD28	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_43	DD26	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_44	BG18	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_45	DC11	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_46	DH26	DI/DO	General input/output interface	1.8V	--
GPIO_47	DF6	DI/DO	General input/output interface	1.8V	--
GPIO_48	CE19	DI/DO	General input/output	1.8V	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
			interface		
GPIO_49	DC4	DO	General output interface	1.8V	--
GPIO_50	DD4	DO	General output interface	1.8V	--
GPIO_51	CH22	DO	General output interface	1.8V	--
GPIO_52	CD31	DO	General output interface	1.8V	--
GPIO_53	DC3	DO	General output interface	1.8V	--
GPIO_54	DA11	DO	General output interface	1.8V	--
GPIO_55	DB11	DO	General output interface	1.8V	--
GPIO_56	DA10	DO	General output interface	1.8V	--
GPIO_57	DH10	DI/DO	General input/output interface	1.8V	--
GPIO_58	CG25	DI/DO	General input/output interface	1.8V	--
GPIO_59	CE21	DI/DO	General input/output interface	1.8V	--
GPIO_60	AD24	DI/DO	General input/output interface	1.8V	--
GPIO_61	AG10	DI/DO	General input/output interface	1.8V	--
GPIO_62	DH22	DI/DO	General input/output interface	1.8V	--
GPIO_63	DH14	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_64	DG14	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_65	AF9	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_66	AE17	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_67	CG7	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_68	BH22	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_69	CH8	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_70	BD4	DO	General output interface	1.8V	Can be used for backup antenna switching control
GPIO_71	BH24	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_72	BG24	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_73	BG25	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_74	BH25	DI/DO	General input/output interface	1.8V	Interrupt input can be supported
GPIO_75	CD26	DI/DO	General input/output interface	1.8V	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
GPIO_76	CD28	DI/DO	General input/output interface	1.8V	--
GPIO_77	AD21	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to PWM0
GPIO_78	DH8	DI/DO	General input/output interface	1.8V	● Interrupt input can be supported ● Multiplexable to PWM1
GPIO_79	BH19	DI/DO	General input/output interface	1.8V	Multiplexable to PWM2
GPIO_80	DD17	DO	General output interface	1.8V	--
GPIO_81	DD15	DO	General output interface	1.8V	--
GPIO_100	AE5	DO	General output interface	1.8V	--
GPIO_101	AE6	DO	General output interface	1.8V	--
GPIO_102	AD4	DO	General output interface	1.8V	--
GPIO_103	DE29	DO	General output interface	1.8V	--
GPIO_104	DE18	DO	General output interface	1.8V	--
GPIO_105	DD14	DO	General output interface	1.8V	--
GPIO_106	DF22	DO	General output interface	1.8V	--
GPIO_107	DD16	DO	General output interface	1.8V	--
GPIO_108	DF21	DO	General output interface	1.8V	--
GPIO_109	DF23	DO	General output interface	1.8V	--
GPIO_110	CB28	DI/DO	General input/output interface	1.8V	--
GPIO_111	AF10	DI/DO	General input/output interface	1.8V	--
GPIO_112	CE26	DI/DO	General input/output interface	1.8V	--

3.15 DP Interface

The AN762S-GL module supports a set of DP 4-Lane interfaces, and supports DP1.4 compatible USB Type-C interfaces with a maximum speed of 8.1 Gbps/lane. The DP interface pin definition is listed in the following table:

Table 3-22 DP interface definition

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
DP_AUX_M	CB3	AI/AO	DP auxiliary channel -	--	--
DP_AUX_P	CA3	AI/AO	DP auxiliary channel +	--	--
DP_LN0_TX_M	CA5	AI/AO	DP transmission link LN0-	--	--
DP_LN0_TX_P	CB5	AI/AO	DP transmission link LN0+	--	--
DP_LN1_TX_M	CC4	AI/AO	DP transmission link LN1-	--	--

Pin Name	Pin No.	I/O	Description	I/O Voltage	Remark
DP_LN1_TX_P	CD4	AI/AO	DP transmission link LN1+	--	--
DP_HPD	AH22	DI	DP hot-plug signal	1.8V	Multiplexable to SPI3_CLK
USB0_SS_TX_M	CA6	AO	USB 3.0 differential data transmission -	--	● Multiplexing DP_LN2_TX_M ● Adaptive switching is not supported
USB0_SS_TX_P	CB6	AO	USB 3.0 differential data transmission +	--	● Multiplexing DP_LN2_TX_P ● Adaptive switching is not supported
USB0_SS_RX_M	CD5	AI	USB3.0 differential data reception -	--	● Multiplexing DP_LN3_TX_M ● Adaptive switching is not supported
USB0_SS_RX_P	CE5	AI	USB3.0 differential data reception +	--	● Multiplexing DP_LN3_TX_P ● Adaptive switching is not supported

The DP interface circuit reference design is as follows:

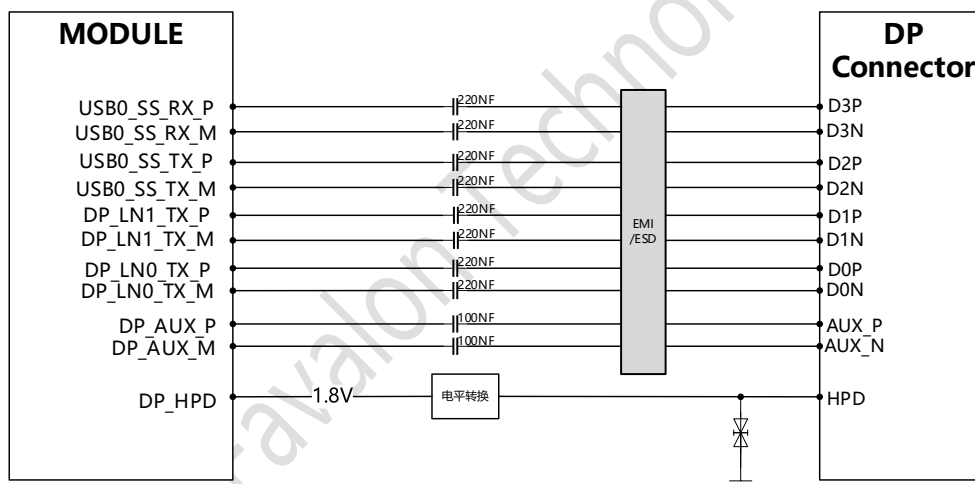


Figure 3-21 DP interface circuit reference design

Design considerations:

- 1) ESD device parasitic capacitance must be less than 0.2pF; DP/DN DC blocking capacitance is 0.22uF; AUX_P/N DC blocking capacitance is 0.1uF.
- 2) The voltage level of HPD signal is 1.8V, pay attention to level conversion and ESD protection.
- 3) AUX signal needs to add bias assistance at the slave end of the DC blocking capacitor to add 100K-ohm pull-up resistor in AUX_N/100K-ohm pull-down resistor in AUX_P respectively.
- 4) The error of equal length processing of differential signal lines is less than 5 mils, and the difference between pairs of lines is less than 30 mils; and the differential signal group requires grounding, DP/N signal and other signals must meet 6 times DP width.
- 5) The trace impedance should be controlled at 90 ohms $\pm$ 10%, and the number of vias should be less than 2.

- 6) The trace length from the module to the connector should be less than 4000 mils.

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4 Antenna Interface

4.1 MAIN/DRX Antenna

The AN762S_GL module provides four cellular antenna interfaces with different frequency bands and ranges.

Table 4-1 Antenna interface definition

Pin Name	Pin No.	I/O	Description	Remark
ANT1	BA6	I/O	MAIN	--
ANT2	BA10	I/O	DRX/AUX	--
ANT3	BA14	I/O	MIMO3	--
ANT4	BA18	I/O	MIMO4	--

Table 4-2 Band antenna assignments

BAND	TX	PRX	DRX	PRX_MIMO	DRX_MIMO
GSM850/GSM900/DCS1800/PCS1900	1	1	2	--	--
WCDMA B1/2/4/5/8	1	1	2	--	--
LTE B29/32 NR N29/75	--	1	2	--	--
LTE B5/8/12/13/14/17/20/26/28/40/71 NR N5/8/12/14/20/28/40/71	1	1	2	--	--
LTE B1/2/3/7/25/38/41/42/48/66 NR N1/2/3/7/25/38/41/48/66/77/78	1	1	2	3	4
Note: 1=ANT1 MAIN; 2=ANT2 DRX/AUX; 3=ANT3 MIMO3; 4=ANT4 MIMO4					

4.1.1 Operating Bands

Table 4-3 MT8676 operating bands

Band	Tx	Rx	Unit
GSM850	824 - 849	869 - 894	MHz
EGSM900	880 - 915	925 - 960	MHz
DCS1800	1710 - 1785	1805 - 1880	MHz
PCS1900	1850 - 1910	1930 - 1990	MHz
WCDMA B1	1920 - 1980	2110 - 2170	MHz
WCDMA B2	1850 - 1910	1930 - 1990	MHz
WCDMA B4	1710 - 1755	2110 - 2155	MHz
WCDMA B5	824 - 849	869 - 894	MHz
WCDMA B8	880 - 915	925 - 960	MHz
LTE-FDD B1	1920 - 1980	2110 - 2170	MHz

Band	Tx	Rx	Unit
LTE-FDD B2	1850 - 1910	1930 - 1990	MHz
LTE-FDD B3	1710 - 1785	1805 - 1880	MHz
LTE-FDD B4	1710 - 1755	2110 - 2155	MHz
LTE-FDD B5	824 - 849	869 - 894	MHz
LTE-FDD B7	2500 - 2570	2620 - 2690	MHz
LTE-FDD B8	880 - 915	925 - 960	MHz
LTE-FDD B12	699 - 716	729 - 746	MHz
LTE-FDD B13	777 - 787	748 - 756	MHz
LTE-FDD B14	788 - 798	758 - 768	MHz
LTE-FDD B17	704 - 716	734 - 746	MHz
LTE-FDD B20	832 - 862	791 - 821	MHz
LTE-FDD B25	1850 - 1915	1930 - 1995	MHz
LTE-FDD B26	814 - 849	859 - 894	MHz
LTE-FDD B28	703 - 748	758 - 803	MHz
LTE-FDD B29	N/A	717 - 728	MHz
LTE-FDD B32	N/A	1452 - 1496	MHz
LTE-TDD B38	2570 - 2620	2570 - 2620	MHz
LTE-TDD B40	2300 - 2400	2300 - 2400	MHz
LTE-TDD B41	2496 - 2690	2496 - 2690	MHz
LTE-TDD B42	3400 - 3599.9	3400 - 3599.9	MHz
LTE-TDD B48	3550 - 3700	3550 - 3700	MHz
LTE-FDD B66	1710 - 1780	2110 - 2200	MHz
LTE-FDD B71	663 - 698	617 - 652	MHz
5G NR n1	1920 - 1980	2110 - 2170	MHz
5G NR n2	1850 - 1910	1930 - 1990	MHz
5G NR n3	1710 - 1785	1805 - 1880	MHz
5G NR n5	824 - 849	869 - 894	MHz
5G NR n7	2500 - 2570	2620 - 2690	MHz
5G NR n8	880 - 915	925 - 960	MHz
5G NR n12	699 - 716	729 - 746	MHz
5G NR n14	788 - 798	758 - 768	MHz
5G NR n20	832 - 862	791 - 821	MHz
5G NR n25	1850 - 1915	1930 - 1995	MHz
5G NR n28	703 - 748	758 - 803	MHz
5G NR n29	N/A	717 - 728	MHz
5G NR n38	2570 - 2620	2570 - 2620	MHz
5G NR n40	2300 - 2400	2300 - 2400	MHz
5G NR n41	2496 - 2690	2496 - 2690	MHz
5G NR n48	3550 - 3700	3550 - 3700	MHz

Band	Tx	Rx	Unit
5G NR n66	1710 - 1780	2110 - 2200	MHz
5G NR n71	663 - 698	617 - 652	MHz
5G NR n75	N/A	1432-1517	MHz
5G NR n77	3300 - 4200	3300 - 4200	MHz
5G NR n78	3300 - 3800	3300 - 3800	MHz

4.1.2 Circuit Reference Design

When using the AN762S module, it is necessary to connect the antenna pins to the RF connector or antenna feed point on the motherboard through RF traces. It is recommended to use microstrip lines for the RF traces. The second layer should be hollowed out, with the third layer's GND as the reference, and the impedance should be controlled at 50Ω. A T-type circuit should be reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel devices should be directly connected across the RF traces without pulling out branches.

The reference circuit is shown in the following figure:

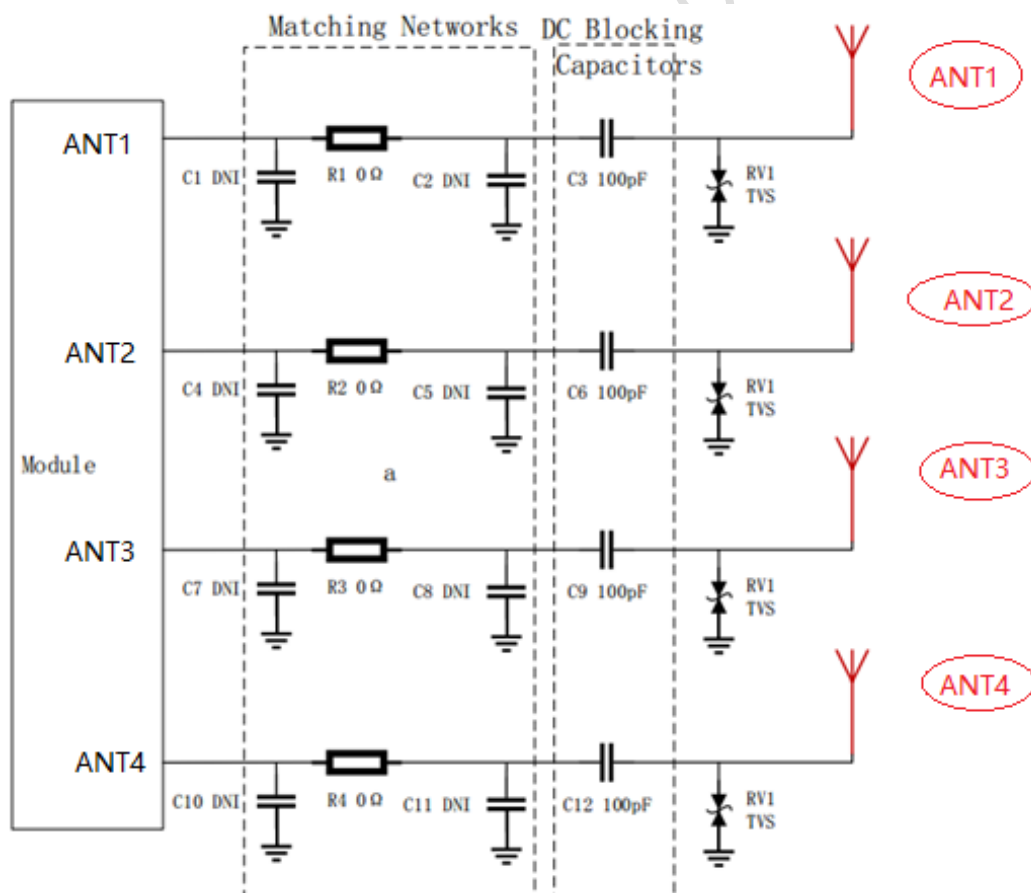


Figure 4-1 ANT antenna circuit design

4.2 WIFI/BT Antenna

For the RF traces of the WIFI/BT antennas, microstrip lines are recommended. The second layer should be hollowed out, with the third - layer GND as the reference, and the impedance should be controlled at 50Ω.

Table 4-4 WIFI/BT antenna interface definition

Pin Name	Pin No.	I/O	Description	Remark
ANT_WB0	BA30	I/O	WIFI_BT antenna interface	--
ANT_WB1	BA26	I/O	WIFI antenna interface	--

4.2.1 Operating Bands

Table 4-5 WIFI/BT operating bands

Mode	Frequency	Unit
WIFI	2412-2484	MHz
	5180-7125	MHz
BT5.3	2402-2480	MHz

4.2.2 Circuit Reference Design

The reference circuit is shown in the following figure:

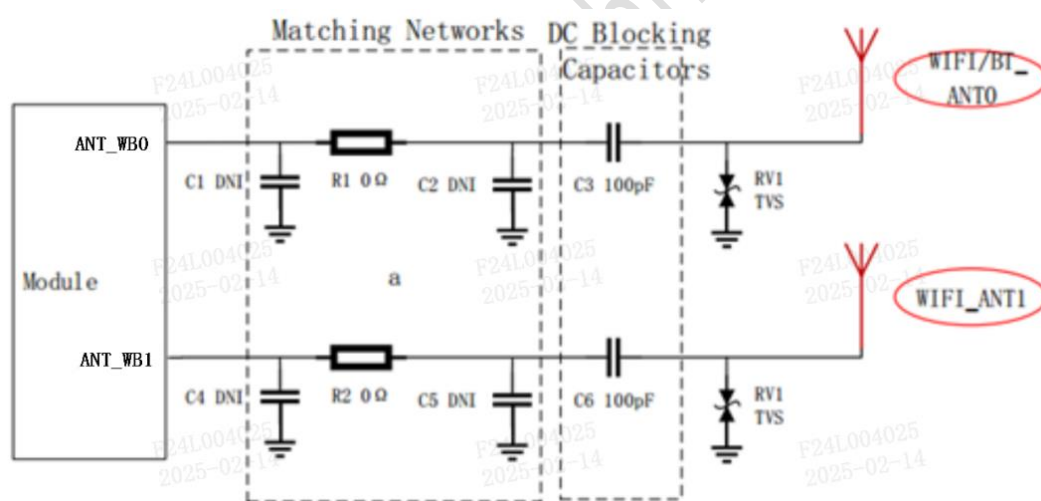


Figure 4-2 WIFI/BT reference circuit design

4.3 GNSS Antenna

GNSS supports GPS, GLONASS, Galileo, BeiDou, and QZSS.

Table 4-4 GNSS antenna interface definition

Pin Name	Pin No.	I/O	Description	Remark
GNSS_ANT	BA34	I/O	GNSS antenna	--

4.3.1 Operating Bands

Table 4-7 GNSS operating bands

Mode	Band	Bandwidth	Unit
GPS L1CA	1575.42	2.046	MHz
GLONASS R1	$1602 \pm 0.5625 * n, n = -7 \sim 6$	8.34	MHz
Galileo E1	1575.42	4.092	MHz
BeiDou B1C	1575.42	4.092	MHz
BeiDou B1I	1561.098	4.092	MHz
GPS L5/Galileo E5a/BeiDou B2a/QZSS	1176.45	20.46	MHz

4.3.2 Circuit Reference Design

The AN762S module has no built-in LNA, and active antennas are used in the design of the whole machine. Microstrip line is recommended for GNSS RF trace, with insertion loss control within 0.5dB, and impedance control within 50Ω. The connection reference circuit is shown in the following figure.

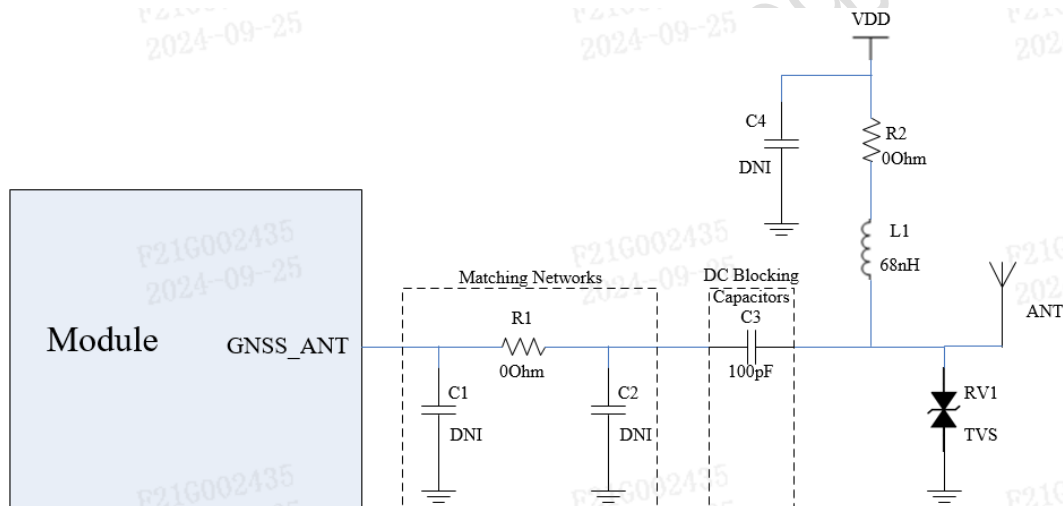


Figure 4-3 GNSS active antenna reference circuit design

The power supply for the active antenna is fed through the inductor L1 from the antenna's signal line. Commonly, active antennas are powered with a voltage ranging from 3.3V to 5.0V.

The active antenna itself consumes very little power, but it requires a stable and clean power supply. It is recommended to use a high - performance LDO to power the antenna. The recommended range for the total gain of the active antenna is [14:20] dB. If the gain is greater than 20 dB, a reserved π - type matching circuit should be used to add an attenuation network.

4.4 Antenna Requirements

The AN762S module provides six antenna interfaces: 5G, WIFI/BT, and GNSS, and the antenna requirements are shown in the following table:

Table 4-6 Antenna requirements

Type	Antenna Requirements
GSM/WCDMA/LTE/5G	VSWR: ≤ 2 Gain (dBi): 1 Maximum input power (W): 50 Input impedance (Ω): 50 Polarization type: Vertical Insertion loss: < 1dB (LB) Insertion loss: < 1.5dB (MB) Insertion loss: < 2dB (HB)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Maximum input power (W): 50 Input impedance (Ω): 50 Polarization type: Vertical Insertion loss: < 1dB
GNSS	Frequency range: 1559MHz to 1607MHz, 1166 MHz to 1187MHz Polarization type: right-handed circular polarization or linear polarization VSWR: < 2 (typical) Active antenna noise coefficient: < 1.5dB (typical) Active antenna gain: > -2dBi Active antenna built-in LNA gain range [14:24]dB

5 RF Signal Cable Layout

- The impedance of the RF signal line must be controlled at 50Ω , with reference to the projected layer. It is not recommended to perform coplanar impedance control.
- The RF signal line should have fewer vias, and the traces should be short, straight and flat. It should be surrounded by a three-dimensional ground, and the ground vias should be evenly distributed along the RF line.
- The RF line should be kept away from power sources and interfering signals.
- When the RF line is routed on the surface layer, it should avoid being routed under other components or modules.
- For the RF line coming out of the module, if it is routed on the surface layer, it should exit straightly and can only make a turn after leaving the module area. It should avoid routing on the surface layer within the projected area of the module.
- For the RF line coming out of the module, if it is routed on the surface layer, it is recommended that the line width be 0.3mm to 0.5mm. The clearance distance of the ground surrounding on the same layer is recommended to be $2W$. If there is no space, the minimum requirement is $1W$. The impedance control should be carried out according to the reference projected layer. If the line width of the adjacent layer used as a reference cannot meet the requirements, it is recommended to refer across layers, and the hollowed-out distance of the adjacent layer should be the same as that of the surface layer.
- The GND pins adjacent to the RF pins should not be made into thermal pads, and they should be in full contact with the ground.
- The RF signal line should avoid routing at right angles or acute angles. The recommended routing angle is 135° , and the angle should be an arc.
- The ground plane referenced by the RF signal line should be complete and well-connected to the main ground.

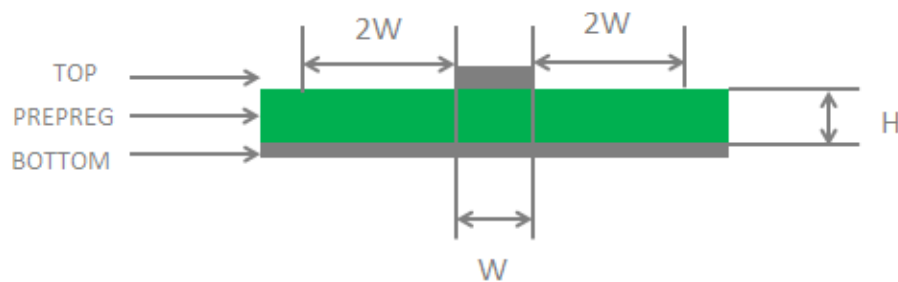


Figure 5-1 Reference adjacent layers

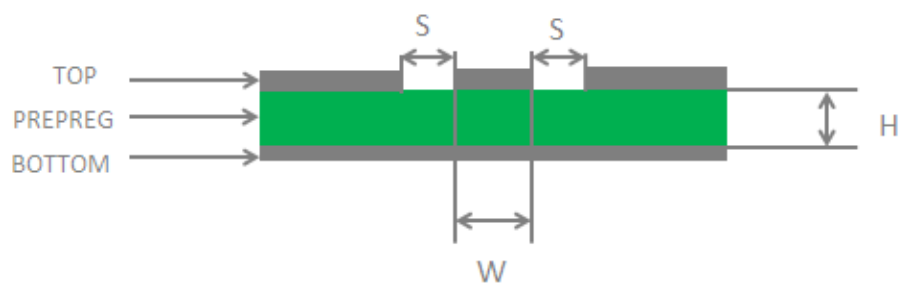


Figure 5-2 Cross-layer reference

6 WIFI and Bluetooth

6.1 WIFI Overview

The AN762S module supports 2.4G and 5G/6G WLAN wireless communication, supports 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac, and 802.11ax, and the highest rate can reach 2.8Gbps. Its characteristics are as follows:

- Supports WAPI
- Supports AP mode
- Supports Wi-Fi Direct
- Supports MCS 0-7 for HT20 and HT40
- Supports MCS 0-8 for VHT20
- Supports MCS 0-9 for VHT40, VHT80 and VHT160
- Supports MCS 0-11 for HE20, HE40, HE80 and HE160.

6.2 WIFI Performance Indicators

Test conditions: supply voltage 4.0V, ambient temperature 25°C.

Table 6-1 WIFI transmitting power

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	16±2dBm
		11Mbps	20	16±2dBm
	802.11g	6Mbps	20	14±2dBm
		54Mbps	20	13±2dBm
	802.11n	MCS0	20	14±2dBm
		MCS7	20	12.5±2dBm
		MCS0	40	14±2dBm
		MCS7	40	12±2dBm
	802.11ax	MCS0	20	14±2dBm
		MCS11	20	10±2dBm
		MCS0	40	14±2dBm
		MCS11	40	9.5±2dBm
5G	802.11a	6Mbs	20	12.5±2.5dBm
		54Mbps	20	11.5±2.5dBm
	802.11n	MCS0	20	12.5±2.5dBm
		MCS7	20	11±2.5dBm
		MCS0	40	11.5±2.5dBm

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
		MCS7	40	10±2.5dBm
		MCS0	20	12.5±2.5dBm
		MCS8	20	9±2.5dBm
		MCS0	40	11.5±2.5dBm
		MCS9	40	8.5±2.5dBm
		MCS0	80	11.5±2.5dBm
		MCS9	80	8.5±2.5dBm
		MCS0	160	9±2.5dBm
		MCS9	160	6±2.5dBm
	802.11ax	MCS0	20	12.5±2.5dBm
		MCS11	20	7±2.5dBm
		MCS0	40	11.5±2.5dBm
		MCS11	40	7±2.5dBm
		MCS0	80	11.5±2.5dBm
		MCS11	80	7±2.5dBm
		MCS0	160	9±2.5dBm
		MCS11	160	4.5±2.5dBm
6G	802.11ax	MCS0	20	10±2dBm
		MCS11	20	4.5±2.5dBm
		MCS0	40	9±2.5dBm
		MCS11	40	4.5±2.5dBm
		MCS0	80	9±2.5dBm
		MCS11	80	4.5±2.5dBm
		MCS0	160	6±2.5dBm
		MCS11	160	2.5±2.5dBm

Table 6-2 WIFI reception sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity(dBm) ²⁾
2.4G	802.11b	1Mbps	20	-97.6
		11Mbps	20	-89.8
	802.11g	6Mbps	20	-94.3
		54Mbps	20	-77.1
	802.11n	MCS0	20	-93.8
		MCS7	20	-75
		MCS0	40	-91.1
		MCS7	40	-72.3
	802.11ax	MCS0	20	-94.1
		MCS11	20	-64.3
		MCS0	40	-91.8

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity(dBm) ²⁾
		MCS11	40	-61.3
5G	802.11a	6Mbps	20	-92.3
		54Mbps	20	-74.5
	802.11n	MCS0	20	-91.2
		MCS7	20	-72.8
		MCS0	40	-88.8
		MCS7	40	-70.2
	802.11ac	MCS0	20	-91.3
		MCS8	20	-69.1
		MCS0	40	-89.3
		MCS9	40	-64.6
		MCS0	80	-86.3
		MCS9	80	-61.7
		MCS0	160	-82
		MCS9	160	-57
	802.11ax	MCS0	20	-91
		MCS11	20	-61.9
		MCS0	40	-89.4
		MCS11	40	-59
		MCS0	80	-86
		MCS11	80	-55.5
		MCS0	160	-82
		MCS11	160	-52
6G	802.11ax	MCS0	20	-92.5
		MCS11	20	-62
		MCS0	40	-89.5
		MCS11	40	-59.5
		MCS0	80	-87
		MCS11	80	-56
		MCS0	160	-85
		MCS11	160	-54



Note

1) Sensitivity is typical here.

6.3 Bluetooth Overview

The AN762S module supports BT5.3 (BR/EDR+BLE) specification, modulation mode supports GFSK, 8-DPSK and

$\pi/4$ -DQPSK. The BR/EDR channel bandwidth is 1MHz, which can accommodate 79 channels; The BLE channel bandwidth is 2MHz, which can accommodate 40 channels. Its main characteristics are as follows:

- BT5.3 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave, and page scanning)

Table 6-3 BT rate and version information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	70Kbit/s	--
BT2.0+EDR	3Mbit/s	2.1Mbit/s	--
BT3.0+HS	24Mbit/s	Refer to 3.0+HS	--
BT4.2 BLE	1Mbit/s	Refer to 4.2 BLE	--
BT5.3 BLE	2Mbit/s	Refer to 5.3	--

6.4 Bluetooth Performance Indicators

Test conditions: supply voltage 4.0V, ambient temperature 25°C.

Table 6-4 BT performance indicators

Type	DH-5	2-DH5	3-DH5	Unit
Transmitter	11±2	9±2.5	9±2.5	dBm
Sensitivity	-94	-94	-87	dBm

7 GNSS

7.1 Overview

The AN762S module supports GPS, GLONASS, Galileo, QZSS and Beidou positioning systems. There is no built-in LNA in the module. It is recommended to use an active antenna, which can effectively improve the sensitivity of GNSS.

7.2 Performance Indicators

Test conditions: supply voltage 4.0V, ambient temperature 25°C, test environment GNSS + LNA.

Table 7-1 GNSS positioning performance

Parameter	Description	Type Result	Unit
Sensitivity	Acquisition	-149	dBm
	Tracking	-161	dBm
C/N	-130dBm	43	dB-Hz
TTFF	Cold Start	31	s
	Hot Start	0.3	s
CEP	Static accuracy (95% @-130dbm)	1.5	m

i Note:

- 1) The testing environment is GNSS + LNA, and the test is carried out based on 6 GPS satellites. The gain coefficient of the LNA is 16dB.
- 2) The input requirement for the pins of the module is that the gain range is [16:20] dB, that is, the gain range of the customer's external LNA is [16:20] dB (between the antenna and the module). The gain range of [16:20] dB is being further confirmed on the MTK platform.

8 Electrical, Reliability and RF Performance

8.1 Recommended Parameters

Table 8-1 Recommended parameters

Parameter	Min	Normal	Max	Unit
VBAT	3.8	4.0	4.2	V
Operating Temperature	-40	25	85	°C
Storage Temperature	-40	25	95	°C

8.2 Operating Current

Test conditions: supply voltage 4.0V, ambient temperature 25°C.

Table 8-2 Operating current

Parameter	Description	Condition	Type	Unit
I _{off}	Power Off	Power Off	220	uA
I _{sleep}	Airplane	AIR1	TBD	mA

8.3 RF Transmitting Power

The transmitting power of AN762S module in each frequency band is shown in the following table:

Test conditions: supply voltage 4.0V, ambient temperature 25°C, LTE maximum power test 10M bandwidth 12RB.

Table 8-3 RF transmitting power

Standard	Band	3GPP Requirement	Max Power Typ.	Unit	Remark
GSM	GSM850	33+2/-2	33	dBm	--
	GSM900	33+2/-2	33	dBm	--
	DCS1800	30+2/-2	30	dBm	--
	PCS1900	30+2/-2	30	dBm	--
WCDMA	Band 1	24+1.7/-3.7	25	dBm	--
	Band 2	24+1.7/-3.7	25	dBm	--
	Band 4	24+1.7/-3.7	25	dBm	--
	Band 5	24+1.7/-3.7	25	dBm	--
	Band 8	24+1.7/-3.7	25	dBm	--
LTE FDD	Band 1	23±2.7	25	dBm	--
	Band 2	23±2.7	25	dBm	--
	Band 3	23±2.7	25	dBm	--
	Band 4	23±2.7	25	dBm	--

Standard	Band	3GPP Requirement	Max Power Typ.	Unit	Remark
	Band 5	23±2.7	25	dBm	--
	Band 7	23±2.7	25	dBm	--
	Band 8	23±2.7	25	dBm	--
	Band 12	23±2.7	25	dBm	--
	Band 13	23±2.7	25	dBm	--
	Band 14	23±2.7	25	dBm	--
	Band 17	23±2.7	25	dBm	--
	Band 20	23±2.7	25	dBm	--
	Band 25	23±2.7	25	dBm	--
	Band 26	23±2.7	25	dBm	--
	Band 28	23±2.7	25	dBm	--
	Band 66	23±2.7	25	dBm	--
	Band 71	23±2.7	25	dBm	--
	Band 38	23±2.7	25	dBm	--
	Band 40	23±2.7	25	dBm	--
	Band 41	23±2.7	25	dBm	--
	Band 42	23±2.7	25	dBm	--
	Band 48	23±2.7	25	dBm	--
5G NR	n1	23±2.7	25	dBm	--
	n2	23±2.7	25	dBm	--
	n3	23±2.7	25	dBm	--
	n5	23±2.7	25	dBm	--
	n7	23±2.7	25	dBm	--
	n8	23±2.7	25	dBm	--
	n12	23±2.7	25	dBm	--
	n14	23±2.7	25	dBm	--
	n20	23±2.7	25	dBm	--
	n25	23±2.7	25	dBm	--
	n28	23+2.7/-3.2	25	dBm	--
	n66	23±2.7	24	dBm	--
	n71	23+2.7/-3.2	24	dBm	--
	n38	23±2.7	25	dBm	--
	n40	23±2.7	25	dBm	--
	n48	23±2.7	25	dBm	--
	n41	26+2.7 /-3.7	26	dBm	--
	n77	26+3 /-4	26	dBm	--
	n78	26+3 /-4	26	dBm	--

8.4 Dual-Antenna RX Sensitivity

The sensitivity of each frequency band under dual-antenna of AN762 module is shown in the following table:

Test conditions: supply voltage 4.0V, ambient temperature 25°C, LTE sensitivity test bandwidth 10M. For RB configuration, reference to 3GPP.

Table 8-4 AN762S-GL module RF reception sensitivity

Standard	Band	3GPP Requirement	Rx Sensitivity Typ.	Unit	Remark
GSM	GSM850 (200K)	-102.4	-111	dBm	--
	GSM900 (200K)	-102.4	-112	dBm	--
	DCS1800 (200K)	-102.4	-112	dBm	--
	PCS1900 (200K)	-102.4	-112	dBm	--
WCDMA	Band 1 (5M)	-106.7	-114	dBm	--
	Band 2 (5M)	-104.7	-113.5	dBm	--
	Band 4 (5M)	-106.7	-114	dBm	--
	Band 5 (5M)	-104.7	-114	dBm	--
	Band 8 (5M)	-103.7	-114	dBm	--
LTE FDD	Band 1 (10M)	-96.3	-102	dBm	--
	Band 2 (10M)	-94.3	-102	dBm	--
	Band 3 (10M)	-93.3	-102	dBm	--
	Band 4 (10M)	-96.3	-102	dBm	--
	Band 5 (10M)	-94.3	-101	dBm	--
	Band 7 (10M)	-94.3	-100.5	dBm	--
	Band 8 (10M)	-93.3	-102	dBm	--
	Band 12 (10M)	-93.3	-101	dBm	--
	Band 13 (10M)	-93.3	-102	dBm	--
	Band 14 (10M)	-93.3	-102	dBm	--
	Band 17 (10M)	-93.3	-101	dBm	--
	Band 20 (10M)	-93.3	-102	dBm	--
	Band 25 (10M)	-92.8	-102	dBm	--
	Band 26 (10M)	-93.8	-101	dBm	--
	Band 28 (10M)	-94.8	-102	dBm	--
	Band 29 (10M)	-93.3	-101	dBm	--
	Band 32 (10M)	-93.3	-101	dBm	--
	Band 66 (10M)	-95.8	-101.5	dBm	--
	Band 71 (10M)	-93.5	-102	dBm	--
LTE TDD	Band 38 (10M)	-96.3	-100.5	dBm	--
	Band 40 (10M)	-96.3	-100.5	dBm	--
	Band 41 (10M)	-94.3	-100	dBm	--
	Band 42 (10M)	-95	-102	dBm	--
	Band 48 (10M)	-95	-102	dBm	--

Standard	Band	3GPP Requirement	Rx Sensitivity Typ.	Unit	Remark
NR	n1 (20M)	-93.1	-97.5	dBm	--
	n2 (20M)	-91.1	-97.5	dBm	--
	n3 (20M)	-90.1	-97.5	dBm	--
	n5 (20M)	-86.1	-98	dBm	--
	n7 (20M)	-91.1	-98	dBm	--
	n8 (20M)	-85.1	-98	dBm	--
	n12 (10M)	-83.3	-100.5	dBm	--
	n14 (10M)	-93.1	-101.5	dBm	--
	n20 (20M)	-89.1	-98	dBm	--
	n25 (20M)	-89.6	-99	dBm	--
	n28 (20M)	-90.1	-99	dBm	--
	n29 (10M)	-93.1	-100	dBm	--
	n38 (20M)	-90.0	-98	dBm	--
	n40 (20M)	-86.9	-97	dBm	--
	n41 (100M)	-84.0	-89	dBm	--
	n48 (20M)	-84.9	-100	dBm	--
	n66 (20M)	-92.6	-98.5	dBm	--
	n71 (20M)	-85.3	-99	dBm	--
	n75 (20M)	-84	-98	dBm	--
	n77 (100M)	-84.4	-91	dBm	--
	n78 (100M)	-84.9	-91.5	dBm	--

8.5 Four-Antenna RX Sensitivity

The AN762S module supports 4 x 4 MIMO in both the medium and high frequencies.

Table 8-5 AN762S-GL module RF reception sensitivity

Standard	Band	3GPP Requirement	Rx Sensitivity Typ.	Unit	Remark
LTE (10M)	Band 1 (10M)	-99	-105	dBm	--
	Band 2 (10M)	-97	-105	dBm	--
	Band 3 (10M)	-96	-105	dBm	--
	Band 4 (10M)	-99	-105	dBm	--
	Band 7 (10M)	-97	-104	dBm	--
	Band 25 (10M)	-95.5	-104	dBm	--
	Band 66 (10M)	-98.5	-104	dBm	--
	Band 38 (10M)	-97	-103	dBm	--
	Band 41 (10M)	-97	-102	dBm	--
	Band 42 (10M)	-97.2	-105	dBm	--
	Band 48 (10M)	-97	-105	dBm	--

Standard	Band	3GPP Requirement	Rx Sensitivity Typ.	Unit	Remark
5G NR	n1 (20M)	-95.8	-100.5	dBm	--
	n2 (20M)	-93.8	-100.5	dBm	--
	n3 (20M)	-92.8	-100.5	dBm	--
	n7 (20M)	-93.8	-101	dBm	--
	n25 (20M)	-93.8	-101	dBm	--
	n38 (20M)	-92.8	-100	dBm	--
	n41 (100M)	-86.8	-92	dBm	--
	n48 (20M)	-87.1	-103	dBm	--
	n66 (20M)	-95.3	-101	dBm	--
	n77 (100M)	-86.6	-94	dBm	--
	n78 (100M)	-87.1	-94.5	dBm	--

i Note:

1) Sensitivity is typical here.

8.6 Electrostatic Protection

In the module application, due to the human body static electricity, microelectronics between the charged friction and other static electricity, through a variety of ways to discharge to the module, may cause some damage to the module, so ESD protection should be taken seriously. In the process of research and development, production, assembly and testing, especially in product design, should take ESD protection measures. For example, in the circuit design of the interface and susceptible to electrostatic discharge damage or impact of the point, should increase the anti-static protection; production should wear anti-static gloves etc.

ESD performance parameters (temperature: 25 °C, humidity: 45% to 60%) as shown in the table below:

Table 8-6 ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
USB	±8	±15	KV
Antenna Interface	±8	±15	KV
USB Interface	±0.5	±1	KV

9 Structure Specifications

9.1 Product Appearance

The product appearance of the AN762S module is shown in the following figure:

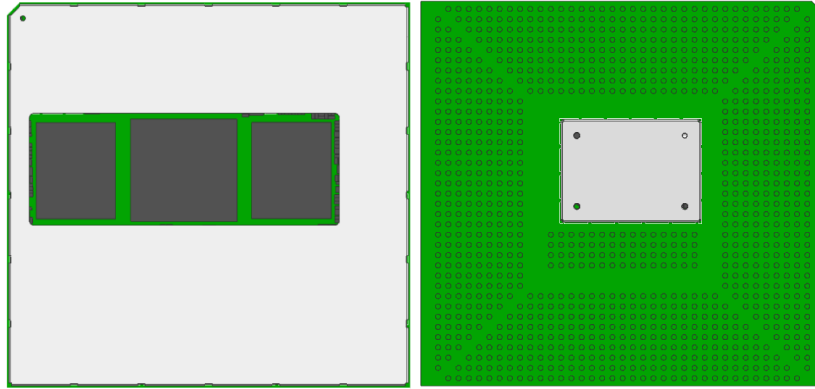


Figure 9-1 Product appearance

9.2 Structure Dimensions

The structure dimensions of the AN762S module are shown in the following figure:

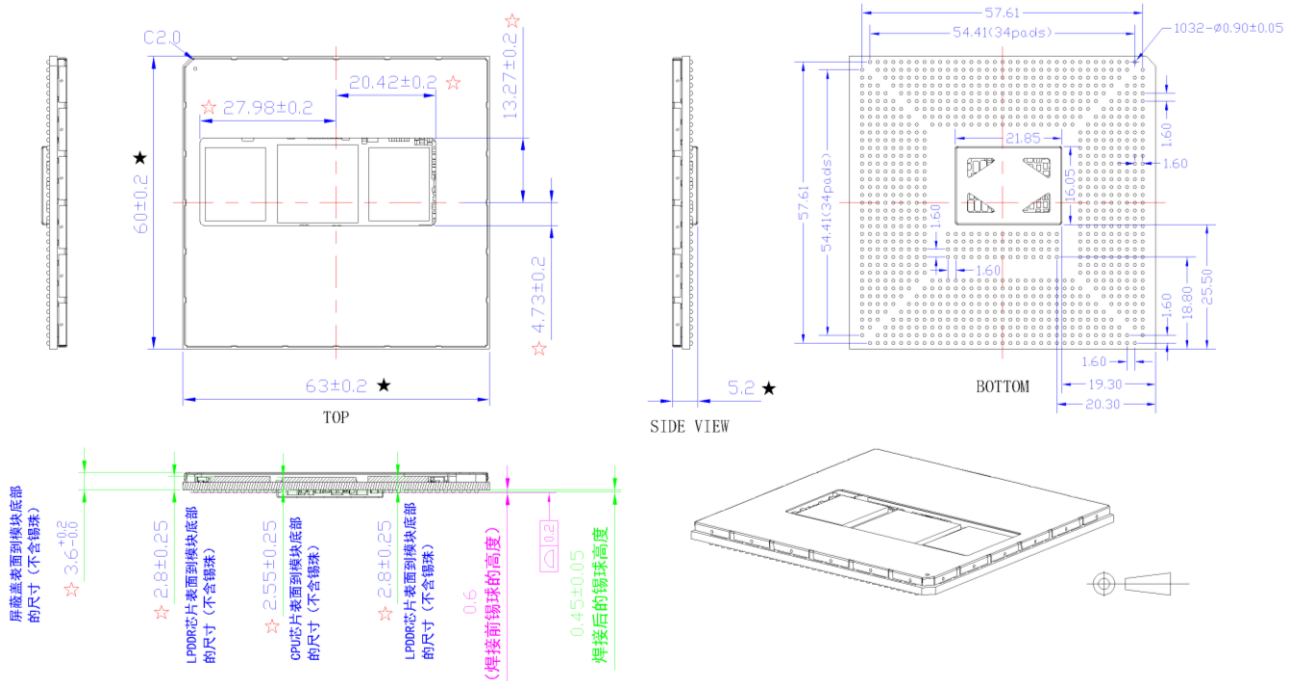


Figure 9-2 Structure dimensions

9.3 Recommended PCB Pad and Stencil Designs

Refer to "Favalon_AN762S_SMT Application Design Notes".

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10 Production and Storage

10.1 SMT Mounting

Refer to "Favalon_AN762S_SMT Application Design Notes".

10.2 Packaging and Storage

Refer to " Favalon_AN762S_ SMT Application Design Notes ".

Appendix A Abbreviations

Abbreviation	Full Name
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
I _{max}	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module

Abbreviation	Full Name
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Appendix B Operating Band and Frequency Range of 2G/3G/4G/5G NR Sub-6

Band	Mode	Tx (MHz)	Rx (MHz)
Band 1	NR/LTE FDD/WCDMA	1920 - 1980	2110 - 2170
Band 2	NR/LTE FDD/WCDMA	1850 - 1910	1930 - 1990
Band 3	NR/LTE FDD/WCDMA/GSM	1710 - 1785	1805 - 1880
Band 4	LTE FDD/WCDMA	1710 - 1755	2110 - 2155
Band 5	NR/LTE FDD/WCDMA/GSM	824 - 849	869 - 894
Band 7	LTE FDD	2500-2570	2620-2690
Band 8	NR/LTE FDD/WCDMA/GSM	880 - 915	925 - 960
Band11	LTE FDD	1427.9 – 1447.9	1475.9 - 1495.9
Band12	LTE FDD	699 - 716	729 - 746
Band13	LTE FDD	777 - 787	746 - 756
Band14	LTE FDD	788 - 798	758 - 768
Band17	LTE FDD	704 - 716	734 - 746
Band18	LTE FDD	815 - 830	860 - 875
Band19	LTE FDD/WCDMA	830 - 845	875 - 890
Band20	NR/LTE FDD	832 - 862	791- 821
Band21	LTE FDD	1447.9 - 1462.9	1495.9 - 1510.9
Band25	LTE FDD	1850 - 1915	1930 - 1995
Band26	LTE FDD	814 - 849	859 - 894
Band28	NR/LTE FDD	703 – 748	758 - 803
Band29	LTE FDD	NA	717 - 728
Band30	LTE FDD	2305 – 2315	2350 - 2360
Band32	LTE FDD	NA	1452 - 1496
Band 34	LTE TDD	2010-2025	2010-2025
Band 38	LTE TDD	2570- 2620	2570- 2620
Band 39	LTE TDD	1880 – 1920	1880 - 1920
Band 40	LTE TDD	2300 – 2400	2300 - 2400
Band 41	NR/LTE TDD	2496– 2690	2496– 2690
Band 42	LTE TDD	3400-3600	3400-3600
Band 47	LTE TDD	5855-5925	5855-5925
Band 48	LTE TDD	3550-3700	3550-3700
Band 66	NR/LTE FDD	1710– 1780	2110– 2200
Band 71	NR/LTE FDD	663– 698	617– 652
n77	NR	3300-4200	3300-4200

Band	Mode	Tx (MHz)	Rx (MHz)
n78	NR	3300-3800	3300-3800
n79	NR	4400-5000	4400-5000

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FCC regulatory compliance statement

§15.19 Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§15.21 Information to user

Warning: changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

- **List of applicable FCC rules:**

47 CFR Part 15.247, 15.407, 22, 24, 27, 90, 96

- **Summarize the specific operational use conditions**

This module can be used in IOT devices, the input voltage to the module is nominally DC 4V.

- **Limited module procedures**

This module is a single module.

- **Trace antenna designs**

The antenna is not a trace antenna.

- **RF exposure considerations**

This Module complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

- **Antennas**

If you desire to increase antenna gain and either change antenna type or use same antenna type certified, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

- **Label and compliance information**

Please notice that if the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains FCC ID: 2A8RBAN762SGL" any similar wording that expresses the same meaning may be used.

§ 15.19 Labelling requirements shall be complied on end user device.

Labelling rules for special device, please refer to §2.925, § 15.19 (a)(5) and relevant KDB publications. For E-label, please refer to §2.935.

- **Information on test modes and additional testing requirements**

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module.

The module is limited to installation in mobile application, a separate approval is required for all other operating configurations, including portable configurations with respect to §2.1093 and difference antenna configurations.

● FCC other Parts, Part 15B Compliance Requirements for Host product manufacturer

This modular transmitter is only FCC authorized for the specific rule parts listed on our grant, host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

Host manufacturer in any case shall ensure host product which is installed and operating with the module is in compliant with Part 15B requirements.

Please note that For a Class B or Class A digital device or peripheral, the instructions furnished the user manual of the end-user product shall include statement set out in §15.105 *Information to the user* or such similar statement and place it in a prominent location in the text of host product manual. Original texts as following:

For Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.*
- Increase the separation between the equipment and receiver.*
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- Consult the dealer or an experienced radio/TV technician for help.*

ISED Compliance Statements

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

- (1) This device may not cause interference.
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) L'appareil ne doit pas produire de brouillage;
- (2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Please notice that if the IC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains IC: 29662-AN762SGL" any similar wording that expresses the same meaning may be used.

L'étiquette d'homologation d'un module d'Innovation, Sciences et Développement économique Canada devra être posée sur le produit hôte à un endroit bien en vue, en tout temps. En l'absence d'étiquette, le produit hôte doit porter une étiquette sur laquelle figure le numéro d'homologation du module d'Innovation, Sciences et Développement économique Canada, précédé du mot « contient », ou d'une formulation similaire allant dans le même sens et qui va comme suit: Contient IC : 29662-AN762SGL est le numéro d'homologation du module.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal.

RF Exposure Compliance for FCC/IC ID

This equipment complies with FCC/IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This

equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations IC CNR-102 établies pour un environnement non contrôlé. Cet émetteur ne doit pas être colocalisé ou fonctionner en conjonction avec une autre antenne ou un autre émetteur. Cet équipement doit être installé et utilisé avec une distance minimale de 20cm entre le radiateur et votre corps.

RF Exposure Compliance for RED

The functions of Wireless Access Systems including Radio Local Area Networks(WAS/RLANs) within the band 5150-5350 MHz and 5945-6425MHz for this device are restricted to indoor use only within all European Union countries (BE/BG/CZ/DK/DE/EE/IE/EL/ES/FR/HR/IT/CY/LV/LT/LU/HU/MT/NL/AT/PL/PT/RO/SI/SK/FI/SE/TR/NO/CH/IS/LI/UK(N I)).

Indoor Client 6XD statement for FCC ID

1. FCC regulations restrict the operation of this device to indoor use only.
2. The device will only associate and connect with a low-power indoor access point or subordinate device and never directly connect to other client devices.
3. The device will always initiate transmission under the control of a low-power indoor AP or subordinate except for brief transmissions before joining a network. These short messages will only occur if the client has detected an indoor AP or subordinate operating on a channel. These brief messages will have a time-out mechanism such that if it does not receive a response from an AP it will not continually repeat the request.
4. transmissions will be lower or equal to the power advertised by the indoor low-power access point or subordinate and never above the maximum output power allowed by the FCC grant for equipment class 6XD.
5. Prohibited for control of or communications with unmanned aircraft systems, including drones.

Wi-Fi 6E Statement for IC ID:

Devices shall not be used for control of or communications with unmanned aircraft systems.

Low-power indoor access points and indoor subordinate devices shall bear statements acknowledging both of the following restrictions in the user manual and, where feasible, in a conspicuous location on the device.

Operation shall be limited to indoor use only.

Operation on oil platforms, automobiles, trains, maritime vessels and aircraft shall be prohibited except for on large aircraft flying above 3,048 m (10,000 ft).

L'équipement ne doit pas être utilisé pour le contrôle ou la communication des systèmes d'aéronefs sans pilote.

Les points d'accès intérieurs de faible puissance et les accessoires intérieurs doivent indiquer les restrictions suivantes dans le manuel de l'utilisateur et, si possible, à un endroit bien en vue de l'appareil: Le fonctionnement doit être limité à un usage intérieur. Il est interdit de travailler sur les plates - formes pétrolières, les voitures, les trains, les navires maritimes et les aéronefs, à l'exception des gros aéronefs de plus de 3 048 mètres (10 000 pieds).

Transmitters in the 5.925-7.125 GHz band are prohibited from operating to control or communicate with unmanned aircraft systems.