



Monarch 2 Platform

GM02S Module

Data Sheet



SEQUANS Communications
15-55 Boulevard Charles de Gaulle
F-92700 COLOMBES, France
☎ + 33 1 70 72 16 00
✉ contact@sequans.com
<https://www.sequans.com>

ABOUT THIS DATA SHEET

Purpose and Scope

The GM02S is a complete LTE Cat M1/NB1/NB2 module with baseband, RF and memory, targeted at narrow band low data rate M2M and IoT devices for wide deployment. This document provides technical information about GM02S LGA module. GM02S is based on Sequans's Monarch 2 platform.

Who Should Read this Document?

This document is intended for engineers who develop User Equipment (UE) for LTE systems.

Changes History

This is revision 22 of the GM02S data sheet, superseding version 21.

The signal list delivered as MS-Excel companion file to this data sheet is unchanged.

Table 1. Change history

Version	Date	Changes
22	March 2025	• New P/N GM02RBAQRN.
21	Feb. 2025	• Correction to HTOL temperature. • Remove band 71 from sensitivity table. • Align Environmental Conditions to those of the GC02S1. • New P/N GM02RBAQRO. • New Frequency Bands table. • Rewritten Regulatory Approval section.
20	Oct. 2024	• Reincorporate info about UART3 and associated GPIOs. • Add GM02S to SQN3430 GPIO cross-table. • Remove mention of PULSE0/PULSE1 pads as those are not made available by software. • Changes in the reflow profile in chapter 4.4 (Storage and Mounting).
19	July 2024	• New P/N GM02RBAQRM.
18	June 2024	• Add minimum rise time value for V_{BAT} • Change to marking and packing information to reflect multiple possible countries of origin. • Add various remarks on SPI operation. • Remove B71 (600 MHz) from the list of supported bands. • Precisions on RESETN voltage measurement. • Change the description of the UARTs' default configuration. • Add temperature measurement accuracy in the Thermal Consideration Section.

Table 1. Change history (continued)

Version	Date	Changes
17	Jan. 2024	• Remove all hardware v.2 information (EoL as per PCN 12001-23), GM02RBAQRI/Y. • New P/N GM02RBAQRL. • SIM_VCC output current is increased to 30 mA (instead of 2). • Added a timing diagram in the Power section, as well as a warning related to V_{BAT} levels and power-up slew-rate. • New section on MTTF calculation and figure.
16	Oct. 2023	• New P/N GM02RBAQRK. • Add info on water washing after reflow.
15	Sept. 2023	• Added ADC info. • Added new part numbers GM02RBAQRH and GM02RBAQRI. • Added OTP status for all part numbers. • Correction on pad #14. • Removed references to unusable UART3. • Add a mention that power consumption info is available elsewhere. • Added further info on pads' physical dimensions. • Add new certification information. • Add total capacitance and inductance figures. • Additional info on power modes. • Add a warning about configuring two UART as console.
14	Nov. 2022	• Add reliability figures for hardware v.3 (section 4.7). • Removed part numbers in headers in favour of hardware revisions. • New GM02RBAQRF P/N in Table 2 (hardware v.3). • Added weight of the GM02S hardware rev. 3.
13d	Oct. 2022	• New Part Number GM02RB6QRH in Table 2.
13c	Oct. 2022	• New 'change history' presentation. • Change THB information to 'PASS' in table 29 for hardware v.2.
13b	Aug. 2022	• Updated THB information for hardware v.2. in Table 30.
13a	Aug. 2022	• Harmonised Table 27 to gather information about hardware v.2 and v.3.

Table 1. Change history (continued)

Version	Date	Changes
13	July 2022	• Added information about new hardware v.3 in Section 1.1 Frequency Bands, Section 1.5 Available Part Numbers, Section 1.4 General Features, Section 4.1 Package Description and Section 4.3 Packing. • Created Chapter 6 Regulatory Approval for hardware v.3 (GM02RBAQRY).
12e	Dec. 2022	• New Part Number GM02RB6QRC in Table 2.
12d	Oct. 2022	• New Part Number GM02RB6QRH in Table 2.
12c	Oct. 2022	• New 'change history' presentation. • Change THB information to 'PASS' in table 29 for hardware v.2.
12b	Aug. 2022	• Updated THB information for hardware v.2. in Table 29.
12a	July 2022	• Removed band B.71 operation for hardware v.2 in Section Frequency Bands and Table 22.
12	May 2022	• Added information about LTE-M/NB-IoT dual mode operation in Chapter 1 General Description, Section 1.5 Available Part Numbers and Table 22. • Split Section 4.5 Regulatory Approval to accommodate NB-IoT operation.
11	March 2022	• Updated Section 4.3 Packaging Information. • Erratum to RESETN minimum value (100 ns → 100 μs) in Table 10.
10	Feb. 2022	• Updated Section 1.5 Available Part Numbers with new UE and LR versions updated and new marking codes. • Pad #71 changed to GND instead of DNC in Table 10. • Changes in Power-up Sequence in Section 3.1.2 Power-Up and Reset Sequences.
9	Dec. 2021	• Updated Table 2 in Section 1.5 Available Part Numbers. • Updated Section 4.2 Environmental Conditions. • Updated Section 4.5 Reliability Specification. • Additional RF information and recommendations. • Added Section 5.1.3 NCC Regulatory Approval. • Added performance at 2.2 V.

Table 1. Change history (continued)

Version	Date	Changes
8	Sept. 2021	• Updated Table 2 in Section 1.5 Available Part Numbers. • Updated Section 4.2 Environmental Conditions. • Updated Section 4.5 Reliability Specification.
7	Aug. 2021	• Updated Table 2 Available Part Numbers. • Updated wording related to CTS usage for flow control in Section 2.2 UART. • Updated Section 4.3 Packing with full cardbox's weight. • Added Section 4.5 Reliability Specification.
6	May 2021	• Updated Figure 11 in Section 4.1 Package Description.
5 ⁱ	April 2021	• Reorganised document. • Updated Table 2 Available Part Numbers. • Updated Section 3.1 Power. • Added Section 3.4 Power Supply Dimensioning. • Added Section 3.5 Maximum Electrical Ratings. • Updated Chapter 5 Regulatory Approval: added ACMA Regulatory Marking, JATE TELEC Regulatory Marking, RED Regulatory Safety Notice, UKCA Regulatory Marking. • Updated MS-Excel companion file with additional information.
4	March 2021	• Updated orderable status in Section 1.5 Part Numbers. • Updated Section 3.1.3 Power States. • Added Sections Detailed Behaviour of I/O Pads of BIDIR Type and Detailed Behaviour of I/O Pads of BIDIR_WAKE Type in Section 3.1 Power. • Updated Section 2.2 UART. • Updated Section 2.3 SIM0 Interface. • Updated Section 3.2 Digital I/O Characteristics. • Updated Section 4.1 Package Description. • Updated Section 4.2 Environmental Conditions. • Updated Section 4.4 Storage and Mounting. • Updated Section 5.1.1 FCC Regulatory Approval.
3	Dec. 2020	• Updated part numbers details in Table 1. • Added timing diagrams in Section 3.1 Power. • Added Section 3.1.3 Power States. • Added default Enable status for GPIOs in Section 2.7 GPIO. • Added RING0 polarity information in Table 2-13. • Restrict usage for pad #53 to Reserved. • Updated wake signals default enable state. • Updated V_{BAT} characteristics in Table 2-15. • Updated Section 4.3 Packing. • Added Sections FCC Regulatory Approval and Industry Canada Statement in Chapter 5 Regulatory Approval. • Changed assignment (from GND to DNC) for pads 71, 74, 75, 76, 77.

Table 1. Change history (continued)

Version	Date	Changes
2	Oct.2020	• Updated list of interfaces, added throughput figures in Chapter 2. • Updated Table 1. • Update power group descriptions in Chapter 2 Interfaces. • Updated Figure in Section 4.1 Package Description. • Added reflow profile information in Section 4.4 Storage and Mounting. • Removed humidity figures in document.
1	May 2020	First version.

i. Removed 'Preliminary' mention

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1. GENERAL DESCRIPTION

The Monarch 2 GM02S is an LTE Cat M1/NB1/NB2 module based on Sequans' second generation Monarch 2 chip platform. The GM02S is a total module solution, including a complete, Single-SKU™ RF front end capable of operating on every GSM band worldwide, and an integrated EAL5+ Secure Element (SE) capable of hosting the SIM inside the module with zero compromise on security while lowering cost and reducing complexity. The GM02S is part of Sequans next generation "S" family of modules, featuring a very small and cost-effective form factor that requires no external components.

The GM02S leverages Sequans's 15-plus years of experience in 4G+ technologies and incorporates Sequans's carrier-approved LTE protocol stack and a software suite amongst the most mature in the industry. The GM02S is part of Sequans's next generation "S" family of modules, featuring a very small and cost-effective form factor which requires no external components. The GM02S inherits Monarch's already certified LTE-M and NB-IoT stack and delivers a significantly improved performance and lower power consumption thanks to Sequans's second generation Monarch 2 chip and the new module architecture.

Sequans's technology, both hardware and software, is completely owned by Sequans, ensuring a fast time to market and the lowest total cost of ownership for device makers.

1.1. Frequency Bands

The GM02S supports the following bands:

Table 2. Bands supported by the GM02S, names and limits thereof.

Band	Name	Limits (MHz)
B1	IMT	1920 – 1980
B2	PCS	1850 – 1910
B3	DCS	1710 – 1785
B4	AWS-1	1710 – 1755
B5	Cellular	824 – 849
B8	Extended GSM 900	880 – 915 ⁱ
B12	Lower SMH	699 – 716
B13	Upper SMH	777 – 787
B14	Upper SMH	788 – 798
B17	Lower SMH	704 – 716
B18	Lower 800	815 – 830
B19	Upper 800	830 – 845
B20	800 Digital Dividend	832 – 862
B25	Extended PCS	1850 – 1915
B26	Extended Cellular	814 – 849
B28	APT	703 – 748
B66	Extended AWS	1710 – 1780
B85	Extended Lower SMH	698 – 716

i. In the USA this band is limited to 897.5 – 900.5 MHz.

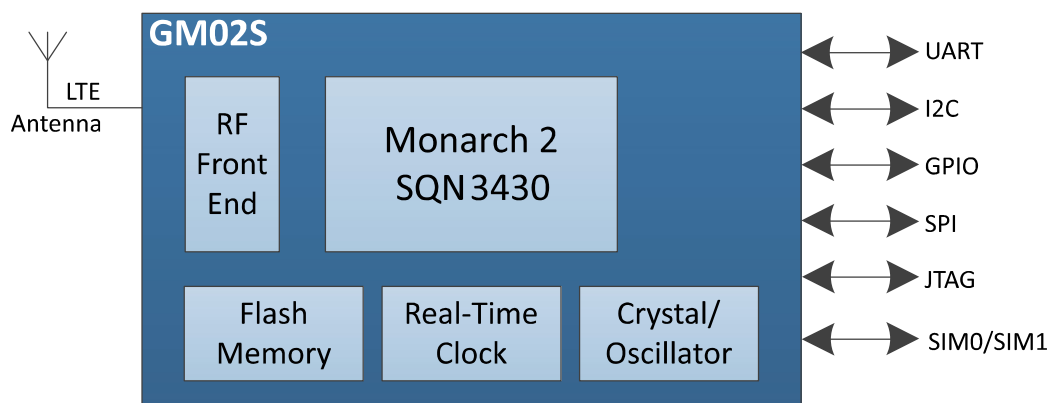
1.2. Applications

The GM02S is ideal for adding LTE-M and/or NB-IoT LTE connectivity to narrow band, low data rate M2M and IoT devices such as utility meters, industrial sensors, health and fitness appliances, asset trackers, and many additional devices in smart home, smart city, and wearable applications.

The GM02S can also be used as a slim modem controlled by an external MCU via its UART. Alternatively, the GM02S can execute applets on its embedded MCU.

1.3. Block Diagram

Figure 1. GM02S Block Diagram



1.4. General Features

Physical Characteristics	LGA module, 120 pads. Size: 16.3 × 17 × 2.3 mm
Temperature Range	Operation temperature range: -40 to +85 °C Storage: MSL3
Power Supply	Voltage range for RF compliance: 2.5 to 5.5 V Functional voltage range: 2.2 to 5.5 V
Tx Power	+23 dBm in each band
Interfaces	• Dual (U)SIM Card Interface: support for external, removable or fixed UICC. Support for integrated UICC (iUICC) with a dedicated p/h; • 4x High-Speed UART Interfaces with flow control, up to 921600 bauds; • GPIOs, I²C, SPI, PWM, I²S/PCM, ADC;
SMS	Text and PDU modes
Firmware Upgrade	UART interface, FOTA, support of full and differential firmware upgrade
RoHS/REACH	All hardware components fully comply with EU RoHS and REACH directives, bromine-free

LTE Features	• 3GPP LTE Release 13/14 Cat M1/NB1/NB2 compliant; • LTE Cat M1: 1.1 Mbps / 0.3 Mbps UL/DL throughput; • LTE Cat NB1: 62.5 kbps / 27.2 kbps UL/DL throughput; • LTE Cat NB2: 160 kbps / 120.7 kbps UL/DL throughput. Cat NB1/NB2 support is planned for upcoming software upgrades
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1.5. Available Part Numbers

GM02S's ECCN is 5A991.

Table 3. Available Part Numbers

Part Number	Hardware Version	Software Build (AT11)	UE Ver- sion (AT11)	PTCRB Model Name / Model	SVN	Availabil- ity Status
GM02RBAQRF	HW Rev. 3 FCC/IC/RED/UKCA ACMA/JATE/TELEC PTCRB/GCF	LR 8.0.5.11	UE 8.0.5.11	GM02S	12	Available with unlocked OTP
GM02RBAQRH		LR 8.0.5.12	UE 8.0.5.12		13	Available with unlocked OTP
GM02RBAQRK		LR 8.2.0.2	UE 8.2.0.2		15	Available with unlocked OTP
GM02RBAQRL		LR 8.0.5.13	UE 8.0.5.13		16	Available with unlocked OTP
GM02RBAQRM		LR 8.2.1.0	UE 8.2.1.0		19	Available with unlocked OTP
GM02RBAQRN						Secured Module available with OTP locked
GM02RBAQRO		LR 8.0.5.14	UE 8.0.5.14		21	Available with unlocked OTP

2. INTERFACES

The GM02S provides electric interfaces connecting it to the external parts, such as communication I/O ports, GPIO and antenna RF I/O. This chapter provides information about all these interfaces.

Power supply pins and details thereof are detailed in section [Electrical, RF and Thermal Characteristics](#).

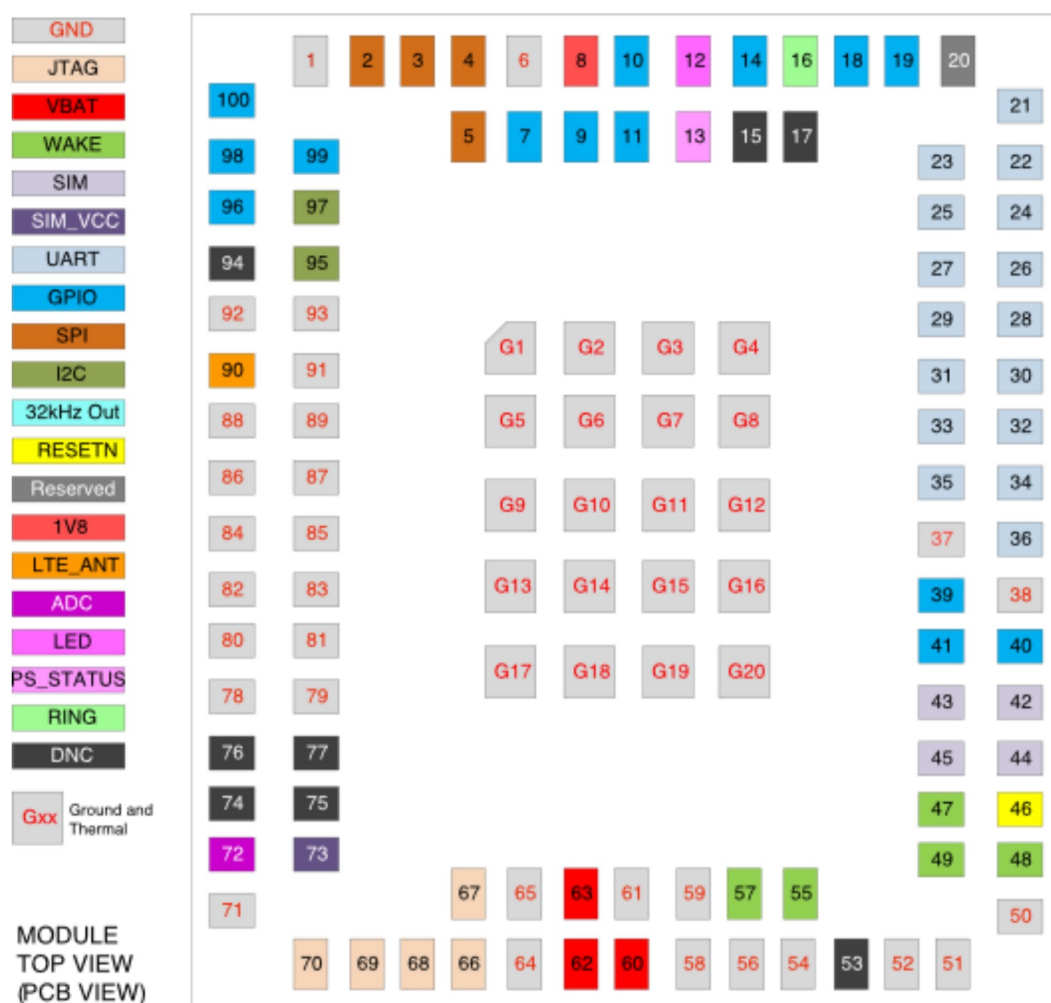


Important: Please refer to this data sheet's companion MS-Excel file for details on each pin's:

- Default assigned function;
- State during low power modes;
- Configuration with AT commands;
- Pull status and requirements.

2.1. Pin Assignment

Figure 2. GM02S Module Pads Assignments



2.2. UART

The GM02S has three available UARTs to communicate with the application processor.

Table 4. UART Signals

Pad #	Pad Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad type ⁱⁱ	Reset state
36	GPIO12/TXD0	TXD0	GPIO12	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		In for primary function, UART0					
34	GPIO13/RXD0	RXD0	GPIO13	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
35	GPIO14/ CTS0	CTS0	GPIO14	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART0					
33	RTS0	RTS0	N/A	PMU_5V	In	IN	High-Z
		Wake signal enabled by default.					
32	TXD1	TXD1	N/A	PVDD_1V8	In	BIDIR	High-Z, 2 mA
		UART1					
30	RXD1	RXD1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
31	CTS1	CTS1	N/A	PVDD_1V8	Out	BIDIR	Out-1, 2 mA
		UART1					
29	RTS1	RTS1	N/A	PMU_5V	In	IN	High-Z
		Wake signal enabled by default.					
28	GPIO15/TXD2	TXD2	GPIO15	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		In for primary function, UART2					
26	GPIO16/RXD2	RXD2	GPIO16	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART2					
27	GPIO17/ CTS2/ DCD0	GPIO17	CTS2/ DCD0	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART2					
25	GPIO18/ RTS2/ DSR0	GPIO18	RTS2/ DSR0	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		UART2					
24	GPIO19/TXD3	GPIO19	TXD3	PVDD_1V8	In/Out	BIDIR	HighZ, 2 mA
		In for primary function, UART3					
22	GPIO20/RXD3	GPIO20	RXD3	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		Out for primary function, UART3					

Table 4. UART Signals (continued)

Pad #	Pad Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad type ⁱⁱ	Reset state
21	GPIO21/CTS3	GPIO21	CTS3	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART3					
23	GPIO22/RTS3	GPIO22	RTS3	PVDD_1V8	In/Out	BIDIR	Out-1, 2 mA
		UART3					

i. Alternate functions will be available in future versions via SW upgrade.

ii. UART pad types's electrical characteristics are detailed in Table 26 and Table 27.



Note: See section [Power](#) for behaviour of I/Os in Deep Sleep mode.

UART Default Configuration

UART interfaces have three function modes:

- The Host-Modem interface, also named 'AT mode', configures and exchanges data with the modem using standard or proprietary AT commands. This mode requires a high-speed UART port with flow control.
- The Modem Console interface copies the logs from the LTE modem.
- The Debug interface (also referred to as DCP) is needed by the DM Tool during design verification or debugging. This interface can be used to upgrade the software using SFU.

The default configuration appears in Table 5.

Table 5. UART Ports Default Configuration

UART#	Baudrate	Flow Control	Application	Wake Source	Manufacturing Upgrade
0	115200	Enabled	AT	Yes	Yes
1	921600	Enabled	AT	Yes	Yes
2	115200	Disabled	Console	No	No

Refer to the Module Manufacturing Guidelines for overriding this default configuration.

UART wiring

The GM02S complies to the DCE-DTE convention for UART lines. It is designed as a DCE (Data Communication Equipment).

The output from the device at one end of the link connects to the corresponding input at the other end of the link and vice versa. The [Figure 3](#) represents the typical implementation for the UART connection (including hardware flow control in case of high-speed UARTs).

The DCE (Data Communication Equipment) device communicates with the customer application (DTE) using the following signals:

- Port TxD on the application board side sends data to the GM02S's TxD signal line.
- Port RxD on the application board side receives data from the GM02S's RxD signal line.

- CTS0, CTS1, CTS2, CTS3: Clear-To-Send signals of resp. UART0, UART1, UART2, UART3 (active low). To be connected to the CTS of the remote UART device. See [Figure 3](#).

Leave CTS unconnected if hardware flow control is not used.

- RTS0, RTS1, RTS2, RTS3: Ready-To-Send signals of resp. UART0, UART1, UART2, UART3 (active low). To be connected to the RTS of the remote UART device. Tie to a 1 kΩ pull-down when flow control is not used. If connected to an external part (like a RS 232 driver), the user must insure that the part presents a low level to the GM02S See [Figure 3](#).



Important: When pull-ups are recommended or required on UART lines, care must be taken that the DC power source pulling-up the signal is on even when the module is in low power mode. For example, never use the 1V8 signal (which is turned off in low power mode).

[Figure 3](#) represents the typical implementation for hardware flow control.

[Figure 3. UART Connection Implementation \(with Hardware Flow Control\)](#)

Please refer to the System Integration Guide document for more details about the possible implementation.



Important: Designs should provide access to UART 1 with hardware flow control to facilitate debug and upgrade during the development of the product. Simple UART connectors or, more conveniently, dedicated UART-to-USB converter ICs paired with a USB connector, as implemented in the EVK reference design, suffice.

Various UART-to-USB converters were tested on modules, including the Exar XR21V1410, FTDI FT234XD or FTDI FT4232H. Implementation examples can be found in reference designs schematics.

2.3. USIM Interfaces

SIM0 Interface

This is the main external SIM interface. It can be used with removable or non-removable SIM cards or with soldered SIM chips. The modem manages the SIM's power supply to keep consumption as low as possible.



Note: See Section [Power](#) for behaviour of I/Os in Deep Sleep mode.

! Important: The GM02S only supports 1.8 V SIMs.

Table 6. SIM0 Signals

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type ⁱ	Reset State	Comment
42	SIM0_CLK	SIM0_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA	Main SIM
45	SIM0_DETECT ⁱⁱ	SIM0_DETECT	PMU_5V	In	IN	High-Z	Main SIM
44	SIM0_IO	SIM0_IO	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA	Main SIM
43	SIM0_RSTN	SIM0_RSTN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA	Main SIM
73	SIM0_VCC ⁱⁱⁱ	SIM0_VCC	PVDD_1V8	Out	SUPPLY	Out-0, 30 mA	Main SIM

i. USIM pad types electrical characteristics are detailed in Table 26 and Table 27.

ii. SIM0_DETECT is active high (high when a card is present, low when no card is present). It can be configured as a WAKE pin via software command.

iii. See range of values in Table 18.

SIM1 Interface

This GM02S's interface to a second SIM is typically meant for soldered SIM chips (since it lacks SIM detect and SIM VCC). If the board makes use of a single SIM, it should be connected to the main SIM interface (see Section SIM0 Interface above).



Note: SIMs connected to the SIM 1 interface need an external 1.8 V power source, since the SIM 1 group lacks a VCC output. It is thus recommended to use SIM 0, except if a dual SIM solution is mandatory.



Note: See Section Power for behaviour of I/Os in Deep Sleep mode.

Table 7. SIM1 Signals

Pad #	Pad Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad Type ⁱⁱ	Reset state
40	GPIO26/SIM1_CLK	GPIO26	SIM1_CLK	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
41	GPIO27/SIM1_RESETN	GPIO27	SIM1_RESETN	PVDD_1V8	Out	BIDIR	Out-0, 2 mA
39	GPIO25/SIM1_IO	GPIO25	SIM1_IO	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA

i. Alternate functions will be available in future versions via SW upgrade.

ii. Pad types electrical characteristics are detailed in Table 26.

Miscellaneous Hardware Considerations

- Use a 100 nF decoupling capacitor on SIM_VCC.
- Use a 4.7 kΩ pull-up resistor between SIM_VCC and SIM_IO.
- The SIM connector should be located as close as possible to the module.
- Please ensure ground continuity between the SIM card and the module.
- If the application handles SIM card hot swapping, the SIM slot must contain a card detector in order for the software to process the event immediately. Default software configuration is to support SIM_DETECT.
- If the SIM card tray does not support SIM_DETECT (not recommended), keep the SIM_DETECT signal high and configure the module for SIM card detection using polling mode.

2.4. I²C



Note: See Section [Power](#) for behaviour of I/Os in **Deep Sleep** mode.

Table 8. I²C Pad Details

Pad #	Pad Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad type ⁱⁱ	Reset State
95	GPIO23/I2C_SDA	GPIO23	I2C_SDA	PVDD_1V8	In/Out	BIDIR	High-Z
97	GPIO24/I2C_SCL	GPIO24	I2C_SCL	PVDD_1V8	In/Out	BIDIR	High-Z

i. Alternate functions will be available in future versions via SW upgrade.

ii. I²C pad types's electrical characteristics are detailed in Table 26.

2.5. PCM



Note: See section [Power](#) for behaviour of I/Os in **Deep Sleep** mode.

Table 9. PCM Pad Details

Pad #	Pad Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad type ⁱⁱ	Reset State
96	GPIO4/PCM_CLK	GPIO4	PCM_CLK	PVDD_1V8	In/Out	BIDIR	High-Z
98	GPIO3/PCM_RXD	GPIO3	PCM_RXD	PVDD_1V8	In/Out	BIDIR	High-Z
99	GPIO5/PCM_FS	GPIO5	PCM_FS	PVDD_1V8	In/Out	BIDIR	High-Z
100	GPIO6/PCM_TXD	GPIO6	PCM_TXD	PVDD_1V8	In/Out	BIDIR	High-Z

i. Alternate functions will be available in future versions via SW upgrade.

ii. PCM pad types's electrical characteristics are detailed Table 26.

2.6. SPI



Note: See section [Power](#) for behaviour of I/Os in **Deep Sleep** mode.

Table 10. SPI Pad Details

Pad #	Pad Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad type ⁱⁱ	Reset state
3	GPIO7/SPI_SDI	GPIO7	SPI_SDI	PVDD_1V8	In/Out	BIDIR	High-Z
4	GPIO8/SPI_SDO	GPIO8	SPI_SDO	PVDD_1V8	In/Out	BIDIR	High-Z
2	GPIO9/SPI_CLK	GPIO9	SPI_CLK	PVDD_1V8	In/Out	BIDIR	High-Z
5	GPIO10/SPI_CSN1	GPIO10	SPI_CSN1	PVDD_1V8	In/Out	BIDIR	High-Z
7	GPIO11/ SPI_CSN2 ⁱⁱⁱ	GPIO11	SPI_CSN2	PVDD_1V8	In/Out	BIDIR	High-Z

i. Alternate functions will be available in future versions via SW upgrade.

ii. SPI pad types' electrical characteristics are detailed in Table 26.

iii. This pin is currently unavailable.

To enable SPI, GPIO 7, 8, 9, 10 and 11 should be disabled.

When SPI is enabled, **SPI_SDO** (Serial Data Output) is an INPUT which is connected to the slave **DO** (Data Output). Conversely, **SPI_SDI** (Serial Data Input) is an OUTPUT connected to the slave's **DI** (Data Input).

2.7. GPIO

33 GPIOs are available on the GM02S: GPIO1 to GPIO28 and GPIO31 to GPIO35. The GPIOs listed in [Table 11](#) are not enabled by default. Their states are controlled by software.

Table 11. GPIO pads detail

GPIO Range	Default State
GPIO3 to GPIO11	Disabled
GPIO17 to GPIO28	Disabled
GPIO31 to GPIO35	Disabled

The GPIOs are documented in this data sheet according to their shared or assigned function. In addition to the GPIO, five wake signals are also available (see section [Other Signals](#)).

GM02S GPIO to SQN 3430 GPIO Number Crosstable

In order to properly use some manufacturing AT commands such as [AT+SMGI](#) or [AT+SMGT](#), the 'internal' (SQN 3430 chipset GPIO) number of each GM02S's GPIO must be known. The following table lists every GM02S's GPIO and gives the corresponding internal number value.

Table 12. GM02S to SQN 3430 GPIO Crosstable

GM02S GPIO Number	Corresponding SQN 3430 GPIO Number
1	38
2	39
3	34
4	33
5	32
6	31
7	21
8	22
9	20
10	23
11	24
12	4
13	5
14	6
15	10
16	11
17	13

Table 12. GM02S to SQN 3430 GPIO Crosstable (continued)

GM02S GPIO Number	Corresponding SQN 3430 GPIO Number
18	12
19	14
20	15
21	16
22	17
23	18
24	19
25	28
26	29
27	30
28	40
31	3
32	1
33	35
34	36
35	37

2.8. Other Signals

Table 13. GND and DNC pads

Pads Type	Pads Number
GND	1, 6, 37, 38, 50, 51, 52, 54, 56, 58, 59, 61, 64, 65, 71, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 91, 92, 93
DNC (Reserved)	15, 17, 53, 74, 75, 76, 77, 94



Note: See Section [Power](#) for behaviour of I/Os in **Deep Sleep** mode.

Table 14. Other Signals (No Interface)

Pad #	Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad Type ⁱⁱ	Reset State
72	ADC1	ADC1 (see below)	N/A	N/A	In	IN	N/A
Analogue-Digital Converter (ADC, IN)							
12	GPIO1/ STATUS_LED	STATUS_LED	GPIO1	PVDD_IV8	In/Out	BIDIR	High-Z, 2 mA
Primary Function: Status LED (STATUS_LED, OUT)							

Table 14. Other Signals (No Interface) (continued)

Pad #	Name	Primary Function	Alternate ⁱ Function	Power Group	Direction	Pad Type ⁱⁱ	Reset State
13	GPIO2/ PS_STATUS	PS_STATUS	GPIO2	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Power Saving status (PS_STATUS, OUT) enabled by default. Active high.					
14	GPIO28/DTR0	GPIO28	DTR0	PVDD_1V8	In/Out	BIDIR	High-Z
19	GPIO31/PWM0/ 19M2_OUT	GPIO31	PWM0/19M2_OUT	PVDD_1V8	In/Out	BIDIR	High-Z
18	GPIO32/PWM1	GPIO32	PWM1	PVDD_1V8	In/Out	BIDIR	High-Z
9	GPIO33/TX_IND	TX_IND	GPIO33	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Transmission indicator (TX_IND, OUT). Active high.					
10	GPIO34/ ANT_TUNE0	ANT_TUNE0	GPIO34	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE0, OUT)					
11	GPIO35/ ANT_TUNE1	ANT_TUNE1	GPIO35	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		Primary Function: Antenna tuning (ANT_TUNE1, OUT)					
20	RESERVED/ FFF_FFH	RESERVED	N/A	PVDD_1V8	N/A	BIDIR	High-Z, 2 mA
		Boot mode selection (FFF_FFH, IN). This pad needs a pull-down resistor by default.					
46	RESETN	RESETN	N/A	PMU_5V	In	IN	In, Pull-up
		Module HW reset signal. Active low. The minimum duration of a reset pulse on the RESETN signal is 100 µs.					
16	RING0	RING0	N/A	PVDD_1V8	In/Out	BIDIR	High-Z, 2 mA
		UART0 ring line (RING0, OUT). Enabled by default with inverted polarity.					
48	WAKE0	WAKE0	N/A	PMU_5V	In	IN	High-Z
		Wake #0 input line (WAKE0, IN), disabled by default.					
47	WAKE1	WAKE1	N/A	PMU_5V	In	IN	High-Z
		Wake #1 input line (WAKE1, IN), disabled by default.					
49	WAKE2	WAKE2	N/A	PMU_5V	In	IN	High-Z
		Wake #2 input line (WAKE2, IN), disabled by default.					
55	WAKE3	WAKE3	N/A	PMU_5V	In	IN	High-Z
		Wake #3 input line (WAKE3, IN), disabled by default.					
57	WAKE4	WAKE4	N/A	PMU_5V	In	IN	High-Z
		Wake #4 input line (WAKE4, IN), disabled by default.					

i. Functions will be available in future versions via SW upgrade.

ii. Pad types' electrical characteristics are detailed in Table 26 and Table 27.

ADC Specifications

The ADC1 pin 72 has the following specifications:

Table 15. ADC Specifications

Parameter	Value	Unit
Resolution	14	bit
Dynamic Range	75	dB
Signal-to-Noise Ratio (SNR)	68	dB
Effective Number of Bits	11	bit
Input Signal Bandwidth	1.4	MHz
Full-scale Voltage	1.8	V
Input Resistance	40	kΩ

Don't connect the ADC if it is not used (no need for resistive or capacitive termination).

2.9. JTAG



Note: See Section [Power](#) for behaviour of I/Os in **Deep Sleep** mode.

Table 16. JTAG pads Details

Pad #	Pad Name	Primary Function	Power Group	Direction	Pad type ⁱ	Reset State
69	JTAG_TCK	JTAG_TCK	PVDD_1V8	In	IN	In, Pull-down, Schmitt-trigger
67	JTAG_TDI	JTAG_TDI	PVDD_1V8	In	IN	In, Pull-up
68	JTAG_TDO	JTAG_TDO	PVDD_1V8	Out	BIDIR	Out, 0
66	JTAG_TMS	JTAG_TMS	PVDD_1V8	In	IN	In, Pull-up
70	JTAG_TRSTN	JTAG_TRSTN	PVDD_1V8	In	IN	In, Pull-down

i. JTAG pad types's electrical characteristics are detailed in [Table 26](#).



Note: The GM02S does not support boundary scan (IEEE 1149.1) for production testing.

2.10. Antenna

Table 17. Antenna pad Details

Pad #	Pad Name	Direction	Comments
90	LTE_ANT	In/Out	Main LTE Antenna, for Rx and Tx

3. ELECTRICAL, RF AND THERMAL CHARACTERISTICS

3.1. Power

! Important: Details about power consumption can be found in the Software Release note corresponding to the product's software version installed.

Power Pads Characteristics

✎ Note: Pad 1V8 is the reference voltage for I/Os. It can be used to provide power to small devices (100 mA maximum usage). This voltage is not available when the modem is in Deep Sleep mode. When the modem is in standby the voltage drops to 1.62 V as per Table 18.

Table 18. Power Pads

Pad #	Pad Name	Power Group	Direction	Min Value	Typical Value	Max Value
8	1V8 (see Note above)	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
73	SIM_VCC ⁱ	PVDD_1V8	Out	1.62 V	1.8 V	1.98 V
60, 62, 63	V _{BAT}	N/A	In	2.2 V		5.5 V

i. See also Section USIM Interfaces.

✎ Note: Reference V_{BAT} voltage range is 2.5 V to 5.5 V for RF-compliant operation and 2.2 V to 5.5 V for functional operation with possible degradation of RF performances.

✎ Note: The GM02S does not use any boost or step-up DC/DC converters.

Power-on, Power-off and Reset

Figure 4. Power Cycle Timing

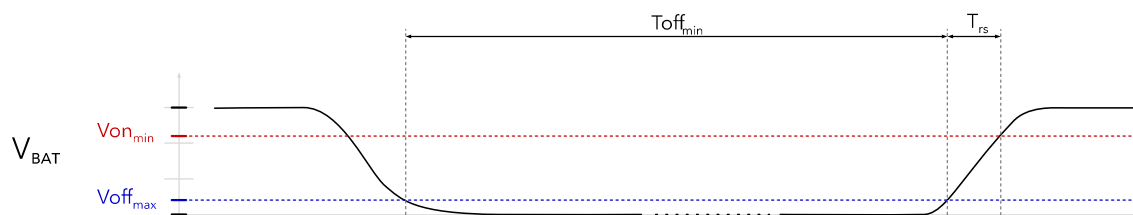


Table 19. Timing values

Name	Description	Min.	Typ.	Max.	Unit
Von _{min}	Minimal ON Voltage	2.2			V
Trs	V _{BAT} Rise Time from Voff _{max} to Von _{min}	1 ⁱ		10 000	μs

i. Shorter rise times can trigger the ESD protection.

The value of Toff_{min} depends on the Voff_{max} voltage. The following table gives three typical figures:

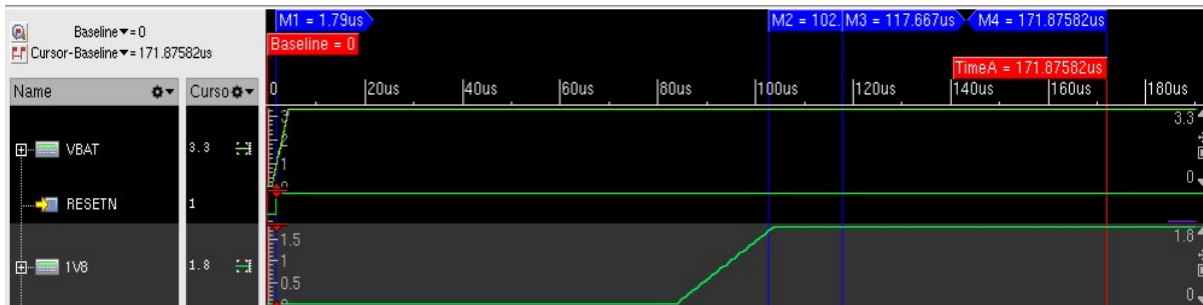
Table 20. $T_{off_{min}}$ vs. $V_{off_{max}}$

Name	Description	Value
$T_{off_{min}}$ @ 50 mV	Minimal OFF ($V_{BAT} \leq V_{off_{max}}$) time to insure complete reset when $V_{off_{max}} = 50$ mV	0.1 s
$T_{off_{min}}$ @ 0.1 V	Minimal OFF ($V_{BAT} \leq V_{off_{max}}$) time to insure complete reset when $V_{off_{max}} = 0.1$ V	0.5 s
$T_{off_{min}}$ @ 0.2 V	Minimal OFF ($V_{BAT} \leq V_{off_{max}}$) time to insure complete reset when $V_{off_{max}} = 0.2$ V	1 s



Caution! V_{BAT} must always be at least equal to $V_{on_{min}}$ during normal operation. Once V_{BAT} has dropped below this threshold, always ensure the voltage keeps on dropping down to $V_{off_{max}}$ and remains low for at least $T_{off_{min}}$. Failure to comply, as well as failure to meet the maximum V_{BAT} rising time requirement (T_{rs}) during power-on, can result in erratic behaviour.

Figure 5. Typical Timing Diagram for Power-Up Sequence



Important: The TV8 power signal can remain low up to 370 μ s after the V_{BAT} rising edge

Figure 6. Typical Timing Diagram for Reset Sequence



Note: since RESETN is pulled-up internally, RESETN does not need to be held low after V_{BAT} is established, as shown in Figure 6. There is no timing condition between RESETN and V_{BAT} .



Note: RESETN minimum duration for reliable detection is 100 μ s.

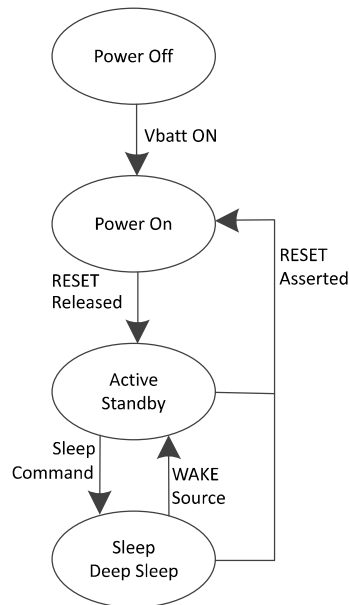


Note: RESETN is pulled up using an internal 1 M Ω + resistance. In order to measure this signal accurately, use a very-high impedance probe.

Power States

Figure 7 represents the electrical states of the module and their transitions.

Figure 7. Electrical States and Transitions



There are four possible power modes:

- Active mode: operational, UART on, RF on, LCPU/MCPU/DSP are running. Power consumption depends on workload and transmit power level.
- Standby mode: Same as active mode, except RF off.
- Sleep mode: MLCPU/LCPU/DSP are power gated, UART off, RAM content is salvaged. Power level 300 μ A circa.
- Deep Sleep Mode: Only the power management unit (PMU) stays active. Power level 1 μ A.

More information is given in the table below:

Table 21. Power Modes Description

Power Mode	LTE Mode	Available Interfaces
Active	Connected (RF on)	All interfaces
Standby	Connected (RF off)	All interfaces
Sleep	Short eDRX idle duration RRC Idle	WAKE pins (including RTS0/I)
Deep Sleep	PSM idle, Long eDRX idle duration, radio-off, airplane mode	WAKE pins (including RTS0/I)

PVDD_1V8 BIDIR Pads State in Deep Sleep Mode

In Deep Sleep mode, the Digital PVDD_1V8 bi-directional I/Os are completely powered off and behave like 50 M Ω high-impedance pins.

PMU_5V IN Pads State in Deep Sleep Mode

In Deep Sleep mode the digital PMU_5V inputs are completely powered off and behave like 180 M Ω high-impedance pins.

Table 22 gives the values of the measured leakage current (measurements taken on silicon) for the PMU wake inputs.

Table 22. Measured Leakage Current for the PMU Wake Inputs

Minimum	Typical	Maximum
3 nA	4 nA	12 nA

Table 23 shows values of the external pull-up/pull-down resistor to be used at the PMU wake inputs pads.

Table 23. External Pull-up/Pull-down Resistor at PMU Wake Input Pads

Minimum	Typical	Maximum
1 k Ω	10 k Ω	100 k Ω

Table 24 details the PMU wake input pulses detection mechanism timings.

Table 24. PMU Wake Input Pulses Detection Mechanism Timings

Maximum pulse width guaranteed to be ignored	Minimum pulse width guaranteed to be recognised
11.1 ns	100 μ s

Table 25 provides the internal pull-up current range at RESETN.

Table 25. Internal Pull-Up Current at RESETN Pad

Minimum	Typical	Maximum
73.5 nA	100 nA	160.5 nA

3.2. Digital I/O Characteristics

This section details the voltage and current characteristics of the various I/O pads of the GM02S.

The I/Os belong either one of two power groups:

- PVDD_1V8
- PMU_5V

The operational voltage range of both power groups is described in Table 26 and Table 27.



Caution! Designers must ensure that the input voltage on any of the I/O pads never exceeds the V_{IH} of the power group they belong to.

See Table 26 for the digital I/O characteristics of the different I/O pads. Refer to each interface of the GM02S in chapter Interfaces for the power group and I/O pad type of each pad. Note that IN pads are inputs only whereas BIDIR can be both inputs and outputs.

Table 26. DC Ratings for Digital I/Os, PVDD_1V8 Power Group

Symbol	Minimum	Maximum	Unit
V _{IH} — Input HIGH level	1.26	3.3	V
V _{IL} — Input LOW level	0	0.54	V
V _{OH} — Output HIGH voltage	1.44	1.8	V
V _{OL} — Output LOW voltage	0	0.36	V
I _{RPU} — Input pull-up resistor current	15		μA
R _{RPU} — Input pull-up resistance	27	34	kΩ
I _{RPD} — Input pull-down resistor current	15		μA
R _{RPD} — Input pull-down resistance	27	34	kΩ
V _H — Input hysteresis	0.18		V
I _{PAD} — Input leakage current, non-tolerant	-1	1	μA
I _{OZ} — Off-State leakage current		1	μA

Table 27. DC Ratings for Digital I/Os, PMU_5V Power Group

Symbol	Minimum	Maximum	Unit
V _{IH} — Input HIGH level	0.8	V _{BAT} + 0.6 (max. 5.5)	V
V _{IL} — Input LOW level	0	0.2	V

The total capacitance of the GM02S is 115 μF. Total inductance is 5.3 μH.

3.3. RF Performance



Important: For proper operation, the VSWR at the antenna pad must be better than 2:1 in conducted mode and 3:1 in radiated mode. A higher value could result either in poor RF performance, reduced Tx power or increased sideband/harmonic emission levels. Very high VSWRs can permanently damage the power amplifier.

It is recommended to add a DC blocking capacitor in series with the module RF input/output pad (#90).

RF Sensitivity

The GM02S exhibits the following typical RF sensitivity at 2.5 V:

Table 28. RF Sensitivity

Technology	Band	Typical Sensitivity
LTE-M	Low Bands: B5, B12, B13, B14, B17, B18, B19, B20, B26, B28, B85	-105 dBm
	High bands: B1, B2, B3, B4, B25, B66	-106 dBm
NB-IoT	Low Bands: B5, B8, B12, B13, B17, B18, B19, B20, B26, B28, B85	-113 dBm
	High bands: B1, B2, B3, B4, B25, B66	-113 dBm