SEQUANS

# Calliope 2 Platform

## GC02S1 Module

# GC02S1 Data Sheet (Preliminary)

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# About this Data Sheet

## Purpose and Scope

The GC02S1 modules are complete LTE Cat1 systems including base-band, RF and memory, targeting mass-market wearables, consumers and M2M / IoT devices. This document provides the technical information about the GC02S1 LGA module family. Calliope 2 modules are based on Sequans's SQN3530 chipset.

## Changes in this Document

This is the seventh preliminary (P6a) revision of the document, superseding version P6 (October 2023).

**Table 1. Revision and changes**

| Rev. | Date | Changes |
|---|---|---|
| P6a | Nov. 2023 | • Add a warning about antenna efficiency<br>• Change FCC and ISED maximum allowed gain in Regulatory Information<br>• Factory Reset now correctly references AT+SQNFACTORY… commands<br>• New style sheet |
| P6 | Oct. 2023 | • Add FCC certification statement<br>• Detail conditions for RF sensitivity measurements<br>• Shows what pin numbers USB signals are connected to in Figure 4 *(on page 17)* |
| P5 | Oct. 2023 | • Reinstate the frequency band table<br>• Reinstate mechanical section<br>• Modify primary function of pins 21 to 24 (GPIO instead of UART 3)<br>• Specify that SIM0_DETECT is not polarity programmable<br>• Update marking for -2 series<br>• Add further hardware/routing recommendations<br>• Note about USB_VBUS being tied to WAKE4<br>• Add RF sensitivities for -NA2 model |
| P4 | June 2023 | • Merge with contents of the *Module Integration Guide* and *Module Manufacturing Guide* documents. General overhaul. |

**Table 1. Revision and changes (continued)**

| Rev. | Date | Changes |
|---|---|---|
| P3 | Nov. 2022 | • Added band 14 (NA2 model)<br>• Added section 3.1.2 and table 15<br>• Added description/info of signals TX_IND, Status LED and USBREADY<br>• Added emergency shut down function for WAKE2<br>• Updated band grouping in section 1.1<br>• Updated section 2.3 USB<br>• Updated info in table 19 |
| P2 | Apr. 2022 | • Added operating bands for the EU variant<br>• Changes in recommended voltage operating range in § 3.3.2<br>• Added marking info for JP and EU variants |
| P1 | Feb. 2022 | N/A |

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# 1. General Description

The Calliope 2 GC02S1 modules are based on Sequans's second-generation Calliope 2 silicon and delivers optimised 4G LTE Cat 1 connectivity for IoT, M2M and consumer devices such as wearables and hearables that require voice support and speed higher than LTE-M.

Calliope 2 provides significant improvements in performance and power consumption over Calliope 1, while offering a seamless migration, because it also leverages Sequans's existing 4G LTE protocol stack, one of the most mature and proven in the entire LTE ecosystem. The Calliope 2 GC02S1 modules include Sequans's Calliope 2 platform and all other elements needed for a LTE modem system, including an LTE optimised transceiver, an RF front end, and key interfaces in a compact, cost-effective form factor that needs no external components.

It also includes an integrated EAL5+ secure enclave providing secure key storage, cryptographic applications and integrated SIM (iSIM) functionality.

Calliope 2 GC02S1 modules are manufactured in three regional variants covering North America, Japan and Europe.

Calliope 2 based modules are compatible with Sequans's *Monarch 2 GM02S* modules, easing the migration and the integration into already existing LTE-M or NB1 designs.

## 1.1. Frequency Bands

The GC02S1 modules support the following bands, according to their designated region:

**Table 2. Band Support per Module Variant**

| Variant Name | Bands | Region |
|---|---|---|
| GC02S1-NA2 | B25 [B2]/B66 [B4]/B5/B12 [B17]/B13/B14 | North America |
| GC02S1-JP1 | B1/B26 [B18/B19] | Japan |
| GC02S1-EU2 | B1/B3/B8/B20 and B28 | Europe |

## 1.2. Block Diagram

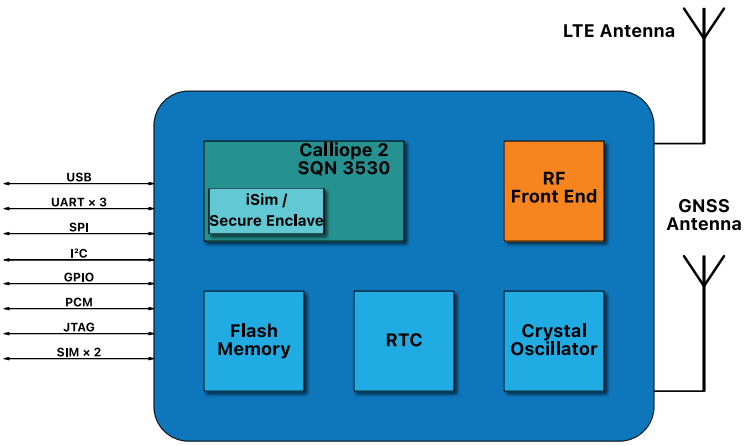



Figure 1. GC02S1 Block Diagram

## 1.3. General Features

| | |
|---|---|
| Physical Characteristics | LGA module, 142 pads. Size: 21 × 19.5 × 1.8 mm typ. |
| Temperature and Humidity Ranges | Board temperature range: -40 to +85 °C<br>Humidity: 10 to 85% (non-condensing)<br>Storage: MSL3 |
| Power Supply | 3.2 to 5.5 V (see section Power *(on page 27)*) |
| Maximum Tx Power | +23 dBm in each band |
| Interfaces | • Dual (U)SIM Card Interface: support for external, removable or fixed UICC. Support for integrated UICC (iUICC) with a dedicated p/n<br>• USB 2.0<br>• 4x High-Speed UART Interfaces with flow control, up to 3.6 Mbauds<br>• GPIOs, I²C, SPI, PWM, Pulse Counter, I²S/PCM, ADC |
| SMS | SMS over IMS or NAS |
| Firmware Upgrade | USB or UART interfaces, FOTA, support of differential firmware upgrade |
| RoHS | All hardware components are fully compliant with EU RoHS directive, bromine-free |
| LTE Features | • 3GPP LTE Release 14 Cat 1 bis compliant<br>• Hardware ready for 3GPP LTE Release 15<br>• 10Mbps / 5Mbps DL/UL throughput |

## 1.4. Applications

The Calliope 2 GC02S1 modules are ideal to bring LTE Connectivity to M2M and IoT devices, including:

- Utility meters
- Industrial sensors
- Security and alarm systems
- Payment systems
- Asset trackers
- Smart home devices
- Smart meters
- Wearable consumer applications.

## 1.5. Available Part Numbers

**Table 3. Available Part Numbers**

| Available Part Number | Product Name | Software Build (ATI1) | UE Version (ATI1) | PTCRB Model Name / Model | SVN | Availability |
|---|---|---|---|---|---|---|
| GC02RNAQRA | GC02S1-NA2 | Will be provided in a future edition of the document | TBD | Will be provided in a future edition of the document | TBD | Samples |
| GC02REUQRA | GC02S1-EU2 | Will be provided in a future edition of the document | TBD | Will be provided in a future edition of the document | TBD | Samples |
| GC02RJPQRA | GC02S1-JP1 | Will be provided in a future edition of the document | TBD | Will be provided in a future edition of the document | TBD | Samples |

**Note:** Please contact your local technical representative to pick the appropriate part number for your project.

# 2. Interfaces

The GC02S1 modules includes communication I/O ports, GPIO and antenna RF I/O. This chapter provides description of all the GC02S1's interfaces.

Power supply pins pin-out and characteristics are detailed in section Electrical, RF and Thermal Characteristics *(on page 27)*.

## 2.1. Pin Assignment

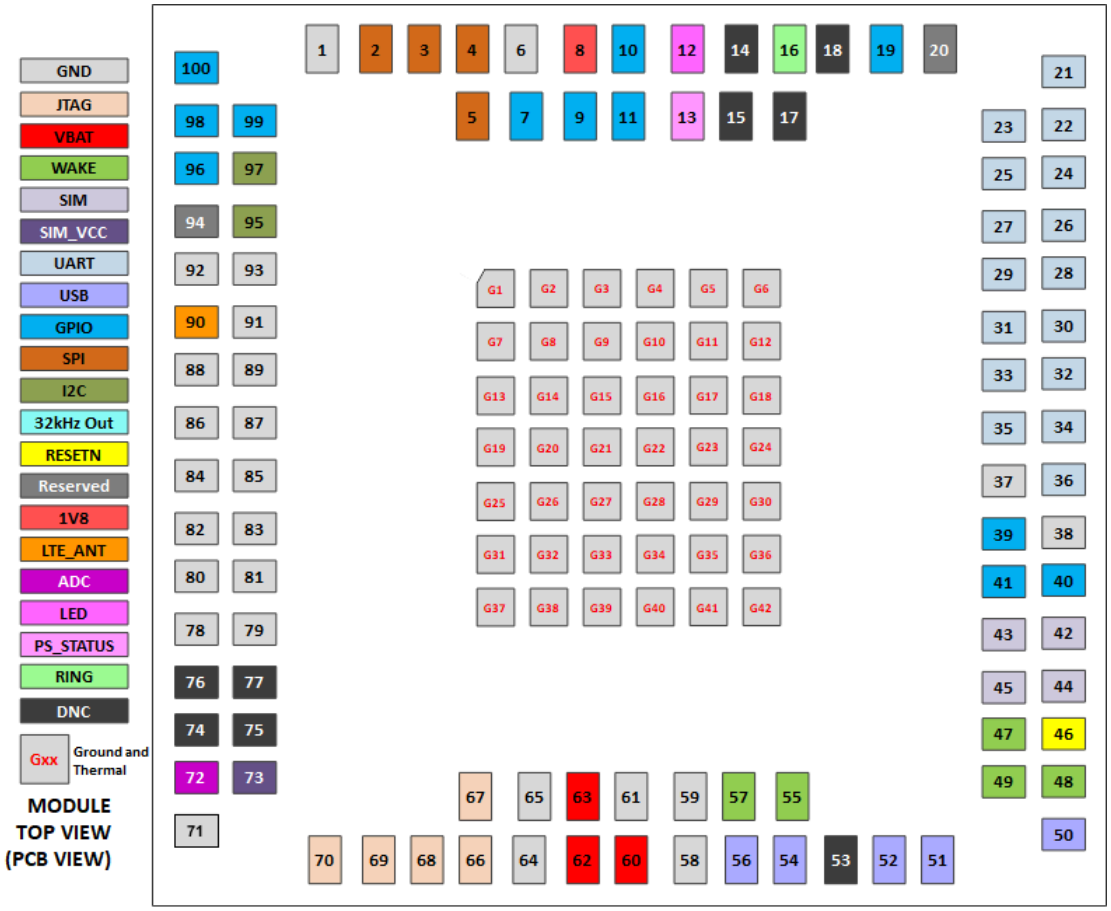



Figure 2. GC02S1 Modules Pads Assignment

**Note:** Pin 20 (RESERVED) must be pulled down.

## 2.2. UART

### 2.2.1. Introduction

Serial communications between the GC02S1 and the host platform can use any of the four UART interfaces named UART 0, 1, 2 and 3, all of which implement flow control.

UART interfaces support three modes:

- The Host-Modem interface, also named '*AT-Commands mode*', configures and exchanges data with the modem using standard or proprietary AT commands. This mode requires a high-speed UART port with flow control.
- The Modem Console interface copies the logs from the LTE modem
- The Debug interface (also referred to as DCP) is needed by the *DMTool* during design verification or debugging. This interface can be used to upgrade with SFU.

**Table 4. UART Interfaces Usage Synthesis**

| UART Port | Default Usage of Port | Available Usage of Port |
|---|---|---|
| UART 0 | AT Commands | Host-Modem interface |
| UART 1[1] | AT Commands | Manufacturing, debug and upgrade |
| UART 2 | Modem Console | Modem Console |
| UART 3 | Reserved, do not use | Reserved, do not use |

The default configuration is shown in Table 4 *(on page 11)*, and is configurable by software.

**Important:** Designs based on the GC02S1 should provide access to UART 1 with hardware flow control to facilitate debug and upgrade during the development of the product. Simple UART connectors or, more conveniently, dedicated UART-to-USB converter ICs paired with a USB connector, as implemented in the NEKTAR reference design, suffice.

Various UART-to-USB converters were tested on Calliope 2 modules, including the Exar XR21V1410™, FTDI FT234XD™ or FTDI FT4232H™. Implementation examples are available in Sequans's or NEKTAR's reference designs schematics.

The following sections detail these interfaces.

### 2.2.2. UART Electrical Characteristics

**CAUTION:** Voltage on any pads must never exceed $V_{IH}$ max.

**Table 5. UART Pads DC Characteristics**

| Symbol | Minimum | Maximum | Unit |
|---|---|---|---|
| $V_{IH}$ Input High level | 1.26 | 3.3 | V |
| $V_{IL}$ Input Low level | 0 | 0.54 | V |
| $V_{OH}$ Output High voltage | 1.44 | 1.8 | V |
| $V_{OL}$ Output Low voltage | 0 | 0.36 | V |

1. UART 1 is configured by default in AT Commands mode, but must be set to DCP mode during product manufacturing. See more details in the *Module Manufacturing Guidelines* document.

### 2.2.3. UART Signals

**Table 6. UART Signals**

| Pad # | Pad Name | Primary Function | Alternate[2] Function | Direction | Pad type | Voltage | Drive[3] Strength | Reset state |
|---|---|---|---|---|---|---|---|---|
| UART0 | | | | | | | | |
| 36 | GPIO12/ TXD0 | TXD0 | GPIO12 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | In for primary function, UART0. | | | | | | |
| 34 | GPIO13/ RXD0 | RXD0 | GPIO13 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | Out for primary function, UART0. | | | | | | |
| 35 | GPIO14/ CTS0 | CTS0 | GPIO14 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | Out for primary function, UART0. | | | | | | |
| 33 | RTS0 | RTS0 | N/A | In | IN | VBAT | N/A | High-Z |
| | | Wake signal enabled by default. | | | | | | |
| UART1 | | | | | | | | |
| 32 | TXD1 | TXD1 | N/A | In | BIDIR | 1.8 V | T to H | High-Z, T |
| | | UART1 | | | | | | |
| 30 | RXD1 | RXD1 | N/A | Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | UART1 | | | | | | |
| 31 | CTS1 | CTS1 | N/A | Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | UART1 | | | | | | |
| 29 | RTS1 | RTS1 | N/A | In | IN | VBAT | N/A | High-Z |
| | | Wake signal enabled by default. | | | | | | |
| UART2 | | | | | | | | |
| 28 | GPIO15/ TXD2 | TXD2 | GPIO15 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | In for primary function, UART2. | | | | | | |
| 26 | GPIO16/ RXD2 | RXD2 | GPIO16 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | Out for primary function, UART2. | | | | | | |
| 27 | GPIO17/ CTS2/ DCD0 | GPIO17 | CTS2/ DCD0 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | UART2 | | | | | | |
| 25 | GPIO18/ RTS2/ DSR0 | GPIO18 | RTS2/ DSR0 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | UART2 | | | | | | |
| UART3 | | | | | | | | |
| 24 | GPIO19/ TXD3 | GPIO19 | TXD3 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | GPIO19 | | | | | | |

2. Alternate functions will be available in future versions of the module via SW upgrade.
3. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

**Table 6. UART Signals (continued)**

| Pad # | Pad Name | Primary Function | Alternate[2] Function | Direction | Pad type | Voltage | Drive[3] Strength | Reset state |
|---|---|---|---|---|---|---|---|---|
| 22 | GPIO20/ RXD3 | GPIO20 | RXD3 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | GPIO20 | | | | | | |
| 21 | GPIO21/ CTS3 | GPIO21 | CTS3 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | GPIO21 | | | | | | |
| 23 | GPIO22/ RTS3 | GPIO22 | RTS3 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| | | GPIO22 | | | | | | |

High-Speed UARTs Flow Control Signals:

- CTS0, CTS1, CTS2, CTS3: Clear-To-Send signals of resp. UART0, UART1, UART2, UART3 (active low). To be connected to the CTS of the remote UART device. If connected to an external component (such as an RS-232 driver), make sure that this component drives the signal low.

  Leave CTS unconnected if hardware flow control is not used.

- RTS0, RTS1, RTS2, RTS3: Request-To-Send signals of resp. UART0, UART1, UART2, UART3 (active low). To be connected to the RTS of the remote UART device. Use a 1 kΩ pull-down when flow control is not used.

In order for the module to properly enter low power mode, if hardware flow control is not used, it must also be disabled using `AT+SQNHWCFG`.

Figure 3 *(on page 13)* represents the typical implementation for hardware flow control.

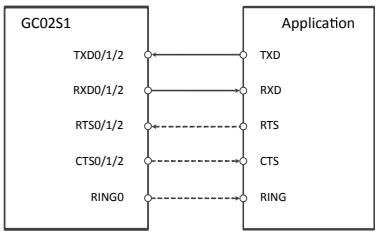



Figure 3. UART Convention and Flow Control

**Note:** After configuring specific software registers and setting the CTS signal to 0, high-speed UARTs can be used as low-speed UARTs. Please contact Sequans's customer support for details.

**Attention:** When pull-ups are recommended or required on UART lines, care must be taken that the DC power source pulling-up the signal remains on when the module goes into low power mode. Never use the GC02S1 1V8 signal (which is turned off in low power mode).

2. Alternate functions will be available in future versions of the module via SW upgrade.
3. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

### 2.2.4. UART 0 Interface

**Important:**

- UART 0 signals should be connected to test points.
- A pull-up is recommended on UART 0's RTS and CTS signals (see warning above).
- UART 0's tracks should be routed on a buried layer to reduce the EM leakage.

#### *Default Configuration*

UART 0 is in 'AT-Commands mode' by default with hardware flow control on. Serial link configuration:

- Baud rate: 115200 (maximum speed: 3686400 bit/s)
- Data: 8 bits
- Parity: None
- Stop : 1 bit
- Flow control: Hardware (RTS/CTS)

#### *Behaviour in Low Power Mode*

- The module power mode selection is internally managed by the module software.
- RTS0 signal is an input to the module. The host uses it to wake the module up. A pull-up, either internal or external, is recommended on this signal to avoid the module waking up if the host goes into low power mode and leaves the pad floating.
- CTS0 is an output of the module. It signals when the modem is ready to receive characters. Since the modem does not drive this signal during deep sleep mode, it is preferable to pull the signal up either internally or externally.

### 2.2.5. UART 1 Interface

**Important:**

- UART 1's signals should be connected to test points.
- A pull-up is recommended on UART 1's RTS signal (see warning above).

#### *Default Configuration*

UART 1 is in 'AT-command' mode by default.

Default serial parameters:

- Baud rate: 921600 (maximum speed: 3686400 bit/s)
- Data: 8 bits
- Parity: None

- Stop: 1 bit
- Flow control: Hardware (RTS/CTS)

#### *Behaviour in Low Power Mode*

- The module power mode selection is internally managed by the module's software.
- The RTS1 signal can be used by the host as an alternative to RTS0 to wake the module up.

### 2.2.6. UART 2 Interface

**Important:** UART 2 signals should be connected to test points.

#### *Default Configuration*

UART 2 is in console mode by default. The boot log is sent on this interface.

Default serial configuration:

- Baud rate: 115200 (max speed: 115200 bit/s)
- Data: 8 bits
- Parity: None
- Stop : 1 bit
- Flow control: None

#### *Behaviour in Low Power Mode*

UART 2 RTS cannot be used to wake the module from low power modes.

### 2.2.7. UART 3 Interface

**Important:** UART 3 is reserved for future use.

## 2.3. USB

The GC02S1 modules have one USB hardware interface. Once enumerated, the USB interface exposes the following profiles:

- USB CDC_ACM: Data and control from external MCU using AT commands (UART emulation)
- USB CDC_ECM: Data (IP) from external MCU (IP traffic sent on the LTE network)
- USB SFU: Firmware upgrade

The USB profile can be configured to present multiple ACM/ECM interfaces. Please refer to the `AT+SQNUSBCFG`, `AT+BIND` and `AT+SQNHWCFG` commands in the relevant *AT Commands Reference Manual* for more information.

**Note:**

- All `USB CDC_ACM` ports are initially configured in AT mode
- Changes made by the `AT+BIND` command are lost with any subsequent RESET. Persistent changes must use the `AT+SQNHWCFG` command.

**Table 7. USB Pad Details**

| Pad # | Pad Name | Primary Function | Direction | Pad type | Mandatory |
|---|---|---|---|---|---|
| 50 | USB_EXT_VBUS_VLD (WAKE4, see below) | Wake from sleep | In | VBAT | NO |
| 51 | USB_DP | USB In/Out | In/Out | BIDIR | YES |
| 52 | USB_DM | USB In/Out | In/Out | BIDIR | YES |
| 54 | USB_CC1 | USB In/Out | In/Out | BIDIR | NO |
| 56 | USB_CC2 | USB In/Out | In/Out | BIDIR | NO |
| 7 | GPIO11/SPI_CSN2/USBREADY | USBREADY | Output | BIDIR | NO |

Refer to Table 23 *(on page 30)* and Table 24 *(on page 30)* for electrical max. values.

**Important:** The USB_CC1 and USB_CC2 pins need not be connected for the interface to work properly.

**Important:** Pin 7 (USBREADY) is an optional pin that can be used to wake the host up in case the USB controller doesn't support remote suspend/resume. When the module has pending data to deliver in its output buffer, it uses the `USBREADY` signal (see Table 15 *(on page 22)*) to wake up the host.

**Important:** `USB_EXT_VBUS_VLD` is internally connected to `WAKE4`, which is disabled by default. Enabling `WAKE4` is done using the `AT+SQNHWCFG` command (see the *AT Commands Reference Manual LR 9.0*).

### USB Example Schematics

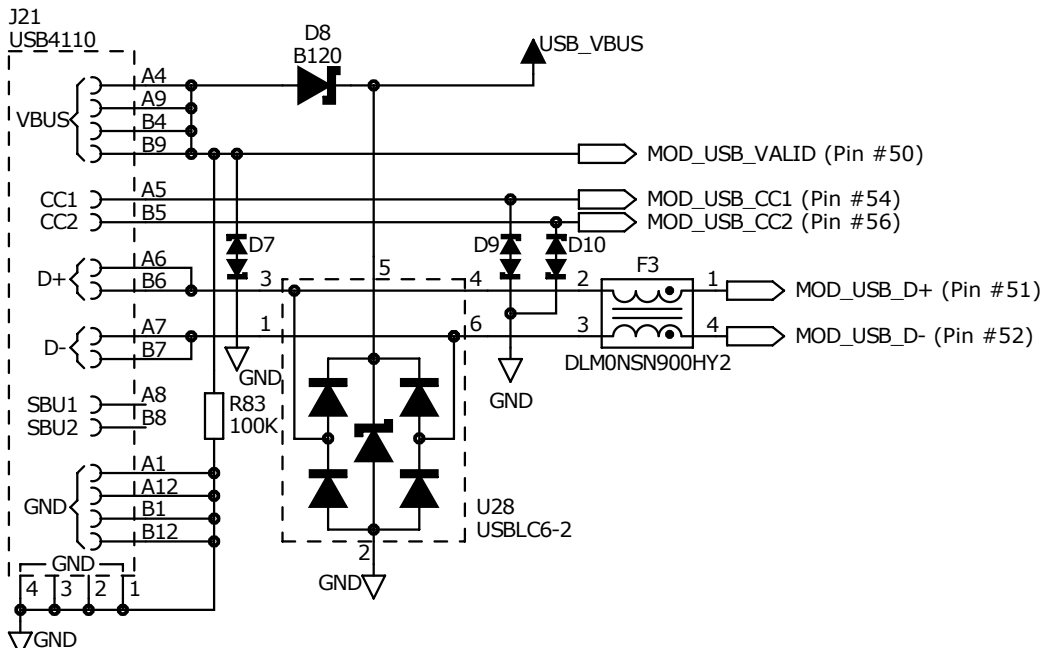



Figure 4. USB Wiring

### USB and UART Availability for Built-in Software Services

The UART/USB interfaces of the GC02S1 are used by different built-in service providers. Table details the interfaces available to the different services bundled with the standard software releases issued by Sequans. If interface and service are compatible, the corresponding cell is filled with a 'x', otherwise it is left blank.

**Table 8. Interface Availability vs Software Service**

| SERVICE | UARTx | USB_ACMx | USB_ECM |
|---|---|---|---|
| PPP | x | x | |
| AT Commands | x | x | |
| MUX | x | | |
| Console | x | x | |
| SFU Upgrade | x | x | |
| Debug (DM Tool) | x | x | |

**Note:**

1. Only one CDC_ECM interface is available, but this interface supports VLAN (multiplexed IP channels)
2. ECM is exclusive to every other data access protocol. When ECM is enabled with the `AT+SQNHWCFG` command, PPP and the internal IP stack are unavailable.

## 2.4. USIM Interfaces

### *SIM0 Interface*

This is the main external SIM interface. It can be used with removable or soldered SIM chips. The modem manages the SIM's power supply to keep the power budget as low as possible.

**Important:** Both SIM0 and SIM1 interfaces use 1.8 V signalling.

**Important:** The SIM0_DETECT signal is optional. When wired, it is active high. Its polarity is **NOT** configurable.

**Table 9. SIM0 Signals**

| Pad # | Pad Name | Direction | Pad type [4] | Voltage | Drive [5] Strength | Reset State | Comment |
|---|---|---|---|---|---|---|---|
| 42 | SIM0_CLK | Out | BIDIR | 1.8 V | T to H | Out-0, T | Main SIM |
| 45 | SIM0_DETECT [6] | In | IN | VBAT | N/A | High-Z | Main SIM |
| 44 | SIM0_IO | In/Out | BIDIR | 1.8 V | T to H | High-Z, T | Main SIM |
| 43 | SIM0_RSTN | Out | BIDIR | 1.8 V | T to H | Out-0, T | Main SIM |
| 73 | SIM0_VCC [7] | Out | SUPPLY | 1.8 V | T to H | Out-0, T | Main SIM |

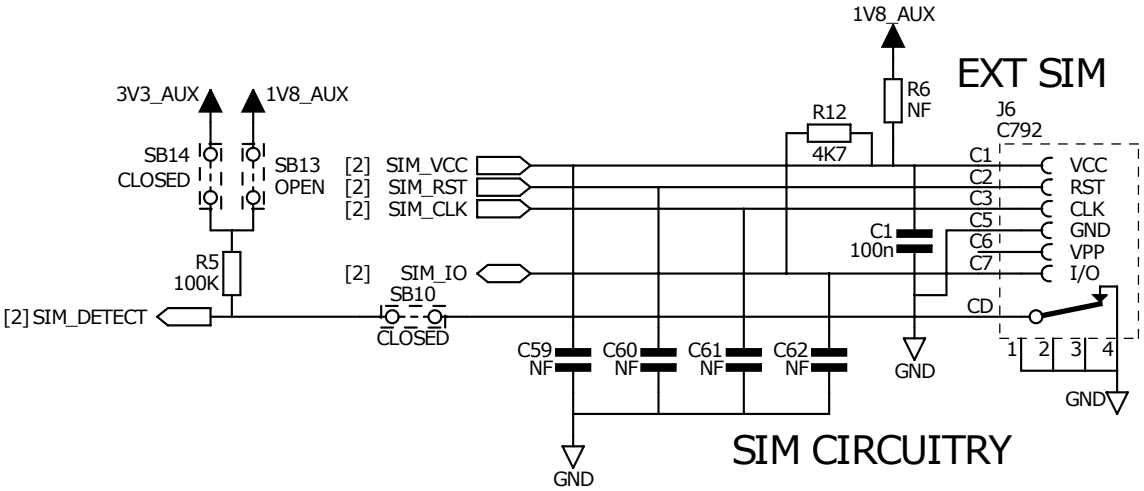



Figure 5. Example of External SIM Interfacing

### *SIM1 Interface*

This GC02S1 's interface to a second SIM is typically dedicated to soldered SIM chips (neither SIM detect nor SIM VCC are provided). The soldered SIM can be powered from the VBAT signal using a DC/DC regulator, if need be. If the board uses a single SIM, it should be connected to the main SIM interface (see Section SIM0 Interface *(on page 18)* above).

4. USIM pad types electrical characteristics are detailed in Table 23 *(on page 30)* and Table 24 *(on page 30)*.
5. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.
6. SIM0_DETECT can be configured as a WAKE pin via software command.
7. See range of values in Table 20 *(on page 27)*.

**Table 10. SIM1 Signals**

| Pad # | Pad Name | Primary Function | Alternate[8] Function | Direction | Pad Type[9] | Voltage | Drive[10] Strength | Reset state |
|---|---|---|---|---|---|---|---|---|
| 40 | GPIO26/SIM1_CLK | GPIO26 | SIM1_CLK | Out | BIDIR | 1.8 V | T to H | Out-0, T |
| 41 | GPIO27/SIM1_-RESETN | GPIO27 | SIM1_-RESETN | Out | BIDIR | 1.8 V | T to H | Out-0, T |
| 39 | GPIO25/SIM1_IO | GPIO25 | SIM1_IO | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |

### *Other Hardware Considerations*

- Use a 100 nF decoupling capacitor on SIM_VCC
- Use a 4.7 kΩ pull-up resistor between SIM_VCC and SIM_IO
- The SIM connector should be located as close as possible to the GC02S1
- Please ensure ground continuity between the SIM card and the GC02S1
- If the application handles SIM card hot swapping, the SIM slot must contain a card detector in order for the software to process the event immediately. Default software configuration is to support SIM_DETECT
- If the SIM card tray does not support SIM_DETECT (not recommended), keep the SIM_DETECT signal high and configure the module for SIM card detection using polling mode

## 2.5. I²C

**Table 11. I²C Pad Details**

| Pad # | Pad Name | Primary Function | Alternate[11] Function | Direction | Pad type[12] | Voltage | Drive[13] Strength | Reset State |
|---|---|---|---|---|---|---|---|---|
| 95 | GPIO23/I2C_SDA | GPIO23 | I2C_SDA | In/Out | BIDIR | 1.8 V | T to M | High-Z |
| 97 | GPIO24/I2C_SCL | GPIO24 | I2C_SCL | In/Out | BIDIR | 1.8 V | T to M | High-Z |

**Note:** Both I2C_SDA and I2C_SCL must be pulled up with a 100 kΩ resistor tied to an external power supply.

**Note:** I²C is not yet software supported. It is reserved for future use.

8. Alternate functions will be available in future versions via SW upgrade.
9. Pad types electrical characteristics are detailed in Table 23 *(on page 30)*.
10. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.
11. Alternate functions will be available in future versions via SW upgrade.
12. I²C pad types's electrical characteristics are detailed in Table 23 *(on page 30)*.
13. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

## 2.6. PCM/I²S

**Table 12. PCM Pad Details**

| Pad # | Pad Name | Primary Function | Alternate Function[14] | Direction | Pad type[15] | Voltage | Drive Strength[16] | Reset State |
|---|---|---|---|---|---|---|---|---|
| 96 | GPIO4/PCM_CLK | GPIO4 | PCM_CLK | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 98 | GPIO3/PCM_RXD | GPIO3 | PCM_RXD | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 99 | GPIO5/PCM_FS | GPIO5 | PCM_FS | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 100 | GPIO6/PCM_TXD | GPIO6 | PCM_TXD | In/Out | BIDIR | 1.8 V | T, L | High-Z |

**Note:** PCM/I²S is not yet software supported. It is reserved for future use.

## 2.7. SPI

**Table 13. SPI Pad Details**

| Pad # | Pad Name | Primary Function | Alternate Function[17] | Direction | Pad type[18] | Voltage | Drive Strength[19] | Reset state |
|---|---|---|---|---|---|---|---|---|
| 3 | GPIO7/SPI_SDI | GPIO7 | SPI_SDI | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 4 | GPIO8/SPI_SDO | GPIO8 | SPI_SDO | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 2 | GPIO9/SPI_CLK | GPIO9 | SPI_CLK | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 5 | GPIO10/SPI_CSN1 | GPIO10 | SPI_CSN1 | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 7 | GPIO11/SPI_-CSN2/USBREADY | GPIO11 | SPI_-CSN2/USBREADY | In/Out | BIDIR | 1.8 V | T, L | High-Z |

**Note:** SPI is not yet software supported. It is reserved for future use.

## 2.8. GPIO

31 GPIOs are available on the GC02S1: the first 27 are named GPIO1 to GPIO27 and the last five GPIO31 to GPIO35 (GPIO32 corresponds to the $\overline{\text{RESET}}$ signal is and therefore unavailable). The GPIOs are documented in this data sheet based on their shared or assigned function.

| Pin | Functions | Primary Function | Alternate | Dir. | Pad Type | Voltage | Drive Strength[20] | Reset |
|---|---|---|---|---|---|---|---|---|
| 12 | GPIO1/STATUS_LED | STATUS_LED | GPIO1 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Status LED (STATUS_LED, OUT). On when the module is attached to the network, blinks during data transmission. | | | | | | |

14. Alternate functions will be available in future versions via SW upgrade.
15. PCM pad types's electrical characteristics are detailed Table 23 *(on page 30)*.
16. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.
17. Alternate functions will be available in future versions via SW upgrade.
18. SPI pad types' electrical characteristics are detailed in Table 23 *(on page 30)*.
19. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.
20. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

| Pin | Functions | Primary Function | Alternate | Dir. | Pad Type | Voltage | Drive[20] Strength | Reset |
|---|---|---|---|---|---|---|---|---|
| 13 | GPIO2/PS_STATUS | PS_STATUS | GPIO2 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Power Saving status (PS_STATUS, OUT) enabled by default. Active high. | | | | | | |
| 98 | GPIO3/PCM_RXD | GPIO3 | PCM_RXD | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 96 | GPIO4/PCM_CLK | GPIO4 | PCM_CLK | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 99 | GPIO5/PCM_FS | GPIO5 | PCM_FS | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 100 | GPIO6/PCM_TXD | GPIO6 | PCM_TXD | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 3 | GPIO7/SPI_SDI | GPIO7 | SPI_SDI | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 4 | GPIO8/SPI_SDO | GPIO8 | SPI_SDO | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 2 | GPIO9/SPI_CLK | GPIO9 | SPI_CLK | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 5 | GPIO10/SPI_CSN1 | GPIO10 | SPI_CSN1 | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 7 | GPIO11/SPI_-CSN2/USBREADY | GPIO11 | SPI_-CSN2/USBREADY | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 36 | GPIO12/TXD0 | TXD0 | GPIO12 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| 34 | GPIO13/RXD0 | RXD0 | GPIO13 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 35 | GPIO14/ CTS0 | CTS0 | GPIO14 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 28 | GPIO15/TXD2 | TXD2 | GPIO15 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| 26 | GPIO16/RXD2 | RXD2 | GPIO16 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 27 | GPIO17/ CTS2/ DCD0 | GPIO17 | CTS2/ DCD0 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 25 | GPIO18/ RTS2/ DSR0 | GPIO18 | RTS2/ DSR0 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| 24 | GPIO19/TXD3 | GPIO19 | TXD3 | In/Out | BIDIR | 1.8 V | T to H | HighZ, T |
| 22 | GPIO20/RXD3 | GPIO20 | RXD3 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 21 | GPIO21/ CTS3 | GPIO21 | CTS3 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 23 | GPIO22/ RTS3 | GPIO22 | RTS3 | In/Out | BIDIR | 1.8 V | T to H | Out-1, T |
| 95 | GPIO23/I2C_SDA | GPIO23 | I2C_SDA | In/Out | BIDIR | 1.8 V | T to L | High-Z |
| 97 | GPIO24/I2C_SCL | GPIO24 | I2C_SCL | In/Out | BIDIR | 1.8 V | T to L | High-Z |
| 39 | GPIO25/SIM1_IO | GPIO25 | SIM1_IO | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| 40 | GPIO26/SIM1_CLK | GPIO26 | SIM1_CLK | Out | BIDIR | 1.8 V | T to H | Out-0, T |
| 41 | GPIO27/SIM1_-RESETN | GPIO27 | SIM1_RESETN | Out | BIDIR | 1.8 V | T to H | Out-0, T |
| 19 | GPIO31/PWM0/ PULSE0/ 19M2_-CLK_OUT | GPIO31 | PWM0/ PULSE0/ 19M2_CLK_-OUT | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 9 | GPIO33/TX_IND | TX_IND | GPIO33 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |

20. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

| Pin | Functions | Primary Function | Alternate | Dir. | Pad Type | Voltage | Drive[20] Strength | Reset |
|---|---|---|---|---|---|---|---|---|
| | | Primary Function: Transmission indicator (TX_IND, OUT): high when the output power exceeds a configurable threshold. | | | | | | |
| 10 | GPIO34/ANT_-TUNE0 | ANT_TUNE0 | GPIO34 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Antenna tuning (ANT_TUNE0, OUT) | | | | | | |
| 11 | GPIO35/ANT_-TUNE1 | ANT_TUNE1 | GPIO35 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Antenna tuning (ANT_TUNE1, OUT) | | | | | | |

In addition to the GPIOs, five WAKE signals are available, documented in Other Signals *(on page 22)*.

## 2.9. Other Signals

### *General Information*

**Table 14. GND and DNC pads**

| Pads Type | Pads Number |
|---|---|
| GND | 1, 6, 37, 38, 58, 59, 61, 64, 65, 71, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 91, 92, 93 |
| DNC (Reserved) | 14, 15, 17, 18, 53, 74, 75, 76, 77, 94 |

**Table 15. Other Signals (No Interface)**

| Pad # | Name | Primary Function | Alternate[21] Function | Direction | Pad Type[22] | Voltage | Drive[23] Strength | Reset State |
|---|---|---|---|---|---|---|---|---|
| 72 | ADC1 | ADC1 (see below) | N/A | In | IN | 1.8 V | N/A | N/A |
| | | Analogue to Digital Converter (ADC, IN) | | | | | | |
| 12 | GPIO1/STATUS_LED | STATUS_LED | GPIO1 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Status LED (STATUS_LED, OUT). On when the module is attached to the network, blinks during data transmission.<br><br>An AT command sets it active high (1.8 V). Please refer to the *AT Commands Reference Manual*. It is recommended to add a pull down resistor and an inverter or a MOSFET-N to avoid extra power consumption in the deepest power saving mode. | | | | | | |
| 13 | GPIO2/PS_S-TATUS | PS_STATUS | GPIO2 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |

20. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.
21. Functions will be available in future versions via SW upgrade.
22. Pad types' electrical characteristics are detailed in Table 23 *(on page 30)* and Table 24 *(on page 30)*.
23. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

**Table 15. Other Signals (No Interface) (continued)**

| Pad # | Name | Primary Function | Alternate[21] Function | Direction | Pad Type[22] | Voltage | Drive[23] Strength | Reset State |
|---|---|---|---|---|---|---|---|---|
| | | Primary Function: Power Saving status (PS_STATUS, OUT) enabled by default. Active high. Should be connected to a test point for debugging and a 100 kΩ pull-down resistor.<br><br>This pad mirrors the power saving status.<br><br>• High level: the module is active.<br>• Low level: the module is in low power mode.<br><br>When the pad is low the modem requires to be woken up using a WAKE signal such as RTS 0, RTS 1 or a dedicated WAKE. PS_STATUS can also be used to turn unneeded external active circuits (such as RF switches on the antenna path) off while in sleep mode. | | | | | | |
| 19 | GPIO31/PWM0/ PULSE0/ 19M2_-CLK_OUT | GPIO31 | PWM0/ PULSE0/ 19M2_CLK_-OUT | In/Out | BIDIR | 1.8 V | T, L | High-Z |
| 9 | GPIO33/TX_IND | TX_IND | GPIO33 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Transmission indicator (TX_IND, OUT): high when the output power exceeds a configurable threshold (see `AT+SQNHWCFG="txIndicator"` sub-command in the *AT Commands Reference Manual*). | | | | | | |
| 10 | GPIO34/ANT_-TUNE0 | ANT_TUNE0 | GPIO34 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Antenna tuning (ANT_TUNE0, OUT). Can be used to drive an antenna tuning circuit, as described in . | | | | | | |
| 11 | GPIO35/ANT_-TUNE1 | ANT_TUNE1 | GPIO35 | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Primary Function: Antenna tuning (ANT_TUNE1, OUT). Can be used to drive an antenna tuning circuit, as described in . | | | | | | |
| 20 | FFF_FFH | RESERVED | N/A | N/A | BIDIR | 1.8 V | T to H | High-Z, T |
| | | Boot mode selection (FFF_FFH, IN). This pad needs a pull-down resistor by default | | | | | | |
| 46 | EXT_RST_N | EXT_RST_N | N/A | In | IN | VBAT | N/A | In, Pull-up |
| | | Module HW reset signal. Active low. The minimum duration of a reset pulse on the EXT_RST_N signal is 100 µs. A 10 pF decoupling capacitor should be placed as close as possible to this pad. | | | | | | |
| 16 | RING0 | RING0 | N/A | In/Out | BIDIR | 1.8 V | T to H | High-Z, T |
| | | UART0 ring line (RING0, OUT). Enabled by default and active low. Signals the host there are data or URC pending on the UART line. A 100 kΩ pull-up (either on the host input or on the PCB) is recommended as this signal transitions to High-Z when the modem enters deep sleep or shuts down. | | | | | | |
| 48 | WAKE0 | WAKE0 | N/A | In | IN | VBAT | N/A | High-Z |

21. Functions will be available in future versions via SW upgrade.
22. Pad types' electrical characteristics are detailed in Table 23 *(on page 30)* and Table 24 *(on page 30)*.
23. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

**Table 15. Other Signals (No Interface) (continued)**

| Pad # | Name | Primary Function | Alternate[21] Function | Direction | Pad Type[22] | Voltage | Drive[23] Strength | Reset State |
|---|---|---|---|---|---|---|---|---|
| | | Wake #0 input line (WAKE0, IN). Disabled by default. When enabled, a high level wakes the modem up from deep sleep mode. Note: there is no current leakage at low level. | | | | | | |
| 47 | WAKE1 | WAKE1 | N/A | In | IN | VBAT | N/A | High-Z |
| | | Wake #1 input line (WAKE1, IN). Disabled by default. When enabled, a high level wakes the modem up from deep sleep mode. Note: there is no current leakage at low level. | | | | | | |
| 49 | WAKE2 | WAKE2 | N/A | In | IN | VBAT | N/A | High-Z |
| | | Wake #2 input line (WAKE2, IN). Disabled by default. When enabled, a high level wakes the modem up from deep sleep mode. Note: there is no current leakage at low level.<br><br>Can also be used to trigger an emergency shut down (module is shut off without notifying the network) | | | | | | |
| 55 | WAKE3 | WAKE3 | N/A | In | IN | VBAT | N/A | High-Z |
| | | Wake #3 input line (WAKE3, IN). Disabled by default. When enabled, a high level wakes the modem up from deep sleep mode. Note: there is no current leakage at low level. | | | | | | |
| 57 | WAKE4 | WAKE4 | N/A | In | IN | VBAT | N/A | High-Z |
| | | Wake #4 input line (WAKE4, IN). Disabled by default. When enabled, a high level wakes the modem up from deep sleep mode. Note: there is no current leakage at low level. | | | | | | |

### *Analogue to Digital Converter (ADC1)*

The characteristics of the ADC1 pin are given below:

**Table 16. ADC1 Specification**

| Performance Specification | Description | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typical | Max. | |
| Voltage Range | | 0 | | 1.8 | V |
| Tolerance | Input Referred Offset Error | | ± 1 | | % FS |
| Non Linearity | | | | ± 1.5 | LSB |
| Resolution | Effective Number of Bits | | 10 | | bit |
| Dynamic Range | | 71 | | | dB |
| Input Resistance | | 3.5 | 3.9 | | kΩ |
| Input Capacitance | | 1.4 | 1.7 | 2.1 | pF |

21. Functions will be available in future versions via SW upgrade.
22. Pad types' electrical characteristics are detailed in Table 23 *(on page 30)* and Table 24 *(on page 30)*.
23. Drive Strength is programmable. Numerical values are given in table Table 25 *(on page 30)*.

The ADC1 pin can be used either as a general purpose analogue input, or be part of a special application, such as a SWR meter. Don't connect the ADC1 pin if not used (no need for resistive or capacitive termination).

### RING0 Signal

The host MCU has two reasons to monitor the `RING0` line:

- Be warned of a pending URC when the UART is active and in online mode
- Reconnect to the UART to receive URCs and user data

By default, the `RING` line is active low and is asserted when an URC is pending on the UART, whether it is connected or not. It remains low for five seconds. The `RING` line configuration can be modified with the `AT +SQNRICFG` command. The user can decide what event triggers the RING line and how long it remains active.

### WAKE Signals

Several pins of the module can be used as external wake sources: `WAKE0`, `WAKE1`, `WAKE2`, `WAKE3`, `WAKE4` (`USB_EXT_VBUS_VLD`), `RTS0`, `RTS1`. Additionally `USB_DP` and `USB_DM` can be used to wake up the module using a *USB Resume* procedure.

The external wake signals have two different roles:

- If a wake signal is enabled, active and the platform wants to perform a LPM cycle, this wake signal prevents it to enter the low power state.
- If a wake signal is enabled, active and the platform is in low power, this wake signal wakes up the module.

WAKE inputs must last at least 100 µs in order to insure a reliable detection.

The `AT+SQNHWCFG` command can be used to show the wake source configuration and change it. Please refer to the *AT Commands Use Cases* document for more information.

In addition, as mentioned above in table Table 15 *(on page 22)*, the WAKE2 pin can be used for emergency shut down.

### STATUS_LED Signal

The STATUS_LED signal reports when the module is attached to a network. It blinks when the module is transmitting data.

The `AT+SQNHWCFG` command can be used to turn this signal on or off and configure the polarity. Please refer to the *AT Commands Reference Manual* for details on this command.

### PS_STATUS Signal

The `PS_STATUS` (Power Saving Status) signal reflects the module sleep mode. It is high when the module is active and goes low when the module enters sleep mode.

When the host processor does not support UART hardware flow control, monitoring `PS_STATUS` together with AT polling is mandatory to ensure no data sent over the UART interfaces are lost.

`PS_STATUS` can also be used to supply power to antenna switches for dynamic matching, or to power any component that needs to be turned on when the modem wakes up.

### *TX_IND Signal*

The `TX_IND` signal toggles when the module is in TX mode and the radiated power exceeds a programmable threshold. The `AT+SQNHWCFG` command can be used to turn this signal on or off and configure the threshold. Please refer to the *AT Commands Reference Manual* for details on this command.

### *ANT_TUNE Signals*

On small PCBs, it is difficult to design a proper antenna matching circuit for a wide range of frequencies. One option consists in switching between different narrowband antenna matching circuits, according to the active RF band. The configuration command `AT+SQNHWCFG="antennaTuning"` can be used to activate, deactivate and configure the antenna tuning signals `ANT_TUNE0` and `ANT_TUNE1`, which in turn drive RF switches to select the proper matching circuit (please refer to the *AT Commands Reference Manual*). One possible configuration is given in the following table:

**Table 17. Example of antenna tuning configuration**

| | Bands 12, 17 | Bands 2, 4, 5, 66 | All other bands |
|---|---|---|---|
| ANT_-TUNE0 | 0 | 1 | 1 |
| ANT_-TUNE1 | 0 | 0 | 1 |

## 2.10. JTAG

**Table 18. JTAG pads Details**

| Pad # | Pad Name | Primary Function | Voltage | Direction | Pad type [24] | Reset State |
|---|---|---|---|---|---|---|
| 69 | JTAG_TCK | JTAG_TCK | 1.8 V | In | IN | In, Pull-down, Schmitt-trigger |
| 67 | JTAG_TDI | JTAG_TDI | 1.8 V | In | IN | In, Pull-up |
| 68 | JTAG_TDO | JTAG_TDO | 1.8 V | Out | BIDIR | Out, 0 |
| 66 | JTAG_TMS | JTAG_TMS | 1.8 V | In | IN | In, Pull-up |
| 70 | JTAG_TRSTN | JTAG_TRSTN | 1.8 V | In | IN | In, Pull-down |

## 2.11. Antenna

**Table 19. Antenna pad Details**

| Pad # | Pad Name | Direction | Comments |
|---|---|---|---|
| 90 | LTE_ANT | In/Out | Main Antenna, for Rx and Tx |

**Important:** The GC02S1 is designed to work with antennas whose efficiency is at least 40%.

24. JTAG pad types's electrical characteristics are detailed in Table 23 *(on page 30)*.

# 3. Electrical, RF and Thermal Characteristics

## 3.1. Power

### *Power Pads Characteristics*

**Note:** Pad 1V8 is the reference voltage for I/Os. It can be used to provide power to small devices (100 mA maximum usage). **This voltage is not available when the modem is in Deep Sleep mode.** When the modem is in standby the voltage drops to 1.62 V as per Table 20 *(on page 27)*.

**Table 20. Power Pads**

| Pad # | Pad Name | Supply | Direction | Min Value (V) | Typical Value (V) | Max Value (V) |
|---|---|---|---|---|---|---|
| 8 | 1V8 (see Note above) | 1.8 V | Out | 1.62 | 1.8 | 1.98 |
| 73 | SIM_VCC [25] | 1.8 V | Out | 1.62 | 1.8 | 1.98 |
| 60, 62, 63 | VBAT (USB inactive) | N/A | In | 3.2 | 3.8 | 5.5 |
| | VBAT (USB active) | | | 3.3 | | |

### *Power-up Timing*

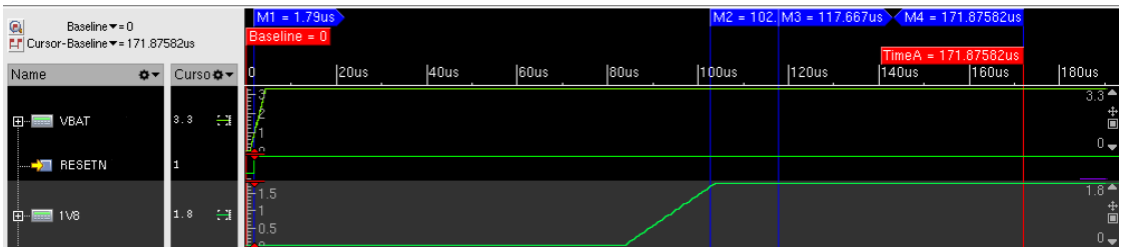



Figure 6. Typical Timing Diagram for Power-Up Sequence

**Important:** The 1V8 power signal can remain low up to 370 µs after the VBAT rising edge.

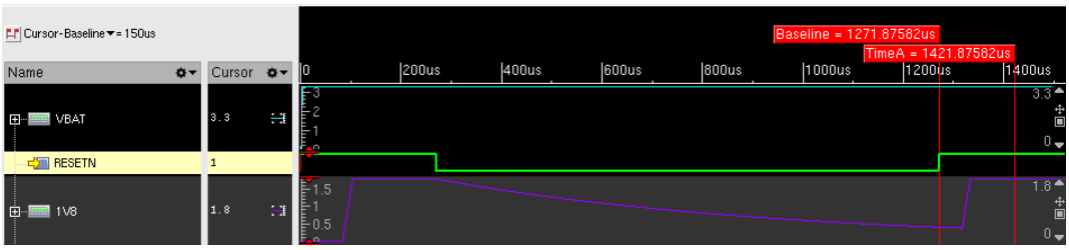



Figure 7. Typical Timing Diagram for Reset Sequence

**Note:** Since RESETN is pulled-up internally, RESETN does not need to be held low after VBAT is established, as shown in Figure 7 *(on page 27)*. There is no timing condition between RESETN and VBAT.

25. See also Section USIM Interfaces *(on page 18)*.

**Note:** RESETN minimum duration for reliable detection is 100 µs.

### Power Down

Module's powering down is typically triggered by the `AT+SQNSSHDN` command. Once the `+SHUTDOWN` URC is received, a small delay must be observed (typically around 1 s) before switching the power off. Failure to observe this delay might result in data loss (unperformed or incomplete Flash writes).

### Power States

Figure 8 *(on page 28)* represents the electrical states of the module and their transitions.

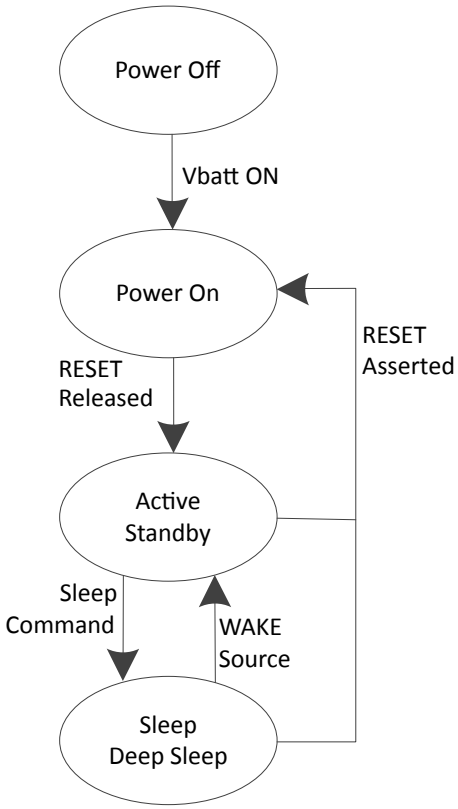



Figure 8. Electrical States and Transitions

Power modes are described in Table 21 *(on page 28)* and illustrated in Figure 8 *(on page 28)*.

**Table 21. Power Modes Description**

| Power Mode | LTE Mode | Available Interfaces |
|---|---|---|
| Active | Connected (RF on) | All interfaces |
| Standby | Connected (RF off) | All interfaces |
| Sleep | RRC Idle | WAKE pins (including RTS0/1) |
| Deep Sleep | radio off, airplane mode | WAKE pins (including RTS0/1) |

### *Pads Voltage per State*

The following table details the typical voltage levels of the 1V8 and SIM_VCC pads when the module is in the following states:

- Active: RF on, connected, all interfaces active
- Standby: RF off, connected, all interfaces active
- Sleep: RRC idle period
- Deep Sleep: radio off, airplane mode

**Table 22. Power Supply Voltages vs. Current Module State**

| State | 1V8 pad typ. level (V) | SIM_VCC pad typ. level (V) |
|---|---|---|
| Active | 1.8 | 1.8 |
| Standby | 1.8 | 1.8 |
| Sleep | 1.6 | 1.6 |
| Deep Sleep | 0 | 0 |

### *Test Points and Measurement Access*

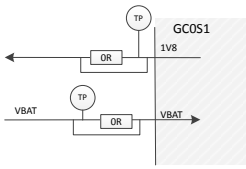



Figure 9. Power Supply System Example

It is recommended to place test points and gaps bridged with 0 Ω SMD resistors on all supply nets to allow for easy voltage and current measurements. The size of the 0 Ω shorting chips should match the width of the supply track, which in turn depends on the current throughput.

## 3.2. Digital I/O Characteristics

This section details the voltage and current characteristics of the various I/O pads of the GC02S1.

The I/Os belong either one of two power groups:

- 1.8 V
- VBAT

The operational voltage range of both power groups is described in Table 23 *(on page 30)* and Table 24 *(on page 30)*.

**CAUTION:** Designers must ensure that the input voltage on any of the I/O pads never exceeds the $V_{IH}$ of the power group they belong to.

**CAUTION:** $V_{OH}$ values in the tables below do not apply to GPIOs configured in open drain mode. When in open drain mode GPIOs either drive the line to $V_{OL}$, or leave it floating, to be pulled up by an external resistance. The PCB designer must ensure that the voltage on these pads never exceeds the $V_{IH}$ value of the I/O group the GPIOs belong to.

See Table 23 *(on page 30)* for the digital I/O characteristics of the different I/O pads. Refer to each interface of the GC02S1 in chapter Interfaces *(on page 10)* for the power group and I/O pad type of each pad. Note that IN pads are inputs only whereas BIDIR can be both inputs and outputs.

**Table 23. DC Ratings for Digital I/Os, 1.8 V, BIDIR and IN Types**

| Symbol | Minimum | Maximum | Unit |
|---|---|---|---|
| $V_{IH}$ Input HIGH level | 1.26 | 3.3 | V |
| $V_{IL}$ Input LOW level | 0 | 0.54 | V |
| $V_{OH}$ Output HIGH voltage | 1.44 | 1.8 | V |
| $V_{OL}$ Output LOW voltage | 0 | 0.36 | V |
| $I_{RPU}$ Input pull-up resistor current | 15 | | µA |
| $R_{RPU}$ Input pull-up resistance | 27 | 34 | kΩ |
| $I_{RPD}$ Input pull-down resistor current | 15 | | µA |
| $R_{RPD}$ Input pull-down resistance | 27 | 34 | kΩ |
| $V_H$ Input hysteresis | 0.18 | | V |
| $I_{PAD}$ Input leakage current, non-tolerant | -1 | 1 | µA |
| $I_{OZ}$ Off-State leakage current | | 1 | µA |

**Table 24. DC Ratings for Digital I/Os, VBAT Type**

| Symbol | Minimum | Maximum | Unit |
|---|---|---|---|
| $V_{IH}$ Input HIGH level | 0.8 | VBAT + 0.6 (max. 5.5) | V |
| $V_{IL}$ Input LOW level | 0 | 0.2 | V |

**Table 25. Max. DC Current Output/Input per Drive Strength Class**

| Drive Strength Class | $I_{OH}$ (mA) | $I_{OL}$ (mA) |
|---|---|---|
| T | 1.1 | 1.11 |
| L | 2.2 | 2.25 |
| M | 4.4 | 4.48 |
| H | 6.6 | 6.72 |

## 3.3. RF Performance

**Important:** For proper operation, the VSWR at the antenna pad must be better than 2:1 in conducted mode and 3:1 in radiated mode. A higher value could result either in poor RF performance, reduced Tx power or increased sideband/harmonic emission levels. Very high VSWRs can permanently damage the power amplifier.

It is recommended to add a DC blocking capacitor in series with the module RF input/output pad (#90).

### *RF Sensitivity for GC02S1-NA2 module*

The figures given below are measured at ambient temperature over a 10-MHz bandwidth.

**Table 26. RF Sensitivity Figures NA2**

| Bands | RF Sensitivity Level (dBm) | 3GPP Limits (dBm) | |
|---|---|---|---|
| | | CAT 1 | CAT 1 bis |
| 25, 2 | -98.5 | -93.5/-95 | -92 |
| 66,4 | -99 | -96.5/-97 | -94 |
| 5 | -99.5 | -95 | -92.5 |
| 12, 17 | -99.5 | -94 | -91 |
| 13 | -99.5 | -94 | -91 |
| 14 | -99 | -94 | -91 |

### *RF Sensitivity for GC02S1-JP/EU2 module*

**Table 27. RF Sensitivity Figures JP/EU2**

| Bands | RF Sensitivity Level |
|---|---|
| All bands | Target: -98 dBm over a 10 MHz channel in typical conditions (ambient temperature) |

### *RF Output Power*

The GC02S1 maximum output power within the recommended operating range (from 3.1 to 5.5 V) is given in Table 28 *(on page 31)*.

**Table 28. RF Max Output Power**

| Bands | Output Power |
|---|---|
| All Bands | 23 dBm ± 1 dB |

# 4. Hardware Design Recommendations

## 4.1. RF Interface

### 4.1.1. Circuit Diagram Example

**Important:** Figure 10 *(on page 32)* must be strictly followed as a topology reference. It is advised to copy the schematics verbatim. This document also describes the imperative layout constraints.

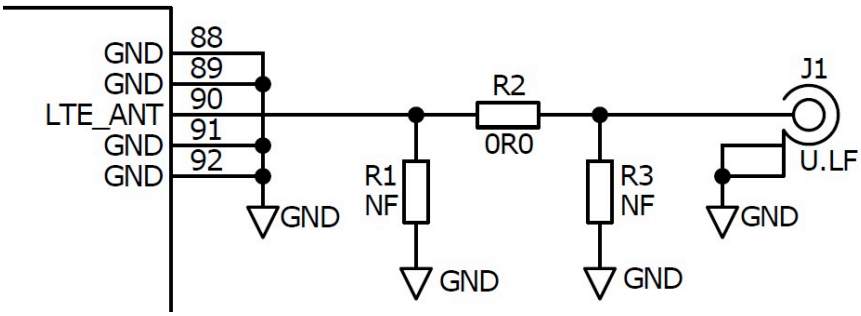



Figure 10. RF Typical Circuit

LTE_ANT is the main antenna pin and serves for both TX and RX signals.

Run a 50 Ω transmission line from this pin to the 50 Ω Primary Antenna/Antenna-connector.

As Figure 10 *(on page 32)* shows, use a π or T-type network for matching, if needed. This document shows π-type networks, but T-type are equally acceptable.

See Antennas and RF Design Considerations *(on page 32)* for more detail on connecting to these pins and on the π-type matching network and ESD protection.

### 4.1.2. Antennas and RF Design Considerations

#### *General Considerations*

- For optimal RF performance, power tracks should be preferred over power planes.
- RF tracks must always be kept as short as possible.
- Use many ground vias, especially all over ground patches/islands

#### *π-Type Matching*

A 3-component π-type (or T-type) matching network is recommended. The three components of the matching network should be laid out adjacent one to another to minimise the interconnecting tracks' lengths. Use small parts with high Q.

Solder the ground side of the shunt(s) part directly to a ground plane, or use wide and short tracks to minimise the series inductance. The shunt part(s) need not be fitted if matching is unnecessary. The ground plane used for grounding the shunt element(s) of the matching circuit should ideally be the same as the 50 Ω transmission line's reference ground plane.

### ESD Protection

ESD protection is a discretionary requirement and only required if necessary, for higher ESD specifications than those of the GC02S1.

It is recommended to select an ESD device with very low parasitic capacitance and a small size (0201) to avoid impacting the RF impedance.

### Standard Impedance Transmission Lines

There are four possible methods to design a 50 Ω transmission line:

1. If the RF track runs on the outer metal layer:
    - Microstrip
    - Coplanar waveguides
2. If the RF track runs on an inner metal layer:
    - Embedded microstrip
    - Stripline

Irrespective of which one is selected:

- Pay attention that the maximum insertion loss between the RF pad and the antenna must be kept under 0.5 dB
- Transmission lines EM fields extend beyond the RF track and couple to adjacent layers:

  For microstrip, the lateral gap running along the track must be at least twice the thickness between the track and its underlying ground plane.

  Both in microstrip and co-planar cases, adjacent metal areas must be present and be properly connected to the main ground plane, so as to terminate the fringing EM fields.

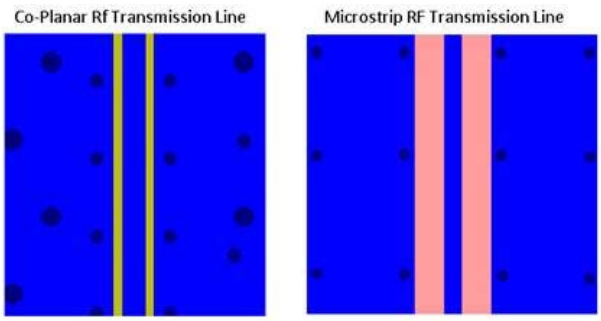



Figure 11. Transmission Line Implementation Examples

Figure 11 *(on page 33)* provides examples of both transmission line implementations, specifically showing:

1. The distance between the transmission line and the side-running grounded area on layer 1.
2. The periodic via connections connecting the top metal layer to the reference GND layer of the transmission line.

- Avoid routing noisy signal tracks along the RF transmission lines to minimize cross-coupling into GC02S1 's RF ports.
- The component pads of the SMD parts used in the 3-component π-type matching circuit are effectively very short transmission lines. To minimise the RF insertion loss ($s_{11}$, VSWR) caused by the width step, use tapered ends.

### *ANT_LTE Specific Footprint Design*

The ANT_LTE pad must be considered as a short transmission line whose width is the same as the pad's width. To minimise discontinuity, the ground layer immediately below the pad must be cut out as shown in Figure 12 *(on page 34)* . Use a quasi-static (in coplanar wave mode) or full-wave EM simulator to compute the extent of the underlying ground area that needs to be removed in order to reach the 50 Ω goal impedance. The recommended clearance between the ANT_LTE pad and the ground plane underneath is 200 µm.

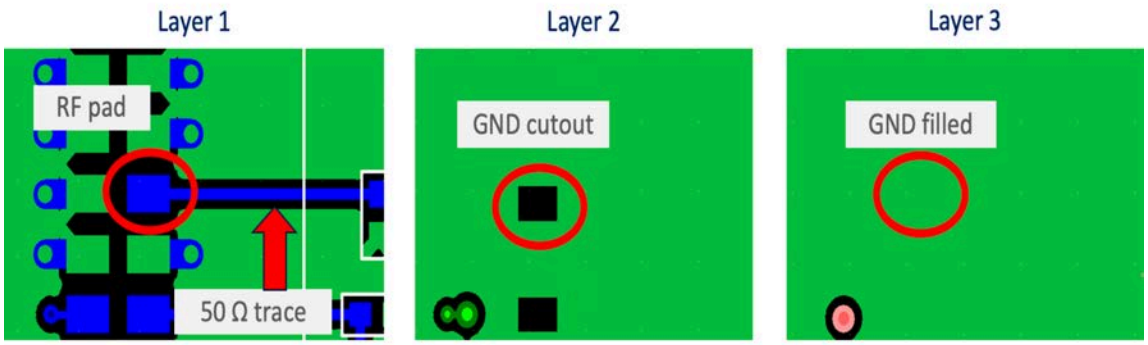



Figure 12. ANT_LTE Pad Design

Because the RF pad is not located on the edge of the module, the section of the RF track that lies under the module must run straight out and be orthogonal to the module's edge.

## 4.1.3. Antenna Matching Circuitry

The GC02S1 supports antenna matching. An example implementation is provided in Calliope 2 reference design that uses two switches and an inverter. Signal matching uses the ANT_TUNE0 and ANT_TUNE1 signals as shown on Figure 13 *(on page 34)*.

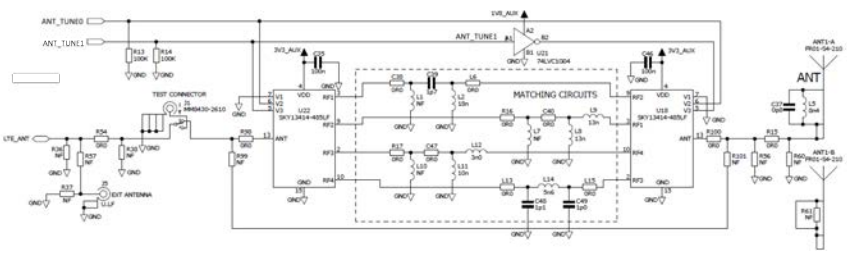



Figure 13. Antenna Matching in Reference Design Schematics

In this implementation, the switches and the inverter are always on. To improve the power consumption, use PS_STATUS to turn the power supply of both switches and the inverter either on or off, as illustrated in Figure 14 *(on page 35)*, where the external ICs are switched off when the module is in low power mode.

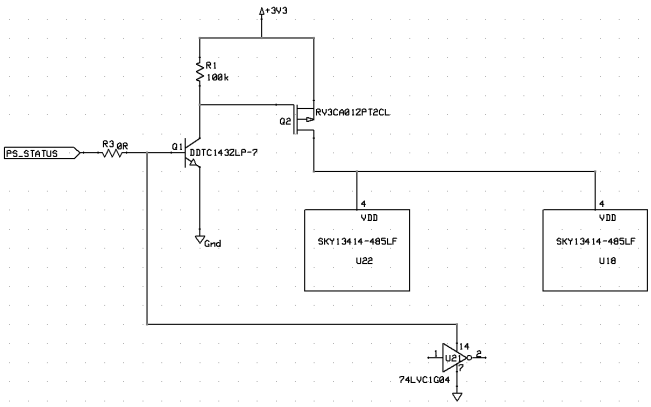



Figure 14. Power Enable Control for Switched and Inverter

### 4.1.4. Test Points and Measurement Access

Engineering and Production teams need 50 Ω termination points, for example J1 in Figure 10 *(on page 32)*, for the assessment of the RF performance.

It might be needed to check the RF path and/or optimise the π-type matching network. This involves measurements from the pin #90 (LTE_ANT) down to the 50 Ω RF connector. To carry out measures at the pin 90, a coaxial cable (usually Ø 1.25 mm semi-rigid) can be attached to it. It is crucial that a grounded area be available on the top layer next to LTE_ANT (GND pads are typically sufficient) to ensure good RF ground continuity and provide strong mechanical attachment of the coaxial cable itself.

Please refer to Antennas and RF Design Considerations *(on page 32)* for more detail on RF track design.

## 4.2. PCB Layout Rules

This section provides general PCB layout good practices.

### 4.2.1. Placement

Place all the major components blocks before routing any section of the PCB design. Specifically:

- The GC02S1 module itself
- The RF interface

Initial placement of these parts allows assessment of the PCB floor layer usage and prevents significant changes to final routed areas of the design, should a placement issue be found. It also provides an opportunity for Sequans to review the PCB.

During the placement:

1. Keep the tracks in the same quadrant than the interface they connect to.
2. Consider orientation to avoid track crossing when routing.
3. Keep the parts as close as possible to the GC02S1 module where possible.
4. Remember that a patch/on-board antenna radiates EM power that can interfere with the proper functioning of the parts located in its vicinity. Keep sensitive devices as far away as possible from the antenna.

5. Place as many ground vias as possible underneath the module in order to insure both excellent electrical grounding and thermal conduction (see section Thermal Considerations *(on page 38)*)
6. Add test points for critical signals such as UART2 and the FFF_FFH pad.
7. Reserve space for pull-ups (especially on UARTs CTS/RTS and SIM interface signals).

### 4.2.2. PCB Layers

Use more layers, for example 6 instead of 4, to increase the freedom in burying and shielding RF traces and noisy signals. A 6-layer PCB design fits the need of an evaluation board that contains many signals, . Conversely, a 4-layer PCB design should implement only a minimal set of signals .

### 4.2.3. Track Design Advice

This section explains some standard design rules applicable to the different types of signals (digital, power supply, RF).

#### *General rules*

- Every track is a potential spurious antenna, especially if open-ended. Never route unneeded signals, and keep the tracks as short as possible
- If a track cannot be shortened, try and bury it.
- Manage a large clearance around RF tracks
- Avoid 'via stubs', use through-hole vias only when connecting tracks running on the top and bottom layers. In all other cases, use blind or micro vias.

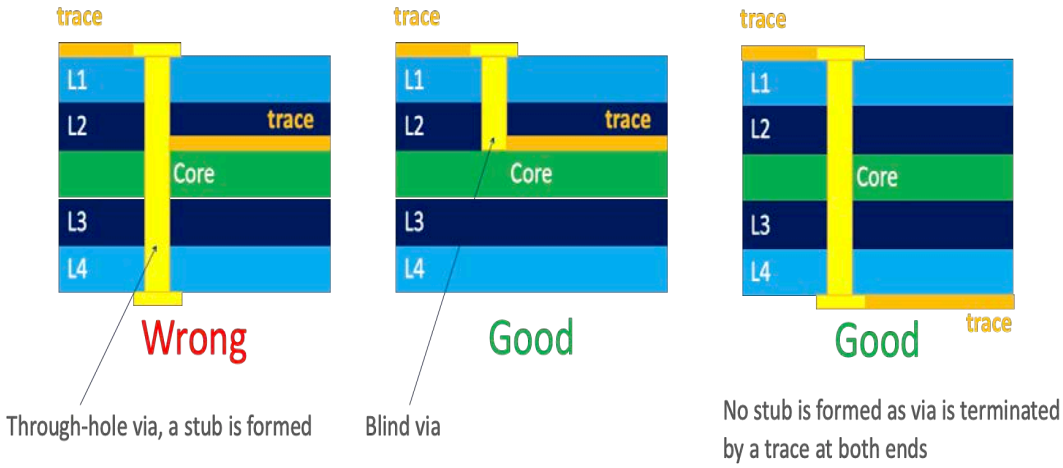



Figure 15. Via manufacturing recommendations

#### *Digital Tracks*

1. Careful and sensible placement of digital signals is required to minimise cross-coupling between tracks.
2. Pay attention to ground currents during routing. Make sure that the grounding surrounding the tracks (from source to load) remains continuous, with no notches or gaps. Long and/or winding ground return currents can create EMI problems.
3. Ensure the tips listed in Section Controlled Impedance Tracks *(on page 38)* are taken into account for digital tracks requiring specific impedance. This is especially the case for USB data tracks (USB_DP /

USB_DM) which require 90 Ω differential impedance, with shielded ground planes in adjacent layers (shielded coplanar type tracks).

4. Keep digital tracks with no impedance needs thin to avoid a buildup of capacitance, while keeping them within manufacturing constraints.
5. If tracks are routed one atop the other, keep them orthogonal. Alternate layer tracks' direction to minimise cross-coupling.
6. Important recommendations related to SIM connector placement can be found in the section SIM Recommendations *(on page 19)* .
7. Shield the clock signal vias.
8. The top and bottom layers should be filled with ground planes interrupted with the minimal number of tracks.
9. Bury as many tracks as possible, especially data (UART, etc) and clock tracks. If it is not possible to bury everything, leave only static signals (such as reset, etc) on the external layers.
10. A few signals can be further filtered, although this is not typically necessary. These signals are:
    - 1V8_LTE, with a π filter. The default BOM has a 0R series resistor.
    - All SIM signals, with decoupling capacitors placed as close as possible to the SIM connector (NF by default).
    - The ANT_TUNE lines controlling the antenna switches, with RC filters. The default BOM has a series 0R resistor.
11. The tracks between the SIM connector and the GC02S1 should be kept as short as possible, and away from the antenna.
12. Data and clock signals should be routed as far as possible from the antenna area.

### *Power Supply Tracks*

1. Size the power supply tracks appropriately to provide a low resistance, low impedance source: the recommended width of the VBAT signal must be greater than 1 mm. Pay attention to the number of vias used when routing tracks across multiple layers, as they add spurious series resistance. This is especially true for high current signals such as the PA supply voltage.
2. The decoupling capacitors ground pad of each power supply signal must be connected to the ground return of the source.
3. Keep digital tracks well away from the power supply tracks.
4. Sequans does not recommend power planes for this design.

### *RF Tracks*

1. Avoid burying these tracks as much as possible, because it increases RF losses w/r to top/bottom routing.
2. Keep tracks as short as possible to help reduce RF losses.
3. Try to mitigate impedance discontinuities. Use tapered ends to improve the matching with SMD pads.
4. Ensure the steps provided in Section Controlled Impedance Tracks *(on page 38)* are taken into account when setting the track width.

### *Controlled Impedance Tracks*

- Calculation of tracks width and spacing:

  Use simple RF design tools to compute the track's width based on:

  1. The thickness of the dielectric substrate lying between the RF track and its associated ground plane.
  2. The spacing between the track and the adjacent ground plane (on the same layer).
  3. The dielectric constant of the PCB substrate material.

  Sometimes the required track width is impossible to manufacture. The design must then be altered until feasibility is guaranteed. Possible solutions:

  - Use of a thicker substrate.
  - Moving the reference ground plane further down.

  Please also note that impedance error increases as the track's width narrows (this is due to mechanical tolerances becoming proportionally more noticeable).

- In general:

  1. Careful placement is required to keep RF tracks short and straight.
  2. Do not route RF tracks on buried layers.
  3. Ground planes beneath RF tracks should be continuous.
  4. The ground plane running along the RF tracks should be kept distant enough to not alter the track's impedance.

- RF matching component footprints:

  Use tapering to minimise impedance mismatch at the end of tracks. If the parts are significantly wider than the transmission lines, the ground reference should be lowered.

### *Grounding*

1. RF ground planes should be as large and continuous as possible and not be cut into chunks. Check that strings of signal vias do not inadvertently create slots in ground.
2. Apply ground plane flooding on all layers.
3. Apply extensive via stitching. Make sure to scatter the vias evenly over the ground planes.
4. Use extra vias around sensitive areas such as RF tracks and noisy lines.
5. Stitch tight all along the board edges to create a Faraday's cage.

## 4.2.4. Thermal Considerations

This section summarises important design requirements about thermal dissipation. Unless the board is meant to be used in a cold environment, designing for an efficient thermal flow is critical. The temperature of the module, measured by the embedded thermistor, must always remain within acceptable limits (85 °C), especially when the product operates at its maximum permissible ambient temperature in a closed, not vented box.

### *Module Grounding Pads*

- All Gxx pads must be tied to a large ground plane which serves as a thermal sink
- That ground area below the Gxx pads must be stitched with through vias, which conduct heat towards the opposite side of the board
- Besides, adding blind vias surrounding the Gxx pads area help spread the heat flow evenly amongst layers
- If a metal casing is used, it should ideally be in tight contact with the bottom ground layer so as to serve as a terminal heat sink
- If these measures cannot be implemented, or do not suffice, additional elements such as heat sinks, fans or thermal grease (GapPad™) can be used.

## 4.2.5. Example of a 6-Layer PCB Design

This section details an example of a 6-layer PCB design.

> **Attention:** CAVEAT: SIM and JTAG connectors ought to be placed opposite the antenna side and closer to the module.

1. Top Layer
   - Reserved for RF signals. As few other signals as possible. The rest is a ground plane without islands.

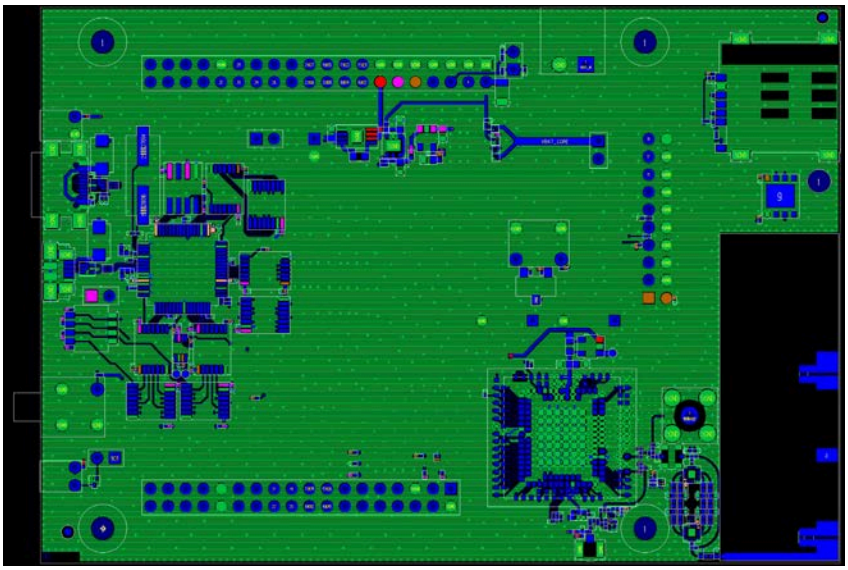


Figure 16. Top Layer View

2. Layer 2
   - Ground plane, no signal
   - Vias are evenly distributed across the surface

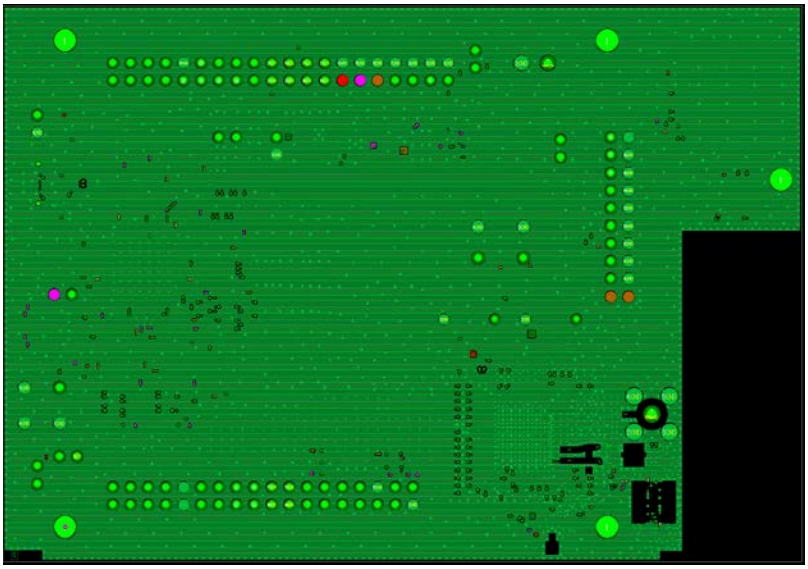


Figure 17. Layer 2 View

3. Layer 3
    - Power traces
    - The remaining space is flooded with ground with proper stitching and even via distribution

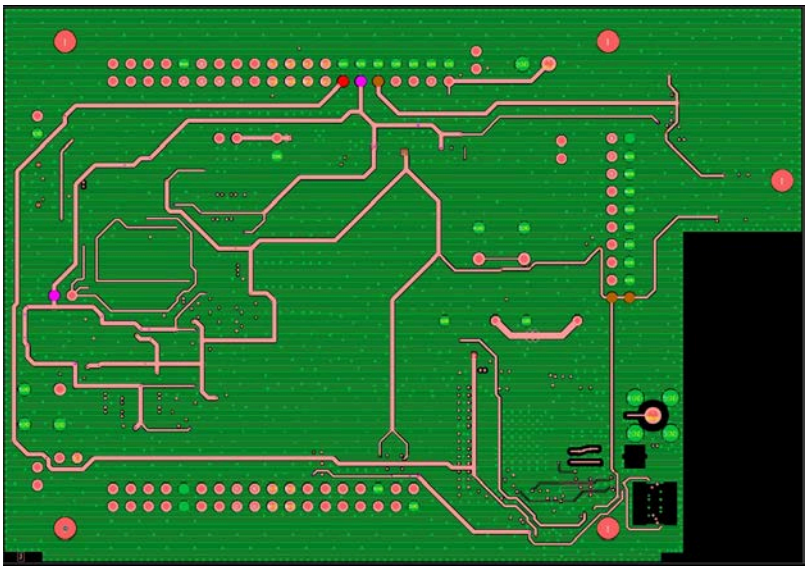


Figure 18. Layer 3 View

4. Layer 4
    - Signal layer
    - All signals are routed vertically on this plane, if possible
    - The remaining space is flooded with ground with proper stitching and even via distribution

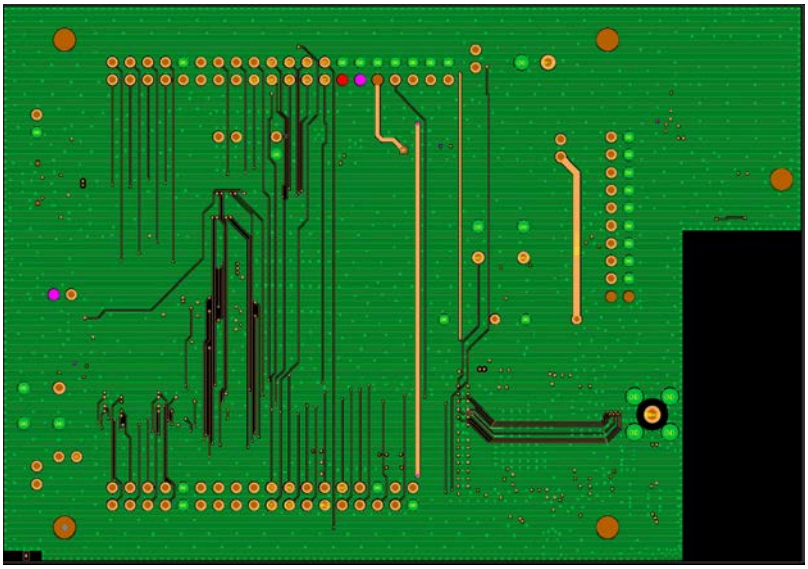


Figure 19. Layer 4 View

5. Layer 5
    - Signal layer
    - The signals are routed horizontally, to minimise cross-coupling with layer 4
    - When this is not possible, precautions are taken to ensure that no layer 4 signal runs atop a layer 5 track
    - The remaining surface is flooded with ground with proper stitching and even via distribution

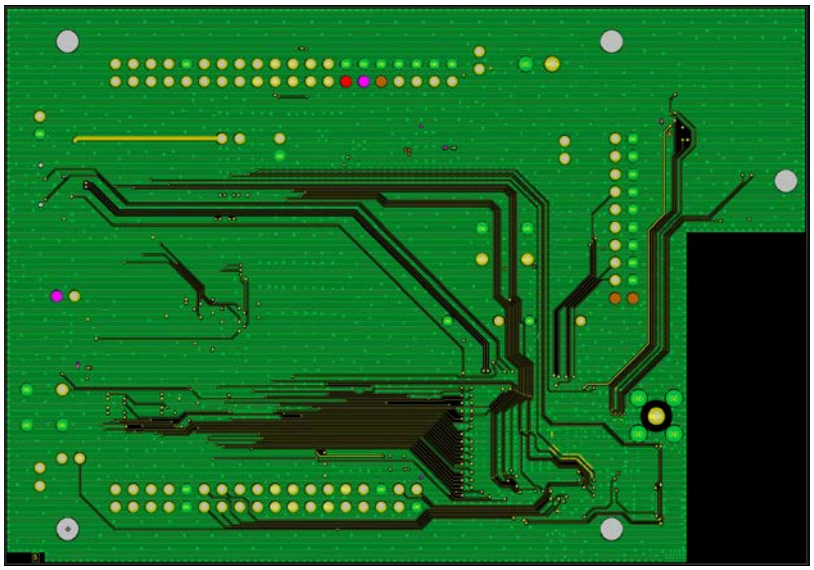


Figure 20. Layer 5 View

6. Bottom Layer
    - Minimal signal traces
    - Ground plane flooding with a lot of ground stitching (in green)
    - The red colour represents 5V0_USB, pink 3V3_AUX, orange 1V8_AUX

- Vias are evenly distributed across the surface
- Tight stitching around the board edges (Faraday's cage)

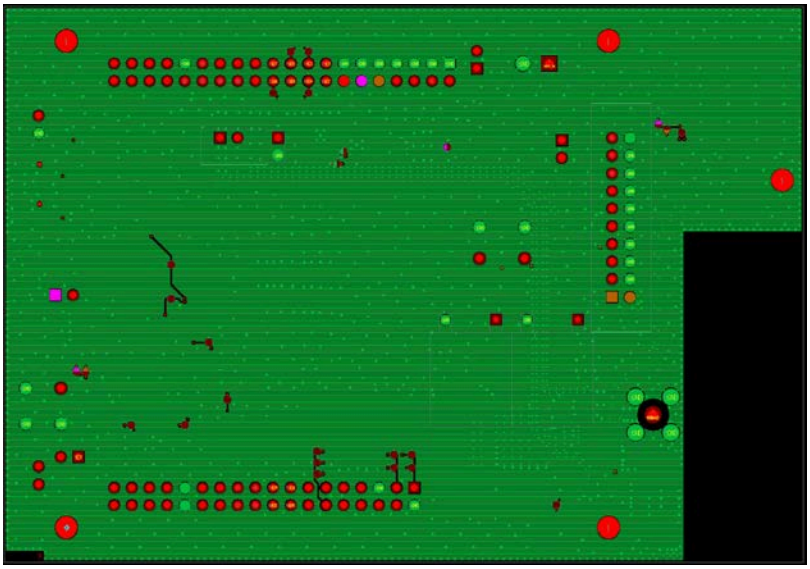


Figure 21. Bottom Layer View

Signals are transferred from the module pads (L1/blue) to the other layers as close as possible using blind and buried vias. Many ground vias are used below the module and around the module to ensure a proper return path to the main ground plane on L2, and aid in thermal dissipation.

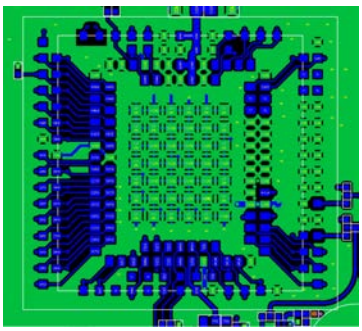


Figure 22. Module Pads (in Blue) on the Top Layer

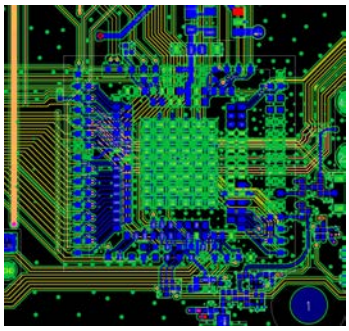


Figure 23. Internal Signals on Layer 4 and 5.

Even if all traces are buried between ground planes, clock signals are also shielded with ground strips. This can be seen on Layer 5, cf. Figure 24 *(on page 43)*.

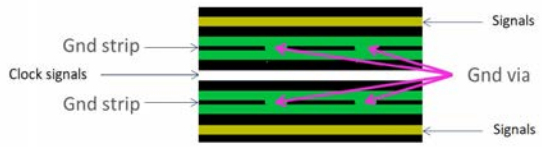



Figure 24. Shielding Clock Signals with Ground Strips

## 4.3. Hardware Test Preparation

### 4.3.1. LTE RF Test Preparation

To ensure that the RF test platform provides the most reliable interface for testing, the following setup is recommended for measuring RF characteristics of the GC02S1 system.

The shield box cavity is configured as shown on Figure 25 *(on page 43)*:

- The DUT is connected to the computer using the UART 1.
- The DUT is also connected by one RF cable.

**Important:** It is paramount that RF tests be conducted in a shield box, away from external RF sources. Please also make sure that no cable runs above or below the device under test.

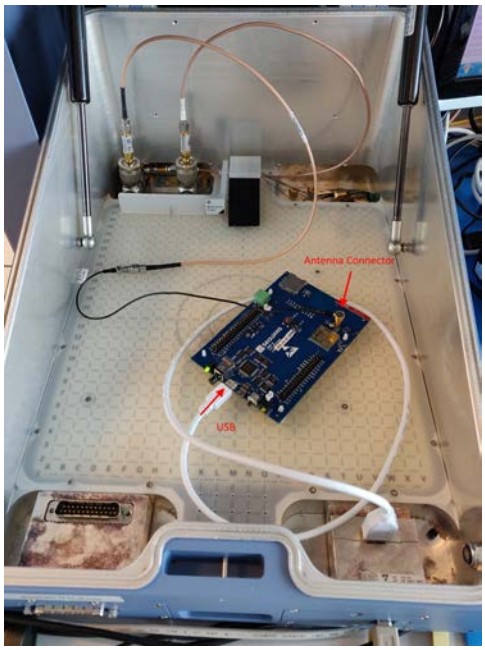



Figure 25. Shield Box Cavity View

Figure 26 *(on page 44)* shows the required configuration for calibration and screening. It consists of:

- 1 x ZN2PD2-50-S + power splitter if the signal analyser and the signal generator are two distinct equipments. R&S® CMW100 or CMW500 for instance allow the use of a single bidirectional RF port and obviate the need for a power splitter.
- 1 x RF cable to the MXA (if needed)

- 1 x RF cable to the MXG (if needed)
- 1 x RF cable to the DUT (in the shield box)

Figure 26. Configuration for Calibration and Screening

### 4.3.2. USB and Power Interfacing

A customer board must provide a mean to connect GC02S1 USB data interface to a laptop/desktop, while disconnecting it from the on-board host processor (if any) on customer's board. This is mandatory to bring-up GC02S1 and start RF tests.

A rewiring of the USB connector is required to provide power to the GC02S1 board.

The aim of this rework is to avoid any laptop power supply issue by using an external power supply on Vbus.

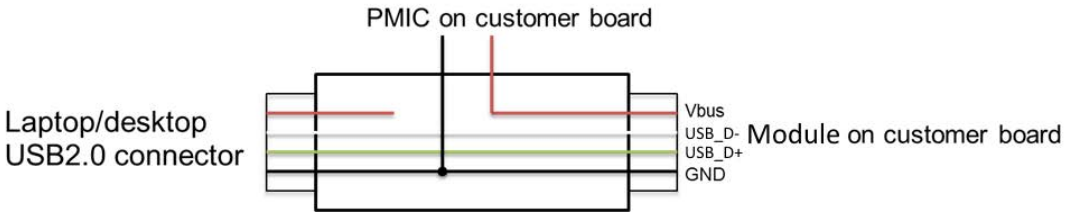



Figure 27. USB Rework Description

The rework procedure is:

- Disconnect GC02S1 USB data pads (USB_D+ / USB_D-) from on-board host
- Connect them to the USB 2.0 connector of an external laptop/desktop
- GND shall be connected to customer board and laptop/desktop
- Vbus comes from either an External Power Supply unit of local GC02S1 host Supply

## 4.4. Bring-Up and Testing

### 4.4.1. Introduction

The purpose of this chapter is to describe board bring-up, test and qualification.

The expectations at this stage are:

1. Any inconsistent and potentially hazardous manufacturing faults must be eliminated.
2. Clearance to proceed with further detailed calibration and measurements.
3. Evaluate the board's performances.

### 4.4.2. Prerequisites

Hardware Qualification consists of:

- Checking for RF losses between the GC02S1 RF ports and the board's RF output
- A sanity check of the connections to the GC02S1
- Debugging, if necessary

Hardware Qualification procedures make use of:

1. An external Host PC / Laptop for monitoring the UART 1 interface

   **Note:** Detailed information will be provided in a future revision of this document.

2. LTE RF test equipment:
   a. A shielding box to avoid any RF interference caused by the environment
   b. RF components such as: cables, splitters, 50 Ω dummy loads
3. A power supply with ammeter

### 4.4.3. Power Supply

#### *Test Procedure*

Figure 28 *(on page 45)* presents the necessary equipment and the configuration to perform the power supply test.

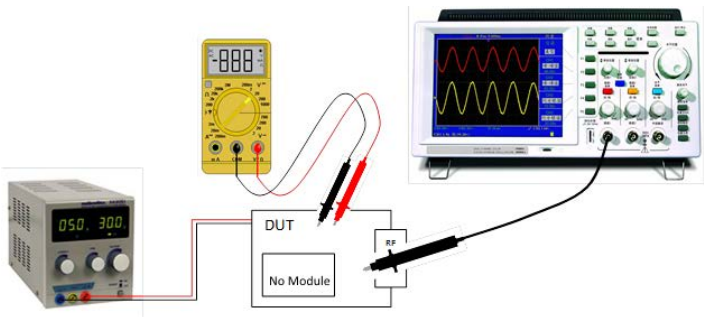



Figure 28. Pre-Test Configuration (No Module on Board)

Test voltage values: test the voltage delivered by the power supply with an oscilloscope before connecting the DUT. The voltage level must be correct and ripple-free. Once this is checked, the DUT can be powered and the test points' voltages measured with a multimeter. At this stage, only VBAT1 can be tested.

Check at each voltage test point, as illustrated on Figure 29 *(on page 46)*, that the voltage value corresponds to what is expected. The value of VBAT1 must be in the range specified in the *GC02S1 Data Sheet*, section *Electrical Operating Conditions*.

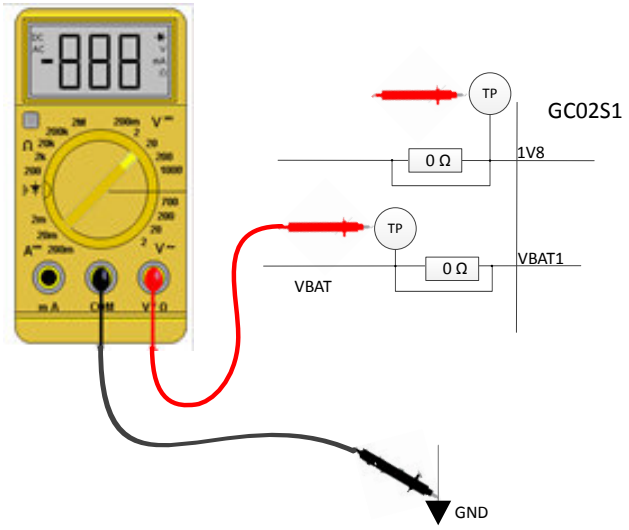



Figure 29. Measuring Voltage Value (GC02S1)

### *Troubleshooting*

If the VBAT1 voltage is incorrect, check any resistor link to detect unexpected short or open circuits.

## 4.4.4. Confirm Module Power-Up Operation (UART 2)

An extract of the output of the OS console on UART 2 port is provided below (boot in FFF mode):

```
[0000000000] boot: Switched to flash, timeout 10000, proto thp
[0000000000] Running on Windbond flash sector 0x1C030000
[0000000000] RBBombyx 11.11@50892 '8.0.0.0 [50892]'
[0000000004] Reset cause 'BUTTON' (real 'BUTTON') (bootWDG : '0') [rawRst '0x00000001']
[0000000012] regConfig 0x1BBB0BA3@1
[0000000015] boot: Current flash, timeout 10000, proto thp
[0000000020] boot: FFF mode
[0000000179] elf: ELF format selected
[0000000183] elf: Header finished
[0000000186] elf: Waiting for 480 bytes
[0000000189] elf: PH 0x00333DE0, 28 bytes
[0000000193] elf: Note 0x63727A04
[0000000196] elf: PH 0x00000000, 20 bytes
[0000000200] elf: Note 0x4D415000
[0000000203] elf: PH 0x00001000, 86 bytes
[0000000207] elf: PH 0x00001060, 1920 bytes
[0000000210] elf: PH 0x000017E0, 119824 bytes
[0000000218] elf: PH 0x0001EBF0, 8 bytes
[0000000221] elf: PH 0x0001EBF8, 56 bytes
[0000000225] elf: PH 0x0001EC30, 100 bytes
[0000000229] elf: PH 0x0001EC94, 624 bytes
[0000000233] elf: PH 0x0001EF04, 2676 bytes
[0000000237] elf: PH 0x00336000, 32 bytes
[0000000240] elf: PH 0x00710000, 196656 bytes
[0000000249] elf: PH 0x00750000, 129576 bytes
[0000000257] elf: PH 0x007A0000, 325728 bytes
[0000000269] elf: PH 0x00334000, 8192 bytes
[0000000273] elf: Program Header finished
[0000000277] sbp: no ACPU found
[0000000280] sbp: MCPU Booting at 0x1C1002F0...
fs: Mounting /flash0...done
fs: Overlay filesystem mounted on /fs
[USIM] PSI USIM rev = 2
[USIM] Default slot=0 itf=0 OK
[USIM] ITF(0) slot(0) enabled(1) polling(0)
[USIM] ITF(1) slot(0) enabled(0) polling(0)
[USIM] ITF(2) slot(0) enabled(0) polling(0)
>INFO> DCP : Init over='serial'
eem: Memory initialized
#WARN# ATF : can't find device related to id=4!
[PSP] initializing
fs: Mounting upgrade filesystem ...
fs: Mounting done
QKI pools init...done
rrcInitCallbacks 440
RrcPersistEco - error: 'rootFsDir' is unresolved
```

```
feeds: 510 Configure enter EAPPS
feeds: 520 Configure leave EAPPS
feeds: 520 Configure enter MQTT
feeds: 520 Configure leave MQTT
feeds: 530 Init enter EAPPS
feeds: 560 Init leave EAPPS
feeds: 560 Init enter LWM2M
feeds: 560 Init leave LWM2M
feeds: 560 Init enter MQTT
feeds: 560 Init leave MQTT
feeds: 560 Init enter SQNSMS
feeds: 570 Init leave SQNSMS
[PSP] initialized
[PSP] starting
reserved room 7/150
::hell terminal::
-> [ZSP0] started after 2 ms, version 261.6
[ZSP1] started after 1 ms, version 261.1
ue: Waiting for LCPU IRQ...done
xpc (mcpu): Initalized
xpc (lcpu): Initalized
done
ue: Waiting for LCPU DLP to start...dLPU boot confirmation
done
ue: Waiting for LCPU to run...[L1P] started
hp: Started
feeds: 960 Start enter EAPPS
feeds: 1180 Start leave EAPPS
feeds: 1180 Start enter LWM2M
feeds: 1190 Start leave LWM2M
feeds: 1190 Start enter MQTT
feeds: 1190 Start leave MQTT
feeds: 1190 Start enter SQNSMS
feeds: 1200 Start leave SQNSMS
[PSP] started
```

### 4.4.5. GPIOs

#### *Procedure*

This section helps confirm GPIO's behaviour.

Use the manufacturing AT command `AT+SMGT`.

> **Note:** The manufacturing AT commands are available when the device has been brought into manufacturing mode with the `AT+CFUN=5` command.

The first 32-bits triplet of parameters is a bit-mask to address the GPIO, the second 32-bits triplet of parameters is the bit-mask of the value the GPIO must take, and the third 32-bits triplet provides the expected polarity setting for the GPIO. Refer to *AT Commands Reference Manual* for more detail on this command.

The following command tests the GC02S1's GPIO_22 (GPIO[22]) setting to 1, active high. Value 22 is represented by the bitmask `0x400000`, (= $2^{22}$) coded as the triplet `0,0,0x400000`.

```
AT+SMGT=0,0,0x400000,0,0,0x400000,0,0,0
```

The following command tests GC02S1_GPIO_38 (GPIO[38]) setting to 1, active low. Value 38 is represented by bitmask `0x4000000000`, (= $2^{38}$) coded as the triplet `0,0x40,0`.

```
AT+SMGT=0,0x40,0,0,0x40,0,0,0x40,0
```

Test the expected behaviour as needed by your implementation.

### *Troubleshooting*

- Unexpected AT command error:
  1. Make sure that you activated the Manufacturing mode with `AT+CFUN=5` before trying to use the `AT+SMGT` command.
  2. Make sure that the version of the firmware used is the correct one.
- Unexpected GPIO behaviour:
  - Ensure that there exists no short or open circuit between the test point and the GC02S1.

## 4.4.6. SIM Communication

### *Procedure*

Confirmation of SIM behaviour:

Use the following commands to verify the SIM is working properly:

1. Send `AT+CMEE=2` to activate error logs.
2. Send `AT+CFUN=4` to start reading the SIM card.
3. Wait 10 seconds.
4. Send `AT+CIMI`. It will answer either:
   - `+CME ERROR: SIM not inserted` if no SIM card was detected
   - `+CME ERROR: SIM busy`. Wait for a few more seconds and check if the IMSI is returned. If not, please refer to section Troubleshooting *(on page 48)*.
   - `<IMSI value>` if the test completed successfully
5. Alternatively, the `AT+SMST` command can be used in manufacturing mode to test the SIM connectivity:

```
AT+CFUN=5
OK
AT+SMST=1
+SMST: OK
OK
```

If there is no communication with the SIM card, then the commands fails:

```
AT+SMST=1
+SMST: NO SIM
```

### *Troubleshooting*

- Unexpected AT command error:

  Make sure that the version of the firmware used is correct.
- Unexpected SIM behaviour:
  - Check all the connections between the SIM housing and ensure the board respects the recommendations detailed here *(on page 19)*.
  - Check for short or open circuits between the SIM housing and the GC02S1.
  - Check ground continuity on all SIM housing ground pins and casing.

# 5. Manufacturing

## 5.1. Module Configuration

The following sections describe how to read, modify and save the module configuration in manufacturing mode.

### 5.1.1. Read Device Data

The list below details all the identity elements and software and hardware versions that can be read from the device.

- Read product's manufacturer, model and software version.

```
ATI0
SEQUANS Communications
GC02S1-NA
UE9.0.1
OK
```

- Read product's software version and firmware release.

```
ATI1
UE9.0.1
LR9.0.1.0-59060
OK
```

- Read product's serial number and IMEI.

```
ATI2
SERIAL: C2C2208240006009
IMEISV: 0160740000052700
OK
```

- Read manufacturer identification

```
AT+CGMI
SEQUANS Communications
OK
```

- Read product's IMEI

```
AT+CGSN=1
+CGSN: "016074000005279"
OK
```

- Read product's SVN (Software Version Number)

```
AT+CGSN=3
+CGSN: "00"
OK
```

### 5.1.2. Customise Configuration

#### *Enable Manufacturing Mode*

In order to enable manufacturing mode, please use AT command:

```
AT+CFUN=5
OK
```

In manufacturing mode, specific AT commands can be used. Please refer to the *AT Command Reference Manual* for the details on the manufacturing AT commands.

Each change requires the following steps:

1. Modify the HW configuration of the module
2. Reboot the module with `AT^RESET` to apply the modifications
3. Create a restore point

It is possible to modify the configuration of the following hardware interfaces of the GC02S1:

- UART
- Wake pins
- Antenna tuner configuration
- SIM interface

Examples of common modifications during product manufacturing are provided in the following sections.

### *UART Management (Hardware Configuration Change)*

The 3 UART interfaces are configured by default as listed in Table 29 *(on page 50)*.

**Table 29. UART Ports Default Configuration**

| UART# | Baudrate | Flow Control | Application | Wake Source | Manufacturing Upgrade |
|---|---|---|---|---|---|
| UART0 | 115200 | Enabled | AT | Yes | Yes |
| UART1 | 921600 | Enabled | AT | Yes | Yes |
| UART2 | 115200 | Disabled | Console | No | No |

Both UART0 and UART1 can be used during manufacturing. Typically, UART0 is connected to MCU host and is used only if the manufacturing process happens via the MCU host. If this is not the case, then UART1 shall be used for manufacturing process. In this case the board shall provision the necessary connector or test points to use UART1.

Note that both UART0 and UART1 have their wake source on RTS enabled by default. This means that the module can be waken up from low power mode with either UART. In addition both are configured by default to receive AT commands.

**Note:** If two AT ports are enabled by default, all URCs will be sent by the modem to both of them. Not flushing these URCs will prevent the modem to enter into deep sleep mode.

If UART1 is being used for manufacturing, disabling the wake and putting the UART in DCP mode should be the last step of the manufacturing process:

```
AT+SQNHWCFG="uart1","enable","rtscts","921600","8","none","1","dcp"
```

See section Wake Pins Configuration *(on page 50)* for details on wake function disable.

Changing back UART1 to AT mode can be achieved via UART0.

In addition to the above mentioned considerations, the AT sub-command `AT+SQNHWCFG="uartX"` can be used to configure the baud rate and flow control of any UART. When making these changes, keep in mind that they only apply after next reset.

### *Wake Pins Configuration*

Wake function can also be configured by AT command.

For instance, if UART1 needs to remain accessible during the lifetime of the product for field upgrades or debug, the `wakeRTS1` function can remain enabled (this is the recommended setting). In this case a pull-up needs to be provisioned in the hardware design. Alternatively it can be disabled with AT command:

```
AT+SQNHWCFG="wakeRTS1","disable"
```

#### *Antenna Tuning Configuration*

The GC02S1 supports antenna tuner feature based on GPIO control. A typical HW implementation example, implemented in the GC02S1 NEKTAR Evaluation Kit, is detailed in section Antenna Matching Circuitry *(on page 34)*.

#### *Customise Primary and Alternate Pin Functions*

AT Command `AT+SQNHWCFG` is to be used to configure primary and alternate module's pins functions as described in the data sheet. However, please contact first your Sequans' representative to confirm the software support of the function.

#### *Block Debug Ports*

It is highly recommended that once in mass production, the device blocks the debug ports as part of the manufacturing process. This may be required to meet certain security certifications and it is overall a good security practice.

On Calliope 2 products, the debug ports are:

- UART1
- UART2
- JTAG

All of them can be disabled via the AT command `AT+SQNHWCFG`.

Please refer to *AT Reference Manual* and to *Use Cases with AT Commands* documents.

Notes:

1. UART1 and UART2 can be enabled again through UART0, so it is the host MCU responsibility to control access to the modem's UART0 .
2. Once JTAG is disabled, it can't be enabled again (it uses a fuse mechanism).

### 5.1.3. Save Device Configuration

Once the settings and modifications are done, it is mandatory to issue the AT command `AT+SQNFACTORYSAVE` in order to save into the module that configuration as the default one, and create a restoration point.

```
AT+CFUN?
+CFUN: 5
OK
AT+SQNFACTORYSAVE="OEM"
OK
```

The AT command syntax is detailed in the *AT Commands Reference Manual*.

In case a factory reset (see below) is needed, the restoration point provides the new default values.

### *Factory Reset*

The aim of this operation is to restore the parameters set during the OEM manufacturing phase.

> **Important:** To perform a reset of the modem to factory settings, please note that a restoration point MUST have been created using the command `AT+SQNFACTORYSAVE`.

To perform a reset to customer saved configuration, use the command `AT+SQNFACTORYRESET`.

The AT command syntax is detailed in the *AT Commands Reference Manual* and the *AT Commands Use Cases* documents.

The restore point previously created using `AT+SQNFACTORYSAVE` is used.

```
AT+SQNFACTORYRESET
OK
AT^RESET
OK

+SHUTDOWN

+SYSSTART
```

### 5.1.4. Update the Flash Software Image

GC02S1 modules are delivered with an embedded software, described in the device part numbers table at the beginning of this document. Depending on your needs, you may be required to perform a modem software upgrade during the manufacturing process. Sequans provides an upgrade tool called "SFU". Please refer to the *SFU Upgrade Tool User Manual* for all details, available in Sequans' cloud.

- GC02S1 supports software upgrade over all UART and USB interfaces
- GC02S1 supports differential software upgrade. Please contact Sequans support team to get differential software packages, depending on your needs.

The SFU tool allows upgrade in two modes, "upgrade" and "raster". The "upgrade" mode takes a `.dup` file as input, whose format is described in the *SFU Upgrade Tool User Manual* document. It typically upgrades only the modem part (either full or differential upgrade). For instance:

```
sfu upgrade -z 2 -b 921600 COM45 GC02S1-EU1_REL10_LR9.0.1.0-59060.dup
```

For each software delivery, Sequans provides a *Software Release Note* that describes the method and exact command to use to perform the upgrade.

## 5.2. Functional Verification with Assembled Module

> **Attention:** If a fault is discovered, consider the impact of the issue observed on all manufactured samples.

The purpose of this section is to validate the assembly process of the module.

This test covers the following GC02S1's pins and features:

1. Power supply
2. UART 1 console output during power-up operation
3. SIM Interface
4. GPIOs

5. ADC
6. The nominal power consumption
7. GC02S1's boot
8. GNSS Performance

### 5.2.1. Power Supply

#### *Procedure*

1. Turn on the device under test.
2. Confirm that the current delivered by the Host power supply is nominal

#### *Troubleshooting*

- If excessive current is drawn, check all GC02S1 supply pin for short circuits. Voltages should be at their nominal values.
- If no, or very little, current is drawn, either check the external power supply wiring or look for dry joints between adjacent pin(s) and the power supply source.

### 5.2.2. RF Test Environment

#### *Test Setup*

A simple test setup such as described in Figure 30 *(on page 53)* is required which can be performed "over the air" OTA.

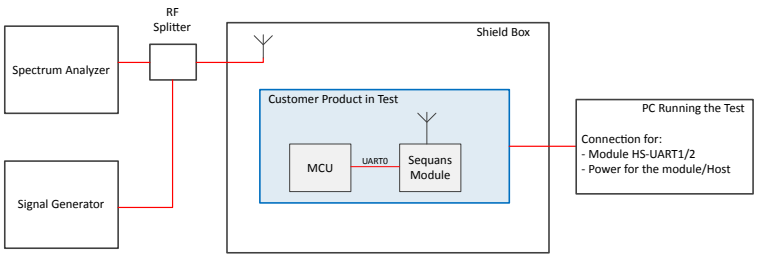



Figure 30. Test Setup Representation

1. Shield Box

   It is possible to make measurements without a Shield Box but it does provide isolation from both interfering signals which could compromise the measurement taken & also antenna Field changes because of local environment.

2. Spectrum Analyser

   to measure the RF power coming from the GC02S1

3. Signal Generator

   to provide the RF signal to catch and measure on the GC02S1

4. PC

   Interface to control the GC02S1 and execute RF test commands

5. RF splitter

   Needed to share the RF path between both equipments.

6. Test fixture

   Houses the Test Equipment Antenna & the device under test. Some recommendations:

   - Shield box should be lined with a type of RF absorption material, to reduce internal RF reflections & avoid large variations in measurements
   - RF Attenuation target should be > 50dB for all bands of operation
   - Digital & Analogue signals should pass through decoupled chassis mount interfaces
   - The DUT should sit in some type of bedding. This helps improve the measurement reliability as the DUT location is repeatable

7. Antenna

   Should be broad band. High Gain (very directive) would be preferable but not compulsory.

8. Interfacing signals

   Should be tied/fixed down within the shield box, not left loose. This is to avoid changed in the RF signal field withing the box.

#### *Test Overview*

Every Product should be tested for it its capability to Transmit & to Receive for any test type (signalling or non-signalling) . It should be performed:

- All product bands of operation
- 3 Frequencies : low, mid and high
- One TX power level, 23dBm
- One RX signal level -45dBm

### 5.2.3. Calibration of the RF Setup

Over-the-Air (OTA, or radiated) measurements can never be as accurate as those used for conducted measurements, but it is important to ensure that the setup is made as accurate as possible. The following information can help with this.

To ensure that the measurements are reasonably accurate, the RF Path Losses from the GC02S1 module antenna to the Shield Box antenna need to be calibrated. This can be done by the following procedure:

1. Place a reference “golden” product into the Shield Box. The conducted RF performances, especially TX power measurements at 23dBm, for this reference “golden” product must be known.
2. Record the TX power measurements for each band of operation
3. For each band of operation, compute the difference of the conducted reference power measured vs the radiated power measured. These values are recorded as the Band path losses.
4. Remove the reference “golden” product from the Shield Box
5. Each RF path loss is then used to correct the TX and RX measurements as follows:

6. ◦ TX: the loss value is added to the Integrated Tx Power Measurement

   ◦ RX: the Signal Generator Signal is increased by the path loss value

Notes:

1. It is recommended to repeat steps 1 to step 4 at least 5 times.

   This allows to catch any possible measurement variation due to subtle changes in RF signal propogation within the Shield Box. This variation would also need to be included into Pass/Fail Criteria for the TX and RX measurement limits.

2. Any adjustment to the Shield Box internal arrangement (antenna moved, bedding shape changed or moved, supply and communication cables adjusted) impacts the measurements. In such case, the process shall be repeated.

### 5.2.4. Testing in Non-Signalling Mode

The procedure to test Rx and Tx performance in CW mode will be detailed in a future release of this document.

### 5.2.5. Testing in Signalling Mode

Make sure that samples of the product are routinely checked for RF performances in signalling mode. 'Routinely' means here to randomly test a sample of a product from manufacture batches.

A specific test equipment, such as CMW500 with signalling software, is required to perform signalling mode test, including connection and RF measurement to emulate a real LTE Category-1 connection.

This CMW500 replaces the Signal Generator and the Spectrum Analyser shown in Figure 30 *(on page 53)*.

Simply power up the module (configured in auto-connect mode) and it should automatically attach to the tester.

## 5.3. Storage and Mounting

#### *Storage Conditions*

The GC02S1 module is Moisture Level 3 rated as per JEDEC industrial standard.

#### *Reflow Profile*

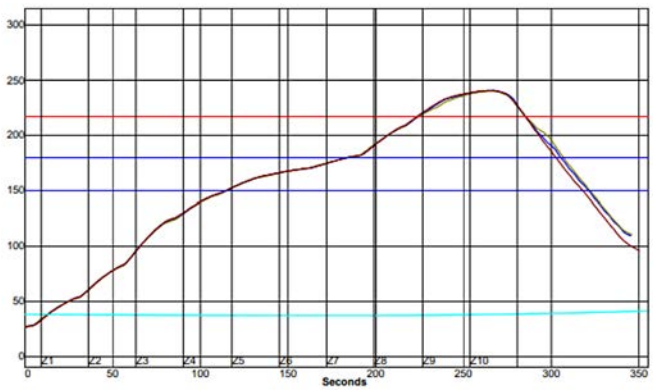



Figure 31. Reflow Profile Parameters

**Table 30. Reflow Parameters**

| Parameter | Min. Value | Max. value | Unit |
|---|---|---|---|
| Slope between 25 and 150 °C (averaged over 20 s.) | 0.5 | 4 | °C/s |
| Max. falling slope (averaged over 1 s.) | -4 | -1 | °C/s |
| Soak Time from 150 to 180 °C | 60 | 120 | s |
| Time spent above reflow temperature (217 °C) | 45 | 90 | s |
| Peak Temperature | | 245 | °C |
| Number of Possible Reflows | | 3 | |

## 5.4. Reliability Specification

The GC02S1 reliability figures will be provided in a future release of this document.

# 6. Mechanical Characteristics

## 6.1. Package Description

The package size with tolerance is (19.5 ± 0.10) mm × (21.0 ± 0.10) mm × (1.9 max) mm. Maximum 'warpage' is 0.13 mm (as per JEITA ED7306).

The GC02S1 weighs 1.78 g.

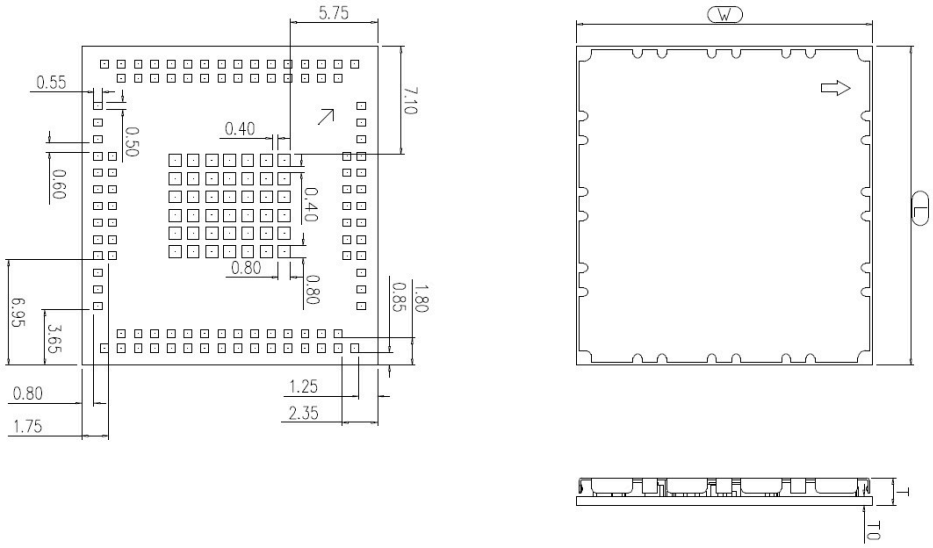
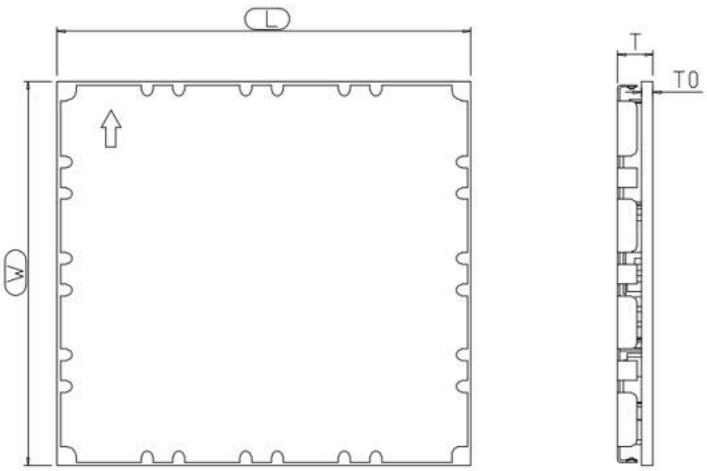



Figure 32. Module PCB View




| | Dim. | Tol. |
|---|---|---|
| L | 21.00 | ±0.10 |
| W | 19.50 | ±0.10 |
| T | 1.80 | ±0.10 |
| T0 | 0.60 | ±0.06 |

Figure 33. Module Physical Dimensions

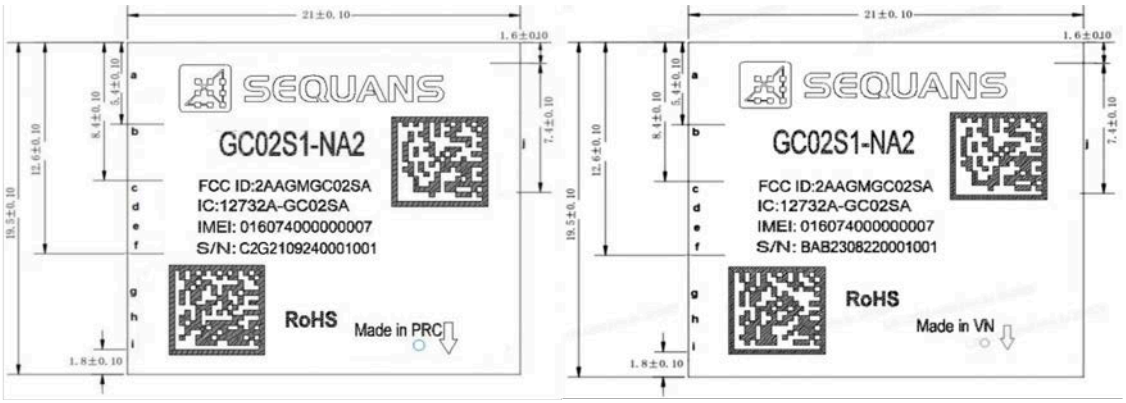



Figure 34. NA Module Laser Marking

Notes on Figure 34 *(on page 58)*:

1. The triangle in the bottom-right corner provides pin #1 location.
2. FCC ID: 2AAGMGC02SA
3. IC: 12732A-GC02SA
4. IMEI:*XXXXXXXXXXXXXXX*
5. S/N:C2A*YYMMDDNNNNSSS* (16 digits)
    - C2A: reserved, value subject to change at Sequans's discretion (3 digits);
    - *YYMMDD*: Manufacturing Date (YY:Year;MM:Month,DD:Day);
    - *NNNN*: Panel counter (from 0001~9999);
    - *SSS*: Piece location on panel (from 001~036)
6. 2D marked "a" refer to IMEI Barcode
7. 2D marked "b" refer to S/N Barcode

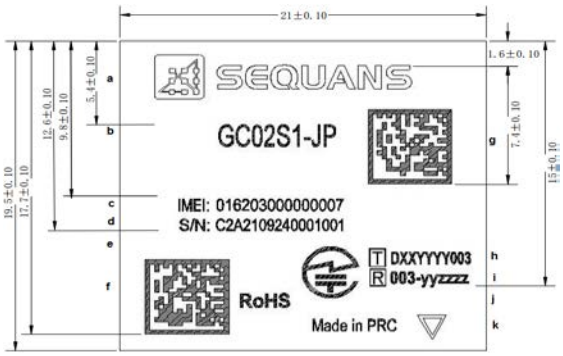



Figure 35. JP Module Laser Marking

Notes on Figure 35 *(on page 58)*:

1. The triangle in the bottom-right corner provides pin #1 location.
2. S/N:C2A*YYMMDDNNNNSSS* (16 digits)

- C2A: reserved, value subject to change at Sequans's discretion (3 digits);
- *YYMMDD*: Manufacturing Date (YY:Year;MM:Month,DD:Day);
- *NNNN*: Panel counter (from 0001~9999);
- *SSS*: Piece location on panel (from 001~024)

3. TELEC Certificate Logo
4. 2D marked "a" refer to IMEI Barcode
5. 2D marked "b" refer to S/N Barcode
6. JATE Certification Code
7. TELEC Certification code

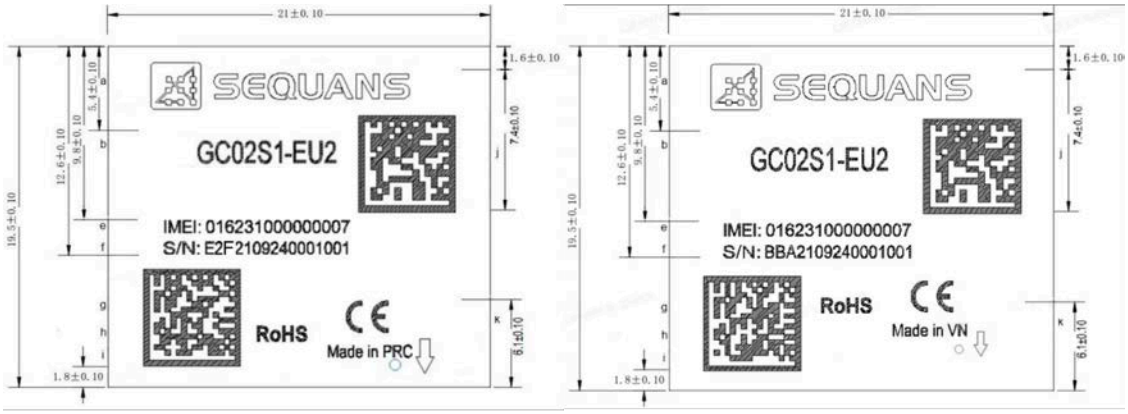



Figure 36. EU Module Laser Marking

Notes on Figure 36 *(on page 59)*:

1. The triangle in the bottom-right corner provides pin #1 location.
2. IMEI:*XXXXXXXXXXXXXXX*
3. S/N:C2A*YYMMDDNNNNSSS* (16 digits)
   - C2A: reserved, value subject to change at Sequans's discretion (3 digits);
   - *YYMMDD*: Manufacturing Date (YY:Year;MM:Month,DD:Day);
   - *NNNN*: Panel counter (from 0001~9999);
   - *SSS*: Piece location on panel (from 001~036)
4. 2D marked "a" refer to IMEI Barcode
5. 2D marked "b" refer to S/N Barcode
6. 'CE' Marking

## 6.2. Environmental Conditions

GC02S1 operating conditions:

- Temperature (PCB temperature as measured by on-board thermistor):
  - Operational: -40°C to +85°C;
  - RF compliant: -30°C to +85°C
- Humidity: 10% to 85% (non-condensing)

## 6.3. Packing

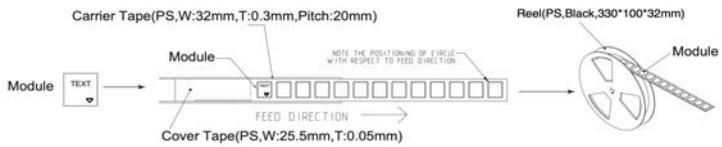



Figure 37. Packing Modules in Reels

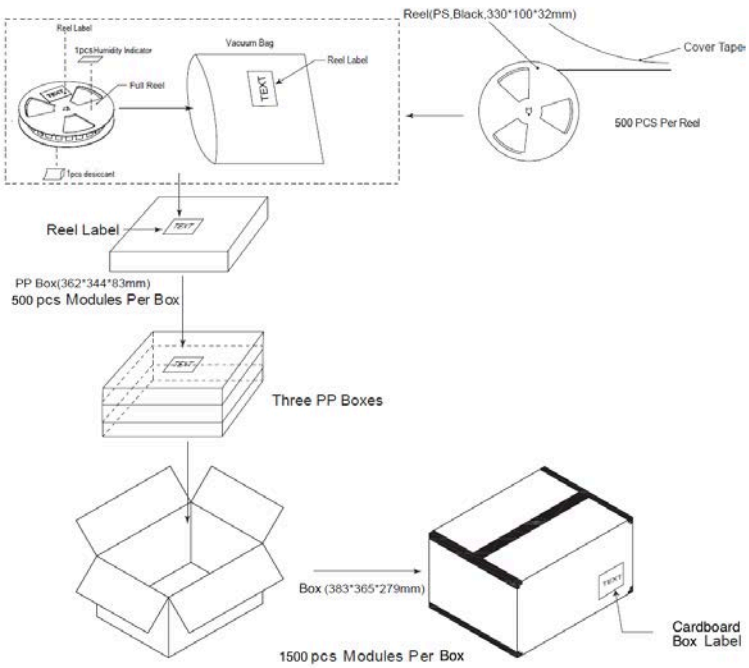



Figure 38. Packing Reels in Boxes

Other details will be provided in a future release of this document.

# 7. Regulatory Approval

JATE/TELEC regulatory approval details will be provided in a future revision of this document (GC02S1-JP)

RED conformity details will be provided in a future revision of this document (GC02S1-EU)

## 7.1. GC02S1-EU2 Certi ication

The GC02S1-EU2 will be certified by RED and GCF.

## 7.2. GC02S1-NA2 Certi ication

The GC02S1-NA2 will be certified by the FCC (ISED), PTCRB, GCF, Verizon, AT&T, Bell, Telus and Rogers.

### 7.2.1. FCC Regulatory Approval

FCC-ID: 2AAGMGC02SA (single modular approval)
This above identified LTE radio module is not intended to be provided to end-users but is for installation by OEM integrators only.

This radio module was tested and found in compliance with the FCC rules using the following antennae:
OmniLOG® 90200: Peak gain 2.0 dBi
TRIO mXTENDTM (FR01-S4-210): Peak gain 2.4 dBi

***Installation/Integration***
OEM integrators must follow Sequans' installation instructions to provide for and benefit from FCC compliant module integrations and must abide especially by the following provisions:

The maximum antenna gain values (accounting for cable attenuation) to comply with the FCC maximum ERP/EIRP limits and with RF Exposure rules:

- LTE band 2 (1900 PCS): 10.25 dBi
- LTE band 4 (AWS-1): 7.06 dBi
- LTE band 5 (850): 11.66 dBi
- LTE band 12 (700a): 10.77 dBi
- LTE band 13 (700c): 10.93 dBi
- LTE band 14: 11.15 dBi
- LTE band 17 (700b): 10.77 dBi
- LTE band 25 (1900+): 10.35 dBi
- LTE band 66 (AWS-3): 7.06 dBi

Sequans's module integration guidelines must be closely followed.

Compliance of host integrations of the module is limited to hosts adaptation designs which are identical to Sequans' reference design.

Host integrations with adaption designs deviating from Sequans' reference design require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

Host integrations with co-located (simultaneously operating) radio transmitters must be evaluated in accordance with FCC multi-transmitter rules and may require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID, dependent on the result of the evaluation; Inquiry at FCC or a TCB is urgently recommended.

Integrations of the module into host products which are intended for portable use, i.e. less than 20cm distance between its radiating structures (antenna) and the body of nearby persons, or which otherwise put additional technical requirements like Hearing Aid compatibility require either class 2 permissive change to this modular approval or a separate host approval with different FCC-ID;

***Compliance with Unwanted Emission Limits for Digital Device***

If the OEM host integration fully complies with the above described reference design and can completely inherit and rest on compliance of the existing modular approval the OEM remains still responsible to show compliance of the overall end-product with the FCC limits for unwanted conducted and radiated emissions from the digital device (unintentional radio) portion of such end-product (commonly addressed as part 15B compliance or similar).

***End-product Labelling***

- The module's FCC-ID must either be visible from the exterior of the host product (e.g. per window) or per electronic display, or shall be displayed on an additional exterior label per the following or similar string: contains FCC-ID: 2AAGMGM02SA
- The module's FCC-ID must either be visible from the exterior of the host product (e.g. per window) or per electronic display, or shall be displayed on an additional exterior label per the following or similar string: contains FCC-ID: 2AAGMGM02SA
- Digital Device - Unwanted Emissions Notice: If the end-product falls under part 15 of the FCC rules (it shall display the following user notice on its exterior acc. to part 15.19 (the notice may be printed in the manual in case the host is too small):

  This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.
- Further Labelling Requirements may apply dependent on the FCC rule parts relevant to the host product.
- End-product User Instructions / Notices in the Manual: At a minimum, end-product users must be provided with the following notices at a prominent location of the product literature furnished with the product:
  - Product Modifications: Modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
  - RF Exposure Compliance: This equipment complies with FCC radio frequency radiation exposure rules and limits set forth for an uncontrolled environment, when installed and operated with minimum distance of 20 cm between its radiating structures (antenna) and the body of nearby persons and when not operated simultaneously with other nearby radio-transmitters.
  - Maximum Antenna Gain: The user instructions of end-products equipped with standard external antenna connectors for the modular radio transmitter providing the option to connect other antennae than those which may or may not be bundled with the end-product must list the maximum allowed antenna gain values as derived from those given above, accounting for the cable attenuations of the actual installation.
  - Digital Device - Unwanted Emissions Notice: If the end-product is or contains a digital device (unintentional radio portions) and is not exempted by its use case (like vehicular use) the following part 15.105 (b) user notice shall be provided at prominent location of the product literature:

    This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no

guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna;
- Increase the separation between the equipment and receiver;
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected;
- Consult the dealer or an experienced radio/TV technician for help

◦ Further User Notices: May be required dependent on the FCC rule parts relevant to the host product.

◦ Non-allowed User Instructions: The end-product user guidance may NOT include instructions about how to install or de-install the module.

### 7.2.2. ISED Regulatory Approval

This device complies with ISED's licence exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR de l'ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit supporter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

This radio module was tested and found in compliance with the ISED using the following antennae:
Ce module radio a été testé et jugé conforme à ISDE en utilisant les antennes suivantes :
OmniLOG® 90200: Peak gain 2.0 dBi
TRIO mXTENDTM (FR01-S4-210): Peak gain 2.4 dBi

**This device is intended only for OEM integrators under the following conditions: (For module device use)**

1. The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2. The transmitter module may not be co located with any other transmitter or antenna.

As long as the two conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end product for any additional compliance requirements required with this module installed.

**Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)**

1. L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2. Le module émetteur peut ne pas être co implanté avec un autre émetteur ou antenne.

Tant que les deux conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

- LTE band 2 (1900 PCS): 10.25 dBi
- LTE band 4 (AWS-1): 7.06 dBi
- LTE band 5 (850): 8.37 dBi
- LTE band 12 (700a): 7.7 dBi
- LTE band 13 (700c): 7.72 dBi

- LTE band 14: 7.92 dBi
- LTE band 17 (700b): 7.7 dBi
- LTE band 25 (1900+): 10.35 dBi
- LTE band 66 (AWS-3): 7.06 dBi

**IMPORTANT NOTE:**

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorisation is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorisation.

**NOTE IMPORTANTE:**

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

**End Product Labelling**

This transmitter module is authorised only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC:12732A-GC02SA”.

**Plaque signalétique du produit final**

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20 cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: “Contient des IC: 12732A-GC02SA”.

**Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

**Manuel d'information à l'utilisateur final**

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

## 7.3. GC02S1-JP1 Certification

The GC02S1-JP1 will be certified by JATE/TELEC, NTT Docomo and KDDI.

# A. Troubleshooting

JTAG interface is required to access the processor if the board does not boot properly and provides no console output.

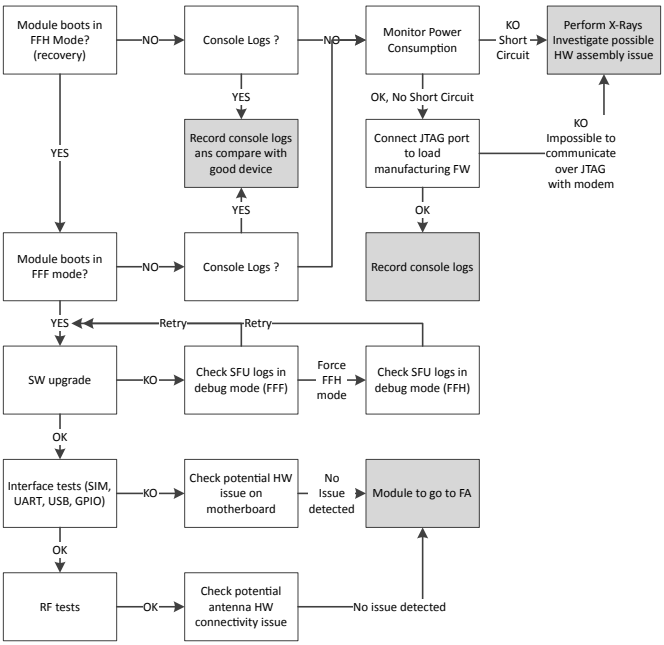



Figure 39. Troubleshoot Flowchart

## 1.1. JTAG Investigations

This annexe provides details on the hardware and software requirements to operate JTAG on the GC02S1 module.

### *Hardware Setup*

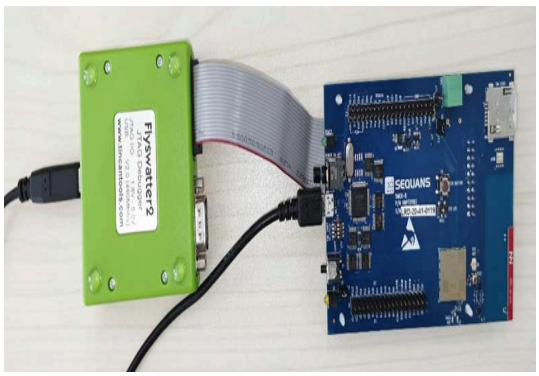



Figure 40. JTAG Hardware Setup

Figure 41. JTAG Connector Detail

### *Software Setup*

The *Flyswatter* box is used as JTAG probe with Calliope 2 chipsets.

Its reference is to be found at http://www.andestech.com/en/products-solutions/andeshape-platforms/aice-mcu/.

**Note:** You need an additional set of files with specific software settings and patches to use NDES AICE-MCU box with Calliope 2 platform. Please contact your Sequans' technical representative to get them.

The required software setup is a PC running Linux. Several steps are required before JTAG operation:

- Enable Linux for using JTAG without root access
- Customize the ANDES AICE-MCU box's firmware.
  - Edit JTAG configuration file
  - Patch OpenOCD

1. The following procedure needs to be done only once on your Linux, to be able to use the JTAG without root access:
   a. Create a file `/etc/udev/rules.d/99-andes.rules` in which you put the following line:

   ```
   SUBSYSTEMS=="usb", ACTION=="add", ATTRS{idVendor}=="1cfc",
   GROUP="plugdev", MODE="0664"
   ```

   b. Then reload your `udev` rules:

   ```
   sudo udevadm control --reload-rules
   ```

   c. Then add yourself into the `plugdev` group if you are not already:

   ```
   sudo usermod -a -G plugdev $USER
   ```

   See step 2 for verification or go to step 3 for the procedure.

2. Confirm that the AICE box is recognized by your PC:

   ```
   $> dmesg | tail
   [  537.324026] usb 3-1.3.3: new high-speed USB device number 6 using ehci_hcd
   [  544.956983] usb 3-1.3.3: New USB device found, idVendor=1cfc, idProduct=0000
   [  544.956989] usb 3-1.3.3: New USB device strings: Mfr=1, Product=2, SerialNumber=0
   [  544.956993] usb 3-1.3.3: Product: AndeShape AICE
   [  544.956995] usb 3-1.3.3: Manufacturer: Andes Technology Corp.
   ```

If you have followed the PC configuration section above, you should have read/write access to the USB device. This is confirmed by the first line of the output listed above.

```
[  537.324026] usb 3-1.3.3: new high-speed USB device number 6 using ehci_hcd
```

The first digit of the `usb 3-1.3.3` part is the USB bus number, 3 in this case. The device number is 6.

This means that your USB device file is located at `/dev/bus/003/006`:

```
$> ls -l /dev/bus/usb/003/006
crw-rw-r-T 1 root plugdev 189, 261 Apr  5 16:07 /dev/bus/usb/003/006
```

The file is owned by the `plugdev` group and that the group have the read and write permissions on it, all is fine.

However, if the file is owned only by `root`, then type the following command to change the owning group to `plugdev`:

```
$> sudo chgrp plugdev /dev/bus/usb/003/006
```

3. Download and update the JTAG repository:

```
git clone ssh://$USER@git-share.sequans.com:29418/4G/platform/jtag
```

We will refer to this repository as `JTAG/`.

Edit the file `JTAG/amontec/helpers/generic.cfg` and uncomment the following line:

```
source [file join [file dirname [info script]] ".." "gerbil" "Andeshape_AICE.cfg"]
```

4. Rebuild OpenOCD

Download the OpenOCD repository:

```
git clone ssh://$USER@git-share.sequans.com:29418/4G/platform/openocd
```

To build OpenOCD, go into the source directory and execute:

```
./bootstrap
./configure MAKEINFO=true --enable-aice --disable-werror
make
make install
```

**Note:**

- You may need to run `sudo make install`
- If you use recent system (`aclocal` > 1.11), you should revert to `4f1c4f3e48cf2a2a4c9bf1e8a7ca83c23ff78535` before doing this procedure.

### *Run OpenOCD*

To start openocd, go to the JTAG/amontec/helpers directory and run:

```
$> openocd -f ../gerbil/gerbil-rst.cfg
Open On-Chip Debugger 0.9.0 (2017-03-01-16:46)
Licensed under GNU GPL v2
For bug reports, read  http://openocd.org/doc/doxygen/bugs.html
script ../gerbil/gerbil.cfg
Info : only one transport option; autoselect 'aice_jtag'
trst_and_srst separate srst_gates_jtag trst_push_pull srst_open_drain
    connect_deassert_srst
adapter speed: 24000 kHz
adapter speed: 100 kHz
trst_only separate trst_push_pull
adapter speed: 24000 kHz
Info : AICE version: hw_ver = 0x10001, fw_ver = 0xa, fpga_ver = 0xc
Info : AICE hardware features: 0xc0000004
Info : AICE batch data buffer size: 512 words
Andes AICE-MCU v1.10.12
Info : AICE initialization started
There is 1 core in target
```

```
Core #0: EDM version 0x0
Info : AICE JTAG Interface ready
JTAG frequency 24 MHz
Info : clock speed 24000 kHz
Info : bb: soft-reset-halt: off
Info : bb: global stop: off
 ----------------------------------
| Board ready for JTAG debugging.  |
 ----------------------------------

Telenet to localhost, port 4444 (shell command : telnet localhost 4444),
or connect to remote target via GDB, port 3333 (command inside GDB : target
remote localhost:3333).
```

**Important:** When OpenOCD is started, the target is automatically halted. Note that only the MCPU is halted by the JTAG, the LCPU will still be running by itself

There are two methods to communicate with OpenOCD, GDB and Telnet. They are both described below.

- GDB

  The preferred way to debug with JTAG is by using GDB.

  GDB is provided by the Andes toolchain, the binary name is `nds32be-elf-gdb`.

- Telnet

  You can use telnet to communicate with openocd:

  ```
  $> telnet localhost 4444
  Trying ::1...
  Trying 127.0.0.1...
  Connected to localhost.
  Escape character is '^]'.
  Open On-Chip Debugger
  >
  ```

  You can type '`help`' to get all supported commands.

  You can erase parts of the flash by using the command `erase <offset> <size>`:

  ```
  erase 0x20000 1024
  ```

  You can burn a raw file into the flash by using the command `flash_file <file> <offset>`:

  ```
  flash_file /tmp/bootrom.rast 0
  ```

  **Note:** If the flash was already written before, it is necessary to use `erase` command to clear the flash before using `flash_file` command, otherwise you will hit readback errors.

  To boot mTools, use following command:

  ```
  load_image mtools.elf
  resume 0x1000
  ```

  `load_image` command takes around 10 minutes to finish.

# B. Acronyms

| Acronym | Definition |
|---|---|
| ADC | Analogue to Digital Converter |
| CPU | Central Processing Unit |
| DL | Downlink |
| ESD | Electro-static discharge |
| ETSI | European Telecommunications Standard Institute |
| GND | Ground |
| GNSS | Global Navigation Satellite System |
| GPIO | General Purpose Input Output |
| I/O | Input/Output |
| I²C | Inter-Integrated Circuit interface |
| IMEI | International Mobile Equipment Identity |
| IP | Internet Protocol |
| JTAG | Joint Test Action Group |
| LNA | Low-Noise Amplifier |
| LTE | Long Term Evolution, or 4G. Standard is developed by the 3GPP. |
| MIMO | Multiple In Multiple Out |
| NAS | Network Access Server |
| PCM | Pulse-Code Modulation |
| PHY | Physical Layer |
| RED | European Radio Equipment Directive |
| SAW | Surface Acoustic Wave (filter) |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| Rx | Reception |
| S/N | or SN: Serial Number |
| SIM | Subscriber Identification Module |
| SMS | Short Message Service |
| SPI | Serial Peripheral Interface |
| Tx | Transmission |
| UART | Universal Asynchronous Receiver Transmitter |
| UE | User Equipment |
| UL | Uplink |
| USB | Universal Serial Bus |