



ZigBee-Ready RF Transceiver Module (IEEE 802.15.4) CTL3585 CTL3575

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ZigBee- Ready RF Transceiver Module CTL3585_CTL3575**Revision**

Rev.	Date (DD-MM-YYYY)	History
1	21-01-2015	First Released
2	05-08-2015	Changed the PCB size, Power settings and etc.
3	08-06-2018	Add CTL3575 in the PRD

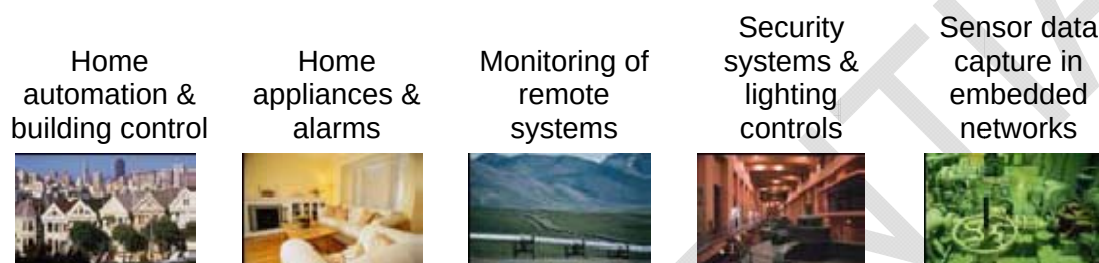
Table of Contents

1. General Description	1
2. Applications	1
3. Features	1
4. Absolute Maximum Ratings.....	2
5. Recommended Operating Conditions	2
6. Electrical Specifications.....	2
7. Typical application block	3
8. Pin Assignment.....	4
9. Pin Description	5
10. Block Diagram.....	9
11. RF Frequency Detail.....	10
12. PCB Layout Recommendations.....	11
13. Mechanical Dimensions	12

1. General Description

The CTL3585/CTL3575 are compact surface mounted High Power Wireless RF Transceiver Module specially designed for Ember ZigBee™ protocol stack for wireless networks, EmberZNet, based on IEEE 802.15.4 standard in the 2.4GHz world-wide ISM band. The size of CTL3585(CTL3575) is 24.5 x 17 x 2.8 mm. It integrated a 2.4GHz, IEEE 802.15.4-2003 compliant transceiver with a 32-bit network processor (ARM Cortex-M3 Processor) to run EmberZNet. It contains embedded FLASH and integrated RAM for program and data storage. It utilizes the non-intrusive SIF module for powerful software debugging and programming of the network processor.

2. Applications



3. Features

- Complete ZigBee-ready module with integrated PCB antenna
- Integrated IEEE 802.15.4 PHY and MAC layer
- Non-intrusive debug interface (SIF)
- SPI interface for communication and controlled by the Host using the EmberZNet Serial Protocol (EZSP)
- Internal RC oscillator for timer
- High performance direct sequence spread spectrum (DSSS) RF transceiver
- 16 channels in the 2.4 GHz ISM band
- On-chip regulator for 2.1-3.6V operation.
- Three deep low power modes
- 32-bit ARM® Cortex™-M3 processor
- 256KB or 512KB FLASH, with optional read protection and 32 or 64KB RAM(CTL3585)
- 128KB or 192KB FLASH, with optional read protection and 12KB RAM(CTL3575)
- +20dBm Max. transmission power
- -100dBm sensitivity
- Small footprint: 24.5x17x2.8mm
- Extremely low Deep Sleep Current.

4. Absolute Maximum Ratings

Parameter	Test Conditions	Min.	Max.	Unit
Regulator input voltage (VDD_PADS)		-0.3	+3.6	V
Voltage on any GPIO (PA[7:0], PB[7:0], PC[7:0]), SWCLK, nRESET, VREG_OUT		-0.3	VDD_PADS +0.3	V
Voltage on any GPIO pin (PA4, PA5, PB5, PB6, PB7, PC1), when used as an input to the general purpose ADC with the low voltage range selected		-0.3	2.0	V
Voltage on OSCA, OSCB, NC		-0.3	VDD_PADS +0.3	V
Storage temperature		-40	+85	°C

5. Recommended Operating Conditions

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Regulator input voltage (VDD_PADS)		2.1		3.6	V
Operating temperature range		-40		+85	°C
Moisture Sensitivity Level (MSL)		MSL3			

6. Electrical Specifications

T=25°C, VCC = 3.0V, Fo =2450MHz, if nothing else stated.

Parameter	Condition / Note	Min	Typ.	Max	Unit
RF Operating frequency	Programmable in 5MHz steps, 5 MHz steps for IEEE 802.15.4 compliance	2.4		2.5	GHz
Number of channels	For IEEE 802.15.4 compliance		16		
Channel spacing	For IEEE 802.15.4 compliance		5		MHz
Frequency stability				+/-40	ppm
Transmit power	Programmable from firmware			+20	dBm
Sensitivity	PER = 1% PER, 20byte packet defined by IEEE 802.15.4 Boost mode		-100		dBm
Adjacent channel rejection +/-5 MHz	IEEE 802.15.4 compliance at -82 dBm		35/35		dB
Adjacent channel rejection +/-10 MHz	IEEE 802.15.4 compliance at -82 dBm		40/40		dB

ZigBee- Ready RF Transceiver Module CTL3585_CTL3575

Parameter	Condition / Note	Min	Typ.	Max	Unit
Supply voltage		2.1		3.6	V
Current consumption, RX mode	Max RX sensitivity		30		mA
Current consumption, TX mode			150		mA
Deep sleep current			2.8		uA
Flash Memory	FLASH memory in EM3585		512		KB
	FLASH memory in EM357		192		KB
MCU clock frequency			24		MHz
MCU Low Speed Clock	External crystal or Ext 32.768KHz clock		32.768		KHz

7. Typical application block

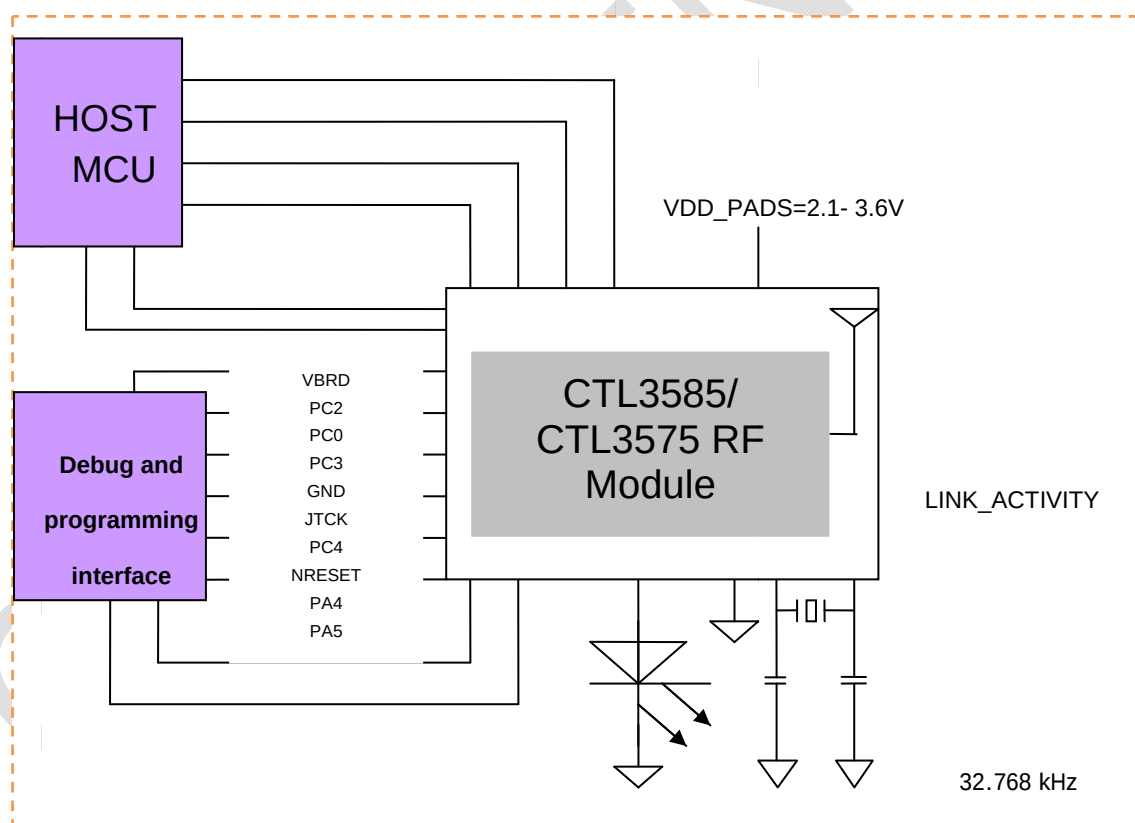


Figure 1: Example of application circuit

8. Pin Assignment

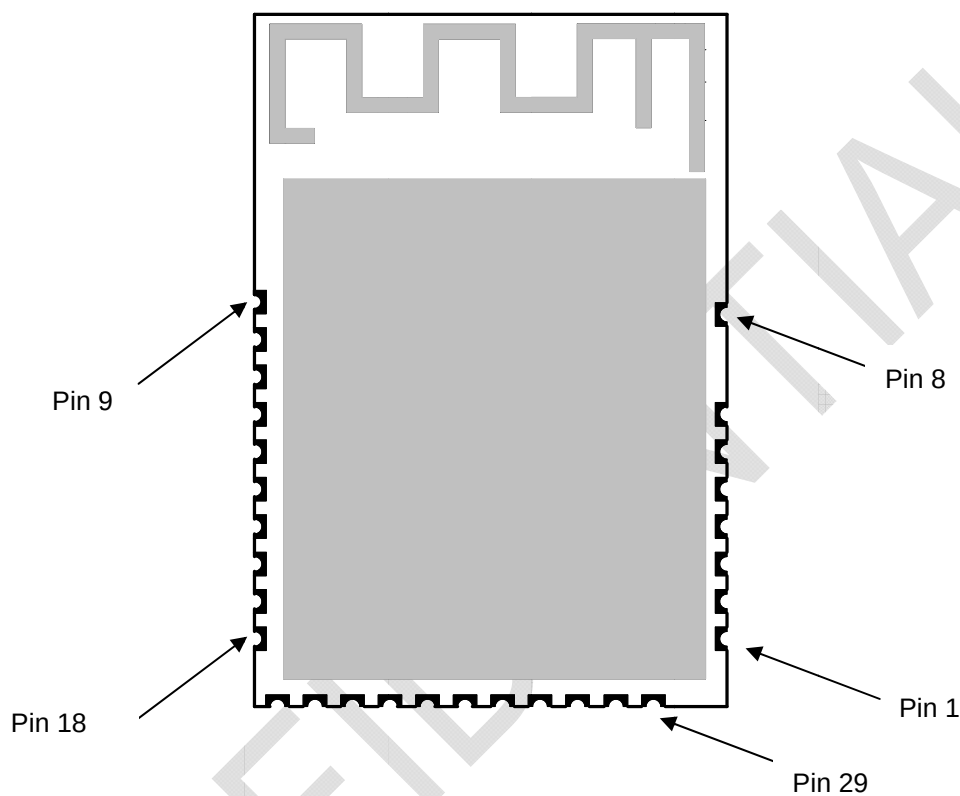


Figure 2: CTL3585/CTL3575 pin assignment

9. Pin Description

Moduel Pin#	EM3585/ EM357 Pin#	Pin Name	Direction	Description
1	36	PB0	I/O	Digital I/O
		VREF	Analog O	ADC reference output
		VREF	Analog I	ADC reference input
		IRQA	I	External interrupt source A
		TRACECLK	O	Synchronous CPU trace clock
		TIM1CLK	I	Timer 1 external clock input
		TIM2MSK	I	Timer 2 external clock mask input
2	49	GND		
3	40	PC0	I/O High current	Digital I/O Either Enable with GPIO_DBGCFG[5]
		JRST	I	JTAG reset input from debugger
		IRQD	I	Default external interrupt source D
		TRACEDATA1	O	Synchronous CPU trace data bit 1
4	41	PB7	I/O High current	Digital I/O
		ADC2	Analog	ADC input 2
		IRQC	I	Default external interrupt source C
		TIM1C2	O	Timer 1 channel 2 output
		TIM1C2	I	Timer 1 channel 2 input
5	42	PB6	I/O High current	Digital I/O
		ADC1	Analog	ADC input 1
		IRQB	I	External interrupt source B
		TIM1C1	O	Timer 1 channel 1 output
		TIM1C1	I	Timer 1 channel 1 input

ZigBee- Ready RF Transceiver Module CTL3585_CTL3575

Module Pin#	EM3585/EM357 Pin#	Pin Name	Direction	Description
6	43	PB5	I/O	Digital I/O
		ADC0	Analog	ADC input 0
		TIM2CLK	I	Timer 2 external clock input
		TIM1CLK	I	Timer 1 external clock mask input
7	49	GND		
8	49	GND		
9	49	GND		
10	12	nRESET	I	Active low chip reset(internal pull-up)
11	13	PC6	I/O	Digital I/O
		OSC32B	I/O	32.768KHz crystal oscillator.
		NTX_ACTIVE	O	Inverted TX_ACTIVE signal
12	14	PC7	I/O	Digital I/O
		OSC32A	I/O	32.768KHz crystal oscillator.
		OSC32_EXT	I	Digital 32.768KHz clock input source
13	16,23,28,37	VDD_PADS	Power	Pads supply(2.1-3.6V)
14	18	PA7	I/O High current	Digital I/O Disable REG_EN with GPIO_DBGCFG [4]
		TIM1C4	O	Timer 1 channel 4 output
		TIM1C4	I	Timer 1 channel 4 input
		REG_EN	O	External regulator open drain output
15	19	PB3	I/O	Digital I/O
		TIM2C3	O	Timer 2 channel 3 output
		TIM2C3	I	Timer 2 channel 3 input
		SC1nCTS	I	UART CTS handshake of Serial Controller 1
		SC1SCLK	O	SPI master clock of serial Controller 1
		SC1SCLK	I	SPI slave clock of serial Controller 1

ZigBee- Ready RF Transceiver Module CTL3585_CTL3575

Moduel Pin#	EM3585/EM357 Pin#	Pin Name	Direction	Description
16	20	PB4	I/O	Digital I/O
		TIM2C4	O	Timer 2 channel 4 output
		TIM2C4	i	Timer 2 channel 4 input
		SC1nRTS	O	UART RTS handshake of serial controller 1
		SC1nSSEL	I	SPI slave select of serial controller 1
17	21	PA0	I/O	Digital I/O
		TIM2C1	O	Timer 2 channel 1 output
		TIM2C1	I	Timer 2 channel 1 input
		SC2MOSI	O	SPI master data out of serial controller 2
		SC2MOSI	I	SPI slave data in of serial controller 2
18	22	PA1	I/O	Digital I/O
		TIM2C3	O	Timer 2 channel 3 output
		TIM2C3	I	Timer 2 channel 3 input
		SC2SDA	I/O	TWI data of serial controller 2
		SC2MISO	O	SPI slave data out of serial controller 2
		SC2MISO	I	SPI master data in of serial controller 2
19	24	PA2	I/O	Digital I/O
		TIM2C4	O	Timer 2 channel 4 output
		TIM2C4	I	Timer 2 channel 4 input
		SC2SCL	I/O	TWI clock of serial controller 2
		SC2SCLK	O	SPI master clock of serial controller 2
		SC2SCLK	I	SPI slave clock of serial controller 2
20	25	PA3	I/O	Digital I/O
		SC2Nssel	I	SPI slave select of serial controller 2
		TIM2C2	O	Timer 2 channel 2 output
		TIM2C2	I	Timer 2 channel 2 input

ZigBee- Ready RF Transceiver Module CTL3585_CTL3575

Moduel Pin#	EM3585/EM357 Pin#	Pin Name	Direction	Description
21	26	PA4	I/O	Digital I/O
		ADC4	Analog	ADC input 4
		PTI_EN	O	Frame signal of packet trace interface
		TRACEDATA2	O	Synchronous CPU trace data bit 2
22	27	PA5	I/O	Digital I/O
		ADC5	Analog	ADC input 5
		PTI_DATA	O	Data signal of packet trace interface
		NBOOTMODE	I	Embedded serial bootloader activation out of reset
		TRACEDATA3	O	Synchronous CPU trace data bit 3
23	29	PA6	I/O High current	Digital I/O
		TIM1C3	O	Timer 1 channel 3 output
		TIM1C3	I	Timer 1 channel 3 input
24	30	PB1	I/O	Digital I/O
		SC1MISO	O	SPI slave data out of serial controller 1
		SC1MOSI	O	SPI master data out of serial controller 1
		SC1SDA	I/O	I2C data of serial controller 1
		SC1TXD	O	UART transmit data of serial controller 1
		TIM2C1	O	Timer 2 channel 1 output
		TIM2C1	I	Timer 2 channel 1 input
25	31	PB2	I/O	Digital I/O
		SC1MISO	I	SPI master data in of serial controller 1
		SC1MOSI	I	SPI slave data in of serial controller 1
		SC1SCL	I/O	I2C clock of serial controller 1
		SC1RXD	I	UART receive data of serial controller 1
		TIM2C2	O	Timer 2 channel 2 output
		TIM2C2	I	Timer 2 channel 2 input
26	32	JTCK	I	JTAG clock input from debugger
		SWCLK	I/O	Serial Wire Clock input/output with debugger

ZigBee- Ready RF Transceiver Module CTL3585_CTL3575

Mod uel Pin#	EM3585/E M357 Pin#	Pin Name	Direction	Description
27	33	PC2	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTDO	O	JTAG data out to debugger
		SWO	O	Serial Wire Output asynchronous trace output to debugger
		TRACEDATA0	O	Synchronous CPU trace data bit3
28	34	PC3	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
		JTDI	I	JTAG data in from debugger
		TRACECLK	O	Synchronous CPU trace clock
29	35	PC4	I/O	Digital I/O Either Enable with GPIO_DBGCFG[5]
		JTMS	I	JTAG mode select from debugger
		SWDIO	I/O	Serial Wire bidirectional data to/from debugger

10. Block Diagram

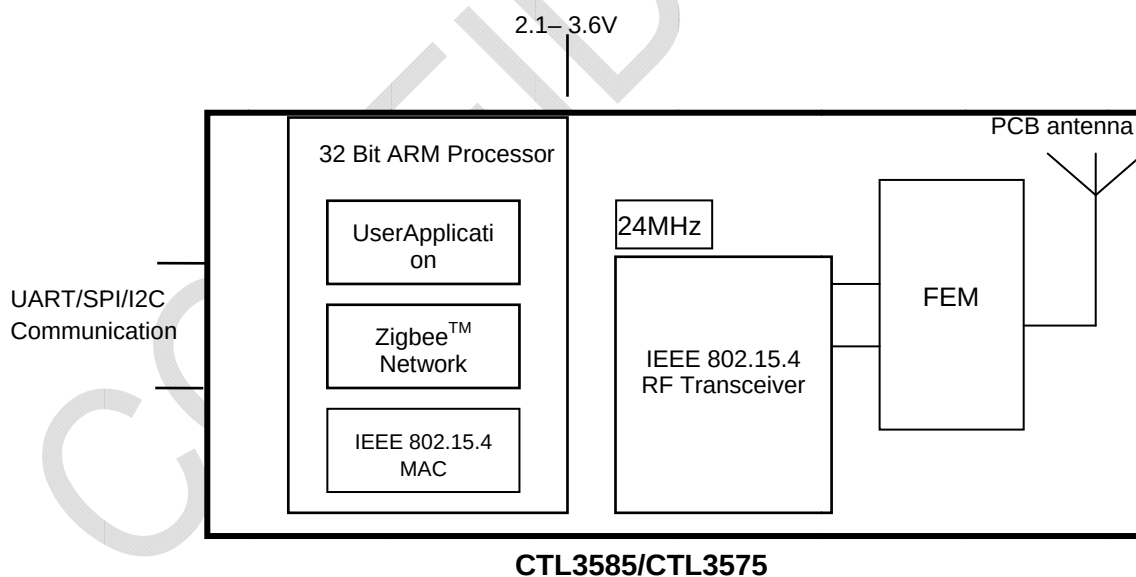


Figure 3: Block Diagram

11. RF Frequency Detail

The following table shows the RF channels as defined by the IEEE 802.15.4 standard.

RF channel	Frequency
11	2405MHz
12	2410MHz
13	2415MHz
14	2420MHz
15	2425MHz
16	2430MHz
17	2435MHz
18	2440MHz
19	2445MHz
20	2450MHz
21	2455MHz
22	2460MHz
23	2465MHz
24	2470MHz
25	2475MHz
26	2480MHz

Note: the output power of CTL3585/CTL3575 should be configured lower than -24dBm for 2480M channel to Comply FCC requirement.

The use of RF frequencies and maximum allowed RF power should according to different national regulations. The CTL3585/CTL3575 are complying with the applicable regulations for the world wide 2.4GHz ISM band.

The following table is the setting for the CTL3585 and CTL3575 to US market:

FCC		
Channel	CH11~25	CH26
Freq(MHz)	2405~2475	2480
Ember setting	-4dBm +No boost	-24dBm + No boost

The following table is the setting for the PA:

PA SETTINGS			
	PB3	PC1	PC5
ALL OFF	0	0	0
RX BY PASS	0	1	0
LNA	1	1	0
TX	X	1	1

12. PCB Layout Recommendations

Please reference Mechanical Dimensions shown in next section for PCB layout.

The area underneath the module should be covered with solder mask in order to prevent short circuit on the test pads on the back side of the module. A solid ground plane under the module is preferred.

As the module integrated with onboard PCB trace antenna, the mounting position of the module will have great impact on the RF performance. There should not be any trace, ground plane or metal part underneath or nearby the area of the onboard PCB trace antenna. The figure below shows an example how the module positioned on the mother PCB.

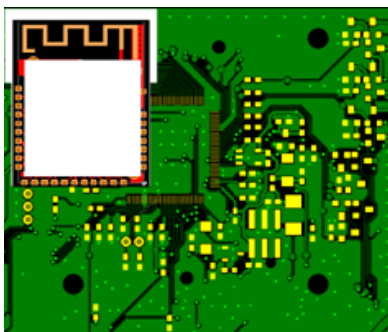
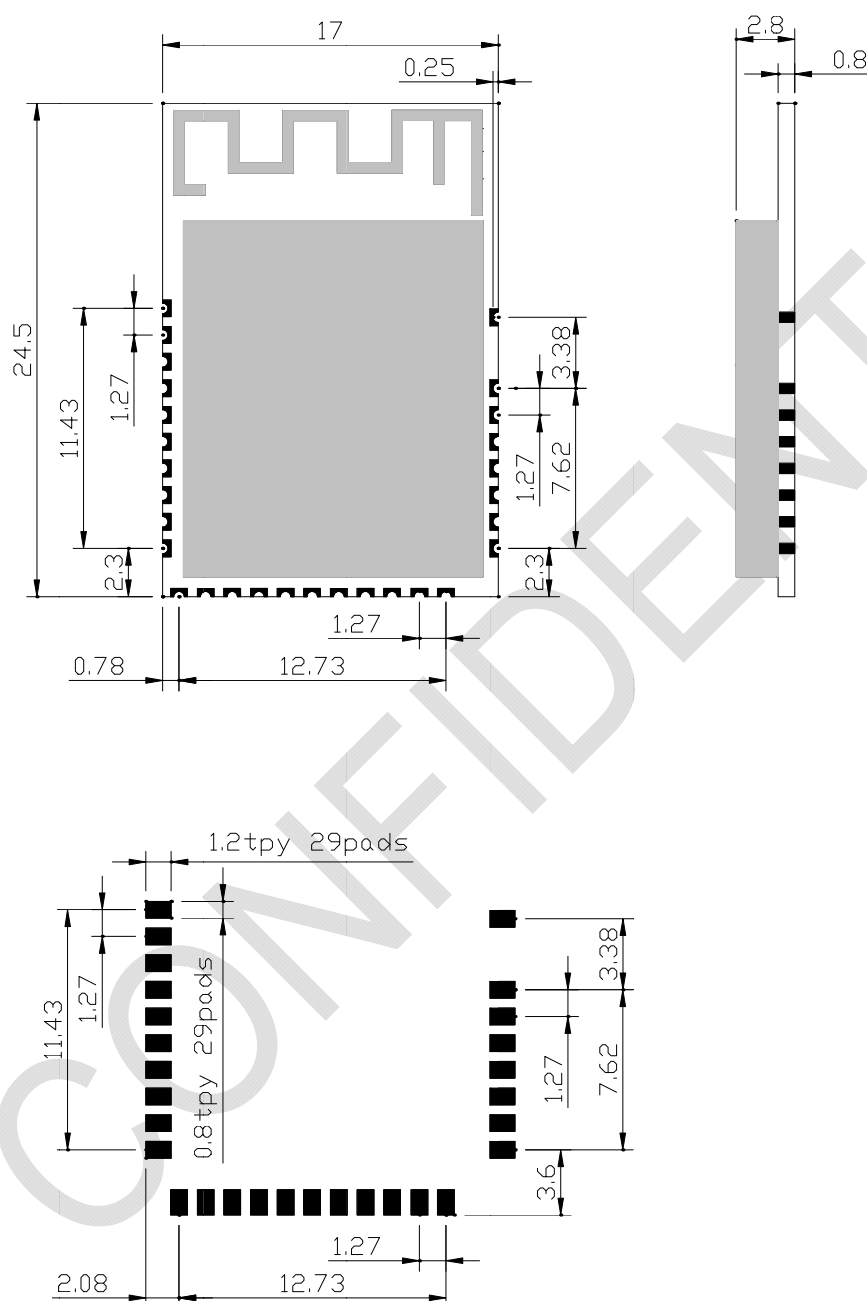


Figure 4: A recommended placement of the module on a main PCB

Figure 5: Mechanical Dimensions of CTL3585/CTL3575



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Regulatory Information

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Radiation Exposure Statement

The modular can be installed or integrated in mobile or fix devices only. This modular cannot be installed in any portable device, for example, USB dongle like transmitters is forbidden.

This modular complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This modular must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: 2AAUQ-CTL3575 or Contains FCC ID: 2AAUQ-CTL3575"

When the module is installed inside another device, the user manual of this device must contain below warning statements;

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.

2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.

IC Statement:

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme aux CNR exemptes de licence d'Industrie Canada. Son fonctionnement est soumis aux deux conditions suivantes :

- (1) Ce dispositif ne peut causer d'interférences ; et
- (2) Ce dispositif doit accepter toute interférence , y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

IC Radiation Exposure Statement

The modular can be installed or integrated in mobile or fix devices only. This modular cannot be installed in any portable device, for example, USB dongle like transmitters is forbidden.

This modular complies with IC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This modular must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

Cette modulaire doit être installé et utilisé à une distance minimum de 20 cm entre le radiateur et le corps de l'utilisateur.

If the IC number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains

IC: 1700A-CTL3575"

when the module is installed inside another device, the user manual of this device must contain below warning statements;

1. This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

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Contact information

COMPUTIME CORPORATE HQ

9/F Tower One, Lippo Centre,
89 Queensway,
Hong Kong
Tel: +852.2260.0300
Fax: +852.2790.3996
e-mail: hq@computime.com

COMPUTIME NORTH AMERICA HQ,

4700 Duke Dr.
Suite 200
Mason OH 45040
USA
Tel: +1(513).398.2579
Fax: +1(513).754.8955
e-mail: na@computime.com

Cincinnati Technologies

4700 Duke Dr.
Suite 200
Mason OH 45040
USA
Tel: +1(513).754.8935
Fax: +1(513).754.8955
e-mail: ctws@computime.com

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