MT7628DAN Core Module

Oolite V3.5_Module _SPEC_EN

Specification Version V1.0.2

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June 12, 2018

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Revision	Date	Contents of Revision Change	Remark
1.0.0	2018-03-28	First release	James
1.0.1	2018-03-28	Update pictures	James
1.0.2	2018-03-28	Add Pins Map	James

INTRODUCTION

Oolite V3.5 is powerful, reliable,easy to use and with extremely small size(23.7mm x 23.7mm x 2.7mm).Low power consumption so can use on IOT device.

MT7628DAN with 580/575 MHz MIPS 24KEc with 64 KB I-Cache and 32 KB D-Cache. WiFi: 2T2R 2.4 GHz With 300Mbps 802.11 b/g/n. MCM 64 Mbytes DDR2 KGD(Build in MT7628DAN Chipset) .16MB SPI NOR Flash ROM(8MB/16MB/32MB/64MB optional).

The MT7628DAN router-on-a-chip includes an 802.11n MAC and baseband, a 2.4 GHz radio and FEM, a 575/580 MHz MIPS® 24K™ CPU core, a 5-port 10/100 fast ethernet switch. The MT7628DAN includes everything needed to build an AP router from a single chip. The embedded high performance CPU can process advanced applications effortlessly, such as routing, security and VoIP. The MT7628DAN also includes a selection of interfaces to support a variety of applications, such as a USB port for accessing external storage.

FEATURES:

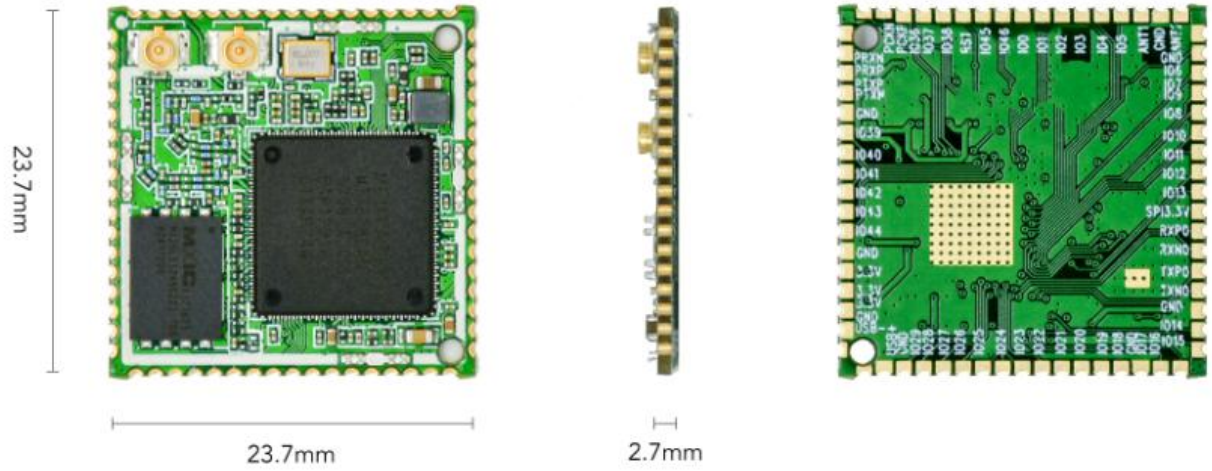
- CPU: MT7628DAN with 580/575 MHz MIPS 24KEc
- RAM: MCM 64 Mbytes DDR2 KGD(Build in MT7628DAN Chipset)
- Flash: 16MBytes SPI NOR Flash ROM(8MB/16MB/32MB/64MB optional)
- WiFi: SISO for 802.11b/g, MIMO for 802.11n20/n40.
- GPIO: 37(total and share with), High-speed UART for console support
- USB: 1 x USB 2.0 master interface, support USB hub extension
- Ethernet Port : 5-port 10/100 FE PHY in Gateway Mode
- Ethernet Port : 1-port 10/100 FE PHY in IOT Mode
- Mini-Pcie: 1×Mini-PCIE interface
- Antenna: 2 × IPEX external antenna(default) or use the stamp hole pins interface
- UART(Debug): serial debugging interface has lead out.
- Power supply voltage: 3.3V
- Size: 23.7mm x 23.7mm x 2.7mm (without shield)

FUNCTIONAL BLOCK DIAGRAM(MT7628DAN)

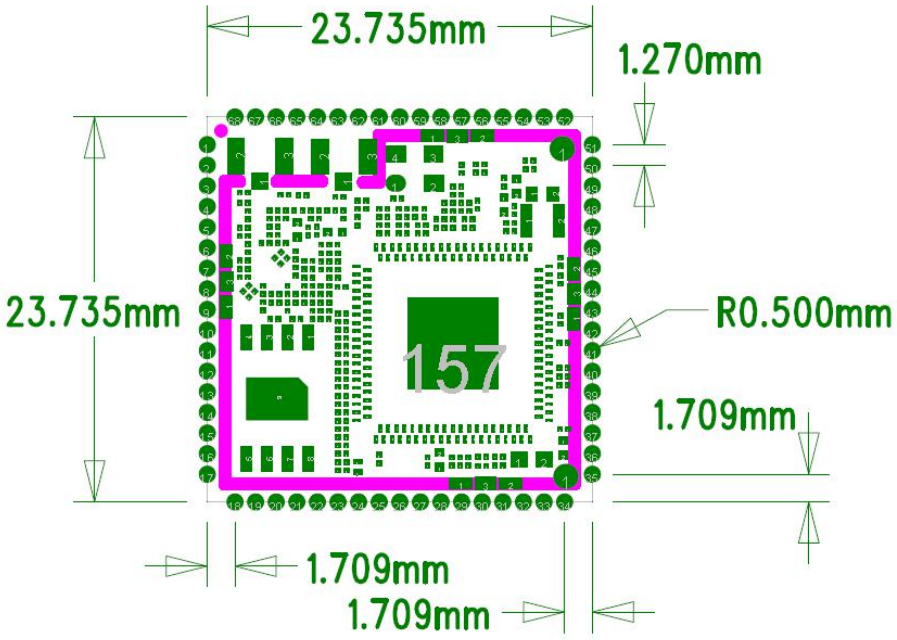
Features	MT7628DAN
CPU	MIPS24KEc (575/580 MHz)
Total DMIPs	580 x 1.6 DMIPs
I-Cache, D-Cache	64 KB, 32 KB
L2 Cache	n/a
Memory	
DDR2	512 Gb, 193 MHz, MCM
SPI Flash	3B addr mode (max 128Mbit) 4B addr mode (max 512Mbit)
SD	SD-XC (class 10)
RF	2T2R 802.11n 2.4 GHz
PCIe	1
USB 2.0	1
Switch	5p FE SW
I2S	1
PCM	1
I2C	1
UART	2 (Lite)
JTAG	1
Package	DR-QFN156- 12 mm x 12 mm

PICTURES

MECHANICAL



Length	Width	Height (without shield)
23.7mm (Tolerance:±0.2mm)	23.7mm (Tolerance:±0.2mm)	2.7mm (Tolerance:±0.2mm)



PIN DEFINITION

Pin	Name	Type	Description
1	GND	-	Exposed ground pad
2	SPI_CS1	O,IPD	SPI chip select1/GPIO#6
3	SPI_CLK	O,IPD	SPI clock/GPIO#7
4	SPI_MISO	I/O	SPI Master input/Slave output GPIO#9
5	SPI_MOSI	I/O,IPD	SPI Master output/Slave input GPIO#8
6	SPI_CS0	O	SPI chip select0/GPIO#10
7	GPIO#11	I/O,IPD	GPIO#11
8	UART_TXD0	O,IPD	UART0 Lite TXD/GPIO#12
9	UART_RXD0	I	UART0 Lite RXD/GPIO#13
10	3.3V	-	Supply voltage for digital blocks
11	MDI_RP_P0	A	10/100 PHY Port #0 RXN
12	MDI_RN_P0	A	10/100 PHY Port #0 RXP
13	MDI_TP_P0	A	10/100 PHY Port #0 TXN
14	MDI_TN_P0	A	10/100 PHY Port #0 TXP
15	GND	-	Exposed ground pad
16	MDI_TP_P1	A	SD-XC/eMMC/GPIO#14
17	MDI_TN_P1	A	SD-XC/eMMC/GPIO#15

Note:

- IPD : Internal pull-down
- IPU : Internal pull-up
- I : Input
- O : Output
- IO : Bi-directional

Pin	Name	Type	Description
18	MDI_RP_P1	A	SD-XC/eMMC/GPIO#16
19	MDI_RN_P1	A	SD-XC/eMMC/GPIO#17
20	GND	-	Exposed ground pad
21	MDI_RP_P2	A	SD-XC/eMMC/GPIO#18
22	MDI_RN_P2	A	SD-XC/eMMC/GPIO#19
23	MDI_TP_P2	A	SD-XC/eMMC/GPIO#20
24	MDI_TN_P2	A	SD-XC/eMMC/GPIO#21
25	MDI_TP_P3	A	SD-XC/eMMC/GPIO#22
26	MDI_TN_P3	A	SD-XC/eMMC/GPIO#23
27	MDI_RP_P3	A	SD-XC/eMMC/GPIO#24
28	MDI_RN_P3	A	SD-XC/eMMC/GPIO#25
29	MDI_RP_P4	A	SD-XC/eMMC/GPIO#26
30	MDI_RN_P4	A	SD-XC/eMMC/GPIO#27
31	MDI_TP_P4	A	SD-XC/eMMC/GPIO#28
32	MDI_TN_P4	A	SD-XC/eMMC/GPIO#29
33	GND	-	Exposed ground pad
34	USP_DP	I/O	USB port0 data pin Data+

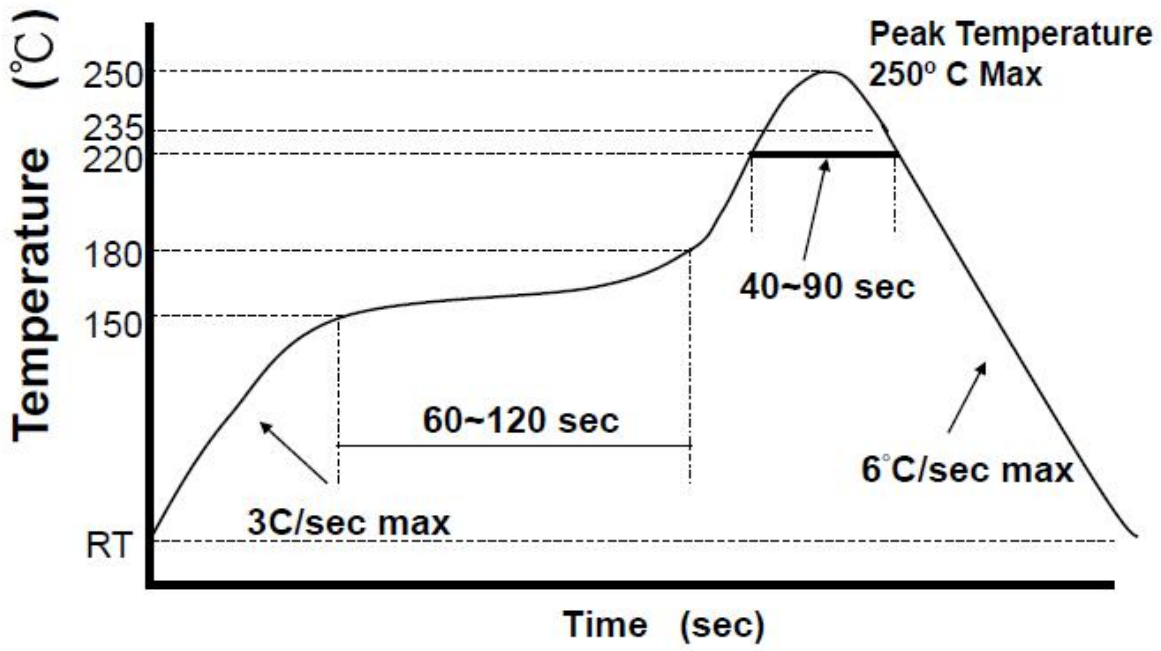
Pin	Name	Type	Description
35	USB_DN	I/O	USB port0 data pin Data-
36	GND	-	Exposed ground pad
37	3.3V	-	Supply voltage for digital blocks
38	3.3V	-	Supply voltage for digital blocks
39	3.3V	-	Supply voltage for digital blocks
40	GND	-	Exposed ground pad
41	WLED_N	O	WLAN Activity LED/GPIO#44
42	EPHY_LED0_N_JTDO	I/O	Port#0 activity LED/GPIO#43/JTAG_TDO
43	EPHY_LED1_N_JTDI	I/O	Port#1 activity LED/GPIO#42/JTAG_TDI
44	EPHY_LED2_N_JTMS	I/O	Port#2 activity LED/GPIO#41/JTAG_TMS
45	EPHY_LED3_N_JTCLK	I/O	Port#3 activity LED/GPIO#40/JTAG_CLK
46	EPHY_LED4_N_JTRST_N	I/O	Port#4 activity LED//GPIO#39/JTAG_TRST_N
47	GND	-	Exposed ground pads
48	PCIE_TXN0	I/O	PCIe0 differential transmit TX -
49	PCIE_TXP0	I/O	PCIe0 differential transmit TX +
50	PCIE_RXP0	I/O	PCIe0 differential transmit RX +
51	PCIE_RXN0	I/O	PCIe0 differential transmit TX -

Pin	Name	Type	Description
52	PCIE_CKN0	O	External reference clock output (negative)
53	PCIE_CKP0	O	External reference clock output (positive)
54	PERST_N	O,IPD	PCIe device reset/GPIO#36
55	REF_CLK0	O,IPD	Reference Clock Ouptut/GPIO#37
56	WDT_RST_N	O	Watchdog Reset/GPIO#38/SW Reset
57	PORST_N	O,IPU	CPURST_N/Power on reset/HW Reset
58	UART_TXD1	O,IPU	UART1 Lite TXD/GPIO#45
59	UART_RXD1	I	UART1 Lite RXD/GPIO#46
60	I2S_SDI	O	I2S data input/GPIO#0
61	I2S_SDO	I/O,IPD	I2S data output/GPIO#1
62	I2S_WS	O	I2S word select/GPIO#2
63	I2S_CLK	I/O	I2S clock/GPIO#3
64	I2C_CLK	I/O	I2C clock/GPIO#4
65	I2S_SD	I/O	I2C Data/GPIO#5
66	WiFi ANT1	A	WiFi ANT1
67	GND	-	Exposed ground pad
68	WiFi ANT1	A	WiFi ANT2

ENVIRONAMENT

Power Supply	3.3V (2.97V-3.63V)
Operating Temperature	-20℃ ~ 55℃
Operating Humidity	<60% non-condensing
Storage Temperature	0℃ ~ 50℃
Storage Humidity	Storage Humidity: <90% non-condensing in sealed

REFLOW PROFILE GUIDELINE



Notes:

1. Reflow profile guideline is designed for SnAgCulead-free solder paste.
2. Reflow temperature is defined at the solder ball of package/or the lead of package.
3. MTK would recommend customer following the solder paste vendor's guideline to design a profile appropriate your line and products.
4. Appropriate N2 atmosphere is recommended since it would widen the process window and mitigate the risk for having solder open issues.

Modular installation instrucations

WIFI Module -OoliteV3.5 Integrates high-speed GPIO and peripheral interface.Please pay attention to the installation direction (pin direction).

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.
This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter.
NOTE:
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.
These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the followingmeasures:
-- Reorient or relocate the receiving antenna.
-- Increase the separation between the equipment and receiver.
-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-- Consult the dealer or an experienced radio/TV technician for help.

FCC ID: 2AB5EOOLITE

ATTENTION
This device is intended only for OEM integrators under the following conditions:
1) The antenna must be installed such that 20 cm is maintained between the antenna and users
2) This device and its antenna(s) must not be co‑located with any other transmitters except in accordance with FCC multi‑transmitter product procedures. Referring to the multi‑transmitter policy, multiple‑transmitter(s) and module(s) can be operated simultaneously without C2P.
3) For all products market in US, OEM has to limit the operation channels in CH1 to CH11 for 2.4G band by supplied firmware programming tool. OEM shall not supply any tool or info to the end‑user regarding to Regulatory Domain change.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio‑frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference and
(2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains FCC ID: 2AB5EOOLITE". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference and
(2) this device must accept any interference received, including interference that may cause undesired operation.