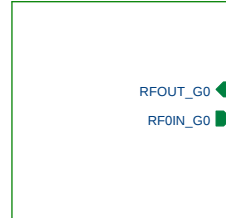


2-MEMORY



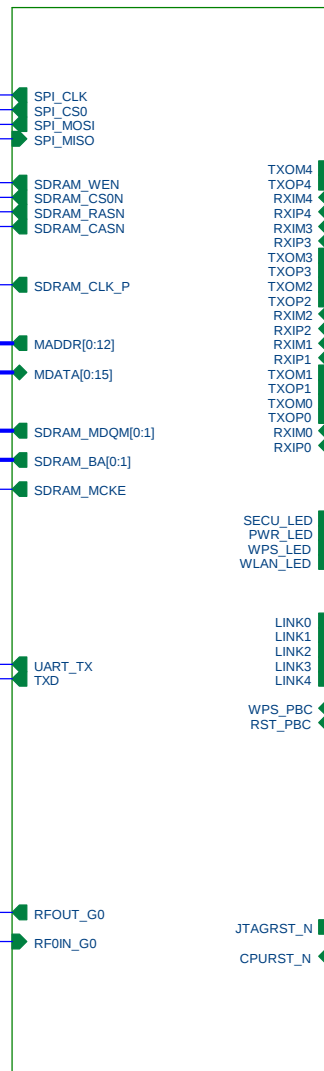
2-MEMORY

3-WLAN



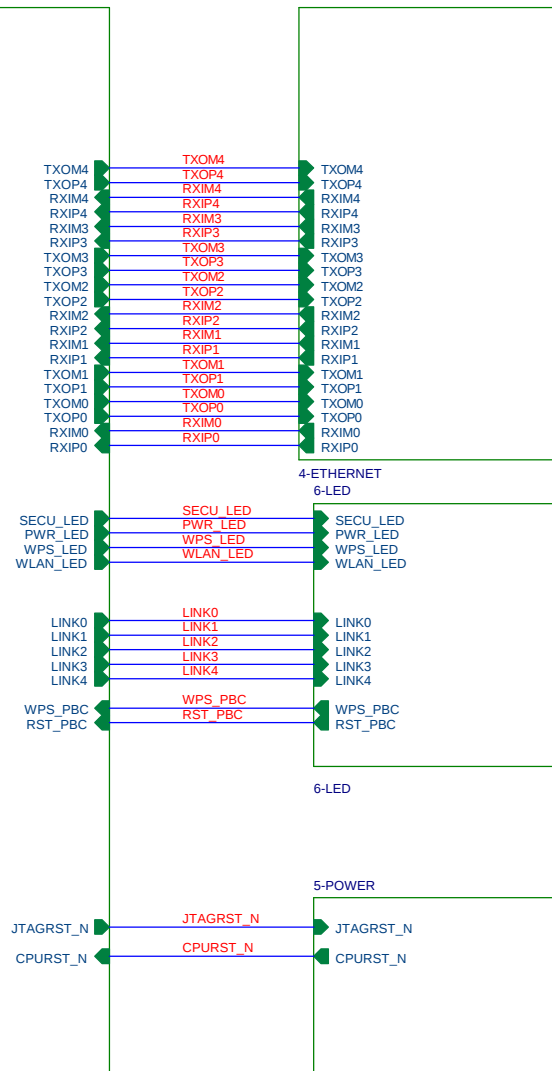
3-WLAN

1-CPU-RT5350



1-CPU-RT5350

4-ETHERNET



6-LED

5-POWER

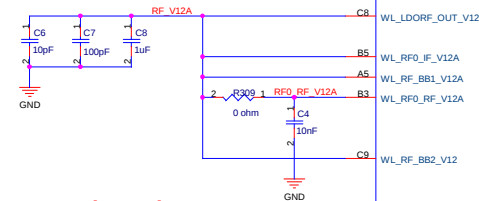
5-POWER

Filename:
AP-RT5350-V22-SPI-SDRAM-1X1-110713.DSN

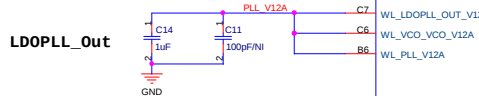
		<i>RALINK TECHNOLOGY, CORP. CONFIDENTIAL</i>		
		Title 11n 2.4G AP-RT5350		
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LDORF_Out

C8 layout close D8

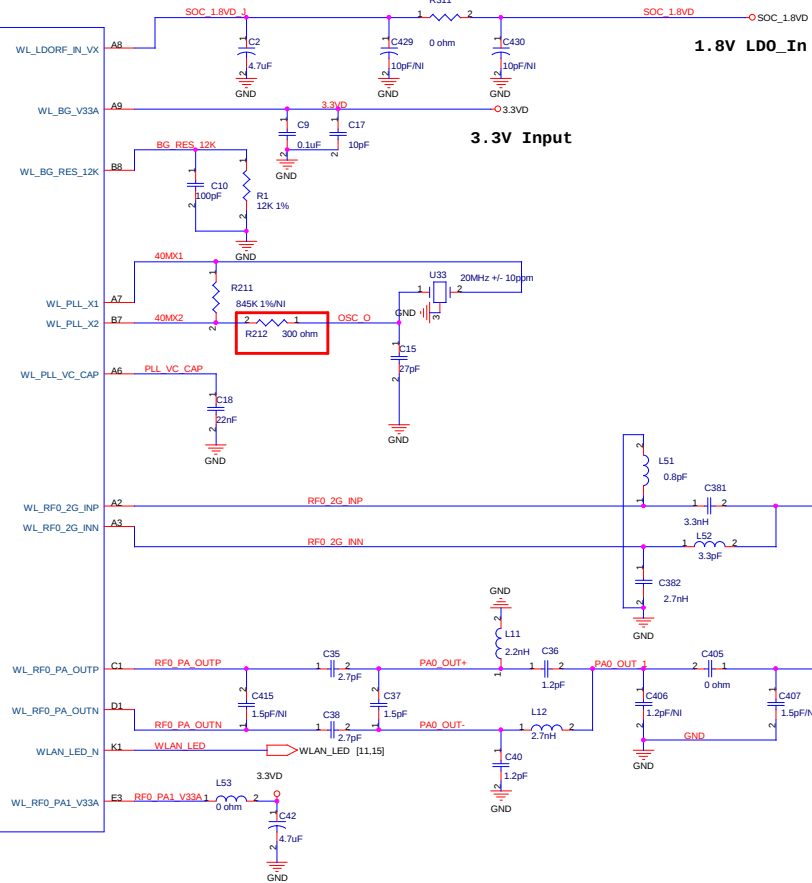
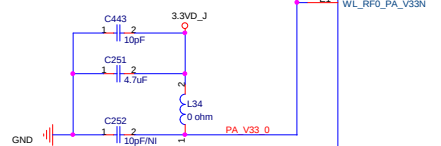


C11 layout close C7



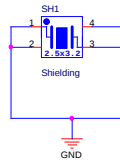
LDOPLL_Out

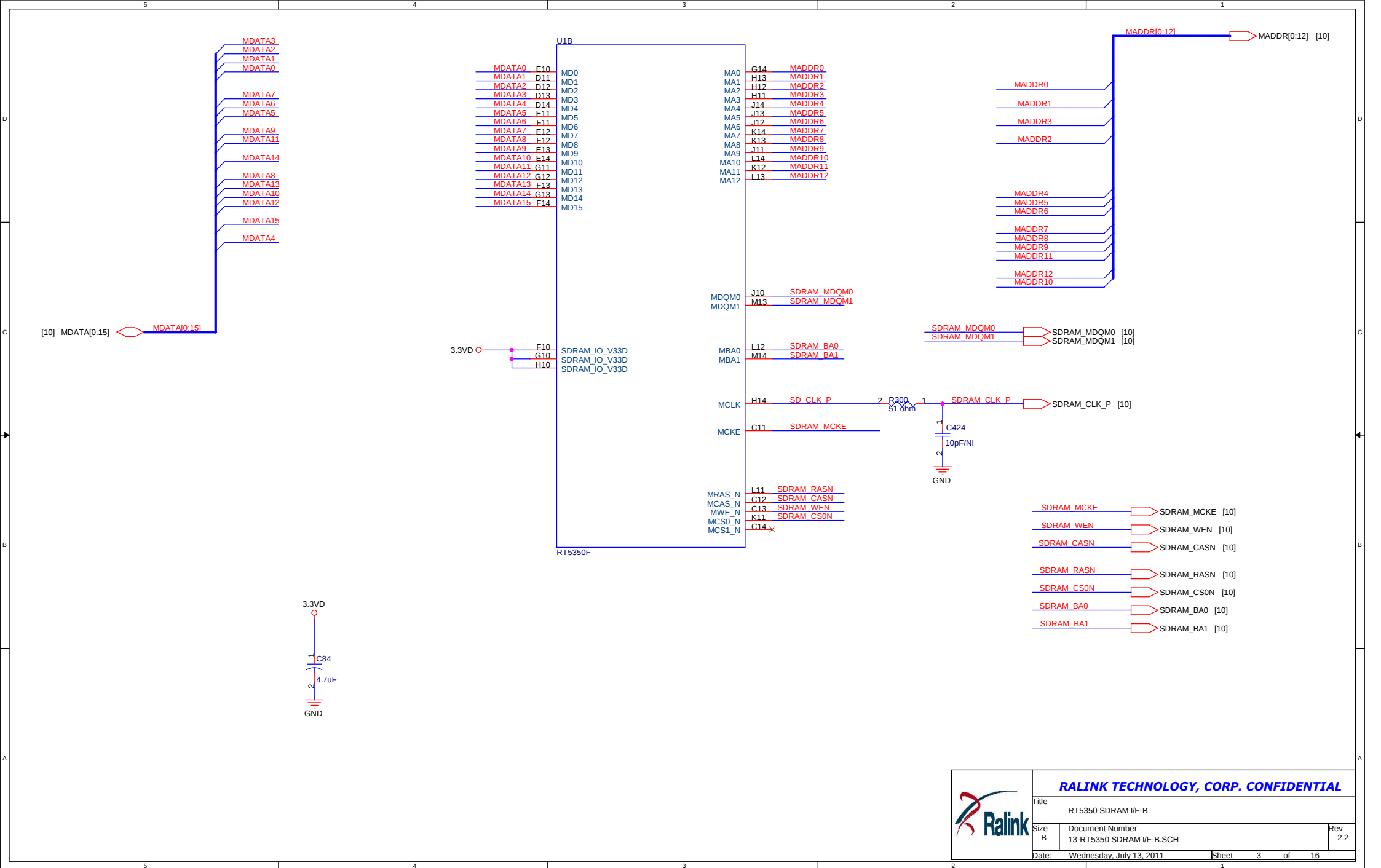
L34 ,C252 layout close C1 and F1

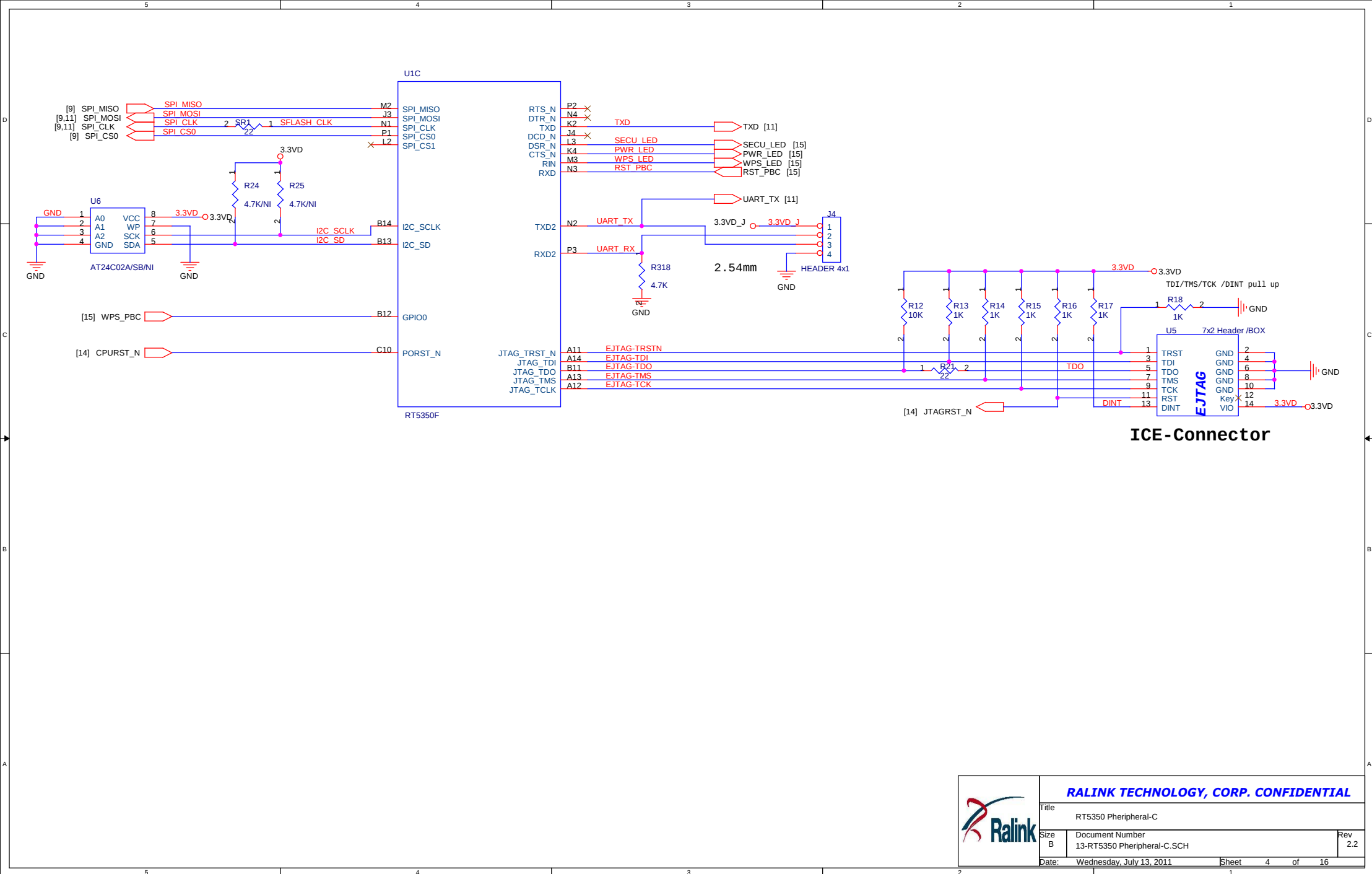


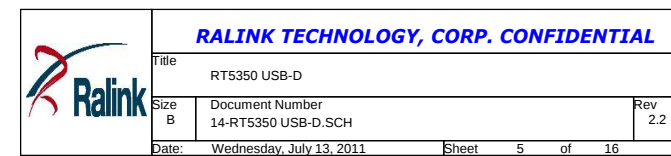
1.8V LDO_In

3.3V Input

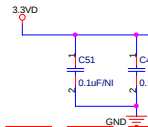








Close to RT5350



Close to RT5350



U1E

EPHY_V33A
EPHY_V33A
EPHY_V33A
EPHY_V33A

EPHY_TXN_p3
EPHY_TXP_p3
EPHY_RXN_p3
EPHY_RXP_p3

EPHY_TXN_p2
EPHY_TXP_p2
EPHY_RXN_p2
EPHY_RXP_p2

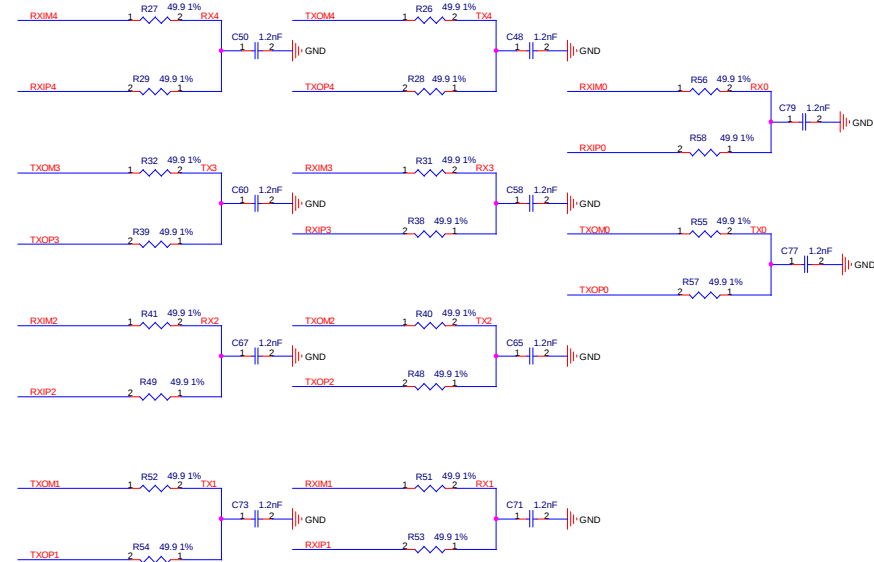
EPHY_TXN_p1
EPHY_TXP_p1
EPHY_RXN_p1
EPHY_RXP_p1

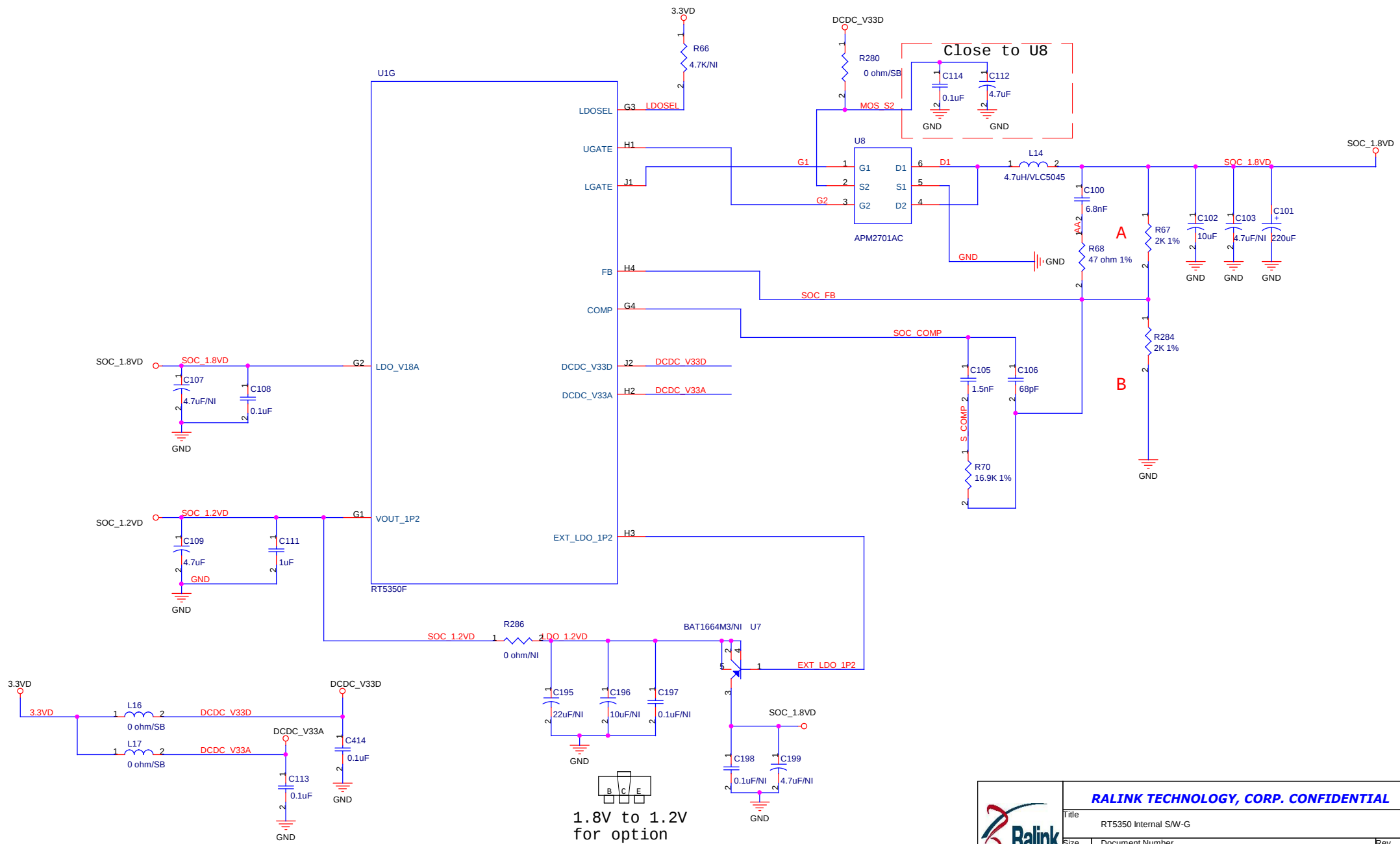
EPHY_TXN_p0
EPHY_TXP_p0
EPHY_RXN_p0
EPHY_RXP_p0

EPHY_LED4_N
EPHY_LED3_N
EPHY_LED2_N
EPHY_LED1_N
EPHY_LED0_N

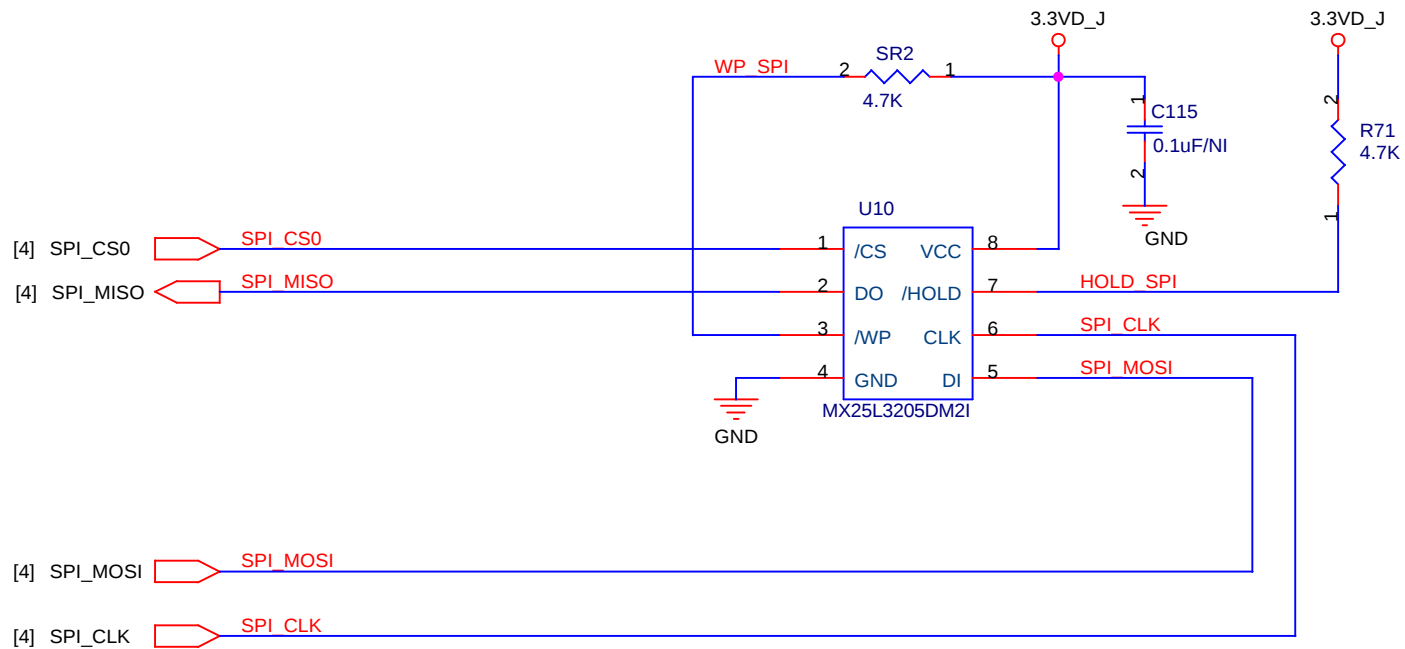
RT5350F

PHY address 5'd0	-> Internal PHY for port 0
PHY address 5'd1	-> Internal PHY for port 1
PHY address 5'd2	-> Internal PHY for port 2
PHY address 5'd3	-> Internal PHY for port 3
PHY address 5'd4	-> Internal PHY for port 4
PHY address 5'd5	-> default for the external Port 5
PHY address 5'd5 ~ 5'd31 are free for the external PHY.	



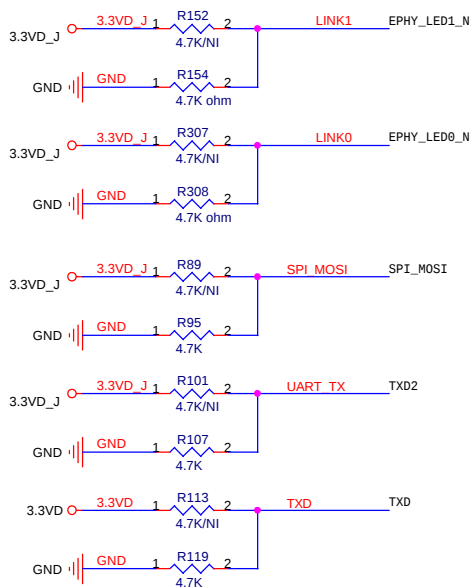
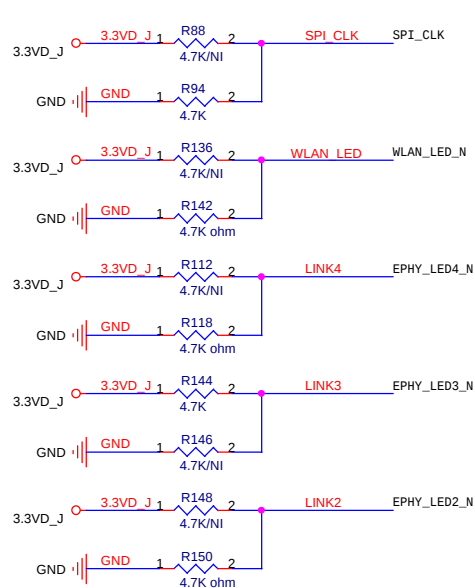
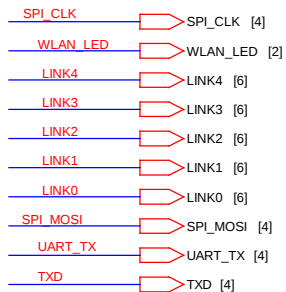


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RT5350 Boot Up Strapping

Pin Name	Description	Value=0	Value=1
SPI_CLK	XTAL_FREQ_HI	20MHz	40MHz
WLAN_LED_N	Big Endian	Little Endian	Big Endian
EPHY_LED4_N	DRAM_FROM_EE	from boot strapping	from EEPROM
{EPHY_LED3_N, EPHT_LED2_N}	DRAM_SIZE	INIC/AP(SDR) 00: 2MB/8MB 01: 8MB/16MB 10: 16 MB/32 MB, 32 MB*2 11: 32MB	
{EPHY_LED1_N, EPHT_LED0_N}	CPU_CLK_SEL	CPU clock select 00: 360MHz 01: Reserved 10: 320MHz 11: 300MHz	
{SPI_MOSI, TXD2, TXD}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes 000 : Normal mode(boot fromSPI serial flash) 001 : iNIC-USB mode 010 : Reserved 011 : Reserved 100 : Reserved 101 : iNIC-PHY mode 110 : SCAN mode 111 : TEST/DEBUG mode	



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