General Description

BDE-LE2340RGEC is a Bluetooth® 5.4 Low Energy, Thread, and Proprietary 2.4-GHz wireless module series based on Texas Instruments (TI)'s single-chip wireless microcontroller (MCU) CC2340R. In order to fulfil different integration scenarios, we provide different variants for this module series. They are listed and described in Table 1.

BDE-LE2340RGEC module series integrates an Arm® Cortex®-M0+ MCU, which supports Bluetooth® 5.4 Low Energy, SimpleLink™ TI 15.4-stack and Proprietary systems. This device is optimized for low-power wireless communication with on-chip dual image Over the Air Download (OAD) support in building automation (wireless sensors, lighting control, beacons), asset tracking, medical, retail EPOS (electronic point of sale), ESL (electronic shelf label), and personal electronics (toys, HID, stylus pens) markets.

BDE-LE2340RGEC module series is with ultra-low standby current less than 0.71 μA with RTC operational and full RAM retention that enables significant battery life extension especially for applications with longer sleep intervals. The module series supports for Bluetooth® 5 features: High Speed Mode (2 Mbps PHY), Long Range (LE Coded 125 kbps and 500 kbps PHYs), Privacy 1.2.1 and Channel Selection Algorithm #2, as well as backwards compatibility and support for key features from the Bluetooth® 4.2 and earlier Low Energy specifications.

BDE-LE2340RGEC module series highly integrates the radio with required passives, high-frequency clock, low-frequency clock, filter, antenna, etc., and also a fully-qualified Bluetooth® 5.4 software protocol stack and profiles from TI. It can work standalone without using an external MCU. With its best-in-class radio performance, ultra-low power, small form factor and low cost, the BDE-LE2340RGEC module series is the best choice for the applications that are sensitive to power consumption, size and cost.

Table 1. Module Variants

Orderable Part Number	Chipset	Flash (KB)	SRAM (KB)	Antenna Options	On-board SPI Flash (Mbit)	Operating Temperature (℃)
BDE-LE2340R52GEAC	CC2340R52N0RGER	512	36	PCB antenna	0	-40 ~ 85
BDE-LE2340R21GEAC	CC2340R21N0RGER	256	28	PCB antenna	0	-40 ~ 85

Key Features

- **Wireless microcontroller**
  - Optimized 48-MHz Arm® Cortex®-M0+ processor
  - 512/256 KB of in-system programmable flash
  - 12 KB of ROM for bootloader and drivers
  - 36/28 KB of ultra-low leakage SRAM. Full RAM retention in standby mode
  - 2.4-GHz RF transceiver compatible with Bluetooth®5.4 Low Energy and IEEE 802.15.4 PHY and MAC
  - Supports over-the-air upgrade (OTA)
  - Serial Wire Debug (SWD)
- **Low power consumption**
  - MCU consumption:
    - 2.6 mA active mode, CoreMark®
    - 53 μA/MHz running CoreMark®
    - <710 nA standby mode, RTC, 36 KB RAM
    - 165 nA shutdown mode, wake-up on pin

- Radio Consumption:
  - 5.3 mA RX
  - 5.1 mA TX at +0 dBm
  - <11.0 mA TX at +8 dBm

- **Wireless protocol support**
  - Bluetooth® 5.4 Low Energy
  - Thread
  - Proprietary systems
- **High performance radio**
  - -101 dBm for Bluetooth® Low Energy 125 kbps
  - -94.5 dBm for Bluetooth® Low Energy 1 Mbps
  - Output power up to +8 dBm with temperature compensation
- **MCU peripherals**
  - Up to 10 I/O Pads
    - 2 IO pads SWD, muxed with GPIOs
    - 2 IO pads LFXT, muxed with GPIOs (On-board LFXT is populated by default, these two IOs are not exposed by default. They can be reserved for users if on-board LFXT is not required. Contact BDE if you need to use these two IOs)
    - Up to 8 DIOs (analog or digital IOs)
    - Four IOs are assigned to on-board SPI flash in SPI variants, refer to Section 2.1
  - 3x 16-bit or 1x 24-bit general-purpose timers, quadrature decode mode support
  - 12-bit ADC, 1.2 Msps with external reference, 267 ksps with internal reference, up to 12 external ADC inputs
  - 1x low power comparator
  - 1x UART
  - 1x SPI
  - 1x I^2C
  - Real-time clock (RTC)
  - Integrated temperature and battery monitor
  - Watchdog timer
- **Security enablers**
  - AES 128-bit cryptographic accelerator
  - Random number generator from on-chip analog noise
- **Integrated 32-Mbit SPI flash (SPI flash variants)**
- **Additional integrated components**
  - 48-MHz HFXT
  - 32.768-kHz LFXT
  - RF filter and passive components
- **Antenna options**
  - Integrated PCB antenna
- **Operating range**
  - 1.71-V to 3.8-V single supply voltage
  - Operating temperature range:
    - -40℃ to +85℃
- **Package**
  - Dimension:
    - 11.5 mm x 13.5 mm x 2.2 mm (-A variants)
  - RoHS-compliant package
- **Development options**
  - Functions as a SoC using TI SDK
  - Functions as a UART pass-through using BDE's pre-programmed BDE-SPP firmware with AT comments
  - Functions as a Wireless Network Process (WNP)
- **Qualification and regulatory compliance**
  - Bluetooth SIG, DN: Q332693
  - FCC ID: 2ABRU-2340RGEC
  - IC: 25657-2340RGEC
  - CE-RED

Applications

- Medical
  - Home healthcare – blood glucose monitors, blood pressure monitor, CPAP machine, electronic thermometer
  - Patient monitoring & diagnostics – medical sensor patches

- Personal care & Fitness – electric toothbrush, wearable fitness & activity monitor

- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor
  - Fire safety system – smoke and heat detector
  - Video surveillance – IP network camera
- Lighting
  - LED luminaire
  - Lighting control – daylight sensor, lighting sensor, wireless control
- Factory automation and control
- Retail automation & payment – Electronic point of sale
  - Electronic shelf label
- Communication equipment
  - Wired networking
  - Wireless LAN or Wi-Fi access points, edge router
- Personal electronics
  - Connected peripherals – consumer wireless module, pointing devices, keyboards and keypads
  - Gaming – electronic and robotic toys
  - Wearables (non-medical) – smart trackers, smart clothing

Reference

[1] CC2340R5 resources: https://www.ti.com/product/CC2340R5
[2] CC2340R2 resources: https://www.ti.com/product/CC2340R2

Module Family

Table 2. Module Family

Model Number	Orderable Part Number	Chipset	Flash (KB)	SRAM (KB)	Antenna Options	GPIO	On-Board SPI Nor Flash (Mbit)	Operating Temperature (℃)
BDE-LE2340RGEAC	BDE-LE2340R52GEAC	CC2340R52N0RGER	512	36	PCB Trace Antenna	10	0	-40 ~ 85
	BDE-LE2340R21GEAC	CC2340R21N0RGER	256	28	PCB Trace Antenna	10	0	-40 ~ 85

Naming Convention

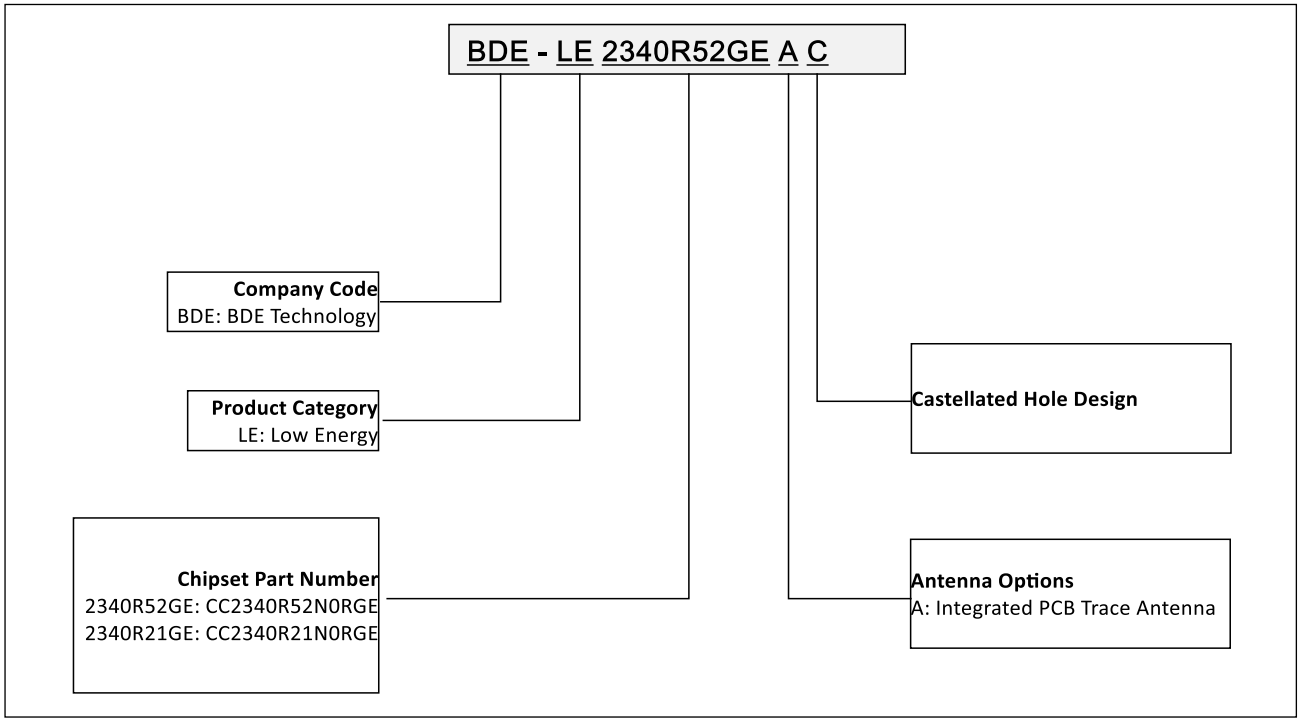

Figure 1. Module Naming Convention

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1. System Overview

1.1. Block Diagram

BDE-LE2340RGEC module series is based on the TI's CC2340R single chip wireless MCU. With clocks, other required passives and antenna/connector (optional) integrated, it allows faster time to market at reduced development cost.

The block diagram of the module series, as shown below, comprises:

- 48-MHz HFXT
- 32.768-kHz LFXT
- Power inductors and capacitors
- Pull-up resistor
- Matching circuit
- PCB antenna

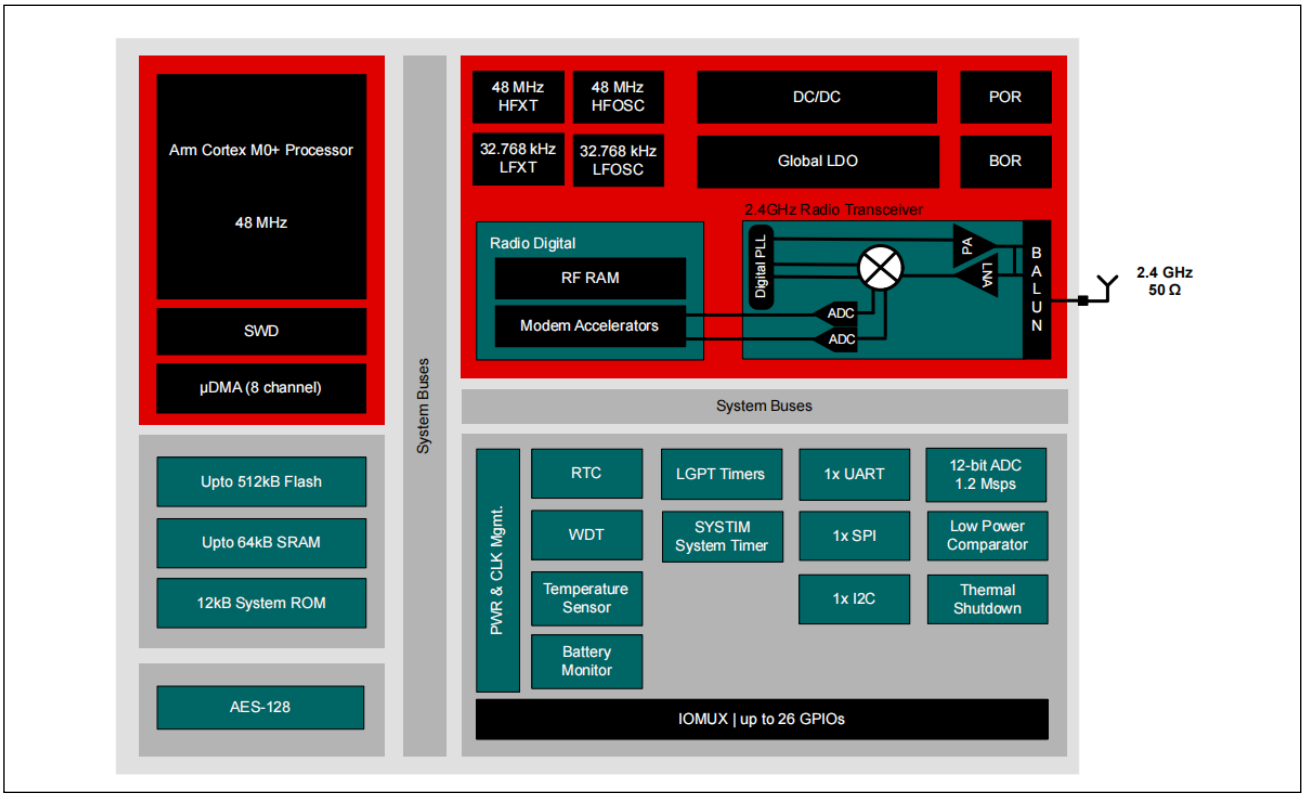


Figure 2. The block diagram of CC2340R5 (Adopted from CC2340R5 datasheet)

1.2. System CPU

The BDE-LE2340RGEC module series utilizes CC2340R SimpleLink™ Wireless MCU. The MCU contains an Arm® Cortex®-

M0+ system CPU, which runs the application, the protocol stacks, and the radio. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

1.3. Radio (RF Core)

The low-power RF Core (LRF) implements a high performance and highly flexible RF sub system containing RF and baseband circuitry in addition to a software defined digital radio (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The software-defined modem is not programmable by customers but is instead loaded with pre-compiled images provided in the radio driver in the SimpleLink™ CC23xx software development kit (SDK from TI). This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory, thus image loading from NV memory only occurs once after boot and also, no patching is required when exiting power modes.

1.3.1. Bluetooth 5.4 Low Energy

The RF Core offers full support for Bluetooth 5.4 Low Energy, including the high-speed 2 Mbps physical layer and the 500 kbps and 125 kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.4 stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.4 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth Low Energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.4 enables fast, reliable firmware updates.

1.4. Memory

Up to 512KB/256KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. A special flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and drivers are provided to configure the device. This configuration is done through the ccfg.c source file that is included in all provided examples.

The ultra-low leakage system static 36KB/28KB RAM (SRAM) can be used for both storage of data and execution of code.

Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. System SRAM is always initialized to zeroes upon code execution during boot.

The ROM includes device bootcode firmware handling initial device trimming operations, security configurations and device lifecycle management. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

The module also provides an option with integrated an on-board 32-Mbit SPI flash for the applications that need to store large application data.

1.5. Cryptography

The device comes with AES-128 cryptography hardware accelerator, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread.

The AES hardware accelerators supports the following block cipher modes and message authentication codes:

- AES ECB encrypt
- AES CBC encrypt
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AES GCM
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)

The device supports Random Number Generation (RNG) using on-chip analog noise as the non-deterministic noise source for the purpose of generating a seed for a cryptographically secure counter deterministic random bit generator (CTR-DRBG) that in turn is used to generate random numbers for keys, initialization vectors (IVs), and other random number requirements. Hardware acceleration of AES CTR-DRBG is supported.

1.6. Timer

A large selection of timers are available as part of the device. These timers are:

- Real-Time Clock (RTC)
- System Timer (SYSTIM)
- General Purpose Timers (LGPT)
- Watchdog timer

1.7. Serial Peripherals and I/O

The device provides 1x UART, 1x SPI and 1x I2C serial peripherals.

The SPI module supports both SPI controller and peripheral up to 12 MHz with configurable phase and polarity.

The UART module implements universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps and IRDA SIR mode of operation.

The I2C module is used to communicate with devices compatible with the I2C standard. The I2C interface can handle 100 kHz and 400 kHz operation, and can serve as both controller and target.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open source. Some GPIOs have high-drive capabilities, which are marked in bold in Section 2.1.

1.8. Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

1.9. µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

1.10. Debug

On-chip debug is supported through the serial wire debug (SWD) interface, which is an ARM bi-directional 2-wire protocol that communicates with the JTAG Test Access Port (TAP) controller and allows for complete debug functionality. SWD is fully compatible with TI's XDS family of debug probes.

1.11. Clock

The module has the following internal system clocks.

The 48 MHz HFCLK is used as the main system (MCU and peripherals) clock. This is driven by the internal 48 MHz RC Oscillator (HFOSC), which can track its accuracy against an external 48 MHz crystal (HFXT). Radio operation requires an

external 48 MHz crystal.

The 32.768 kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer before or after Standby power mode. LFCLK can be driven by the internal 32.8 kHz RC Oscillator (LFOSC), a 32.768 kHz watch-type crystal, or clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32 kHz LFCLK signal to other devices, thereby reducing the overall system cost.

The module includes two crystals on board, a high frequency crystal (HFXT) with 48-MHz and a low frequency crystal (LFXT) with 32.768-KHz. The characteristics for two crystals can be found in Section 3.15.

1.12. Network Processor

Depending on the product configuration, the module can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC - with the application and protocol stack running on the system CPU inside the device). In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

1.13. Power Management

To minimize power consumption, the CC2340R supports a number of power modes and power management features. See Table 3.

Table 3. Power Modes

Mode	Software Configurable Power Modes (1)				Reset Pin Held
	Active	Idle	Standby	Shutdown	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
CPU register retention	Full	Full	Full (2)	No	No
SRAM retention	Full	Full	Full	Off	Off
48 MHz high-speed clock (HFCLK)	HFOSC (tracks HFXT)	HFOSC (tracks HFXT)	HFOSC (tracks HFXT)	Off	Off
32 kHz low-speed clock (LFCLK)	LFXT or LFOSC	LFXT or LFOSC	LFXT or LFOSC	Off	Off
Peripherals	Available	Available	IOC, BATMON, RTC, LPCOMP	Off	Off
Wake-up on RTC	N/A	Available	Available	Off	Off
Wake-up on pin edge	N/A	Available	Available	Available	Off

Mode	Software Configurable Power Modes (1)				Reset Pin Held
	Active	Idle	Standby	Shutdown	
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	On	On
Watchdog timer (WDT)	Available	Available	Available	Off	Off

(1) "Available" indicates that the specific IP or feature can be enabled by user application in the corresponding device operating modes. "On" indicates that the specific IP or feature is turned on irrespective of the user application configuration of the device in the corresponding device operating mode. "Off" indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode;
(2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode.

In the Active mode, both of MCU and AON (always-on) power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU.

In Idle mode the CPU is in sleep but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on state of the DMA and debug subsystem.

In Standby mode, only the AON domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. Pin Reset will also drive the device from Standby to Active. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In Shutdown mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a wake from shutdown pin wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset, or thermal shutdown reset, by reading the reset status register. The only state retained in this mode are the latched I/O state, 3V register bank, and the flash memory contents.

The power, RF and clock management for the module require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2340R software development kit (SDK). Therefore, BDE highly recommends using this software framework for all application development on the device. The complete SDK with FreeRTOS, device drivers, and examples are offered free of charge in source code.

1.14. Antenna

The module series provides three different types of antenna integration, integrated PCB antenna, U.FL connector and ANT pin for connecting external antenna. Detail characteristics for the antennas can be found in Section 3.3 and Table 29.

2. Pinout Functions

The module series is with LGA-48 package, 48 pas are exposed for user. This section describes pinout functions of the module in details.

2.1. Pinout Diagram

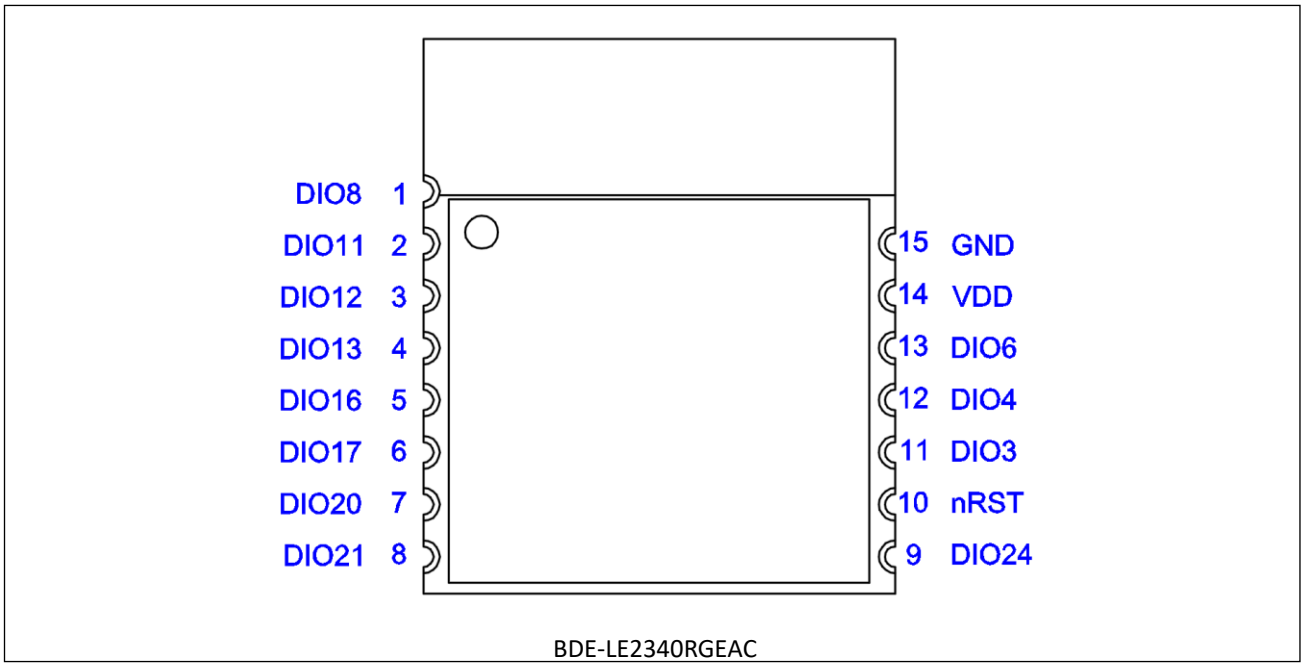


Figure 3. Pinout Diagram of BDE- LE2340RGEC Top View

The following I/O pins marked in **bold** in Figure 3 have high-drive capabilities:

- Pin 3, DIO12
- Pin 5, DIO16_SWDIO
- Pin 6, DIO17_SWDCK
- Pin 9, DIO24_A7

The following I/O pins marked in *italics* in Figure 3 have analog capabilities:

- Pin 7, DIO20_A11
- Pin 8, DIO21_A10
- Pin 9, DIO24_A7
- Pin 13, DIO6_A1

The following four I/O pins are assigned to on-board 32-Mbit SPI flash for SPI flash variants:

- Pin 2, SFL_CS_DIO11
- Pin 3, SFL_MISO_DIO12

- Pin 4, SFL_MOSI_DIO13
- Pin 9, SFL_CLK_DIO24_A7

2.2. Pinout Descriptions

Table 4 describes the definitions of the pins of the module. Pin number of CC2340R chip is also stated here, because the chip pin is referred to in the software design kit (SDK).

Table 4. Pinout Description (1)

Module Pin #	Pin Name	Type	CC2340R Pin #	Description
1	DIO8	I/O	3	GPIO
2	SFL_CS/DIO11	I/O	4	SFL_CS(2), GPIO
3	SFL_MISO/DIO12	I/O	5	SFL_MISO(2), GPIO, high-drive capability
4	SFL_MOSI/DIO13	I/O	6	SFL_MOSI(2), GPIO
5	DIO16_SWDIO	I/O	7	GPIO, SWD interface: mode select or SWDIO, high-drive capability
6	DIO17_SWDCK	I/O	8	GPIO, SWD interface: clock, high-drive capability
7	DIO20_A11	I/O	9	GPIO, analog capability
8	DIO21_A10	I/O	10	GPIO, analog capability
9	SFL_SCLK/DIO24_A7	I/O	12	SFL_SCLK(2),GPIO, analog capability, high-drive capability
10	nRESET	I	13	Reset, active low, internal 100Kpull-up and 100nF decouple
11	NC	-	-	NC or DIO3(4)
12	NC	-	-	NC or DIO4(4)
13	DIO6_A1	I/O	19	GPIO, analog capability
14	VDD(5)	Power		1.71-V to 3.8-V or 2.3-V to 3.8-V power supply
15	GND	GND	-	Ground

(1) For pin multiplexing details, refer to Table 6 and Table 7 or CC2340R SimpleLink™ 32-bit Arm® Cortex®-M0+ Bluetooth® Low Energy wireless MCU;
(2) Pin 25 (DIO3) and pin 28 (DIO4) are assigned as LFXT pins by default. They can be used as GPIOs if the on-board LFXT are unpopulated (by request);
(3) For operating voltage, please refer to Table 10.

2.3. Connections for Unused Pins

Table 5. Connections for Unused Pins

Function	Signal Name	Acceptable Practice	Proffered Practice
GPIO (Digital or analog)	DIOn	NC, GND or VDD	NC
SWD	DIO16_SWDIO, DIO17_SWDCK	NC, GND or VDD	NC

2.4. Peripheral Pin Mapping

Table 6. Peripheral Pin Mapping

Module Pin #	Chip Pin #	Pin Name	Signal Name	Signal Direction	Pin Mux Encoding
25	14	DIO3	GPIO3	I/O	0
			LFCI	O	1
			T0C1N	O	2
			LRFD0	O	3
			T3C1	I/O	4
			T1C2	O	5
			LFXT_P	I	6
			DTB7	O	7
28	15	DIO4	GPIO4	I/O	0
			T0C2N	O	1
			UART0TXD	O	2
			LRFD1	O	3
			SPI0PICO	I/O	4
			T0C2	O	5
			LFXT_N	I	6
			DTB8	O	7
2	19	DIO6_A1	GPIO6	I/O	0
			SPI0CSN	I/O	1
			I2C0SCL	I/O	2
			T1C2	O	3
			LRFD2	O	4
			UART0TXD	O	5
			ADC1/AREF+	I	6
			DTB6	O	7
4	3	DIO8	GPIO8	I/O	0
			SPI0SCLK	I/O	1
			UART0RTS	O	2
			T1C0N	O	3
			I2C0SDA	I/O	4
			T0C0N	O	5
			DTB3	O	7
7	4	DIO11	GPIO11	I/O	0
			SPI0CSN	I/O	1
			T1C2N	O	2
			T0C0	O	3
			LRFD0	O	4
			SPI0POCI	I/O	5
			DTB9	O	7
8	5	DIO12	GPIO12	I/O	0
			SPI0POCI	I/O	1

Module Pin #	Chip Pin #	Pin Name	Signal Name	Signal Direction	Pin Mux Encoding
			SPI0PICO	I/O	2
			UART0RXD	I	3
			T1C1	O	4
			I2C0SDA	I/O	5
			DTB13	O	7
9	6	DIO13	GPIO13	I/O	0
			SPI0POCI	I/O	1
			SPI0PICO	I/O	2
			UART0TXD	O	3
			T0C0N	O	4
			T1F	O	5
			DTB4	O	7
13	7	DIO16_SWDIO	GPIO16	I/O	0
			SPI0PICO	I/O	1
			UART0RXD	I	2
			I2C0SDA	I/O	3
			T1C2	O	4
			T1C0N	O	5
			DTB10	O	7
14	8	DIO17_SWDCK	GPIO17	I/O	0
			SPI0SCLK	I/O	1
			UART0TXD	O	2
			I2C0SCL	I/O	3
			T1C1N	O	4
			T0C2	O	5
			DTB11	O	7
17	9	DIO20_A11	GPIO20	I/O	0
			LPCO	O	1
			UART0TXD	O	2
			UART0RXD	I	3
			T1C0	O	4
			SPI0POCI	I/O	5
			ADC11	I	6
			DTB14	O	7
18	10	DIO21_A10	GPIO21	I/O	0
			UART0CTS	I	1
			T1C1N	O	2
			T0C1	O	3
			SPI0POCI	I/O	4
			LRFD1	O	5

Module Pin #	Chip Pin #	Pin Name	Signal Name	Signal Direction	Pin Mux Encoding
			ADC10/LPC+	I	6
			DTB15	O	7
21	12	DIO24_A7	GPIO24	I/O	0
			SPI0SCLK	I/O	1
			T1C0	O	2
			T3C0	O	3
			T0PE	O	4
			I2C0SCL	I/O	5
			ADC7/LPC+/LPC-	I	6
			DTB5	O	7

2.5. Peripheral Signal Descriptions

Table 7. Peripheral Signal Descriptions

Function	Signal Name	Module Pin #	Chip Pin #	Signal Direction	Description
ADC	ADC1	13	19	I	HP ADC channel 1 input
	ADC7	9	12		HP ADC channel 7 input
	ADC10	8	10		HP ADC channel 10 input
	ADC11	7	9		HP ADC channel 11 input
ADC Reference	AREF+	13	19	I	ADC external voltage reference, positive terminal
Clock	X32P	11	14	I	32-kHz crystal oscillator pin 1, Optional TCXO input
	X32N	12	15		32-kHz crystal oscillator pin 2
	LFCI	11	14		Low frequency clock input (LFXT bypass clock from pin)
Comparator	LPCO	7	9	O	Low power comparator output
Digital Test Bus	DTB3	1	3	O	Digital test bus output 3
	DTB4	4	6		Digital test bus output 4
	DTB5	9	12		Digital test bus output 5
	DTB6	13	19		Digital test bus output 6
	DTB7	11	14		Digital test bus output 7
	DTB8	12	15		Digital test bus output 8
	DTB9	2	4		Digital test bus output 9
	DTB10	5	7		Digital test bus output 10
	DTB11	6	8		Digital test bus output 11
	DTB13	3	5		Digital test bus output 13
	DTB14	7	9		Digital test bus output 14
	DTB15	8	10		Digital test bus output 15
GPIO	GPIO3	11	14	I/O	General-purpose input or output
	GPIO4	12	15		
	GPIO6	13	19		

Function	Signal Name	Module Pin #	Chip Pin #	Signal Direction	Description
	GPIO8	1	3		
	GPIO11	2	4		
	GPIO12	3	5		
	GPIO13	4	6		
	GPIO16	5	7		
	GPIO17	6	8		
	GPIO20	7	9		
	GPIO21	8	10		
	GPIO24	9	12		
I^2C	I2C0SCL	9	12	I/O	I^2C clock data
		13	19		
		6	8		
	I2C0SDA	1	3	I/O	I^2C data
		3	5		
		5	7		
LRF Digital Output	LRFD0	11	14	O	LRF digital output 0
		2	4		
	LRFD1	8	10		LRF digital output 1
		12	15		
	LRFD2	13	19		LRF digital output 2
SPI	SPI0SCLK	9	12	I/O	SPI clock
		1	3		
		6	8		
	SPI0POCI	8	10	I/O	SPI POCI
		2	4		
		3	5		
		4	6		
		7	9		
	SPI0CSN	13	19	I/O	SPI chip select
		2	4		
	SPI0PICO	12	15	I/O	SPI PICO
		3	5		
		4	6		
		5	7		
SWD	SWDIO	5	7	I/O	JTAG/SWD TCK. Reset default pinout
	SWDCK	6	8	I	JTAG/SWD TMS. Reset default pinout
Timers –Capture / Compare	T0C0	2	4	I/O	Capture/compare Output-0 from Timer-0
	T0C1	8	10		Capture/compare Output-1 from Timer-0
	T0C2	12	15		Capture/compare Output-2 from Timer-0

Function	Signal Name	Module Pin #	Chip Pin #	Signal Direction	Description
		6	8		
	T1C0	9	12	I/O	Capture/compare Output-0 from Timer-1
		7	9		
	T1C1	3	5		Capture/compare Output-1 from Timer-1
	T1C2	11	14		Capture/compare Output-2 from Timer-1
		13	19		
		5	7		
	T3C0	9	12	I/O	Capture/compare Output-0 from Timer-3
	T3C1	11	14		Capture/compare Output-1 from Timer-3
Timers - Complementary Capture / Compare	T0C0N	1	3	O	Complementary compare/PWM Output-0 from Timer-0
		4	6		
	T0C1N	11	14		Complementary compare/PWM Output-1 from Timer-0
	T0C2N	12	15		Complementary compare/PWM Output-2 from Timer-0
	T1C0N	1	3	O	Complementary compare/PWM Output-0 from Timer-1
		5	7		
	T1C1N	8	10		Complementary compare/PWM Output-1 from Timer-1
		6	8		
	T1C2N	2	4		Complementary compare/PWM Output-2 from Timer-1
Timers – Fault input	T1F	4	6	I	Fault input for Timer-1
Timers -Prescaler Event	T0PE	9	12	O	Prescaler event output from Timer-0
UART	UART0TXD	12	15	O	UART0 TX data
		13	19		
		4	6		
		6	8		
		7	9		
	UART0RXD	3	5	I	UART0 RX data
		5	7		
		7	9		
	UART0CTS	8	10	I	UART0 clear-to-send input (active low)
	UART0RTS	1	3	O	UART0 request-to-send (active low)

3. Characteristics

3.1. Electrical Characteristics

3.1.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Over operating free-air temperature range (unless otherwise noted).

Table 8. Absolute Maximum Ratings

Parameter	MIN	MAX	Unit	Note
VDD, Supply voltage	-0.3	4.1	V	
Voltage on any digital pins	-0.3	VDD+0.3≤4.1	V	Including DIOs with analog capability
Voltage on ADC input	0	VDD	V	
T_{STG}, Storage temperature	-40	85	°C	

3.1.2. ESD Ratings

Table 9. ESD Ratings

Parameter	Description	Value	Unit	Note
Electrostatic discharge	Contact discharge	4000	V	As per EN 301-489
	Air discharge	8000	V	As per EN 301-489

3.1.3. Recommended Operating Conditions

Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.

Over operating free-air temperature range (unless otherwise noted).

Table 10. Recommended Operating Conditions

Parameter	MIN	TYP	MAX	Unit	Note
VDD, Supply voltage	1.71	3.3	3.8	V	
T_A, Operating Temperature	-40	25	85	°C	
Rising supply voltage slew rate	0		100	mV/µs	
Falling supply voltage slew rate	0		1	mV/µs	

3.1.4. Power Consumption

The measurement is made with the evaluation board for BDE-LE2340RGEC with T_A = 25 °C, VDD = 3.0 V, DCDC enabled, GLDO disabled, unless otherwise noted.

Table 11. Power Consumption – Power Modes

Power Mode	Test Condition	TYP	Unit
Core Current Consumption with DCDC			
Active	MCU running CoreMark from flash at 48 MHz	2.6	mA
	MCU running CoreMark from flash at 48 MHz	53	uA/MHz
Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	0.8	mA
	Supply Systems and RAM powered, flash disabled, DMA enabled	0.8	mA
	Supply Systems and RAM powered, flash enabled, DMA disabled	1.1	mA
	Supply Systems and RAM powered, flash enabled, DMA enabled	1.2	mA
Standby	RTC running, 36kB RAM retention, LFOSC, DCDC recharge current setting (ipeak = 1)	0.71	µA
	RTC running, 36kB RAM retention, LFXT, DCDC recharge current setting (ipeak = 1)	0.74	µA
Core Current consumption with GLDO			
Active	MCU running CoreMark from flash at 48 MHz	4.1	mA
Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	1.2	mA
	Supply Systems and RAM powered, flash disabled, DMA enabled	1.3	mA
	Supply Systems and RAM powered, flash enabled, DMA disabled	1.5	mA
	Supply Systems and RAM powered, flash enabled, DMA enabled	1.7	mA
Standby	RTC running, full RAM retention LFOSC, default GLDO recharge current setting	1.1	uA
	RTC running, full RAM retention LFXT default GLDO recharge current setting	1.15	uA
Reset, Shutdown Current Consumption			
Reset	Reset. nRESET pin asserted or VDD below power-on-reset threshold	165	nA
Shutdown	Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled	165	nA
Peripheral Current Consumption			
RF	Delta current, clock enabled, RF subsystem idle	40	uA
Timers	Delta current with clock enabled, module is idle, one LGPT timer	2.4	uA
I2C	Delta current with clock enabled, module is idle	10.6	uA
SPI	Delta current with clock enabled, module is idle	3.4	uA
UART	Delta current with clock enabled, module is idle	24.5	uA
CRYPTO (AES)	Delta current with clock enabled, module is idle	3.8	uA

Table 12. Power Consumption – Radio Modes

Power Mode	Test Condition	TYP	Unit
Radio receive current	2440 MHz, 1 Mbps, GFSK, system bus off (idle mode, DMA disabled, flash disabled)	5.3	mA
Radio receive current	2440 MHz, 1 Mbps, GFSK, DCDC OFF, system bus off	9	mA
Radio transmit	-8 dBm output power setting	4.5	mA

Power Mode	Test Condition	TYP	Unit
current	2440 MHz system bus off (idle mode, DMA disabled, flash disabled)		
	0 dBm output power setting 2440 MHz system bus off (idle mode, DMA disabled, flash disabled)	5.1	mA
	0 dBm output power setting 2440 MHz DCDC OFF, system bus off (idle mode, DMA disabled, flash disabled)	9.0	mA
	4 dBm output power setting 2440 MHz system bus off (idle mode, DMA disabled, flash disabled)	7.9	mA
	6 dBm output power setting 2440 MHz system bus off (idle mode, DMA disabled, flash disabled)	8.9	mA
	8 dBm output power setting 2440 MHz system bus off (idle mode, DMA disabled, flash disabled)	10.7	mA
	8 dBm output power setting 2440 MHz DCDC OFF, system bus off (idle mode, DMA disabled, flash disabled)	19	mA

3.1.5. Clock Characteristics

Table 13. 48-MHz Crystal Oscillator (HFXT) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			48		MHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-10		+10	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			7		pF

Table 14. 32.768-KHz Crystal Oscillator (LFXT) Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Crystal frequency			32.768		KHz
ESR, Equivalent series resistance					Ω
Frequency tolerance	T_A: 25°C	-20		+20	ppm
Frequency stability	T_A: -40°C ~ 85°C	-30		+30	ppm
C_L, Crystal load capacitance			12.5		pF

3.1.6. Reset Timing

Table 15. Reset Timing

Parameter	MIN	TYP	MAX	Unit
nRESET low duration	1			us

3.1.7. UART Characteristics

Table 16. UART Characteristics

Parameter	MIN	TYP	MAX	Unit
UART baud rate			3	MBaud

3.1.8. SPI Characteristics

Table 17. SPI Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
SPI clock frequency	Controller Mode and Peripheral Mode 2.7 < VDD < 3.8			12	MHz
	Controller Mode and Peripheral Mode VDD < 2.7			8	
SPI duty cycle		45	50	55	%

For timing characteristics or other details, please refer to CC2340R datasheet: CC2340R SimpleLink™ 32-bit Arm® Cortex®-M0+ Bluetooth® Low Energy wireless MCU.

3.1.9. I2C Characteristics

Table 18. I2C Characteristics

Parameter	MIN	TYP	MAX	Unit
I2C clock frequency	0		400	KHz

For timing characteristics or other details, please refer to CC2340R datasheet: CC2340R SimpleLink™ 32-bit Arm® Cortex®-M0+ Bluetooth® Low Energy wireless MCU.

3.1.10. GPIO DC Characteristics

Table 19. GPIO DC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
TA = 25 °C, VDD = 1.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	39	66	109	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD	10	21	40	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	0.91	1.11	1.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	0.59	0.75	0.91	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.26	0.35	0.44	V

Parameter	Test Condition	MIN	TYP	MAX	Unit
TA = 25 °C, VDD = 3.0 V					
GPIO VOH at 10 mA load	high-drive GPIOs only, max drive setting	2.47			V
GPIO VOL at 10 mA load	high-drive GPIOs only, max drive setting			0.25	V
GPIO VOH at 2 mA load	standard drive GPIOs	2.52			V
GPIO VOL at 2 mA load	standard drive GPIOs			0.20	V
TA = 25 °C, VDD = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	170	262	393	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD	60	110	172	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	1.76	1.98	2.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	1.26	1.52	1.79	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.40	0.47	0.54	V
TA = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a High	0.8*VDD			V
VIL	Highest GPIO input voltage reliably interpreted as a Low			0.2*VDD	V

3.1.11. ADC Characteristics

Table 20. ADC Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Resolution	All ADC analog input pins Ax		12		bit
sampling rate			1.2		Msps
Input voltage range	All ADC analog input pins Ax	0		VDD	V
Positive external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF+)	1.4		VDD	V
Negative external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF-)			0	V
Positive ADC reference voltage	ADC reference sourced from VDD		VDD		V
Internal ADC Reference Voltage	ADCREF_EN = 1, ADCREF_VSEL = 0, VDD = 1.71V - VDDmax		1.4		V
	ADCREF_EN = 1, ADCREF_VSEL = 1, VDD = 2.7V - VDDmax		2.5		V
Signal-to-noise and distortion ratio	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		69.18		dB
	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		64.37		dB

Parameter	Test Condition	MIN	TYP	MAX	Unit
	VDD reference, RES = 0x0 (12-bit)		69.18		dB

For timing characteristics or other details, please refer to CC2340R datasheet: CC2340R SimpleLink™ 32-bit Arm® Cortex®-M0+ Bluetooth® Low Energy wireless MCU.

3.1.12. Comparator Characteristics

Table 21. Comparator Characteristics

Parameter	Test Condition	MIN	TYP	MAX	Unit
Input voltage range		0		VDD	V
Clock frequency			32		KHz
Voltage Divider Accuracy	Input voltage range is between VDD/4 and VDD		98%		
Offset	Measured at VDD / 2 (Errors seen when using two external inputs)		± 27.3		mV
Decision time	Step from –50 mV to 50 mV		1	3	Clock Cycle
Comparator enable time	COMP_LP disable → enable, VIN+, VIN- from pins, Overdrive ≥ 20 mV		70		µs
Current consumption	Including using VDD/2 as internal reference at VIN- comparator terminal		370		nA

3.2. RF Characteristics

The measurement is made with the evaluation module (EM board) for BDE-LE2340RGEC with T_A = 25 °C, VDD = 3.3 V, DCDC enabled, GLDO disabled, unless otherwise noted.

3.2.1. Receive (RX) Characteristics - Bluetooth Low Energy

Table 22. Receive (RX) Characteristics– Bluetooth Low Energy

Parameter	Test Condition	TYP	Unit
125 kbps (LE Coded)			
Receiver sensitivity	BER = 10^{-3}	-102	dBm
Receiver situation	BER = 10^{-3}	5	dBm
Co-channel rejection (1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}	-6	dB
Selectivity, ±1 MHz (1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}	9 / 5 (2)	dB
Selectivity, ±2 MHz	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	44 / 31	dB
Selectivity, ±3 MHz	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	47 / 42	dB
Selectivity, ±4 MHz	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	49 / 45	dB
Selectivity, ±6 MHz	Wanted signal at –79 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}	52 / 48	
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ±7 MHz, BER = 10^{-3}	54 / 49	

Parameter	Test Condition	TYP	Unit
Selectivity, image frequency	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}	31	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	5 / 42	dB
500 kbps (LE Coded)			
Receiver sensitivity	BER = 10^{-3}	-98.5	dBm
Receiver situation	BER = 10^{-3}	5	dBm
Co-channel rejection (1)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}	-4.5	dB
Selectivity, ±1 MHz (1)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}	9 / 5	dB
Selectivity, ±2 MHz	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	42 / 31	dB
Selectivity, ±3 MHz	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	45 / 41	dB
Selectivity, ±4 MHz	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	46 / 42	dB
Selectivity, ±6 MHz	Wanted signal at –72 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}	50 / 45	dB
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ±7 MHz, BER = 10^{-3}	51 / 46	dB
Selectivity, image frequency	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}	31	dB
Selectivity, image frequency ±1 MHz (1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	5 / 41	dB
1 Mbps (LE 1M)			
Receiver sensitivity	BER = 10^{-3}	-94.5	dBm
Receiver situation	BER = 10^{-3}	5	dBm
Co-channel rejection	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}	-6	dB
Selectivity, ±1 MHz	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}	7 / 5	dB
Selectivity, ±2 MHz	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	39 / 28	dB
Selectivity, ±3 MHz	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	38 / 38	dB
Selectivity, ±4 MHz	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	47 / 35	dB
Selectivity, ±5 MHz or more	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}	40	dB
Selectivity, image frequency	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}	28	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	5 / 38	dB
Out-of-band blocking	30 MHz to 2000 MHz	-10	dBm
Out-of-band blocking	2003 MHz to 2399 MHz	-10	dBm
Out-of-band blocking	2484 MHz to 2997 MHz	-10	dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)	-2	dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level	-37	dBm

Parameter	Test Condition	TYP	Unit
Spurious emissions, 30 to 1000 MHz	Measurement in a 50-Ω single-ended load	< –59	dBm
Spurious emissions, 1 to 12.75 GHz	Measurement in a 50-Ω single-ended load	< –47	dBm
RSSI dynamic range		70	dB
RSSI accuracy		±4	dB
RSSI resolution		1	dB
2 Mbps (LE 2M)			
Receiver sensitivity	BER = 10^{-3}	-90.5	dBm
Receiver situation	BER = 10^{-3}	2	dBm
Co-channel rejection	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}	-8	dB
Selectivity, ±2 MHz	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}	9 / 5	dB
Selectivity, ±4 MHz	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}	40 / 32	dB
Selectivity, ±6 MHz	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}	46 / 40	dB
Selectivity, image frequency	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}	5	dB
Selectivity, image frequency ±1 MHz	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}	-8 / 32	dB
Out-of-band blocking	30 MHz to 2000 MHz	-10	dBm
Out-of-band blocking	2003 MHz to 2399 MHz	-10	dBm
Out-of-band blocking	2484 MHz to 2997 MHz	-12	dBm
Out-of-band blocking	3000 MHz to 12.75 GHz (excluding VCO frequency)	-10	dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level	-38	dBm

(1) Numbers given as I/C dB;
(2) X / Y, where X is +N MHz and Y is –N MHz.

3.2.2. Transmit (TX) Characteristics - Bluetooth Low Energy

The measurement is made with the evaluation board for BDE-LE2340RGEC with TA = 25 °C, VDD = 3.0 V, f_{RF} = 2440 MHz, DCDC enabled, GLDO disabled, unless otherwise noted.

Table 23. Transmit (TX) Characteristics- Bluetooth Low Energy

Parameter	Test Condition	TYP	Unit
Max output power	Conducted output from ANT pin of the module, 8dBm setting	7.1	dBm
	Conducted output from ANT pin of the module, 7dBm setting	6.3	dBm
	Conducted output from ANT pin of the module, 6dBm setting	5.4	dBm
	Conducted output from ANT pin of the module, 5dBm setting	4.3	dBm

Parameter	Test Condition	TYP	Unit
	Conducted output from ANT pin of the module, 4dBm setting	3.1	dBm
	Conducted output from ANT pin of the module, 3dBm setting	2.1	dBm
	Conducted output from ANT pin of the module, 2dBm setting	1.0	dBm
	Conducted output from ANT pin of the module, 1dBm setting	0.4	dBm
	Conducted output from ANT pin of the module, 0dBm setting	-0.6	dBm
Output power programmable range	Conducted output from U.FL connector of the module	28	dB

3.2.3. Receive (RX) Characteristics – Proprietary Radio Mode

Table 24. Receive (RX) Characteristics –Proprietary Radio Mode

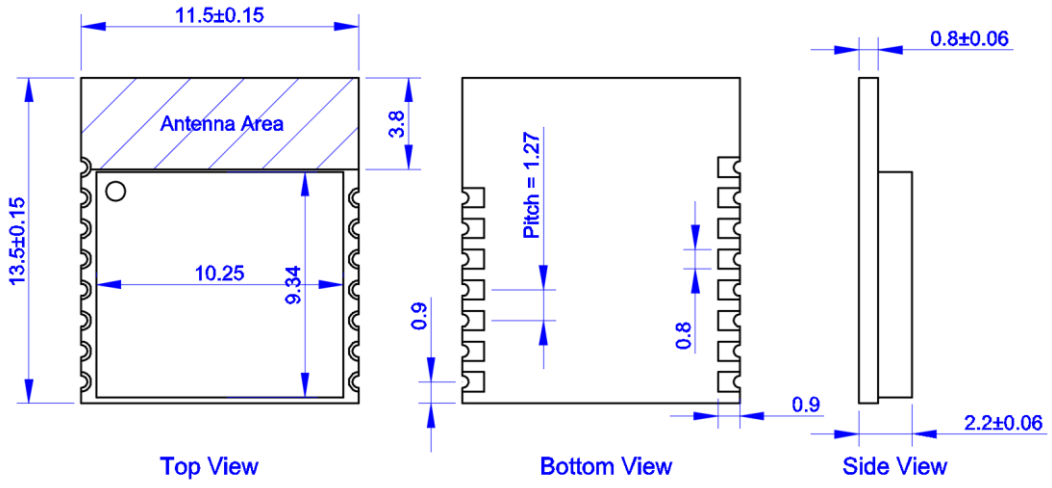
Parameter	Test Condition	TYP	Unit
Receive sensitivity	2 Mbps GFSK (HID), 320 kHz deviation, PER30.8, payload 37 bytes	-88	dBm

4. Mechanical Specifications

The following section includes mechanical and footprint drawings of the modules.

4.1. Module Dimensions

The module dimensions are presented in the following figure:

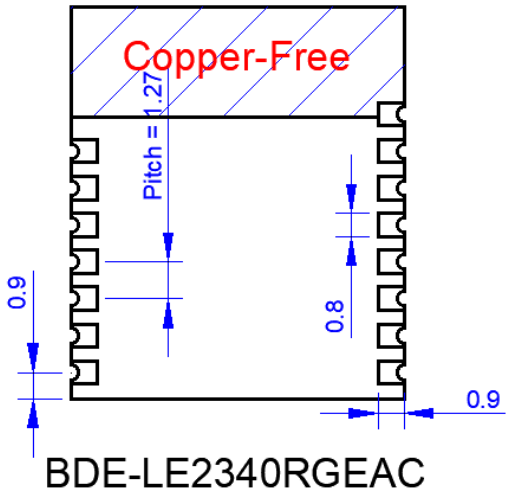


Note: All dimensions are in millimeter

Figure 4. Module Dimensions of BDE-LE2340RGEAC Variants

4.2. PCB Footprint

The recommended footprint for the PCB is presented in the following figure:



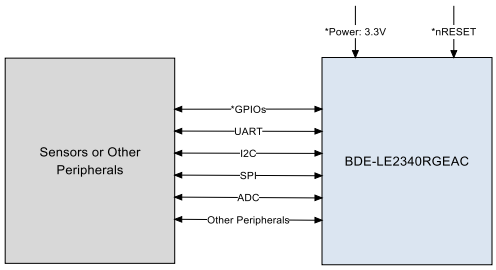
(1) All dimensions are in millimeter;
(2) Solder mask should be the same or 5% larger than the dimension of the pad;
(3) Solder paste must be the same as the pin for all peripheral pads. For thermal pads, make the solder paste 20% smaller than the pad;
(4) Copper-free means no copper in this area in all layers, including traces, ground or components etc;
(5) Customers can modify the land pattern dimensions based on their manufacturing experience.

Figure 5. Module Dimensions of BDE-LE2340RGEAC Variants

5. Integration Guidelines

5.1. SoC Mode

Below block diagram is applicable when the module is used as a SoC running the application and the protocol stack in the system CUP inside the module.



(1) The module has already been implemented with required decoupling capacitors, therefore, external decoupling capacitors are not needed. However, proper decoupling capacitors can also be added to increase module power stability depending on customer's application;

(2) A ferrite bead is recommended to add to the power pin of the module to increase EMI performance if the module is used with other digital or analog or switching circuitry in the system. In addition, adding the bead can also help with the power to meet the slew rate requirement. The ferrite bead utilized in our evaluation board is BLM18HE152SN1D from Murata for reference;

(3) The module has the internal reset circuit on board, e.g. a 100K ohm pull-up resistors and a 0.1uF decouple capacitor. Therefore, external reset circuit is not needed for the same purpose;

Figure 6. High-Level System Block Diagram

5.2. WNP Mode

The module can also function as the WNP (Wireless Network Processor), in this case, an external MCU will be needed to run the application and the protocol stack, and the interface between the external MCU and the module can be UART/SPI.

5.3. UART Pass-Through Mode

The module can come with a pre-programmed BDE-SPP firmware where the module can be used a UART pass-through, the host MCU only needs to send AT comments to the module to configure the module and transfer data. A couple of IOs are also used. For more detail information, please refer to BDE-SPP user guide.

5.4. Module Placement

The placement of the module in the base board is critical in your design. Improper placement can lead to poor antenna performance. BDE recommend following below recommended placement in your design.

Any form of proximity to the metal or other material will change/degrade the antenna performance. Keep the antenna area as far as possible to the metal material in any direction.

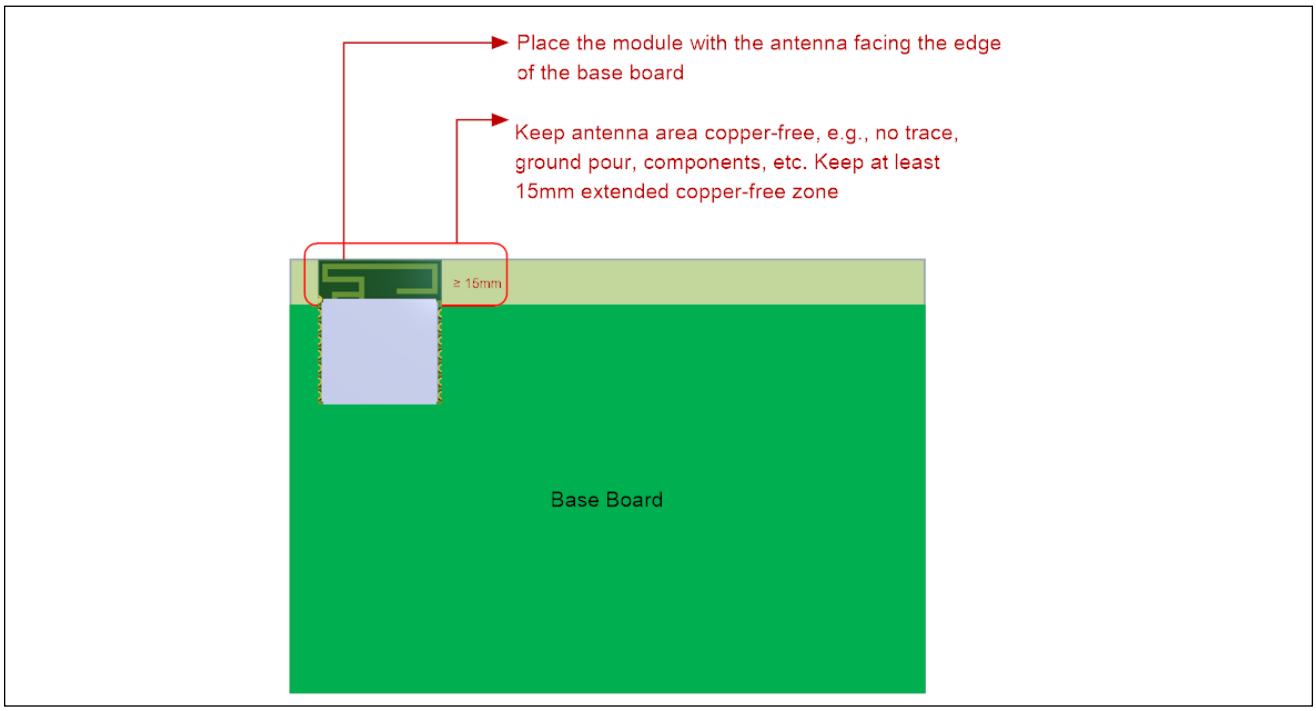


Figure 7. Module Placement Recommendations

5.5. Other Design Considerations

Table 25. Other Design Considerations

Thermal	
1	The proximity of ground vias must be close to each ground pad of the module.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
RF Trace and Antenna Routing	
7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45° with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.
10	RF traces must have constant impedance (50-ohm Coplanar or microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product.

	The proximity of the antenna to the enclosure and the enclosure material must also be considered.
14	BDE recommends using double-shielded coaxial RF cable to connect with the U.FL connector with antenna if the U.FL variants are selected.
15	Do not place or run the RF cable right above or below the module.
16	If there are some other radios besides this module in the system, try to place them apart as far as possible. And ensure there is at least 25 dB isolation between the antenna port of every radio.
Supply and Interface	
17	The power trace for VDD must be at least 20-mil wide.
18	Make VDD traces as wide as possible to ensure reduced inductance and trace resistance.
19	If possible, shield VDD traces with ground above, below, and beside the traces.

5.6. Evaluation Kit

BDE provides an evaluation board for evaluating the modules. For more information on the EVK, please visit the product page of the module on bdecomm.com.

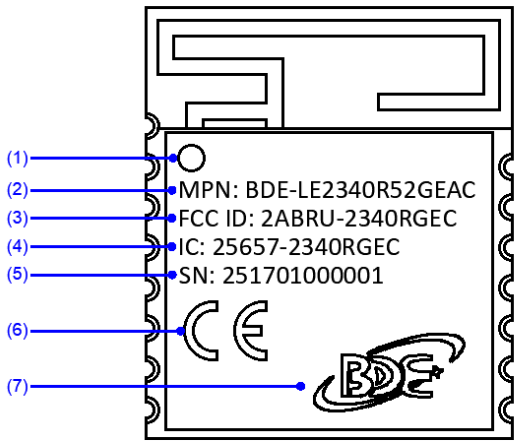
6. Handling Instructions

The module is the surface mount module with LGA footprint. It is designed to conform to the major manufacturing guidelines, including the commercial, industrial manufacturing process.

In this section, we will cover the basic shipping information, including the module markings, packaging and labeling. And also the instructions on how to handle the module in terms of storage, assembly and so on.

6.1. Module Marking

Below figure shows the metal shield marking for the BDE-LE2340RGEC module series.



(1) Pin 1 index;
(2) Orderable Manufacturer Part Number. Refer to Table 1;
(3) FCC ID;
(4) IC ID;
(5) Serial number for traceability;
(6) CE mark;
(7) BDE logo.

Figure 8. Module Marking

6.2. Assembly Instruction

6.2.1. Moisture Sensitive Level

The MSL (Moisture Sensitive Level) of the module is MSL-3. Handling guidelines are listed as below:

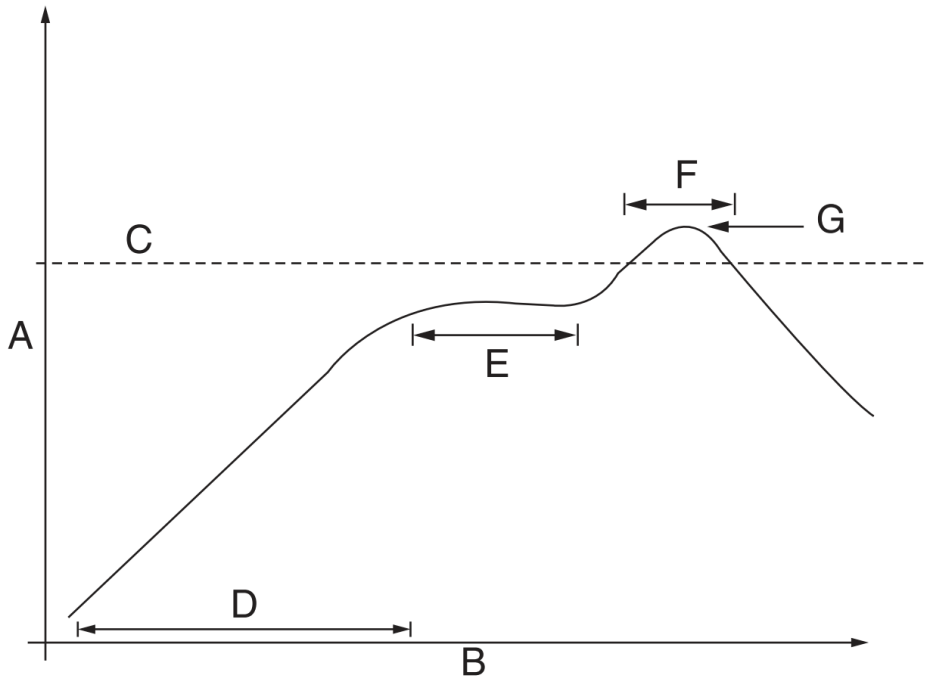
(1) The floor life for MSL-3 device is 168 hours in ambient environment 30°C/60%RH. Before assembly, make sure to

check if the modules are packaged with desiccate and humidity indicator card;

(2) After the bag is opened, make sure to mount the modules within 168 hours at factory conditions (< 30°C/60% RH) or stored at <10% RH. Repackage is needed with new desiccate and humidity indicator card if the modules are not mounted before exceeding floor life;

(3) If the card reads >10%, or the modules have been exposed for over 168 hours, the modules need to be baked before mounted. Recommended baking condition is 125℃ for 8 hours.

6.2.2. Reflow Profile



(1) A – Temperature
(2) B – Time
(3) C – Alloy liquidus temperature
(4) D – Preheat slope = temperature ramp rate
(5) E – Preheat dwell = soak time
(6) F – Time above liquidus
(7) G – Peak temperature = maximum assembly temperature

Figure 9. Thermal Profile Schematic

Table 26. Reflow Profile Parameters [(1) (3)]

Item	Temperature Range	Ramp Rate / Time
D, preheat zone	30°C ~ 175°C	2°C ~ 4°C per second
E, soak zone	150°C ~ 200°C	60 ~ 120 seconds
C, Alloy liquidus temperature	217°C ~ 220°C	-
F, reflow zone	230°C ~ 245°C	60 ~ 90 seconds
G, target maximum reflow temperature	250°C	-

Item	Temperature Range	Ramp Rate / Time
Absolute peak temperature (2)	260°C	-

(1) This is for Pb-free (SAC 305) paste. Different pastes require different profiles for optimum performance, so it is important to consult the paste manufacturer before developing the solder profile;
(2) Exceed the absolute peak temperature for certain period, e.g. 20s might damage the device or affect the reliability;
(3) It is recommended that the modules do not go through the reflow process more than one time.

6.2.3. Other Consideration

(1) Ultrasonic cleaning process is discouraged for the modules as the process might damage the module permanently, especially for the crystal oscillator in the module;
(2) Conformal coating is not allowed to this module. It will impact the reliability of the module once the coating flooded into the shield. Avoid the module while applying the conformal coating to the host board.

7. Certification

7.1. Bluetooth Qualification

7.1.1. Bluetooth Qualification Information

The module series is qualified and listed on the Bluetooth SIG with the DN (Design Number) of Q332693, referencing a Controller and Host Subsystem combination. The detail information can be found in below table.

Table 27. Bluetooth Qualification Information

Design Number	Included Design	
Q332693	RFHPY	196592
	Host Stack	Q312647

7.1.2. Bluetooth Qualification Process

Below Bluetooth qualification process is provided for customers when they are listing their end product referencing BDE module.

(1) Go to https://launchstudio.bluetooth.com/ and log in;
(2) Select **Start the Bluetooth Qualification Process with No Required Testing**;
(3) Project Basics:
  (a) Enter your project name, it can be the product name or the product series name;
  (b) Enter DN that the product reference, in this case the DN is Q332693.
(4) Product Declaration:
  (a) Select the listing date. You can select a date that you want your product listed and go public, although the qualification will complete immediately after your submission.

(b) Add every product that integrated with this module. You can add a series of individual product models that use the same design/module without any modification.

(5) Declaration ID:

(a) Select a DID. If you don't have one, you need to purchase a DID for your product by clicking Pay Declaration Fee.

(6) Review and Submit:

(a) Review all information that you have entered and make sure no mistakes;

(b) Tick all check boxes if you confirmed above information and add your name to the signature page;

(c) Click **Signature Confirmed – Complete Project & Submit Product(s) for Qualification**.

(7) The qualification will be done immediately and your product will be listed to the Bluetooth SIG website as per your required listed date in step (4).

For more information about listing your product to Bluetooth SIG, please visit below webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

7.2. Regulatory Compliance

The module is certified for FCC, IC/ISED and ETSI/CE as listed in below table. More regions can be cover by request.

Table 28. Certification Information

Regulatory Body / Region	Standard	ID	MPN
FCC (USA)	FCC CFR 47 PART 15 C (15.247)	2ABRU-2340RGEC	BDE-LE2340R52GEAC BDE-LE2340R21GEAC
IC/ISED (Canada)	RSS-247 Issue 3 RSS-Gen Issue 5	25657-2340RGEC	
ETSI/CE (Europe)	ETSI EN 301 489-1 V2.2.3 (2019-11) ETSI EN 301 489-17 V3.2.4 (2020-09) ETSI EN 300 328 V2.2.2 (2019-07) EN 62311: 2020 EN 50665: 2017 EN62368-1: 2014+A11: 2017	NA	

7.2.1. Certified Antennas

The BDE-LE2340RGEC module series has been tested and certified with one antenna, where BDE-LE2340RGEAC variants utilize an integrated PCB antenna.

The characteristic of the antenna is listed in below table.

Table 29. Certified Antenna List

Antenna Type	Manufacturer	MPN	Peak Gain (dBi)	Note
PCB trace antenna	BDE	BDE-ANT-LE2340RGEAC	-0.86	Internal

Customers are encouraged to use the certified antennas in the case of external antenna options to reduce certification testing effort and risk of failing. If customer want to choose another antenna that fits their product, there are some scenarios that need to be considered.

If the external antenna is of the same antenna type and of equal or less gain compared to the ones listed in above table, and with similar in-band and out-of-band characteristic, then the antenna can be used with the module in USA and Canada where modular approval is applicable, as long as the spot-check testing of the new antenna with host is performed to verified that it will not change the performance. However, in countries such as EU countries applying the ETSI standards where the modular approval is not applicable, the radiated emissions are always tested with the end product with any antennas.

If the external antenna is of a different type or with non-similar in-band and out-of-band characteristic, but still has equal gain or less gain compared to the above listed antennas. The new antenna can be added to the existing modular grant/certificate by filing a permissive change, C2PC (Class II Permissive Change) in case of FCC and ISED. The radiated emission testing is needed, but re-certification is not required.

In the case of the external antenna with higher gain than the peak gain listed in above table are very likely to require a full new end product certification. However, we recommended that you consult with your certification house to understand the correct approaches for your product case by case.

7.2.2. FCC Compliance

7.2.2.1. FCC Statement

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

7.2.2.2. FCC Caution

Any changes or modifications to this unit not expressly approved by BDE for compliance could void the user's authority to operate the equipment. The integrator will be responsible to satisfy SAR/RF Exposure requirements, when the module integrated into the host device.

7.2.2.3. Integration Instructions

List of applicable FCC rules

FCC Part 15.247

Specific operational use conditions

This transmitter/module and its antenna(s) must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer's instruction manual.

Limited module procedures

Not applicable

Trace antenna designs

Not applicable

RF exposure considerations

This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This compliance to FCC radiation exposure limits for an uncontrolled environment, and minimum of 20cm separation between antenna and body. The host product manufacturer would provide the above information to end users in their end-product manuals.

Antennas

Refer to Table 29.

Label and compliance information

The end product must carry a physical label or shall use e-labeling followed KDB784748D01 and KDB784748 stating "Contains Transmitter Module FCC ID: 2ABRU-2340RGEC"

Information on test modes and additional testing requirements

Contact BDE for more information

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.

(OEM) Integrator has to assure compliance of the entire end-product that includes the BDE-LE2340RGEC module. For 15 B (§15.107 and if applicable §15.109) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally the integrator has to apply the appropriate equipment

authorization (e.g. Verification) for the new host device per definition in §15.101. Integrator is reminded to assure that these installation instructions will not be made available to the end-user of the final host device.

7.2.3. IC/ISED Compliance

7.2.3.1. IC Statement

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licencecontenudans le présentappareilestconforme aux CNR d'Innovation, Sciences et Développementéconomique Canada applicables aux appareils radio exempts de licence. L'exploitationestautorisée aux deux conditions suivantes :

(1) L' appareil ne doit pas produire de brouillage;

(2) L' appareildoit accepter tout brouillageradioélectriquesubi, mêmesi le brouillageest susceptible d' encompromettre le fonctionnement.

7.2.3.2. IC Caution

Any changes or modifications to this unit not expressly approved by BDE for compliance could void the user's authority to operate the equipment. The integrator will be responsible to satisfy SAR/RF Exposure requirements, when the module integrated into the host device.

7.2.3.3. Integration Instructions

Label and compliance information

The final host device, into which this RF module is integrated has to be labeled with an auxiliary label stating the IC of the RF module, such as" Contains transmitter module IC: 25657-2340RGEC".

Informations sur l'étiquette et la conformité

Le périphériquehôte final, danslequelce module RF estintégré "doitêtreétiqueté avec uneétiquetteauxiliaireindiquant le CI du module RF, tel que" Contient le module émetteur IC: 25657-2340RGEC".

Radio Frequency Exposure Statement for IC

The device has been evaluated to meet general RF exposure requirements. The device can be used in mobile exposure conditions. The min separation distance is 20cm.

Déclaration d'exposition aux radiofréquences pour IC

L'appareil a été évalué pour répondre aux exigences générales en matière d'exposition aux RF. L'appareil peut être utilisé dans des conditions d'exposition mobiles. La distance de séparation minimale est de 20 cm.

This radio transmitter [IC: 25657-2340RGEC] has been approved by Innovation, Science and Economic Development

Canada to operate with the antenna types listed in Table 29, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Cet émetteur radio [IC: 25657-2340RGEC] a été approuvé par Innovation, Sciences et Développement économique Canada
pour fonctionner avec les types d'antenne énumérés ci-dessous, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste qui ont un gain supérieur au gain maximum indiqué pour tout type répertorié sont strictement interdits pour une utilisation avec cet appareil.

7.2.4. ETSI/CE Compliance

The BDE-LE2340RGEC module is certified with required EU radio and EMC directives. See Table 28 for detailed standards the module complies with, or refer to UK Declaration of Conformity.

8. Ordering Information

Table 30. Ordering Information

Part Number	Description	Size (mm)	Package	MPQ
BDE-LE2340R52GEAC	BDE Bluetooth 5.4 Low Energy Module Based on CC2340R52N0RGER, with PCB Antenna, -40℃ to +85℃	11.5 x 13.5 x 2.2	Tape & Reel	1.5K
BDE-LE2340R21GEAC	BDE Bluetooth 5.4 Low Energy Module Based on CC2340R21N0RGER, with PCB Antenna, -40℃ to +85℃	11.5 x 13.5 x 2.2	Tape & Reel	1.5K

9. Revision History

Table 31. Revision History

Revision	Date	Description
E1	13-Jun-2025	Preliminary, draft

Important Notice and Disclaimer

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