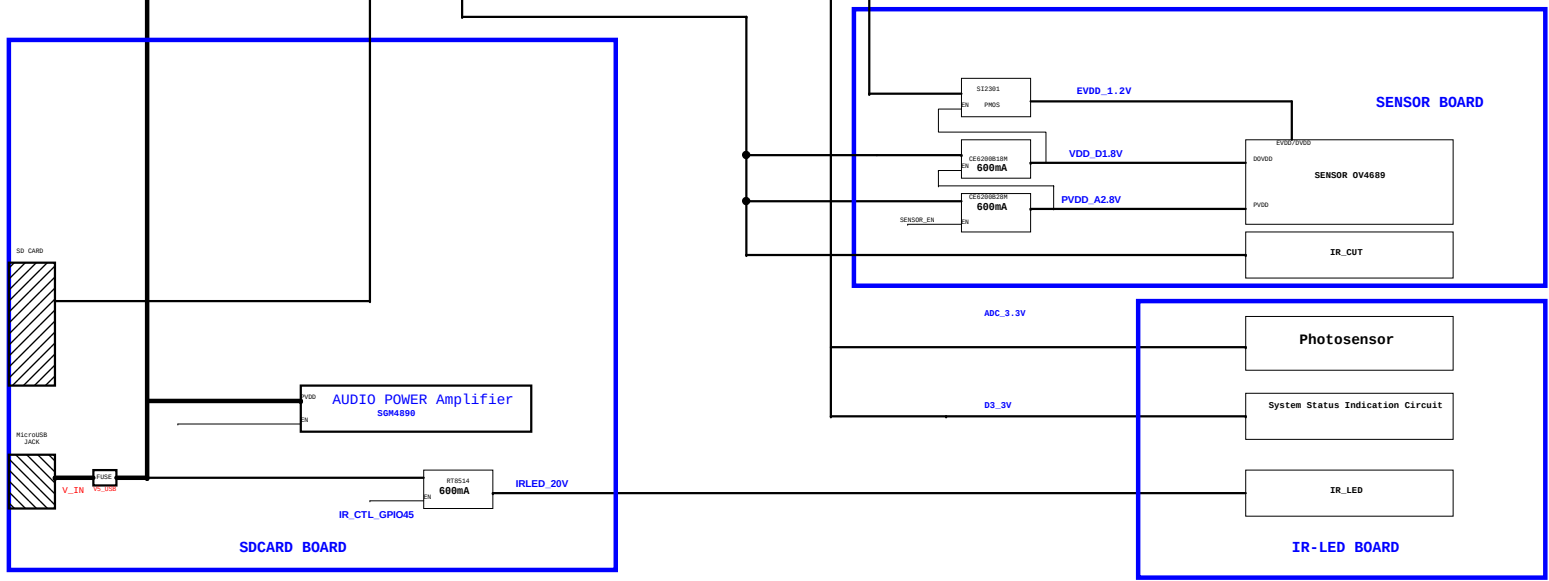
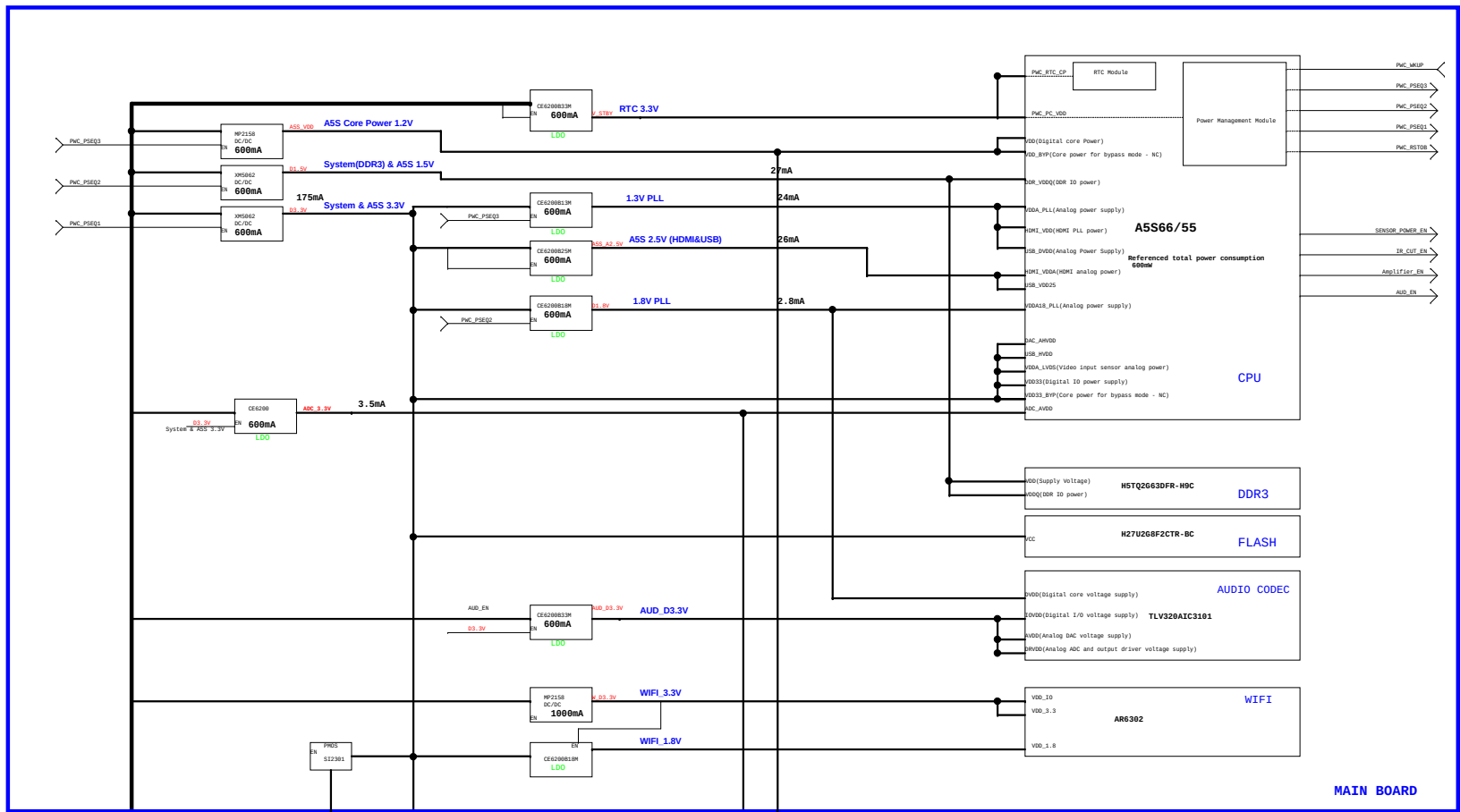






A5S Power-On-Config (VD0_OUT0~15)

VD0_OUT0

Boot Media Select

0: NAND flash

1: Reserved

VD0_OUT[3:1]

Clock: iDSP / vDSP / DRAM

000: 126 / 108 / 300 MHz

001: 120 / 96 / 300 MHz

010: 108 / 108 / 240 MHz

011: 96 / 96 / 192 MHz

100: 117 / 108 / 300 MHz

101: 117 / 96 / 300 MHz

110: 117 / 108 / 240 MHz

111: 96 / 96 / 192 MHz

VD0_OUT4

PLL_UNLOCK_TRIG_RESET

0: disable generating GRST when core PLL out of lock (default)

1: enable generating GRST when core PLL out of lock

VD0_OUT5

NAND Flash Page Size

0: 512 Bytes

1: 2K Bytes

VD0_OUT6

NAND Read Confirm

0: No "Read Confirm" needed

1: Requires "Read Confirm"

VD0_OUT7

Select ENET

0: disable

1: enable

VD0_OUT8

Boot Bypass

0: disable (no boot bypass)

1: enable

VD0_OUT9

Flash Fast Boot Mode

0: disable

1: enable

VD0_OUT10

IO Flash BOOT

0: USB

1: Flash

VD0_OUT11

Reserved

Set to 0

VD0_OUT12

EMA Select

Set to 0

VD0_OUT13

ARM Sync Lock Mode

0: disable

1: enable

VD0_OUT14

ARM Mode Change Issue Reset

0: GRST_L not issued when switching between ARM sync/async modes

1: GRST_L issued when switching between ARM sync/async modes

VD0_OUT15

RMII Select

Set to 0

A5S Power-On-Config Setting

A5S Power-On-Config (VD1_OUT0~15)

VD1_OUT0

SPI Boot

0: USB / Flash

1: SPI

VD1_OUT1

HIF Enable

0: disable

1: enable host interface

VD0_OUT2

Reserved

Set to 0

VD1_OUT3

HIF Type

0: Intel

1: Motorola

VD1_OUT4

RDY Polarity

0: HIF_RDY active low

1: HIF_RDY active high

VD1_OUT5

HIF Secure Mode

0: normal

1: secure mode

VD1_OUT6

Reserved

Set to 0

VD1_OUT7

USB Clock Source Select

0: choose internal clock for USBPHY

1: choose external clock for USBPHY

VD1_OUT[9:8]

Reserved

Set to 0

VD1_OUT[10]

REF_CLK for USB

Set to 1

VD1_OUT[11]

Reserved

Set to 0

VD1_OUT[12]

Reserved

Set to 0

VD1_OUT[14:13]

SYS_CONFIG

00: use power-on-config set on external pins

01: select pre-set option 1

10: select pre-set option 2

11: illegal

VD1_OUT[15]

Config Source Select

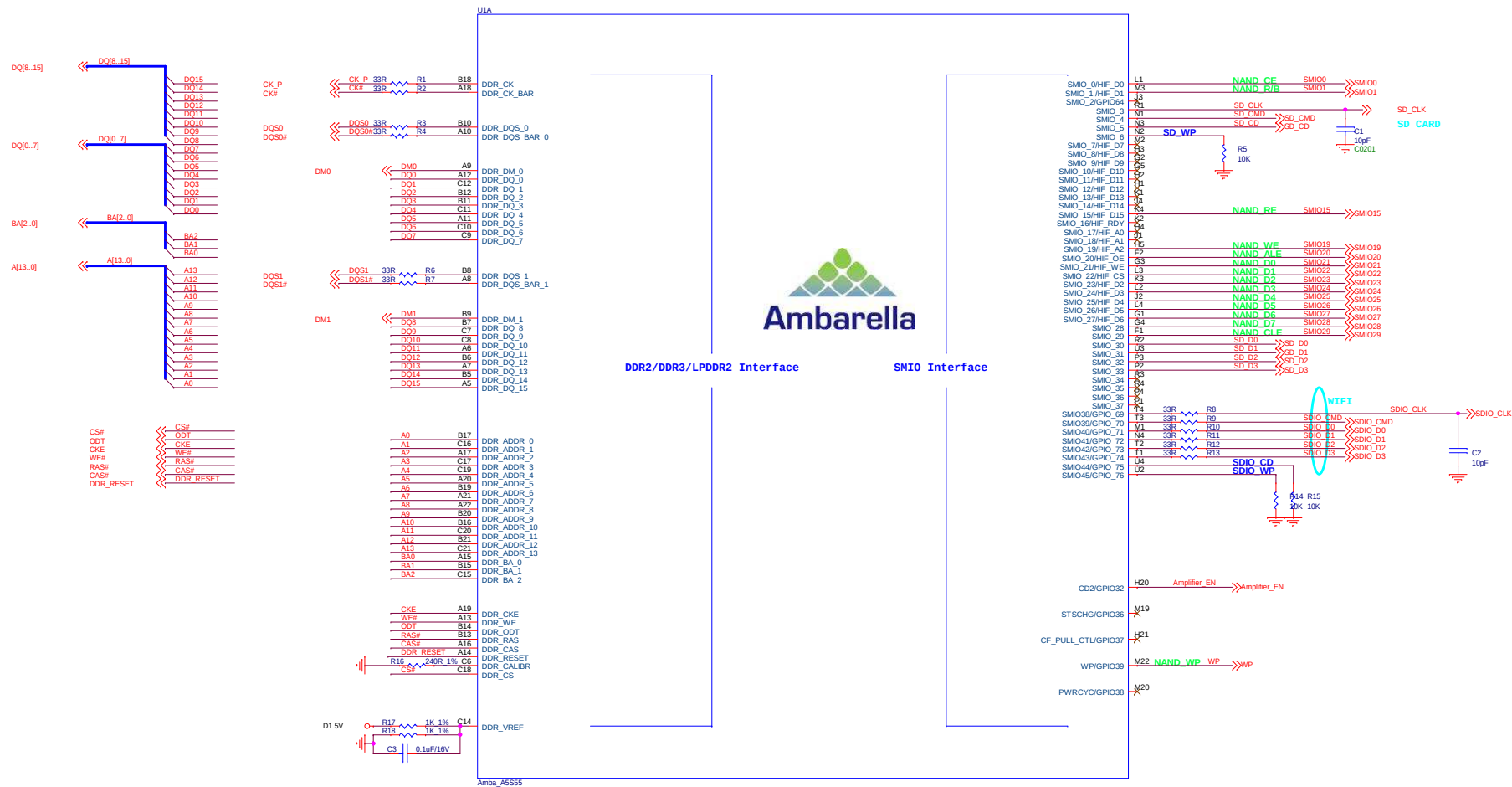
0: depends on that configured by VD1_OUT[14:13]

1: on-chip EEPROM (Efuse)

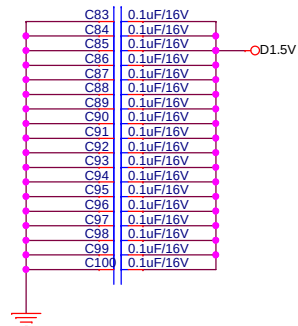
Note:

all GPIO pins(89 Pins) are in Hi-Z state during reset assertion and are initialized to be inputs.

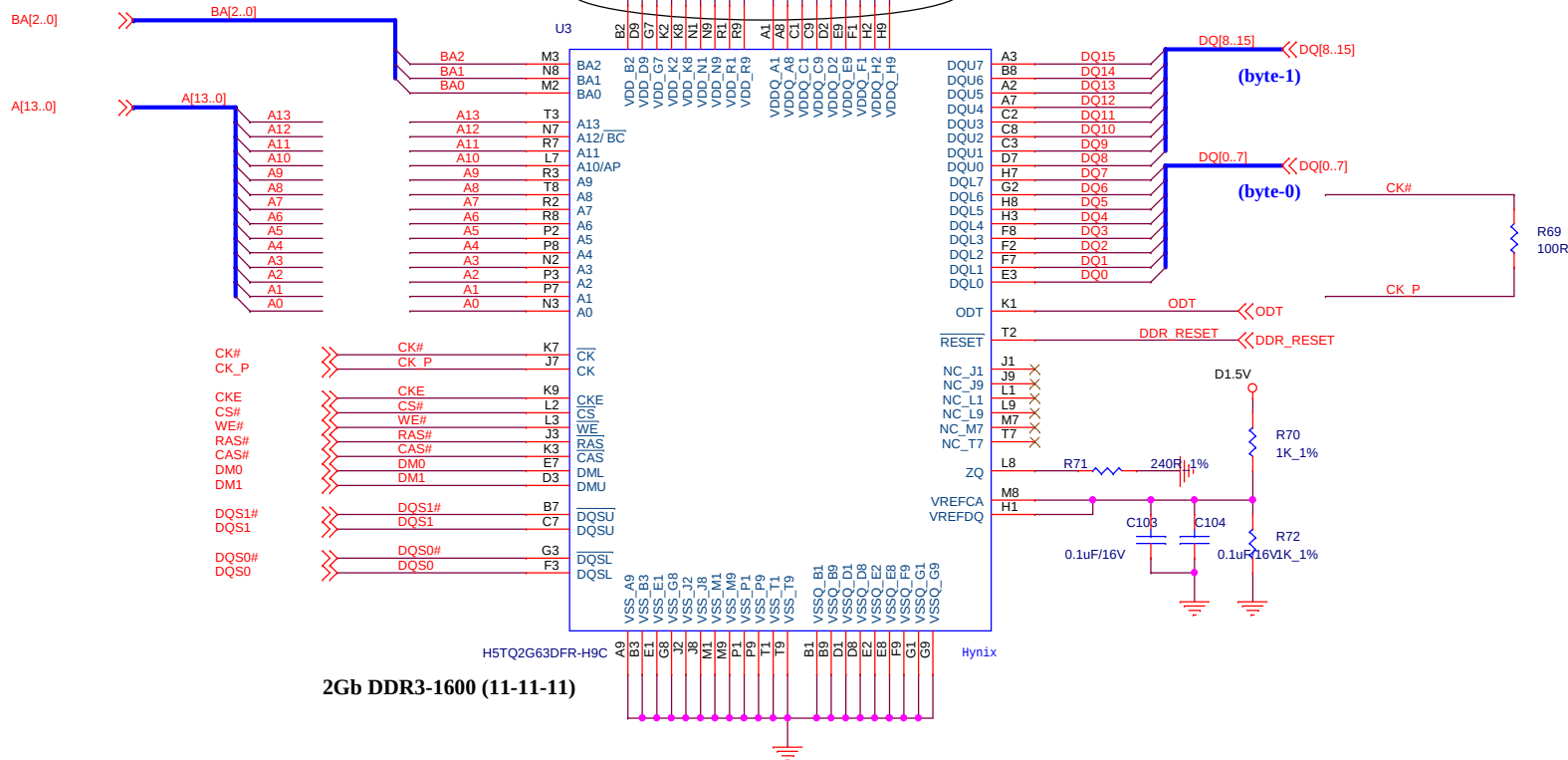
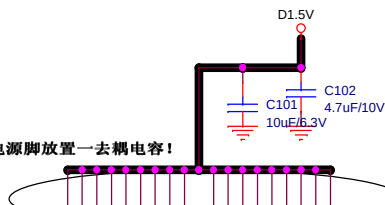
System GPIO Table



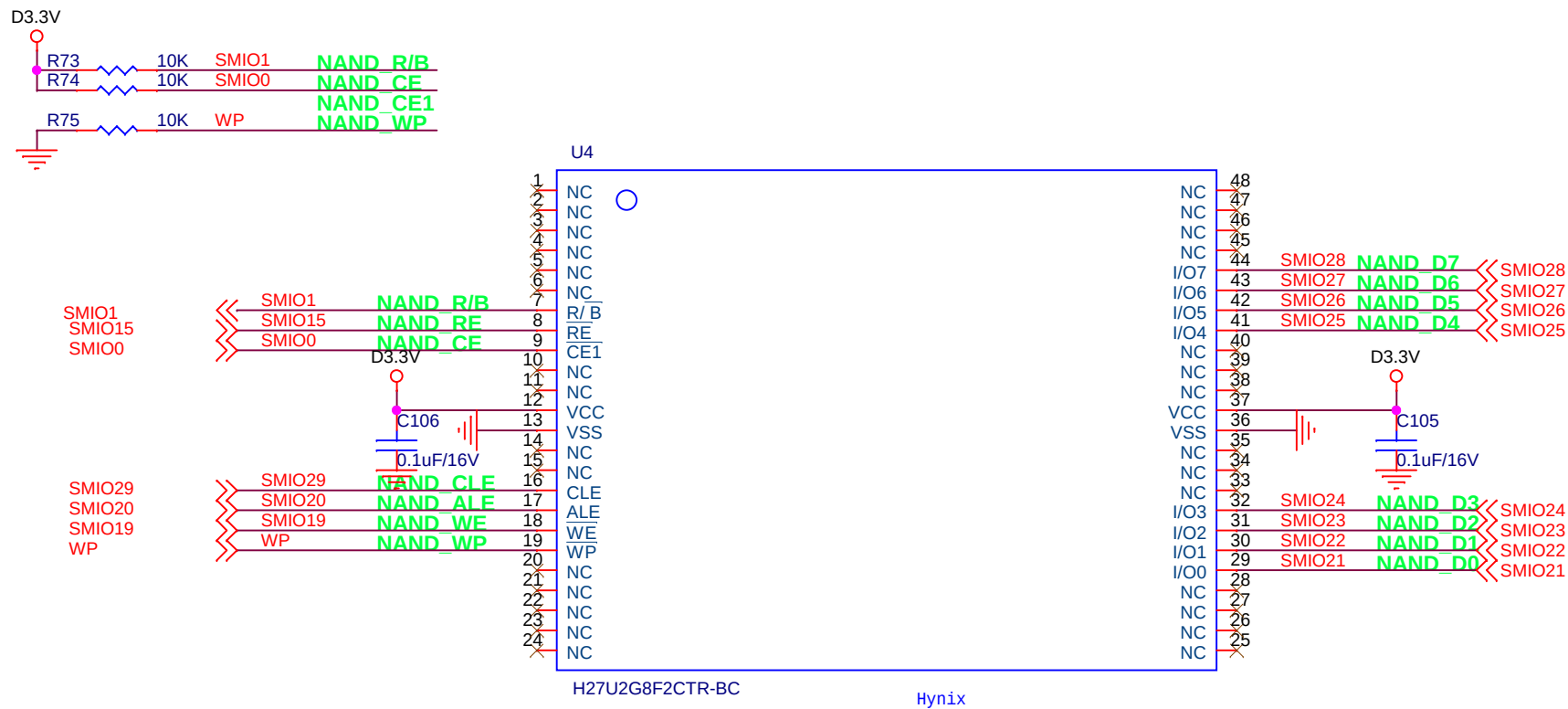
DDR3 Decoupling Capacitors

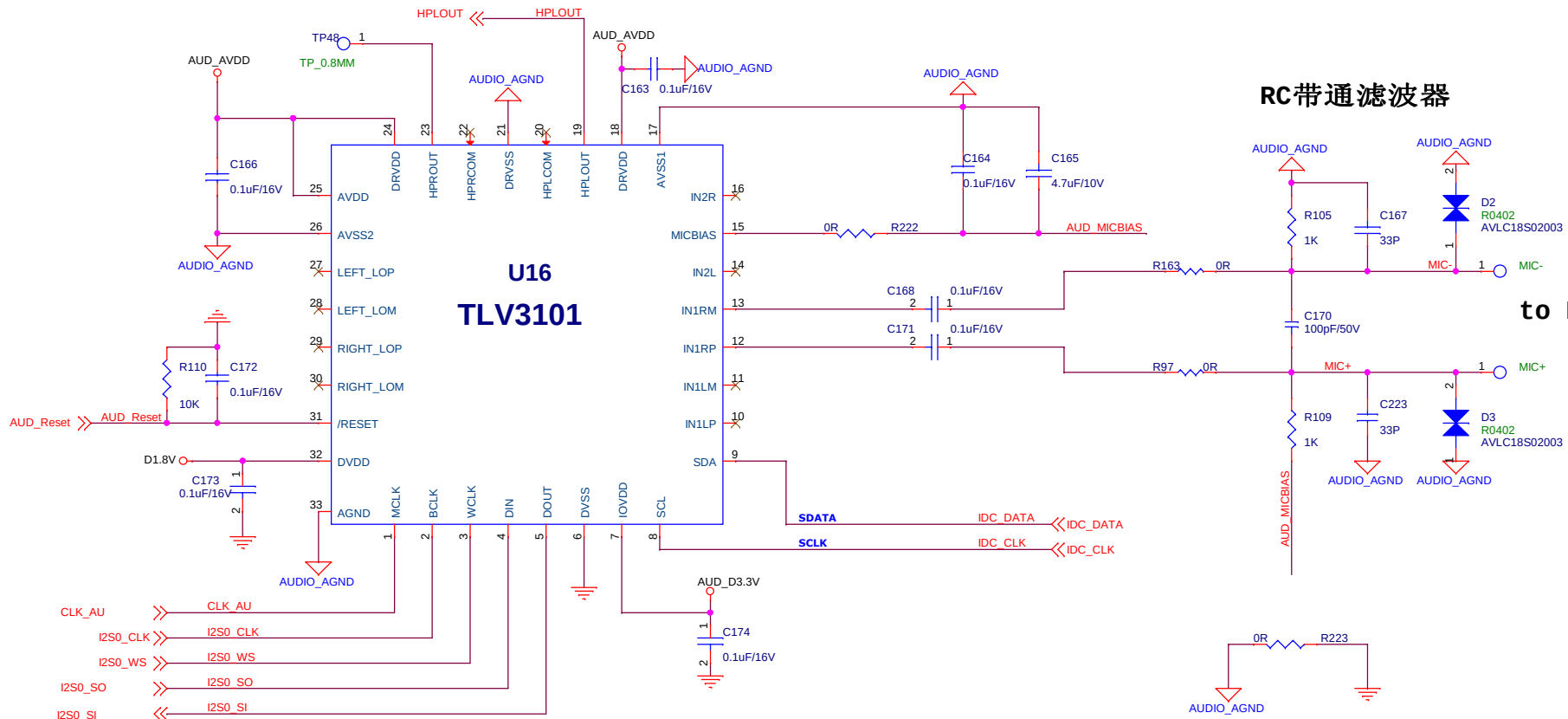


layout时, 紧靠DDR3每个电源脚放置一去耦电容!



SKY LIGHT Electronic (ShenZhen) Limited	
Title	HPC02AB
Size	Document Number
B	DDRIII-128Mx16
Date:	Tuesday, March 08, 2016
Sheet	10 of 17
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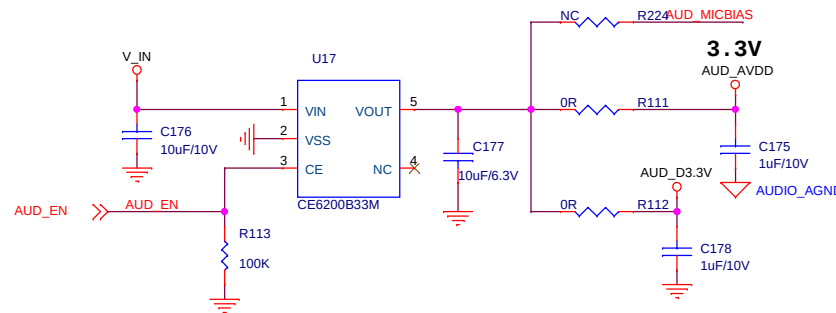




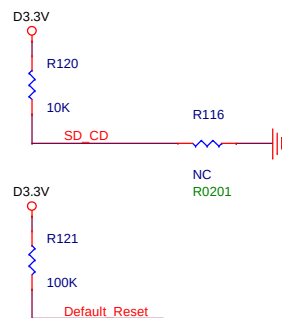
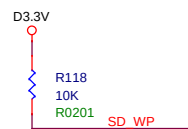
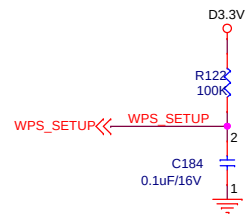
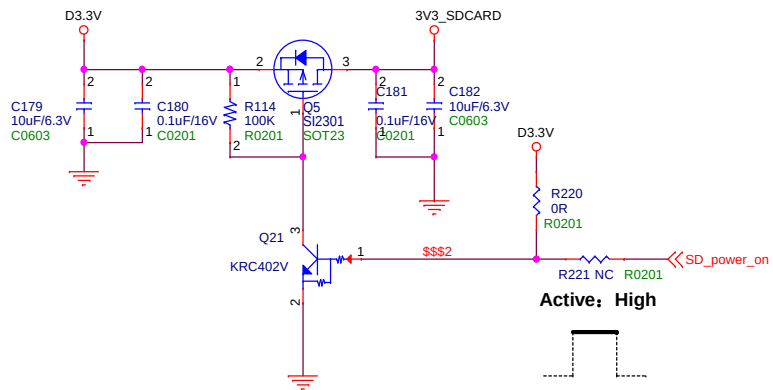
RC带通滤波器

to MIC

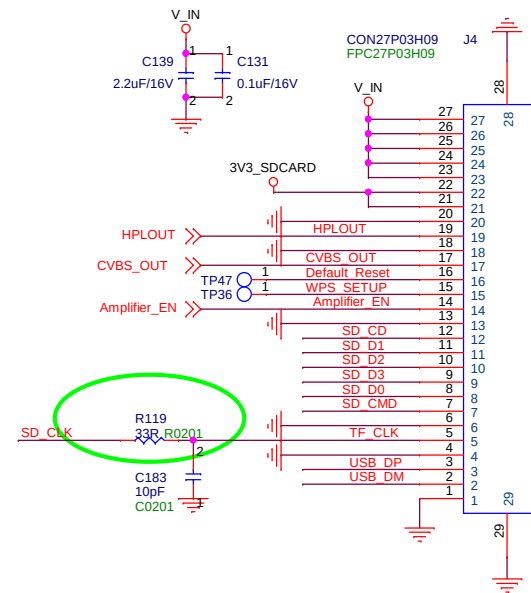
鉴于DVT阶段HPC02音频问题，参考规格书做分地处理，模拟地和数字地采用0欧电阻隔离



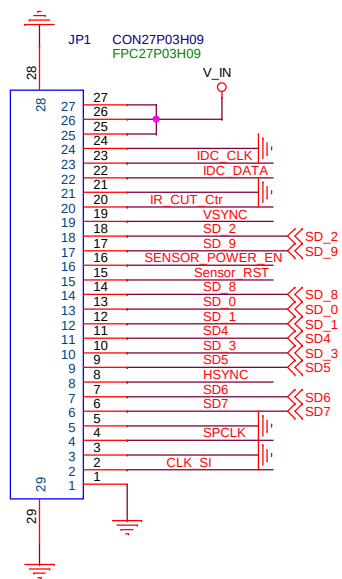
SKY LIGHT Electronic (ShenZhen) Limited		
Title		Drawn By
HPC02AB		Lizhiqiang
Size	Document Number	Rev
B	Audio Codec	002.02
Date: Tuesday, March 08, 2016		
Sheet 13 of 17		



更改SD卡9_PIN CD脚接至SD_CD加上拉20150330



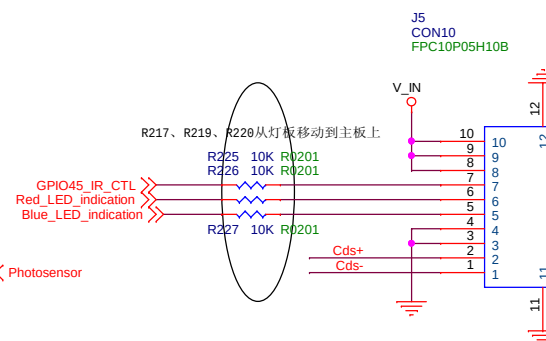
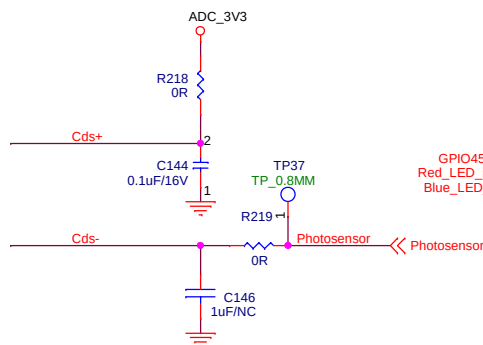
SKY LIGHT Electronic (ShenZhen) Limited			
Title		Drawn By	
HPC02AB		wangguanming	
Size		Document Number	
B		TF Card-Connector	
Date:		Rev	
Monday, March 14, 2016		V02.03	
Sheet		of	
1		17	



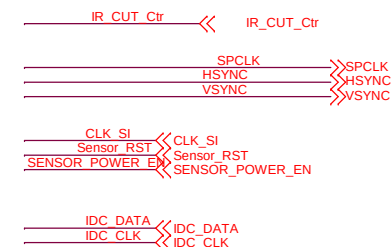
To Sensor Board (FPC座子)

FPC座 27Pin PH0.3

Sensor型号为: OV9712



To IRLED Board



 Sky Light Electronic (Shen Zhen) Limited	
Title	HPC02AB
Size	Document Number
B	Sensor-OV9712
Date:	Tuesday, March 08, 2016
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Drawn By	wangguanming

