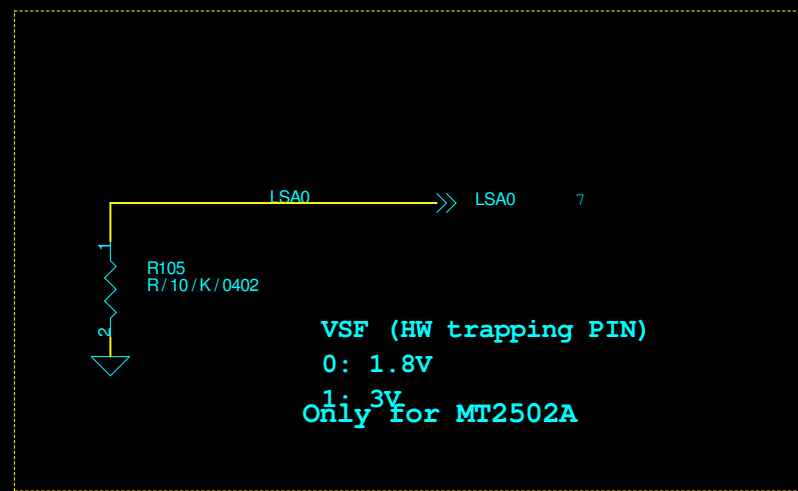
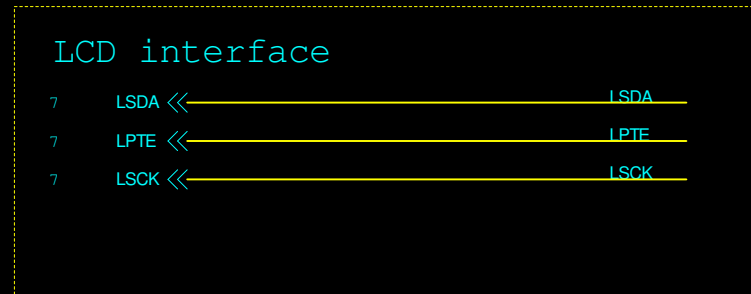
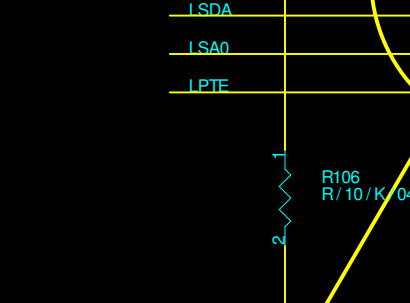


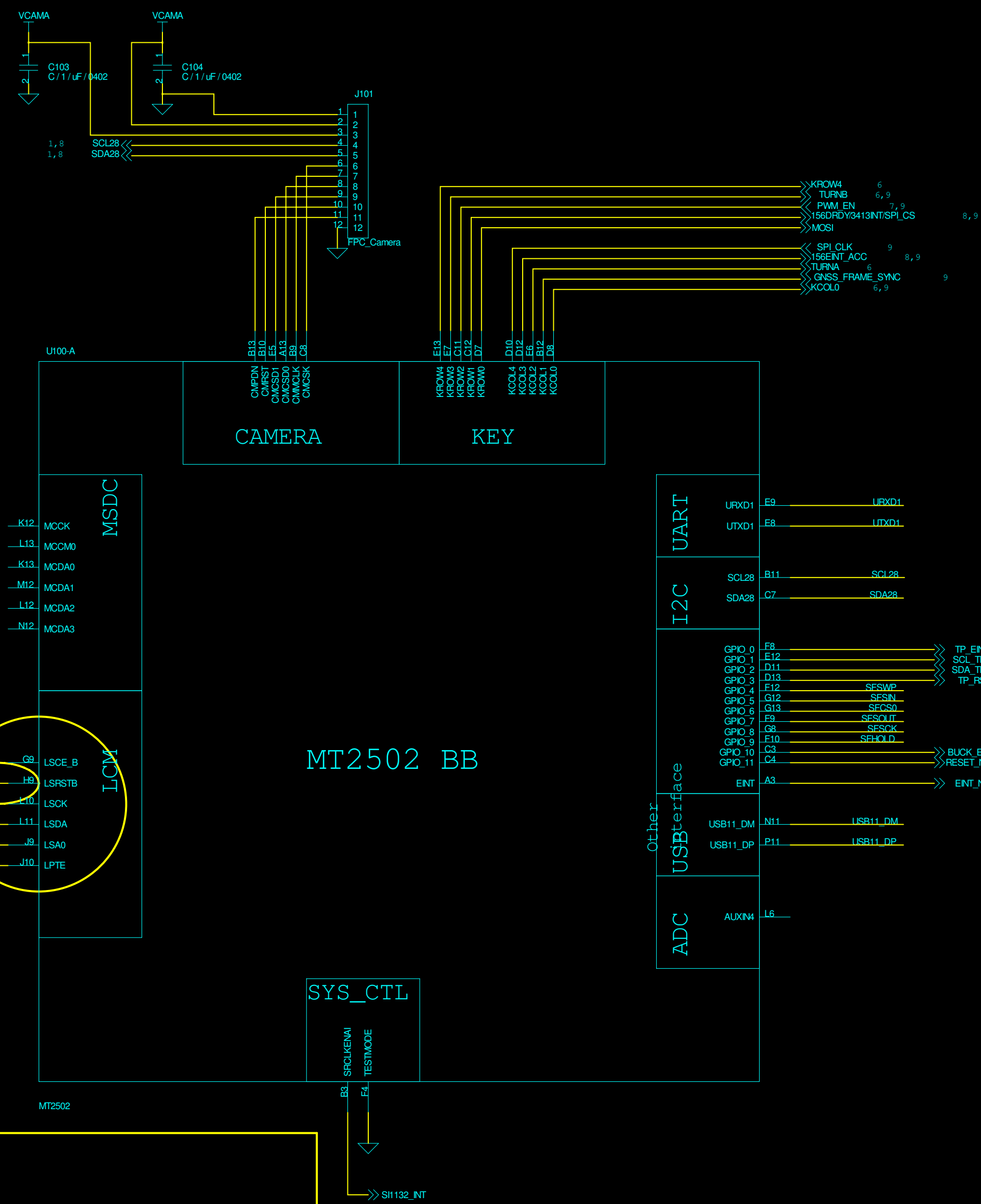


LSRSTB only for test mode ,
can't use for any part

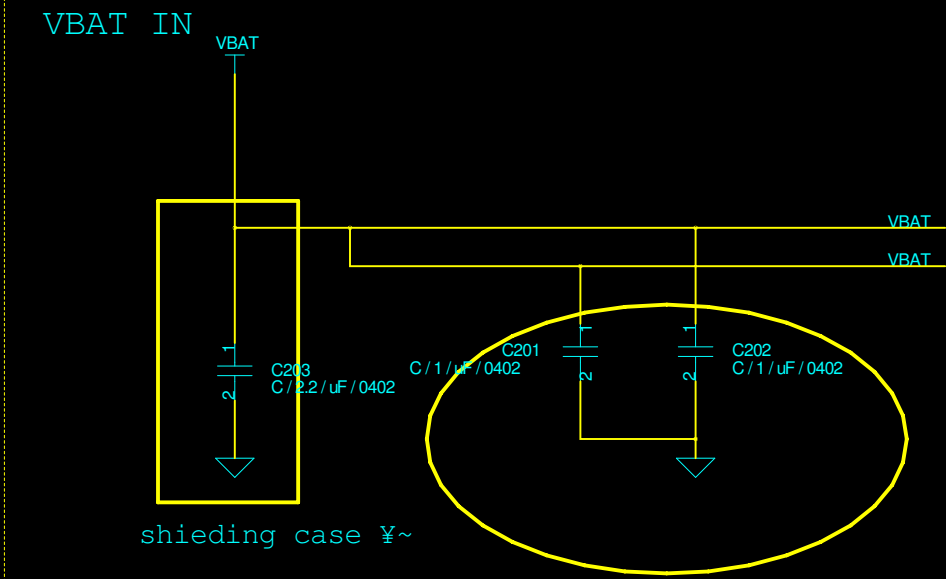
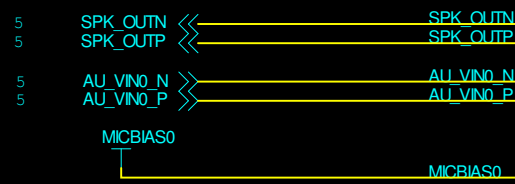
LSCK can't have any pull up
circuit



Lcm I/O power domain is VI018 ,In sleep mode ,VI018 will
shut off, if use LCM I/O for external device, please make
sure , in sleep mode with shut off VI018 ,the device is no
leakage , and once again wake up system , can normal
work .If have any question,please call MTK



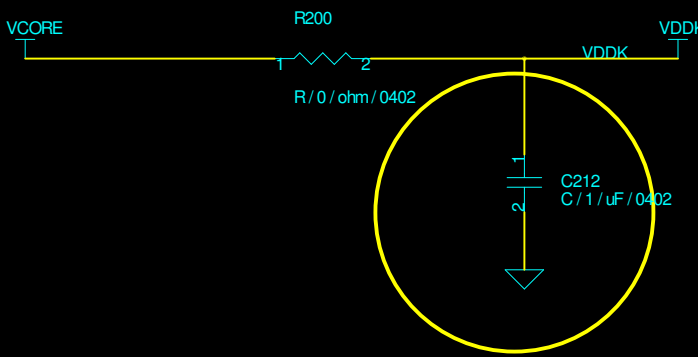
Audio



close to MT2502 each power in ball (M10,E1)

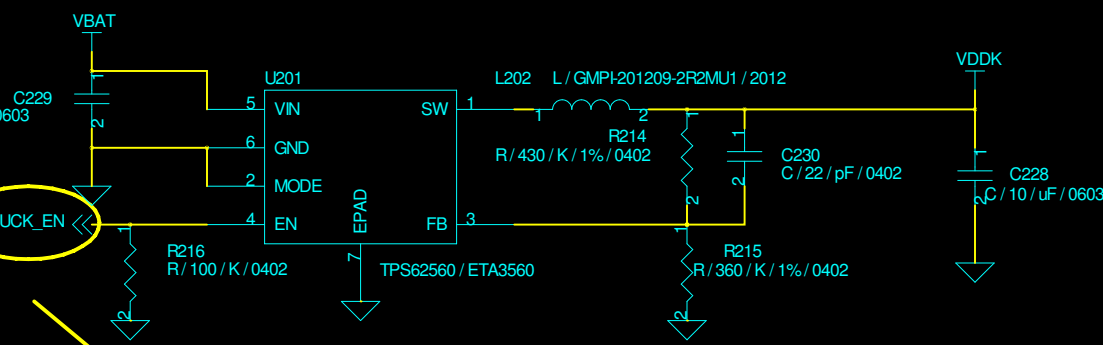
POWER IN

With or without use of the external buckf
R200 must SMT



close to MT2502 VDDK Pin (A11)

DC-DC Backup



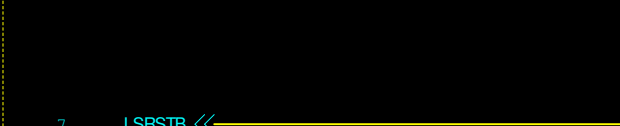
Material Determination of single BUCK1*		
PART NUMBER:	PACKAGE:	Notes:
ETA3406		
ETA3415	ETA3415G08KTB0518 Pin to Pin	Design native external buck part

RTC_XOSC32_ENB

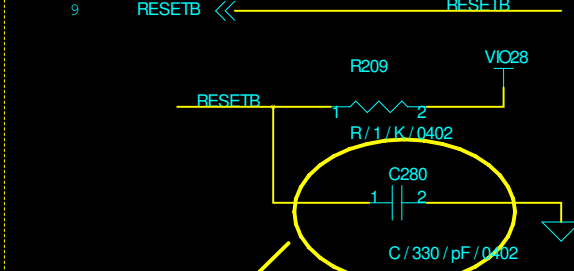


XTAL_SEL: VRTC domain
1: f32k_ck src INT clock source
0: f32k_ck src EXT clock source

LCD IF:

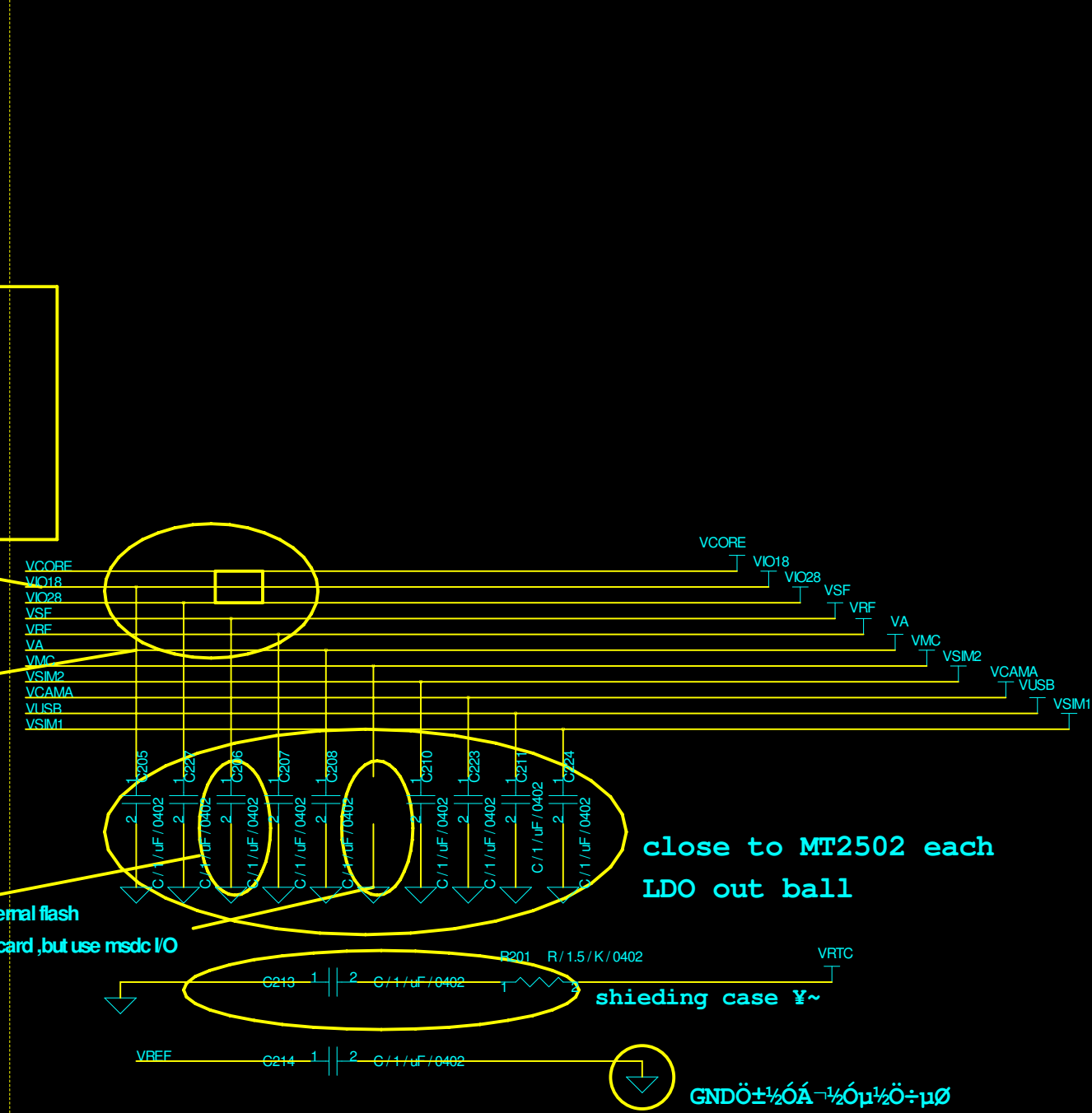


SYSTEM CONTROL



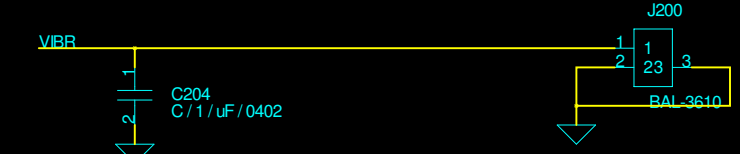
This CAP(330pF) is optional for better ESD performance
This Cap should be placed near BB

PMU LDO

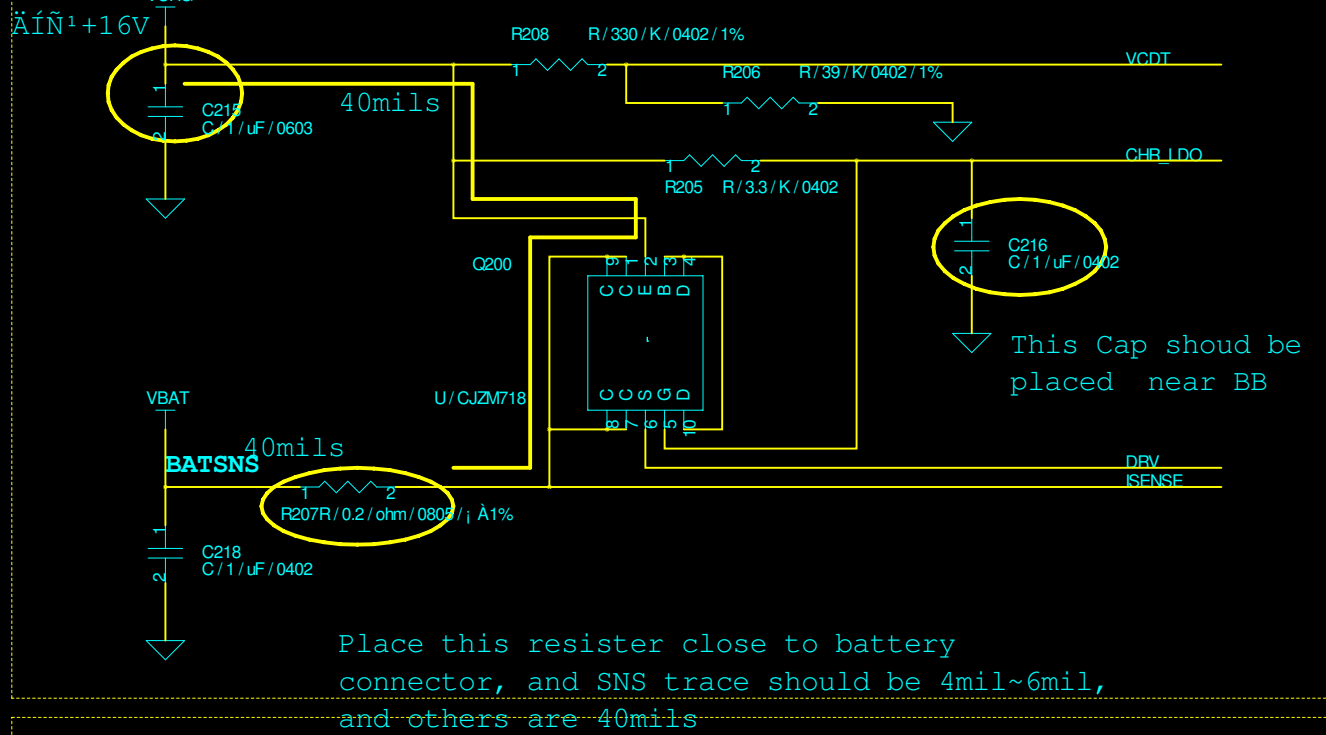


C214 close to MT2502
LDO out ball

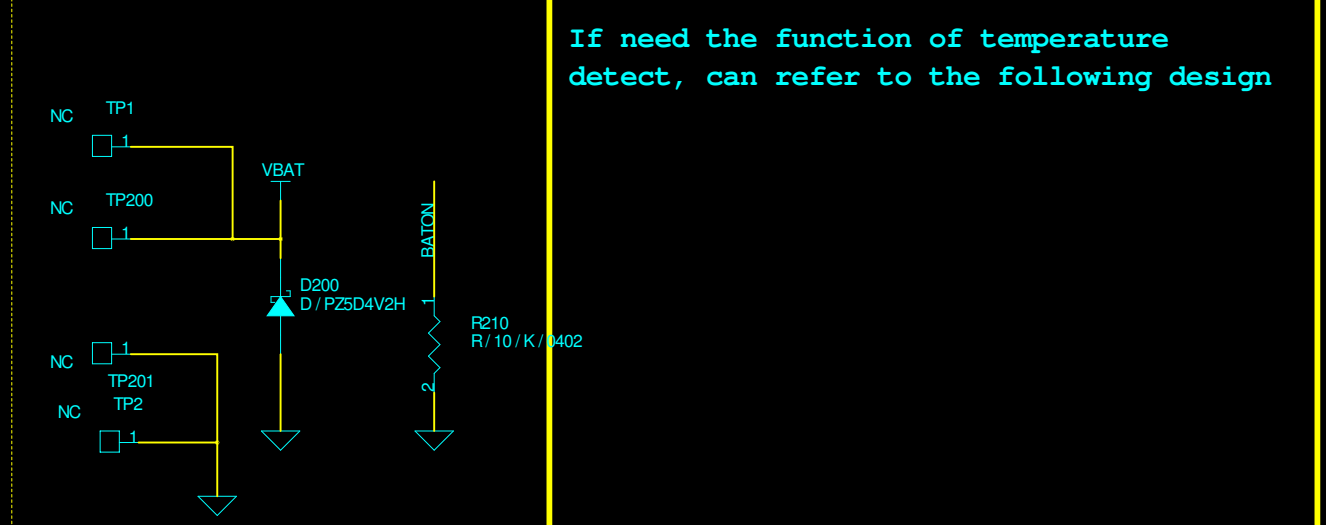
Vibrator

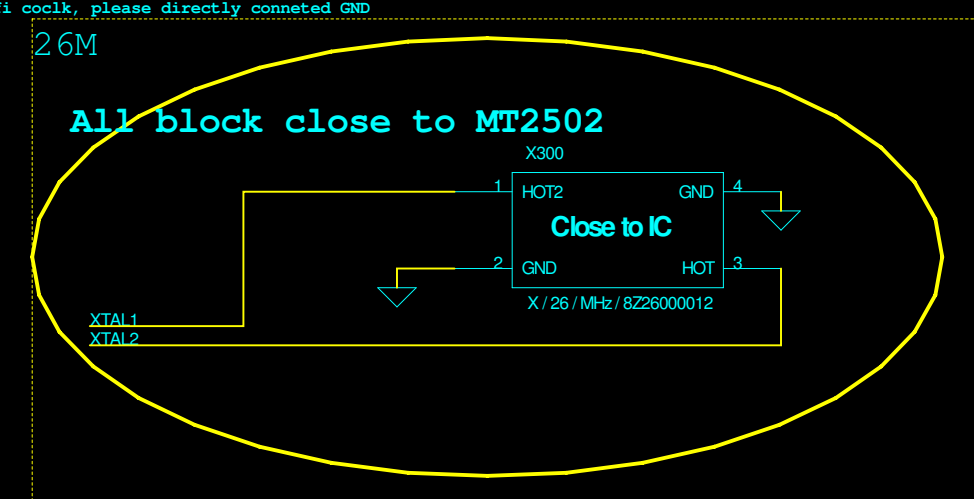


Charge

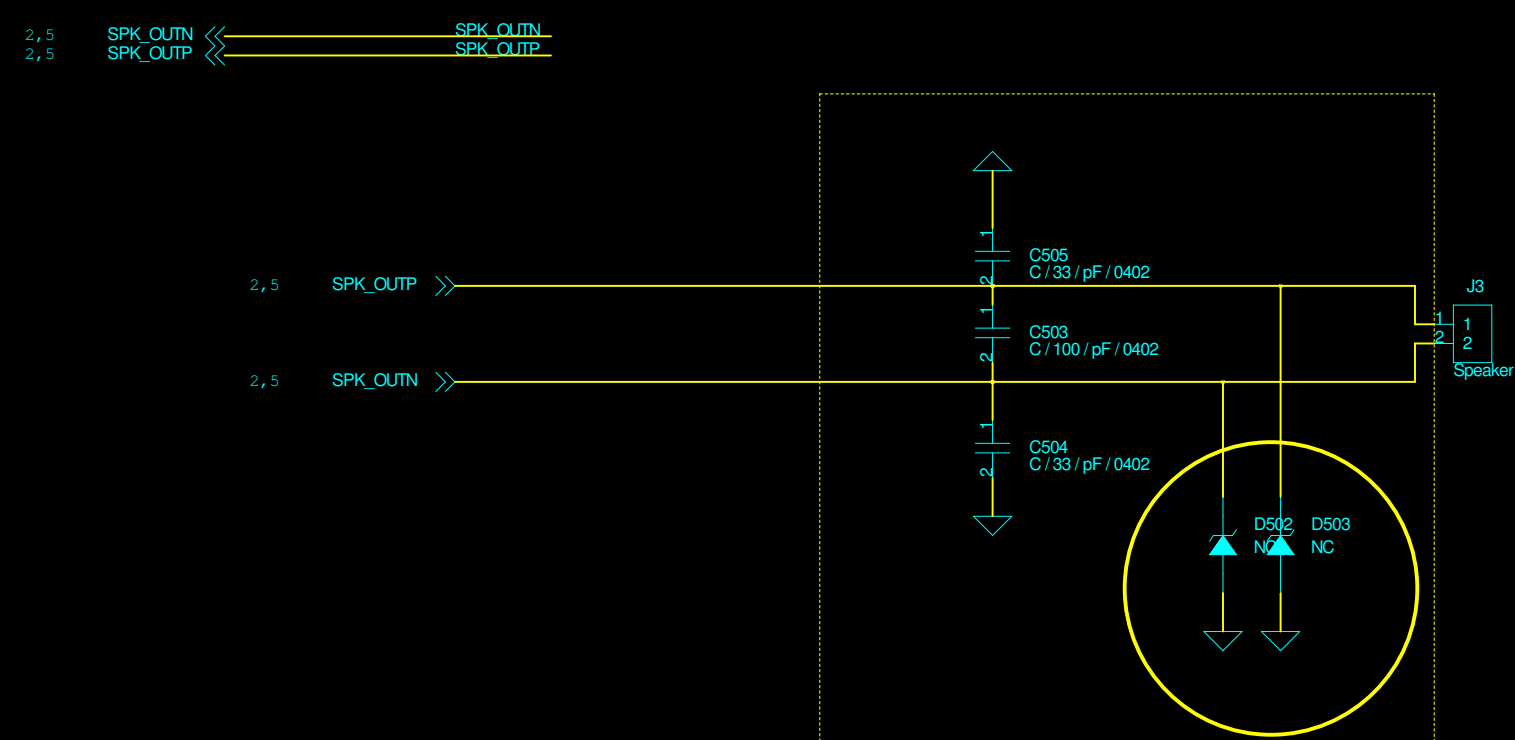


Battery connector



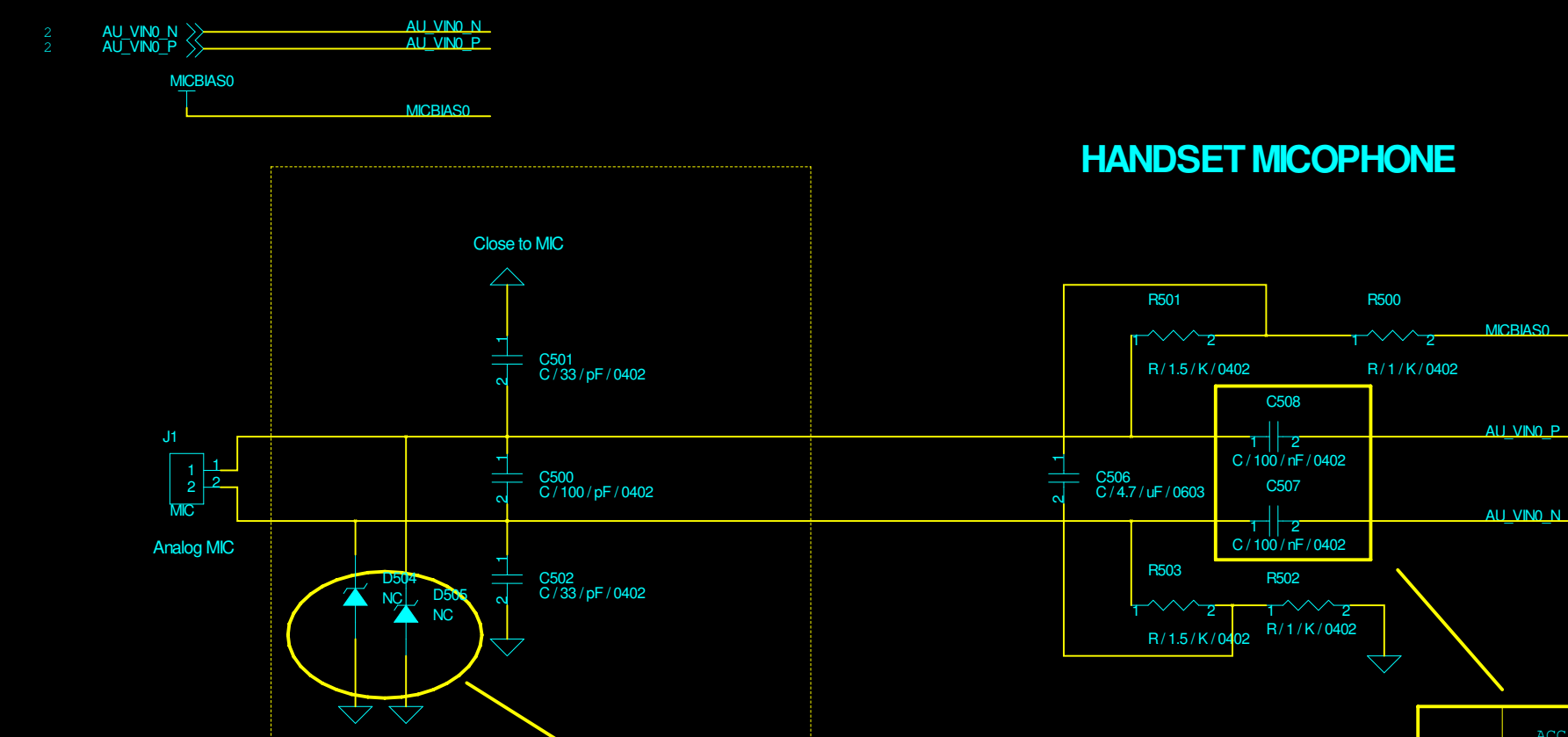


Speaker



NOTE: 1. Total C load of Audio output must < 330pf and close to JACK
2. For DC couple case please choose Bi-direction component

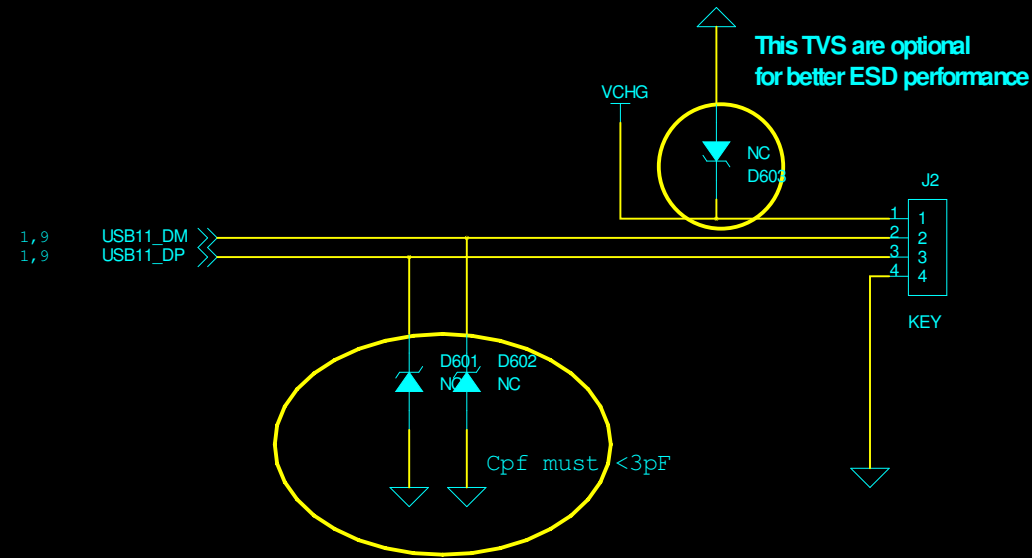
MIC



This ESD components are optional for better ESD performance
NOTE: 1. Total C load of mic input must < 330pf and close to JACK
2. For DC couple case please choose Bi-direction component

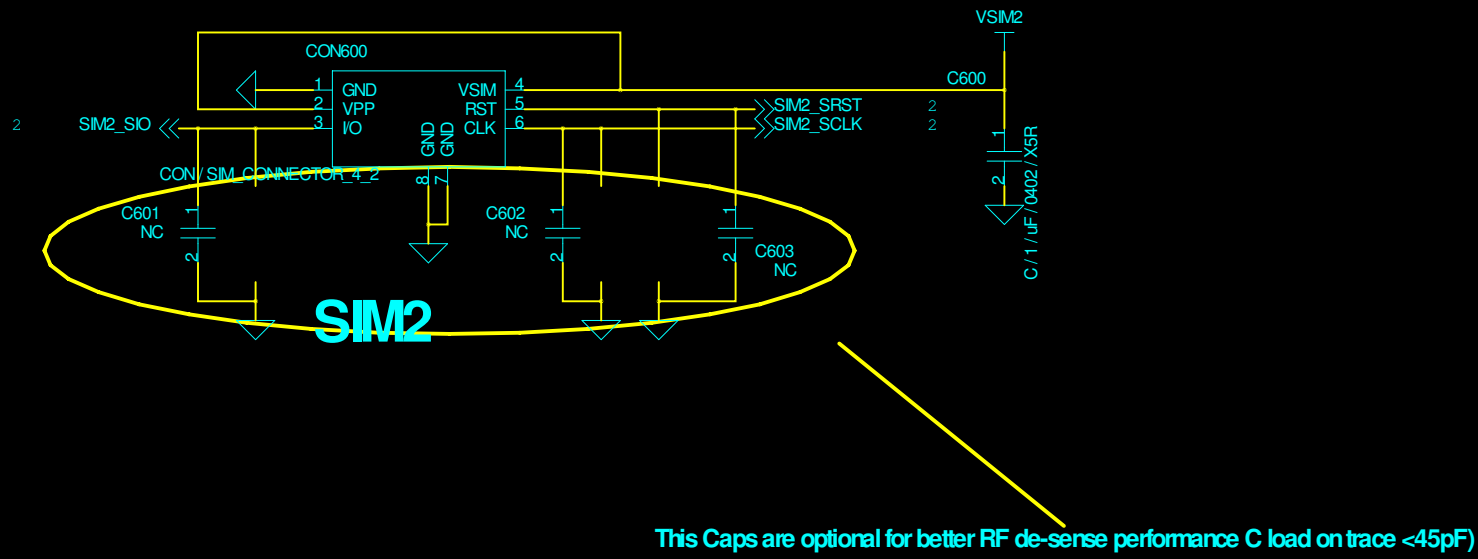
	ACC mode	Low cost mode
C508	100nF	Short
C507	100nF	Short

USB

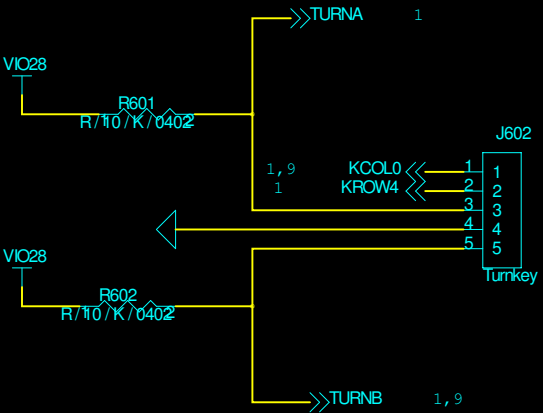
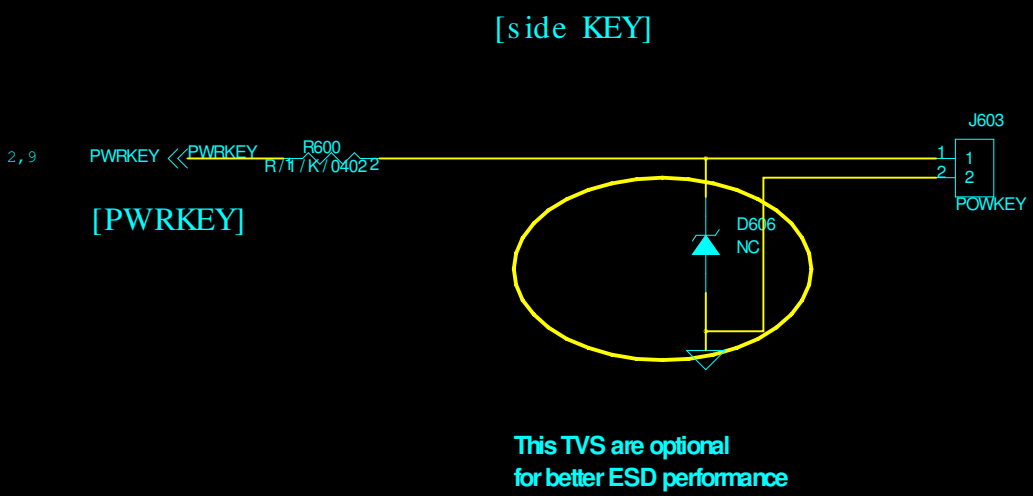


This ESD components are optional for better ESD performance
NOTE: 1. C load must < 3pf and close to JACK

SIM



KEY



[illegible][illegible][illegible]

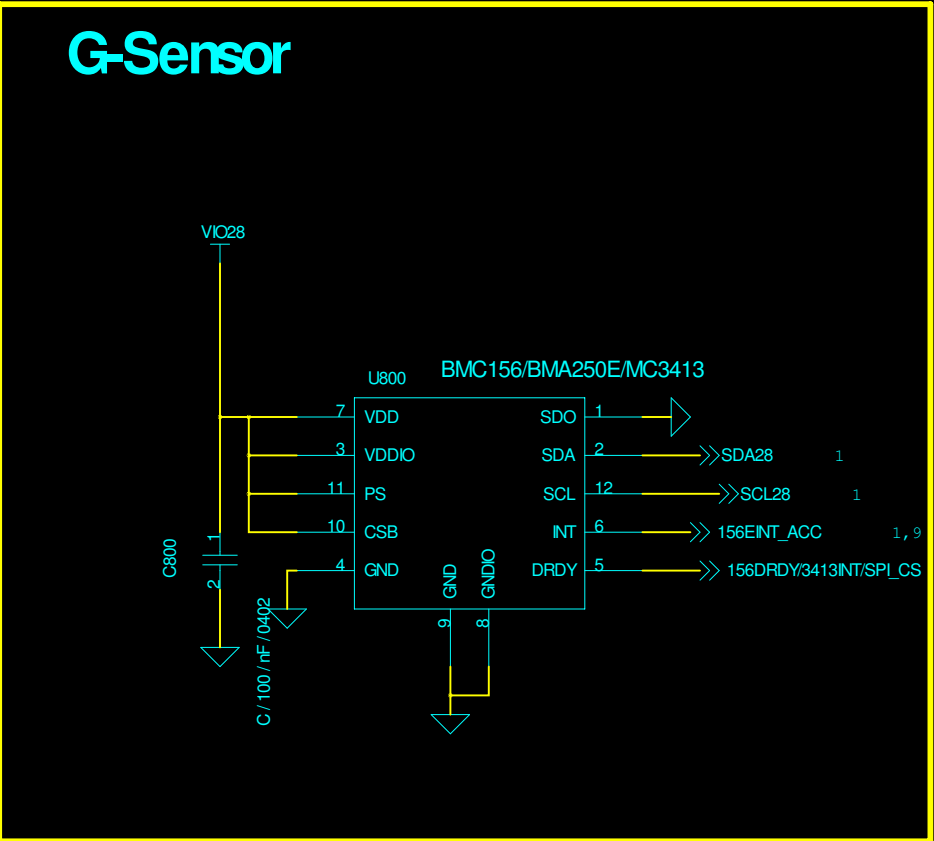


Figure 10 shows the pin connections for the ATmega328P. The connections are as follows:

- TP903 is connected to LUTXD1.
- TP911 is connected to LRXD1.
- TP912 is connected to VBAT.
- TP900 and TP902 are connected to PWIRKEY.

The diagram shows a square wave pulse on a line labeled TP915. The pulse starts at a low level (ground), rises to a high level (VCHG), and then returns to the low level. The high level is labeled VCHG at both the start and end of the pulse.

JTAG trap
 00:X(BPI_BUS1,BPI_BUS2)
 01:KEYPAD(BPI_BUS1,BPI_BUS2)
 10:Reserve
 11:CAM(BPI_BUS1,BPI_BUS2)

MT2502 JTAG MUX Keypad / CAM by HW trapping , Pull high use 10K , pull down use 10K

Pinmux diagram showing connections for JTAG and Keypad interface. The diagram includes pins TP904 through TP910, JTAG pins (JTAG0, JTAG1, JTAG2, JTAG3, JTAG4, JTAG5), and Keypad pins (KEYPAD0 through KEYPAD5). Internal components like SPI CLK, 15E2NT ACC, GSS, FRAME, SYNC, TURN, PWR, EN, 156DRDVS413, INT, S, L, CS, RESETB, and JTAG pins are also shown.

JTAG Pin mux with keypad , Please reserve test point on related GPIO / Keypad interface

Serial Flash

Shielding case all sheet

MXIC MX25U12835FZNI-10G,
1.8V,128Mb,WSON 6*8:

SHOLD : SIO3
SWP : SIO2
SOUT : SQT_SI : DQ0
SIN : SQT_SO : DQ1 Option only for MT2502A

**MXIC MX25U12835FZNI-10G,
1.8V,128Mb,WSO 6*8:**

