



SPZB32Wxy1.z

802.15.4 ZigBee® modules based on the STM32W chipset

Features

- 2.4 GHz IEEE 802.15.4-compliant SMD modules based on the ST STM32W chipset solution featuring:
 - Integrated 2.4 GHz transceiver
 - PHY and MAC IEEE 802.15.4 features
 - Integrated ARM® Cortex-M3 core
 - Integrated embedded Flash and RAM
 - Integrated encryption (AES-128) accelerator
- Power amplified RF performances:
 - Up to 20 dBm nominal TX output power
 - Up to 105 dBm RX sensitivity
- Robust Wi-Fi and Bluetooth® coexistence
- 16 channels (IEEE 802.15.4 channel 11 to 26)
- Multiple configurable interfaces available (UART, SPI, I2C, ADC, GPIOs)
- Industry standard JTAG programming
- Onboard 24 MHz and 32.768 kHz stable Xtal
- Less than 2 μ A typ power consumption in deep sleep mode (32.768 Xtal)
- Multiple antenna options: integrated antenna or integrated UFL connector
- Multiple Protocol Stack Options
- Single voltage supply (2.1 to 3.6 V)
- FCC and CE compliant qualified
- Small Form Factor : 16.4 x 26.5 mm
- Operating temperature range: -40 °C to +85 °C



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1 Description

SPZB32Wxy1.z is a series of ready-to-use IEEE 802.15.4/ZigBee compliant and power amplified RF modules optimized for embedded applications that require low data rate communications and high transmission range capabilities based on the STM32W single chip that integrates a 2.4 GHz, IEEE 802.15.4-compliant transceiver together with an ARM® Cortex embedded processor .

The modules are very compact and enable OEMs to easily add wireless capabilities to electronics devices by optimizing time-to-market, cost, size, and consumption of their target applications. No RF experience or expertise is required to add this powerful networking capability to the final product.

24 MHz high stability Xtal is available aboard the modules to perform the timing requirements as per IEEE 802.15.4/ZigBee® specifications; additionally a 32.768kHz Xtal is also provided onboard for low power operation.

A single supply voltage is requested to power the modules. The supply is in the range of 2.1 to 3.6 V. The voltage supply also determines the I/O ports level allowing an easy interface with additional peripherals.

An advanced solution integrating PA and LNA in a single package is aboard to ensure excellent power transmission and receiver sensitivity performances.

To support user defined applications, a number of peripherals such as GPIO, UART, I2C, ADC and general purpose timers are available and user selectable.

The size and footprint of this series of modules is equivalent to that of the series SPZB32Wxy2.z to facilitate the evaluation of the different range options on the target application.

The series groups multiple versions that differ in terms of memory size , antenna (ceramic antenna or integrated u.fl connector for the connection of an external antenna) and stacks options (ZigBee, RF4CE, SimpleMAC).

The SPZB32W1y1.z versions are based on the STM32W108CB chipset integrating 128 kB of embedded flash memory and 8 kB of RAM available for data and program storage.

For technical details on the STM32W108CB chipset refer to the related datasheet. For technical details on the supported stacks refer to the related user guide and application notes.

2 RoHS compliance

ST modules are RoHS compliant and comply with ECOPACK[®] norms.

3 Application

- Smart energy applications
- Machine2Machine industrial control
- Wireless sensor networks
- Home/building automation
- Smart appliances
- Wireless alarms and security systems
- Lighting control
- Remote monitoring

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4 Block diagram

Figure 1. SPZB32WxA1.z block diagram

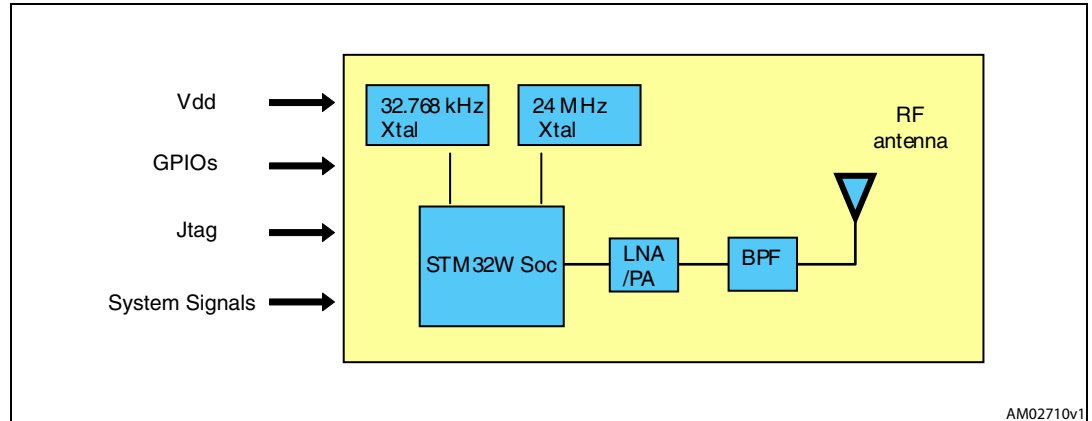
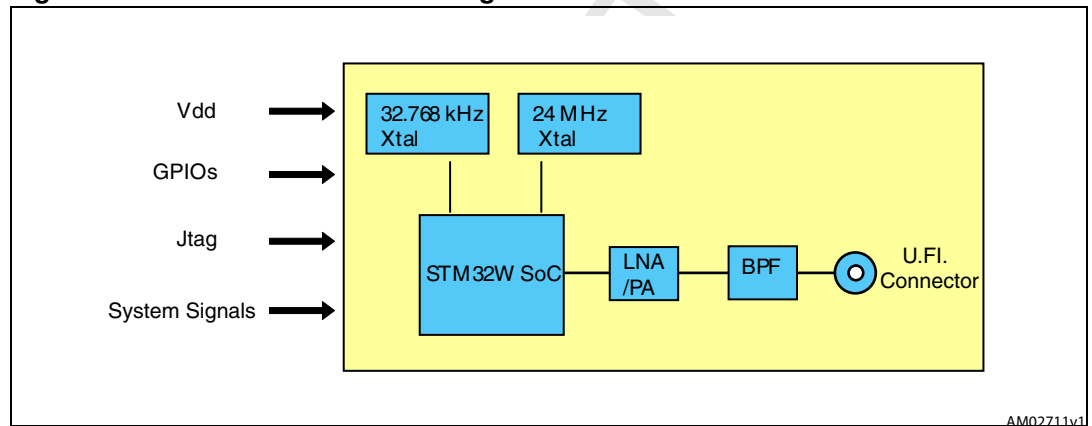


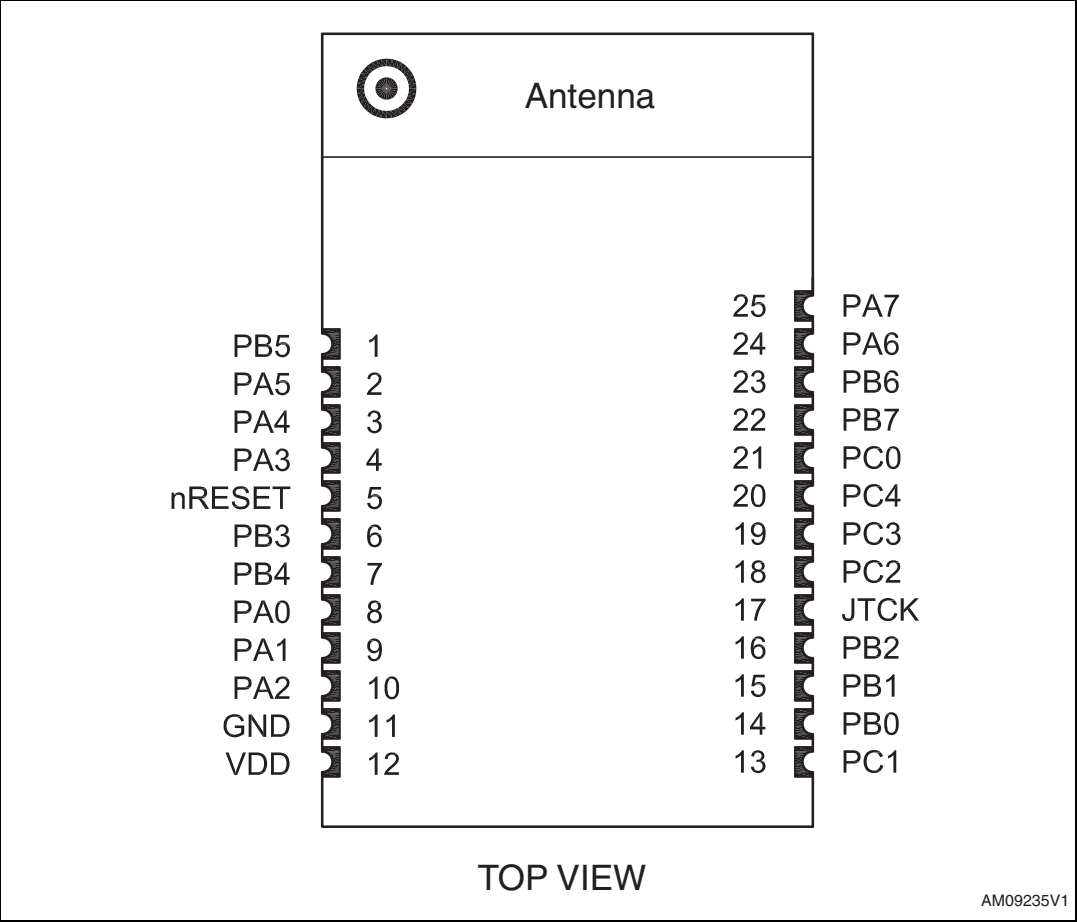
Figure 2. SPZB32WxC1.z block diagram



5 Pin settings

5.1 Pin connections

Figure 3. Pin connection diagram





5.2 Pin description

Table 1. Pin description

Module pin n°	Pin name	Direction	STM32W pin	Description
1	PB5	I/O	43	Digital I/O
	ADC0	Analog	43	ADC Input 0
	TIM2CLK	I	43	Timer 2 external clock input
	TIM1MSK	I	43	Timer 1 external clock mask input
2	PA5	I/O	27	Digital I/O
	ADC5	Analog	27	ADC Input 1
	PTI_DATA	O	27	Frame signal of PTI (Packet Trace Interface)
	nBOOTMODE	I	27	Embedded serial bootloader activation out of reset
	TRACEDATA3	O	27	Synchronous CPU trace data bit 3
3	PA4	I/O	26	Digital I/O
	ADC4	Analog	26	ADC Input 0
	PTI_EN	O	26	Frame signal of PTI (Packet Trace Interface)
	TRACEDATA2	O	26	Synchronous CPU trace data bit 2
4	PA3	I/O	25	Digital I/O
	SC2nSSEL	I	25	SPI SLAVE SELECT of Serial Controller 2
	TIM2_CH2	I/O	25	Timer 2 channel 2 output (or input - Disable remap with TIM2_OR[5])
	TRACECLK	O	25	Synchronous CPU trace clock
5	nRESET	I	12	Active low reset (an internal pull-up of 30 kohm typ. is provided)
6	PB3	I/O	19	Digital I/O
	UART_CTS	I	19	UART CTS handshake of Serial Controller 1
	SC1SCLK	I/O	19	SPI slaver clock of Serial Controller SC1 / SPI master clock of Serial Controller SC1
	TIM2_CH3	I/O	19	Timer 2 channel 3 input / Timer 2 channel 3 output

**Table 1. Pin description (continued)**

Module pin n°	Pin name	Direction	STM32W pin	Description
7	PB4	I/O	20	Digital I/O
	UART_RTS	O	20	UART RTS handshake of Serial Controller 1
	TIM2_CH4	I/O	20	Timer 2 channel 4 input / Timer 2 channel 4 output
	SC1nSSEL	I	20	SPI slave select of Serial Controller 1
8	PA0	I/O	21	Digital I/O
	SC2MOSI	O	21	SPI Master data out of Serial Controller 2
	SC2MOSI	I	21	SPI Slave data in of Serial Controller 2
	TIM2_CH1	I/O	21	Timer 2 channel 1 input / Timer 2 channel 1 output
9	PA1	I/O	22	Digital I/O
	SC2MISO	I	22	SPI Master data in of Serial Controller 2
	SC2MISO	O	22	SPI Slave data out of Serial Controller 2
	SC2SDA	I/O	22	TWI (I2C) data of Serial Controller 2
	TIM2_CH3	I/O	22	Timer 2 channel 3 input / Timer 2 channel 3 output
10	PA2	I/O	24	Digital I/O
	SC2SCLK	O	24	SPI Master clock of Serial Controller 2
	SC2SCLK	I	24	SPI Slave clock of Serial Controller 2
	SC2SCL	I/O	24	TWI (I2C) clock of Serial Controller 2
	TIM2_CH4	I/O	24	Timer 2 channel 4 input / Timer 2 channel 4 output
11	GND	--	49	Ground
12	VDD	Power	16,23,28,37	Input power supply
13	PC1	I/O	38	Digital I/O
	ADC3	Analog	38	ADC Input 3
	SWO	O	38	Serial Wire Output asynchronous trace output to debugger
	TRACEDATA0	O	38	Synchronous CPU trace data bit 0

**Table 1. Pin description (continued)**

Module pin n°	Pin name	Direction	STM32W pin	Description
14	PB0	I/O	36	Digital I/O
	VREF (O/I)	Analog	36	ADC reference output / ADC reference input
	TIM1CLK	I	36	Timer 1 external clock input
	TIM2MSK	I	36	Timer 2 external clock mask input
	IRQA	I	36	External interrupt source A
	TRACECLK	O	36	Synchronous CPU trace clock
15	PB1	I/O	30	Digital I/O
	SC1TXD	O	30	UART transmit data of Serial Controller 1
	SC1MOSI / SC1MISO	O	30	SPI master data out of Serial Controller 1 / SPI slave data out of Serial Controller 1
	SC1SDA	I/O	30	TWI (I2C) data of Serial Controller 1
	TIM2_CH1	I/O	30	Timer 2 channel 1 input / Timer 2 channel 1 output
16	PB2	I/O	31	Digital I/O
	SC1RXD	I	31	UART receive data of Serial Controller 1
	SC1MISO / SC1MOSI	I	31	SPI master data in of Serial Controller SC1 / SPI slave data in of Serial Controller 1
	SC1SCL	I/O	31	TWI (I2C) clock of Serial Controller 1
	TIM2_CH2	I/O	31	Timer 2 channel 2 input / Timer 2 channel 2 output
17	JTCK	I	32	JTAG clock input from debugger
	SWCLK	I/O	32	Serial Wire clock input/output with debugger
18	PC2	I/O	33	Digital I/O
	JTDO	O	33	JTAG data out to debugger
	SWO	O	33	Serial Wire Output asynchronous trace output to debugger
19	PC3	I/O	34	Digital I/O
	JTDI	I	34	JTAG data in from debugger
20	PC4	I/O	35	Digital I/O
	JTMS	I	35	JTAG mode select from debugger
	SWDIO	I/O	35	Serial Wire bidirectional data to/from debugger

**Table 1. Pin description (continued)**

Module pin n°	Pin name	Direction	STM32W pin	Description
21	PC0	I/O	40	Digital I/O (high current)
	JRST	I	40	JTAG reset input from debugger
	TRACEDATA1	O	40	Synchronous CPU trace data bit 1
	IRQD	I	40	External interrupt source D
22	PB7	I/O	41	Digital I/O
	TIM1_CH2	O	41	Timer 1 channel 2 output
	TIM1_CH2	I	41	Timer 1 channel 2 input
	IRQC	I	41	External interrupt source C
	ADC2	I	41	ADC input 2
23	PB6	I/O	42	Digital I/O
	TIM1_CH1	O	42	Timer 1 channel 1 output
	TIM1_CH1	I	42	Timer 1 channel 1 input
	IRQB	I	42	External interrupt source B
	ADC1	Analog	42	ADC input 1
24	LNA/ENABLE	I	29	Digital input, module firmware dependent, externally forced by the user dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L internal LNA. (HIGH= internal LNA enabled, LOW= internal LNA disabled).
	PA6/LNA_ENABLE	O	29	Digital output, module firmware dependent, internally forced by application dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L internal LNA. (HIGH= internal LNA enabled, LOW= internal LNA disabled).
25	RF_STANDBY	I	18	Digital input, module firmware dependent, externally forced by the user dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L front-end STANDBY state. (HIGH= Front-end enabled, LOW= Front-end forced in the STANDBY state).
	PA7/RF_STANDBY	O	18	Digital output, module firmware dependent, internally forced by application dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L front-end STANDBY state. (HIGH= Front-end enabled, LOW= Front-end forced into STANDBY state).

6 Electrical characteristics

6.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Module supply voltage	- 0.3	3.6	V
V_{in}	Input voltage on any digital pin	- 0.3	$V_{DD} + 0.3$	V
T_{stg}	Storage temperature	-40	+85	°C
T_{sld}	Soldering temperature < 10s		250	°C

6.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Module supply voltage	$-40\text{ °C} < T < +85\text{ °C}$	2.1	3.3	3.6	V
T_{stg}	Operating ambient temperature		-40		+85	°C

6.3 DC electrical characteristics

Table 4. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IRX	RX current	$V_{DD} = 3.3\text{ V}$, $T = 25\text{ °C}$	-	20	-	mA
ITX	TX current	$P_o = 18\text{ dBm}$, $V_{DD} = 3.3\text{ V}$, $T = 25\text{ °C}$, $F = 2450\text{ MHz}$	-	120	-	mA
IDS	Deep sleep current (32.768 kHz oscillator)	$V_{DD} = 3.3\text{ V}$, $T = 25\text{ °C}$	-	1.3	-	mA

6.4 Digital I/O specifications

Table 5. Digital I/O specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	$2.1 < V_{dd} < 3.6 \text{ V}$	0		$0.5 \times V_{dd}$	V
V_{IH}	High level input voltage	$2.1 < V_{dd} < 3.6 \text{ V}$	$0.62 \times V_{dd}$		V_{dd}	V
I_{il}	Input current for logic 0	$2.1 < V_{dd} < 3.6 \text{ V}$			-0.5	mA
I_{ih}	Input current for logic 1	$2.1 < V_{dd} < 3.6 \text{ V}$			0.5	mA
R_{ipu}	Input pull-up resistor			30		$k\Omega$
R_{ipd}	Input pull-down resistor			30		$k\Omega$
V_{OL}	Low level output voltage		0		$0.18 \times V_{dd}$	V
V_{OH}	High level output voltage		$0.82 \times V_{dd}$		V_{dd}	V
I_{OHS}	Output source current (standard)				4	mA
I_{OLS}	Output sink current (standard)				4	mA
I_{OHH}	Output source current (high current)				8	mA
I_{OLH}	Output sink current (high current)				8	mA
I_{OTot}	Total output current for I/O				40	mA

6.5 RF electrical characteristics

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Frequency range	$V_{dd} = 3.3 \text{ V}$, $T = 25 \text{ }^{\circ}\text{C}$	2405		2480	MHz
TX	Output power	$V_{dd} = 3.3 \text{ V}$, $T = 25 \text{ }^{\circ}\text{C}$			20	dBm
RX	Sensitivity	$V_{dd} = 3.3 \text{ V}$, 1 % PER			-105	dBm
	Adjacent channel rejection	$\pm 5 \text{ MHz}$ $\pm 10 \text{ MHz}$		35 40		dBm

7 Mechanical dimensions

Figure 4. Mechanical dimensions

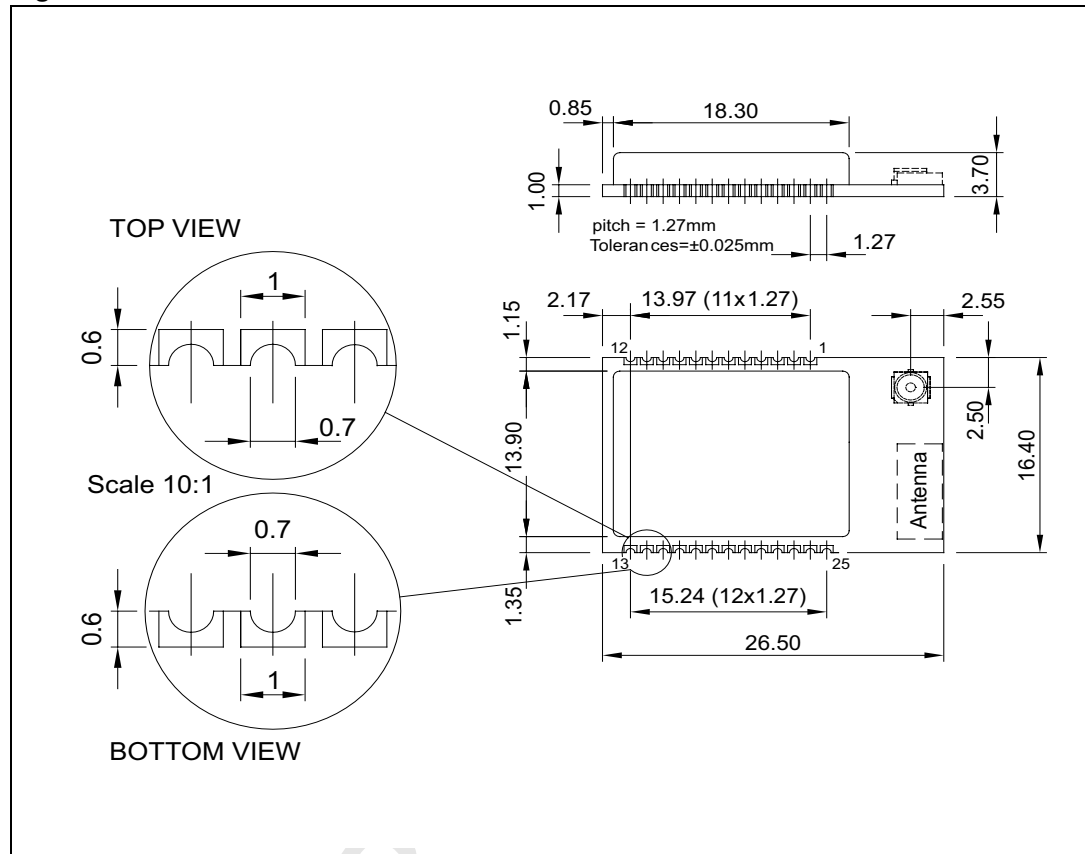
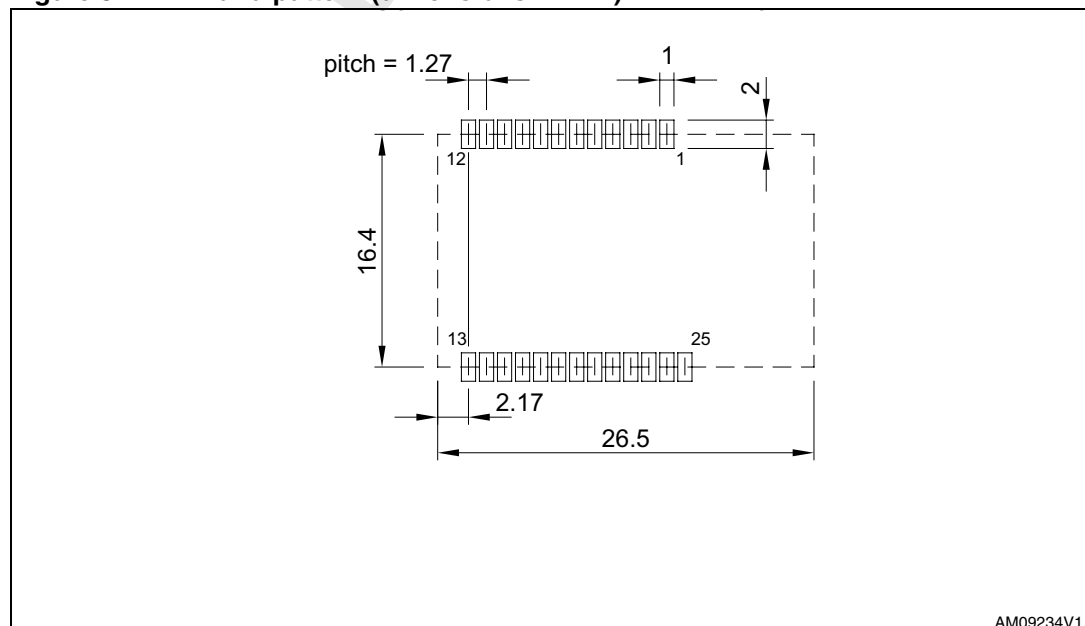


Figure 5. Pin land pattern (dimensions in mm)



8 Soldering

The soldering phase must be carefully executed; in order to avoid undesired melting phenomenon, particular attention must be paid to the set-up of the peak temperature.

Below are some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations

Table 7. Soldering

Profile feature	PB free assembly
Average ramp up rate ($T_{S\text{MAX}}$ to T_P)	3 °C / sec max.
Preheat	
Temperature min. ($T_{S\text{MIN}}$)	150 °C
Temperature max. ($T_{S\text{MAX}}$)	200 °C
Time ($T_{S\text{MIN}}$ to $T_{S\text{MAX}}$) (t_s)	60 – 100 sec
Time maintained above:	
Temperature T_L	217 °C
Time t_L	40 – 70 sec
Peak temperature (T_P)	240 + 0 °C
Time within 5 °C of actual peak temperature (t_p)	10 – 20 sec
Ramp down rate	6 °C / sec
Time from 25 °C to peak temperature	8 minutes max.

9 Product approvals

This series of modules has been designed to meet national regulations for world wide use. Different versions of modules belonging to the same series are orderable as it is specified in the [Section 10](#). They differ in terms of integrated memory size and protocol stack enabled to run while sharing the same manufacturing , design and radios capabilities. As representative of the series from the RF design and radios capabilities, the versions using 128 kB Flash/8kB RAM and Zigbee PRO Protocol stack (i.e. SPZB32W1A1.1 and SPZB32W1C1.1) have been used during the certification tests. The following certifications have been obtained.

9.1 FCC approvals

The SPZB32W1A1.1 device, with integrated antenna, as well as the SPZB32W1C1.1, with the antenna specified in [Table 8](#), have been tested and found to comply with the limits for a Class B digital device , pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected

Consult the dealer or an experienced radio/TV technician for help

Module type: ZigBee® module *SPZB32W1A1.1 / SPZB32W1C1.1*

FCC-ID: S9NZB32C1

Modular type: single modular

Table 8. Antenna used for FCC approvals

ITEM	Part N°	Manufacturer
1	2010B4844-01 (Titanis Antenna)	Antenova

Any changes or modifications not expressed approved by the part responsible for compliance could cause the module to cease to comply with FCC rules part 15, and thus void the user's authority to operate the equipment.

While the applicant for a device into which the SPZB32W1A1.1 or the SPZB32W1C2.1 with the antenna specified in [Table 8](#) installed is not required to obtain new authorization for the module, this does not preclude the possibility that some other form of authorization or testing may be required for the end product.

9.1.1 FCC labeling requirements

When integrating the *SPZB32W1A1.1* / *SPZB32W1C1.1* into the final product, it must be ensured that the FCC labelling requirements, as specified below, are satisfied.

Based on the Public Notice from FCC, the product into which our transmitter module is installed must display a label referring to the enclosed module.

The label should use wording such as “Contains Transmitter module FCC ID: S9NZB32C1” or “Contains FCC ID: S9NZB32C1”, any similar wording that expressed the same meaning may be used.

An example is:

Contains FCC ID: S9NZB32C1

9.2 European certification

SPZB32W1A1.1 and SPZB32W1C2.1 devices are CE certified:

CE 0051

Expert opinion N. xxx-xxxxxx released by IMQ refers to the following normative:

Radio: EN300 328: V1.7.1:2006-10

EMC: EN301 489 17 V2.1.1:2009

Safety: EN60950-1:2006 + A11:2009

10 Ordering information scheme

Table 9. Ordering information scheme

	SPZB	32Wx	y	1	.z
802.15.4 / ZigBee modules					
Memory options:					
x --> 1: 128 kB Flash; 8 kB RAM					
x --> 2: 256 kB Flash; 16 kB RAM					
Antenna options:					
y --> A: Integrated ceramic antenna					
y --> C: Integrated UFL connector					
1: Long TX range					
Firmware options:					
z --> 1: ZigBee PRO (EmberZnet)					
z --> 2: STM ZigBee					
z --> 3: RF4CE					
z --> 4: SimpleMAC					
z --> 5: Zigbee IP					

Note: Check availability of the different versions with your ST sales representative.

11 Revision history

Table 10. Document revision history

Date	Revision	Changes
28-Jul-2011	1	Initial release

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