

The Equipment Under Test (EUT) is a Speed Sensor which is mounted on a baseball bat and used to measure swing speed and swing radius. The EUT can operate while connected and controlled by an IOS device (Apple iphone) via Bluetooth radio link. The EUT can only support Bluetooth 4.0 BLE. The Bluetooth portion occupies frequency range of 2402MHz to 2480MHz (40 channels with channel spacing of 2MHz). The EUT is powered by a CR2032 3.0V Lithium battery.

The main components are described below:

1. U1 (CC2541) is a System-On-Chip (SOC) solution incorporating with Bluetooth 4.0 BLE Compliant radio, 8051 MCU, 8k RAM, CODEC and other I/O peripherals.
2. B241 (LFB182G45BG2D280) is the balance matching band-pass filter for the 2.4GHz ISM band.
3. C242 and L243 are components of the antenna matching network.
4. X1 (32MHz crystal) provides system clock for U1 (CC2541).
5. X2 (32.768kHz crystal) provides a slow clock for reducing operating energy.
6. U3 and U4 (ADXL377) are accelerometers for sensing motions.
7. BC1 is CR2032 3.0V Lithium battery.
8. U2 (TPS62730) is DC/DC converter provides 3.3V regulated power supply.
9. J2 is 2 character LCD display.
10. S1 is ON/OFF button.
11. D1 is green LED indicator.

Bluetooth Portion

Modulation Type: GFSK

Antenna Type: Internal, Internal (PCB Trace)

Frequency Range: 2402MHz to 2480MHz, 2MHz channel spacing, 40 channels

Antenna Gain: 0dBi

Normal rated field strength: 91.8dB μ V/m @ 3m

Maximum allowed field strength of production tolerance: +/-4dB

CC2541 Bluetooth 4.0 BLE Channel Table

Channel	Frequency (MHz)
1	2402
2	2404
3	2406
4	2408
5	2410
6	2412
7	2414
8	2416
9	2418
10	2420
11	2422
12	2424
13	2426
14	2428
15	2430
16	2432
17	2434
18	2436
19	2438
20	2440
21	2442
22	2444
23	2446
24	2448
25	2450
26	2452
27	2454
28	2456
29	2458
30	2460
31	2462
32	2464
33	2466
34	2468
35	2470
36	2472
37	2474
38	2476
39	2478
40	2480

2.4-GHz *Bluetooth*™ low energy and Proprietary System-on-Chip

Check for Samples: [CC2541](#)

FEATURES

- **RF**
 - 2.4-GHz *Bluetooth* low energy Compliant and Proprietary RF System-on-Chip
 - Supports 250-kbps, 500-kbps, 1-Mbps, 2-Mbps Data Rates
 - Excellent Link Budget, Enabling Long-Range Applications Without External Front End
 - Programmable Output Power up to 0 dBm
 - Excellent Receiver Sensitivity (–94 dBm at 1 Mbps), Selectivity, and Blocking Performance
 - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- **Layout**
 - Few External Components
 - Reference Design Provided
 - 6-mm × 6-mm QFN-40 Package
 - Pin-Compatible With CC2540 (When Not Using USB or I²C)
- **Low Power**
 - Active-Mode RX Down to: 17.9 mA
 - Active-Mode TX (0 dBm): 18.2 mA
 - Power Mode 1 (4-μs Wake-Up): 270 μA
 - Power Mode 2 (Sleep Timer On): 1 μA
 - Power Mode 3 (External Interrupts): 0.5 μA
 - Wide Supply-Voltage Range (2 V–3.6 V)
- **TPS62730 Compatible Low Power in Active Mode**
 - RX Down to: 14.7 mA (3-V supply)
 - TX (0 dBm): 14.3 mA (3-V supply)
- **High-Performance and Low-Power 8051 Microcontroller Core With Code Prefetch**
- **In-System-Programmable Flash, 128- or 256-KB**
- **8-KB RAM With Retention in All Power Modes**
- **Hardware Debug Support**
- **Extensive Baseband Automation, Including Auto-Acknowledgment and Address Decoding**
- **Retention of All Relevant Registers in All Power Modes**
- **Peripherals**
 - Powerful Five-Channel DMA
 - General-Purpose Timers (One 16-Bit, Two 8-Bit)
 - IR Generation Circuitry
 - 32-kHz Sleep Timer With Capture
 - Accurate Digital RSSI Support
 - Battery Monitor and Temperature Sensor
 - 12-Bit ADC With Eight Channels and Configurable Resolution
 - AES Security Coprocessor
 - Two Powerful USARTs With Support for Several Serial Protocols
 - 23 General-Purpose I/O Pins (21 × 4 mA, 2 × 20 mA)
 - I²C interface
 - 2 I/O Pins Have LED Driving Capabilities
 - Watchdog Timer
 - Integrated High-Performance Comparator
- **Development Tools**
 - CC2541 Evaluation Module Kit (CC2541EMK)
 - CC2541 Mini Development Kit (CC2541DK-MINI)
 - SmartRF™ Software
 - IAR Embedded Workbench™ Available
- **Microcontroller**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Bluetooth is a trademark of Bluetooth SIG, Inc..

ZigBee is a registered trademark of ZigBee Alliance.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012–2013, Texas Instruments Incorporated

SOFTWARE FEATURES

- **Bluetooth v4.0 Compliant Protocol Stack for Single-Mode BLE Solution**
 - Complete Power-Optimized Stack, Including Controller and Host
 - GAP – Central, Peripheral, Observer, or Broadcaster (Including Combination Roles)
 - ATT / GATT – Client and Server
 - SMP – AES-128 Encryption and Decryption
 - L2CAP
 - Sample Applications and Profiles
 - Generic Applications for GAP Central and Peripheral Roles
 - Proximity, Accelerometer, Simple Keys, and Battery GATT Services
 - More Applications Supported in [BLE Software Stack](#)
 - Multiple Configuration Options
 - Single-Chip Configuration, Allowing Applications to Run on CC2541
 - Network Processor Interface for Applications Running on an External Microcontroller
 - BTool – Windows PC Application for Evaluation, Development, and Test

APPLICATIONS

- 2.4-GHz *Bluetooth* low energy Systems
- Proprietary 2.4-GHz Systems
- Human-Interface Devices (Keyboard, Mouse, Remote Control)
- Sports and Leisure Equipment
- Mobile Phone Accessories
- Consumer Electronics

CC2541 WITH TPS62730

- **TPS62730** is a 2-MHz Step-Down Converter With Bypass Mode
- Extends Battery Lifetime by up to 20%
- Reduced Current in All Active Modes
- 30-nA Bypass Mode Current to Support Low-Power Modes
- RF Performance Unchanged
- Small Package Allows for Small Solution Size
- CC2541 Controllable

DESCRIPTION

The CC2541 is a power-optimized true system-on-chip (SoC) solution for both *Bluetooth* low energy and proprietary 2.4-GHz applications. It enables robust network nodes to be built with low total bill-of-material costs. The CC2541 combines the excellent performance of a leading RF transceiver with an industry-standard enhanced 8051 MCU, in-system programmable flash memory, 64KB RAM, and many other powerful supporting features and peripherals. The CC2541 is highly suited for systems where ultralow power consumption is required. This is specified by various operating modes. Short transition times between operating modes further enable low power consumption.

The CC2541 is pin-compatible with the CC2540 in the 4mm × 4mm QFN package, if the USB is not used on the CC2540 and the I²C extra I/O is not used on the CC2541. Compared to the CC2540, the CC2541 provides lower RF current consumption. The CC2541 does not have the USB interface of the CC2540, and provides lower maximum output power in TX mode. The CC2541 also adds a 4W I²C interface.

The CC2541 is pin-compatible with the CC2533 RFFE-optimized IEEE 802.15.4 SoC.

The CC2541 comes in two different versions: CC2541-128K256, with 128KB and 256KB of flash memory, respectively.

For the CC2541 block diagram, see [Figure 1](#).



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

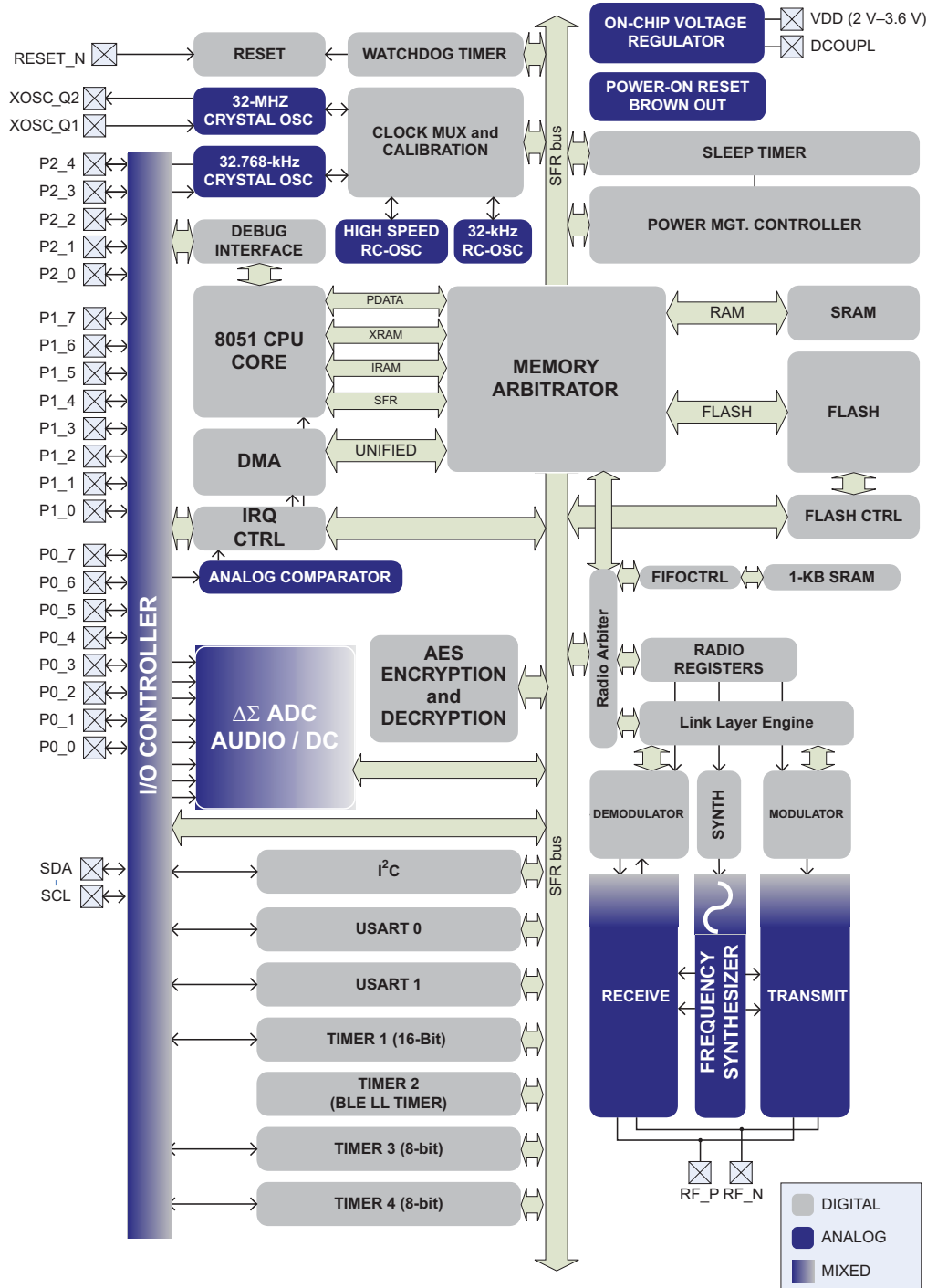


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range unless otherwise noted

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.0	V
Voltage on any digital pin		–0.3	VDD + 0.3 ≤ 3.0	V
Input R _{MS} level			10	dBm
Storage temperature range		–0	120	°C
ESD ⁽²⁾	All pins, excluding pins 20 and 21, according to human-body model, JEDEC STD 22, method A114		2	kV
	All pins, according to human-body model, JEDEC STD 22, method A114		1	kV
	According to charged-device model, JEDEC STD 22, method C101		100	V

⁽¹⁾ Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

⁽²⁾ **CAUTION:** ESD sensitive device. Precautions should be used when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

	MIN	NOM	MAX	UNIT
Operating ambient temperature range, T _A	–0		0	°C
Operating supply voltage	2		3.0	V

ELECTRICAL CHARACTERISTICSmeasured on Texas Instruments CC2541 E reference design with T_A = 25°C and VDD = 3 V,**1 Mbps, GFSK, 250-kHz deviation, Bluetooth low energy mode, and 0.1% BER**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{core} Core current consumption	R mode, standard mode, no peripherals active, low CPU activity		10		mA
	R mode, high-gain mode, no peripherals active, low CPU activity		20.2		
	T mode, –20 dBm output power, no peripherals active, low CPU activity		10		
	T mode, 0 dBm output power, no peripherals active, low CPU activity		12		
	Power mode 1. Digital regulator on, 32.768 kHz RCOSC and 32.768 kHz crystal oscillator off, 32.768 kHz OSC, POR, BOD and sleep timer active, RA and register retention		20		µA
	Power mode 2. Digital regulator off, 32.768 kHz RCOSC and 32.768 kHz crystal oscillator off, 32.768 kHz OSC, POR, and sleep timer active, RA and register retention		1		
	Power mode 3. Digital regulator off, no clocks, POR active, RA and register retention		0.0		
	Low CPU activity, 32.768 kHz OSC running. No radio or peripherals. Limited flash access, no RA access.		0.0		mA
I _{peri} Peripheral current consumption Adds to core current I _{core} for each peripheral unit activated	Timer 1. Timer running, 32.768 kHz OSC used		0		µA
	Timer 2. Timer running, 32.768 kHz OSC used		0		
	Timer 3. Timer running, 32.768 kHz OSC used		0		
	Timer 4. Timer running, 32.768 kHz OSC used		0		
	Sleep timer, including 32.768 kHz RCOSC		0.0		
	ADC, when converting		1.2		mA

GENERAL CHARACTERISTICS

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 1000 RCOSC and 32000 crystal oscillator off. Start-up of 1000 RCOSC		0		μs
Power mode 2 or 3 → Active	Digital regulator off, 1000 RCOSC and 32000 crystal oscillator off. Start-up of regulator and 1000 RCOSC		120		μs
Active → Toff or Roff	Crystal ESR ≤ 1 Ω. Initially running on 1000 RCOSC, with 32000 OSC On		100		μs
	With 32000 OSC initially on		10		μs
Roff turnaround	Proprietary auto mode		130		μs
	B/E mode		10		
RADIO PART					
Rf frequency range	Programmable in 1000 steps	2300		2000	000
Data rate and modulation format	20 kbps, GFSK, 100 kHz deviation 20 kbps, GFSK, 320 kHz deviation 10 kbps, GFSK, 200 kHz deviation 10 kbps, GFSK, 100 kHz deviation 100 kbps, SFSK 200 kbps, GFSK, 100 kHz deviation 200 kbps, SFSK				

RF RECEIVE SECTION

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, $f_c = 2400\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Receiver sensitivity			-90		dBm
Saturation	BER $\leq 0.1\%$		-1		dBm
Co-channel rejection	Wanted signal at -90 dBm		-9		dB
In-band blocking rejection	2000 offset, 0.1% BER, wanted signal -90 dBm		-2		dB
	10000 offset, 0.1% BER, wanted signal -90 dBm		30		
	10000 or greater offset, 0.1% BER, wanted signal -90 dBm		1		
Frequency error tolerance ¹	Including both initial tolerance and drift. Sensitivity better than -90 dBm, 200 byte payload. BER 0.1%	-300		300	kHz
Symbol rate error tolerance ²	Maximum packet length. Sensitivity better than -90 dBm, 200 byte payload. BER 0.1%	-120		120	ppm
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER					
Receiver sensitivity			-90		dBm
Saturation	BER $\leq 0.1\%$		-9		dBm
Co-channel rejection	Wanted signal at -90 dBm		-12		dB
In-band blocking rejection	2000 offset, 0.1% BER, wanted signal -90 dBm		-1		dB
	10000 offset, 0.1% BER, wanted signal -90 dBm		30		
	10000 or greater offset, 0.1% BER, wanted signal -90 dBm		30		
Frequency error tolerance ¹	Including both initial tolerance and drift. Sensitivity better than -90 dBm, 200 byte payload. BER 0.1%	-300		300	kHz
Symbol rate error tolerance ²	Maximum packet length. Sensitivity better than -90 dBm, 200 byte payload. BER 0.1%	-120		120	ppm

¹ Difference between center frequency of the received RF signal and local oscillator frequency

² Difference between incoming symbol rate and the internally generated symbol rate

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$, $f_c = 2400\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps, GFSK, 250-kHz Deviation, Bluetooth low energy Mode, 0.1% BER					
Receiver sensitivity ⁽³⁾	High gain mode		-88		dBm
	Standard mode		-88		
Saturation ⁽¹⁾	BER = 0.1%		0		dBm
Co-channel rejection ⁽¹⁾	Wanted signal -88 dBm		-88		dB
In-band blocking rejection ⁽¹⁾	1 MHz offset, 0.1% BER, wanted signal -88 dBm		-2		dB
	2 MHz offset, 0.1% BER, wanted signal -88 dBm		20		
	3 MHz offset, 0.1% BER, wanted signal -88 dBm		30		
	4 MHz offset, 0.1% BER, wanted signal -88 dBm		33		
Out-of-band blocking rejection ⁽¹⁾	Minimum interferer level = 2 GHz, Wanted signal -88 dBm		-21		dBm
	Minimum interferer level = 2 GHz, 3 GHz, Wanted signal -88 dBm		-20		
	Minimum interferer level = 3 GHz, Wanted signal -88 dBm		-88		
Intermodulation ⁽¹⁾	Minimum interferer level		-30		dBm
Frequency error tolerance ⁽¹⁾	Including both initial tolerance and drift. Sensitivity better than -88 dBm, 200 byte payload. BER 0.1%	-200		200	kHz
Symbol rate error tolerance ⁽¹⁾	Maximum packet length. Sensitivity better than -88 dBm, 200 byte payload. BER 0.1%	-88		0	ppm
1 Mbps, GFSK, 160-kHz Deviation, 0.1% BER					
Receiver sensitivity ⁽¹⁾			-81		dBm
Saturation	BER = 0.1%		0		dBm
Co-channel rejection	Wanted signal 10 dB above sensitivity level		-88		dB
In-band blocking rejection	1 MHz offset, 0.1% BER, wanted signal -88 dBm		2		dB
	2 MHz offset, 0.1% BER, wanted signal -88 dBm		20		
	3 MHz offset, 0.1% BER, wanted signal -88 dBm		20		
	4 MHz offset, 0.1% BER, wanted signal -88 dBm		32		
Frequency error tolerance ⁽¹⁾	Including both initial tolerance and drift. Sensitivity better than -88 dBm, 200 byte payload. BER 0.1%	-200		200	kHz
Symbol rate error tolerance ⁽¹⁾	Maximum packet length. Sensitivity better than -88 dBm, 200 byte payload. BER 0.1%	-88		0	ppm
500 kbps, MSK, 0.1% BER					
Receiver sensitivity ⁽¹⁾			-88		dBm
Saturation	BER = 0.1%		0		dBm
Co-channel rejection	Wanted signal -88 dBm		-88		dB
In-band blocking rejection	1 MHz offset, 0.1% BER, wanted signal -88 dBm		20		dB
	2 MHz offset, 0.1% BER, wanted signal -88 dBm		20		
	2 MHz offset, 0.1% BER, wanted signal -88 dBm		20		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than -88 dBm, 200 byte payload. BER 0.1%	-100		100	kHz
Symbol rate error tolerance	Maximum packet length. Sensitivity better than -88 dBm, 200 byte payload. BER 0.1%	-88		0	ppm

(3) The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.

(1) Results based on standard gain mode.

(2) Difference between center frequency of the received RF signal and local oscillator frequency

(3) Difference between incoming symbol rate and the internally generated symbol rate

(4) Results based on high gain mode.

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2541 E reference design with T_A 25°C, VDD 3 V, f_c 2400 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
250 kbps, GFSK, 160 kHz Deviation, 0.1% BER					
Receiver sensitivity			–80		dBm
Saturation	BER 0.1%		0		dBm
Co-channel rejection	Wanted signal 0 dBm		–3		dB
In-band blocking rejection	100 MHz offset, 0.1% BER, wanted signal –80 dBm		23		dB
	200 MHz offset, 0.1% BER, wanted signal –80 dBm		20		
	250 MHz offset, 0.1% BER, wanted signal –80 dBm		20		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than –80 dBm, 200-byte payload. BER 0.1%	–100		100	kHz
Symbol rate error tolerance ¹⁰	Maximum packet length. Sensitivity better than –80 dBm, 200-byte payload. BER 0.1%	–0		0	ppm
250 kbps, MSK, 0.1% BER					
Receiver sensitivity ¹¹			–80		dBm
Saturation	BER 0.1%		0		dBm
Co-channel rejection	Wanted signal 0 dBm		–0		dB
In-band blocking rejection	100 MHz offset, 0.1% BER, wanted signal –80 dBm		20		dB
	200 MHz offset, 0.1% BER, wanted signal –80 dBm		20		
	250 MHz offset, 0.1% BER, wanted signal –80 dBm		30		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than –80 dBm, 200-byte payload. BER 0.1%	–100		100	kHz
Symbol rate error tolerance	Maximum packet length. Sensitivity better than –80 dBm, 200-byte payload. BER 0.1%	–0		0	ppm
ALL RATES/FORMATS					
Spurious emission in R ₁ . Conducted measurement	f 1 GHz		–80		dBm
Spurious emission in R ₂ . Conducted measurement	f 1 GHz		–80		dBm

Results based on standard gain mode.

Difference between center frequency of the received RF signal and local oscillator frequency

10 Difference between incoming symbol rate and the internally generated symbol rate

11 Results based on high gain mode.

RF TRANSMIT SECTION

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2400\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended $50\text{-}\Omega$ load through a balun using maximum recommended output power setting		0		dBm
	Delivered to a single-ended $50\text{-}\Omega$ load through a balun using minimum recommended output power setting		-23		
Programmable output power range	Delivered to a single-ended $50\text{-}\Omega$ load through a balun using minimum recommended output power setting		23		dB
Spurious emission conducted measurement	$f = 1\text{ GHz}$		-2		dBm
	$f = 1\text{ GHz}$		-		dBm
	Suitable for systems targeting compliance with worldwide radio frequency regulations ETSI EN 300 320 and EN 300 340 Class 2 (Europe), FCC CFR Part 15 (US), and ARIB STD-T10 (Japan)				
Optimum load impedance	Differential impedance as seen from the R _{port} (R _{DP} and R _{DN}) toward the antenna		30	30	Ω

Designs with antenna connectors that require conducted ETSI compliance at 1 GHz should insert an LC resonator in front of the antenna connector. Use a 1-nH inductor in parallel with a 1-pF capacitor. Connect both from the signal trace to a good RF ground.

CURRENT CONSUMPTION WITH TPS62730

Measured on Texas Instruments CC2541 TPA230 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2400\text{ MHz}$, 1 Mbps, GFSK, 250-kHz deviation, Bluetooth™ low energy Mode, 1% BER⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption	R _{port} mode, standard mode, no peripherals active, low CPU activity, CPU at 1 MHz		1		mA
	R _{port} mode, high-gain mode, no peripherals active, low CPU activity, CPU at 1 MHz		1		
	T _{port} mode, -20 dBm output power, no peripherals active, low CPU activity, CPU at 1 MHz		13.1		
	T _{port} mode, 0 dBm output power, no peripherals active, low CPU activity, CPU at 1 MHz		1	3	

(1) 0.1% BER maps to 30.0% PER

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32		MHz
Crystal frequency accuracy requirement ⁽¹⁾		-0		0	ppm
ESR Equivalent series resistance				0	Ω
C ₀ Crystal shunt capacitance		1			pF
C _L Crystal load capacitance		10		1	pF
Startup time			0.2		ms
Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by (1)

32.768-kHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal frequency			32.768		kHz
Crystal frequency accuracy requirement ¹		-10		10	ppm
ESR Equivalent series resistance			10	130	k Ω
C_0 Crystal shunt capacitance			0.5	2	pF
C_L Crystal load capacitance			12	15	pF
Startup time			0.5		s

¹ Including aging and temperature dependency, as specified by [1]

32-kHz RC OSCILLATOR

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated frequency ¹			32.768		kHz
Frequency accuracy after calibration			0.2		ppm
Temperature coefficient ²			0.1		ppm/ $^\circ\text{C}$
Supply voltage coefficient ³			3		ppm/V
Calibration time ⁴			2		ms

¹ The calibrated 32.768-kHz RC oscillator frequency is the 32.768-kHz TA frequency divided by [1].

² Frequency drift when temperature changes after calibration

³ Frequency drift when supply voltage changes after calibration

⁴ When the 32.768-kHz RC oscillator is enabled, it is calibrated when a switch from the 1-MHz RC oscillator to the 32.768-kHz crystal oscillator is performed while SLEEP_CTRL.OSC32kHzCALDIS is set to 0.

16-MHz RC OSCILLATOR

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency ¹			16		MHz
Uncalibrated frequency accuracy			1		ppm
Calibrated frequency accuracy			0.1		ppm
Startup time			10		μs
Initial calibration time ²			10		μs

¹ The calibrated 16-MHz RC oscillator frequency is the 32.768-kHz TA frequency divided by 2.

² When the 1-MHz RC oscillator is enabled, it is calibrated when a switch from the 1-MHz RC oscillator to the 32.768-kHz crystal oscillator is performed while SLEEP_CTRL.OSC16kHzCALDIS is set to 0.

RSSI CHARACTERISTICS

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Useful RSSI range ¹	Reduced gain by AGC algorithm		0		dB
	High gain by AGC algorithm		0		
RSSI offset ¹	Reduced gain by AGC algorithm		0		dBm
	High gain by AGC algorithm		0		
Absolute uncalibrated accuracy ¹			0		dB
Step size LSB value			1		dB
All Other Rates/Formats					
Useful RSSI range ¹	Standard mode		0		dB
	High gain mode		0		
RSSI offset ¹	Standard mode		0		dBm
	High gain mode		10		
Absolute uncalibrated accuracy ¹			3		dB
Step size LSB value			1		dB

¹ Assuming CC2541 E reference design. Other R designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2400\text{ MHz}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At 100 kHz offset from carrier		-10		dBc/Hz
	At 3 MHz offset from carrier		-112		
	At 10 MHz offset from carrier		-11		

ANALOG TEMPERATURE SENSOR

Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output	Measured using integrated ADC, internal bandgap voltage reference, and maximum resolution		1000		12-bit
Temperature coefficient			0		1°C
Voltage coefficient			1		0.1 V
Initial accuracy without calibration			10		°C
Accuracy using 1-point calibration			0		°C
Current consumption when enabled			0		mA

COMPARATOR CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$. All measurement results are obtained using the CC2541 reference designs, post-calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common-mode maximum voltage			V_{DD}		V
Common-mode minimum voltage		-0.3			
Input offset voltage			1		mV
Offset vs temperature			1		µV/°C
Offset vs operating voltage			0		mV/V
Supply current			230		nA
Offset hysteresis			0.1		mV

ADC CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ and $V_{DD} = 3\text{ V}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	VDD is voltage on AVDD pin	0		VDD	V
External reference voltage	VDD is voltage on AVDD pin	0		VDD	V
External reference voltage differential	VDD is voltage on AVDD pin	0		VDD	V
Input resistance, signal	Simulated using 100 MHz clock speed		100		k Ω
Full-scale signal ⁽¹⁾	Peak-to-peak, defines 0 dBFS		2.00		V
ENOB ⁽¹⁾ Effective number of bits	Single-ended input, 8-bit setting		8.0		bits
	Single-ended input, 10-bit setting		10.3		
	Single-ended input, 12-bit setting		12.0		
	Differential input, 8-bit setting		8.0		
	Differential input, 10-bit setting		10.0		
	Differential input, 12-bit setting		12.0		
	10-bit setting, clocked by RCOSC		10.0		
	12-bit setting, clocked by RCOSC		12.0		
	Useful power bandwidth		0–20		
	12-bit setting, both single and differential		0–20		
THD Total harmonic distortion	Single ended input, 12-bit setting, –0 dBFS ⁽¹⁾		–0.2		dB
	Differential input, 12-bit setting, –0 dBFS ⁽¹⁾		–0.3		
Signal to nonharmonic ratio	Single-ended input, 12-bit setting ⁽¹⁾		0.2		dB
	Differential input, 12-bit setting ⁽¹⁾		0.3		
	Single-ended input, 12-bit setting, –0 dBFS ⁽¹⁾		0.1		
	Differential input, 12-bit setting, –0 dBFS ⁽¹⁾		0.1		
CMRR Common-mode rejection ratio	Differential input, 12-bit setting, 1 kHz sine –0 dBFS, limited by ADC resolution		0.0		dB
Crosstalk	Single ended input, 12-bit setting, 1 kHz sine –0 dBFS, limited by ADC resolution		0.0		dB
Offset	Mid-scale		–3		mV
Gain error			0.00		
DNL Differential nonlinearity	12-bit setting, mean ⁽¹⁾		0.0		LSB
	12-bit setting, maximum ⁽¹⁾		0.1		
INL Integral nonlinearity	12-bit setting, mean ⁽¹⁾		0.0		LSB
	12-bit setting, maximum ⁽¹⁾		13.3		
	12-bit setting, mean, clocked by RCOSC		10		
	12-bit setting, max, clocked by RCOSC		2.0		
SINAD ⁽¹⁾ SNR ⁽¹⁾ Signal to noise and distortion	Single ended input, 8-bit setting ⁽¹⁾		3.0		dB
	Single ended input, 10-bit setting ⁽¹⁾		10.0		
	Single ended input, 12-bit setting ⁽¹⁾		12.0		
	Differential input, 8-bit setting ⁽¹⁾		0.0		
	Differential input, 10-bit setting ⁽¹⁾		1.0		
	Differential input, 12-bit setting ⁽¹⁾		1.0		
	Differential input, 12-bit setting ⁽¹⁾		0.0		
	Differential input, 12-bit setting ⁽¹⁾		0.0		
Conversion time	8-bit setting		20		μs
	10-bit setting		3.0		
	12-bit setting		132		
	12-bit setting		132		

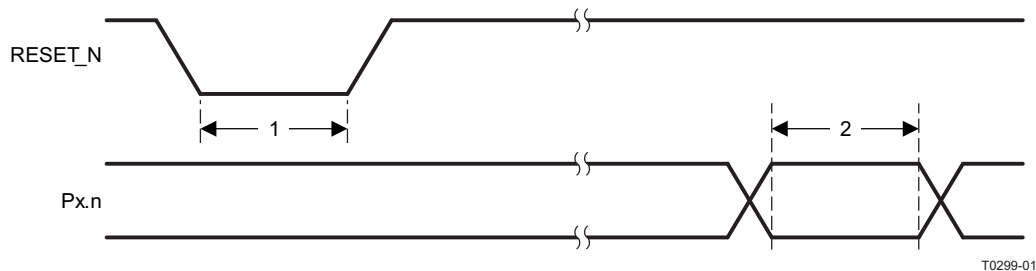
⁽¹⁾ Measured with 300 kHz sine-wave input and VDD as reference.

ADC CHARACTERISTICS (continued)T_A □ 2□□C and VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power consumption			1.2		mA
Internal reference VDD coefficient			□		mV/V
Internal reference temperature coefficient			0.□		mV/10□C
Internal reference voltage			1.2□		V

CONTROL INPUT AC CHARACTERISTICST_A □ –□0□C to □□□C, VDD □ 2 V to 3.□ V

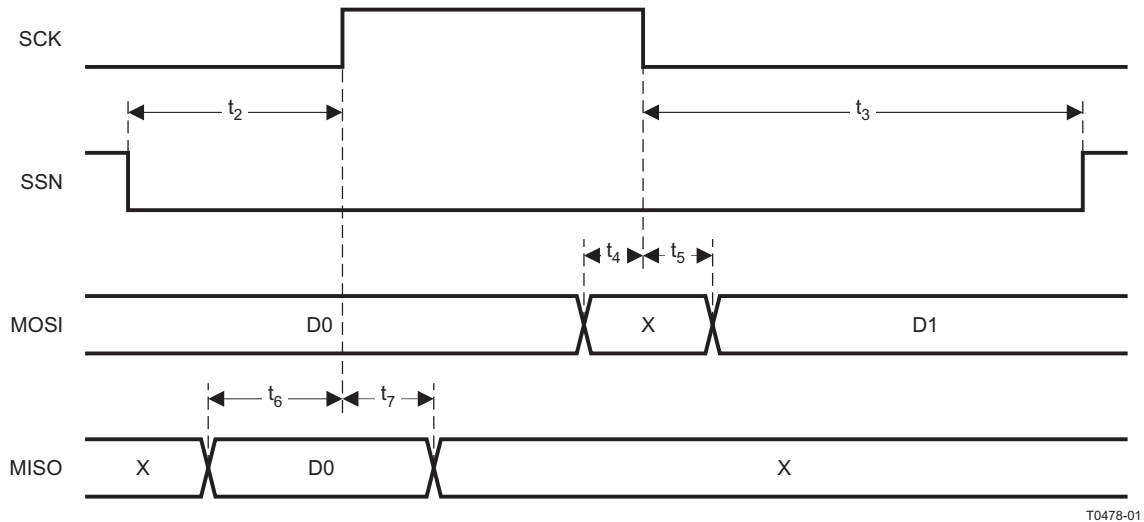
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f _{sysc} □ t _{sysc} □ □ 1□f _{sysc} □	The undivided system clock is 32 □□□ when crystal oscillator is used. The undivided system clock is 1□□□□ when calibrated 1□□□□ RC oscillator is used.	1□		32	□□□
RESET□N low duration	See item 1, Figure 2 . This is the shortest pulse that is recognized as a complete reset pin re□uest. Note that shorter pulses may be recognized but do not lead to complete reset of all modules within the chip.	1			□s
Interrupt pulse duration	See item 2, Figure 2 . This is the shortest pulse that is recognized as an interrupt re□uest.	20			ns

**Figure 2. Control Input AC Characteristics**

SPI AC CHARACTERISTICS

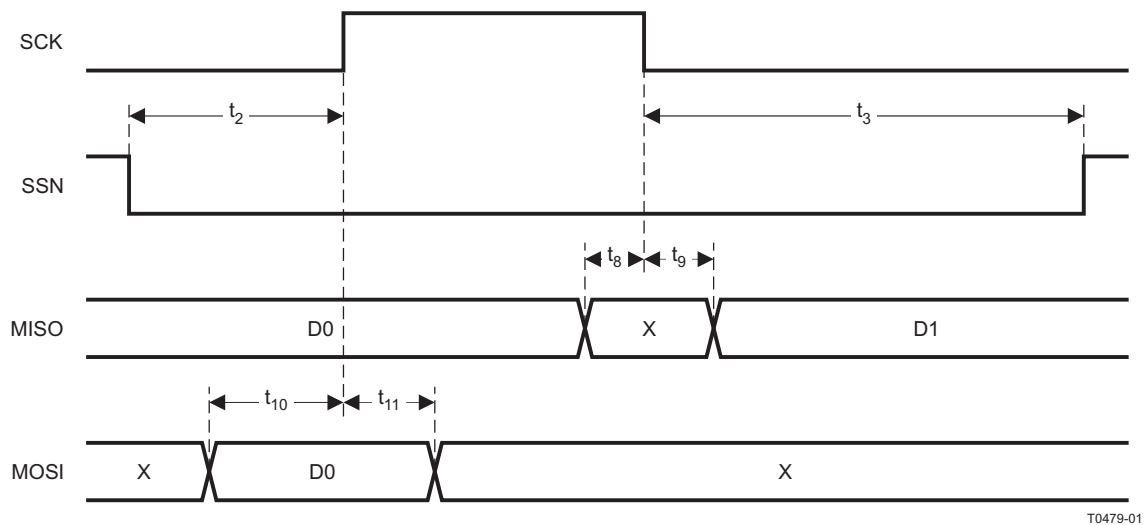
T_A = –40°C to 100°C, VDD = 2 V to 3.0 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t ₁ SC _Q period	Master, R _Q and T _Q	20			ns
	Slave, R _Q and T _Q	20			
SC _Q duty cycle	Master		50		
t ₂ SSN low to SC _Q	Master	3			ns
	Slave	3			
t ₃ SC _Q to SSN high	Master	3			ns
	Slave	3			
t ₄ Q _{OSI} early out	Master, load = 10 pF				ns
t ₅ Q _{OSI} late out	Master, load = 10 pF			10	ns
t ₆ Q _{ISO} setup	Master	0			ns
t ₇ Q _{ISO} hold	Master	10			ns
SC _Q duty cycle	Slave		50		ns
t ₁₀ Q _{OSI} setup	Slave	3			ns
t ₁₁ Q _{OSI} hold	Slave	10			ns
t ₁₂ Q _{ISO} late out	Slave, load = 10 pF				ns
Operating frequency	Master, T _Q only				MHz
	Master, R _Q and T _Q				
	Slave, R _Q only				
	Slave, R _Q and T _Q				



T0478-01

Figure 3. SPI Master AC Characteristics



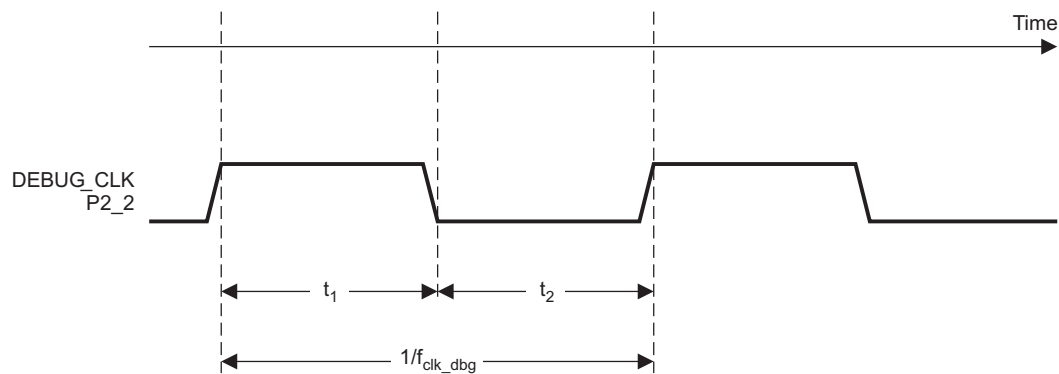
T0479-01

Figure 4. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

T_A = -40°C to 100°C, V_{DD} = 2 V to 3.0 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock frequency (see Figure 1)				12	kHz
t_1	Allowed high pulse on clock (see Figure 1)		3			ns
t_2	Allowed low pulse on clock (see Figure 1)		3			ns
t_3	EMT_RESETN low to first falling edge on debug clock (see Figure 1)		1			ns
t_4	Falling edge on clock to EMT_RESETN high (see Figure 1)		3			ns
t_5	EMT_RESETN high to first debug command (see Figure 1)		3			ns
t_6	Debug data setup (see Figure 1)		2			ns
t_7	Debug data hold (see Figure 1)					ns
t_8	Clock-to-data delay (see Figure 1)	Load = 10 pF			30	ns



T0436-01

Figure 5. Debug Clock – Basic Timing

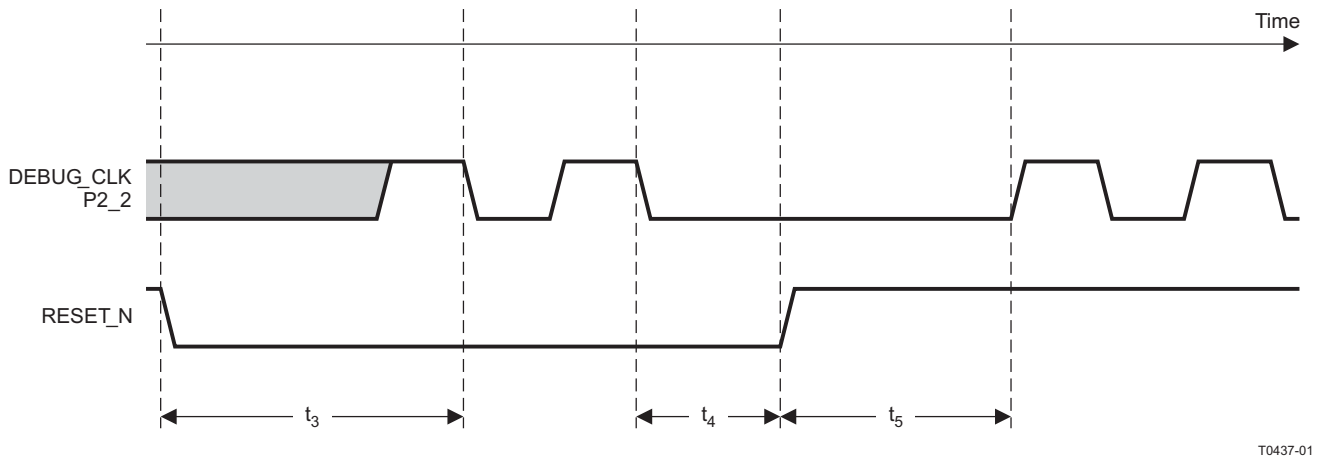


Figure 6. Debug Enable Timing

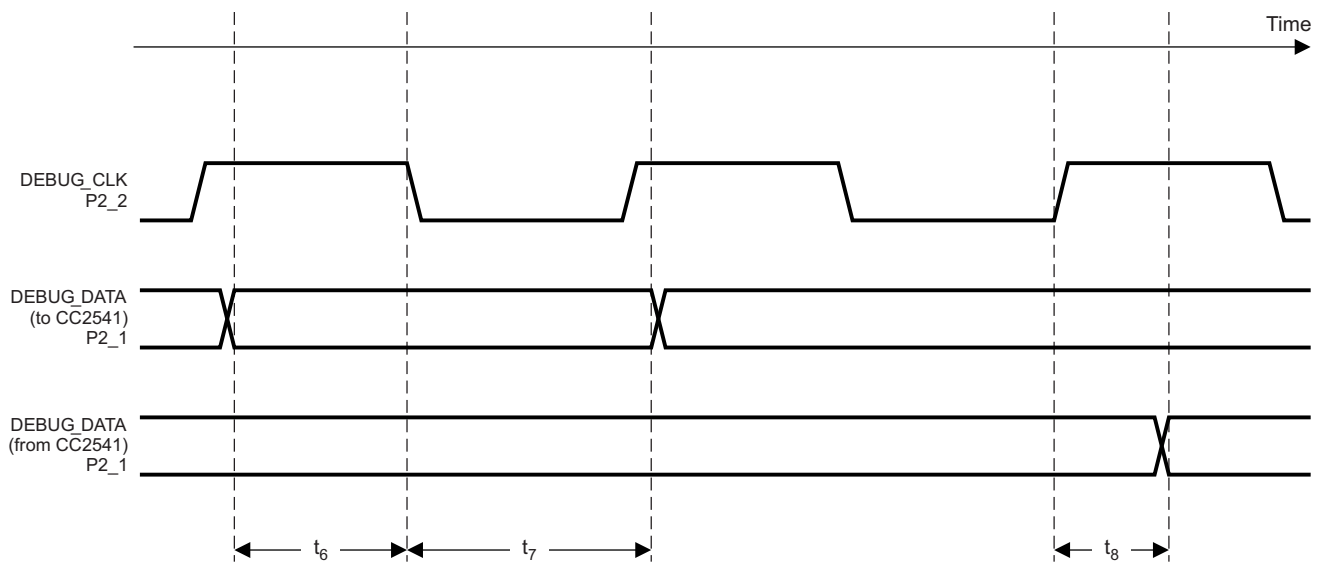


Figure 7. Data Setup and Hold Timing

TIMER INPUTS AC CHARACTERISTICS

T_A = -40°C to 105°C , V_{DD} = 2 V to 3.0 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate at the current system clock rate of 1 MHz or 32 MHz	1.0			t_{sysc}

DC CHARACTERISTICS

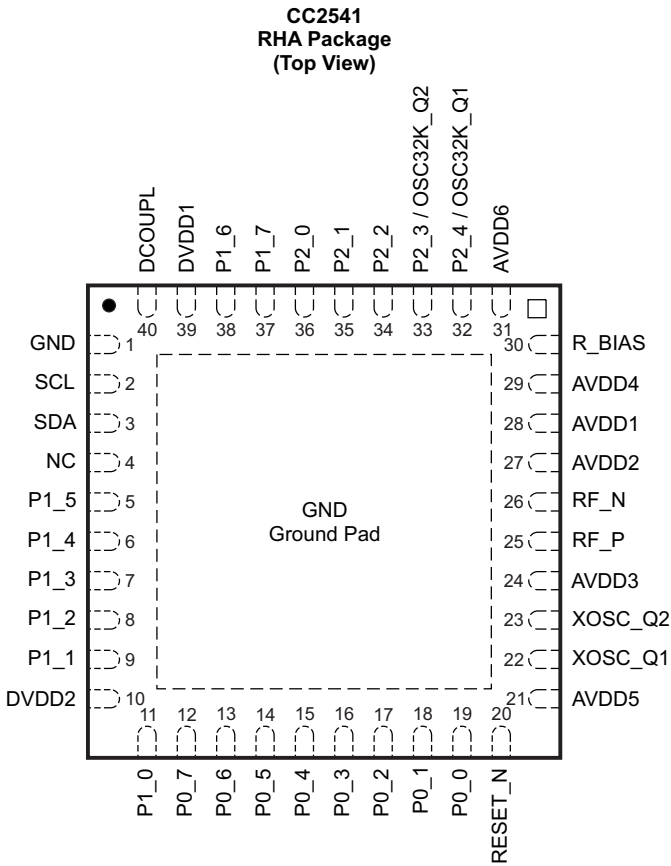
T_A □ 2□□C, VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
□logic:0 input voltage				0.□	V
□logic:1 input voltage		2.□			V
□logic:0 input current	Input e□uals 0 V	–□0		□0	nA
□logic:1 input current	Input e□uals VDD	–□0		□0	nA
I□□pin pullup and pulldown resistors			20		k□
□logic:0 output voltage, □□mA pins	Output load □ mA			0.□	V
□logic:1 output voltage, □□mA pins	Output load □ mA	2.□			V
□logic:0 output voltage, 20□mA pins	Output load 20 mA			0.□	V
□logic:1 output voltage, 20□mA pins	Output load 20 mA	2.□			V

DEVICE INFORMATION

PIN DESCRIPTIONS

The CC2□□1 pinout is shown in □igure □ and a short description of the pins follows.



NOTE□ The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 8. Pinout Top View

PIN DESCRIPTIONS

PIN NAME	PIN	PIN TYPE	DESCRIPTION
AVDD1	2□	Power □analog□	2□V–3.□V analog power□supply connection
AVDD2	2□	Power □analog□	2□V–3.□V analog power□supply connection
AVDD3	2□	Power □analog□	2□V–3.□V analog power□supply connection
AVDD□	2□	Power □analog□	2□V–3.□V analog power□supply connection
AVDD□	21	Power □analog□	2□V–3.□V analog power□supply connection
AVDD□	31	Power □analog□	2□V–3.□V analog power□supply connection
DCOUP□	□0	Power □digital□	1.□V digital power□supply decoupling. Do not use for supplying external circuits.
DVDD1	3□	Power □digital□	2□V–3.□V digital power□supply connection
DVDD2	10	Power □digital□	2□V–3.□V digital power□supply connection
GND	1	Ground pin	Connect to GND
GND	□	Ground	The ground pad must be connected to a solid ground plane.
NC	□	Unused pins	Not connected
P0□0	1□	Digital I/O	Port 0.0
P0□1	1□	Digital I/O	Port 0.1
P0□2	1□	Digital I/O	Port 0.2
P0□3	1□	Digital I/O	Port 0.3
P0□□	1□	Digital I/O	Port 0.□
P0□□	1□	Digital I/O	Port 0.□
P0□□	13	Digital I/O	Port 0.□
P0□□	12	Digital I/O	Port 0.□
P1□0	11	Digital I/O	Port 1.0 – 20□mA drive capability
P1□1	□	Digital I/O	Port 1.1 – 20□mA drive capability
P1□2	□	Digital I/O	Port 1.2
P1□3	□	Digital I/O	Port 1.3
P1□□	□	Digital I/O	Port 1.□
P1□□	□	Digital I/O	Port 1.□
P1□□	3□	Digital I/O	Port 1.□
P1□□	3□	Digital I/O	Port 1.□
P2□0	3□	Digital I/O	Port 2.0
P2□1□DD	3□	Digital I/O	Port 2.1 □debug data
P2□2□DC	3□	Digital I/O	Port 2.2 □debug clock
P2□3□ OSC32□□□2	33	Digital I/O, Analog I/O	Port 2.3□32.□□□ k□□□OSC
P2□□□ OSC32□□□1	32	Digital I/O, Analog I/O	Port 2.□32.□□□ k□□□OSC
RBIAS	30	Analog I/O	External precision bias resistor for reference current
RESET□N	20	Digital input	Reset, active□low
R□□N	2□	R□ I/O	Negative R□ input signal to □NA during R□ Negative R□ output signal from PA during T□
R□□P	2□	R□ I/O	Positive R□ input signal to □NA during R□ Positive R□ output signal from PA during T□
SC□	2	I ² C clock or digital I/O	Can be used as I ² C clock pin or digital I/O. □eave floating if not used. If grounded disable pull up
SDA	3	I ² C clock or digital I/O	Can be used as I ² C data pin or digital I/O. □eave floating if not used. If grounded disable pull up
□OSC□□1	22	Analog I/O	32□□□□crystal oscillator pin 1 or external clock input
□OSC□□2	23	Analog I/O	32□□□□crystal oscillator pin 2

BLOCK DIAGRAM

A block diagram of the CC2541 is shown in Figure 9. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

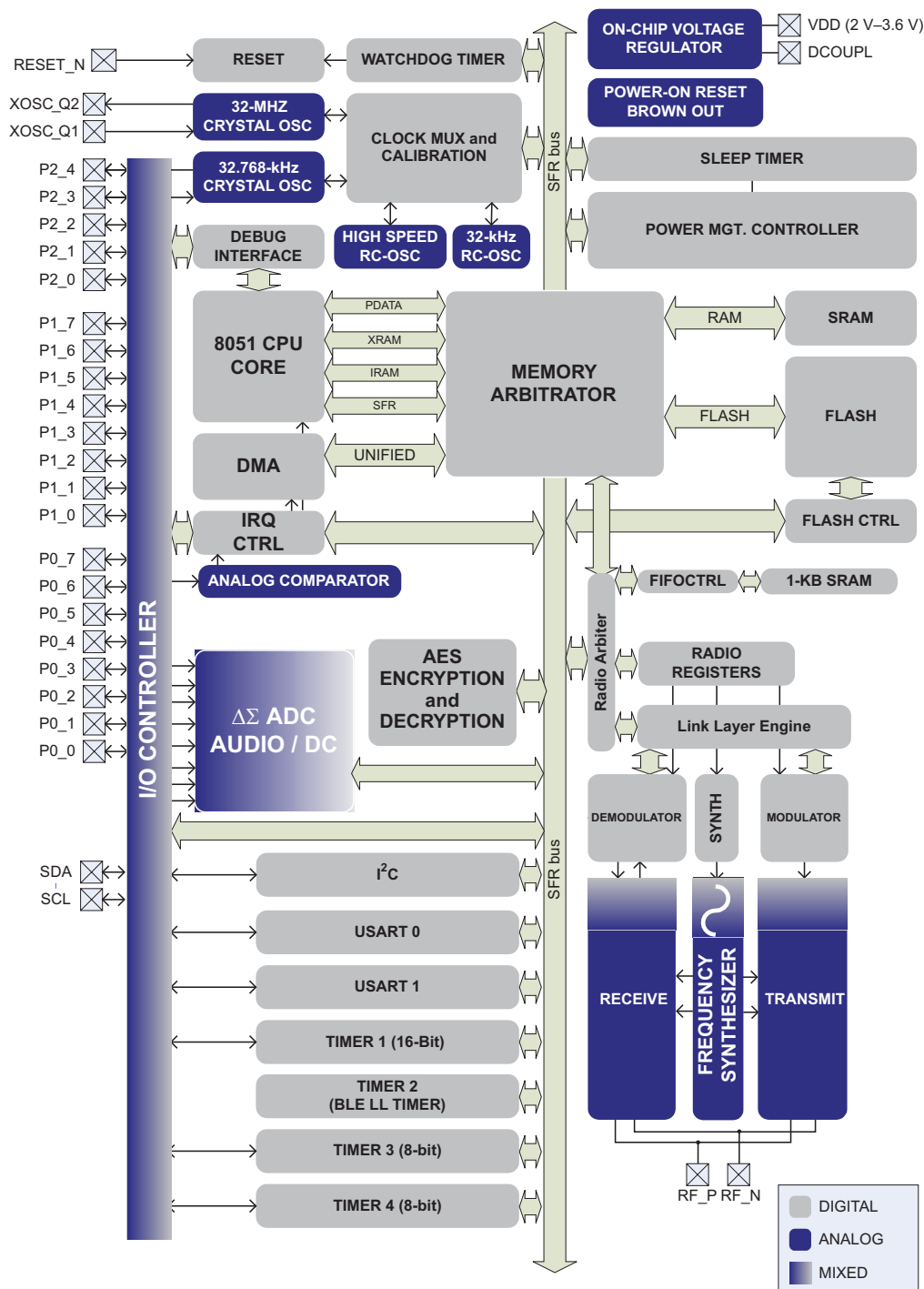


Figure 9. CC2541 Block Diagram

BLOCK DESCRIPTIONS

A block diagram of the CC2541 is shown in [Figure 9](#). The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE→DATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and D→A controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRA→, flash memory, and →RE→SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in [Figure 9](#) as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into →DATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the →DATA memory spaces. The SRA→ is an ultralow-power SRA→ that retains its contents even when the digital part is powered off (power mode 2 and mode 3).

The **128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and →DATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User →uide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the →DATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with D→A descriptors that can be located anywhere in memory. →any of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the D→A controller for efficient operation by performing data transfers between a single SFR or →RE→ address and flash(SRA→).

Each CC2541 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specification.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I→ and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2541 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I→ pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I→ pins can choose between two different I→ pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.→8-k→ crystal oscillator or an internal 32.→53-k→ RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power mode 1 or mode 2.

A built-in **watchdog timer** allows the CC2541 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PW functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PW output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit output compare registers and two 24-bit overflow compare registers that can be used to give exact timing for start of R or T to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PW functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PW output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both R and T and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SC directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

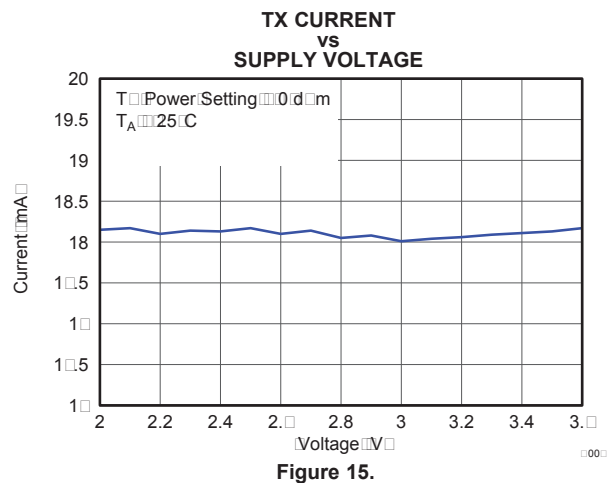
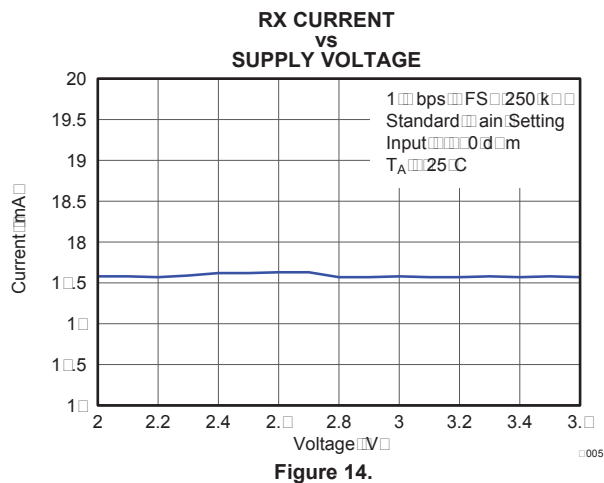
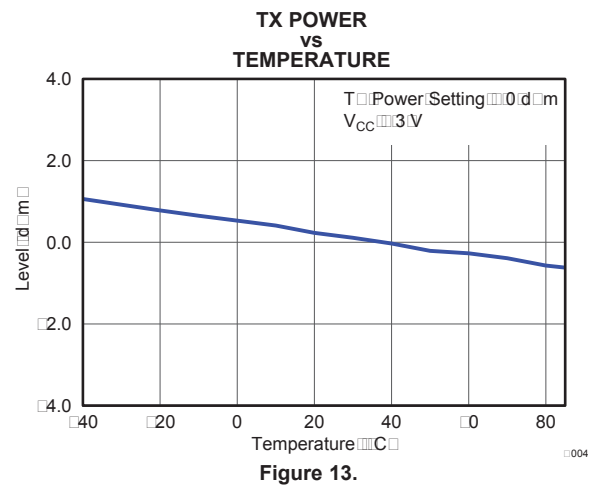
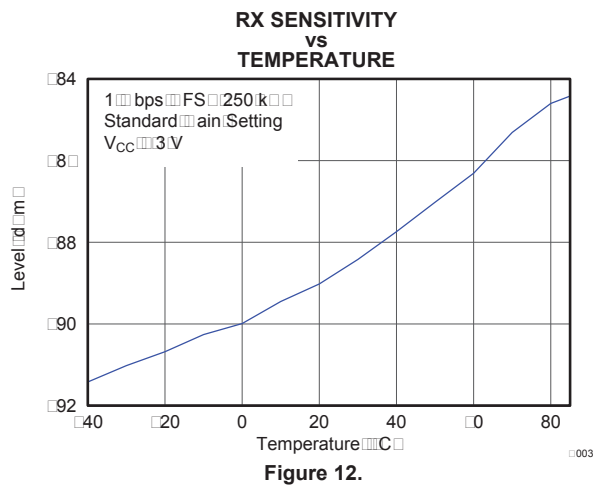
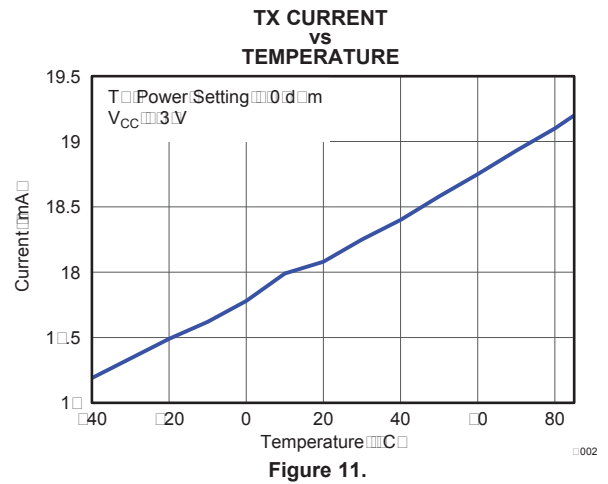
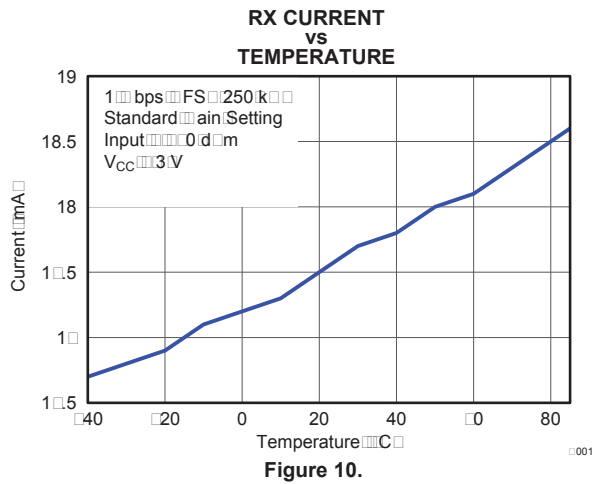
The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CCM-AC, as well as hardware support for CC.

The **ADC** supports 8 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (11 controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **I²C** module provides a digital peripheral connection with two pins and supports both master and slave operation. I²C support is compliant with the NXP I²C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit device addressing modes are supported, as well as master and slave modes.

The ultralow-power **analog comparator** enables applications to wake up from P2 or P3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I controller interrupt detector and can be treated by the MCU as a regular I pin interrupt.

TYPICAL CHARACTERISTICS



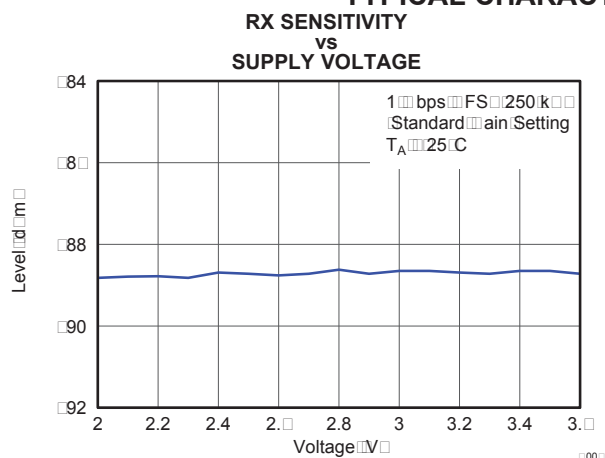
TYPICAL CHARACTERISTICS (continued)

Figure 16.

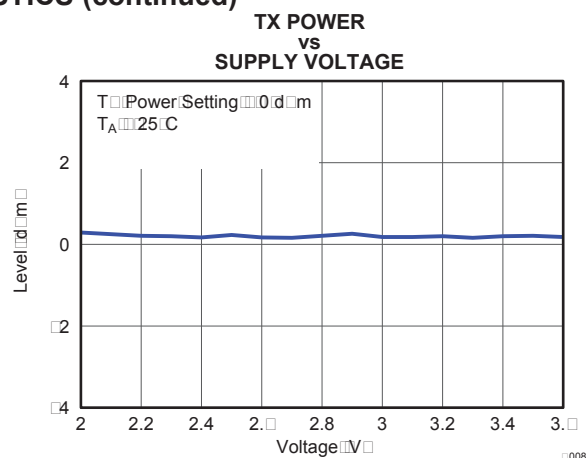


Figure 17.

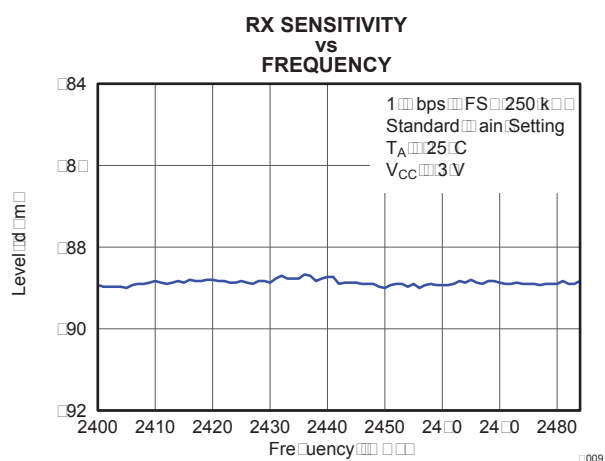


Figure 18.

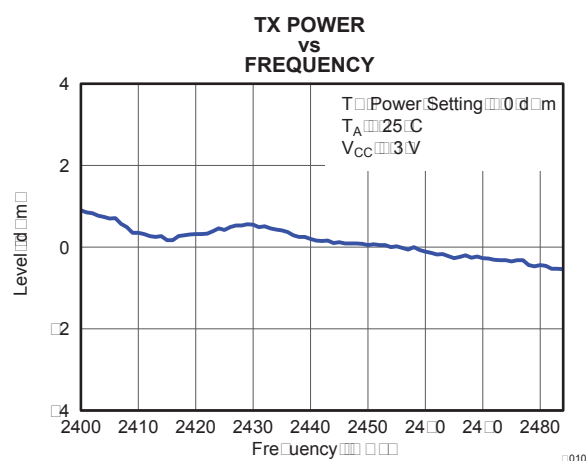


Figure 19.

Table 1. Output Power⁽¹⁾⁽²⁾

TXPOWER Setting	Typical Output Power (dBm)
0xE1	0
0xD1	-2
0xC1	-4
0xB1	-6
0xA1	-8
0x91	-10
0x81	-12
0x71	-14
0x61	-16
0x51	-18
0x41	-20
0x31	-23

⁽¹⁾ Measured on Texas Instruments CC2541 E reference design with TA = 25°C, VDD = 3 V and fc = 2440 MHz. See [SWRU191](#) for recommended register settings.

⁽²⁾ 1 Mbps, FS, 250-kHz deviation, Bluetooth low energy mode, 1% BER

Table 2. Output Power and Current Consumption

Typical Output Power (dBm)	Typical Current Consumption (mA) ⁽¹⁾	Typical Current Consumption With TPS62730 (mA) ⁽²⁾
0	18.2	14.3
–20	18.8	13.1

- ⁽¹⁾ Measured on Texas Instruments CC2541 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ kHz}$. See [SWRU191](#) for recommended register settings.
- ⁽²⁾ Measured on Texas Instruments CC2541 TPS62730 E reference design with $T_A = 25^\circ\text{C}$, $V_{DD} = 3\text{ V}$ and $f_c = 2440\text{ kHz}$. See [SWRU191](#) for recommended register settings.

TYPICAL CURRENT SAVINGS WHEN USING TPS62730

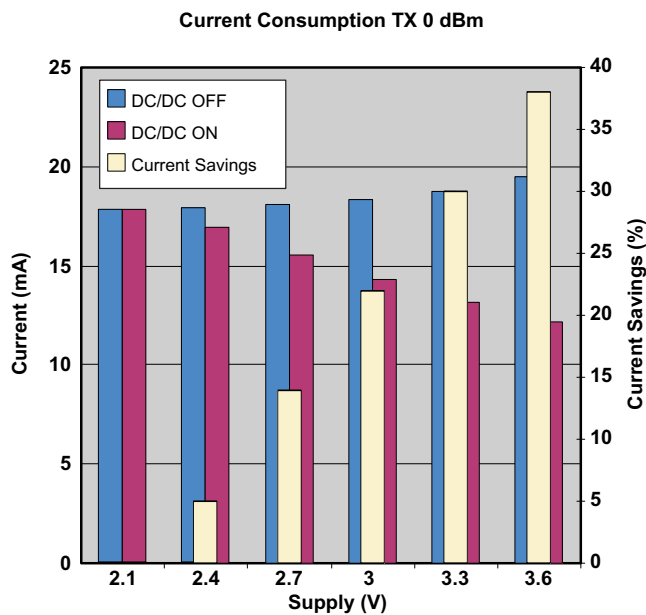


Figure 20. Current Savings in TX at Room Temperature

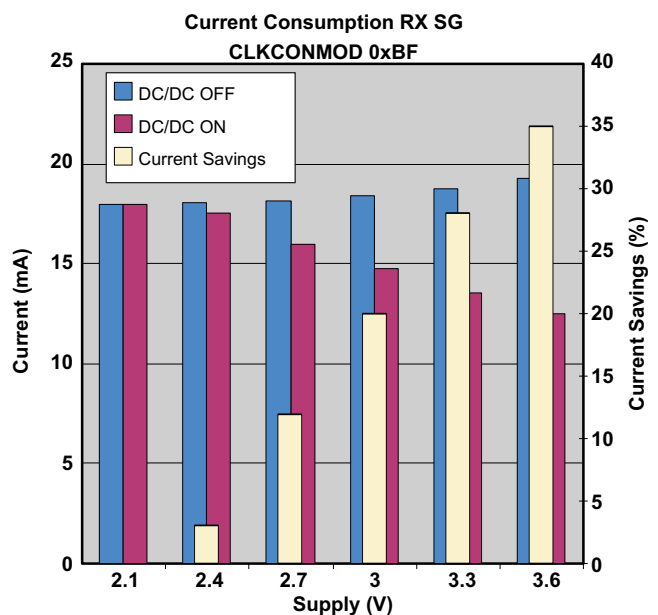
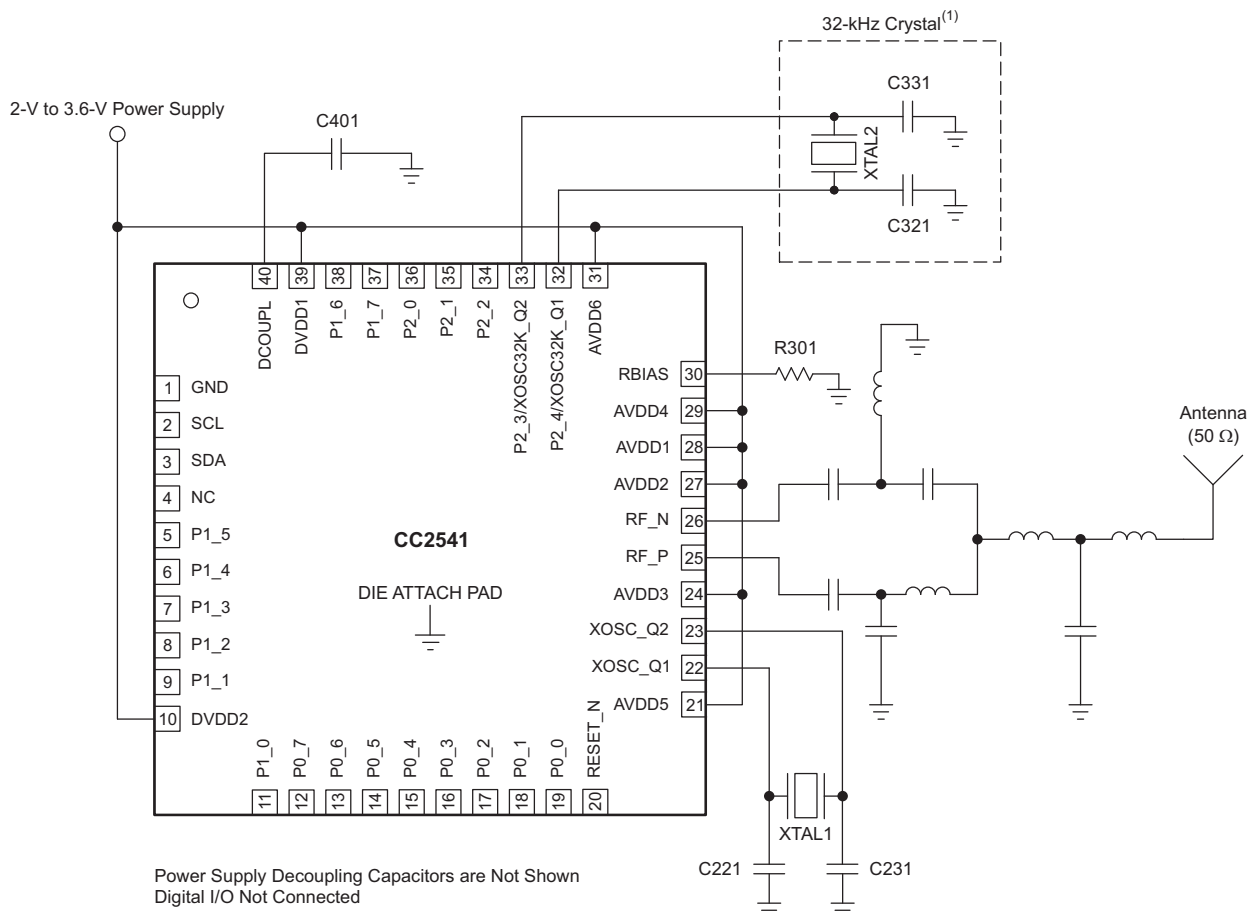


Figure 21. Current Savings in RX at Room Temperature

The application note [SWRA35](#) has information regarding the CC2541 and TPS62730 combo board and the current savings that can be achieved using the combo board.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2541. A typical application circuit is shown in Figure 22.



1 32-k crystal is mandatory when running the LE protocol stack in low-power modes, except if the link layer is in the standby state. Vol. 1 Part 1 Section 1.1 in 1.

NOTE: Different antenna alternatives will be provided as reference designs.

Figure 22. CC2541 Application Circuit

Table 3. Overview of External Components (Excluding Supply Decoupling Capacitors)

Component	Description	Value
C401	Decoupling capacitor for the internal 1.8-V digital voltage regulator	1 μ F
R301	Precision resistor 1%, used for internal biasing	5 k Ω

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2541E, for recommended balun.

Crystal

An external 32-kHz crystal, XTAL1, with two loading capacitors (C221 and C231) is used for the 32-kHz crystal oscillator. See [32-kHz CRYSTAL OSCILLATOR](#) for details. The load capacitance seen by the 32-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{\text{parasitic}} \quad (1)$$

XTAL2 is an optional 32.768-kHz crystal, with two loading capacitors (C321 and C331) used for the 32.768-kHz crystal oscillator. The 32.768-kHz crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.768-kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{\text{parasitic}} \quad (2)$$

A series resistor may be used to comply with the ESR requirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator requires a decoupling capacitor (C401) for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

References

1. *Bluetooth* Core Technical Specification document, version 4.0
<http://www.bluetooth.com/SiteCollectionDocuments/CoreV40.zip>
2. CC253x System-on-Chip Solution for 2.4-GHz IEEE 802.15.4 and ZigBee Applications CC2541 System-on-Chip Solution for 2.4-GHz Bluetooth low energy Applications [SWRU191](#)
3. Current Savings in CC254x Using the TPS2230 [SWRA355](#)

Additional Information

Texas Instruments offers a wide selection of cost-effective, low-power RF solutions for proprietary and standard-based wireless applications for use in industrial and consumer applications. Our selection includes RF transceivers, RF transmitters, RF front ends, and System-on-Chips as well as various software solutions for the sub-1- and 2.4-GHz frequency bands.

In addition, Texas Instruments provides a large selection of support collateral such as development tools, technical documentation, reference designs, application expertise, customer support, third-party and university programs.

The Low-Power RF E2E Online Community provides technical support forums, videos and blogs, and the chance to interact with fellow engineers from all over the world.

With a broad selection of product solutions, end application possibilities, and a range of technical support, Texas Instruments offers the broadest low-power RF portfolio. We make RF easy.

The following subsections point to where to find more information.

Texas Instruments Low-Power RF Web Site

- Forums, videos, and blogs
- RF design help
- E2E interaction

Join us today at www.ti.com/lprf-forum.

Texas Instruments Low-Power RF Developer Network

Texas Instruments has launched an extensive network of low-power RF development partners to help customers speed up their application development. The network consists of recommended companies, RF consultants, and independent design houses that provide a series of hardware module products and design services, including:

- RF circuit, low-power RF, and  design services
- Low-power RF and  module solutions and development tools
- RF certification services and RF circuit manufacturing

Need help with modules, engineering services or development tools □

Search the Low-Power RF Developer Network tool to find a suitable partner.

www.ti.com/lprfnetwork

Low-Power RF eNewsletter

The Low-Power RF eNewsletter keeps you up-to-date on new products, news releases, developers' news, and other news and events associated with low-power RF products from TI. The Low-Power RF eNewsletter articles include links to get more online information.

Sign up today on

www.ti.com/lprfnewsletter

REVISION HISTORY

Changes from Original (January 2012) to Revision A	Page
□ Changed data sheet status from Product Preview to Production Data	1
Changes from Revision A (February 2012) to Revision B	Page
□ Changed the Temperature coefficient Unit value From: mV/°C To: □0.1°C	10
□ Changed Figure 22 text From: □ptional 32-k□□Crystal To: 32-k□□Crystal	24
Changes from Revision B (August 2012) to Revision C	Page
□ Changed the □Internal reference voltage□TYP value From 1.15 V To: 1.24 V	12
□ Changed pin □□SC□□1 Pin Type From Analog □ To: Analog I□□, and changed the Pin Description	1□
□ Changed pin □□SC□□2 Pin Type From Analog □ To: Analog I□□	1□
Changes from Revision C (November 2012) to Revision D	Page
□ Changed the RF TRANS□IT SECTI□N, □utput power TYP value From: –20 To: –23	8
□ Changed the RF TRANS□IT SECTI□N, Programmable output power range TYP value From: 20 To: 23	8
□ Added row 0x31 to Table 1	22



Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	1 □					2 □	□□	3 □		4 5 □	
CC2541F128R□AR	ACTIVE	V□FN	R□A	40	2500	□reen□Ro□S □□no□Sb□□r□	CUNIPDAU□□ CUNIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F128	Samples
CC2541F128R□AT	ACTIVE	V□FN	R□A	40	250	□reen□Ro□S □□no□Sb□□r□	CUNIPDAU□□ CUNIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F128	Samples
CC2541F25□R□AR	ACTIVE	V□FN	R□A	40	2500	□reen□Ro□S □□no□Sb□□r□	CUNIPDAU□□ CUNIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F25□	Samples
CC2541F25□R□AT	ACTIVE	V□FN	R□A	40	250	□reen□Ro□S □□no□Sb□□r□	CUNIPDAU□□ CUNIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F25□	Samples

ACTIVE: Product device recommended for new designs.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free Green conversion plan has not been defined.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

(6) Lead and Finish values may have multiple material finish options. If Finish options are separated by a vertical ruled line, Lead and Finish values may wrap to two lines if the finish value exceeds the maximum column width.

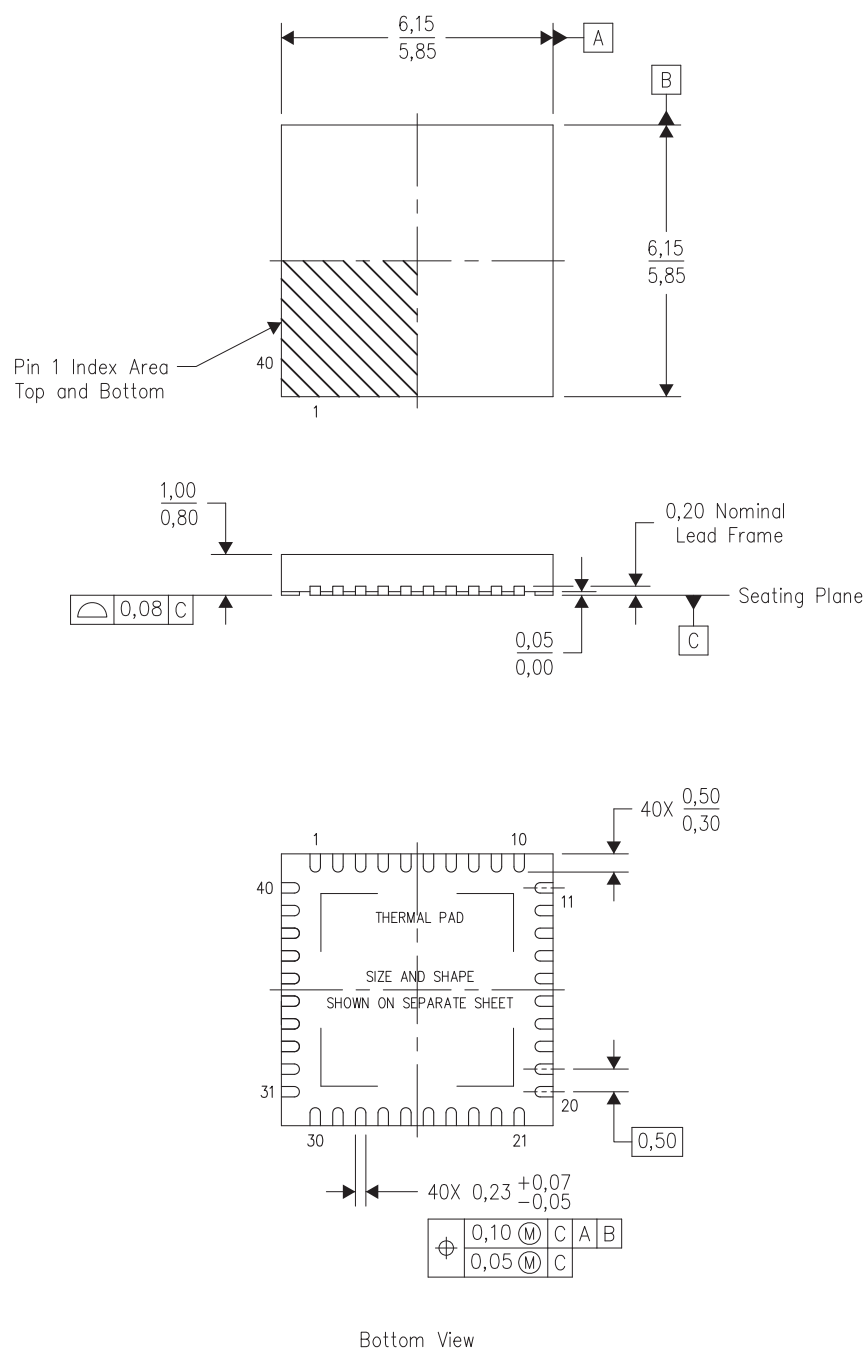
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Package complies to JEDEC MO-220 variation VJJD-2.

THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

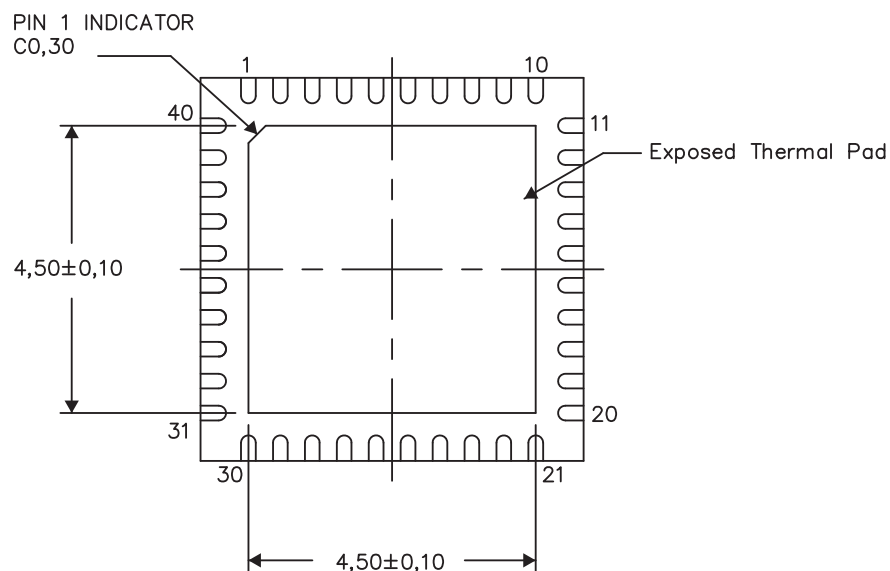
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

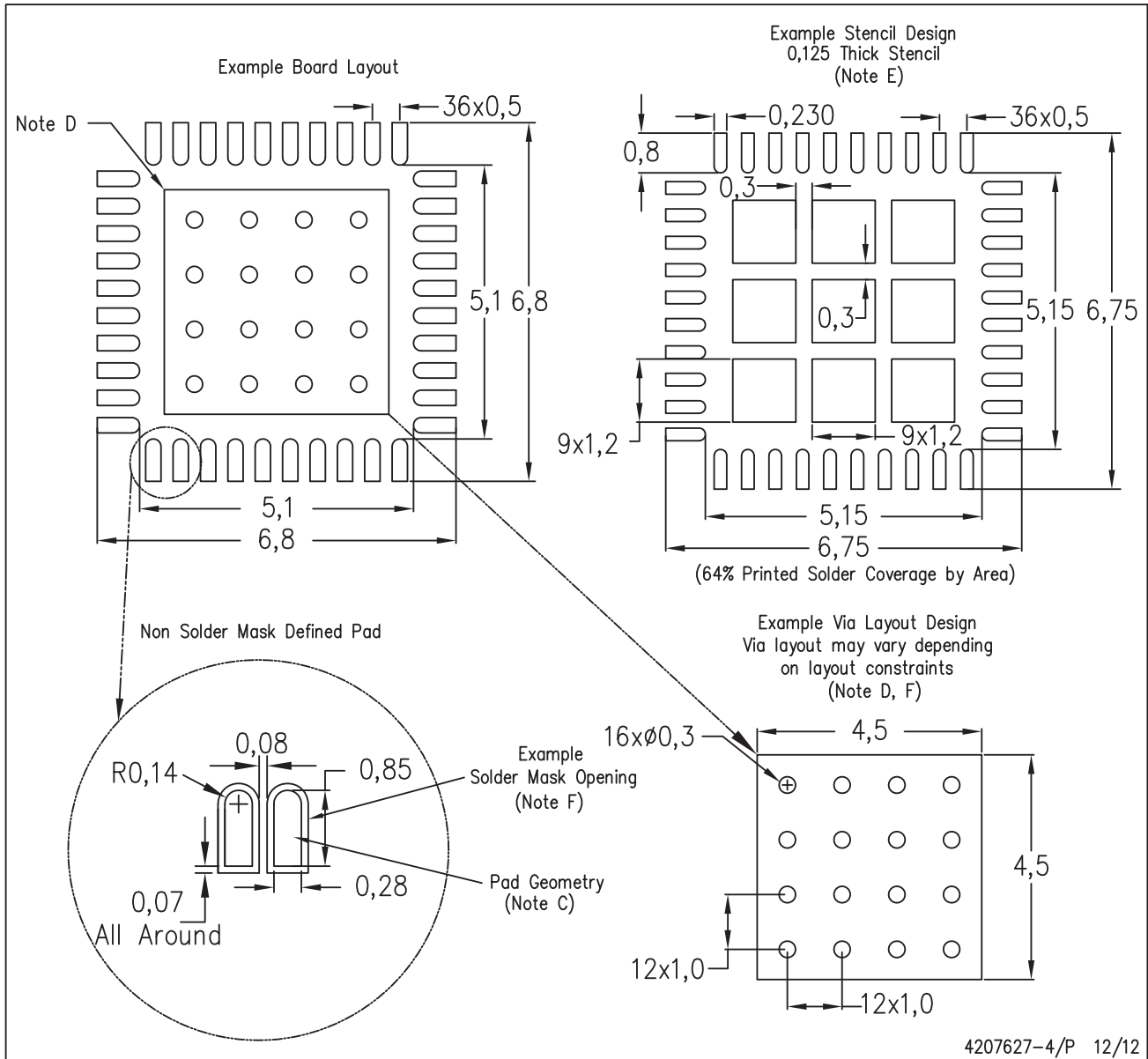
4206355-4/U 12/12

NOTES: A. All linear dimensions are in millimeters

LAND PATTERN DATA

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4207627-4/P 12/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries ("TI") reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD48, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products also referred to herein as "components" are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with buyers' products and applications, buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III or similar life-critical medical equipment unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or enhanced plastic are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the buyer's risk, and that buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Management	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com