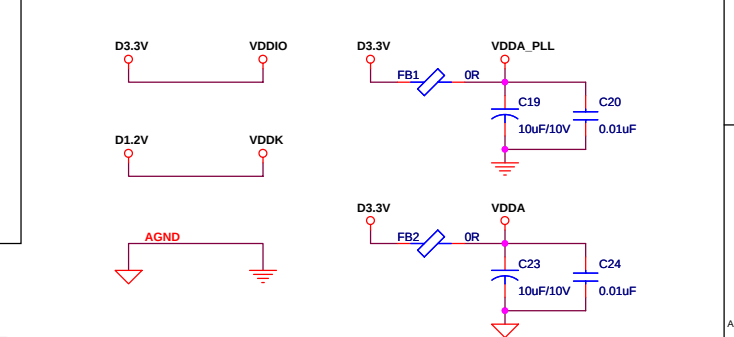
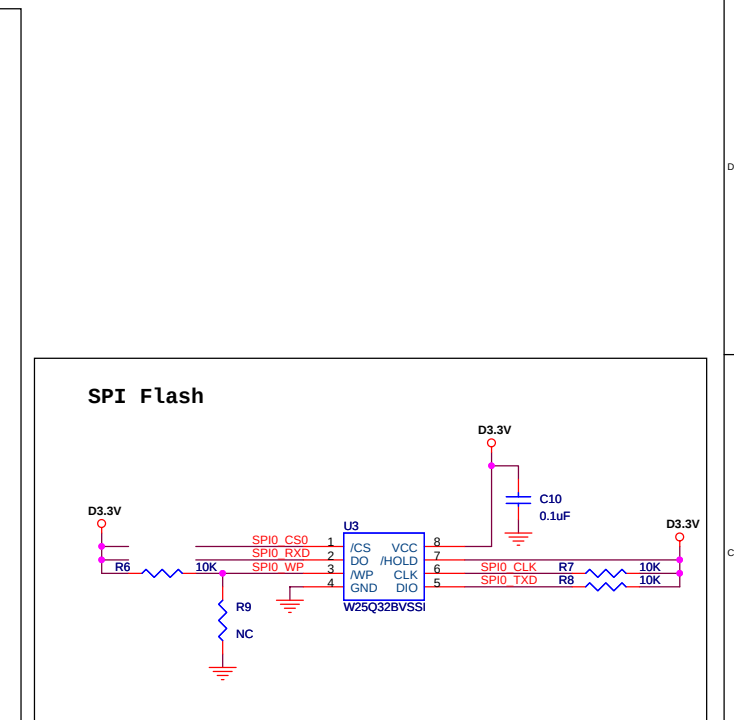
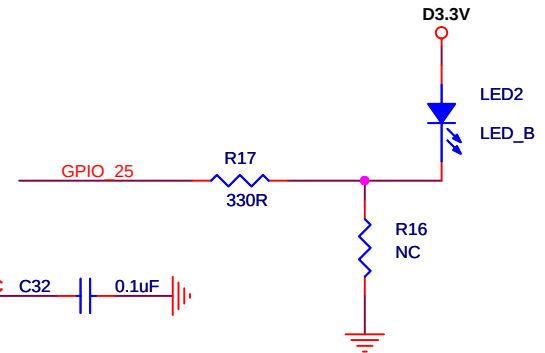
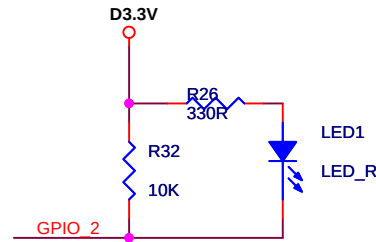
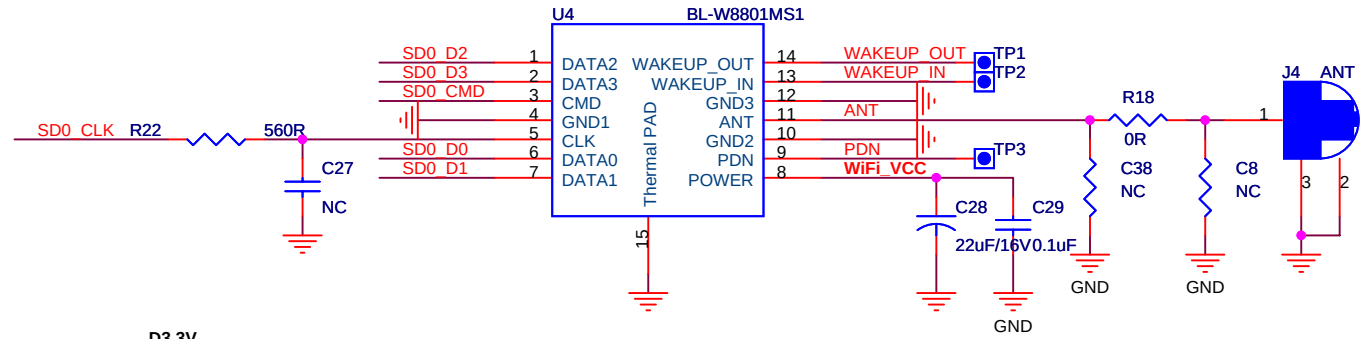
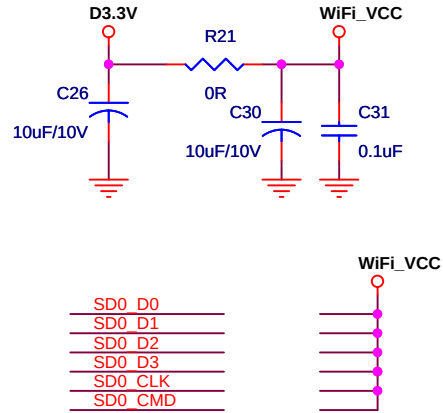
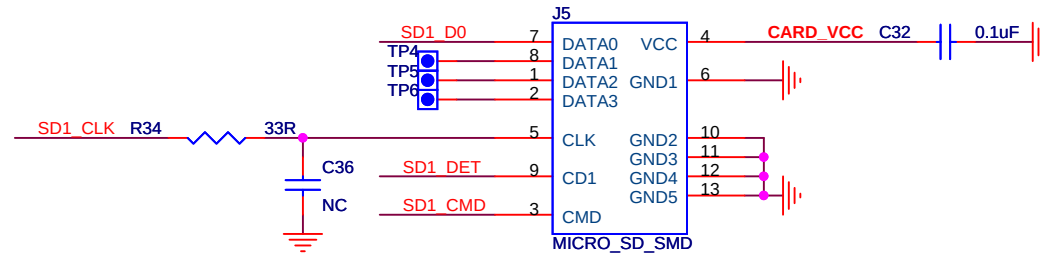
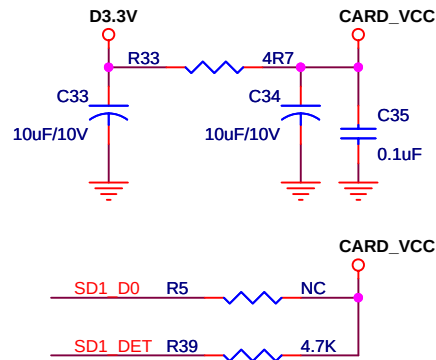


WiFi模组 (SDIO)



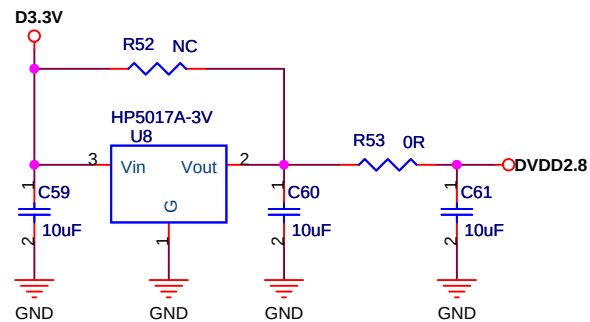
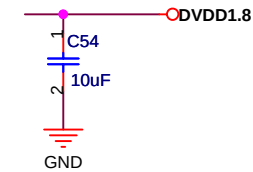
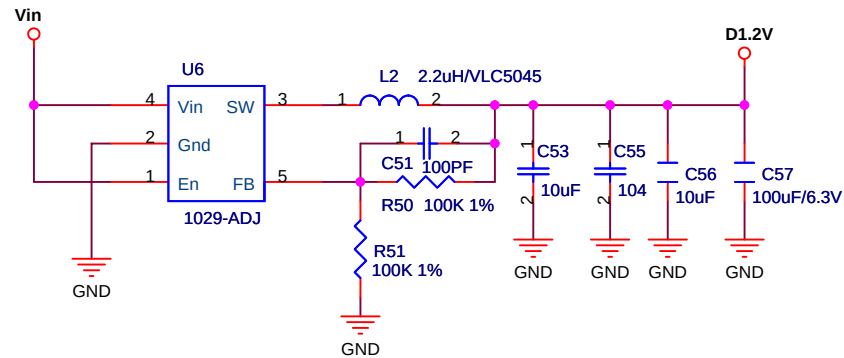
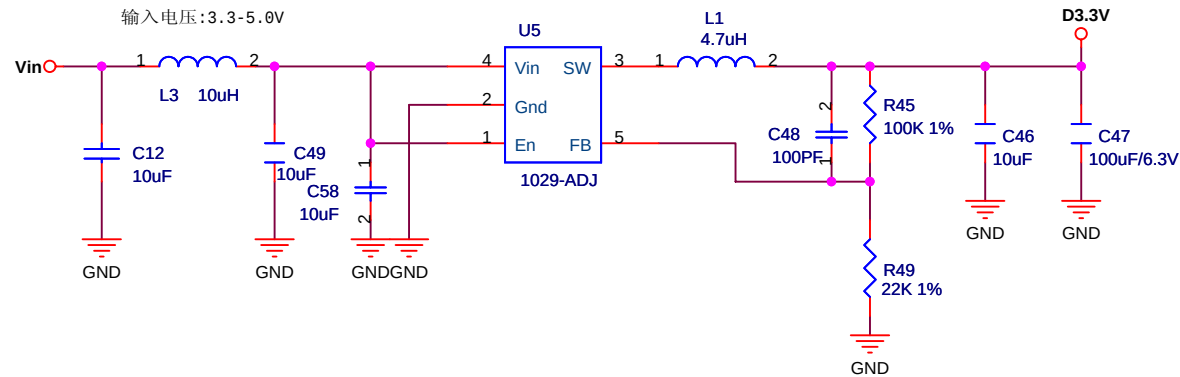
SD卡 (1位数据模式)



1 SPI0_CS1	» SPI0_CS1
1 GPIO_2	» GPIO_2
1 GPIO_3	» GPIO_3
1 GPIO_10	» GPIO_10
1 GPIO_25	» GPIO_25
1 SD0_D[3:0]	» SD0_D[3:0]
1 SD0_CLK	» SD0_CLK
1 SD0_CMD	» SD0_CMD
1 SD1_D0	» SD1_D0
1 SD1_CLK	» SD1_CLK
1 SD1_CMD	» SD1_CMD
1 SD1_DET	» SD1_DET
1 D3.3V	» D3.3V
1 GND	» GND

			WIFI&TF CARD+MIC	
			Size A4	Document Description
Date: Wednesday, September 28, 2016			Sheet 2	Rev A

Power Supply



			POWER	
Size A4	Document Description			Rev A
Date: Monday, June 27, 2016			Sheet 3 of 3	

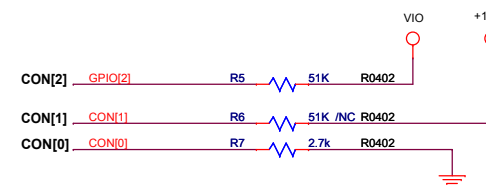
The schematic diagram illustrates the power supply network for the AD9239. A +1.8V_CHIP supply is connected to a series of AVDD18 pins (18_8 to 18_19). A +1.8V_INT supply is connected to a network of capacitors (C23, C1206) and a load (NL). Decoupling capacitors (C17, C18, C21, C22, C26, C27, C28, C29, C30, C31, C36, C37) are placed at each AVDD18 pin, with values of 0.01uF or 10pF. The capacitors are connected to ground.

VIO & VIO_SD

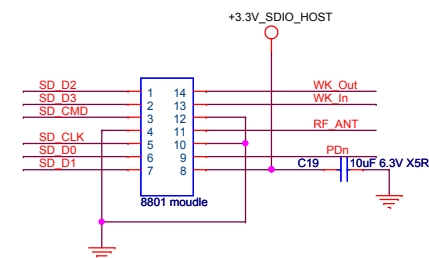
[illegible]

RF FRONT END

CON	FUNCTION
2	Reference clock frequency selection 1 - 38.4 MHz (Default)
1:0	Boot options: 10 - SDIO



SOC Strap Config



SDIO HOST, Moudle Pin

