

ATWINC15x0-MR210xB IEEE 802.11 b/g/n SmartConnect IoT Module

ATWINC15x0

www.microchip.com Product Pages: [ATWINC1500](#), [ATWINC1510](#)



Introduction

The ATWINC15x0-MR210xB is a low power consumption 802.11 b/g/n IoT (Internet of Things) module, specifically optimized for low power IoT applications. The module integrates Power Amplifier (PA), Low-Noise Amplifier (LNA), Switch, Power Management and a printed antenna or a micro co-ax (U.FL) connector for an external antenna resulting in a small form factor (21.7 x 14.7 x 2.1 mm) design. It is interoperable with various vendors' 802.11 b/g/n access points. This module provides Serial Peripheral Interface (SPI) ports to interface with a host controller.

The references to the ATWINC15x0-MR210xB module include the module devices listed in the following:

- ATWINC1500-MR210PB
- ATWINC1500-MR210UB
- ATWINC1510-MR210PB
- ATWINC1510-MR210UB

Features

- IEEE 802.11 b/g/n, Single Stream (1x1) 20 MHz Bandwidth WLAN Link
 - Compatible with Wi-Fi® 6/7 2.4 GHz band
- Single Spatial Stream in 2.4 GHz ISM Band
- Integrated Transmit/Receive Switch
- Integrated PCB Antenna or U.FL micro co-ax Connector for External Antenna
- Superior Sensitivity and Range via Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Soft-AP Support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- Support Enterprise Security with WPA/WPA2 (802.1X)⁽¹⁾
 - EAP-TLS
 - EAP-PEAPv0/1 with TLS
 - EAP-TTLSv0 with MSCHAPv2
 - EAP-PEAPv0/1 with MSCHAPv2
- Superior MAC Throughput Through Hardware Accelerated Aggregate A-MPDUs/A-MDSU Frame Reception and Block Acknowledgment
- On-chip Memory Management Engine to Reduce Host Load
- SPI Host Interface

- Operating Temperature Range from -40°C to +85°C. RF Performance at Room Temperature of 25°C with a 2-3 dB Change at Boundary Conditions
- Power supply for I/O (VDDIO) Ranges from 2.7V to 3.6V
- Power Supply for DC/DC Converter (VBAT) Ranges from 3.0V to 4.2V
- Built-in 26 MHz Crystal
- Integrated Flash Memory for System Software
- Power Save Modes
 - 4 μ A Power-Down mode typical at 3.3V I/O
 - 380 μ A Doze mode with chip settings preserved (used for beacon monitoring) ⁽²⁾
 - On-chip low power sleep oscillator
 - Fast host wake-up from Doze mode by a pin or SPI transaction
- Fast Boot Options
 - On-chip boot ROM (Firmware instant boot)
 - SPI flash boot
 - Low-leakage on-chip memory for state variables
 - Fast AP re-association (150 ms)
- On-Chip Network Stack to Offload MCU
 - Network features TCP, UDP, DHCP, ARP, HTTP, TLS and DNS
 - Hardware accelerators for Wi-Fi and TLS security to improve connection time
- Hardware Accelerator for IP Checksum
- Hardware Accelerators for OTA Security
- Small Footprint Host Driver
- Wi-Fi Alliance® Certifications for Connectivity and Optimizations
 - ID: [WFA61069](#)

Notes:

1. For more information on the software features, refer to the *Wi-Fi Network Controller Software Design Guide* at ww1.microchip.com/downloads/en/DeviceDoc/00002389A.pdf.
2. For more information on the module power modes, refer to [Power Consumption](#).

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1. Ordering Information and Module Marking

The following table provides the ordering information for the ATWINC15x0-MR210xB modules.

Table 1-1. Ordering Information

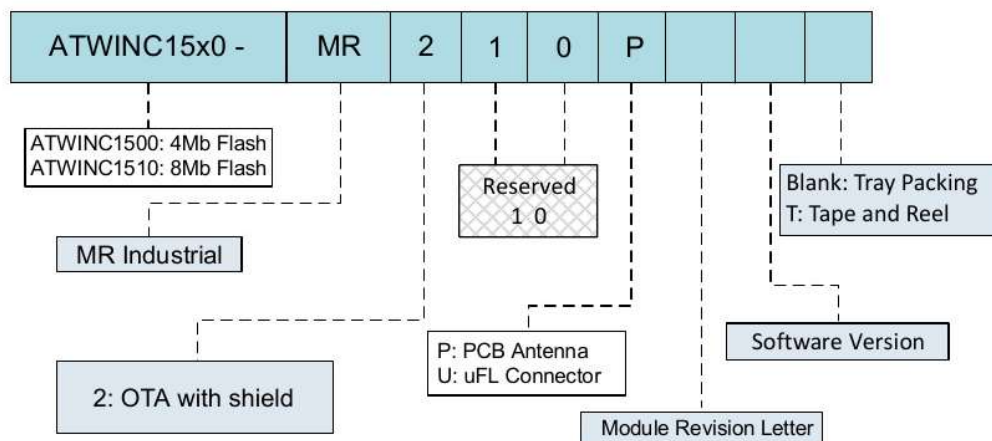
Model Number	Ordering Code ⁽¹⁾	Package Dimension	No. of Pins	Description	Regulatory Certification
ATWINC1500-MR210PB	ATWINC1500-MR210PBXXXX	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1500B chip (4Mb Flash) and PCB printed antenna	FCC, ISED, CE, MIC, KCC, NCC, SRRC, ANATEL
ATWINC1500-MR210UB	ATWINC1500-MR210UBXXXX	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1500B chip (4Mb Flash) and U.FL connector	FCC, ISED, CE, ANATEL
ATWINC1510-MR210PB	ATWINC1510-MR210PBXXXX	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1510B chip (8Mb Flash) and PCB printed antenna	FCC, ISED, CE, MIC, KCC, NCC, SRRC, ANATEL
ATWINC1510-MR210UB	ATWINC1510-MR210UBXXXX	21.7 x 14.7 x 2.1 mm	28	Certified Module with ATWINC1510B chip (8Mb Flash) and U.FL connector	FCC, ISED, CE, ANATEL

Note:

- XXXX in the Ordering Code represents the Firmware version of the product. For more details, refer to the *Software Release Notes* available on the [Microchip web page](#).

The following figure illustrates the ATWINC15x0-MR210xB modules' marking information.

Figure 1-1. Marking Information

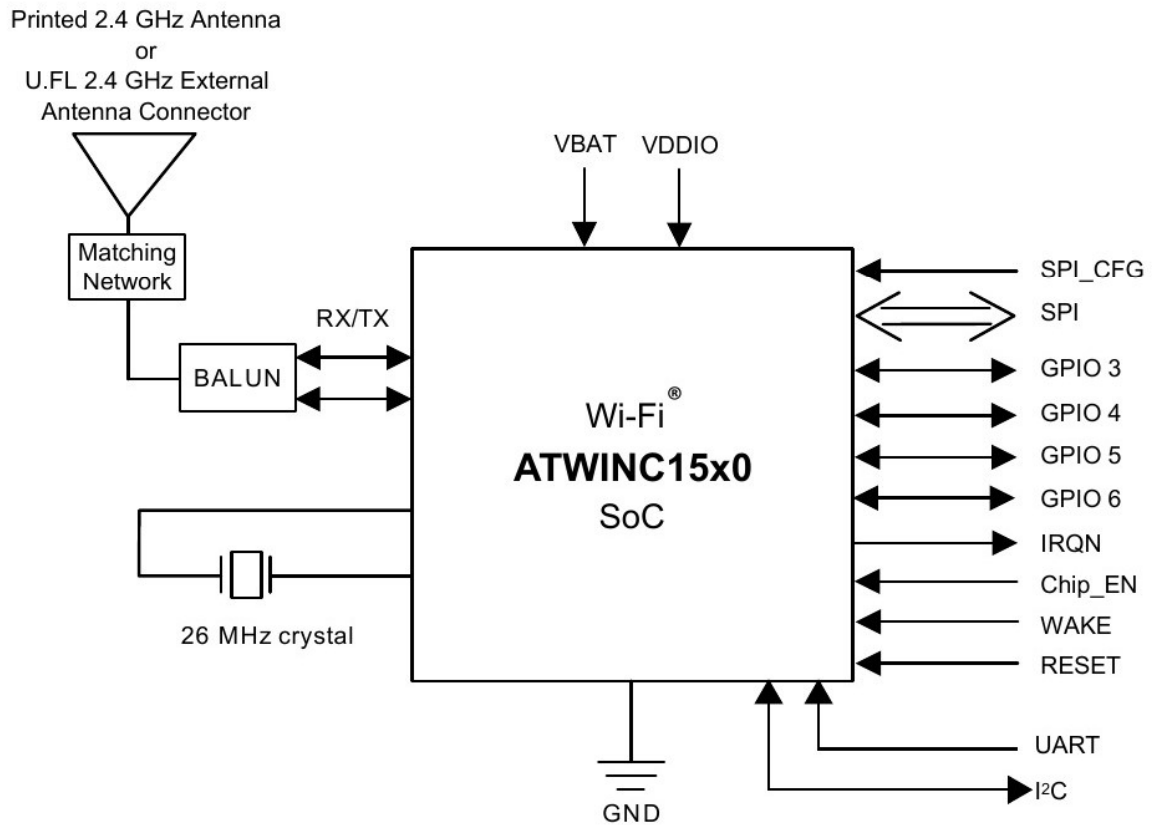


2. Functional Overview

2.1 Block Diagram

The following figure illustrates the ATWINC15x0 block diagram.

Figure 2-1. ATWINC15x0-MR210xB Module Block Diagram



2.2 Pin Description

The following figure illustrates the ATWINC15x0-MR210xB module pin out. This module has an exposed ground pad that must be connected to the system board ground.

Figure 2-2. Pin Diagram

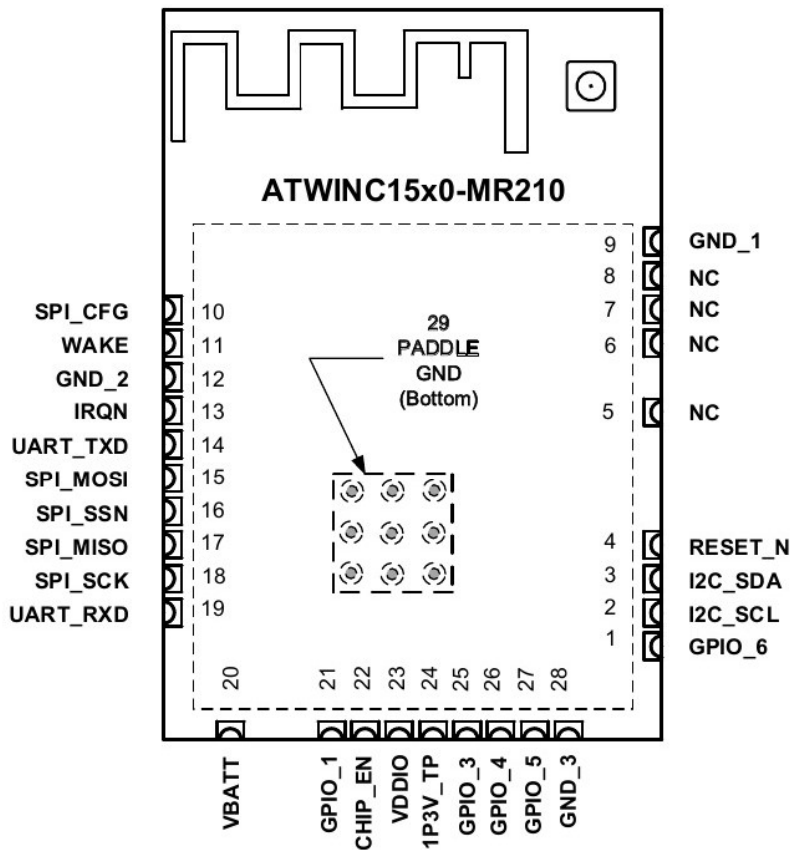


Table 2-1. ATWINC15x0-MR210xB Pin Description

Pin #	Name	Type	Description	Programmable Pull-up Resistor
1	GPIO_6	I/O	General purpose I/O ⁽¹⁾	Yes
2	I2C_SCL	I/O	I ² C Client Clock. Currently used only for development debugging. Leave unconnected. It is recommended to add Test Point to this pin.	Yes
3	I2C_SDA	I/O	I ² C Client Data. Currently used only for development debugging. Leave unconnected. It is recommended to add Test Point to this pin.	Yes
4	RESET_N	I	Active-Low Hard Reset. When this pin is asserted low, the module is set to the Reset state. When this pin is asserted high, the module comes out of Reset and functions normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1 M Ω pull-down resistor to ensure a low level at power-up.	No
5	NC	—	No connect	—
6	NC	—	No connect	—
7	NC	—	No connect	—
8	NC	—	No connect	—
9	GND_1	—	GND	—
10	SPI_CFG	I	Tie to VDDIO through a 1 M Ω resistor to enable the SPI interface.	No

Table 2-1. ATWINC15x0-MR210xB Pin Description (continued)

Pin #	Name	Type	Description	Programmable Pull-up Resistor
11	WAKE	I	Host Wake control ⁽²⁾	Yes
12	GND_2	—	GND	—
13	IRQN	O	ATWINC15x0-MR210xB Device Interrupt output. Connect to host interrupt input pin.	Yes
14	UART_TXD	O	UART Transmit Output from ATWINC15x0-MR210xB Added for debugging and testing only.	Yes
15	SPI_MOSI	I	SPI MOSI (Host Out, Client In) pin	Yes
16	SPI_SSN	I	SPI Client Select. Active-low.	Yes
17	SPI_MISO	O	SPI MISO (Host In, Client Out) pin	Yes
18	SPI_SCK	I	SPI Clock	Yes
19	UART_RXD	I	UART Receive input to ATWINC15x0-MR210xB Added for debugging and testing only.	Yes
20	VBATT	—	Battery power supply	—
21	GPIO_1	I	General Purpose I/O ⁽¹⁾	Yes
22	CHIP_EN	I	Module enable. High level enables the module; low level places the module in Power-Down mode. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull-down resistor to ensure a low level at power-up.	No
23	VDDIO	—	I/O Power Supply. Must match the host I/O voltage.	—
24	1P3V_TP	—	1.3V VDD Core Test Point. Decouple with the 10 μF and 0.01 μF to the GND. Close to the pin.	—
25	GPIO_3	I/O	General purpose I/O ⁽¹⁾	Yes
26	GPIO_4	I/O	General purpose I/O ⁽¹⁾	Yes
27	GPIO_5	I/O	General purpose I/O ⁽¹⁾	Yes
28	GND_3	—	GND	—
29	PADDLE GND	—	GND	—

Note:

1. Usage of the GPIO functionality is not supported by the ATWINC15x0 firmware. The data sheet will be updated when the support for this feature is added.
2. While the current firmware implementation wakes the ATWINC device through the SPI interface, it is recommended that the WAKE pin is connected to a host I/O pin for possible future use.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Absolute maximum ratings for the ATWINC15x0-MR210xB modules are listed below.

Table 3-1. Conditions

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	5.0	V
Operating Temperature	—	-40	+85	°C

CAUTION Stresses listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to the maximum rating conditions for extended periods may affect the device's reliability.

3.2 Recommended Operating Conditions

Table 3-2. Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit
VBATT	3.0	3.3	4.2	V
VDDIO	2.7	3.3	3.6	V

3.3 DC Electrical Characteristics

The following table provides the DC characteristics for the ATWINC15x0-MR210xB digital pads.

Table 3-3. ATWINC15x0-MR210xB Electrical Characteristics

Characteristic	Min.	Typ.	Max.	Unit
Input low voltage (V_{IL})	-0.30	—	0.65	V
Input high voltage (V_{IH})	VDDIO-0.60	—	VDDIO+0.30	
Output low voltage (V_{OL})	—	—	0.45	
Output high voltage (V_{OH})	VDDIO-0.50	—	—	
Output loading	—	—	20	pF
Digital input load	—	—	6	
Pad drive strength (regular pads ⁽¹⁾)	8	13.5	—	mA
Pad drive strength (high-drive pads ⁽¹⁾)	16	27	—	

Note:

1. The I2C_SCL and I2C_SDA are high-drive pads and all other pads are regular.

3.3.1 Current Consumption in Various Device States

The following table provides the current consumption of ATWINC15x0-MR210xB in various device states.

Table 3-4. ATWINC15x0-MR210xB Current Consumption

Device State	Code Rate	Output Power, dBm	Current Consumption ⁽¹⁾	
			IVBATT	IVDDIO
ON_Transmit	802.11b 1 Mbps	17.5	268 mA	22 mA
	802.11b 11 Mbps	18.5	264 mA	22 mA
	802.11g 6 Mbps	17.5	269 mA	22 mA
	802.11g 54 Mbps	16.0	266 mA	22 mA
	802.11n MCS 0	17.0	268 mA	22 mA
	802.11n MCS 7	14.5	265 mA	22 mA
ON_Receive	802.11b 1 Mbps	N/A	61 mA	22 mA
	802.11b 11 Mbps	N/A	61 mA	22 mA
	802.11g 6 Mbps	N/A	61 mA	22 mA
	802.11g 54 Mbps	N/A	61 mA	22 mA
	802.11n MCS 0	N/A	61 mA	22 mA
	802.11n MCS 7	N/A	61 mA	22 mA
ON_Doze	N/A	N/A	380 μ A	<10 μ A
Power_Down	N/A	N/A	<0.5 μ A	<3.5 μ A

Note:

1. Conditions: VBATT =3.3V, VDDIO=3.3V and at 25°C

3.4 Receiver Performance

Table 3-5. Receiver Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency	—	2,412	—	2,484	MHz

Table 3-5. Receiver Performance (continued)

Parameter	Description	Minimum	Typical	Maximum	Unit
Sensitivity 802.11b	1 Mbps DSS	—	-95	—	dBm
	2 Mbps DSS	—	-90	—	
	5.5 Mbps DSS	—	-92	—	
	11 Mbps DSS	—	-86	—	
Sensitivity 802.11g	6 Mbps OFDM	—	-90	—	
	9 Mbps OFDM	—	-89	—	
	12 Mbps OFDM	—	-88	—	
	18 Mbps OFDM	—	-85	—	
	24 Mbps OFDM	—	-83	—	
	36 Mbps OFDM	—	-80	—	
	48 Mbps OFDM	—	-76	—	
	54 Mbps OFDM	—	-74	—	
Sensitivity 802.11n (BW=20 MHz)	MCS 0	—	-89	—	
	MCS 1	—	-87	—	
	MCS 2	—	-85	—	
	MCS 3	—	-82	—	
	MCS 4	—	-77	—	
	MCS 5	—	-74	—	
	MCS 6	—	-72	—	
	MCS 7	—	-70.5	—	
Maximum Receive Signal Level	1-11 Mbps DSS	—	0	—	
	6-54 Mbps OFDM	—	0	—	
	MCS 0-7	—	0	—	
Adjacent Channel Rejection	1 Mbps DSS (30 MHz offset)	—	50	—	dB
	11 Mbps DSS (25 MHz offset)	—	43	—	
	6 Mbps OFDM (25 MHz offset)	—	40	—	
	54 Mbps OFDM (25 MHz offset)	—	25	—	
	MCS 0-20 MHz BW (25 MHz offset)	—	40	—	
	MCS 7-20 MHz BW (25 MHz offset)	—	20	—	
Cellular Blocker Immunity	776-794 MHz CDMA	—	-14	—	dBm
	824-849 MHz GSM	—	-10	—	
	880-915 MHz GSM	—	-10	—	
	1710-1785 MHz GSM	—	-15	—	
	1850-1910 MHz GSM	—	-15	—	
	1850-1910 MHz WCDMA	—	-24	—	
	1920-1980 MHz WCDMA	—	-24	—	

Note:

1. Receiver sensitivity is measured in the Test mode condition on a conducted RF test setup.

3.5 Transmitter Performance

Table 3-6. Transmitter Performance^(3, 4, 5, 6, 7)

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency	—	2,412	—	2,484	MHz
Output Power ^(1, 2) ON_Transmit	802.11b 1 Mbps	—	13.6	—	dBm
	802.11b 11 Mbps	—	15.3	—	
	802.11g 6 Mbps	—	18.9	—	
	802.11g 54 Mbps	—	14.3	—	
	802.11n MCS 0	—	18.9	—	
	802.11n MCS 7	—	12.2	—	
TX Power Accuracy	—	—	±1.5 ⁽²⁾	—	dB
Carrier Suppression	—	—	30.0	—	dBc
Harmonic Output Power	2nd	—	—	-41	dBm/MHz
	3rd	—	—	-41	

Notes:

1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at balun output.
3. Operating temperature range is -40°C to +85°C. RF performance is ensured at a room temperature of 25°C with a 2-3 dB change at boundary conditions.
4. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
5. The availability of some specific channels and/or operational frequency bands are country dependent and must be programmed at the host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.
6. The RF parameters for the ATWINC15x0-MR210UB is reduced approximately by 1 dB. This insertion loss accounts for PCB trace loss and a filter network to RF U.FL connector.
7. For more details on the I²C Client interface, refer to 6.1 “I²C Client Interface” from the *ATWINC15x0B-MU IEEE® 802.11 b/g/n Network Controller SoC Datasheet* ([DS70005374](#)).

3.6 SPI Timing Characteristics

The SPI timing is provided in the following figure and table.

Figure 3-1. SPI Timing Diagram (SPI Mode CPOL = 0, CPHA = 0)

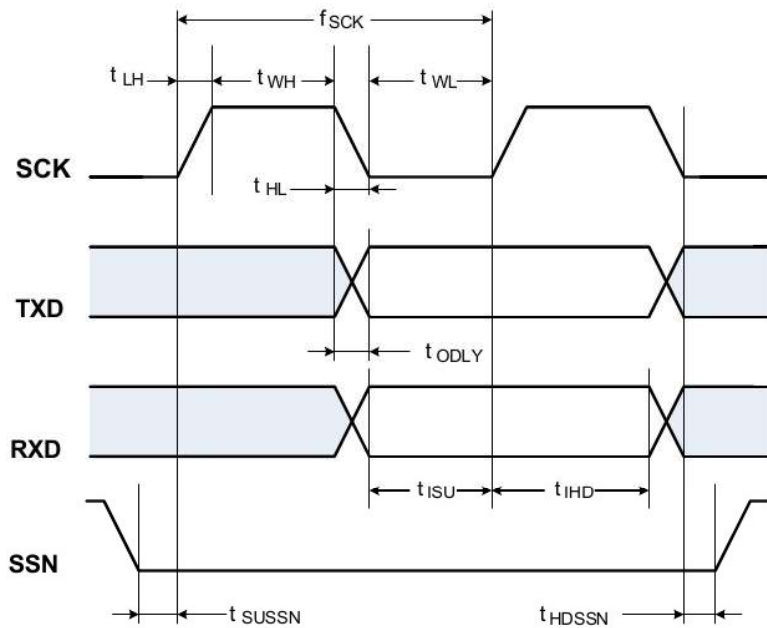


Table 3-7. SPI Client Timing Parameters⁽¹⁾

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency ⁽²⁾	f_{SCK}	—	48	MHz
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay ⁽³⁾	t_{ODLY}	4	9 from SCK fall	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Notes:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Client interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading under all conditions, $t_{LH} + t_{WH} + t_{HL} + t_{WL}$ must be less than or equal to $1/f_{SCK}$.

4. CPU and Memory Subsystems

4.1 Processor

The ATWINC15x0-MR210xB modules have a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to the association, authentication, power management, security key management and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

4.2 Memory Subsystem

The APS3 core uses a 128 kB instruction/boot ROM along with a 160 kB instruction RAM and a 64 kB data RAM. The ATWINC15x0-MR210xB modules come populated with either 4 Mb or 8 Mb of Flash memory depending on the module model that is ordered. This memory can be used for system software. See [Table 1-1](#) for more information. In addition, the device uses a 128 kB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

4.3 Nonvolatile Memory (eFuse)

The ATWINC15x0-MR210xB modules have 768 bits of nonvolatile eFuse memory that can be read by the CPU after device reset. The eFuse is partitioned into six 128-bit banks (Bank 0 – Bank 5). Each bank has the same bit map (see the following figure). The purpose of the first 108 bits in each bank is fixed and the remaining 20 bits are general-purpose software-dependent bits or reserved for future use.

Notes: If IQ Amp Used, IQ Amp Correction, IQ Pha Used and IQ Pha Correction bit fields are programmed, Bank 0 must not be programmed with any values, and only the Bank Invalid bit must be programmed. This nonvolatile one-time-programmable (OTP) memory can be used for storing the following customer-specific parameters:

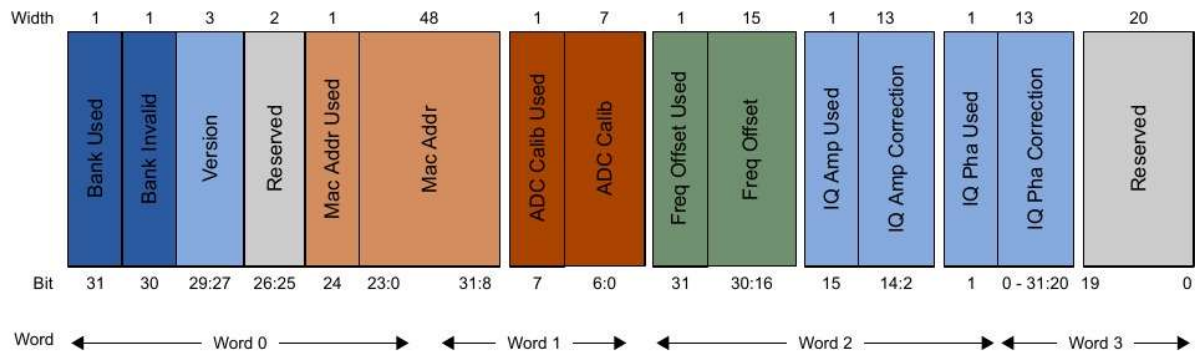
- MAC address
- Calibration information (crystal frequency offset and so on)
- Other software-specific configuration parameters

Each bank can be programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address is currently programmed in Bank 2 and to update the new MAC address, perform the following steps:

1. Invalidate the contents of Bank 2 by programming the Bank Invalid bit field of Bank 2.
2. Program Bank 3 with the new MAC address along with the values of ADC Calib (if used in Bank 2), Frequency Offset (from Bank 2), IQ Amp Correction (from Bank 2) and IQ Pha Correction (from Bank 2). The Used bit field for each corresponding value bit field should also be programmed.
3. Validate the contents of Bank 3 by programming the Bank Used bit field of Bank 3.

Each bit field (i.e., MAC Address, ADC Calibration, Frequency Offset, IQ Amp Correction and IQ Pha Correction) has its corresponding Used bit field. Each Used bit field indicates the firmware that the value in the related bit field is valid. A value of '0' in the Used bit field indicates that the following bit field is invalid and a value of '1' programmed to the Used bit field indicates that the corresponding bit field is valid and can be used by firmware. By default, ATWINC15x0-MR210xB modules are programmed with the MAC address, Frequency Offset bits, IQ Amp and IQ Phase fields of Bank 2.

Figure 4-1. Bit map for ATWINC15x0-MR210xB eFuse Bank



Note: The bit map has been updated with the IQ Amp correction and IQ Pha Correction fields from firmware version 19.7 onwards. Earlier these bit fields were reserved for future use. For customers using firmware older than 19.7, IQ Amp correction and IQ Pha Correction bit fields are not used by the firmware.

The matrix table below provides details on how different versions of the firmware would handle the IQ Amp used, IQ Amp correction, IQ Pha used and IQ Pha correction bit fields during Initialization.

Firmware Version Used by Customer	IQ Amp Used and IQ Pha Used Bit Status	
	Device with IQ Amp Used and IQ Pha Used Bits with Value '1'	Device with IQ Amp Used and IQ Pha Used Bits with Value '0'
19.7 or later for ATWINC15x0	Firmware loads the IQ cal values from the IQ Amp correction and IQ Pha correction bit fields of corresponding eFuse bank and proceeds with Initialization.	Firmware ignores the values in the IQ Amp correction and IQ pha correction bit fields of corresponding eFuse bank and proceeds with initialization.
Prior to 19.7 for ATWINC15x0	Firmware does not check for the IQ Amp and IQ Pha used bit fields and proceeds with Initialization.	

5. WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY) including the radio.

5.1 MAC

5.1.1 Description

The ATWINC15x0-MR210xB MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, an FCS engine checks the CRC of the transmitting and receiving packets and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP and WPA2 CCMP-AES.

Control functions that have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication) and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in the software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions that need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

5.1.2 Features

The ATWINC15x0-MR210xB IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA Multiple Access Categories.
- Advanced IEEE 802.11n Features:
 - Reception of aggregated MPDUs (A-MPDU)
 - Reception of aggregated MSDUs (A-MSDU)
 - Immediate Block Acknowledgment
 - Reduced Interframe Spacing (RIFS)
- IEEE802.11i and WPA Security with Key Management:
 - WEP 64/128

- WPA-TKIP
 - 128-bit WPA2 CCMP (AES)
- Advanced Power Management:
 - Standard 802.11 Power Save Mode
- RTS-CTS and CTS-self Support
- Either STA or AP Mode in the Infrastructure Basic Service Set Mode

5.2 PHY

5.2.1 Description

The ATWINC1500B WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real-world communication environment with impairments and interference. The PHY implements all the required functions that include FFT, filtering, FEC (Viterbi decoder), frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

5.2.2 Features

The ATWINC1500B IEEE802.11 PHY supports the following functions:

- Single Antenna 1x1 Stream in 20 MHz Channels
- IEEE 802.11b DSSS-CCK Modulation: 1, 2, 5.5, 11 Mbps
- IEEE 802.11g OFDM Modulation: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
- IEEE 802.11n HT Modulations MCS0-7, 20 MHz, 800 and 400 ns Guard Interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2 Mbps⁽¹⁾
- IEEE 802.11n Mixed Mode Operation
- Per Packet TX Power Control
- Advanced Channel Estimation/Equalization, Automatic Gain Control, CCA, Carrier/Symbol Recovery and Frame Detection

Note:

1. Currently, short GI is not supported by firmware. The data sheet will be updated when the feature is supported.

5.3 Radio

This section describes the properties and characteristics of the ATWINC15x0-MR210xB radio device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is ensured at a room temperature of 25°C with a derating of 2-3 dB at boundary conditions.

Measured under the following typical conditions:

- VBATT = 3.3V
- VDDIO = 3.3V
- Temperature: +25°C

Table 5-1. Features and Properties

Feature	Description
Part Number	ATWINC15x0-MR210xB
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant

Table 5-1. Features and Properties (continued)

Feature	Description
Host Interface	SPI
Dimension	21.7 x 14.7 x 2.1 mm
Frequency Range	2.412 GHz ~ 2.484 GHz (2.4 GHz ISM Band)
Number of Channels	• 11 for North America • 13 for Europe • 14 for Japan
Modulation	• 802.11b: DQPSK, DBPSK, CCK • 802.11g/n: OFDM/64-QAM, 16-QAM, QPSK, BPSK
Data Rate	802.11b: 1, 2, 5.5, 11 Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
Data Rate (20 MHz, normal GI, 800 ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps
Data Rate (20 MHz, short GI, 400 ns) ⁽¹⁾	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps
Operating temperature	-40 to +85°C
Storage temperature	-40 to +125°C
Humidity	• Operating Humidity: 10% to 95% Non-condensing • Storage Humidity: 5% to 95% Non-condensing

Note:

1. Currently, short GI is not supported by firmware. The data sheet will be updated when the feature is supported.

6. External Interfaces

The ATWINC15x0-MR210xB external interfaces include:

- I²C for debugging
- SPI for control and data transfer
- UART for debugging
- General Purpose Input/Output pins⁽¹⁾

Note:

1. Usage of the GPIO functionality is not supported by the ATWINC15x0B firmware. The data sheet will be updated once the support for this feature is added.

6.1 Interfacing with the Host Microcontroller

This section describes interfacing the ATWINC15x0-MR210xB module with the host microcontroller. The interface is comprised of a Client SPI and additional control signals, as shown in the following figure. For more information on SPI interface specification and timing, refer to the SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Figure 6-1. Interfacing with the Host Microcontroller

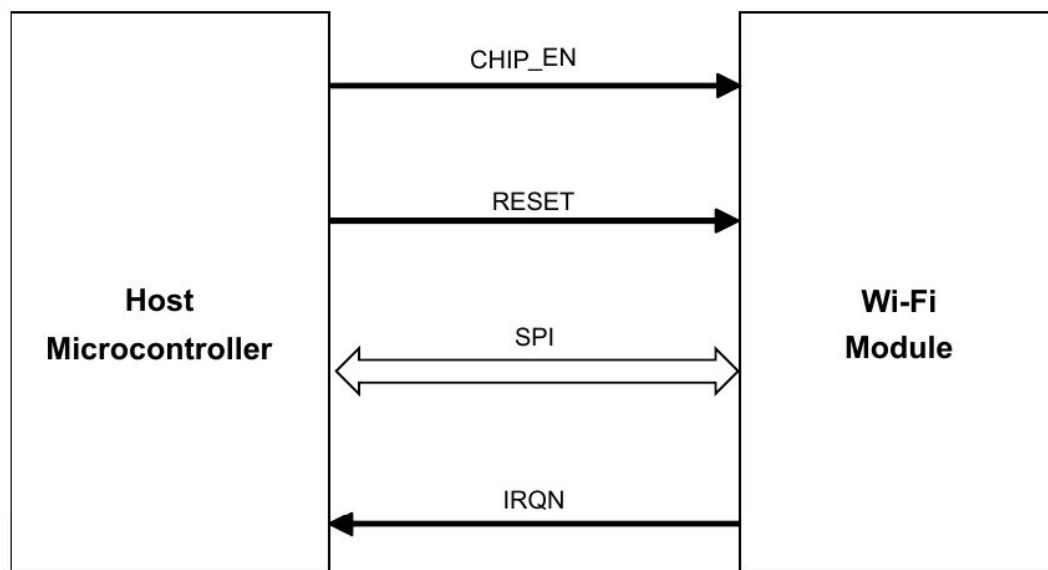


Table 6-1. Host Microcontroller Interface Pins

Pin Number	Function
4	RESET_N
13	IRQ_N
22	CHIP_EN
16	SPI_SSN
15	SPI_MOSI
17	SPI_MISO
18	SPI_SCK

Related Links[SPI Client Interface](#)

6.2 SPI Client Interface

6.2.1 Overview

The ATWINC15x0-MR210xB has a Serial Peripheral Interface (SPI) that operates as an SPI client. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in the following table. The SPI is a full-duplex client-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 6-2. SPI Interface Pin Mapping

Pin #	SPI function
10	CFG: Must be tied to VDDIO
16	SSN: Active-Low Client Select
15	MOSI (RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO (TXD): Serial Data Transmit

When the SPI is not selected, that is, when SSN is high, the SPI interface will not interfere with data transfers between the serial-host and other serial-client devices. When the serial client is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of the ATWINC15x0-MR210xB have internal programmable pull-up resistors. These resistors must be programmed to be disabled; otherwise, if any of the SPI pins are driven to a low level while the ATWINC15x0-MR210xB is in the low power sleep state, the current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

Related Links[Programmable Pull-Up Resistors](#)

6.2.2 SPI Timing

The SPI Client interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

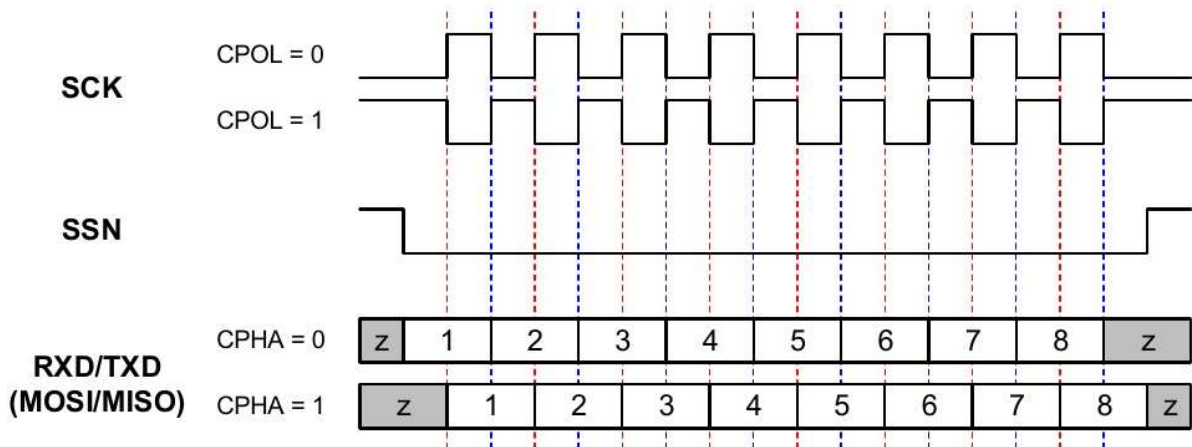
Table 6-3. SPI Client Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Note: The ATWINC15x0 firmware uses “SPI MODE 0” to communicate with the host.

The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Figure 6-2. SPI Client Clock Polarity and Clock Phase Timing



6.3 UART Interface

The ATWINC15x0-MR210xB supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface is intended for debugging purposes only. The two UART pins TXD/RXD are available on pin J14 and pin J19, respectively. The UART is compatible with the RS-232 standard.

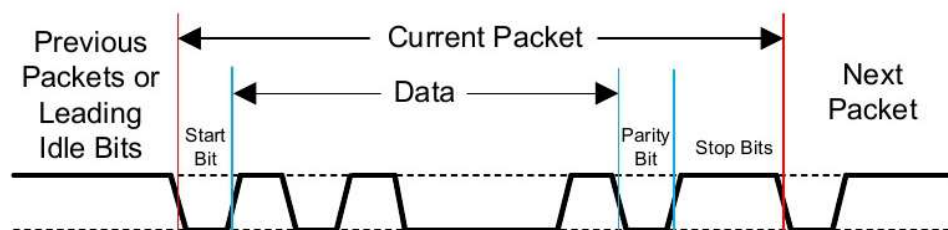
The default configuration for accessing the UART interface of ATWINC15x0-MR210xB is mentioned below:

- Baud rate: 460800
- Data: 8-bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well as the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity and two stop bits.

Figure 6-3. Example of UART RX of TX Packet



6.4 GPIO Pins

Seven General Purpose Input/Output (GPIO) pins, labeled GPIO 0 to 6, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor), where the default mode after power-up is input.

Note: Usage of the GPIO functionality is not supported by the WINC15x0 FW. The datasheet will be updated once the support for this feature is added.