40.8.10. Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							INVEN1	INVEN0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – INVENx Output Waveform x Invert Enable [x=1..0]
Bit x of INVEN[1:0] selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and I/O input pin.
1	Enable inversion of the WO[x] output and I/O input pin.

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40.8.11. Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode
This bit is not affected by a software Reset, and must not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

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40.8.12. Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]
For details on the CC channels number, refer to each TC feature list.
This bit is set when the synchronization of CCx between clock domains is started.
This bit is also set when the CCBUFx is written and cleared on the update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.
This bit is set when the synchronization of PER between clock domains is started.
This bit is also set when the PER is written and cleared on the update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.
This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.
This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.
This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of the ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of the ENABLE bit between the clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of the SWRST bit between the clock domains is complete.
This bit is set when the synchronization of the SWRST bit between the clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST is cleared by hardware.

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40.8.13. Counter Value, 8-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Note: Prior to any read access, this register must be synchronized by the user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD = READSYNC).

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – COUNT[7:0] Counter Value
These bits contain the current counter value.

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40.8.14. Period Value, 8-bit Mode

Name: PER
Offset: 0x1B
Reset: 0xFF
Property: Write-Synchronized

Note: In 8-bit mode, updating the PER register using DMA is not possible in Standby mode.

Bit	7	6	5	4	3	2	1	0
	PER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – PER[7:0] Period Value
These bits hold the value of the TC period count.

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40.8.15. Channel x Compare/Capture Value, 8-bit Mode

Name: CCx
Offset: 0x1C + x*0x01 [x=0..1]
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CC[7:0] Channel x Compare/Capture Value
These bits contain the compare/capture value in 8-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

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40.8.16. Period Buffer Value, 8-bit Mode

Name: PERBUF
Offset: 0x2F
Reset: 0xFF
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	PERBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – PERBUF[7:0] Period Buffer Value
These bits hold the value of the period buffer register. The value is copied to the PER register on the UPDATE condition.

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40.8.17. Channel x Compare Buffer Value, 8-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x01 [x=0..1]
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CCBUF[7:0] Channel x Compare Buffer Value [x=1..0]
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD = 1), the data from buffer registers is copied into the corresponding CCx register under UPDATE condition (CTRLBSET.CMD = 0x3), including the software update command.

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40.9. Register Summary - 16-bit Mode

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK	PRESCALER[2:0]		
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		CLIENT	STOP
0x0C	WAVE	7:0							WAVEGEN[1:0]	
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x11 ... 0x13	Reserved									
0x14	COUNT	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
0x16 ... 0x1B	Reserved									
0x1C	CC0	7:0	CC[7:0]							
		15:8	CC[15:8]							
0x1E	CC1	7:0	CC[7:0]							
		15:8	CC[15:8]							
0x20 ... 0x2F	Reserved									
0x30	CCBUF0	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							
0x32	CCBUF1	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							

40.10. Register Description - 16-Bit Mode

Registers can be 8, 16 or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the PAC. Optional PAC write protection is denoted by the PAC Write-Protection property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the Write-Synchronized or the Read-Synchronized property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the Enable-Protected property in each individual register description.

The following are the list of conventions available in the register description:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'

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- -n = Value at POR
- 1 = Bit is set
- 0 = Bit is cleared
- x = Bit is unknown
- HS = Hardware Set
- HC = Hardware Cleared

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40.10.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
	DMAOS				ALOCK	PRESCALER[2:0]		
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3	—	Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3	—	Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable [x=1..0]
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input. This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable [x=1..0]
Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

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These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit generates a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit generates DMA triggers on each TC cycle.
This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.
This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.
These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.
In Standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.
This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC continues to request the clock when its operation is stopped (STATUS.STOP = 1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in Standby mode.
This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

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Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter must wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.
These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	—	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the Counter mode.
These bits are not synchronized.

Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	—	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is a delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE reads back immediately and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) is set. SYNCBUSY.ENABLE is cleared when the operation is complete.
This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.
Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state and the TC is disabled.
Writing a '1' to CTRLA.SWRST always takes precedence; all other writes in the same write-operation are discarded.
This bit is not enable-protected.

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40.10.2. Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
Writing '0x0' to these bits has no effect.
Writing a '1' to any of these bits clears the pending command.

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit disables one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no update of the registers with the value of its buffered register is performed on the hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before a hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when the input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

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40.10.3. Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-synchronized, Write-Synchronized

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command is executed, the CMD bit group is read back as '0'.

Writing '0x0' to these bits has no effect.

Writing a value different from '0x0' to these bits issues a command for execution.

Important: This command requires synchronization before executing it. The following is a valid sequence:

- Issue CMD command (CTRLBSET.CMD = command)
- Wait for CMD synchronization (SYNCBUSY.CTRLB = 0)
- Wait for CMD read back as zero (CTRLBSET.CMD = 0)

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command is executed, the CMD bit group is read back as '0'.
Writing '0x0' to these bits has no effect.
Writing a value different from '0x0' to these bits issues a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit enables one-shot operation.

Value	Description
0	The TC wraps around and continue counting on an overflow/underflow condition.
1	The TC wraps around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no update of the registers with a value of its buffered register is performed on the hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before a hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

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Writing a '0' to this bit has no effect.
Writing a '1' to this bit sets the LUPD bit.
This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit sets the bit and make the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

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40.10.4. Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV		EVACT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEOx Match or Capture Channel x Event Output Enable [x = 1..0]
These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable
This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable
This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity
This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action
These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1

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Value	Name	Description
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

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40.10.5. Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable [x = 1..0]
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

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40.10.6. Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable [x = 1..0]
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will set the corresponding Match or Capture Channel x Interrupt Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

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40.10.7. Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x [x = 1..0]
This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.
Writing a '0' to these bits has no effect.
Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag
In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR Error Interrupt Flag
This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is no place to store the new capture.
Writing a '0' to these bits has no effect.
Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag
This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.
Writing a '0' to these bits has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

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40.10.8. Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized

Bit	7	6	5	4	3	2	1	0
			CCBUFV1	CCBUFV0	PERBUFV		CLIENT	STOP
Access			R/W	R/W	R/W		R	R
Reset			0	0	0		0	1

Bits 4, 5 – CCBUFVx Channel x Compare or Capture Buffer Valid [x=1..0]
For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register.
The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.
For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register. The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid
This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set or automatically cleared by hardware on the UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – CLIENT Client Status Flag
This bit is only available in 32-bit mode on the Client TC (in other words, TC1, TC3, TC5, TC7 and/or TC9). The bit is set when the associated Host TC (TC0, TC2, TC4, TC6 and/or TC8, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag
This bit is set when the TC is disabled, on a Stop command or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

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40.10.9. Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode
These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation must be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.
These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode, it is the respective MAX value.

Related Links
Waveform Output Operations

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40.10.10. Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							INVEN1	INVEN0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – INVENx Output Waveform x Invert Enable [x=1..0]
Bit x of INVEN[1:0] selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and I/O input pin.
1	Enable inversion of the WO[x] output and I/O input pin.

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40.10.11. Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode
This bit is not affected by a software Reset, and must not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

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40.10.12. Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]
For details on the CC channels number, refer to each TC feature list.
This bit is set when the synchronization of CCx between clock domains is started.
This bit is also set when the CCBUFx is written and cleared on the update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.
This bit is set when the synchronization of PER between clock domains is started.
This bit is also set when the PER is written and cleared on the update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.
This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.
This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.
This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of the ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of the ENABLE bit between the clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of the SWRST bit between the clock domains is complete.
This bit is set when the synchronization of the SWRST bit between the clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST is cleared by hardware.

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40.10.13. Counter Value, 16-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Note: Prior to any read access, this register must be synchronized by the user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD = READSYNC).

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0] Counter Value
These bits contain the current counter value.

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40.10.14. Channel x Compare/Capture Value, 16-bit Mode

Name: CCx
Offset: 0x1C + x*0x02 [x=0..1]
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	CC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CC[15:0] Channel x Compare/Capture Value [x=1..0]
These bits contain the compare/capture value in 16-bit TC mode. In Match Frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

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40.10.15. Channel x Compare Buffer Value, 16-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x02 [x=0..1]
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	CCBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CCBUF[15:0] Channel x Compare Buffer Value [x=1..0]
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD = 1), the data from buffer registers is copied into the corresponding CCx register under the UPDATE condition (CTRLBSET.CMD = 0x3) including the software update command.

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40.11. Register Summary - 32-bit Mode

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK	PRESCALER[2:0]		
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0		CMD[2:0]				ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		CLIENT	STOP
0x0C	WAVE	7:0							WAVEGEN[1:0]	
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x11 ... 0x13	Reserved									
0x14	COUNT	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
		23:16	COUNT[23:16]							
		31:24	COUNT[31:24]							
0x18 ... 0x1B	Reserved									
0x1C	CC0	7:0	CC[7:0]							
		15:8	CC[15:8]							
		23:16	CC[23:16]							
		31:24	CC[31:24]							
0x20	CC1	7:0	CC[7:0]							
		15:8	CC[15:8]							
		23:16	CC[23:16]							
		31:24	CC[31:24]							
0x24 ... 0x2F	Reserved									
0x30	CCBUF0	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							
		23:16	CCBUF[23:16]							
		31:24	CCBUF[31:24]							
0x34	CCBUF1	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							
		23:16	CCBUF[23:16]							
		31:24	CCBUF[31:24]							

40.12. Register Description - 32-Bit Mode

Registers can be 8, 16 or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the PAC. Optional PAC write protection is denoted by the PAC Write-Protection property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the Write-Synchronized or the Read-Synchronized property in each individual register description.

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Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the Enable-Protected property in each individual register description.

The following are the list of conventions available in the register description:

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- 1 = Bit is set
- 0 = Bit is cleared
- x = Bit is unknown
- HS = Hardware Set
- HC = Hardware Cleared

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40.12.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
	DMAOS				ALOCK	PRESCALER[2:0]		
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3	—	Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3	—	Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable [x=1..0]
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input. This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable [x=1..0]
Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

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These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit generates a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit generates DMA triggers on each TC cycle.
This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.
This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.
These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.
In Standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.
This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC continues to request the clock when its operation is stopped (STATUS.STOP = 1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in Standby mode.
This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

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Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter must wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.
These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	—	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the Counter mode.
These bits are not synchronized.

Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	—	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is a delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE reads back immediately and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) is set. SYNCBUSY.ENABLE is cleared when the operation is complete.
This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.
Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state and the TC is disabled.
Writing a '1' to CTRLA.SWRST always takes precedence; all other writes in the same write-operation are discarded.
This bit is not enable-protected.

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40.12.2. Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
Writing '0x0' to these bits has no effect.
Writing a '1' to any of these bits clears the pending command.

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit disables one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no update of the registers with the value of its buffered register is performed on the hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before a hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when the input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

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40.12.3. Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-synchronized, Write-Synchronized

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command is executed, the CMD bit group is read back as '0'.

Writing '0x0' to these bits has no effect.

Writing a value different from '0x0' to these bits issues a command for execution.

Important: This command requires synchronization before executing it. The following is a valid sequence:

- Issue CMD command (CTRLBSET.CMD = command)
- Wait for CMD synchronization (SYNCBUSY.CTRLB = 0)
- Wait for CMD read back as zero (CTRLBSET.CMD = 0)

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command is executed, the CMD bit group is read back as '0'.
Writing '0x0' to these bits has no effect.
Writing a value different from '0x0' to these bits issues a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit enables one-shot operation.

Value	Description
0	The TC wraps around and continue counting on an overflow/underflow condition.
1	The TC wraps around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no update of the registers with a value of its buffered register is performed on the hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before a hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

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Writing a '0' to this bit has no effect.
Writing a '1' to this bit sets the LUPD bit.
This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit sets the bit and make the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

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40.12.4. Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV		EVACT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEOx Match or Capture Channel x Event Output Enable [x = 1..0]
These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable
This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable
This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity
This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action
These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1

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Value	Name	Description
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

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40.12.5. Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable [x = 1..0]
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

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40.12.6. Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable [x = 1..0]
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will set the corresponding Match or Capture Channel x Interrupt Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

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40.12.7. Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x [x = 1..0]
This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.
Writing a '0' to these bits has no effect.
Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag
In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR Error Interrupt Flag
This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is no place to store the new capture.
Writing a '0' to these bits has no effect.
Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag
This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.
Writing a '0' to these bits has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

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40.12.8. Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized

Bit	7	6	5	4	3	2	1	0
			CCBUFV1	CCBUFV0	PERBUFV		CLIENT	STOP
Access			R/W	R/W	R/W		R	R
Reset			0	0	0		0	1

Bits 4, 5 – CCBUFVx Channel x Compare or Capture Buffer Valid [x=1..0]
For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register.
The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.
For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register. The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid
This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set or automatically cleared by hardware on the UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – CLIENT Client Status Flag
This bit is only available in 32-bit mode on the Client TC (in other words, TC1, TC3, TC5, TC7 and/or TC9). The bit is set when the associated Host TC (TC0, TC2, TC4, TC6 and/or TC8, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag
This bit is set when the TC is disabled, on a Stop command or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

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40.12.9. Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode
These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation must be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.
These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode, it is the respective MAX value.

Related Links
Waveform Output Operations

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40.12.10. Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							INVEN1	INVEN0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – INVENx Output Waveform x Invert Enable [x=1..0]
Bit x of INVEN[1:0] selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and I/O input pin.
1	Enable inversion of the WO[x] output and I/O input pin.

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40.12.11. Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode
This bit is not affected by a software Reset, and must not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

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40.12.12. Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]
For details on the CC channels number, refer to each TC feature list.
This bit is set when the synchronization of CCx between clock domains is started.
This bit is also set when the CCBUFx is written and cleared on the update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.
This bit is set when the synchronization of PER between clock domains is started.
This bit is also set when the PER is written and cleared on the update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.
This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.
This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.
This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of the ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of the ENABLE bit between the clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of the SWRST bit between the clock domains is complete.
This bit is set when the synchronization of the SWRST bit between the clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST is cleared by hardware.

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40.12.13. Counter Value, 32-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Note: Prior to any read access, this register must be synchronized by the user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD = READSYNC).

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0] Counter Value
These bits contain the current counter value.

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40.12.14. Channel x Compare/Capture Value, 32-bit Mode

Name: CCx
Offset: 0x1C + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	CC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CC[31:0] Channel x Compare/Capture Value [x=1..0]
These bits contain the compare/capture value in 32-bit TC mode. In Match Frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

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40.12.15. Channel x Compare Buffer Value, 32-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	CCBUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CCBUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CCBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CCBUF[31:0] Channel x Compare Buffer Value [x=1..0]
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD = 1), the data from buffer registers is copied into the corresponding CCx register under the UPDATE condition (CTRLBSET.CMD = 0x3), including the software update command.

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41. Timer/Counter for Control Applications (TCC)

41.1. Overview

The device provides three instances of the Timer/Counter for Control Applications (TCC).

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to time stamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation, such as frequency generation and pulse-width modulation.

Waveform extensions are featured for motor control, ballast, LED, H-bridge, power converters and other types of power control applications. They allow for low-side and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut-down of external drivers.

Note: The TCC configurations, such as channel numbers and features, can be reduced for some of the TCC instances.

Table 41-1. TCC Specific Configuration

TCC No.	Counter Size (SIZE)	Link Role (Host_Client_MODE) (0 = NA, 1 = Host, 2 = Client)	Channels (CC_NUM)	Pins WO_NUM (OW_NUM)
0	24	1	6	6
1	24	2	6	6
2	16	0	2	2

41.2. Features

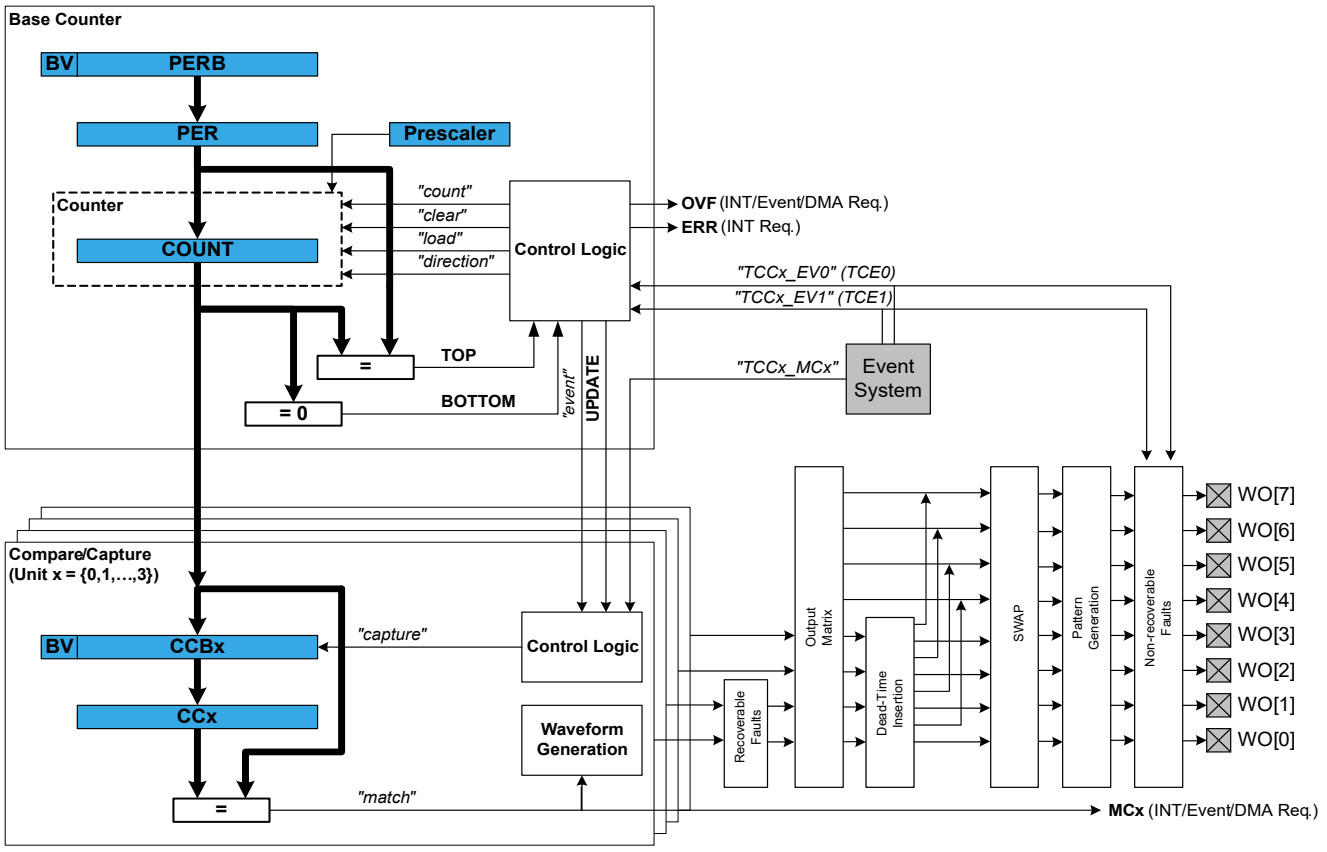
- Up to Six Compare/Capture Channels (CC) with:
  - Double buffered period setting
  - Double buffered compare or capture channel
  - Circular buffer on period and compare channel registers
- Waveform Generation:
  - Frequency generation
  - Single-slope pulse-width modulation (PWM)
  - Dual-slope PWM with half-cycle reload capability
- Input Capture:
  - Event capture
  - Frequency capture
  - Pulse-width capture
- Waveform Extensions:
  - Configurable distribution of compare channels outputs across port pins
  - Low-side and high-side output with programmable dead-time insertion
  - Waveform swap option with double buffer support
  - Pattern generation with double buffer support
  - Dithering support
- Fault Protection for Safe Disabling of Drivers:
  - Two recoverable fault sources

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  - Two non-recoverable fault sources
  - Debugger can be a source of non-recoverable fault
- Input Events:
  - Two input events (EVx) for counter
  - One input event (MCx) for each channel
- Output Events:
  - Three output events (Count, re-trigger and overflow) are available for counter
  - One compare match/input capture event output for each channel
- Interrupts:
  - Overflow and re-trigger interrupt
  - Compare match/input capture interrupt
  - Interrupt on fault detection

41.3. Block Diagram

Figure 41-1. Timer/Counter for Control Applications - Block Diagram



41.4. Signal Description

Table 41-2. Signal Description

Pin Name	Type	Description
TCCx/WO[0]	Digital output	Compare channel 0 waveform output
TCCx/WO[1]	Digital output	Compare channel 1 waveform output

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Table 41-2. Signal Description (continued)

Pin Name	Type	Description
...	...	...
TCCx/WO[WO_NUM-1]	Digital output	Compare channel n waveform output

See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

I/O Ports and Peripheral Pin Select (PPS)

41.5. Product Dependencies

The following sections describe how the other parts of the system must be configured correctly to use this peripheral.

41.5.1. I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Peripheral Pin Select (PPS).

41.5.2. Power Management

This peripheral can continue to operate in any sleep mode (Idle, Standby Sleep) where its source clock is running. The interrupts can wake up the device from the sleep modes. Events connected to the event system can trigger other operations in the system without exiting the sleep modes.

41.5.3. Clocks

A generic clock (GCLK_TCCx) is required to clock the TCC. This clock must be configured and enabled in the generic clock controller before using the TCC.
Note: TCC1 and TCC2 share a single peripheral clock generator.

The generic clocks (GCLK_TCCx) are asynchronous to the bus clock (PB1_CLK). Due to this asynchronicity, writing certain registers requires synchronization between the clock domains.

41.5.4. DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral, the DMAC must be configured first (see *Direct Memory Access Controller (DMAC)* from Related Links).

Related Links

Direct Memory Access Controller (DMAC)

41.5.5. Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links

Nested Vector Interrupt Controller (NVIC)
Nested Vector Interrupt Controller (NVIC)

41.5.6. Events

The events of this peripheral are connected to the Event System.

41.5.7. Debug Operation

When the CPU is halted in Debug mode, this peripheral halts normal operation. This peripheral can be forced to continue operation during debugging. See the *DBGCTRL* register from Related Links.

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Related Links

DBGCTRL

Debug control

41.5.8. Register Access Protection

Registers with write access can be optionally write protected by the PAC, except for the following:

- Interrupt Flag register (INTFLAG)
- Status register (STATUS)
- Period and Period Buffer registers (PER, PERB)
- Compare/Capture and Compare/Capture Buffer registers (CCx, CCBx)
- Control Waveform register (WAVE)
- Pattern Generation Value and Pattern Generation Value Buffer registers (PATT, PATTB)

Note: Optional write protection is indicated by the PAC Write Protection property in the register description.

Write protection does not apply for accesses through an external debugger.

41.5.9. Analog Connections

Not applicable.

41.6. Functional Description

41.6.1. Principle of Operation

The following definitions are used throughout the documentation:

Table 41-3. Timer/Counter for Control Applications – Definitions

Name	Description
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be the same as Period (PER) or the Compare Channel 0 (CC0) register value depending on the Waveform Generator mode in Waveform Output Operations. See *Waveform Output Generation Operations* from Related Links.
ZERO	The counter reaches ZERO when it contains all zeros.
MAX	The counter reaches maximum when it contains all ones.
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source.
Counter	The clock control is handled externally (e.g., counting external events).
CC	For compare operations, the CC are referred to as "compare channels." For capture operations, the CC are referred to as "capture channels."

Each TCC instance has up to six compare/capture channels (CCx).

The Counter register (COUNT), Period registers with Buffer (PER and PERB), and Compare and Capture registers with buffers (CCx and CCBx) are 16- or 24-bit registers, depending on each TCC instance. Each Buffer register has a Buffer Valid (BUFV) flag that indicates when the buffer contains a new value.

Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached TOP or ZERO. In either case, the TCC can generate interrupt requests or generate events for the Event System. In Waveform Generator mode, these comparisons are used to set the waveform period or pulse width.

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A prescaled generic clock (GCLK_TCCx) and events from the event system can be used to control the counter. The event system is also used as a source to the input capture.

The Recoverable Fault Unit enables event-controlled waveforms by acting directly on the generated waveforms of the TCC compare channels output. These events can restart, halt the timer/counter period, shorten the output pulse active time, or disable waveform output as long as the fault condition is present. This can typically be used for current sensing regulation, and zero-crossing and demagnetization re-triggering.

The MCE0 and MCE1 asynchronous event sources are shared with the recoverable fault unit. Only asynchronous events are used internally when fault unit extension is enabled. See *Event System (EVSYS)* from Related Links for further details on how to configure asynchronous events routing.

Recoverable fault sources can be filtered and/or windowed to avoid false triggering, for example from I/O pin glitches, by using digital filtering, input blanking and qualification options. See *Recoverable Faults* from Related Links.

In order to support applications with different types of motor control, ballast, LED, H-bridge, power converter and other types of power switching applications, the following independent units are implemented in some of the TCC instances as optional and successive units:

- Recoverable faults and non-recoverable faults
- Output matrix
- Dead-time insertion
- Swap
- Pattern generation

See *Timer/Counter for Control Applications - Block Diagram* in the *Block Diagram* from Related Links.

The output matrix (OTMX) can distribute and route out the TCC waveform outputs across the port pins in different configurations, each optimized for different application types. The Dead-Time Insertion (DTI) unit splits the four lower OTMX outputs into two non-overlapping signals: the non-inverted Low Side (LS) and inverted High Side (HS) of the waveform output with optional dead-time insertion between LS and HS switching. The SWAP unit can swap the LS and HS pin outputs and can be used for fast decay motor control.

The pattern generation unit can be used to generate synchronized waveforms with constant logic level on TCC UPDATE conditions. This is useful for easy stepper motor and full bridge control.

The non-recoverable fault module enables event-controlled fault protection by acting directly on the generated waveforms of the timer/counter compare channel outputs. When a non-recoverable fault condition is detected, the output waveforms are forced to a preconfigured value that is safe for the application. This is typically used for instant and predictable shut-down and disabling high current or voltage drives.

The count event sources (TCE0 and TCE1) are shared with the non-recoverable fault extension. The events can be optionally filtered. If the filter options are not used, the non-recoverable faults provide an immediate asynchronous action on waveform output, even for cases where the clock is not present. See *Event System (EVSYS)* from Related Links for further details on how to configure asynchronous events routing.

Related Links

Event System (EVSYS)
Block Diagram
Recoverable Faults
Waveform Output Generation Operations

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41.6.2. Basic Operation

41.6.2.1. Initialization

The following registers are enable-protected, meaning that they can only be written when the TCC is disabled (CTRLA.ENABLE=0):

- Control A (CTRLA) register, except Run Standby (RUNSTDBY), Enable (ENABLE) and Software Reset (SWRST) bits
- Recoverable Fault n Control registers (FCTRLA and FCTRLB)
- Waveform Extension Control register (WEXCTRL)
- Drive Control register (DRVCTRL)
- Event Control register (EVCTRL)

Enable-protected bits in the CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'. Enable-protection is denoted by the "Enable-Protected" property in the register description.

Before the TCC is enabled, it must be configured as outlined by the following steps:

1. Enable the TCC bus clock if not already enabled by default (PB1_CLK).
2. If Capture mode is required, enable the channel in Capture mode by writing a '1' to the Capture Enable bit in the Control A register (CTRLA.CPTEN).

Optionally, the following configurations can be set before enabling TCC:

1. Select PRESCALER setting in the Control A register (CTRLA.PRESCALER).
2. Select Prescaler Synchronization setting in Control A register (CTRLA.PRESCSYNC).
3. If down-counting operation is desired, write the Counter Direction bit in the Control B Set register (CTRLBSET.DIR) to '1'. In this case, the COUNT register must be initialized with the desired TOP value.
4. Select the Waveform Generation operation in the WAVE register (WAVE.WAVEGEN).
5. Select the Waveform Output Polarity in the WAVE register (WAVE.POL).
6. The waveform output can be inverted for the individual channels using the Waveform Output Invert Enable bit group in the Driver register (DRVCTRL.INVEN). To ensure deterministic operation, the configuration of the TCC module should always be set/checked programmatically before operation is enabled.

41.6.2.2. Enabling, Disabling and Resetting

The TCC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TCC is disabled by writing a '0' to CTRLA.ENABLE.

The TCC is reset by writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TCC, except DBGCTRL, are reset to their initial state and the TCC is disabled. See the *CTRLA* register from Related Links.

The TCC must be disabled before the TCC is reset to avoid undefined behavior.

41.6.2.3. Prescaler Selection

The GCLK_TCCx clock is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

If the prescaler value is higher than one, the Counter Update condition can be optionally executed on the next GCLK_TCCx clock pulse or the next prescaled clock pulse. For further details, refer to the Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) descriptions.

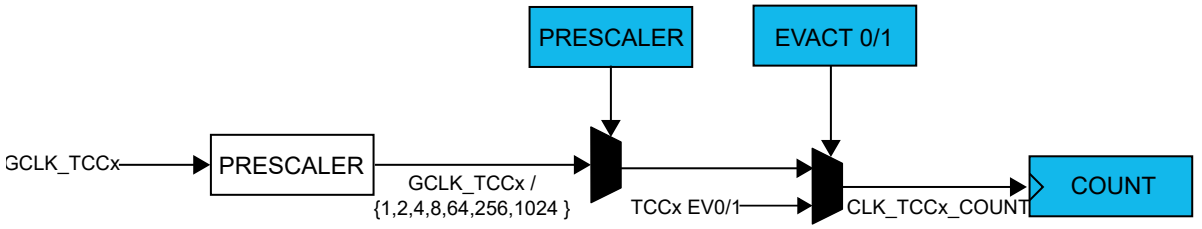
Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

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Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TCCx_COUNT.

Figure 41-2. Prescaler



41.6.2.4. Counter Operation

Depending on the mode of operation, the counter is cleared, reloaded, incremented or decremented at each TCC clock input (CLK_TCCx_COUNT). A counter clear or reload mark the end of the current counter cycle and the start of a new one.

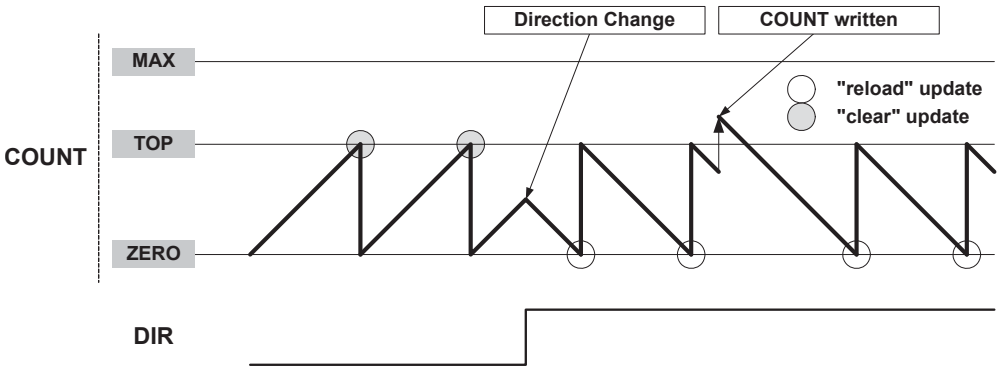
The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If the bit is zero, it is counting up, and, if the bit is one, it is counting down.

The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it is counting up and TOP is reached, the counter is set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) is set. When down-counting, the counter is reloaded with the TOP value when ZERO is reached (underflow) and INTFLAG.OVF is set.

Note: When down-counting, the COUNT register must be initialized to TOP value (PER or CC0 value depending on the mode).

INTFLAG.OVF can be used to trigger an interrupt or an event. An overflow/underflow occurrence (in other words, a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT). The One-Shot feature is explained in the Additional Features section.

Figure 41-3. Counter Operation



It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. The COUNT value will always be ZERO or TOP, depending on the direction set by CTRLBSET.DIR or CTRLBCLR.DIR, when starting the TCC, unless a different value was written to it or the TCC was stopped at a value other than ZERO. The write access has higher priority than count, clear or reload. The direction of the counter can also be changed during normal operation. See Figure 41-3 for more information.

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41.6.2.4.1. Stop Command

A Stop command can be issued from software by using Command bits in the Control B Set register (CTRLBSET.CMD = 0x2, STOP). When a Stop is detected while the counter is running, the counter will get set to bottom/top depending on the direction: up/down. All waveforms are cleared, and the Stop bit in the Status register is set (STATUS.STOP).

41.6.2.4.2. Pause Event Action

A pause command can be issued when the stop event action is configured in the Input Event Action 1 bits in Event Control register (EVCTRL.EVACT1 = 0x3, STOP).

When a pause is detected, the counter can stop immediately maintaining its current value and all waveforms keep their current state until a start event action is detected: Input Event Action 0 bits in Event Control register (EVCTRL.EVACT0 = 0x3, START).

41.6.2.4.3. Re-Trigger Command and Event Action

A re-trigger command can be issued from software by using TCC Command bits in the Control B Set register (CTRLBSET.CMD = 0x1, RETRIGGER) or from an event when the re-trigger event action is configured in the Input Event 0/1 Action bits in Event Control register (EVCTRL.EVACTn = 0x1, RETRIGGER).

When the command is detected during the counting operation, the counter will be reloaded or cleared depending on the counting direction (CTRLBSET.DIR or CTRLBCLR.DIR). When the re-trigger command is detected while the counter is stopped, the counter will resume counting from the current value in the COUNT register.

Note: When a re-trigger event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACTn = 0x1, RETRIGGER), enabling the counter will not start the counter. The counter starts on the next incoming event and restarts on the corresponding following event.

41.6.2.4.4. Start Event Action

The start action can be selected in the Event Control register (EVCTRL.EVACT0 = 0x3, START) and can start the counting operation when previously stopped. The event has no effect if the counter is already counting. When the module is enabled, the counter operation starts when the event is received or when a re-trigger software command is applied.

Note: When a start event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACT0 = 0x3, START), enabling the counter will not start the counter. The counter starts on the next incoming event, but it will not restart on subsequent events.

41.6.2.4.5. Count Event Action

The TCC can count events. When an event is received, the counter increases or decreases the value depending on the direction settings (CTRLBSET.DIR or CTRLBCLR.DIR).

The count event action is selected by the Event Action 0 bit group in the Event Control register (EVCTRL.EVACT0 = 0x5, COUNT).

41.6.2.4.6. Direction Event Action

The direction event action can be selected in the Event Control register (EVCTRL.EVACT1 = 0x2, DIR). When this event is used, the asynchronous event path specified in the event system must be configured or selected. The direction event action can be used to control the direction of the counter operation depending on external events level. When received, the event level overrides the Direction settings (CTRLBSET.DIR or CTRLBCLR.DIR) and the direction bit value is updated accordingly.

41.6.2.4.7. Increment Event Action

The increment event action can be selected in the Event Control register (EVCTRL.EVACT0 = 0x4, INC) and can change the Counter state when an event is received. When the TCE0 event (TCCx_EV0) is received, the counter increments regardless of the direction setting (CTRLBSET.DIR or CTRLBCLR.DIR).

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41.6.2.4.8. Decrement Event Action

The decrement event action can be selected in the Event Control register (EVCTRL.EVACT1 = 0x4, DEC) and can change the Counter state when an event is received. When the TCE1 (TCCx_EV1) event is received, the counter decrements regardless of the direction setting (CTRLBSET.DIR or CTRLBCLR.DIR).

41.6.2.4.9. Non-Recoverable Fault Event Action

Non-recoverable fault actions can be selected in the Event Control register (EVCTRL.EVACTn = 0x7, FAULT). When received, the counter is stopped and the output of the compare channels is overridden according to the Driver Control register settings (DRVCTRL.NREx and DRVCTRL.NRVx). TCE0 and TCE1 must be configured as asynchronous events.

41.6.2.4.10. Event Action Off

If the event action is disabled (EVCTRL.EVACTn = 0x0, OFF), enabling the counter will also start the counter.

41.6.2.5. Compare Operations

By default, the Compare/Capture channel is configured for compare operations. To perform capture operations, it must be re-configured.

When using the TCC with the Compare/Capture Value registers (CCx) for compare operations, the counter value is continuously compared to the values in the CCx registers. This can be used for timer or for waveform operation.

The Channel x Compare/Capture Buffer Value (CCBx) registers provide double buffer capability. The double buffering synchronizes the update of the CCx register with the buffer value at the UPDATE condition or a force update command (CTRLBSET.CMD = 0x3, UPDATE). See *Double Buffering* from Related Links. The synchronization prevents the occurrence of odd-length, non-symmetrical pulses and ensures glitch-free output.

Related Links

Double Buffering

41.6.2.5.1. Waveform Output Generation Operations

The compare channels can be used for waveform generation on output port pins. To make the waveform available on the connected pin, the following requirements must be fulfilled:

1. Choose a Waveform Generation mode in the Waveform Generation Operation bit in Waveform register (WAVE.WAVEGEN).
2. Optionally, invert the waveform output WO[x] by writing the corresponding Waveform Output x Inversion bit in the Driver Control register (DRVCTRL.INVENx).
3. Configure the pins with the I/O Pin Controller. See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.
   Note: Event must not be used when the compare channel is set in waveform output operating mode.

The counter value is continuously compared with each CCx value. On a comparison match, the Match or Capture Channel x bit in the Interrupt Flag Status and Clear register (INTFLAG.MCx) will be set on the next zero-to-one transition of CLK_TCC_COUNT (see Normal Frequency Operation). An interrupt and/or event can be generated on the same condition if Match/Capture occurs, i.e., INTENSET.MCx and/or EVCTRL.MCEOx is '1'. Both interrupt and event can be generated simultaneously.

There are seven waveform configurations for the Waveform Generation Operation bit group in the Waveform register (WAVE.WAVEGEN). This will influence how the waveform is generated and impose restrictions on the top value. The configurations are:

- Normal Frequency (NFRQ)

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- Match Frequency (MFRQ)
- Normal Pulse-Width Modulation (NPWM)
- Dual-slope, interrupt/event at TOP (DSTOP)
- Dual-slope, interrupt/event at ZERO (DSBOTTOM)
- Dual-slope, interrupt/event at Top and ZERO (DSBOTH)
- Dual-slope, critical interrupt/event at ZERO (DSCRITICAL)

When using MFRQ configuration, the TOP value is defined by the CC0 register value. For the other waveform operations, the TOP value is defined by the Period (PER) register value.

For dual-slope waveform operations, the update time occurs when the counter reaches ZERO. For the other Waveforms Generation modes, the update time occurs on counter wraparound, on overflow, underflow or re-trigger.

The table below shows the update counter and overflow event/interrupt generation conditions in different operation modes.

Table 41-4. Counter Update and Overflow Event/interrupt Conditions

Name	Operation	TOP	Update	Output Waveform		OVFIF/Event	
				On Match	On Update	Up	Down
NFRQ	Normal Frequency	PER	TOP/ ZERO	Toggle	Stable	TOP	ZERO
MFRQ	Match Frequency	CC0	TOP/ ZERO	Toggle	Stable	TOP	ZERO
NPWM	Single-slope PWM	PER	TOP/ ZERO	See section 'Output Polarity' below		TOP	ZERO
DSCRITICAL	Dual-slope PWM	PER	ZERO			—	ZERO
DSBOTTOM	Dual-slope PWM	PER	ZERO			—	ZERO
DSBOTH	Dual-slope PWM	PER	TOP(1) & ZERO			TOP	ZERO
DSTOP	Dual-slope PWM	PER	ZERO			TOP	—

1. The UPDATE condition on TOP only will occur when circular buffer is enabled for the channel.

Related Links

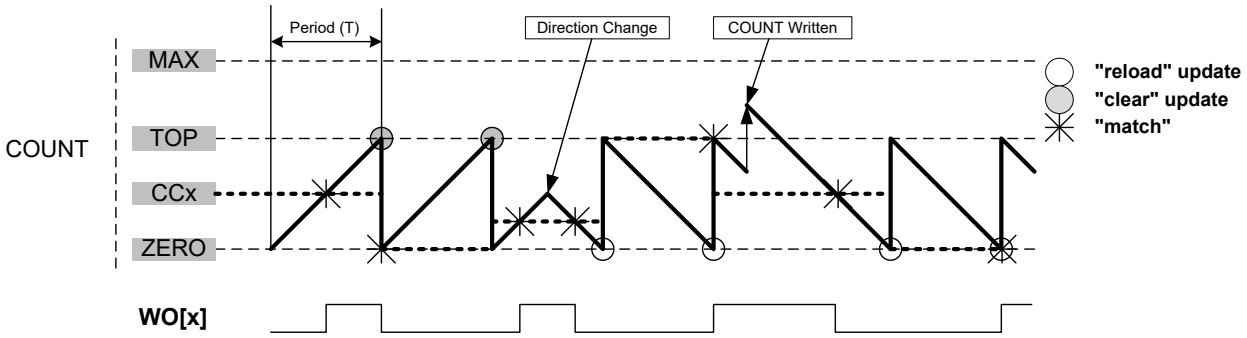
I/O Ports and Peripheral Pin Select (PPS)

41.6.2.5.2. Normal Frequency (NFRQ)

For Normal Frequency generation, the period time (T) is controlled by the period register (PER). The waveform generation output (WO[x]) is toggled on each compare match between COUNT and CCx, and the corresponding Match or Capture Channel x Interrupt Flag (EVCTRL.MCEOx) will be set.

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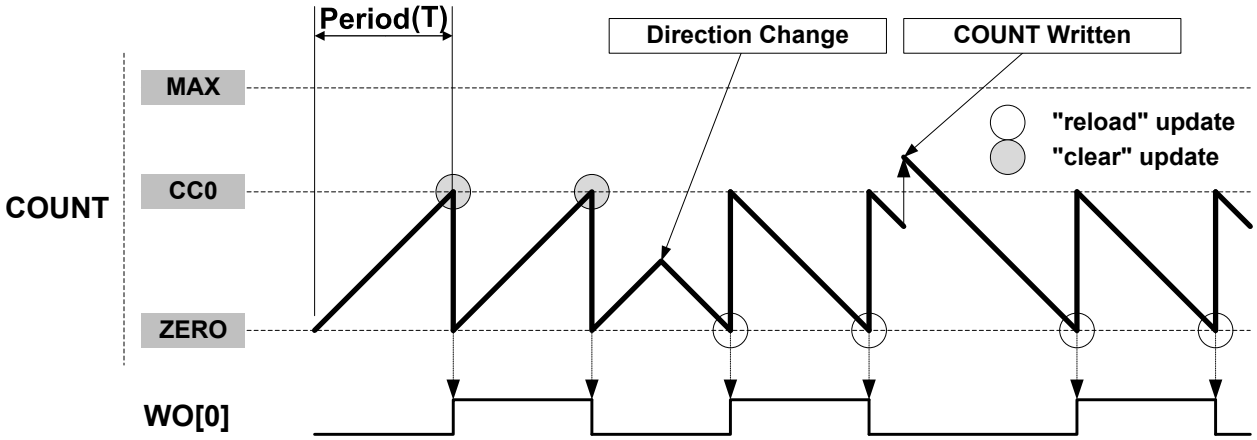
Figure 41-4. Normal Frequency Operation



41.6.2.5.3. Match Frequency (MFRQ)

For Match Frequency generation, the period time (T) is controlled by CC0 register instead of PER. WO[0] toggles on each update condition.

Figure 41-5. Match Frequency Operation



41.6.2.5.4. Normal Pulse-Width Modulation (NPWM)

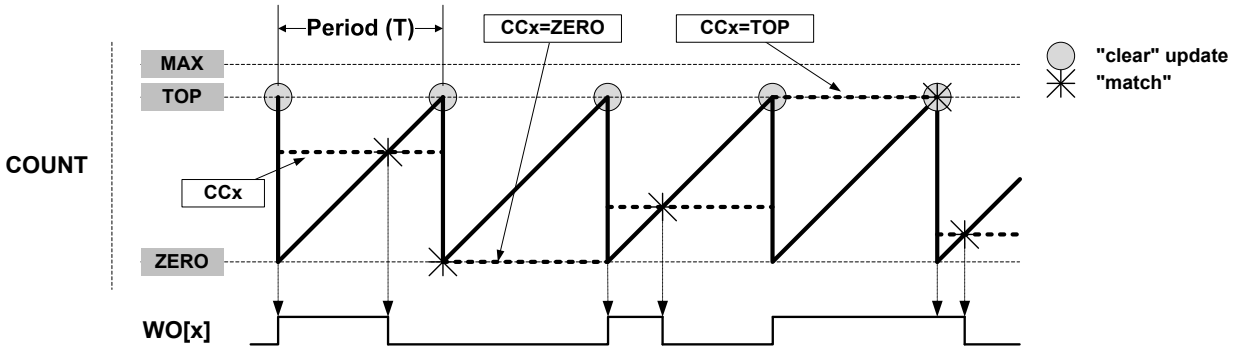
NPWM uses single-slope PWM generation.

41.6.2.5.5. Single-Slope PWM Operation

For single-slope PWM generation, the period time (T) is controlled by Top value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

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Figure 41-6. Single-Slope PWM Operation



The following equation calculates the exact resolution for a single-slope PWM (R_{PWM_SS}) waveform:

$$R_{PWM\_SS} = \frac{\log(TOP+1)}{\log(2)}$$

The PWM frequency depends on the Period register value (PER) and the peripheral clock frequency (f_{GCLK_TCCx}), and can be calculated by the following equation:

$$f_{PWM\_SS} = \frac{f_{GCLK\_TCCx}}{N(TOP+1)}$$

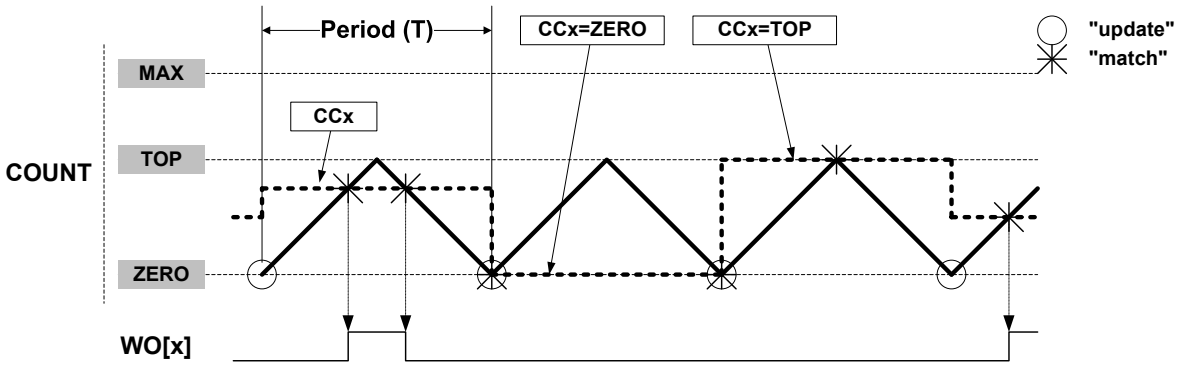
Where N represents the prescaler divider used (1, 2, 4, 8, 16, 64, 256, 1024).

41.6.2.5.6. Dual-Slope PWM Generation

For dual-slope PWM generation, the period setting (TOP) is controlled by PER, while CCx control the duty cycle of the generated waveform output. The figure below shows how the counter repeatedly counts from ZERO to PER and then from PER to ZERO. The waveform generator output is set on compare match when up-counting, and cleared on compare match when down-counting. An interrupt and/or event is generated on TOP (when counting upwards) and/or ZERO (when counting up or down).

In DSBOTH operation, the circular buffer must be enabled to enable the update condition on TOP.

Figure 41-7. Dual-Slope Pulse Width Modulation



Using dual-slope PWM results in a lower maximum operation frequency compared to single-slope PWM generation. The period (TOP) defines the PWM resolution. The minimum resolution is 1 bit (TOP=0x00000001).

The following equation calculates the exact resolution for dual-slope PWM (R_{PWM_DS}):

$$R_{PWM\_DS} = \frac{\log(PER+1)}{\log(2)}.$$

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The PWM frequency f_{PWM_DS} depends on the period setting (TOP) and the peripheral clock frequency f_{GCLK_TCCx}, and can be calculated by the following equation:

$$f_{PWM\_DS} = \frac{f_{GCLK\_TCCx}}{2N \cdot PER}$$

N represents the prescaler divider used. The waveform generated will have a maximum frequency of half of the TCC clock frequency (f_{GCLK_TCCx}) when TOP is set to 0x00000001 and no prescaling is used.

The pulse width (P_{PWM_DS}) depends on the compare channel (CCx) register value and the peripheral clock frequency (f_{GCLK_TCCx}), and can be calculated by the following equation:

$$P_{PWM\_DS} = \frac{2N \cdot (TOP - CCx)}{f_{GCLK\_TCCx}}$$

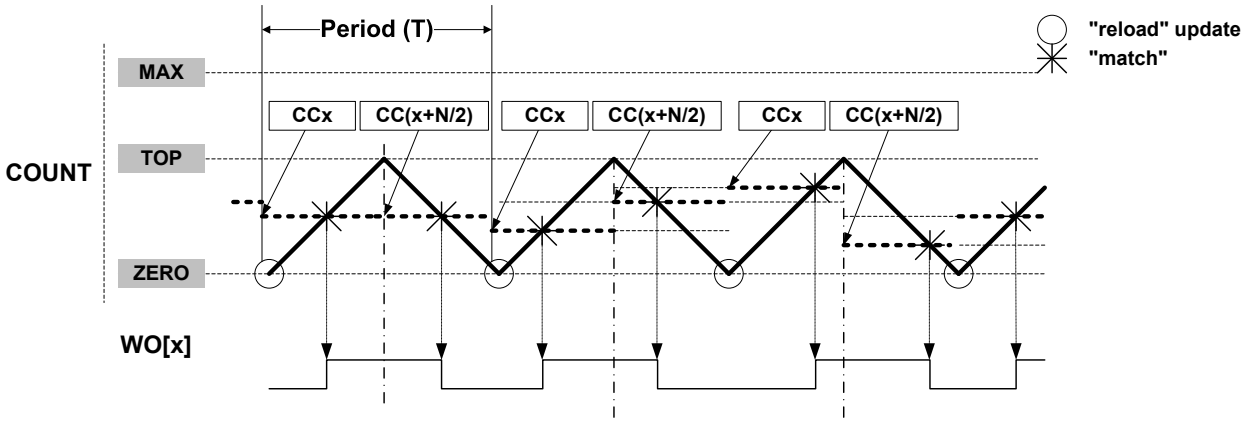
N represents the prescaler divider used.

Note: In DSTOP, DSBOTTOM and DSBOTH operation, when TOP is lower than MAX/2, the CCx MSB bit defines the ramp on which the CCx Match interrupt or event is generated. (Rising if CCx[MSB] = 0, falling if CCx[MSB] = 1.)

41.6.2.5.7. Dual-Slope Critical PWM Generation

Critical mode generation allows generation of non-aligned centered pulses. In this mode, the period time is controlled by PER while CCx control the generated waveform output edge during up-counting and CC(x+CC_NUM/2) control the generated waveform output edge during down-counting.

Figure 41-8. Dual-Slope Critical Pulse Width Modulation (N=CC_NUM)



41.6.2.5.8. Output Polarity

The polarity (WAVE.POLx) is available in all waveform output generation. In single-slope and dual-slope PWM operation, it is possible to invert the pulse edge alignment individually on start or end of a PWM cycle for each compare channels. The table below shows the waveform output set/clear conditions, depending on the settings of timer/counter, direction, and polarity.

Table 41-5. Waveform Generation Set/Clear Conditions

Waveform Generation Operation	DIR	POLx	Waveform Generation Output Update	
			Set	Clear
Single-Slope PWM	0	0	Timer/counter matches TOP	Timer/counter matches CCx
		1	Timer/counter matches CC	Timer/counter matches TOP
	1	0	Timer/counter matches CC	Timer/counter matches ZERO
		1	Timer/counter matches ZERO	Timer/counter matches CC

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Table 41-5. Waveform Generation Set/Clear Conditions (continued)

Waveform Generation Operation	DIR	POLx	Waveform Generation Output Update	
			Set	Clear
Dual-Slope PWM	x	0	Timer/counter matches CC when counting up	Timer/counter matches CC when counting down
		1	Timer/counter matches CC when counting down	Timer/counter matches CC when counting up

In Normal and Match Frequency, the WAVE.POLx value represents the initial state of the waveform output.

41.6.2.6. Double Buffering

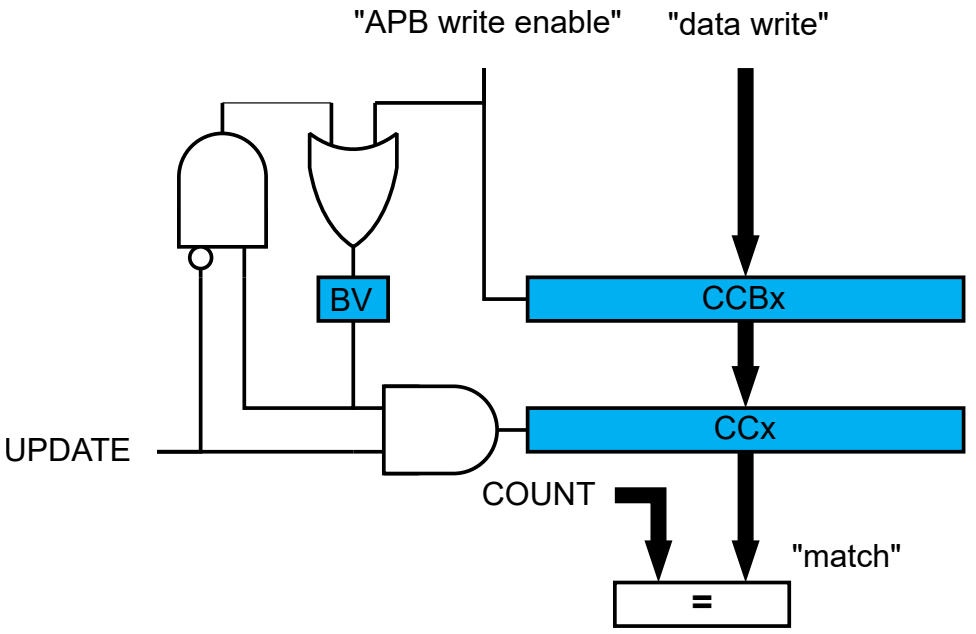
The Pattern (PATT), Period (PER) and Compare Channels (CCx) registers are all double buffered. Each buffer register has a buffer valid (PATTBUFV, PERBUFV and CCBUFVx) bit in the STATUS register that indicates that the Buffer register contains a valid value that can be copied into the corresponding register.

When the Buffer Valid Flag bit in the STATUS register is '1' and the Lock Update bit in the CTRLB register is set to '0', (writing CTRLBCLR.LUPD to '1'), double buffering is enabled: the data from buffer registers is copied into the corresponding register under hardware UPDATE conditions, then, the Buffer Valid flags bit in the STATUS register are automatically cleared by hardware.

Note: The software update command (CTRLBSET.CMD = 0x3) acts independently of the LUPD value.

A compare register is double buffered as illustrated in the following figure.

Figure 41-9. Compare Channel Double Buffering



Both the registers (PATT/PER/CCx) and corresponding Buffer registers (PATTBPERB/CCBx) are available in the I/O register map, and the double buffering feature is not mandatory. The double buffering is disabled by writing a '1' to CTRLSET.LUPD.

Note: In NFRQ, MFRQ or PWM Down-Counting Counter mode (CTRLBSET.DIR = 1), when double buffering is enabled (CTRLBCLR.LUPD = 1), PERB register is continuously copied into the PER independently of update conditions.

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Changing the Period

The counter period can be changed by writing a new Top value to the Period register (PER or CC0, depending on the Waveform Generation mode). Any period update on registers (PER or CCx) is effective after the synchronization delay, regardless of double buffering enabling.

Figure 41-10. Unbuffered Single-Slope Up-Counting Operation

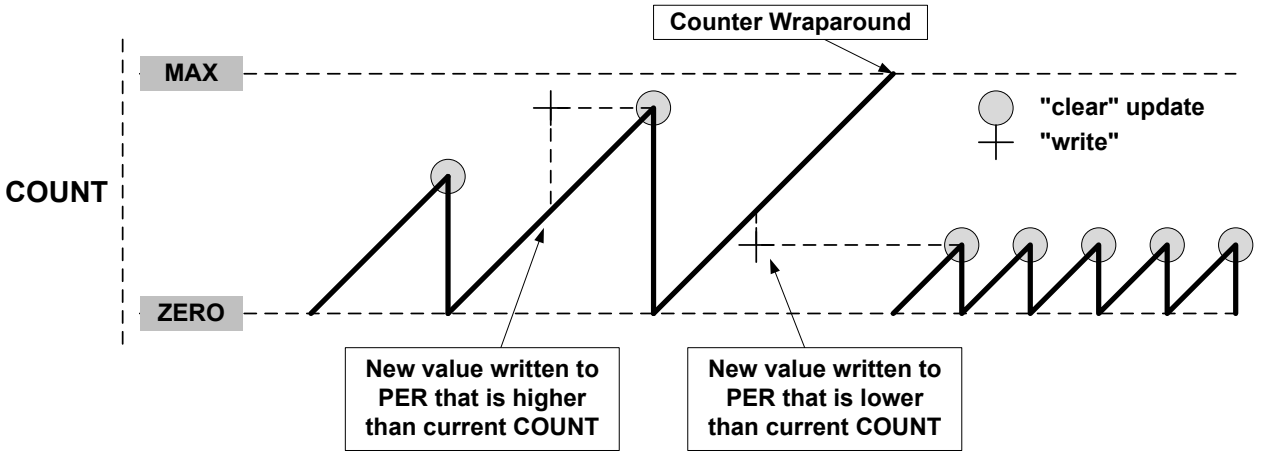
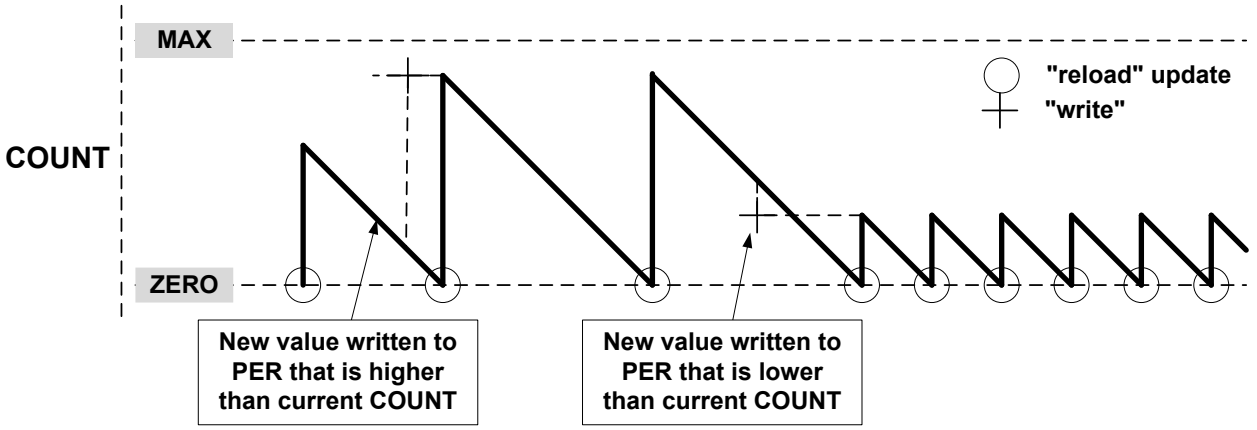


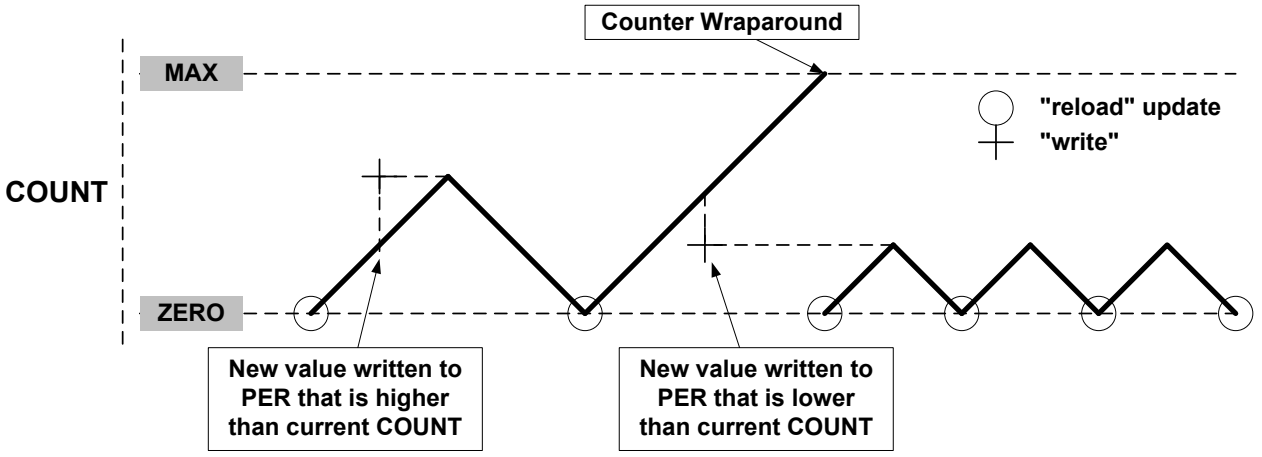
Figure 41-11. Unbuffered Single-Slope Down-Counting Operation



A counter wraparound can occur in any operation mode when up-counting without buffering; see Figure 41-10. COUNT and TOP are continuously compared, so when a new value that is lower than the current COUNT is written to TOP, COUNT wraps before a compare match.

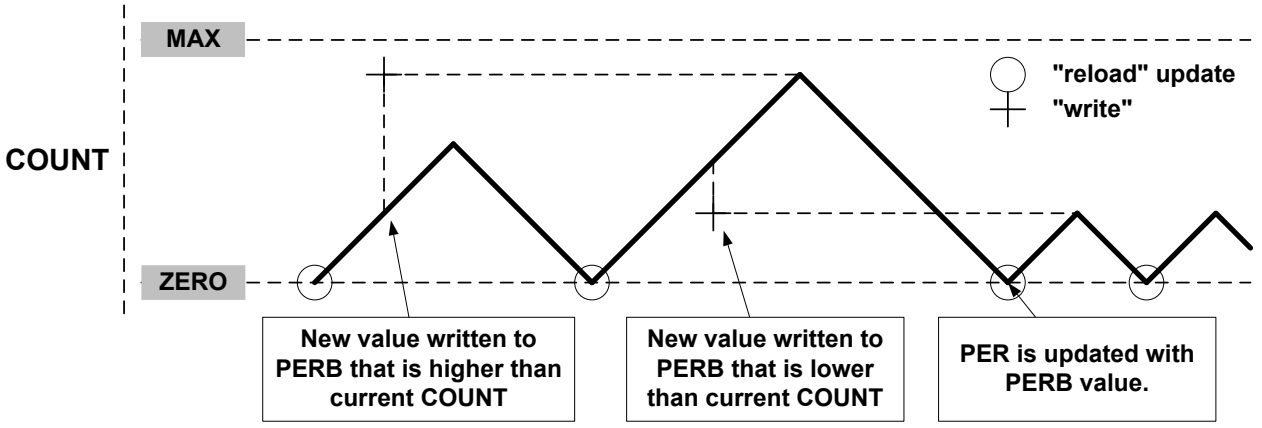
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Figure 41-12. Unbuffered Dual-Slope Operation



When double buffering is used, the buffer can be written at any time and the counter will still maintain correct operation. The period register is always updated on the update condition, as illustrated in the following figure. This prevents wraparound and the generation of odd waveforms.

Figure 41-13. Changing the Period Using Buffering



41.6.2.7. Capture Operations

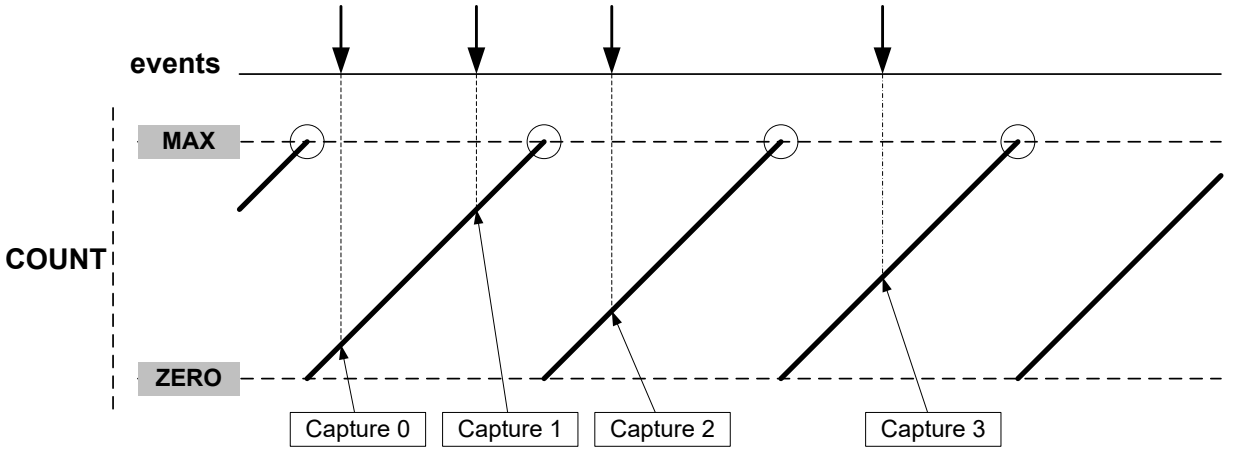
To enable and use capture operations, the Match or Capture Channel x Event Input Enable bit in the Event Control register (EVCTRL.MCEIx) must be written to '1'. The capture channels to be used must also be enabled in the Capture Channel x Enable bit in the Control A register (CTRLA.CPTENx) before capturing can be performed.

Event Capture Action

The compare/capture channels can be used as input capture channels to capture events from the Event System and give them a timestamp. The following figure illustrates four capture events for one capture channel. Event system channels must be configured to operate in asynchronous mode when used for capture operations.

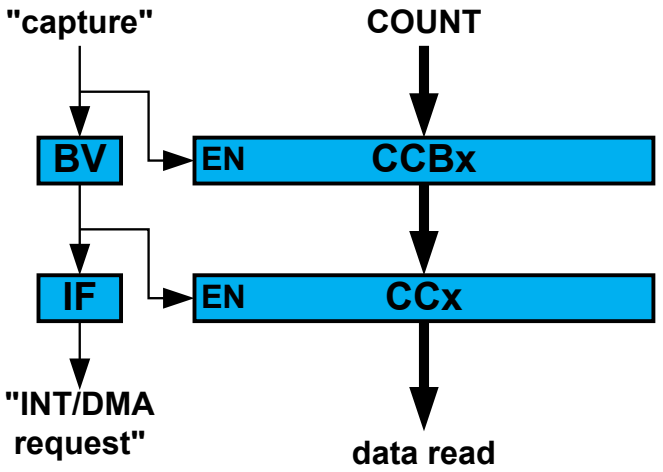
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Figure 41-14. Input Capture Timing



For input capture, the Buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBx is transferred to CCx. The Buffer Valid flag is passed to set the CCx Interrupt flag (IF) and generate the optional interrupt, event or DMA request. The CCBx register value cannot be read; all captured data must be read from the CCx register.

Figure 41-15. Capture Double Buffering



The TCC can detect capture overflow of the input capture channels. When a new capture event is detected while the Capture Buffer Valid flag (STATUS.CCBV) is still set, the new timestamp will not be stored and INTFLAG.ERR is set.

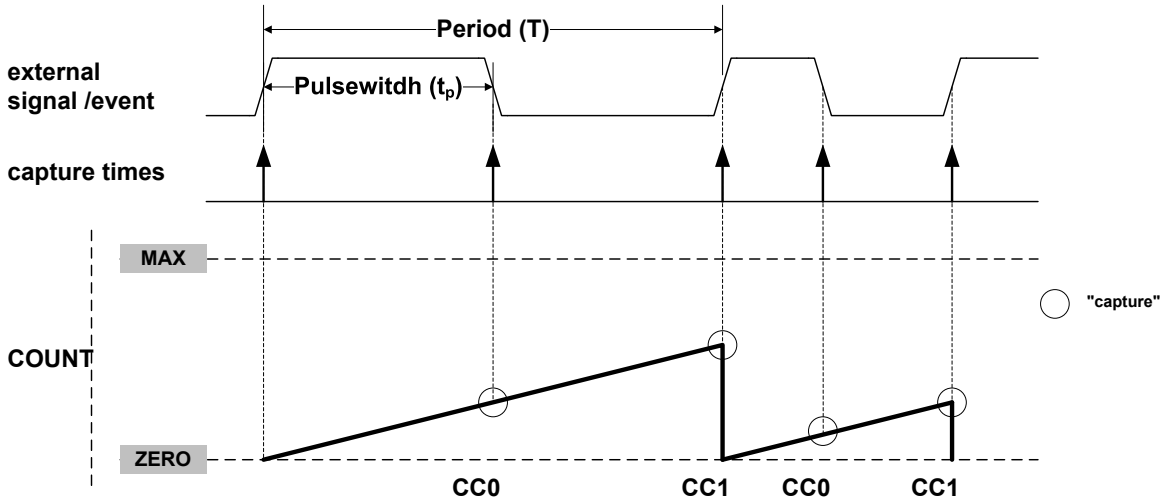
Period and Pulse-Width (PPW) Capture Action

The TCC can perform two input captures and restart the counter on one of the edges. This enables the TCC to measure the pulse-width and period and to characterize the frequency *f* and *dutyCycle* of an input signal, illustrated as follows.

$$f = \frac{1}{T} \quad , \quad dutyCycle = \frac{t_p}{T}$$

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Figure 41-16. PWP Capture



Selecting PWP or PPW in the Timer/Counter Event Input 1 Action bit group in the Event Control register (EVCTRL.EVACT1) enables the TCC to perform one capture action on the rising edge and the other one on the falling edge. When using the PPW event action, period *T* is captured into CC0 and the pulse-width t_p into CC1. The PWP (Pulse-width and Period) event action offers the same functionality, but *T* is captured into CC1 and t_p into CC0.

The Timer/Counter Event x Invert Enable bit in the Event Control register (EVCTRL.TCEINVx) is used for event source x to select whether the wraparound must occur on the rising edge or the falling edge. If EVCTRL.TCEINVx = 1, the wraparound will happen on the falling edge.

The corresponding capture is done only if the channel is enabled in Capture mode (CTRLA.CPTENx = 1). If not, the capture action is ignored and the channel is enabled in compare mode of the operation. When only one of these channels is required, the other channel can be used for other purposes.

The TCC can detect capture overflow of the input capture channels. When a new capture event is detected while the INTFLAG.MCx is still set, the new timestamp will not be stored and INTFLAG.ERR is set.

Notes:

1. When up-counting (CTRLBSET.DIR = 0), counter values lower than '1' cannot be captured in Capture Minimum mode (FCTRLn.CAPTURE = CAPTMIN). To capture the full range including value '0', the TCC must be configured in Down-counting mode (CTRLBSET.DIR = 0).
2. In dual-slope PWM operation and when TOP is lower than MAX/2, the CCx MSB captures the CTRLB.DIR state to identify the ramp where the capture was done. For rising ramps CCx[MSB] is '0'; for falling ramps CCx[MSB] = 1.

41.6.3. Additional Features

41.6.3.1. One-Shot Operation

When one-shot is enabled, the counter automatically stops on the next Counter Overflow or Underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is set and the waveform outputs are set to the value defined by DRVCTRL.NREx and DRVCTRL.NRVx.

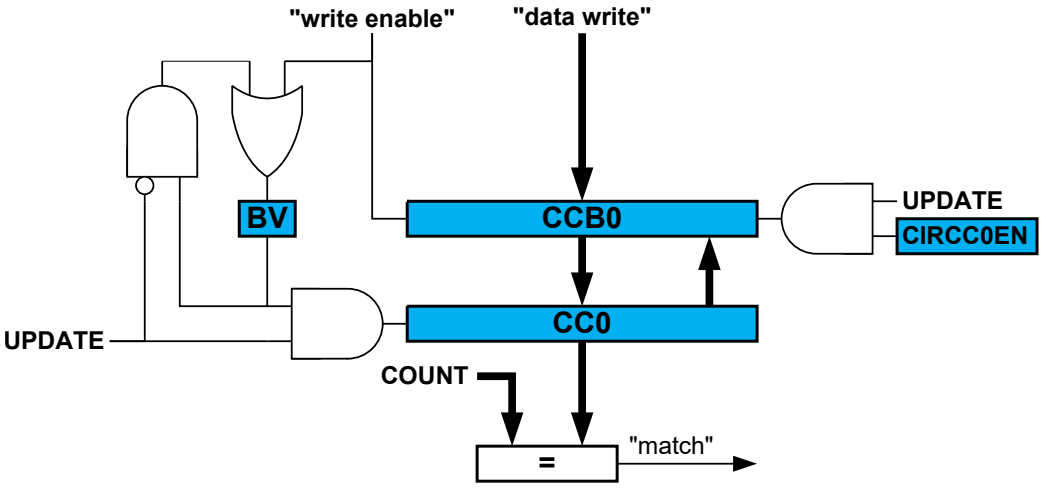
One-shot operation can be enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TCC counts until an overflow or underflow occurs and stops counting. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

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41.6.3.2. Circular Buffer

The Period register (PER) and the Compare Channels register (CC0 toCC5) support circular buffer operation. When circular buffer operation is enabled, the PER or CCx values are copied into the corresponding buffer registers at each update condition. Circular buffering is dedicated to RAMP2, RAMP2A, and DSBOTH operations.

Figure 41-17. Circular Buffer on Channel 0



41.6.3.3. Dithering Operation

The TCC supports dithering on Pulse-width or Period on a 16, 32 or 64 PWM cycles frame.

Dithering consists in adding some extra clocks cycles in a frame of several PWM cycles, and can improve the accuracy of the *average* output pulse width and period. The extra clock cycles are added on some of the compare match signals, one at a time, through a "blue noise" process that minimizes the flickering on the resulting dither patterns.

Dithering is enabled by writing the corresponding configuration in the Enhanced Resolution bits in CTRLA register (CTRLA.RESOLUTION):

- DITH4 enable dithering every 16 PWM frames
- DITH5 enable dithering every 32 PWM frames
- DITH6 enable dithering every 64 PWM frames

The DITHERCY bits of COUNT, PER and CCx define the number of extra cycles to add into the frame (DITHERCY bits from the respective COUNT, PER or CCx registers). The remaining bits of COUNT, PER, CCx define the compare value itself.

The pseudo code, giving the extra cycles insertion regarding the cycle is:

```
int extra_cycle(resolution, dithercy, cycle){
  int MASK;
  int value
  switch (resolution){
    DITH4: MASK = 0x0f;
    DITH5: MASK = 0x1f;
    DITH6: MASK = 0x3f;
  }
  value = cycle * dithercy;
  if (((MASK & value) + dithercy) > MASK)
    return 1;
 return 0;
}
```

Dithering on Period

Writing DITHERCY in PER will lead to an average PWM period configured by the following formulas.

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DITH4 mode:

$$PwmPeriod = \left(\frac{\text{DITHERCY}}{16} + \text{PER}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

Note: If DITH4 mode is enabled, the last 4 significant bits from PER/CCx or COUNT register correspond to the DITHERCY value, rest of the bits corresponds to PER/CCx or COUNT value.

DITH5 mode:

$$PwmPeriod = \left(\frac{\text{DITHERCY}}{32} + \text{PER}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

DITH6 mode:

$$PwmPeriod = \left(\frac{\text{DITHERCY}}{64} + \text{PER}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

Dithering on Pulse-Width

Writing DITHERCY in CCx will lead to an average PWM pulse width configured by the following formula.

DITH4 mode:

$$PwmPulseWidth = \left(\frac{\text{DITHERCY}}{16} + \text{CCx}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

DITH5 mode:

$$PwmPulseWidth = \left(\frac{\text{DITHERCY}}{32} + \text{CCx}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

DITH6 mode:

$$PwmPulseWidth = \left(\frac{\text{DITHERCY}}{64} + \text{CCx}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

Note: The PWM period will remain static in this case.

41.6.3.4. Ramp Operations

Three ramp operation modes are supported. All of them require the timer/counter running in the single-slope PWM generation. The Ramp mode is selected by writing to the Ramp Mode bits in the Waveform Control register (WAVE.RAMP).

RAMP1 Operation

This is the default PWM operation, described in Single-Slope PWM Generation. See *Single-Slope PWM Generation* from Related Links.

RAMP2 Operation

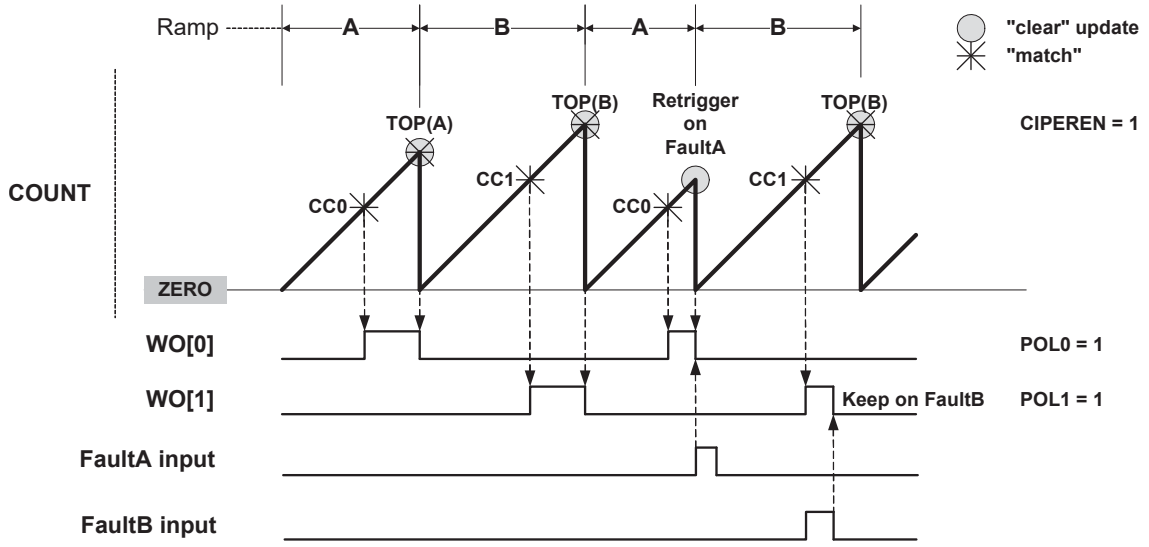
These operation modes are dedicated for Power Factor Correction (PFC), Half-Bridge and Push-Pull SMPS topologies, where two consecutive timer/counter cycles are interleaved; see Figure 41-18. In cycle A, odd channel output is disabled, and, in cycle B, even channel output is disabled. The ramp index changes after each update but can be software modified using the Ramp index command bits in the Control B Set register (CTRLBSET.IDXCMD).

Standard RAMP2 (RAMP2) Operation

Ramp A and B periods are controlled by the PER register value. The PER value can be different on each ramp by the Circular Period buffer option in the Wave register (WAVE.CIPEREN = 1). This mode uses a two-channel TCC to generate two output signals or one output signal with another CC channel enabled in Capture mode.

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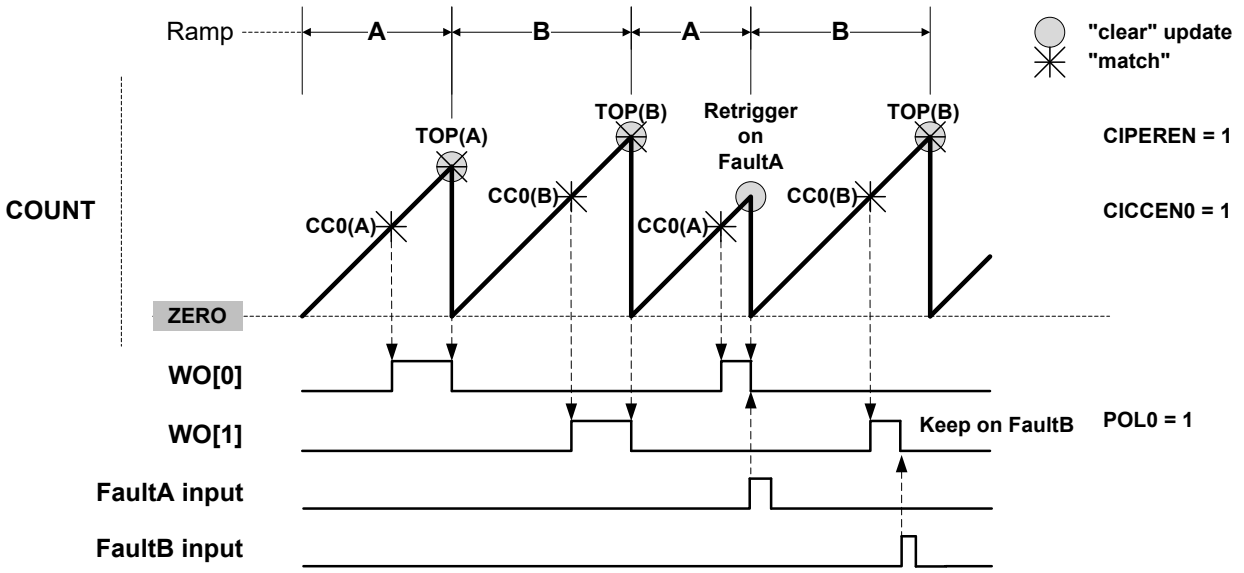
Figure 41-18. RAMP2 Standard Operation



Alternate RAMP2 (RAMP2A) Operation

Alternate RAMP2 operation is similar to RAMP2 but CC0 controls both WO[0] and WO[1] waveforms when the corresponding circular buffer option is enabled (CIPEREN = 1). The waveform polarity is the same on both outputs. Channel 1 can be used in capture mode.

Figure 41-19. RAMP2 Alternate Operation



Critical RAMP2 (RAMP2C) Operation

Critical RAMP2 operation provides a way to cover RAMP2 operation requirements without the update constraint associated with the use of circular buffers. In this mode, CC0 is controlling the period of ramp A and PER is controlling the period of ramp B. When using more than two channels, WO[0] output is controlled by CC2 (HIGH) and CC0 (LOW). On TCC with 2 channels, a pulse on WO[0] will last the entire period of ramp A if WAVE.POL0 = 0.

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Figure 41-20. RAMP2 Critical Operation With More Than 2 Channels

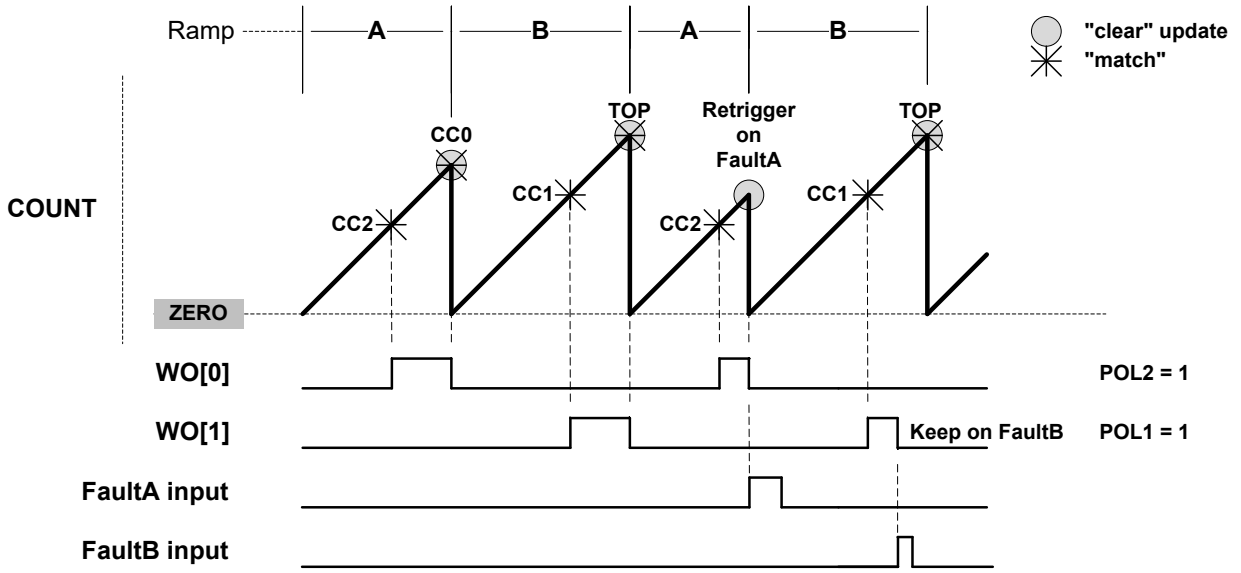
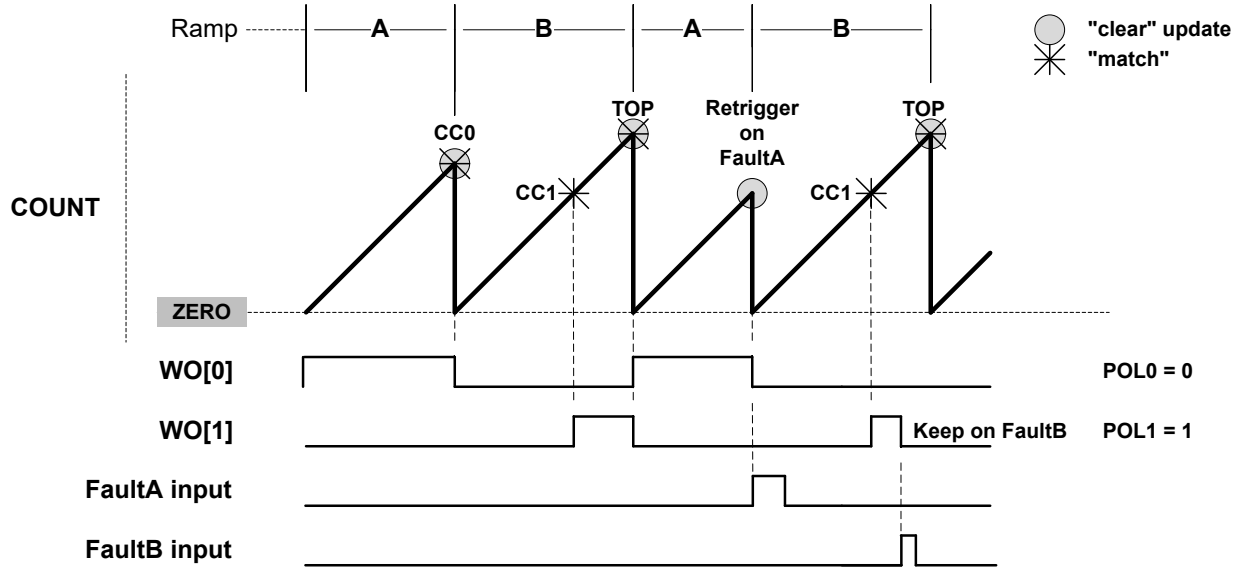


Figure 41-21. RAMP2 Critical Operation With 2 Channels



Related Links

Single-Slope PWM Operation

41.6.3.5. Recoverable Faults

Recoverable faults can restart or halt the timer/counter. Two faults, called Fault A and Fault B, can trigger recoverable fault actions on the compare channels CC0 and CC1 of the TCC. The compare channels' outputs can be clamped to an inactive state either as long as the fault condition is present or from the first valid fault condition detection on until the end of the timer/counter cycle.

Fault Inputs

The first two channel input events (TCCxMC0 and TCCxMC1) can be used as Fault A and Fault B inputs, respectively. Event system channels connected to these fault inputs must be configured as asynchronous. The TCC must work in a PWM mode.

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Fault Filtering

There are three filters available for each input Fault A and Fault B. They are configured by the corresponding Recoverable Fault n Configuration registers (FCTRLA and FCTRLB). The three filters can either be used independently or in any combination.

Input Filtering

By default, the event detection is asynchronous. When the event occurs, the fault system will immediately and asynchronously perform the selected fault action on the compare channel output, and, also, in device power modes where the clock is not available. To avoid false fault detection on external events (for example, due to a glitch on an I/O port), a digital filter can be enabled and configured by the Fault B Filter Value bits in the Fault n Configuration registers (FCTRLn.FILTERVAL). If the event width is less than FILTERVAL (in clock cycles), the event is discarded. A valid event is delayed by FILTERVAL clock cycles.

Fault Blanking

This ignores any fault input for a certain time just after a selected waveform output edge. This can be used to prevent false fault triggering due to signal bouncing, as shown in the figure below. Blanking can be enabled by writing an edge-triggering configuration to the Fault n Blanking Mode bits in the Recoverable Fault n Configuration register (FCTRLn.BLANK). The desired duration of the blanking must be written to the Fault n Blanking Time bits (FCTRLn.BLANKVAL).
The blanking time $t_b$is calculated by

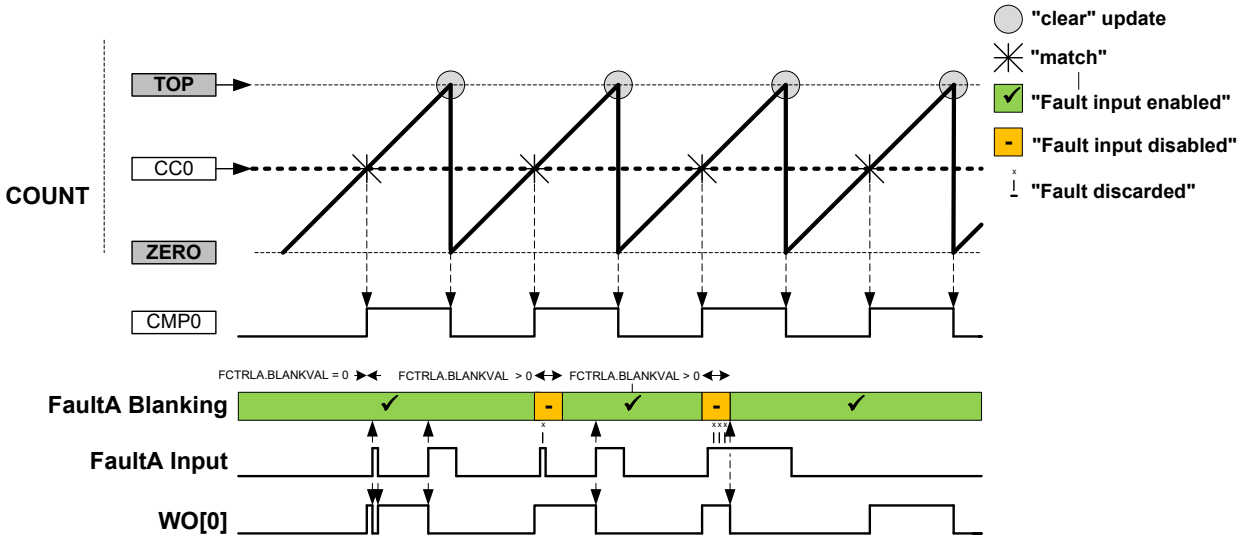
$$t_b = \frac{1 + \text{BLANKVAL}}{f_{\text{GCLK\_TCCx\_PRESC}}}$$

Here, $f_{\text{GCLK\_TCCx\_PRESC}}$ is the frequency of the prescaled peripheral clock frequency $f_{\text{GCLK\_TCCx}}$.

The prescaler is enabled by writing '1' to the Fault n Blanking Prescaler bit (FCTRLn.BLANKPRESC). When disabled, $f_{\text{GCLK\_TCCx\_PRESC}} = f_{\text{GCLK\_TCCx}}$. When enabled, $f_{\text{GCLK\_TCCx\_PRESC}} = f_{\text{GCLK\_TCCx}}/64$.

The maximum blanking time (FCTRLn.BLANKVAL = 255) at $f_{\text{GCLK\_TCCx}}$ = 128 MHz is 2 µs (no prescaler) or 128 µs (prescaling enabled). For $f_{\text{GCLK\_TCCx}}$ = 1 MHz, the maximum blanking time is either 256 µs (no prescaling) or 16.4 ms (prescaling enabled).

Figure 41-22. Fault Blanking in RAMP1 Operation with Inverted Polarity



Fault Qualification

This is enabled by writing a '1' to the Fault n Qualification bit in the Recoverable Fault n Configuration register (FCTRLn.QUAL). When the recoverable fault qualification is

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enabled (FCTRLn.QUAL = 1), the fault input is disabled all the time the corresponding channel output has an inactive level, as illustrated in the following figures.

Figure 41-23. Fault Qualification in RAMP1 Operation

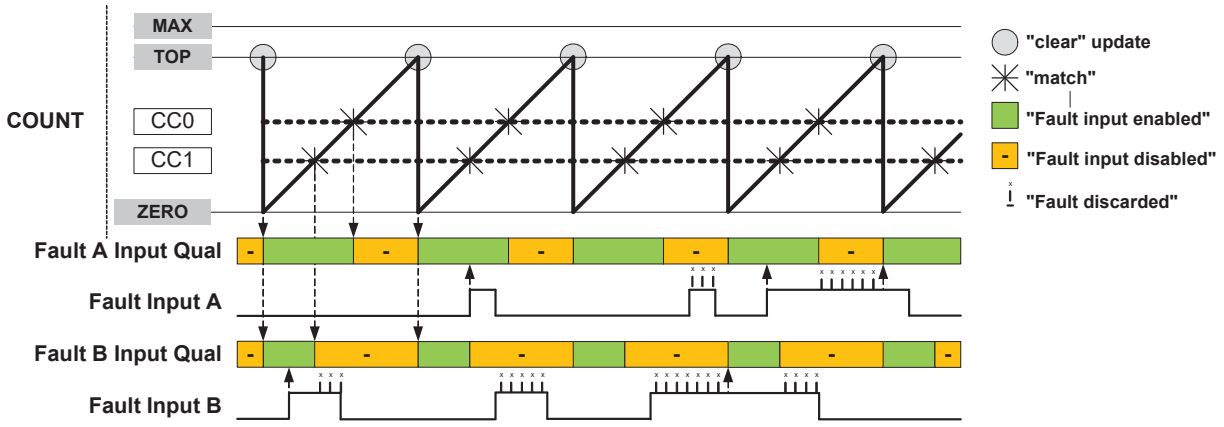
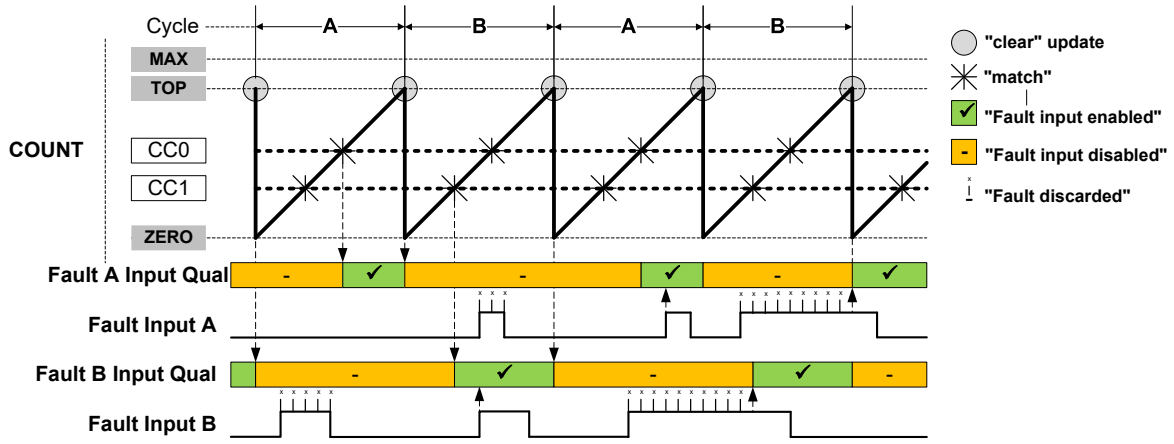


Figure 41-24. Fault Qualification in RAMP2 Operation with Inverted Polarity



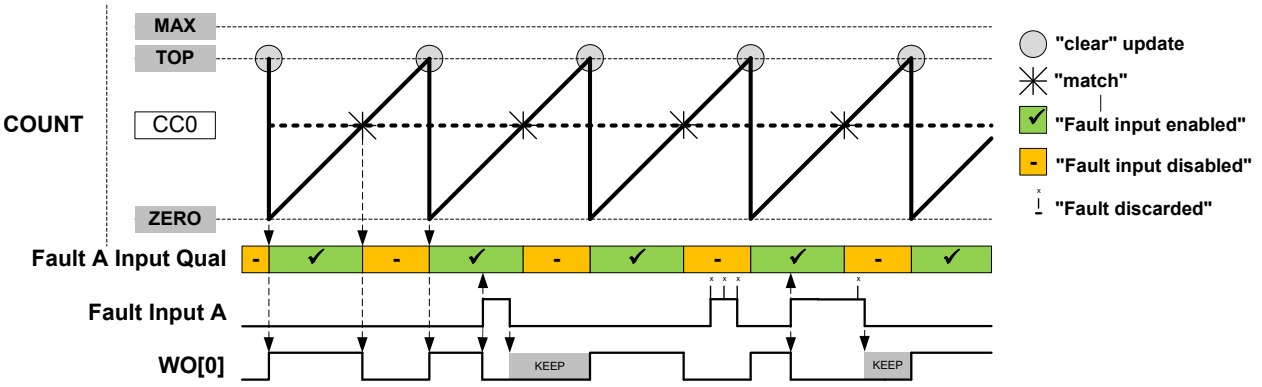
Fault Actions

Different fault actions can be configured individually for Fault A and Fault B. Most fault actions are not mutually exclusive; hence, two or more actions can be enabled at the same time to achieve a result that is a combination of fault actions.

Keep Action This is enabled by writing the Fault n Keeper bit in the Recoverable Fault n Configuration register (FCTRLn.KEEP) to '1'. When enabled, the corresponding channel output is clamped to '0' as long as the fault condition is present. The clamp is released on the start of the first cycle after the fault condition is no longer present; see Figure 41-25.

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Figure 41-25. Waveform Generation with Fault Qualification and Keep Action



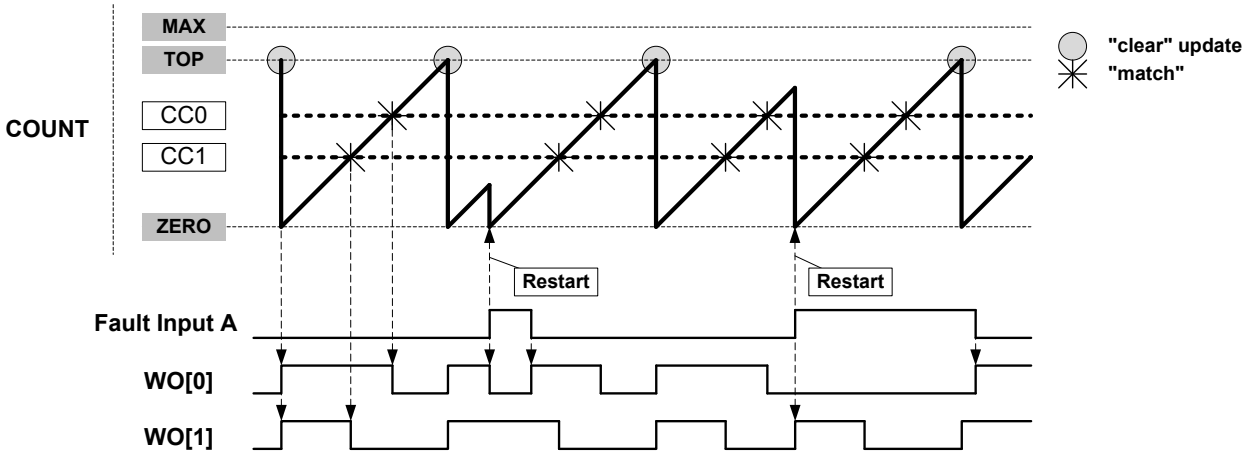
Restart Action

This is enabled by writing the Fault n Restart bit in Recoverable Fault n Configuration register (FCTRLn.RESTART) to '1'. When enabled, the timer/counter is restarted as soon as the corresponding fault condition is present. The ongoing cycle is stopped and the timer/counter starts a new cycle; see Figure 41-26. In Ramp 1 mode, when the new cycle starts, the compare outputs is clamped to inactive level as long as the fault condition is present.

Notes: For the RAMP2 operation, when a new timer/counter cycle starts, the cycle index will change automatically; see Figure 41-27. Fault A and Fault B are qualified only during the cycle A and cycle B respectively:

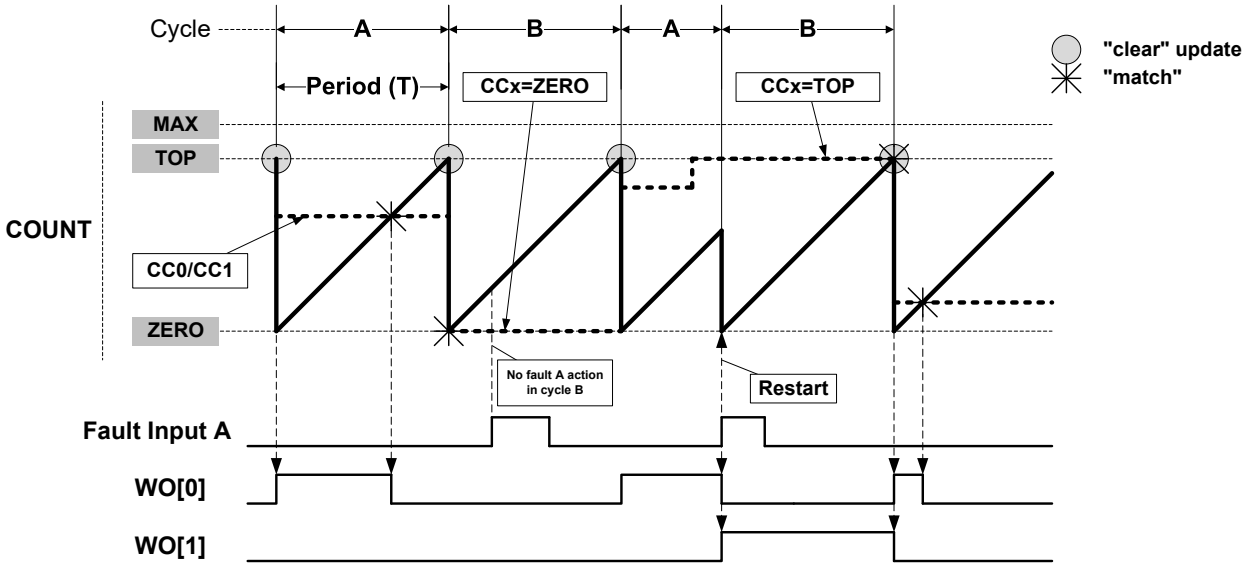
- Fault A is disabled during cycle B
- Fault B is disabled during cycle A

Figure 41-26. Waveform Generation in RAMP1 mode with Restart Action



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Figure 41-27. Waveform Generation in RAMP2 mode with Restart Action



Capture Action

Several capture actions can be selected by writing the Fault n Capture Action bits in the Fault n Control register (FCTRLn.CAPTURE). When one of the capture operations is selected, the counter value is captured when the fault occurs. These capture operations are available:

- CAPT – The equivalent to a standard capture operation; see *Capture Operations* from Related Links
- CAPTMIN – Gets the minimum time stamped value: on each new local minimum captured value, an event or interrupt is issued
- CAPTMAX – Gets the maximum time stamped value: on each new local maximum captured value, an event or interrupt (IT) is issued; see Figure 41-28
- LOCMIN – Notifies by event or interrupt when a local minimum captured value is detected
- LOCMAX – Notifies by event or interrupt when a local maximum captured value is detected
- DERIV0 – Notifies by event or interrupt when a local extreme captured value is detected; see Figure 41-29

CCx Content:

In CAPTMIN and CAPTMAX operations, CCx keeps the respective extremum captured values; see Figure 41-28. In LOCMIN, LOCMAX or DERIV0 operation, CCx follows the counter value at fault time; see Figure 41-29.

Before enabling CAPTMIN or CAPTMAX mode of capture, the user must initialize the corresponding CCx register value to a value different from zero (for CAPTMIN) or top (for CAPTMAX). If the CCx register initial value is zero (for CAPTMIN) or top (for CAPTMAX), no captures are performed using the corresponding channel.

MCx Behavior:

In LOCMIN and LOCMAX operation, capture is performed on each capture event. The MCx interrupt flag is set only when the captured value is above or equal (for LOCMIN) or below or equal (for LOCMAX) to the previous captured value. So the interrupt flag is set when a new relative local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value is detected. DERIV0 is equivalent to an OR function of (LOCMIN, LOCMAX).

In CAPT operation, capture is performed on each capture event. The MCx interrupt flag is set on each new capture.

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In the CAPTMIN and CAPTMAX operation, the capture is performed only when, on capture event time, the counter value is lower (for CAPTMIN) or higher (for CAPMAX) than the last captured value. The MCx interrupt flag is set only when, on capture event time, the counter value is higher or equal (for CAPTMIN) or lower or equal (for CAPTMAX) to the value captured on the previous event. So the interrupt flag is set when a new absolute local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value is detected.

Interrupt Generation:

In CAPT mode, an interrupt is generated on each filtered Fault n and each dedicated CCx channel capture counter value. In other modes, an interrupt is only generated on an extreme captured value.

Figure 41-28. Capture Action CAPTMAX

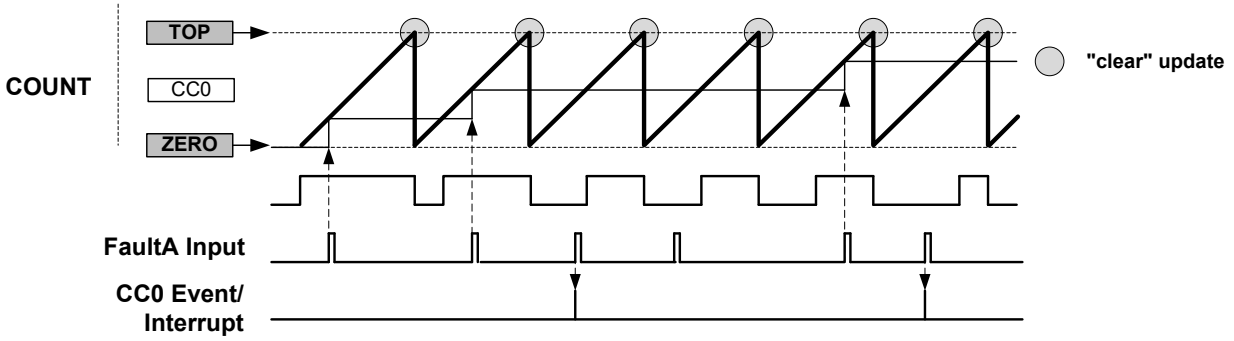
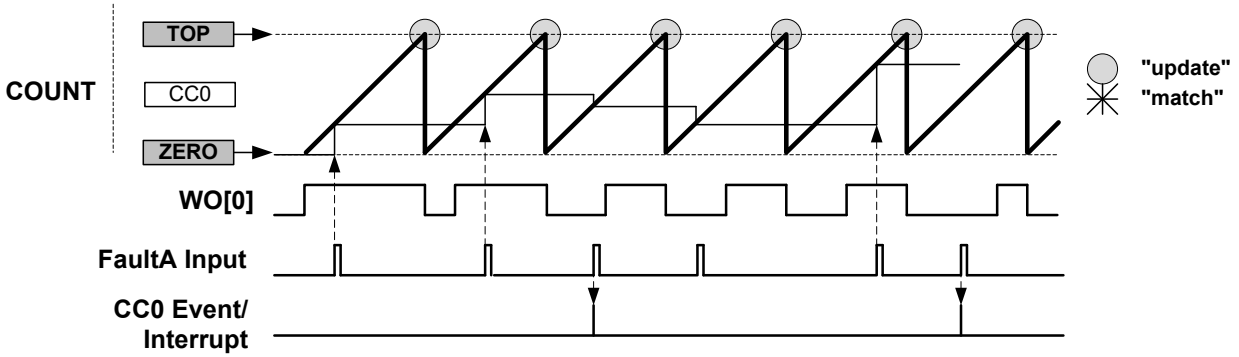


Figure 41-29. Capture Action DERIV0



Hardware Halt Action

This is configured by writing 0x1 to the Fault n Halt mode bits in the Recoverable Fault n Configuration register (FCTRLn.HALT). When enabled, the timer/counter is halted and the cycle is extended as long as the corresponding fault is present.

The Figure 41-30 illustrates an example where both restart action and hardware halt action are enabled for Fault A. The compare channel 0 output is clamped to inactive level as long as the timer/counter is halted. The timer/counter resumes the counting operation as soon as the fault condition is no longer present. As the restart action is enabled in this example, the timer/counter is restarted after the fault condition is no longer present.

The Figure 41-31 illustrates a similar example but with additionally enabled fault qualification. Here, counting is resumed after the fault condition is no longer present.

Note: In RAMP2 and RAMP2A operations, when a new timer/counter cycle starts, the cycle index automatically changes.

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Figure 41-30. Waveform Generation with Halt and Restart Actions

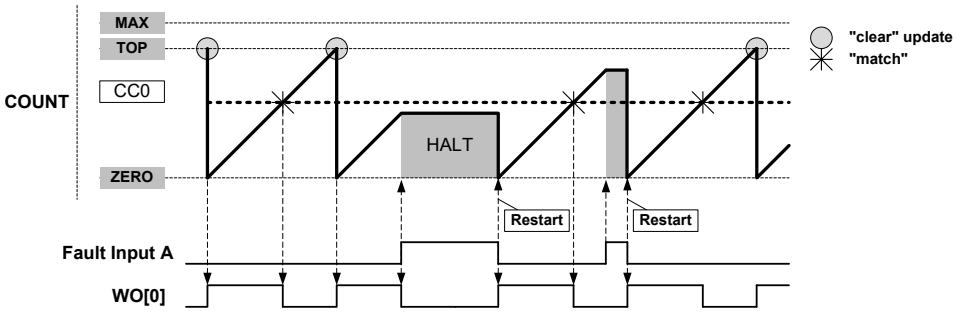
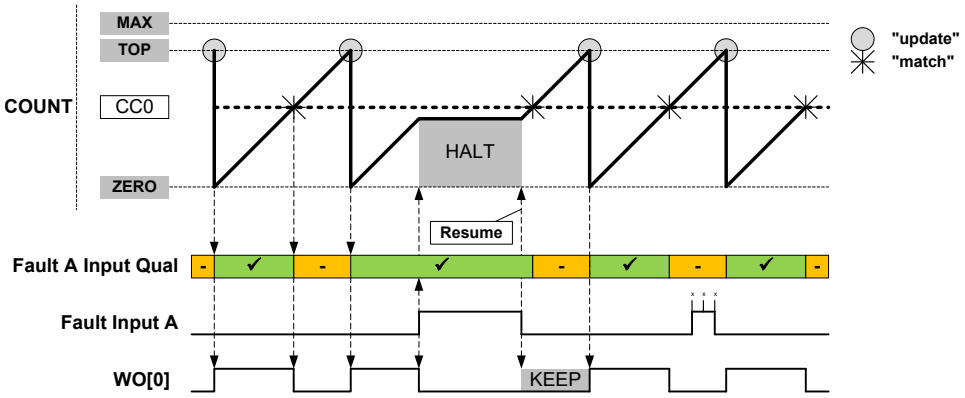
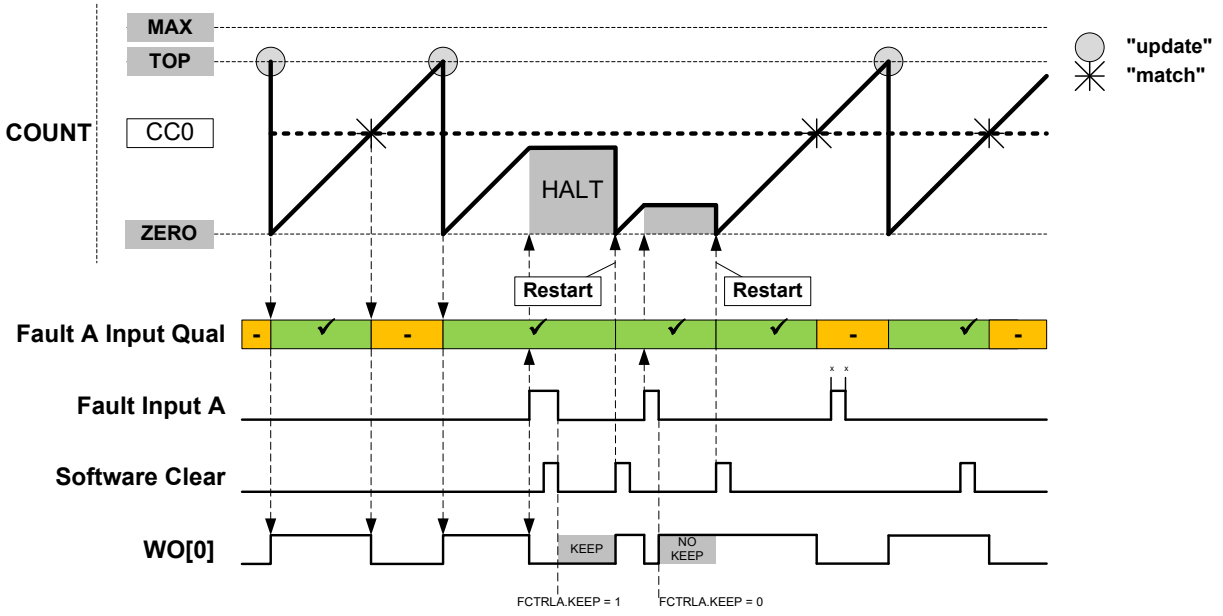


Figure 41-31. Waveform Generation with Fault Qualification and Halt



Software Halt Action This is configured by writing 0x2 to the Fault n Halt mode bits in the Recoverable Fault n configuration register (FCTRLn.HALT). Software halt action is similar to hardware halt action but, to restart the timer/counter, the corresponding fault condition must not be present anymore and the corresponding FAULT n bit in the STATUS register must be cleared by software.

Figure 41-32. Waveform Generation with Software Halt, Fault Qualification, Keep and Restart Actions



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Related Links
Capture Operations

41.6.3.6. Non-Recoverable Faults

The non-recoverable fault action will force all the compare outputs to a pre-defined level programmed into the Driver Control register (DRVCTRL.NRE and DRVCTRL.NRV). The non-recoverable fault input (EV0 and EV1) actions are enabled in Event Control register (EVCTRL.EVACT0 and EVCTRL.EVACT1).

To avoid false fault detection on external events (for example, a glitch on an I/O port) a digital filter can be enabled using Non-Recoverable Fault Input x Filter Value bits in the Driver Control register (DRVCTRL.FILTERVALn). Therefore, the event detection is synchronous, and event action is delayed by the selected digital filter value clock cycles.

When the Fault Detection on Debug Break Detection bit in Debug Control register (DGBCTRL.FDDBD) is written to '1', a non-recoverable Debug Faults State and an interrupt (DFS) is generated when the system goes in debug operation.

In RAMP2, RAMP2A or DSBOTH operation, when the Lock Update bit in the Control B register is set by writing CTRLBSET.LUPD = 1 and the ramp index or counter direction changes, a non-recoverable Update Fault State and the respective interrupt (UFS) are generated.

41.6.3.7. Time-Stamp Capture on Events or I/Os

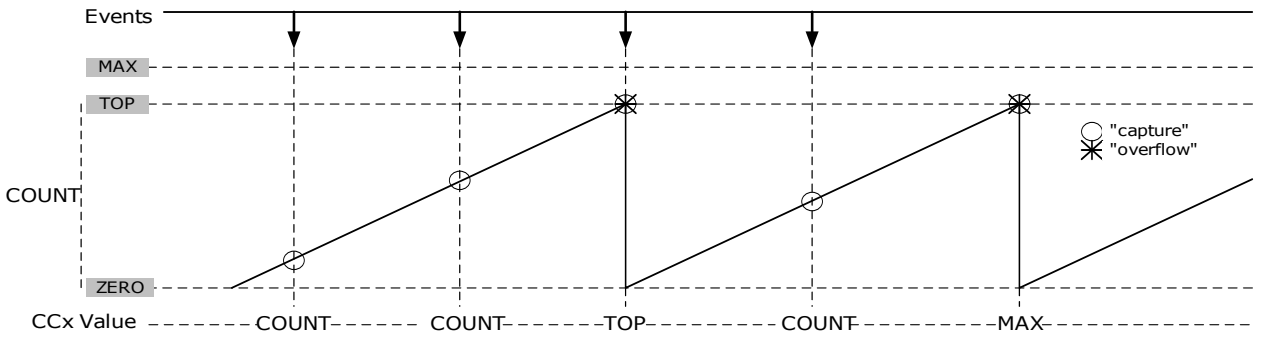
This feature is enabled when the Capture Time Stamp (STAMP) Event Action in Event Control register (EVCTRL.EVACT) is selected. The counter TOP value must be smaller than MAX.

When a capture event from the Event System or the I/O pin is detected, the COUNT value is copied into the corresponding Channel x Compare/Capture Value (CCx) register. In case of an overflow, the MAX value is copied into the corresponding CCx register.

When a valid captured value is present in the capture channel register, the corresponding Capture Channel x Interrupt Flag (INTFLAG.MCx) is set.

The timer/counter can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Channel interrupt flag (INTFLAG.MCx) is still set, the new time-stamp will not be stored and INTFLAG.ERR will be set.

Figure 41-33. Time Stamp



41.6.3.8. Waveform Extension

The following figure illustrates the schematic diagram of actions of the four optional units that follow the recoverable fault stage on a port pin pair: Output Matrix (OTMX), Dead-Time Insertion (DTI), SWAP and Pattern Generation. The DTI and SWAP units can be seen as four port pair slices:

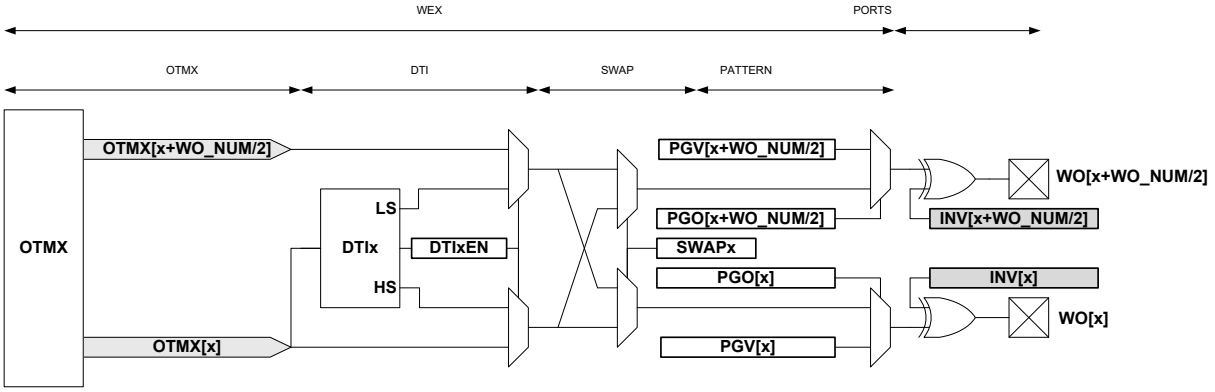
- Slice 0 DTI0/SWAP0 acting on port pins (WO[0], WO[WO_NUM/2 +0])
- Slice 1 DTI1/SWAP1 acting on port pins (WO[1], WO[WO_NUM/2 +1])

And in general:

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- Slice n DTIx/SWAPx acting on port pins (WO[x], WO[WO_NUM/2 +x])

Figure 41-34. Waveform Extension Stage Details



The OTMX unit distributes compare channels according to the selectable configurations in the following table.

Table 41-6. Output Matrix Channel Pin Routing Configuration

WEXCTRL.OTMX	OTMX[5]	OTMX[4]	OTMX[3]	OTMX[2]	OTMX[1]	OTMX[0]
0x0	CC5	CC4	CC3	CC2	CC1	CC0
0x1	CC2	CC1	CC0	CC2	CC1	CC0
0x2	CC0	CC0	CC0	CC0	CC0	CC0
0x3	CC1	CC1	CC1	CC1	CC1	CC0

- Configuration 0x0 is the default configuration. The channel location is the default one and channels are distributed on outputs modulo the number of channels. Channel 0 is routed to the Output matrix output OTMX[0] and Channel 1 to OTMX[1]. If there are more outputs than channels, channel 0 is duplicated to the Output matrix output OTMX[CC_NUM], channel 1 to OTMX[CC_NUM+1] and so on.
- Configuration 0x1 distributes the channels on output modulo half the number of channels. This assigns twice the number of output locations to the lower channels than the default configuration. This can be used, for example, to control the four transistors of a full bridge using only two compare channels.
  Using pattern generation, some of these four outputs can be overwritten by a constant level, enabling the flexible drive of a full bridge in all quadrant configurations.
- Configuration 0x2 distributes compare channel 0 (CC0) to all port pins. With pattern generation, this configuration can control a stepper motor.
- Configuration 0x3 distributes the compare channel CC0 to the first output, and the channel CC1 to all other outputs. Together with pattern generation and the fault extension, this configuration can control up to seven LED strings with a boost stage.

The following table defines an example showing four compare channels on four outputs.

Table 41-7. Four Compare Channels on Four Outputs

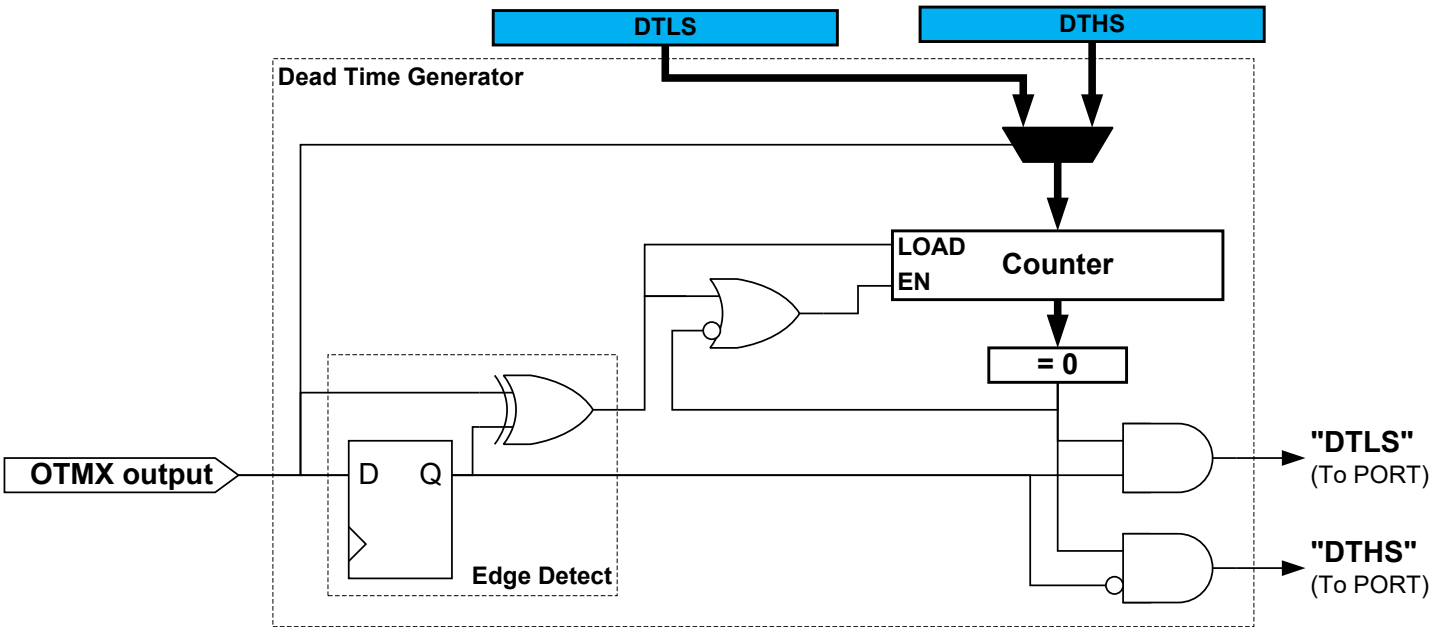
WEXCTRL.OTMX	OTMX[3]	OTMX[2]	OTMX[1]	OTMX[0]
0x0	CC3	CC2	CC1	CC0
0x1	CC1	CC0	CC1	CC0
0x2	CC0	CC0	CC0	CC0
0x3	CC1	CC1	CC1	CC0

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The DTI unit generates OFF time with the non-inverted low side (LS) and inverted high side (HS) of the wave generator output forced at low level. This OFF time is called dead time. Dead-time insertion ensures that the LS and HS will never switch simultaneously.

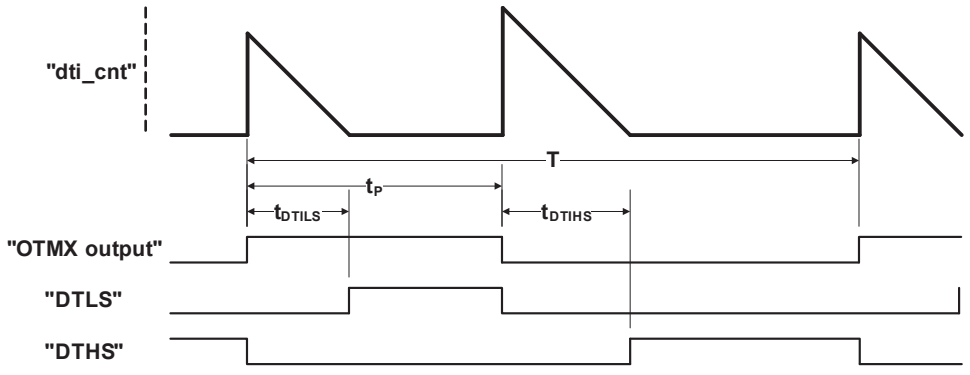
The DTI stage consists of four equal dead-time insertion generators; one for each of the first four compare channels. The following figure illustrates the block diagram of one DTI generator. The four channels have a common register that controls the dead time, which is independent of high side and low side setting.

Figure 41-35. Dead-Time Generator Block Diagram



As illustrated in the following figure, the 8-bit dead-time counter is decremented by one for each peripheral clock cycle until it reaches zero. A non-zero counter value will force both the low side and high side outputs into their OFF state. When the Output Matrix (OTMX) output changes, the dead-time counter is reloaded according to the edge of the input. When the output changes from low to high (positive edge), it initiates a counter reload of the DTLS register. When the output changes from high to low (negative edge), it reloads the DTHS register.

Figure 41-36. Dead-Time Generator Timing Diagram

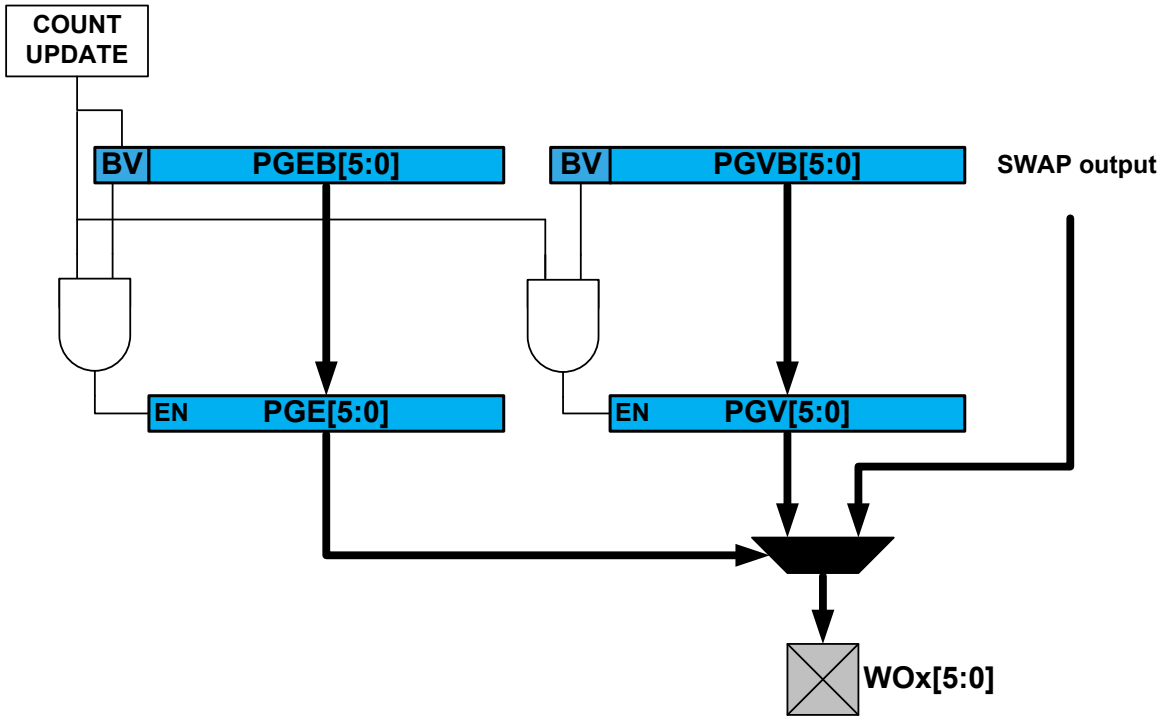


The pattern generator unit produces a synchronized bit pattern across the port pins it is connected to. The pattern generation features are primarily intended for handling the commutation sequence

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in Brushless DC motors (BLDC), stepper motors and full bridge control as illustrated in the following figure.

Figure 41-37. Pattern Generator Block Diagram



As with other double-buffered timer/counter registers, the register update is synchronized to the UPDATE condition set by the timer/counter waveform generation operation. If synchronization is not required by the application, the software can simply access the PATT.PGE, PATT.PGV bits registers directly.

41.6.4. Host/Client Operation

Two or more TCC instances sharing the same GCLK_TCCx clock, can be linked to provide more synchronized CC channels. The operation is enabled by setting the Host Synchronization bit in Control A register (CTRLA.MSYNC) in the Client instance. When the bit is set, the Client TCC instance will synchronize the CC channels to the Host counter.

41.6.5. DMA, Interrupts and Events

Table 41-8. Module Requests for TCC

Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
Overflow/Underflow	Yes	Yes	—	Yes(1)	On DMA acknowledge
Channel Compare Match or Capture	Yes	Yes	Yes(2)	Yes(3)	For circular buffering: on DMA acknowledge For capture channel: when CCx register is read
Retrigger	Yes	Yes	—	—	—
Count	Yes	Yes	—	—	—
Capture Overflow Error	Yes	—	—	—	—
Debug Fault State	Yes	—	—	—	—
Recoverable Faults	Yes	—	—	—	—
Non-Recoverable Faults	Yes	—	—	—	—

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Table 41-8. Module Requests for TCC (continued)

Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
TCCx Event 0 input	—	—	Yes(4)	—	—
TCCx Event 1 input	—	—	Yes(5)	—	—

Notes:

1. DMA request set on Overflow, Underflow or Re-trigger conditions.
2. Can perform capture or generate recoverable fault on an event input.
3. In Capture or Circular modes.
4. On event input, either action can be executed:
   - Re-trigger counter
   - Control counter direction
   - Stop the counter
   - Decrement the counter
   - Perform period and pulse width capture
   - Generate non-recoverable fault
5. On event input, either action can be executed:
   - Re-trigger counter
   - Increment or decrement counter depending on direction
   - Start the counter
   - Increment or decrement counter based on direction
   - Increment counter regardless of direction
   - Generate non-recoverable fault

41.6.5.1. DMA Operation

Note: DMA One-Shot mode is not available in RAMP1/RAMP2C/RAMP2CS modes.

The TCC can generate the following DMA requests:

Counter overflow (OVF)	If the One-shot Trigger mode in the control A register (CTRLA.DMAOS) is written to '0', the TCC generates a DMA request on each cycle when an update condition (Overflow, Underflow or Re-trigger) is detected. When an update condition (Overflow, Underflow or Re-trigger) is detected while CTRLA.DMAOS = 1, the TCC generates a DMA trigger on the cycle following the DMA One-Shot Command written to the Control B register (CTRLBSET.CMD = DMAOS). In both cases, the request is cleared by hardware on DMA acknowledge.
Channel Match (MCx)	A DMA request is set only on a compare match if CTRLA.DMAOS = 0. The request is cleared by hardware on DMA acknowledge. When CTRLA.DMAOS = 1, the DMA requests are not generated.
Channel Capture (MCx)	For a capture channel, the request is set when valid data is present in the CCx register, and cleared when the CCx register is read. In this operation mode, the CTRLA.DMAOS bit value is ignored.

DMA Operation with Circular Buffer

When circular buffer operation is enabled, the Buffer registers must be written in a correct order and synchronized to the update times of the timer. The DMA triggers of the TCC provide a way to ensure a safe and correct update of circular buffers.

Note: Circular buffers are intended to be used with RAMP2, RAMP2A and DSBOTH operation only.

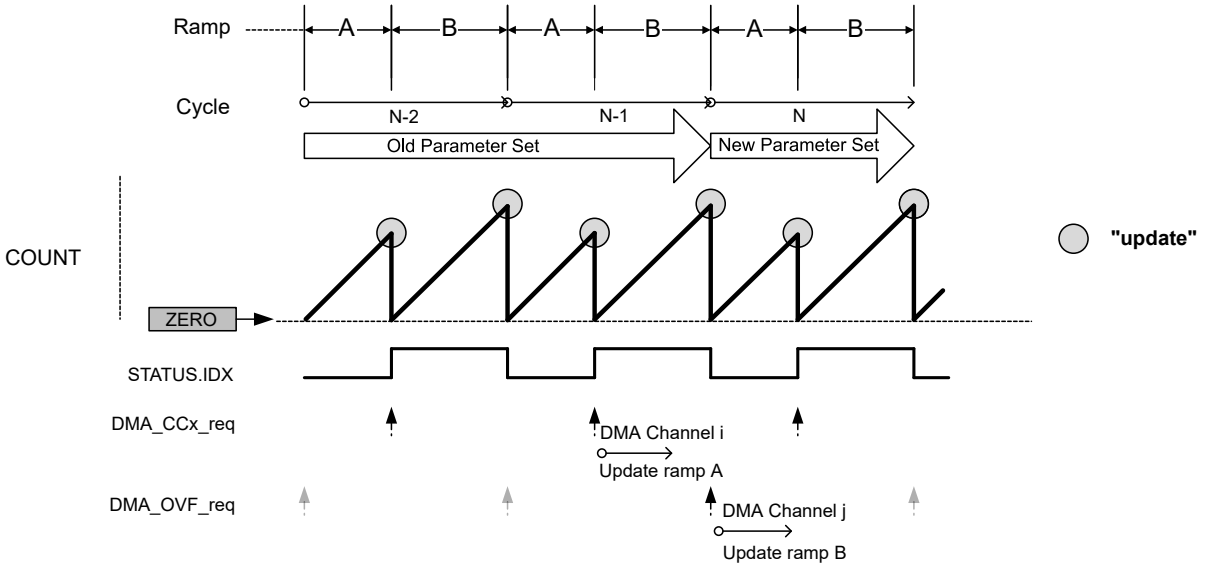
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DMA Operation with Circular Buffer in RAMP2 and RAMP2A Mode:
When a CCx channel is selected as a circular buffer, the related DMA request is not set on a compare match detection but on start of ramp B.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of ramp A with an effective DMA transfer on previous ramp B (DMA acknowledge).

The update of all circular buffer values for ramp A can be done through a DMA channel triggered on an MC trigger. The update of all circular buffer values for ramp B can be done through a second DMA channel triggered by the overflow DMA request.

Figure 41-38. DMA Triggers in RAMP and RAMP2 Operation Mode and Circular Buffer Enabled



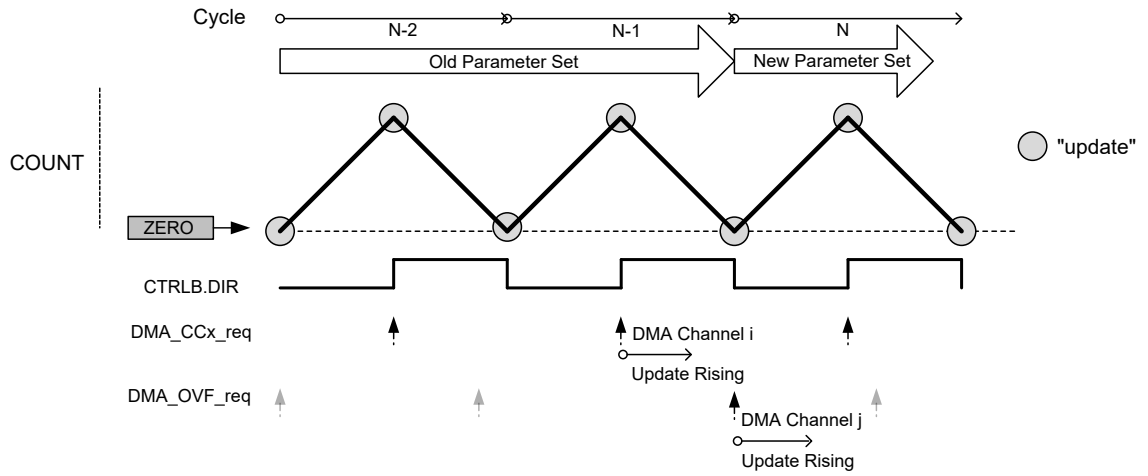
DMA Operation with Circular Buffer in DSBOTH Mode:
When a CC channel is selected as a circular buffer, the related DMA request is not set on a compare match detection but on start of down-counting phase.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of the up-counting phase with an effective DMA transfer on the previous down-counting phase (DMA acknowledge).

When up-counting, all circular buffer values can be updated through a DMA channel triggered by an MC trigger. When down-counting, all circular buffer values can be updated through a second DMA channel, triggered by the OVF DMA request.

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Figure 41-39. DMA Triggers in DSBOTH Operation Mode and Circular Buffer Enabled



41.6.5.2. Interrupts

The TCC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Retrigger (TRG)
- Count (CNT) – Refer also to the description of EVCTRL.CNTSEL
- Capture Overflow Error (ERR)
- Non-Recoverable Update Fault (UFS)
- Debug Fault State (DFS)
- Recoverable Faults (FAULTn)
- Non-recoverable Faults (FAULTx)
- Compare Match or Capture Channels (MCx)

These interrupts are asynchronous wake-up sources.

Each interrupt source has an Interrupt flag associated with it. The Interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the Interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the Interrupt flag is cleared, the interrupt is disabled or the TCC is reset. See *INTFLAG* from Related Links for details on how to clear Interrupt flags. The TCC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which Interrupt condition is present.

Interrupts must be globally enabled for interrupt requests to be generated. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links

Nested Vector Interrupt Controller (NVIC)

INTFLAG

Interrupt Flag Status and Clear

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41.6.5.3. Events

The TCC can generate the following output events:

- Overflow/Underflow (OVF)
- Trigger (TRG)
- Counter (CNT) (For further details, refer to the EVCTRL.CNTSEL description.)
- Compare Match or Capture on compare/capture channels: MCx

Writing a '1' ('0') to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables (disables) the corresponding output event. See *Event System (EVSYS)* from Related Links.

The TCC can take the following actions on a channel input event (MCx):

- Capture event
- Generate a recoverable or non-recoverable fault

The TCC can take the following actions on counter Event 1 (TCCx EV1):

- Counter re-trigger
- Counter direction control
- Stop the counter
- Decrement the counter on event
- Period and pulse width capture
- Non-recoverable fault

The TCC can take the following actions on counter Event 0 (TCCx EV0):

- Counter re-trigger
- Count on event (increment or decrement, depending on counter direction)
- Counter start – Start counting on the event rising edge. Further events will not restart the counter; the counter will keep counting using prescaled GCLK_TCCx, until it reaches TOP or ZERO, depending on the direction.
- Counter increment on event. This will increment the counter, irrespective of the counter direction.
- Count during active state of an asynchronous event (increment or decrement, depending on counter direction). In this case, the counter will be incremented or decremented on each cycle of the prescaled clock, as long as the event is active.
- Non-recoverable fault

The counter Event Actions are available in the Event Control registers (EVCTRL.EVACT0 and EVCTRL.EVACT1). See *EVCTRL* from Related Links.

Writing a '1' ('0') to an Event Input bit in the Event Control register (EVCTRL.MCEIx or EVCTRL.TCEIx) enables (disables) the corresponding action on input event.

Note: When several events are connected to the TCC, the enabled action will apply for each of the incoming events. See *Event System (EVSYS)* from Related Links for details on how to configure the Event System.

Related Links

Event System (EVSYS)

EVCTRL

Event Control

EVCTRL

Event Control

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41.6.6. Sleep Mode Operation

The TCC can be configured to operate in any sleep mode (Standby Sleep, Idle). To be able to run in standby sleep mode, the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. This peripheral can wake up the device from any sleep mode using interrupts or perform actions through the Event System.

41.6.7. Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)
- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Status register (STATUS)
- Pattern and Pattern Buffer registers (PATT and PATTB)
- Waveform register (WAVE)
- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERB)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBx)

The following registers are synchronized when read:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Count Value register (COUNT): synchronization is done on demand through READSYNC command (CTRLBSET.CMD)
- Pattern and Pattern Buffer registers (PATT and PATTB)
- Waveform register (WAVE)
- Period Value and Period Buffer Value registers (PER and PERB)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBx)

Required write synchronization is denoted by the Write-Synchronized property in the register description.

Required read synchronization is denoted by the Read-Synchronized property in the register description.

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41.7. Register Summary

See the *TCCx (x = 0 to 2)* module in the *Product Memory Mapping Overview* from Related Links for the base address based on the TCC instant used.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0		RESOLUTION[1:0]					ENABLE	SWRST
		15:8	MSYNC		PRESCYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
		23:16	DMAOS							
		31:24			CPTEN5	CPTEN4	CPTEN3	CPTEN2	CPTEN1	CPTEN0
0x04	CTRLBCLR	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x06 ... 0x07	Reserved									
0x08	SYNCBUSY	7:0	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
		15:8			CC5	CC4	CC3	CC2	CC1	CC0
		23:16								
		31:24								
0x0C	FCTRLA	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
		15:8	BLANKPRESC	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
		23:16	BLANKVAL[7:0]							
		31:24					FILTERVAL[3:0]			
0x10	FCTRLB	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
		15:8	BLANKPRESC	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
		23:16	BLANKVAL[7:0]							
		31:24					FILTERVAL[3:0]			
0x14	WEXCTRL	7:0							OTMX[1:0]	
		15:8						DTIEN2	DTIEN1	DTIEN0
		23:16	DTLS[7:0]							
		31:24	DTHS[7:0]							
0x18	DRVCTRL	7:0			NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
		15:8			NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
		23:16			INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0
		31:24	FILTERVAL1[3:0]				FILTERVAL0[3:0]			
0x1C ... 0x1D	Reserved									
0x1E	DBGCTRL	7:0						FDDBD		DBGRUN
0x1F	Reserved									
0x20	EVCTRL	7:0	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
		15:8	TCEI1	TCEI0	TCINV1	TCINV0		CNTEO	TRGEO	OVFEO
		23:16			MCEI5	MCEI4	MCEI3	MCEI2	MCEI1	MCEI0
		31:24			MCEO5	MCEO4	MCEO3	MCEO2	MCEO1	MCEO0
0x24	INTENCLR	7:0					ERR	CNT	TRG	OVF
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
		23:16			MC5	MC4	MC3	MC2	MC1	MC0
		31:24								
0x28	INTENSET	7:0					ERR	CNT	TRG	OVF
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
		23:16			MC5	MC4	MC3	MC2	MC1	MC0
		31:24								
0x2C	INTFLAG	7:0					ERR	CNT	TRG	OVF
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
		23:16			MC5	MC4	MC3	MC2	MC1	MC0
		31:24								
0x30	STATUS	7:0	PERBV		PATTBV	CLIENT	DFS	UFS	IDX	STOP
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN
		23:16			CCBV5	CCBV4	CCBV3	CCBV2	CCBV1	CCBV0
		31:24			CMP5	CMP4	CMP3	CMP2	CMP1	CMP0

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x34	COUNT	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
		23:16	COUNT[23:16]							
		31:24								
0x38	PATT	7:0			PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
		15:8			PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
0x3A ... 0x3B	Reserved									
0x3C	WAVE	7:0	CIPEREN		RAMP[1:0]			WAVEGEN[2:0]		
		15:8					CICCEN3	CICCEN2	CICCEN1	CICCEN0
		23:16			POL5	POL4	POL3	POL2	POL1	POL0
		31:24						SWAP2	SWAP1	SWAP0
0x40	PER	7:0	PER[1:0]		DITHER[5:0]					
		15:8	PER[9:2]							
		23:16	PER[17:10]							
		31:24								
0x44	CCx0	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x48	CCx1	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x4C	CCx2	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x50	CCx3	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x54	CCx4	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x58	CCx5	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x5C ... 0x63	Reserved									
0x64	PATTB	7:0			PGEB5	PGEB4	PGEB3	PGEB2	PGEB1	PGEB0
		15:8			PGVB5	PGVB4	PGVB3	PGVB2	PGVB1	PGVB0
0x66 ... 0x6B	Reserved									
0x6C	PERB	7:0	PERB[1:0]		DITHERB[5:0]					
		15:8	PERB[9:2]							
		23:16	PERB[17:10]							
		31:24								
0x70	CCBx0	7:0	CCB[1:0]		DITHERB[5:0]					
		15:8	CCB[9:2]							
		23:16	CCB[17:10]							
		31:24								

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x74	CCBx1	7:0	CCB[1:0]		DITHERB[5:0]					
		15:8	CCB[9:2]							
		23:16	CCB[17:10]							
		31:24								
0x78	CCBx2	7:0	CCB[1:0]		DITHERB[5:0]					
		15:8	CCB[9:2]							
		23:16	CCB[17:10]							
		31:24								
0x7C	CCBx3	7:0	CCB[1:0]		DITHERB[5:0]					
		15:8	CCB[9:2]							
		23:16	CCB[17:10]							
		31:24								
0x80	CCBx4	7:0	CCB[1:0]		DITHERB[5:0]					
		15:8	CCB[9:2]							
		23:16	CCB[17:10]							
		31:24								
0x84	CCBx5	7:0	CCB[1:0]		DITHERB[5:0]					
		15:8	CCB[9:2]							
		23:16	CCB[17:10]							
		31:24								

Related Links

Product Memory Mapping Overview

41.8. Register Description

Registers can be 8, 16 or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the Read-Synchronized and/or Write-Synchronized property in each individual register description.

Optional write protection by the PAC is denoted by the PAC Write Protection property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the Enable-Protected property in each individual register description.

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41.8.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized (ENABLE, SWRST)

Bit	31	30	29	28	27	26	25	24
			CPTEN5	CPTEN4	CPTEN3	CPTEN2	CPTEN1	CPTEN0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DMAOS							
Access	R/W							
Reset	0							

Bit	15	14	13	12	11	10	9	8
	MSYNC		PRESCYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RESOLUTION[1:0]					ENABLE	SWRST
Access		R/W	R/W				R/W	R/W
Reset		0	0				0	0

Bits 24, 25, 26, 27, 28, 29 – CPTEN Capture Channel x Enable
These bits are used to select the capture or compare operation on channel x.
Writing a '1' to CPTENx enables capture on channel x.
Writing a '0' to CPTENx disables capture on channel x.

Bit 23 – DMAOS DMA One-Shot Trigger Mode
This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit generates a DMA trigger on the TCC cycle following a TCC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit generates DMA triggers on each TCC cycle.
This bit is not synchronized.
Note: DMA One-Shot mode is not available in RAMP1/RAMP2C/RAMP2CS modes.

Value	Description
0	The TCC controls its own counter.
1	The counter is controlled by its Host TCC.

Bit 15 – MSYNC Host Synchronization (only for TCC client instance)
This bit must be set if the TCC counting operation must be synchronized on its Host TCC.
This bit is not synchronized.

Value	Description
0	The TCC controls its own counter.
1	The counter is controlled by its Host TCC.

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Bits 13:12 – PRESCYNC[1:0] Prescaler and Counter Synchronization

These bits select if, on re-trigger event, the Counter is cleared or reloaded on either the next GCLK_TCCx clock or on the next prescaled GCLK_TCCx clock. It is also possible to reset the prescaler on the re-trigger event.
These bits are not synchronized.

Value	Name	Description	
		Counter Reloaded	Prescaler
0x0	GCLK	Reload or reset Counter on next GCLK	—
0x1	PRESC	Reload or reset Counter on next prescaler clock	—
0x2	RESYNC	Reload or reset Counter on next GCLK	Reset prescaler counter
0x3	Reserved	—	—

Bit 11 – RUNSTDBY Run in Standby

This bit is used to keep the TCC running in Standby mode.
This bit is not synchronized.

Value	Description
0	The TCC is halted in Standby mode.
1	The TCC continues to run in Standby mode.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the Counter prescaler factor.
These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TCC
0x1	DIV2	Prescaler: GCLK_TCC/2
0x2	DIV4	Prescaler: GCLK_TCC/4
0x3	DIV8	Prescaler: GCLK_TCC/8
0x4	DIV16	Prescaler: GCLK_TCC/16
0x5	DIV64	Prescaler: GCLK_TCC/64
0x6	DIV256	Prescaler: GCLK_TCC/256
0x7	DIV1024	Prescaler: GCLK_TCC/1024

Bits 6:5 – RESOLUTION[1:0] Dithering Resolution

These bits increase the TCC resolution by enabling the dithering options.
These bits are not synchronized.

Table 41-9. Dithering

Value	Name	Description
0x0	NONE	The dithering is disabled.
0x1	DITH4	Dithering is done every 16 PWM frames. PER[3:0] and CCx[3:0] contain dithering pattern selection.
0x2	DITH5	Dithering is done every 32 PWM frames. PER[4:0] and CCx[4:0] contain dithering pattern selection.
0x3	DITH6	Dithering is done every 64 PWM frames. PER[5:0] and CCx[5:0] contain dithering pattern selection.

Bit 1 – ENABLE Enable

Due to synchronization, there is a delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE reads back immediately, and the ENABLE bit in the SYNCBUSY register (SYNCBUSY.ENABLE) is set. SYNCBUSY.ENABLE is cleared when the operation is complete.

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Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.
Writing a '1' to this bit resets all registers in the TCC (except DBGCTRL) to their initial state and the TCC is disabled.
Writing a '1' to CTRLA.SWRST always takes precedence; all other writes in the same write-operation are discarded.
Due to synchronization, there is a delay from writing CTRLA.SWRST until the Reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the Reset is complete.

Value	Description
0	There is no Reset operation ongoing.
1	The Reset operation is ongoing.

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41.8.2. Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

The user can change this register without doing a read-modify-write operation. Changes in this register will, also, be reflected in the Control B Set (CTRLBSET) register.

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – CMD[2:0] TCC Command
Writing a '0' to this bit group has no effect.
Writing a '1' to any of these bits clears the pending command.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Clear start, restart or retrigger
0x2	STOP	Force stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force COUNT read synchronization
0x5	DMAOS	One-shot DMA trigger

Bits 4:3 – IDXCMD[1:0] Ramp Index Command
These bits can be used to force cycle A and cycle B changes in the RAMP2 and RAMP2A operation. On the timer/counter update condition, the command is executed, the IDX flag in STATUS register is updated and the IDXCMD command is cleared.
Writing a '0' to these bits has no effect.
Writing a '1' to any of these bits clears the pending command.

Value	Name	Description
0x0	DISABLE	DISABLE Command disabled: IDX toggles between cycles A and B
0x1	SET	Set IDX: cycle B will be forced in the next cycle
0x2	CLEAR	Clear IDX: cycle A will be forced in next cycle
0x3	HOLD	Hold IDX: the next cycle will be the same as the current cycle.

Bit 2 – ONESHOT One-Shot
This bit controls the one-shot operation of the TCC. When the one-shot operation is enabled, the TCC stops counting on the next overflow/underflow condition or on a stop command.
Writing a '0' to this bit has no effect
Writing a '1' to this bit disables the one-shot operation.

Value	Description
0	The TCC will update the counter value on overflow/underflow condition and continue operation.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TCC buffered registers.
When CTRLB.LUPD is cleared, the hardware UPDATE registers, with the value from their buffered registers, are enabled.
This bit has no effect when the input capture operation is enabled.
Writing a '0' to this bit has no effect.

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Writing a '1' to this bit enables the registers updates on the hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB and PGEB buffer registers values are copied into the corresponding CCx, PER, PGV and PGE registers on hardware update condition.
1	The CCBx, PERB, PGVB and PGEB buffer registers values are not copied into the corresponding CCx, PER, PGV and PGE registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit set the bit and makes the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

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41.8.3. Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

The user can change this register without doing a read-modify-write operation. Changes in this register will, also, be reflected in the Control B Clear (CTRLBCLR) register.

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – CMD[2:0] TCC Command
These bits can be used for software control of the re-triggering and stop commands of the TCC. When a command is executed, the CMD bit field will be read back as zero. The commands are executed on the next prescaled GCLK_TCCx clock cycle.
Writing a '0' to this bit has no effect.
Writing a valid value to this bit group, as shown in the following table, will set the associated command.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force start, restart or retrigger
0x2	STOP	Force stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT
0x5	DMAOS	One-shot DMA trigger

Bits 4:3 – IDXCMD[1:0] Ramp Index Command
These bits can be used to force cycle A and cycle B changes in the RAMP2 and RAMP2A operation. On the timer/counter update condition, the command is executed, the IDX flag in the STATUS register is updated and the IDXCMD command is cleared.
Writing a '0' to this bit has no effect.
Writing a valid value to these bits will set a command.

Value	Name	Description
0x0	DISABLE	Command disabled: IDX toggles between cycles A and B
0x1	SET	Set IDX: cycle B will be forced in the next cycle
0x2	CLEAR	Clear IDX: cycle A will be forced in next cycle
0x3	HOLD	Hold IDX: the next cycle will be the same as the current cycle.

Bit 2 – ONESHOT One-Shot
This bit controls one-shot operation of the TCC. When in one-shot operation, the TCC will stop counting on the next overflow/underflow condition or a stop command.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will enable the one-shot operation.

Value	Description
0	The TCC will count continuously.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TCC buffered registers.

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When CTRLB.LUPD is set, the hardware UPDATE registers, with the value from their buffered registers, are disabled. Disabling the update ensures that all buffer registers are valid before a hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when the input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will disable the register's updates on the hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB and PGEB buffer registers values *are* copied into the corresponding CCx, PER, PGV and PGE registers on hardware update condition.
1	The CCBx, PERB, PGVB and PGEB buffer registers values are *not* copied into CCx, PER, PGV and PGE registers on hardware update condition.

Bit 0 – DIR Counter Direction

Note: When down-counting, the COUNT register must be initialized to TOP value (PER or CC0 value depending on the mode).

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the bit and make the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

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41.8.4. Synchronization Busy

Name: SYNCBUSY
Offset: 0x08
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			CC5	CC4	CC3	CC2	CC1	CC0
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13 – CC Compare/Capture Channel x Synchronization Busy
This bit is cleared when the synchronization of Compare/Capture Channel x register between the clock domains is complete.
This bit is set when the synchronization of Compare/Capture Channel x register between clock domains is started.
CCx bit is available only for existing Compare/Capture Channels. For details on CC channels number, refer to each TCC feature list.
This bit is set when the synchronization of CCx register between clock domains is started.

Bit 7 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER register between the clock domains is complete.
This bit is set when the synchronization of PER register between clock domains is started.

Bit 6 – WAVE WAVE Synchronization Busy
This bit is cleared when the synchronization of WAVE register between the clock domains is complete.
This bit is set when the synchronization of WAVE register between clock domains is started.

Bit 5 – PATT PATT Synchronization Busy
This bit is cleared when the synchronization of PATTERN register between the clock domains is complete.
This bit is set when the synchronization of PATTERN register between clock domains is started.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT register between the clock domains is complete.

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This bit is set when the synchronization of COUNT register between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS register between the clock domains is complete.
This bit is set when the synchronization of STATUS register between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB register between the clock domains is complete.
This bit is set when the synchronization of CTRLB register between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.
This bit is set when the synchronization of SWRST bit between clock domains is started.

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41.8.5. Fault Control A and B

Name: FCTRLn
Offset: 0x0C + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
					FILTERVAL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BLANKVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BLANKPRESC	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bits 27:24 – FILTERVAL[3:0] Recoverable Fault n Filter Value
These bits define the filter value applied on MCEx (x=0,1) event input line. The value must be set to zero when MCEx event is used as synchronous event.

Bits 23:16 – BLANKVAL[7:0] Recoverable Fault n Blanking Value
These bits determine the duration of the blanking of the fault input source. Activation and edge selection of the blank filtering are done by the BLANK bits (FCTRLn.BLANK).
When enabled, the fault input source is internally disabled for BLANKVAL* prescaled GCLK_TCCx periods after the detection of the waveform edge.

Bit 15 – BLANKPRESC Recoverable Fault n Blanking Value Prescaler
This bit enables a factor 64 prescaler factor on used as base frequency of the BLANKVAL value.

Value	Description
0	Blank time is BLANKVAL* prescaled GCLK_TCCx.
1	Blank time is BLANKVAL* 64 * prescaled GCLK_TCCx.

Bits 14:12 – CAPTURE[2:0] Recoverable Fault n Capture Action
These bits select the capture and Fault n interrupt/event conditions.

Table 41-10. Fault n Capture Action

Value	Name	Description
0x0	DISABLE	Capture on valid recoverable Fault n is disabled
0x1	CAPT	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each new captured value.

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Table 41-10. Fault n Capture Action (continued)

Value	Name	Description
0x2	CAPTMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is lower than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local minimum detection.
0x3	CAPTMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is higher than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local maximun detection.
0x4	LOCMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local minimum value detection.
0x5	LOCMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local maximun detection.
0x6	DERIV0	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local maximun or minimum detection.
0x7	CAPTMARK	Capture with ramp index as MSB value.

Bits 11:10 – CHSEL[1:0] Recoverable Fault n Capture Channel

These bits select the channel for capture operation triggered by recoverable Fault n.

Value	Name	Description
0x0	CC0	Capture value stored into CC0
0x1	CC1	Capture value stored into CC1
0x2	CC2	Capture value stored into CC2
0x3	CC3	Capture value stored into CC3

Bits 9:8 – HALT[1:0] Recoverable Fault n Halt Operation

These bits select the halt action for recoverable Fault n.

Value	Name	Description
0x0	DISABLE	Halt action disabled
0x1	HW	Hardware halt action
0x2	SW	Software halt action
0x3	NR	Non-recoverable fault

Bit 7 – RESTART Recoverable Fault n Restart

Setting this bit enables restart action for Fault n.

Value	Description
0	Fault n restart action is disabled.
1	Fault n restart action is enabled.

Bits 6:5 – BLANK[1:0] Recoverable Fault n Blanking Operation

These bits select the blanking start point for recoverable Fault n.

Value	Name	Description
0x0	START	Blanking applied from start of the Ramp period
0x1	RISE	Blanking applied from rising edge of the waveform output
0x2	FALL	Blanking applied from falling edge of the waveform output
0x3	BOTH	Blanking applied from each toggle of the waveform output

Bit 4 – QUAL Recoverable Fault n Qualification

Setting this bit enables the recoverable Fault n input qualification.

Value	Description
0	The recoverable Fault n input is not disabled on CMPx value condition.
1	The recoverable Fault n input is disabled when output signal is at inactive level (CMPx == 0).

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Bit 3 – KEEP Recoverable Fault n Keep
Setting this bit enables the Fault n keep action.

Value	Description
0	The Fault n state is released as soon as the recoverable Fault n is released.
1	The Fault n state is released at the end of TCC cycle.

Bits 1:0 – SRC[1:0] Recoverable Fault n Source
These bits select the TCC event input for recoverable Fault n.
Event system channel connected to MCEx event input, must be configured to route the event asynchronously, when used as a recoverable Fault n input.

Value	Name	Description
0x0	DISABLE	Fault input disabled
0x1	ENABLE	MCEx (x=0,1) event input
0x2	INVERT	Inverted MCEx (x=0,1) event input
0x3	ALTFAULT	Alternate fault (A or B) state at the end of the previous period.

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41.8.6. Waveform Extension Control

Name: WEXCTRL
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	DTHS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DTLS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
						DTIEN2	DTIEN1	DTIEN0
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
							OTMX[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 31:24 – DTHS[7:0] Dead-Time High Side Outputs Value
This register holds the number of GCLK_TCCx clock cycles for the dead-time high side.

Bits 23:16 – DTLS[7:0] Dead-time Low Side Outputs Value
This register holds the number of GCLK_TCCx clock cycles for the dead-time low side.

Bits 8, 9, 10 – DTIENx Dead-time Insertion Generator x Enable [x=0..2]
Setting any of these bits enables the dead-time insertion generator for the corresponding output matrix. This will override the output matrix [x] and [x+WO_NUM/2] with the low-side and high-side waveform, respectively.

Value	Description
0	No dead-time insertion override.
1	Dead time insertion override on signal outputs[x] and [x+WO_NUM/2] from the matrix outputs[x] signal.

Bits 1:0 – OTMX[1:0] Output Matrix
These bits define the matrix routing of the TCC waveform generation outputs to the port pins, according to Waveform Extension. See *Waveform Extension* from Related Links.

Related Links
Waveform Extension

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41.8.7. Driver Control

Name: DRVCTRL
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	FILTERVAL1[3:0]				FILTERVAL0[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 31:28 – FILTERVAL1[3:0] Non-Recoverable Fault Input 1 Filter Value
These bits define the filter value applied on the TCE1 event input line. When the TCE1 event input line is configured as a synchronous event, this value must be 0x0.

Bits 27:24 – FILTERVAL0[3:0] Non-Recoverable Fault Input 0 Filter Value
These bits define the filter value applied on the TCE0 event input line. When the TCE0 event input line is configured as a synchronous event, this value must be 0x0.

Bits 16, 17, 18, 19, 20, 21 – INVENx Waveform Output x Inversion [x=0..5]
These bits are used to select inversion on the output of channel x.
Writing a '1' to INVENx inverts output from WO[x].
Writing a '0' to INVENx disables inversion of output from WO[x].

Bits 8, 9, 10, 11, 12, 13 – NRVx NRVx Non-Recoverable State x Output Value [x=0..5]
These bits define the value of the enabled override outputs under the non-recoverable fault condition.

Bits 0, 1, 2, 3, 4, 5 – NREx Non-Recoverable State x Output Enable [x=0..5]
These bits enable the override of individual outputs by NRVx value under the non-recoverable fault condition.

Value	Description
0	Non-recoverable fault tri-state the output.
1	Non-recoverable faults set the output to NRVx level.

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41.8.8. Debug control

Name: DBGCTRL
Offset: 0x1E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						FDDBD		DBGRUN
Access						R/W		R/W
Reset						0		0

Bit 2 – FDDBD Fault Detection on Debug Break Detection

This bit is not affected by software Reset and must not be changed by software while the TCC is enabled.

By default, this bit is '0', and the On-Chip Debug (OCD) fault protection is disabled. When this bit is written to '1', an OCD break request from the OCD system triggers a non-recoverable fault. When this bit is set, the OCD fault protection is enabled and an OCD break request from the OCD system triggers a non-recoverable fault.

Value	Description
0	No faults are generated when TCC is halted in Debug mode.
1	A non recoverable fault is generated and FAULTD flag is set when TCC is halted in Debug mode.

Bit 0 – DBGRUN Debug Running State

This bit is not affected by a software Reset and must not be changed by software while the TCC is enabled.

Value	Description
0	The TCC is halted when the device is halted in Debug mode.
1	The TCC continues normal operation when the device is halted in Debug mode.

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41.8.9. Event Control

Name: EVCTRL
Offset: 0x20
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
			MCEO5	MCEO4	MCEO3	MCEO2	MCEO1	MCEO0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			MCEI5	MCEI4	MCEI3	MCEI2	MCEI1	MCEI0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TCEI1	TCEI0	TCINV1	TCINV0		CNTEO	TRGEO	OVFEO
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 24, 25, 26, 27, 28, 29 – MCEOx Match or Capture Channel x Event Output Enable [x=0..5]
These bits control if the match/capture event on channel x is enabled and will be generated for every match or capture.

Value	Description
0	Match/capture x event is disabled and will not be generated.
1	Match/capture x event is enabled and will be generated for every compare/capture on channel x.

Bits 16, 17, 18, 19, 20, 21 – MCEIx Match or Capture Channel x Event Input Enable [x=0..5]
These bits indicate if the match/capture x incoming event is enabled.
These bits are used to enable match or capture input events to the CCx channel of TCC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bits 14, 15 – TCEIx Timer/Counter Event Input x Enable [x=0..1]
This bit is used to enable input event x to the TCC.

Value	Description
0	Incoming event x is disabled.
1	Incoming event x is enabled.

Bits 12, 13 – TCINVx Timer/Counter Event x Invert Enable [x=0..1]
This bit inverts the event x input.

Value	Description
0	Input event source x is not inverted.

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Value	Description
1	Input event source x is inverted.

Bit 10 – CNTEO Timer/Counter Event Output Enable

This bit is used to enable the counter cycle event. When enabled, an event will be generated on the beginning or end of the counter cycle depending on the CNTSEL[1:0] settings.

Value	Description
0	Counter cycle output event is disabled and will not be generated.
1	Counter cycle output event is enabled and will be generated depending on CNTSEL[1:0] value.

Bit 9 – TRGEO Retrigger Event Output Enable

This bit is used to enable the counter retrigger event. When enabled, an event will be generated when the counter retriggers operation.

Value	Description
0	Counter retrigger event is disabled and will not be generated.
1	Counter retrigger event is enabled and will be generated for every counter retrigger.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable

This bit is used to enable the overflow/underflow event. When enabled, an event will be generated when the counter reaches the TOP or the ZERO value.

Value	Description
0	Overflow/underflow counter event is disabled and will not be generated.
1	Overflow/underflow counter event is enabled and will be generated for every counter overflow/underflow.

Bits 7:6 – CNTSEL[1:0] Timer/Counter Interrupt and Event Output Selection

These bits define on which part of the counter cycle the counter event output is generated.

Value	Name	Description
0x0	BEGIN	An interrupt/event is generated at begin of each counter cycle
0x1	END	An interrupt/event is generated at end of each counter cycle
0x2	BETWEEN	An interrupt/event is generated between each counter cycle.
0x3	BOUNDARY	An interrupt/event is generated at begin of first counter cycle, and end of last counter cycle.

Bits 5:3 – EVACT1[2:0] Timer/Counter Event Input 1 Action

These bits define the action the TCC will perform on the TCE1 event input.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start, restart or re-trigger TC on event
0x2	DIR (asynch)	Direction control
0x3	STOP	Stop TC on event
0x4	DEC	Decrement TC on event
0x5	PPW	Period captured into CC0 Pulse Width on CC1
0x6	PWP	Period captured into CC1 Pulse Width on CC0
0x7	FAULT	Non-recoverable Fault

Bits 2:0 – EVACT0[2:0] Timer/Counter Event Input 0 Action

These bits define the action the TCC will perform on TCE0 event input.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start, restart or re-trigger TC on event
0x2	COUNTEV	Count on event.
0x3	START	Start TC on event

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Value	Name	Description
0x4	INC	Increment TC on EVENT
0x5	COUNT (async)	Count on active state of asynchronous event
0x6	STAMP	Capture overflow times (Max value)
0x7	FAULT	Non-recoverable Fault

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41.8.10. Interrupt Enable Clear

Name: INTENCLR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			MC5	MC4	MC3	MC2	MC1	MC0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19, 20, 21 – MCx Match or Capture Channel x Interrupt Disable [x=0..5]
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 15 – FAULT1 Non-Recoverable Fault 1 Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Fault 1 Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault 1 interrupt.

Value	Description
0	The Non-Recoverable Fault 1 interrupt is disabled.
1	The Non-Recoverable Fault 1 interrupt is enabled.

Bit 14 – FAULT0 Non-Recoverable Fault 0 Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Fault 0 Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault 0 interrupt.

Value	Description
0	The Non-Recoverable Fault 0 interrupt is disabled.

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Value	Description
1	The Non-Recoverable Fault 0 interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Recoverable Fault B Interrupt Disable/Enable bit, which disables the Recoverable Fault B interrupt.

Value	Description
0	The Recoverable Fault B interrupt is disabled.
1	The Recoverable Fault B interrupt is enabled.

Bit 12 – FAULTA Recoverable Fault A Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Recoverable Fault A Interrupt Disable/Enable bit, which disables the Recoverable Fault A interrupt.

Value	Description
0	The Recoverable Fault A interrupt is disabled.
1	The Recoverable Fault A interrupt is enabled.

Bit 11 – DFS Non-Recoverable Debug Fault State Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Debug Fault State Interrupt Disable/Enable bit, which disables the Debug Fault State interrupt.

Value	Description
0	The Debug Fault State interrupt is disabled.
1	The Debug Fault State interrupt is enabled.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Error Interrupt Disable/Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 2 – CNT Counter Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Counter Interrupt Disable/Enable bit, which disables the Counter interrupt.

Value	Description
0	The Counter interrupt is disabled.
1	The Counter interrupt is enabled.

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Bit 1 – TRG Retrigger Interrupt Disable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Retrigger Interrupt Disable/Enable bit, which disables the Retrigger interrupt.

Value	Description
0	The Retrigger interrupt is disabled.
1	The Retrigger interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Disable/Enable bit, which disables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

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41.8.11. Interrupt Enable Set

Name: INTENSET
Offset: 0x28
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will, also, be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			MC5	MC4	MC3	MC2	MC1	MC0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19, 20, 21 – MC Match or Capture Channel x Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 15 – FAULT1 Non-Recoverable Fault 1 Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Non-Recoverable Fault 1 Interrupt Disable/Enable bit, which enables the Non-Recoverable Fault 1 interrupt.

Value	Description
0	The Non-Recoverable Fault 1 interrupt is disabled.
1	The Non-Recoverable Fault 1 interrupt is enabled.

Bit 14 – FAULT0 Non-Recoverable Fault 0 Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Non-Recoverable Fault 0 Interrupt Disable/Enable bit, which enables the Non-Recoverable Fault 0 interrupt.

Value	Description
0	The Non-Recoverable Fault 0 interrupt is disabled.

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Value	Description
1	The Non-Recoverable Fault 0 interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Recoverable Fault B Interrupt Disable/Enable bit, which enables the Recoverable Fault B interrupt.

Value	Description
0	The Recoverable Fault B interrupt is disabled.
1	The Recoverable Fault B interrupt is enabled.

Bit 12 – FAULTA Recoverable Fault A Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Recoverable Fault A Interrupt Disable/Enable bit, which enables the Recoverable Fault A interrupt.

Value	Description
0	The Recoverable Fault A interrupt is disabled.
1	The Recoverable Fault A interrupt is enabled.

Bit 11 – DFS Non-Recoverable Debug Fault State Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Debug Fault State Interrupt Disable/Enable bit, which enables the Debug Fault State interrupt.

Value	Description
0	The Debug Fault State interrupt is disabled.
1	The Debug Fault State interrupt is enabled.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which enables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Error Interrupt Disable/Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 2 – CNT Counter Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Counter Interrupt Disable/Enable bit, which enables the Counter interrupt.

Value	Description
0	The Counter interrupt is disabled.
1	The Counter interrupt is enabled.

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Bit 1 – TRG Retrigger Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Retrigger Interrupt Disable/Enable bit, which enables the Retrigger interrupt.

Value	Description
0	The Retrigger interrupt is disabled.
1	The Retrigger interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Disable/Enable bit, which enables the Overflow interrupt.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

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41.8.12. Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x2C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			MC5	MC4	MC3	MC2	MC1	MC0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19, 20, 21 – MCx Match or Capture Channel x Interrupt Flag [x=0..5]
This flag is set on the next CLK_TCC_COUNT cycle after a match with the compare condition or when the CCx register contains a valid capture value.
Writing a '0' to one of these bits has no effect.
Writing a '1' to one of these bits clears the corresponding Match or Capture Channel x interrupt flag.
In the Capture operation, this flag is automatically cleared when the CCx register is read.

Bit 15 – FAULT1 Non-Recoverable Fault 1 Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a Non-Recoverable Fault 1 occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Non-Recoverable Fault 1 interrupt flag.

Bit 14 – FAULT0 Non-Recoverable Fault 0 Interrupt Flag
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Non-Recoverable Fault 0 interrupt flag.

Bit 13 – FAULTB Recoverable Fault B Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a Recoverable Fault B occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Recoverable Fault B interrupt flag.

Bit 12 – FAULTA Recoverable Fault A Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a Recoverable Fault A occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Recoverable Fault A interrupt flag.

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Bit 11 – DFS Non-Recoverable Debug Fault State Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a Debug Fault State occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Debug Fault State interrupt flag.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Flag
This flag is set when the RAMP index changes and the Lock Update bit is set (CTRLBSET.LUPD).
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Non-Recoverable Update Fault Interrupt Flag.

Bit 3 – ERR Error Interrupt Flag
This flag is set if a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is one. In which case, there is no place to store the new capture.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Error interrupt flag.

Bit 2 – CNT Counter Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a counter event occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the CNT interrupt flag.

Bit 1 – TRG Retrigger Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a counter retrigger occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Retrigger interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after an overflow condition occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

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41.8.13. Status

Name: STATUS
Offset: 0x30
Reset: 0x00000001
Property: -

Note: Clear STATUS register bits by 32-bits write access only.

Bit	31	30	29	28	27	26	25	24
			CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			CCBV5	CCBV4	CCBV3	CCBV2	CCBV1	CCBV0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN
Access	R/W	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PERBV		PATTBV	CLIENT	DFS	UFS	IDX	STOP
Access	R/W		R/W	R	R/W	R/W	R	R
Reset	0		0	0	0	0	0	1

Bits 24, 25, 26, 27, 28, 29 – CMPx Channel x Compare Value [x=0..5]
This bit reflects the channel x output compare value.

Value	Description
0	Channel compare output value is 0.
1	Channel compare output value is 1.

Bits 16, 17, 18, 19, 20, 21 – CCBVx Channel x Compare or Capture Buffer Valid [x=0..5]
For a compare channel, this bit is set when a new value is written to the corresponding CCBx register. The bit is cleared either by writing a '1' to the corresponding location when CTRLB.LUPD is set or automatically on an UPDATE condition.
For a capture channel, the bit is set when a valid capture value is stored in the CCBx register. The bit is automatically cleared when the CCx register is read.

Bits 14, 15 – FAULTx Non-recoverable Fault x State [x=0..1]
This bit is set by hardware as soon as the non-recoverable Fault x condition occurs.
This bit is cleared by writing a one to this bit and when the corresponding FAULTxIN status bit is low. When this bit is clear, the timer/counter restarts from the last COUNT value. To restart the timer/counter from BOTTOM, the timer/counter restart command must be executed before clearing the corresponding FAULTx bit. For further details on timer/counter commands, refer to the available command description (CTRLBSET.CMD).

Bit 13 – FAULTB Recoverable Fault B State
This bit is set by hardware as soon as the recoverable Fault B condition occurs.

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This bit can be cleared by hardware when Fault B action is resumed or by writing a '1' to this bit when the corresponding FAULTBIN bit is low. If the software halt command is enabled (FAULTB.HALT = SW), clearing this bit releases the timer/counter.

Bit 12 – FAULTA Recoverable Fault A State
This bit is set by hardware as soon as the recoverable Fault A condition occurs.
This bit can be cleared by hardware when Fault A action is resumed or by writing a '1' to this bit when the corresponding FAULTAIN bit is low. If the software halt command is enabled (FAULTA.HALT = SW), clearing this bit releases the timer/counter.

Bit 11 – FAULT1IN Non-Recoverable Fault 1 Input
This bit is set while an active Non-Recoverable Fault 1 input is present.

Bit 10 – FAULT0IN Non-Recoverable Fault 0 Input
This bit is set while an active Non-Recoverable Fault 0 input is present.

Bit 9 – FAULTBIN Recoverable Fault B Input
This bit is set while an active Recoverable Fault B input is present.

Bit 8 – FAULTAIN Recoverable Fault A Input
This bit is set while an active Recoverable Fault A input is present.

Bit 7 – PERBV Period Buffer Valid
This bit is set when a new value is written to the PERB register. This bit is automatically cleared by hardware on the UPDATE condition when CTRLB.LUPD is set or by writing a '1' to this bit.

Bit 5 – PATTBV Pattern Generator Value Buffer Valid
This bit is set when a new value is written to the PATTB register. This bit is automatically cleared by hardware on the UPDATE condition when CTRLB.LUPD is set or by writing a '1' to this bit.

Bit 4 – CLIENT Client Mode Enable
This bit is set when TCC is set in Client mode. This bit follows the CTRLA.MSYNC bit state.

Bit 3 – DFS Debug Fault State
This bit is set by hardware in Debug mode when the DDBGCTRL.FDDBD bit is set. The bit is cleared by writing a '1' to this bit and when the TCC is not in Debug mode.
When the bit is set, the counter is halted and the Waveforms state depend on DRVCTRL.NRE and DRVCTRL.NRV registers.

Bit 2 – UFS Non-recoverable Update Fault State
This bit is set by hardware when the RAMP index changes and the Lock Update bit is set (CTRLBSET.LUPD). The bit is cleared by writing a one to this bit.
When the bit is set, the waveforms state depends on DRVCTRL.NRE and DRVCTRL.NRV registers.

Bit 1 – IDX Ramp Index
In RAMP2 and RAMP2A operation, the bit is cleared during the cycle A and set during the cycle B. In RAMP1 operation, the bit always reads '0'. See *Ramp Operations* from Related Links.

Bit 0 – STOP Stop
This bit is set when the TCC is disabled either on a STOP command or on an UPDATE condition when the One-Shot operation mode is enabled (CTRLBSET.ONESHOT = 1).
This bit is cleared on the next incoming counter increment or decrement.

Value	Description
0	Counter is running.

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Value	Description
1	Counter is stopped.

Related Links

Ramp Operations

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41.8.14. Counter Value

Name: COUNT
Offset: 0x34
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by the user writing the according TCC Command value to the Control B Set register (CTRLBSET.CMD = READSYNC).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – COUNT[23:0] Counter Value
These bits hold the value of the Counter register.
Notes:

- When the TCC is configured as a 16-bit timer/counter, the excess bits are read '0'.
- This bit field occupies the MSBs of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0 (depicted)
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6

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41.8.15. Pattern

Name: PATT
Offset: 0x38
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
			PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13 – PGVx Pattern Generation Output Value [x=0..5]
This register holds the values of pattern for each waveform output.

Bits 0, 1, 2, 3, 4, 5 – PGEx Pattern Generation Output Enable [x=0..5]
This register holds the enable status of pattern generation for each waveform output. A bit written to '1' overrides the corresponding SWAP output with the corresponding PGVx value.

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41.8.16. Waveform

Name: WAVE
Offset: 0x3C
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
						SWAP2	SWAP1	SWAP0
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	23	22	21	20	19	18	17	16
			POL5	POL4	POL3	POL2	POL1	POL0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					CICCEN3	CICCEN2	CICCEN1	CICCEN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CIPEREN		RAMP[1:0]			WAVEGEN[2:0]		
Access	R/W		R/W	R/W		R/W	R/W	R/W
Reset	0		0	0		0	0	0

Bits 24, 25, 26 – SWAPx Swap DTI Output Pair x [x=0..2]
Setting these bits enables the output swap of DTI outputs [x] and [x+WO_NUM/2]. Note: the DTIxEN settings will not affect the swap operation.

Bits 16, 17, 18, 19, 20, 21 – POLx Channel Polarity x [x=0..5]
Setting these bits enables the output polarity in single-slope and dual-slope PWM operations.

Value	Name	Description
0	(single-slope PWM waveform generation)	Compare output is initialized to ~DIR and set to DIR when TCC counter matches CCx value
1	(single-slope PWM waveform generation)	Compare output is initialized to DIR and set to ~DIR when TCC counter matches CCx value.
0	(dual-slope PWM waveform generation)	Compare output is set to ~DIR when TCC counter matches CCx value
1	(dual-slope PWM waveform generation)	Compare output is set to DIR when TCC counter matches CCx value.

Bits 8, 9, 10, 11 – CICCENx Circular CC Enable x [x=0..3]
Setting these bits enables the compare circular buffer option on the first four Compare/Capture channels. When the bit is set, the CCx register value is copied back into the CCBUFx register on the UPDATE condition.

Bit 7 – CIPEREN Circular Period Enable
Setting this bit enables the period circular buffer option. When the bit is set, the PER register value is copied back into the PERBUF register on the UPDATE condition.

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Bits 5:4 – RAMP[1:0] Ramp Operation

These bits select the Ramp operation (RAMP). These bits are not synchronized.

Value	Name	Description
0x0	RAMP1	RAMP1 operation
0x1	RAMP2A	Alternative RAMP2 operation
0x2	RAMP2	RAMP2 operation
0x3	RAMP2C	Critical RAMP2 operation

Bits 2:0 – WAVEGEN[2:0] Waveform Generation Operation

These bits select the waveform generation operation. The settings impact the top value and control if frequency or PWM waveform generation must be used. These bits are not synchronized.

Value	Name	Description						
		Operation	Top	Update	Waveform Output On Match	Waveform Output On Update	OVFIF/Event Up	Down
0x0	NFRQ	Normal Frequency	PER	TOP/Zero	Toggle	Stable	TOP	Zero
0x1	MFRQ	Match Frequency	CC0	TOP/Zero	Toggle	Stable	TOP	Zero
0x2	NPWM	Normal PWM	PER	TOP/Zero	Set	Clear	TOP	Zero
0x3	Reserved	—	—	—	—	—	—	—
0x4	DSCRITICAL	Dual-slope PWM	PER	Zero	~DIR	Stable	—	Zero
0x5	DSBOTTOM	Dual-slope PWM	PER	Zero	~DIR	Stable	—	Zero
0x6	DSBOTH	Dual-slope PWM	PER	TOP & Zero	~DIR	Stable	TOP	Zero
0x7	DSTOP	Dual-slope PWM	PER	Zero	~DIR	Stable	TOP	—

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41.8.17. Period Value

Name: PER
Offset: 0x40
Reset: 0x00FFFFFF
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PER[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	PER[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PER[1:0]		DITHER[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PER[17:0] Period Value
These bits hold the value of the TCC period count.
Note: When the TCC is configured as a 16-bit timer/counter, the excess bits are read as zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHER[5:0] Dithering Cycle Number
These bits hold the number of extra cycles that are added on the PWM pulse period every 64 PWM frames.
Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

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41.8.18. Compare/Capture Channel x

Name: CCx
Offset: 0x44 + x*0x04 [x=0..5]
Reset: 0x00000000
Property: Write-Synchronized, Read-Synchronized

The CCx register represents the 16-, 24- bit value, CCx. The register has two functions depending on the mode of operation.

For the capture operation, this register represents the second buffer level and access point for the CPU and DMA.

For the compare operation, this register is continuously compared to the counter value. Normally, the output from the comparator is, then, used for generating waveforms.

The CCx register is updated with the buffer value from their corresponding CCBx register when an UPDATE condition occurs.

In addition, in the match frequency operation, the CC0 register controls the counter period.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CC[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CC[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CC[1:0]		DITHER[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CC[17:0] Channel x Compare/Capture Value
These bits hold the value of the Channel x compare/capture register.
Notes:

1. When the TCC is configured as a 16-bit timer/counter, the excess bits are read as zero.
2. This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

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Bits 5:0 – DITHER[5:0] Dithering Cycle Number

These bits hold the number of extra cycles that are added on the PWM pulse width every 64 PWM frames.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

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41.8.19. Pattern Buffer

Name: PATTB
Offset: 0x64
Reset: 0x0000
Property: Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
			PGVB5	PGVB4	PGVB3	PGVB2	PGVB1	PGVB0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			PGEB5	PGEB4	PGEB3	PGEB2	PGEB1	PGEB0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13 – PGVBx Pattern Generation Output Value Buffer [x=0..5]
This register is the buffer for the PGV register. If double buffering is used, valid content in this register is copied to the PGVx register on an UPDATE condition.

Bits 0, 1, 2, 3, 4, 5 – PGEBx Pattern Generation Output Enable Buffer [x=0..5]
This register is the buffer of the PGE register. If double buffering is used, valid content in this register is copied into the PGEx register at an UPDATE condition.

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41.8.20. Period Buffer Value

Name: PERB
Offset: 0x6C
Reset: 0x00FFFFFF
Property: Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PERB[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	PERB[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PERB[1:0]		DITHERB[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PERB[17:0] Period Buffer Value
These bits hold the value of the Period Buffer register. The value is copied to the PER register on the UPDATE condition.
Note: When the TCC is configured as a 16-bit timer/counter, the excess bits are read as '0'.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERB[5:0] Dithering Buffer Cycle Number
These bits represent the PER.DITHER bits buffer. When the double buffering is enabled, the value of this bit field is copied to the PER.DITHER bits on an UPDATE condition.
Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	—
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

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41.8.21. Channel x Compare/Capture Buffer Value

Name: CCBx
Offset: 0x70 + x*0x04 [x=0..5]
Reset: 0x00000000
Property: Write-Synchronized, Read-Synchronized

CCBx is copied into CCx at TCC update time.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CCB[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CCB[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCB[1:0]		DITHERB[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CCB[17:0] Channel x Compare/Capture Buffer Value [x=0..5]
These bits hold the value of the Channel x Compare/Capture Buffer Value register. The register serves as the buffer for the associated compare or capture registers (CCx). Accessing this register using the CPU or DMA will affect the corresponding CCBVx status bit.
Notes:

1. When the TCC is configured as a 16-bit timer/counter, the excess bits are read as '0'.
2. This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERB[5:0] Dithering Buffer Cycle Number
These bits represent the CCx.DITHER bits buffer. When the double buffering is enabled, the DITHERBUF bits value is copied to the CCx.DITHER bits on an UPDATE condition.
Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	—
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

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42. 802.15.4 Bluetooth® Radio Subsystem

42.1. Overview

The PIC32CX-BZ6 provides an on-chip IEEE 802.15.4-compliant and Bluetooth Low Energy 6.0 interface with integrated transceivers. The Wireless Subsystem block comprises the following modules:

- Single ultra-low power 2.4 GHz ISM band RF transceiver
- Bluetooth modem
- Bluetooth link layer
- 802.15.4 modem
- 802.15.4 MAC

With integrated Ultra Low-Power 2.4 GHz ISM band single transceiver, modem and MAC, the radio supports both 802.15.4 stack and Bluetooth 6.0 link protocols. An on-board intelligent Radio Arbiter hardware allows the establishment of Bluetooth or 802.15.4 stack links with programmable QoS. The RF transceiver includes switching power amplifiers architecture and a TR switch. Therefore, medium to high power application use cases are supported without external FEM.

The RTOS running on the Cortex M4F CPU handles the arbitration between the application, the Bluetooth link stack, the 802.15.4 stack and miscellaneous maintenance tasks.

42.2. Features

2.4 GHz RF Transceiver

- Integrated 2.4 GHz Ultra-Low Power RF Transceiver Shared Between Bluetooth and 802.15.4 Modems and Link (MAC) Controllers
- Integrated Crystal Oscillator with Support for 16 MHz Crystal
- Internal Parallel PA Paths, Which May Be Shut Down to Control Pout as well as Current Consumption to Improve TX Power Efficiency
- Low BOM Single-Ended TRX RFFE Architecture
  - Integrated balun (single ended RF output) and TRX switch
- Hardware Radio Arbiter with Programmable QoS:
  - Resolution: up to per packet level
  - Based on shared transceiver and antenna

Bluetooth

- Bluetooth Low Energy 6.0 Certified
- Up to +11 dBm Programmable Transmit Output Power
- Typical Receiver Power Sensitivity:
  - -98 dBm for Bluetooth Low Energy 1 Mbps
  - -95 dBm for Bluetooth Low Energy 2 Mbps
  - -108 dBm for Bluetooth Low Energy 125 Kbps
  - -102 dBm for Bluetooth Low Energy 500 Kbps
- Wideband RSSI
  - Enables Interference Robustness and Higher Tolerance to Out-of-Band Blockers
- Bluetooth-Supported Features:
  - 2M uncoded PHY

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  - Long range (Coded PHY)
  - Channel selection algorithm #2
  - Advertising extensions, offloads CPU with hardware based scheduler
  - High duty cycle non-connectible advertising
  - Data length extensions
  - Secure connections
  - Privacy upgrades (with hardware white-list support)
- ECDH P256 Hardware Engine for Link Key Generation When Bluetooth Pairing
- AES128 Hardware Module for Real-Time Bluetooth Payload Data Encryption
- HCI Interface via UART
- LE Power Control
- Bluetooth Low Energy Profiles/Services:
  - Bluetooth Low Energy peripheral and central roles
  - Bluetooth Low Energy APIs for application layer to implement standard or customize GATT based profiles/ services
  - Over-the-air (OTA) update

802.15.4

- PSDU Data Rate: 250 Kbps
- Programmable RX Mode
  - -103 dBm RX sensitivity (typical) in the Continuous mode
  - -100 dBm sensitivity in the RPC mode
  - RPC mode provides lower power consumption in the RX mode to support California Green Energy Specification at the system level
- TX Output Power Up to +11 dBm
- Hardware-Assisted MAC
  - Auto acknowledge
  - Auto retry
  - Channel access back-off
- SFD Detection; Spreading; De-spreading; Framing; CRC-16 Computation
- Independent TX/RX Buffers for Improved CPU Offloading while Handling Upper Layer Data
  - 128-byte TX and 128-byte RX frame buffer
- Hardware Security
  - Advanced Encryption Standard (AES)
  - True Random Number Generator (TRNG)

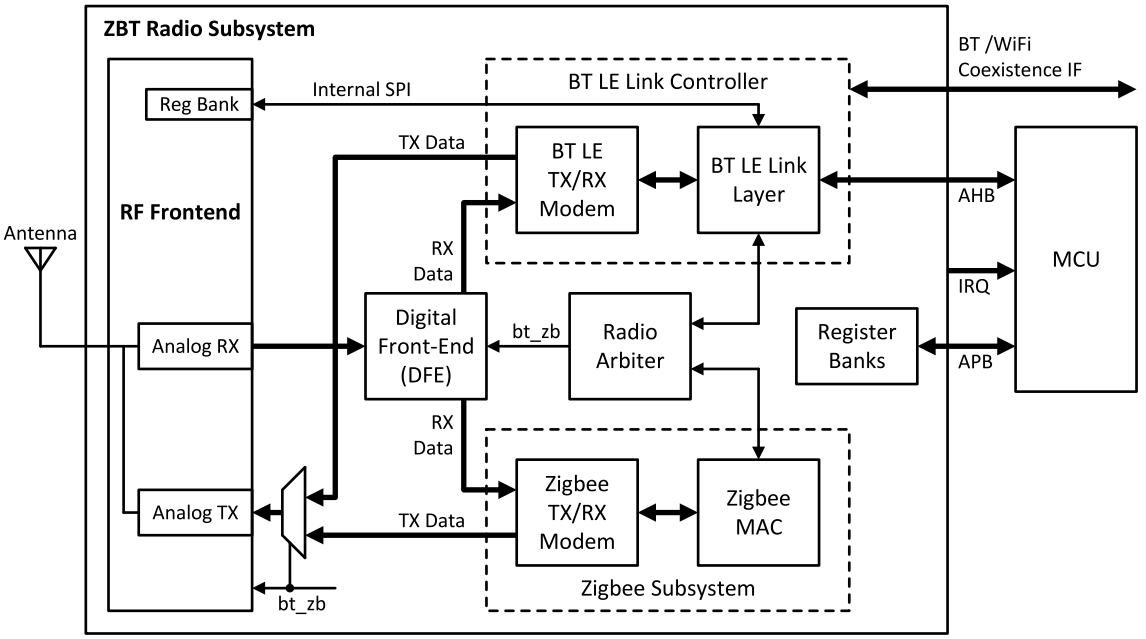
Proprietary Modulation Schemes

- 500 kbps and 1 Mbps are 2.4 GHz Proprietary with DSSS
- 2 Mpbs are 2.4 GHz Proprietary Without DSSS
- Typical Sensitivity Level for the Proprietary Data Rates:
  - 500 Kbps: -98 dBm
  - 1 Mbps: -96 dBm
  - 2 Mbps: -90 dBm

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42.3. Wireless Subsystem Top Level Diagram

Figure 42-1. Wireless Subsystem Top Level Diagram



42.4. Analog RF Front-End

The analog front-end contains the following:

- RF antenna switch
- XTO, connecting to a 16 MHz crystal oscillator
- RF synthesizer
- Analog RX path (LNA, mixer, IF amplifier)
- ADC
- Analog TX path (power amplifier)
- System clock PLL
- RF-related power management (RF-LDOs)
- Analog control logic

42.5. Digital Front-end

The Digital Front-End (DFE) connects to the analog front-end on one side and the Bluetooth or 802.15.4 baseband on the other side. In the receive path, the I/Q data from the ADC are filtered and down-converted. Automatic gain control is also implemented in the DFE. In the transmit path, the 802.15.4 power control is done in the DFE.

42.6. Bluetooth Low Energy Link Controller

The Bluetooth Low Energy link controller consists of the TX/RX modem and the link layer. The modem is responsible for modulation and demodulation of the digital IF data for both Bluetooth classic and Bluetooth Low Energy.

The baseband link layer carries out all Bluetooth operations as transmit or receive tasks. There are several task managers:

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1. Firmware – Firmware can trigger tasks by writing the task controller registers.
2. Hardware schedule controller – This is Bluetooth Low Energy advertisement scheduler controller (Advertiser role).
3. Hardware scanner – This is Bluetooth Low Energy advertisement scanner (Central role).
4. Bluetooth Low Energy advertisement controller – This is Bluetooth Low Energy 4.2 advertisement controller (Advertiser role).

The requests from the task managers are arbitrated and carried out by the task controller.

The RX and TX data are written to common memory via DMA over an AHB interface.

42.7. 802.15.4 Subsystem

The 802.15.4 Subsystem deals with the physical/modem layer and the MAC layer. A digital baseband processor down-converts and demodulates the received IF data. The subsequent modules implement basic MAC functionality and hardware accelerators for features, such as automatic acknowledgment, CSMA_CA and retransmission or automatic FCS check. The flow control is done by a Finite State Machine (FSM). The data is stored in integrated 128-byte RX and TX frame buffers.

42.8. Radio Arbiter

The Radio Arbiter provides a low-level arbitration for using the single RF frontend for both 802.15.4 and Bluetooth links. The arbiter supports the following modes:

- BT static – Radio ownership is with the Bluetooth link controller
- ZB static – Radio ownership is with the 802.15.4 subsystem
- Dynamic – Radio ownership is decided dynamically at every arbitration event (default mode)

At any time, it is possible to configure the Radio Arbiter in either Bluetooth or 802.15.4 static mode. In these modes, no arbitration is done and the radio is owned by either the Bluetooth Link Controller or the 802.15.4 Subsystem.

42.9. Register Banks

The ZBT subsystem contains various register banks to configure and control the digital baseband hardware and state machines. The firmware accesses the registers by the ARM APB bus.

42.10. Coexistence Interface

Bluetooth and Wi-Fi partly operate in the same 2.4 GHz band. Therefore, transmissions can interfere with each other and impact the performance and reliability of the wireless systems. The Coexistence Interface is built from a 3-wire bus that mutually signalizes RF activity when Bluetooth and Wi-Fi chips are available in the same hardware module. Interference can, thus, be avoided.

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43. Controller Area Network (CAN)

43.1. Overview

The CAN communication controller provides hardware support for the CAN protocol version 2.0 part A and B and ISO 11898-1:2015 which includes the CAN Flexible Data Rate Frame format (CAN-FD). The CAN module uses system RAM, which it accesses through a Host AHB bus for FIFO and filter storage.

43.2. Features

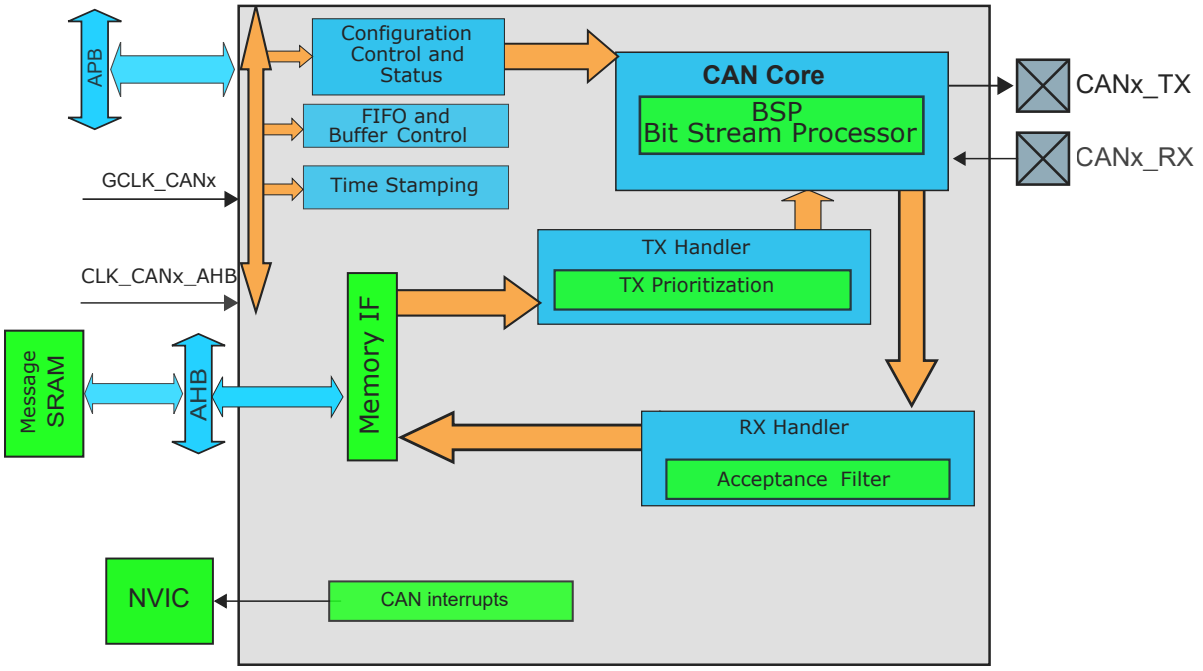
The following are key features of the CAN module:

- Conforms with CAN protocol version 2.0 part A and B plus ISO 11898-1:2015
- Up to two Controller Area Network
  - Supporting CAN2.0 A/B and CAN-FD (ISO 11898-1:2015)
- CAN Error Logging
- Acceptance filtering
  - Up to 128 configurable SID filters and 64 configurable EID filter
  - EID filters can be configured with masking of 29 bit Id's in SAE J1939
  - Separate signaling on reception of High Priority Messages
- AUTOSAR optimized
- SAE J1939 optimized
- Two configurable Receive FIFOs
- Up to 64 dedicated Receive Buffers and up to 32 dedicated Transmit Buffers
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable Loop-Back Test mode
- Maskable module interrupts
- Power-down support; Debug on CAN support
- Transfer rates:
  - 1 Mb/s for CAN 2.0 mode
  - Up to 10 Mb/s for CAN-FD mode

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43.3. Block Diagram

Figure 43-1. CAN Block Diagram



Note: x = 0, 1. This family of devices contain up to two CAN modules.

43.4. Signal Description

Table 43-1. Signal Description

PIN NAME	DESCRIPTION	TYPE
CAN0_RX	CAN0_FD Receive	Digital Input
CAN0_TX	CAN0_FD Transmit	Digital Output
CAN1_RX	CAN1_FD Receive	Digital Input
CAN1_TX	CAN1_FD Transmit	Digital Output

43.5. Peripheral Dependencies

Peripheral Name	Base Address	NVIC IRQ Index:Source	Peripheral Clock Enable/Disable	GCLK Peripheral Channel Clock Name : Register	PAC Peripheral ID (PAC.WRCTRL.PERIDx)	DMA Trigger Index:Source (DMAC.CHCTRLBk.TRIGx)	Power Domain
CAN0	0x4600_2000	51: LINE0, LINE1, ERROR	Peripheral Clock Disable: CFGPCLKGEN4[27]	GCLK_CAN0 : 28	104	67 : DEBUG	VDDREG
CAN1	0x4600_2400	52: LINE0, LINE1, ERROR	Peripheral Clock Disable: CFGPCLKGEN4[31]	GCLK_CAN1 : 29	105	68 : DEBUG	VDDREG

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Note: In order to use this peripheral, other parts of the system must be configured correctly, as described below.

43.5.1. I/O Lines

Using the CAN's I/O lines requires the I/O pins to be configured using the System Configuration and the I/O Peripheral Pin Select (PPS). See *System Configuration and Register Locking (CFG)* and *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.

Related Links

I/O Ports and Peripheral Pin Select (PPS)
System Configuration and Register Locking (CFG)

43.5.2. Clocks

The CAN bus clock (CLK_CAN_APB) can be enabled and disabled in the MCLK. A generic clock (GCLK_CAN) is required to clock the CAN. This clock must be configured and enabled in the generic clock controller before using the CAN. Refer to the generic clock controller chapter for details. One possible configuration is to use the UPLL/EPLL and a REFO divider to achieve the required clock frequency. This generic clock is asynchronous to the bus clock (CLK_CAN_APB). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains.

Note: Regardless of which clock source is used for the CAN, the CAN must receive a 20, 40 or 80 MHz clock to ensure compatibility with other CAN devices.

Note: The CAN IP requests clocks even when it is in reset, therefore any clock requests from the CAN macro should be gated off with the peripheral enable.

43.5.3. DMA

The CAN has a built-in Direct Memory Access (DMA) and will read/write data to/from the system RAM when a CAN transaction takes place. No CPU or DMA Controller (DMAC) resources are required. The DMAC can be used for debug messages functionality.

43.6. Functional Description

43.6.1. Principle of Operation

The CAN performs communication according to ISO 11898-1:2015 (identical to Bosch® CAN protocol specification 2.0 part A,B, ISO CAN FD).

For FIFO and filter storage, the CAN module uses system RAM, which it accesses through a host AHB bus. Each CAN FD instance may use up to 4864 words of system ram which is 17 KB of system memory.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM(1) as well as providing receive message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmit status information.

Acceptance filtering is implemented by a combination of up to up to 128 SID filters and up to 64 EID filter elements where each one can be configured as a range, as a bit mask, or as a dedicated ID filter.

Note:

1. The CAN macro will write and read to/from SRAM 4bytes aligned . User need to define the "Message RAM" as 4bytes aligned.

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43.6.2. Operating Modes

43.6.2.1. Software Initialization

Software initialization is started by setting the CCCR.INIT bit (CCCR <0>), either by software, or by going “bus off.” While the CCCR.INIT bit (CCCR <0>) is set, message transfer from and to the CAN bus is stopped, the status of the CAN bus output CANx_TX is ”recessive” (HIGH). The counters of the Error Management Logic EML are unchanged. Setting the CCCR.INIT bit (CCCR <0>) does not change any configuration register. Resetting the CCCR.INIT bit (CCCR <0>) finishes the software initialization. Afterwords the Bit Stream Processor (BSP) synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive ”recessive” bits (= Bus_Idle) before it can take part in bus activities and start the message transfer.

Access to the CAN configuration registers is only enabled when the CCCR.CCE bit (CCCR <1>) and the CCCR.INIT bit (CCCR <0>) are set (protected write).

The CCCR.CCE bit (CCCR <1>) can only be set and cleared while the CCCR.INIT bit (CCCR <0>) = ‘1’. The CCCR.CCE bit (CCCR <1>) is automatically cleared when the CCCR.INIT bit (CCCR <0>) is cleared.

The following registers are reset when the CCCR.CCE bit (CCCR <1>) is set

- HPMS - High Priority Message Status
- RXF0S - Rx FIFO 0 Status
- RXF1S - Rx FIFO 1 Status
- TXFQS - Tx FIFO/Queue Status
- TXBRP - Tx Buffer Request Pending
- TXBTO - Tx Buffer Transmission Occurred
- TXBCF - Tx Buffer Cancellation Finished
- TXEFS - Tx Event FIFO Status

The Timeout Counter value (TOCV.TOC) bits (TOCV <15:0>) is preset to the value configured by the TOCC.TOP bits (TOCC <31:16>) when the CCCR.CCE bit (CCCR <1>) is set.

In addition, the state machines of the Tx Handler and Rx Handler are held in idle state while the CCCR.CCE bit (CCCR <1>) = ‘1’.

The following registers are only writable while the CCCR.CCE bit (CCCR <1>) = ‘0’.

- TXBAR - Tx Buffer Add Request
- TXBCR - Tx Buffer Cancellation Request

The CCCR.TEST bit (CCCR <7>) and CCCR.MON bit (CCCR <5>) can only be set by the CPU while the CCCR.INIT bit (CCCR <0>) = ‘1’ and CCR.CCE bit (CCCR <1>) = ‘1’. Both bits may be cleared at any time. The CCCR.DAR bit (CCCR <6>) can only be set/cleared while the CCCR.INIT bit (CCCR <0>) = ‘1’ and the CCCR.CCE bit (CCCR <1>) = ‘1’.

43.6.2.2. Normal Operation

Once the CAN is initialized and the CCCR.INIT bit (CCCR <0>) is reset to ‘0’, the CAN synchronizes itself to the CAN bus and is ready for communication.

After passing the acceptance filtering, received messages including the message ID and DLC are stored into a dedicated Rx Buffer or into Rx FIFO0 or Rx FIFO1.

For messages to be transmitted dedicated Tx Buffers and/or a Tx FIFO or a Tx Queue can be initialized or updated. Automated transmission on reception of remote frames is not implemented.

43.6.2.3. CAN FD Operation

There are two variants in the CAN FD frame format, first the CAN FD frame without bit rate switching where the data field of a CAN frame may be longer than 8 bytes. The second variant is the CAN FD

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frame where control field, data field, and CRC field of a CAN frame are transmitted with a higher bit rate than the beginning and the end of the frame.

The previously reserved bit in standard CAN frames with 11-bit identifiers and the first previously reserved bit in extended CAN frames with 29-bit identifiers will now be decoded as FDF bit. A recessive FDF signifies a CAN FD frame, where as a dominant FDF bit signifies a Classic CAN frame. In a CAN FD frame, the two bits following FDF, (i.e.,res and BRS), decide whether the bit rate inside of this CAN FD frame is switched. A CAN FD bit rate switch is signified by a dominant res bit and a recessive BRS bit. The coding of a recessive res bit is reserved for future expansion of the protocol. In case the CAN receives a frame with a recessive FDF bit and a recessive res bit, it will signal a Protocol Exception Event by setting bit PSR.PXE bit (PSR <14>). When Protocol Exception Handling is enabled (CCCR.PXHD bit (CCCR<12>) = '0'), this causes the operation state to change from Receiver (PSR.ACT = "0x2") to synchronizing on CAN communication (PSR.ACT bits (PSR <4:3>) = "0x0") at the next sample point. In case Protocol Exception Handling is disabled (CCCR.PXHD bit (CCCR<12>) = '1'), the CAN will treat a recessive res bit as a form error and will respond with an error frame.

CAN FD operation is enabled by programming CCCR.FDOE bit (CCCR<8>). In case CCCR.FDOE bit (CCCR<8>) = '1', transmission and reception of CAN FD frames is enabled. Transmission and reception of Classic CAN frames is always possible. Whether a CAN FD frame or a Classic CAN frame is transmitted can be configured via FDF bit in the respective Tx Buffer element. With CCCR.FDOE bit (CCCR<8>) = '0', received frames are interpreted as Classic CAN frames, witch leads to the transmission of an error frame when receiving a CAN FD frame. When CAN FD operation is disabled, no CAN FD frames are transmitted even if FDF bit of a Tx Buffer element is set. CCCR.FDOE bit (CCCR<8>) and CCCR.BRSE bit (CCCR<9>) can only be changed while CCCR.INIT bit (CCCR <0>) and CCCR.CCE (CCCR <1>) are both set.

With CCCR.FDOE bit (CCCR<8>) = '0', the setting of FDF and BRS bits is ignored and frames are transmitted in Classic CAN format. With CCCR.FDOE bit (CCCR<8>) = '1' and CCCR.BRSE bit (CCCR<9>) = '0', only bit FDF of a Tx Buffer element is evaluated. With CCCR.FDOE bit (CCCR<8>) = '1' and CCCR.BRSE bit (CCCR<9>) = '1', transmission of CAN FD frames with bit rate switching is enabled. All Tx Buffer elements with FDF and BRS bits set are transmitted in CAN FD format with bit rate switching.

A mode change during CAN operation is only recommended under the following conditions:

- The failure rate in the CAN FD data phase is significantly higher than in the CAN FD arbitration phase. In this case disable the CAN FD bit rate switching option for transmissions.
- During system startup all nodes are transmitting Classic CAN messages until it is verified that they are able to communicate in CAN FD format. If this is true, all nodes switch to CAN FD operation.
- Wake-up messages in CAN Partial Networking have to be transmitted in Classic CAN format.
- End-of-line programming in case not all nodes are CAN FD capable. Non CAN FD nodes are held in silent mode until programming has completed. Then all nodes switch back to Classic CAN communication.

In the CAN FD format, the coding of the DLC differs from the standard CAN format. The DLC codes 0 to 8 have the same coding as in standard CAN. However, the codes 9 to 15, (which in standard CAN all code a data field of 8 bytes), are coded according to the following table.

Table 43-2. Coding of DLC in CAN FD

DLC	9	10	11	12	13	14	15
Number of Data Bytes	12	16	20	24	32	48	64

In CAN FD frames, the bit timing will be switched inside the frame, after the BRS (Bit Rate Switch) bit, if this bit is recessive. Before the BRS bit, in the CAN FD arbitration phase, the nominal CAN bit timing is used as defined by the Nominal Bit Timing & Prescaler Register (NBTP). In the following CAN FD data phase, the fast CAN bit timing is used as defined by the Data Bit Timing & Prescaler

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Register (DBTP). The bit timing is switched back from the fast timing at the CRC delimiter or when an error is detected, whichever occurs first.

The maximum configurable bit rate in the CAN FD data phase depends on the CAN clock frequency (GCLK_CANx). Example: with a CAN clock frequency of 20MHz and the shortest configurable bit time of 4 t_q, the bit rate in the data phase is 5 Mbit/s.

In both data frame formats, CAN FD long and CAN FD fast, the value of the bit ESI (Error Status Indicator) is determined by the transmitter's error state at the start of the transmission. If the transmitter is error passive, ESI is transmitted recessive, else it is transmitted dominant.

43.6.2.4. Transceiver Delay Compensation

During the data phase of a CAN FD transmission only one node is transmitting, all others are receivers. The length of the bus line has no impact. When transmitting via pin CANx_TX the CAN receives the transmitted data from its local CAN transceiver via pin CANx_RX. The received data is delayed by the CAN transceiver's loop delay. In case this delay is greater than TSEG1 (time segment before sample point), a bit error is detected. In order to enable a data phase bit time that is even shorter than the transceiver loop delay, the delay compensation is introduced. Without transceiver delay compensation, the bit rate in the data phase of a CAN FD frame is limited by the transceivers loop delay.

The CAN's protocol unit has implemented a delay compensation mechanism to compensate the transmitter delay, thereby enabling transmission with higher bit rates during the CAN FD data phase independent of the delay of a specific CAN transceiver.

To check for bit errors during the data phase of transmitting nodes, the delayed transmit data is compared against the received data at the Secondary Sample Point SSP. If a bit error is detected, the transmitter will react on this bit error at the next following regular sample point. During arbitration phase the delay compensation is always disabled.

The transmitter delay compensation enables configurations where the data bit time is shorter than the transmitter delay, it is described in detail in the new ISO11898-1. It is enabled by setting the DBTP.TDC bit (DBTP<23>).

The received bit is compared against the transmitted bit at the SSP. The SSP position is defined as the sum of the measured delay from the CAN's transmit output CANx_TX through the transceiver to the receive input CANx_RX plus the transmitter delay compensation offset as configured by TDCR.TDCO bits (TDCR <15:8>). The transmitter delay compensation offset is used to adjust the position of the SSP inside the received bit (e.g. half of the bit time in the data phase). The position of the secondary sample point is rounded down to the next integer number of minimum time quantum (mtq). 1 mtq is equal to time period of GCLK_CANx clock.

The PSR.TDCV bits (PSR <22:16>) show the actual transmitter delay compensation value. PSR.TDCV bits (PSR <22:16>) are cleared when CCCR.INIT bit (CCCR <0>) is set and is updated at each transmission of an FD frame while DBTP.TDC bit (DBTP <23>) is set.

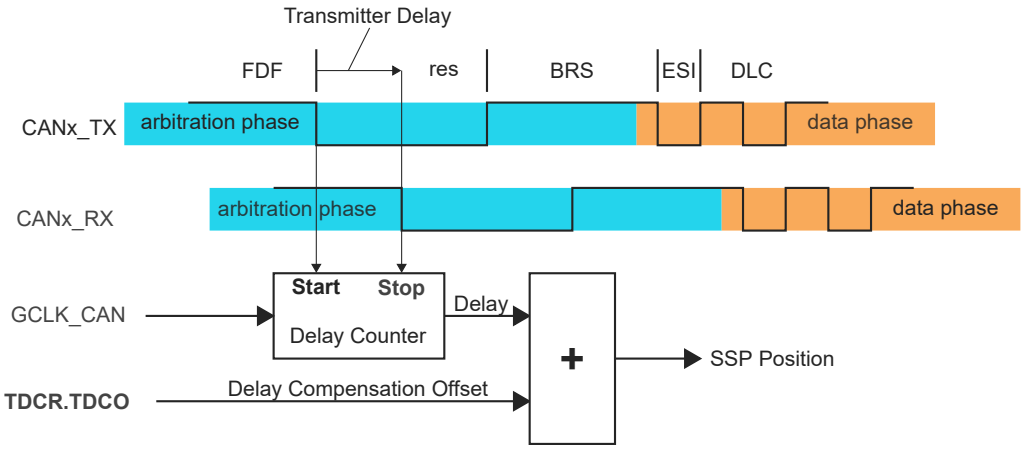
The following boundary conditions have to be considered for the transmitter delay compensation implemented in the CAN:

- The sum of the measured delay from CANx_TX to CANx_RX and the configured transceiver delay compensation offset FBTP.TDCR bits (TDCR <15:8>) has to be less than 6 bit times in the data phase.
- The sum of the measured delay from CANx_TX to CANx_RX and the configured transceiver delay compensation offset FBTP.TDCR bits (TDCR <15:8>) has to be less or equal to 127 mtq. In case this sum exceeds 127 mtq, the maximum value of 127 mtq is used for transceiver delay compensation.
- The data phase ends at the sample point of the CRC delimiter, that stops checking of receive bits at the SSPs.
  Transmitter Delay Compensation Measurement

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If transmitter delay compensation is enabled by programming the DBTP.TDC bit (DBTP <23>) = '1', the measurement is started within each transmitted CAN FD frame at the falling edge of bit FDF to bit res. The measurement is stopped when this edge is seen at the receive input CANx_TX of the transmitter. The resolution of this measurement is one mtq.

Figure 43-2. Transceiver delay measurement



To avoid that a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in a too early SSP position, the use of a transmitter delay compensation filter window can be enabled by programming TDCR.TDCF bit (TDCR <6:0>). This defines a minimum value for the SSP position. Dominant edges of CANx_RX, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least TDCR.TDCF bit (TDCR <6:0>) and CANx_RX is low.

43.6.2.5. Restricted Operation Mode

In Restricted Operation Mode the node is able to receive data and remote frames and to give acknowledge to valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The error counters (ECR.REC bit (ECR <14:8>), ECR.TEC bit (ECR <7:0>)) are frozen while Error Logging (ECR.CEL bit (ECR <23:16>)) is still incremented. The CPU can set the CAN into Restricted Operation mode by setting bit CCCR.ASM bit (CCCR <2>). The bit can only be set by the CPU when both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set to '1'. The bit can be reset by the CPU at any time.

Restricted Operation Mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation Mode, the CPU has to reset CCCR.ASM bit (CCCR <2>).

The Restricted Operation Mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation Mode after it has received a valid frame.

43.6.2.6. Bus Monitoring Mode

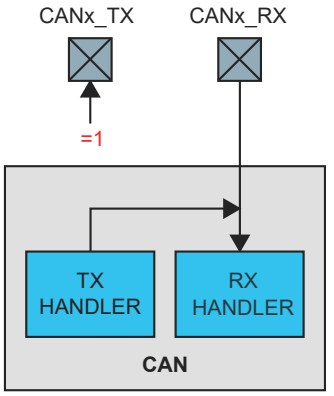
The CAN is set in Bus Monitoring Mode by programming CCCR.MON bit (CCCR <5>) to '1'. In Bus Monitoring Mode (see ISO 11898-1, 10.12 Bus monitoring), the CAN is able to receive valid data frames and valid remote frames, but cannot start a transmission. In this mode, it sends only recessive bits on the CAN bus. If the CAN is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the CAN monitors this dominant bit,

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although the CAN bus may remain in recessive state. In Bus Monitoring Mode register TXBRP is held in reset state.

The Bus Monitoring Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. The figure below shows the connection of signals CANx_TX and CANx_RX to the CAN in Bus Monitoring Mode.

Figure 43-3. Pin Control in Bus Monitoring Mode



Bus Monitoring Mode

43.6.2.7. Disabled Automatic Retransmission

According to the CAN Specification (see ISO 11898-1, 6.3.3 Recovery Management), the CAN provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled. To support time-triggered communication as described in ISO 11898-1, chapter 9.2, the automatic retransmission may be disabled via CCCR.DAR bit (CCCR <6>).

Frame Transmission in DAR Mode

In DAR mode all transmissions are automatically cancelled after they started on the CAN bus. A Tx Buffer's Tx Request Pending bit (TXBRP.TRPx) is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

- Successful transmission:
  - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set
  - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx not set
- Successful transmission in spite of cancellation:
  - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx set
  - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set
- Arbitration lost or frame transmission disturbed:
  - Corresponding Tx Buffer Transmission Occurred bit TXBTO.TOx not set
  - Corresponding Tx Buffer Cancellation Finished bit TXBCF.CFx set

In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = "10" (transmission in spite of cancellation).

43.6.2.8. Test Modes

To enable write access to register TEST, bit CCCR.TEST bit (CCCR <7>) has to be set to '1'. This allows the configuration of the test modes and test functions.

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Four output functions are available for the CAN transmit pin CANx_TX by programming TEST.TX bits (TEST <6:5>). Additionally to its default function – the serial data output – it can drive the CAN Sample Point signal to monitor the CAN's bit timing and it can drive constant dominant or recessive values. The actual value at pin CANx_RX can be read from TEST.RX bit (TEST <7>). Both functions can be used to check the CAN bus' physical layer.

Due to the synchronization mechanism between GCLK_CANx and CLK_CANx_AHB domains, there may be a delay of several CLK_CANx_AHB periods between writing to TEST.TX bits (TEST <6:5>) until the new configuration is visible at output pin CANx_TX. This applies also when reading input pin CANx_RX via TEST.RX bit (TEST <7>).

Note: Test modes should be used for production tests or self test only. The software control for pin CANx_TX interferes with all CAN protocol functions. It is not recommended to use test modes for application.

External Loop Back Mode

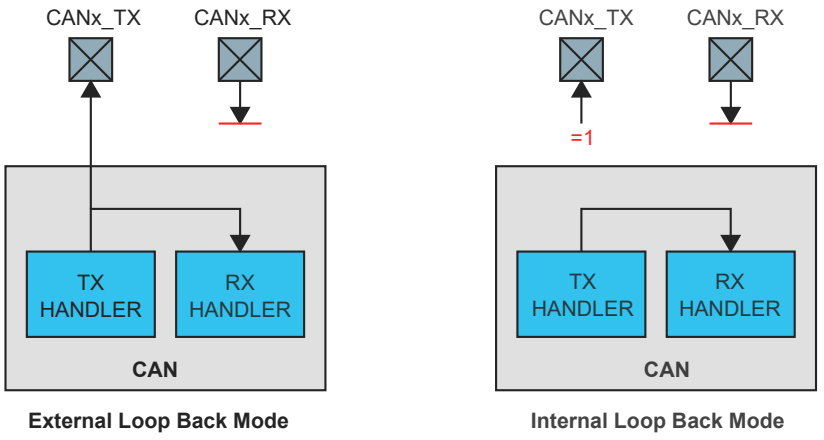
The CAN can be set in External Loop Back Mode by programming TEST.LBCK bit (TEST <4>) to '1'. In Loop Back Mode, the CAN treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into an Rx Buffer or an Rx FIFO. The figure below shows the connection of signals CANx_TX and CANx_RX to the CAN in External Loop Back Mode.

This mode is provided for hardware self-test. To be independent from external stimulation, the CAN ignores acknowledge errors (recessive bit sampled in the acknowledge slot of a data/remote frame) in Loop Back Mode. In this mode the CAN performs an internal feedback from its Tx output to its Rx input. The actual value of the CANx_RX input pin is disregarded by the CAN. The transmitted messages can be monitored at the CANx_TX pin.

Internal Loop Back Mode

Internal Loop Back Mode is entered by programming bits TEST.LBCK bit (TEST <4>) and CCCR.MON bit (CCCR <5>) to '1'. This mode can be used for a "Hot Selftest", meaning the CAN can be tested without affecting a running CAN system connected to the pins CANx_TX and CANx_RX. In this mode pin CANx_RX is disconnected from the CAN and pin CANx_TX is held recessive. The following figure shows the connection of CANx_TX and CANx_RX to the CAN in case of Internal Loop Back Mode.

Figure 43-4. Pin Control in Loop Back Modes



43.6.3. Timestamp Generation

For timestamp generation the CAN supplies a 16-bit wrap-around counter. A prescaler TSCC.TCP bit (TSCC <19:16>) can be configured to clock the counter in multiples of CAN bit times (1...16). The counter is readable via TSCV.TSC bit (TSCV <15:8>). A write access to register TSCV resets the counter to zero. When the timestamp counter wraps around interrupt flag IR.TSW bit (TSW <16>) is set.

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On start of frame reception / transmission the counter value is captured and stored into the timestamp section of an Rx Buffer / Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element.

43.6.4. Timeout Counter

To signal timeout conditions for Rx FIFO 0, Rx FIFO 1, and the Tx Event FIFO the CAN supplies a 16-bit Timeout Counter. It operates as down-counter and uses the same prescaler controlled by TSCC.TCP bit (TSCC <19:16>) as the Timestamp Counter. The Timeout Counter is configured via register TOCC. The actual counter value can be read from TOCV.TOC bits (TOCV <15:0>). The Timeout Counter can only be started while CCCR.INIT bit (CCCR <0>) = '0'. It is stopped when CCCR.INIT bit (CCCR <0>) = '1', e.g. when the CAN enters "bus off" state.

The operation mode is selected by TOCC.TOS bits (TOCC <2:1>). When operating in Continuous Mode, the counter starts when CCCR.INIT bit (CCCR <0>) is reset. A write to TOCV presets the counter to the value configured by TOCC.TOP bits (TOCC <31:16>) and continues down-counting.

When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP bits (TOCC <31:16>). Down-counting is started when the first FIFO element is stored. Writing to TOCV has no effect.

When the counter reaches zero, interrupt flag IR.TOO bit (IR<18>) is set. In Continuous Mode, the counter is immediately restarted at TOCC.TOP bits (TOCC <31:16>).

Note: The clock signal for the Timeout Counter is derived from the CAN Core's sample point signal. Therefore the point in time where the Timeout Counter is decremented may vary due to the synchronization / re-synchronization mechanism of the CAN Core. If the baud rate switch feature in CAN FD is used, the timeout counter is clocked differently in arbitration and data field.

43.6.5. Rx Handling

The Rx Handler controls the acceptance filtering, the transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs, as well as the Rx FIFO's Put and Get Indices.

43.6.5.1. Acceptance Filtering

The CAN offers the possibility to configure two sets of acceptance filters, one for standard identifiers and one for extended identifiers. These filters can be assigned to an Rx Buffer or to Rx FIFO 0,1. For acceptance filtering each list of filters is executed from element #0 until the first matching element. Acceptance filtering stops at the first matching element. The following filter elements are not evaluated for this message.

The main features are:

- Each filter element can be configured as
  - range filter (from - to)
  - filter for one or two dedicated IDs
  - classic bit mask filter
- Each filter element is configurable for acceptance or rejection filtering
- Each filter element can be enabled / disabled individually
- Filters are checked sequentially, execution stops with the first matching filter element

Related configuration registers are:

- Global Filter Configuration GFC
- Standard ID Filter Configuration SIDFC
- Extended ID Filter Configuration XIDFC
- Extended ID AND Mask XIDAM

Depending on the configuration of the filter element (SFEC/EFEC) a match triggers one of the following actions:

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- Store received frame in FIFO 0 or FIFO 1
- Store received frame in Rx Buffer
- Reject received frame
- Set High Priority Message interrupt flag IR.HPM (IR <8>)
- Set High Priority Message interrupt flag IR.HPM (IR <8>) and store received frame in FIFO 0 or FIFO 1

Acceptance filtering is started after the complete identifier has been received. After acceptance filtering has completed, and if a matching Rx Buffer or Rx FIFO has been found, the Message Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If the CAN protocol controller has detected an error condition (e.g. CRC error), this message is discarded with the following impact on the affected Rx Buffer or Rx FIFO:

Rx Buffer

New Data flag of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data. For error type see PSR.LEC bits (PSR <2:0>) respectively PSR.DLEC bit field (PSR<10:8>).

Rx FIFO

Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data. For error type see PSR.LEC bits (PSR <2:0>) respectively PSR.DLEC bit field (PSR<10:8>). In case the matching Rx FIFO is operated in overwrite mode, the boundary conditions described in *Rx FIFO Overwrite Mode* have to be considered.

Note: Note: When an accepted message is written to one of the two Rx FIFOs, or into an Rx Buffer, the unmodified received identifier is stored independent of the filter(s) used. The result of the acceptance filter process is strongly depending on the sequence of configured filter elements.

Range Filter

The filter matches for all received frames with Message IDs in the range defined by SF1ID/SF2ID for standard frames or EF1ID/EF2ID for extended frames.

There are two possibilities when range filtering is used together with extended frames:

EFT = "00"	The Message ID of received frames is AND'ed with the Extended ID AND Mask (XIDAM) before the range filter is applied
EFT = "11"	The Extended ID AND Mask (XIDAM) is not used for range filtering

Filter for specific IDs

A filter element can be configured to filter for one or two specific Message IDs. To filter for one specific Message ID, the filter element has to be configured with SF1ID = SF2ID resp. EF1ID = EF2ID.

Classic Bit Mask Filter

Classic bit mask filtering is intended to filter groups of Message IDs by masking single bits of a received Message ID. With classic bit mask filtering SF1ID/EF1ID is used as Message ID filter, while SF2ID/EF2ID is used as filter mask.

A zero bit at the filter mask will mask out the corresponding bit position of the configured ID filter, e.g. the value of the received Message ID at that bit position is not relevant for acceptance filtering. Only those bits of the received Message ID where the corresponding mask bits are one are relevant for acceptance filtering.

In case all mask bits are one, a match occurs only when the received Message ID and the Message ID filter are identical. If all mask bits are zero, all Message IDs match.

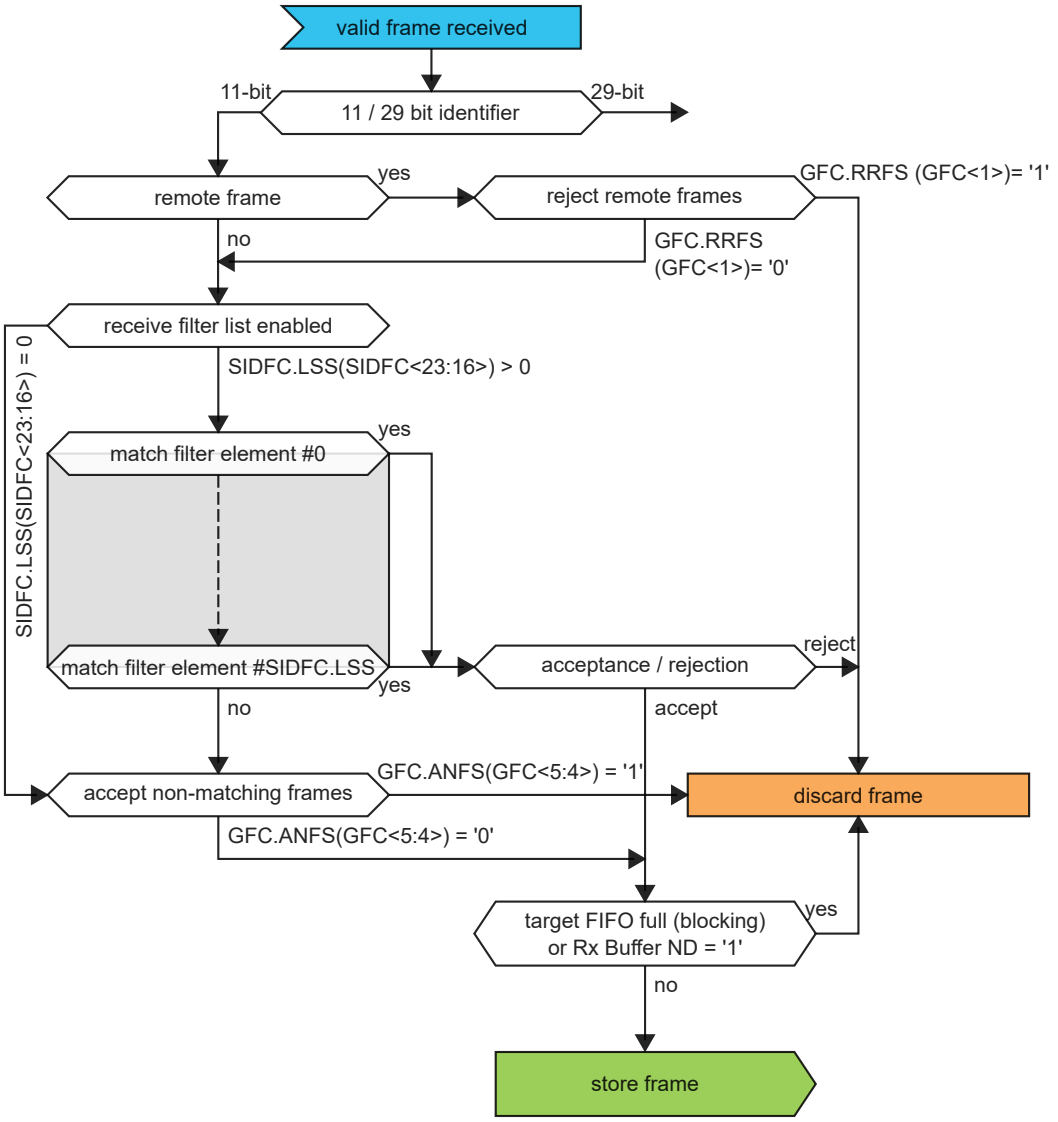
Standard Message ID Filtering

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The figure below shows the flow for standard Message ID (11-bit Identifier) filtering. The Standard Message ID Filter element is described in **[Required-Cleanup]:** .

Controlled by the Global Filter Configuration GFC and the Standard ID Filter Configuration SIDFC Message ID, Remote Transmission Request bit (RTR), and the Identifier Extension bit (IDE) of received frames are compared against the list of configured filter elements.

Figure 43-5. Standard Message ID Filtering



Extended Message ID Filtering

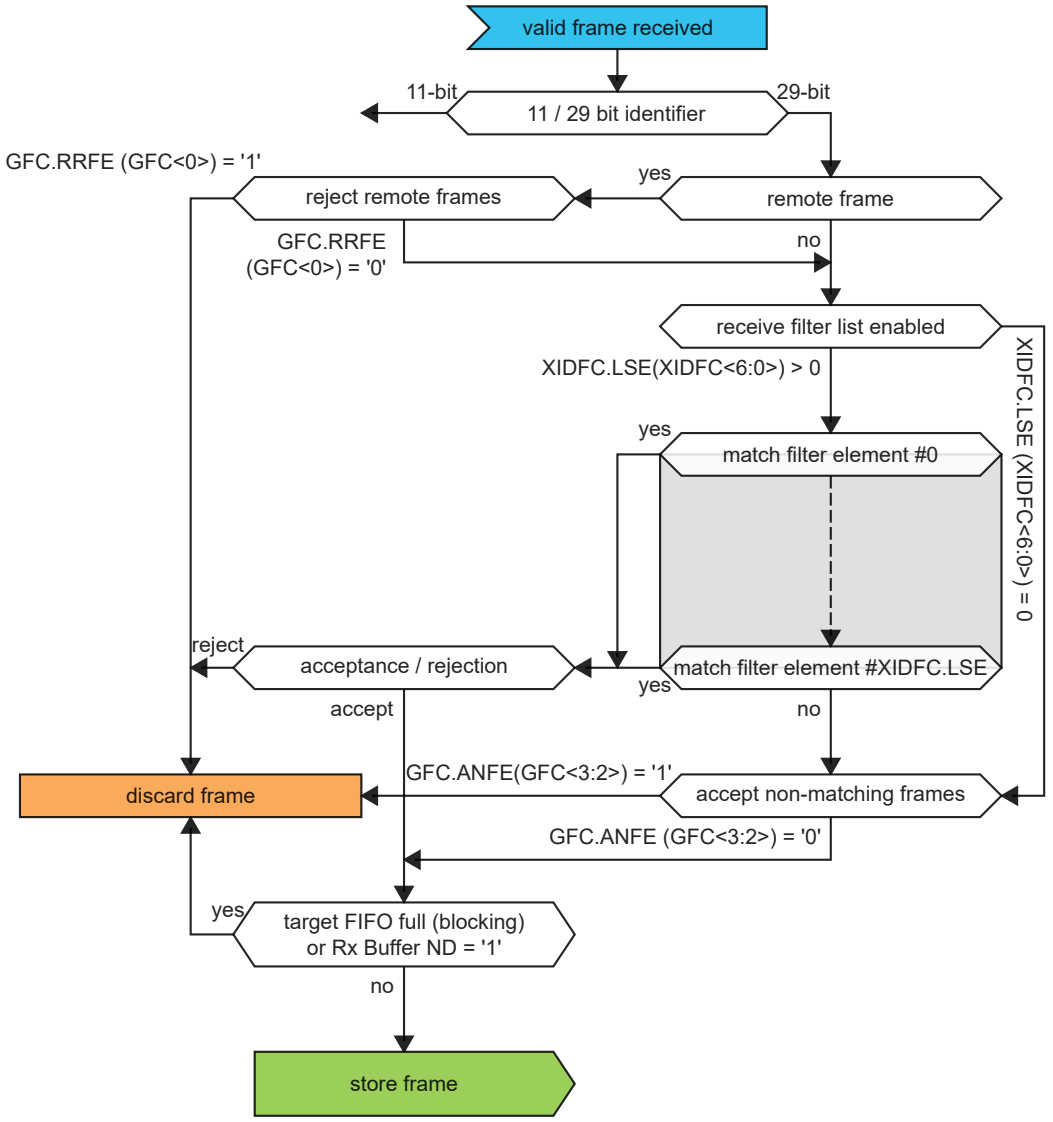
The figure below shows the flow for extended Message ID (29-bit Identifier) filtering. The Extended Message ID Filter element is described in *Extended Message ID Filter Element*.

Controlled by the Global Filter Configuration GFC and the Extended ID Filter Configuration XIDFC Message ID, Remote Transmission Request bit (RTR), and the Identifier Extension bit (IDE) of received frames are compared against the list of configured filter elements.

The Extended ID AND Mask XIDAM is AND'ed with the received identifier before the filter list is executed.

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Figure 43-6. Extended Message ID Filtering



43.6.5.2. Rx FIFOs

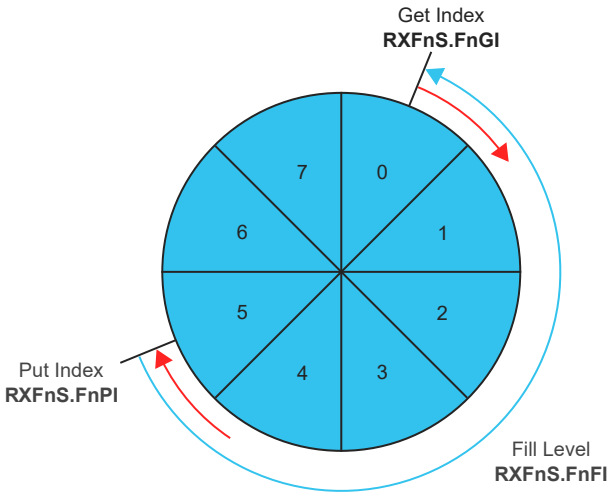
Rx FIFO 0 and Rx FIFO 1 can be configured to hold up to 64 elements each. Configuration of the two Rx FIFOs is done via registers RXF0C and RXF1C.

Received messages that passed acceptance filtering are transferred to the Rx FIFO as configured by the matching filter element. For a description of the filter mechanisms available for Rx FIFO 0 and Rx FIFO 1 see *Acceptance Filtering*. The Rx FIFO element is described in *Rx Buffer and FIFO Element*.

To avoid an Rx FIFO overflow, the Rx FIFO watermark can be used. When the Rx FIFO fill level reaches the Rx FIFO watermark configured by RXFnC.FnWM, interrupt flag IR.RFnW is set. When the Rx FIFO Put Index reaches the Rx FIFO Get Index an Rx FIFO Full condition is signalled by RXFnS.FnF. In addition interrupt flag IR.RFnF is set, where n = 0 for Rx FIFO 0 buffer and n = 1 for Rx FIFO 1 buffer.

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Figure 43-7. Rx FIFO Status (n =0 for Rx FIFO 0 buffer and n=1 for Rx FIFO 1 buffer)



When reading from an Rx FIFO, Rx FIFO Get Index RXFnS.FnGI • FIFO Element Size has to be added to the corresponding Rx FIFO start address RXFnC.FnSA.

Table 43-3. Rx Buffer / FIFO Element Size

RXESC.RBDS[2:0] RXESC.FnDS[2:0]	Data Field [bytes]	FIFO Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

Rx FIFO Blocking Mode

The Rx FIFO blocking mode is configured by RXFnC.FnOM = '0'. This is the default operation mode for the Rx FIFOs.

When an Rx FIFO full condition is reached (RXFnS.FnPI = RXFnS.FnGI), no further messages are written to the corresponding Rx FIFO until at least one message has been read out and the Rx FIFO Get Index has been incremented. An Rx FIFO full condition is signaled by RXFnS.FnF = '1'. In addition interrupt flag IR.RFnF is set.

In case a message is received while the corresponding Rx FIFO is full, this message is discarded and the message lost condition is signalled by RXFnS.RFnL = '1'. In addition interrupt flag IR.RFnL is set.

Rx FIFO Overwrite Mode

The Rx FIFO overwrite mode is configured by RXFnC.FnOM = '1'.

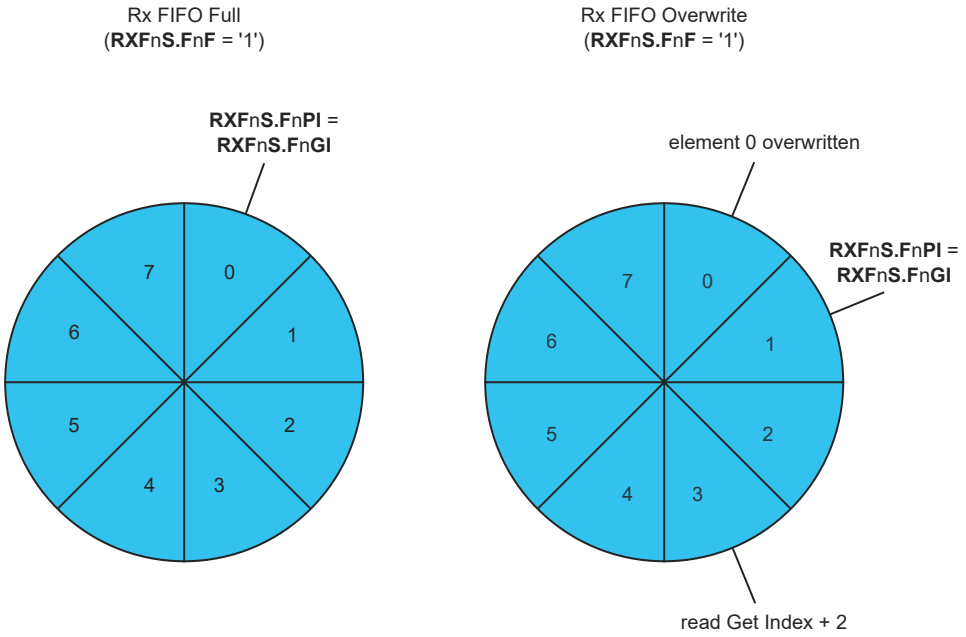
When an Rx FIFO full condition (RXFnS.FnPI = RXFnS.FnGI) is signaled by RXFnS.FnF = '1', the next message accepted for the FIFO will overwrite the oldest FIFO message. Put and get index are both incremented by one.

When an Rx FIFO is operated in overwrite mode and an Rx FIFO full condition is signaled, reading of the Rx FIFO elements should start at least at get index + 1. The reason for that is, that it might

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happen, that a received message is written to the Message RAM (put index) while the CPU is reading from the Message RAM (get index). In this case inconsistent data may be read from the respective Rx FIFO element. Adding an offset to the get index when reading from the Rx FIFO avoids this problem. The offset depends on how fast the CPU accesses the Rx FIFO. The figure below shows an offset of two with respect to the get index when reading the Rx FIFO. In this case the two messages stored in element 1 and 2 are lost.

Figure 43-8. Rx FIFO Overflow Handling (n =0 for Rx FIFO 0 buffer and n=1 for Rx FIFO 1 buffer)



After reading from the Rx FIFO, the number of the last element read has to be written to the Rx FIFO Acknowledge Index RXFnA.FnA. This increments the get index to that element number. In case the put index has not been incremented to this Rx FIFO element, the Rx FIFO full condition is reset (RXFnS.FnF = '0').

43.6.5.3. Dedicated Rx Buffers

The CAN supports up to 64 dedicated Rx Buffers. The start address of the dedicated Rx Buffer section is configured via RXBC.RBSA bits (RXBC <15:0>).

For each Rx Buffer a Standard or Extended Message ID Filter Element with SFEC / EFEC = "111" and SFID2 / EFID2[10:9] = "00" has to be configured (see *Standard Message ID Filter Element* and *Extended Message ID Filter Element*).

After a received message has been accepted by a filter element, the message is stored into the Rx Buffer in the Message RAM referenced by the filter element. The format is the same as for an Rx FIFO element. In addition the flag IR.DRX bit (IR <19>) (Message stored in Dedicated Rx Buffer) in the interrupt register is set.

Table 43-4. Example Filter Configuration for Rx Buffers

Filter Element	SFID1[10:0] / EFID1[28:0]	SFID2[10:9] / EFID2[10:9]	SFID2[5:0] / EFID2[5:0]
0	ID message 1	00	00 0000
1	ID message 2	00	00 0001
2	ID message 3	00	00 0010

After the last word of a matching received message has been written to the Message RAM, the respective New Data flag in register NDAT1, NDAT2 is set. As long as the New Data flag is set, the

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respective Rx Buffer is locked against updates from received matching frames. The New Data flags have to be reset by the CPU by writing a '1' to the respective bit position.

While an Rx Buffer's New Data flag is set, a Message ID Filter Element referencing this specific Rx Buffer will not match, causing the acceptance filtering to continue. Following Message ID Filter Elements may cause the received message to be stored into another Rx Buffer, or into an Rx FIFO, or the message may be rejected, depending on filter configuration.

Rx Buffer Handling

- Reset interrupt flag IR.DRX bit (IR <19>)
- Read New Data registers
- Read messages from Message RAM
- Reset New Data flags of processed messages

43.6.5.4. Debug on CAN Support

Debug messages are stored into Rx Buffers. For debug handling three consecutive Rx buffers (e.g. #61, #62, #63) have to be used for storage of debug messages A, B, and C. The format is the same as for an Rx Buffer or an Rx FIFO element (see *Rx Buffer and FIFO Element*).

Advantage: Fixed start address for the DMA transfers (relative to RXBC.RBSA bits (RXBC <15:0>)), no additional configuration required.

For filtering of debug messages Standard / Extended Filter Elements with SFEC / EFEC = "111" have to be set up. Messages matching these filter elements are stored into the Rx Buffers addressed by SFID2 / EFID2[5:0].

After message C has been stored, the DMA request output is activated and the three messages can be read from the Message RAM under DMA control. The RAM words holding the debug messages will not be changed by the CAN while DMA request is activated. The behavior is similar to that of an Rx Buffers with its New Data flag set.

After the DMA has completed the DMA unit sets the DMA acknowledge. This resets DMA request. Now the CAN is prepared to receive the next set of debug messages.

Filtering for Debug Messages

Filtering for debug messages is done by configuring one Standard / Extended Message ID Filter Element for each of the three debug messages. To enable a filter element to filter for debug messages SFEC / EFEC has to be programmed to "111". In this case fields SFID1 / SFID2 and EFID1 / EFID2 have a different meaning (see *Standard Message ID Filter Element* and *Extended Message ID Filter Element*). While SFID2 / EFID2[10:9] controls the debug message handling state machine, SFID2 / EFID2[5:0] controls the location for storage of a received debug message.

When a debug message is stored, neither the respective New Data flag nor IR.DRX bit (IR <19>) are set. The reception of debug messages can be monitored via RXF1S.DMS bits (RXF1S <31:30>).

Table 43-5. Example Filter Configuration for Debug Messages

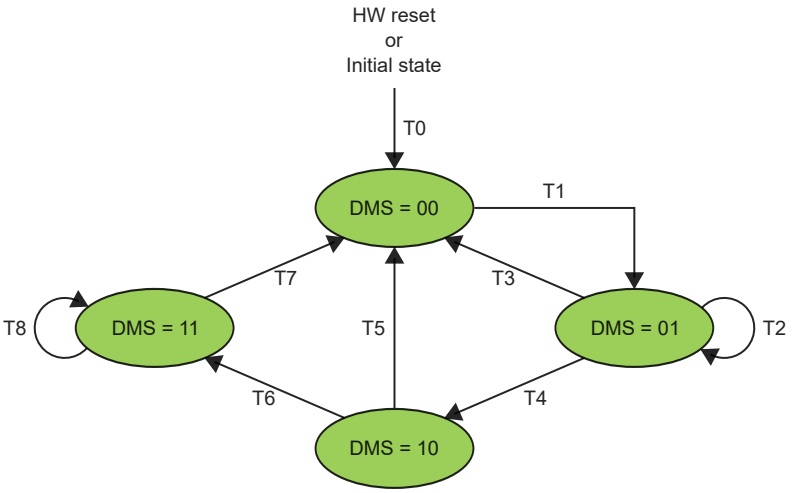
Filter Element	SFID1[10:0] / EFID1[28:0]	SFID2[10:9] / EFID2[10:9]	SFID2[5:0] / EFID2[5:0]
0	ID debug message A	01	11 1101
1	ID debug message B	10	11 1110
2	ID debug message C	11	11 1111

Debug Message Handling

The debug message handling state machine assures that debug messages are stored to three consecutive Rx Buffers in correct order. In case of missing messages the process is restarted. The DMA request is activated only when all three debug messages A, B, C have been received in correct order.

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Figure 43-9. Debug Message Handling State Machine



T0: Reset DMA request output, enable reception of debug message A, B, and C
T1: Reception of debug message A
T2: Reception of debug message A
T3: Reception of debug message C
T4: Reception of debug message B
T5: Reception of debug message A, B
T6: Reception of debug message C
T7: DMA transfer completed
T8: Reception of debug message A, B, C (message rejected)

43.6.6. Tx Handling

The Tx Handler handles transmission requests for the dedicated Tx Buffers, the Tx FIFO, and the Tx Queue. It controls the transfer of transmit messages to the CAN Core, the Put and Get Indices, and the Tx Event FIFO. Up to 32 Tx Buffers can be set up for message transmission. The CAN mode for transmission (Classic CAN or CAN FD) can be configured separately for each Tx Buffer element. The Tx Buffer element is described in *Tx Buffer Element*. The table below describes the possible configurations for frame transmission.

Table 43-6. Possible Configurations for Frame Transmission

CCCR		Tx Buffer Element		Frame Transmission
BRSE	FDOE	FDF	BRS	
ignored	0	ignored	ignored	Classic CAN
0	1	0	ignored	Classic CAN
0	1	1	ignored	FD without bit rate switching
1	1	0	ignored	Classic CAN
1	1	1	0	FD without bit rate switching
1	1	1	1	FD with bit rate switching

Note: AUTOSAR requires at least three Tx Queue Buffers and support of transmit cancellation

The Tx Handler starts a Tx scan to check for the highest priority pending Tx request (Tx Buffer with lowest Message ID) when the Tx Buffer Request Pending register TXBRP is updated, or when a transmission has been started.

43.6.6.1. Transmit Pause

The transmit pause feature is intended for use in CAN systems where the CAN message identifiers are (permanently) specified to specific values and cannot easily be changed. These message identifiers may have a higher CAN arbitration priority than other defined messages, while in a

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specific application their relative arbitration priority should be inverse. This may lead to a case where one ECU sends a burst of CAN messages that cause another ECU's CAN messages to be delayed because that other messages have a lower CAN arbitration priority.

If e.g. CAN ECU-1 has the transmit pause feature enabled and is requested by its application software to transmit four messages, it will, after the first successful message transmission, wait for two CAN bit times of bus idle before it is allowed to start the next requested message. If there are other ECUs with pending messages, those messages are started in the idle time, they would not need to arbitrate with the next message of ECU-1. After having received a message, ECU-1 is allowed to start its next transmission as soon as the received message releases the CAN bus.

The transmit pause feature is controlled by bit CCCR.TXP bit (CCCR<14>). If the bit is set, the CAN will, each time it has successfully transmitted a message, pause for two CAN bit times before starting the next transmission. This enables other CAN nodes in the network to transmit messages even if their messages have lower prior identifiers. Default is transmit pause disabled (CCCR.TXP bit (CCCR<14>) = '0').

This feature looses up burst transmissions coming from a single node and it protects against "babbling idiot" scenarios where the application program erroneously requests too many transmissions.

43.6.6.2. Dedicated Tx Buffers

Dedicated Tx Buffers are intended for message transmission under complete control of the CPU. Each Dedicated Tx Buffer is configured with a specific Message ID. In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first. These Tx buffers shall be requested in ascending order with lowest buffer number first. Alternatively, all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to TXBAR.

If the data section has been updated, a transmission is requested by an Add Request via TXBAR.ARn. The requested messages arbitrate internally with messages from an optional Tx FIFO or Tx Queue and externally with messages on the CAN bus, and are sent out according to their Message ID.

A Dedicated Tx Buffer allocates Element Size 32-bit words in the Message RAM (refer to table below). Therefore the start address of a dedicated Tx Buffer in the Message RAM is calculated by adding transmit buffer index (0...31) • Element Size to the Tx Buffer Start Address TXBC.TBSA bit (TXBC <15:0>).

Table 43-7. Tx Buffer / FIFO / Queue Element Size

TXESC.TBDS[2:0]	Data Field [bytes]	Element Size [RAM words]
000	8	4
001	12	5
010	16	6
011	20	7
100	24	8
101	32	10
110	48	14
111	64	18

43.6.6.3. Tx FIFO

Tx FIFO operation is configured by programming TXBC.TFQM bit (TXBC <30>) to '0'. Messages stored in the Tx FIFO are transmitted starting with the message referenced by the Get Index TXFQS.TFGI bit TXFQS (<12:8>). After each transmission the Get Index is incremented cyclically until the Tx FIFO is empty. The Tx FIFO enables transmission of messages with the same Message ID from different Tx Buffers in the order these messages have been written to the Tx FIFO. The CAN calculates the Tx FIFO Free Level TXFQS.TFFL bits (TXFQS <5:0>) as difference between Get and Put Index. It indicates the number of available (free) Tx FIFO elements.

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New transmit messages have to be written to the Tx FIFO starting with the Tx Buffer referenced by the Put Index TXFQS.TFQPI bits TXFQS (<20:16>). An Add Request increments the Put Index to the next free Tx FIFO element. When the Put Index reaches the Get Index, Tx FIFO Full (TXFQS.TFQF bit (TXFQS <21>) = '1') is signaled. In this case no further messages should be written to the Tx FIFO until the next message has been transmitted and the Get Index has been incremented.

When a single message is added to the Tx FIFO, the transmission is requested by writing a '1' to the TXBAR bit related to the Tx Buffer referenced by the Tx FIFO's Put Index.

When multiple (n) messages are added to the Tx FIFO, they are written to n consecutive Tx Buffers starting with the Put Index. The transmissions are then requested via TXBAR. The Put Index is then cyclically incremented by n. The number of requested Tx buffers should not exceed the number of free Tx Buffers as indicated by the Tx FIFO Free Level.

When a transmission request for the Tx Buffer referenced by the Get Index is canceled, the Get Index is incremented to the next Tx Buffer with pending transmission request and the Tx FIFO Free Level is recalculated. When transmission cancellation is applied to any other Tx Buffer, the Get Index and the FIFO Free Level remain unchanged.

A Tx FIFO element allocates Element Size 32-bit words in the Message RAM (refer to *Tx Buffer / FIFO / Queue Element Size*). Therefore the start address of the next available (free) Tx FIFO Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI bits (TXFQS <20:16>) (0...31).

- Element Size to the Tx Buffer Start Address TXBC.TBSA bits (TXBC <15:0>)

43.6.6.4. Tx Queue

Tx Queue operation is configured by programming TXBC.TFQM bit (TXBC <30>) to '1'. Messages stored in the Tx Queue are transmitted starting with the message with the lowest Message ID (highest priority). In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New messages have to be written to the Tx Buffer referenced by the Put Index TXFQS.TFQPI bits TXFQS (<20:16>). An Add Request cyclically increments the Put Index to the next free Tx Buffer. In case that the Tx Queue is full (TXFQS.TFQF bit (TXFQS <21>) = '1'), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been canceled.

The application may use register TXBRP instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

A Tx Queue Buffer allocates Element Size 32-bit words in the Message RAM (refer to *Tx Buffer / FIFO / Queue Element Size*). Therefore the start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI bits TXFQS (<20:16>) (0...31). Element Size to the Tx Buffer Start Address TXBC.TBSA bits (TXBC <15:0>).

43.6.6.5. Tx Queue

Tx Queue operation is configured by programming TXBC.TFQM bit (TXBC <30>) to '1'. Messages stored in the Tx Queue are transmitted starting with the message with the lowest Message ID (highest priority). In case that multiple Queue Buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the Put index, a prediction of the transmission order is not possible.

New messages have to be written to the Tx Buffer referenced by the Put Index TXFQS.TFQPI bits TXFQS (<20:16>). The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number. In case that the Tx Queue is full (TXFQS.TFQF bit (TXFQS <21>) = '1'), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been canceled.

The application may use register TXBRP instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

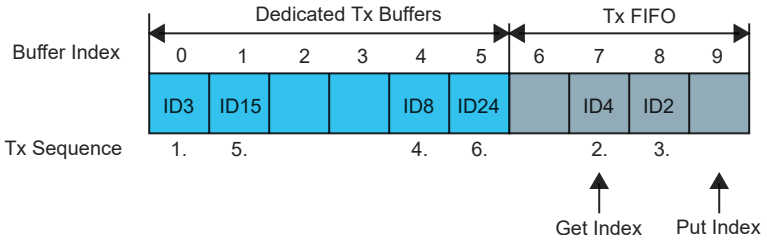
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A Tx Queue Buffer allocates Element Size 32-bit words in the Message RAM (refer to *Tx Buffer / FIFO / Queue Element Size*). Therefore the start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index TXFQS.TFQPI bits TXFQS (<20:16>) (0...31). Element Size to the Tx Buffer Start Address TXBC.TBSA bits (TXBC <15:0>).

43.6.6.6. Mixed Dedicated Tx Buffers / Tx FIFO

In this case the Tx Buffers section in the Message RAM is subdivided into a set of Dedicated Tx Buffers and a Tx FIFO. The number of Dedicated Tx Buffers is configured by TXBC.NDTB bits (TXBC <21:16>). The number of Tx Buffers assigned to the Tx FIFO is configured by TXBC.TFQS bits (TXBC <29:24>). In case TXBC.TFQS bits (TXBC <29:24>) is programmed to zero, only Dedicated Tx Buffers are used.

Figure 43-10. Example of mixed Configuration Dedicated Tx Buffers / Tx FIFO



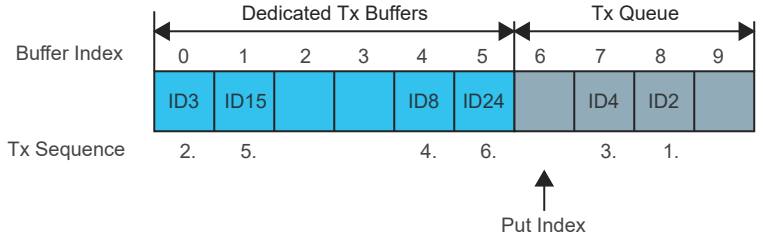
Tx prioritization:

- Scan Dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by TXFQS.TFGI bits (TXFQS <12:8>))
- Buffer with lowest Message ID gets highest priority and is transmitted next
- In case a defined order of transmission is required the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx buffers with same Message ID shall be requested in ascending order with lowest buffer number first or by a single write access to TXBAR. Alternatively a single Tx Buffer can be used to transmit those messages one after the other.

43.6.6.7. Mixed Dedicated Tx Buffers/Tx Queue

In this case the Tx Buffers section in the Message RAM is subdivided into a set of Dedicated Tx Buffers and a Tx Queue. The number of Dedicated Tx Buffers is configured by the TXBC.NDTB bits (TXBC <21:16>). The number of Tx Queue Buffers is configured by the TXBC.TFQS bits (TXBC <29:24>). In case the TXBC.TFQS bits (TXBC <29:24>) is programmed to zero, only Dedicated Tx Buffers are used.

Figure 43-11. Example of mixed Configuration Dedicated Tx Buffers/Tx Queue



Tx prioritization:

- Scan all Tx Buffers with activated transmission request.

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- Tx Buffer with lowest Message ID gets highest priority and is transmitted next.

43.6.6.8. Transmit Cancellation

The CAN supports transmit cancellation. This feature is especially intended for gateway applications and AUTOSAR-based applications. To cancel a requested transmission from a dedicated Tx Buffer or a Tx Queue Buffer the CPU has to write a '1' to the corresponding bit position (eqal to number of Tx Buffer) of the TXBCR register. Transmit cancellation is not intended for the Tx FIFO operation.

Successful cancellation is signaled by setting the corresponding bit of the TXBCF register to '1'.

In case a transmit cancellation is requested while a transmission from a Tx Buffer is already ongoing, the corresponding TXBRP bit remains set as long as the transmission is in progress. If the transmission was successful, the corresponding TXBTO and TXBCF bits are set. If the transmission was not successful, it is not repeated and only the corresponding TXBCF bit is set.

Note: In case a pending transmission is canceled immediately before this transmission could have been started, there follows a short time window where no transmission is started even if another message is also pending in this node. This may enable another node to transmit a message which may have a lower priority than the second message in this node.

43.6.6.9. Tx Event Handling

To support Tx event handling, the CAN has implemented a Tx Event FIFO. After the CAN has transmitted a message on the CAN bus, Message ID and timestamp are stored in a Tx Event FIFO element. To link a Tx event to a Tx Event FIFO element, the Message Marker from the transmitted Tx Buffer is copied into the Tx Event FIFO element.

The Tx Event FIFO can be configured to a maximum of 32 elements. The Tx Event FIFO element is described in *Tx Event FIFO Element*.

When a Tx Event FIFO full condition is signaled by the IR.TEFF bit (IR <14>), no further elements are written to the Tx Event FIFO until at least one element has been read out and the Tx Event FIFO Get Index has been incremented. In case a Tx event occurs while the Tx Event FIFO is full, this event is discarded and the Interrupt Flag IR.TEFL bit (IR <15>) is set.

To avoid a Tx Event FIFO overflow, the Tx Event FIFO watermark can be used. When the Tx Event FIFO fill level reaches the Tx Event FIFO watermark configured by the TXEFC.EFWM bit (TXEFC <29:24>), the Interrupt Flag IR.TEFW bit (IR <13>) is set.

When reading from the Tx Event FIFO, two times the Tx Event FIFO Get Index TXEFS.EFGI bit (TXEFS <12:8>) has to be added to the Tx Event FIFO start address TXEFC.EFSA bit (TXEFC <15:0>).

43.6.7. FIFO Acknowledge Handling

The Get Indexes of Rx FIFO 0, Rx FIFO 1 and the Tx Event FIFO are controlled by writing to the corresponding FIFO Acknowledge Index (refer to the *RXF0A*, *RXF1A* and *TXEFA*). Writing to the FIFO Acknowledge Index will set the FIFO Get Index to the FIFO Acknowledge Index plus one and thereby updates the FIFO Fill Level. There are two use cases:

When only a single element has been read from the FIFO (the one being pointed to by the Get Index), this Get Index value is written to the FIFO Acknowledge Index.

When a sequence of elements has been read from the FIFO, it is sufficient to write the FIFO Acknowledge Index only once at the end of that read sequence (value: Index of the last element read), to update the FIFO's Get Index.

Due to the fact that the CPU has free access to the CAN's Message RAM, special care has to be taken when reading FIFO elements in an arbitrary order (Get Index not considered). This might be useful when reading a high-priority message from one of the two Rx FIFOs. In this case the FIFO's Acknowledge Index should not be written because this would set the Get Index to a wrong position and also alters the FIFO's Fill Level. In this case some of the older FIFO elements would be lost.

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Note: The application has to ensure that a valid value is written to the FIFO Acknowledge Index. The CAN does not check for erroneous values.

43.6.8. Message RAM

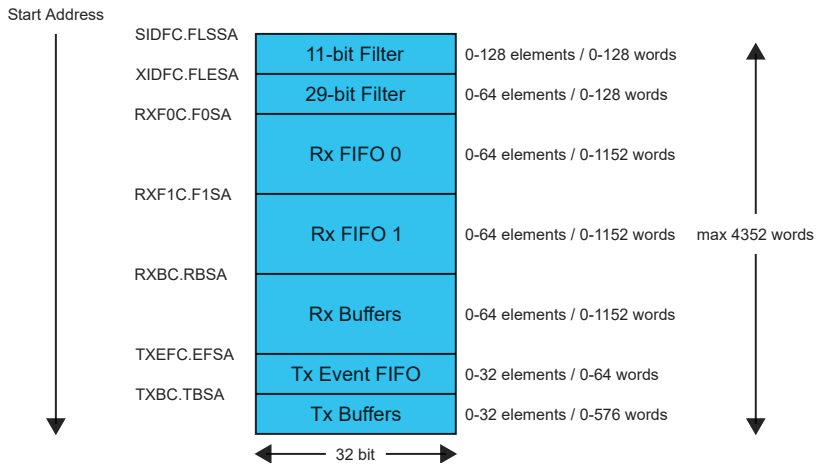
For storage of Rx/Tx messages and for storage of the filter configuration this module uses system RAM and the base address can be set by the CTRLB.OFFSET bits (CTRLB <23:16>).

43.6.8.1. Message RAM Configuration

The Message RAM has a width of 32 bits. The CAN module can be configured to allocate up to 4352 words in the Message RAM. It is not necessary to configure each of the sections listed in the figure below, nor is there any restriction with respect to the sequence of the sections.

When operated in CAN FD mode the required Message RAM size strongly depends on the element size configured for Rx FIFO 0, Rx FIFO 1, Rx Buffers, and Tx Buffers via RXESC.F0DS bits (RXESC <2:0>), RXESC.F1DS bits (RXESC <6:4>), RXESC.RBDS bits (RXESC <10:8>), and TXESC.TBDS bits (TXESC <2:0>).

Figure 43-12. Message RAM Configuration



When the CAN addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses (i.e. only bits 15 to 2 are evaluated and the two LSBs are ignored).

Note: The CAN does not check for erroneous configuration of the Message RAM. Especially the configuration of the start addresses of the different sections and the number of elements of each section has to be done carefully to avoid falsification or loss of data.

43.6.8.2. Rx Buffer and FIFO Element

Up to 64 Rx Buffers and two Rx FIFOs can be configured in the Message RAM. Each Rx FIFO section can be configured to store up to 64 received messages. The structure of a Rx Buffer / FIFO element is shown in the table below. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via register RXESC.

Table 43-8. Rx Buffer and FIFO Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	ESI	XTD	RTR	ID[28:0]																												

Table 43-8. Rx Buffer and FIFO Element (continued)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R1	ANMF	FIDX[6:0]									FDF	BRS	DLC[3:0]				RXTS[15:0]															
R2	DB3[7:0]								DB2[7:0]								DB1[7:0]								DB0[7:0]							
R3	DB7[7:0]								DB6[7:0]								DB5[7:0]								DB4[7:0]							
...	...								...								...								...							
Rn	DBm[7:0]								DBm-1[7:0]								DBm-2[7:0]								DBm-3[7:0]							

R0 Bit 31 - ESI: Error State Indicator

0 : Transmitting node is error active.

1 : Transmitting node is error passive.

R0 Bit 30 - XTD: Extended Identifier

Signals to the Host whether the received frame has a standard or extended identifier.

0 : 11-bit standard identifier.

1 : 29-bit extended identifier.

R0 Bit 29 - RTR: Remote Transmission Request

Signals to the Host whether the received frame is a data frame or a remote frame.

0 : Received frame is a data frame.

1 : Received frame is a remote frame.

Note: There are no remote frames in CAN FD format. In CAN FD frames (FDF = 1'), the dominant RRS (Remote Request Substitution) bit replaces bit RTR (Remote Transmission Request).

R0 Bits 28:0 - ID[28:0]: Identifier

Standard or extended identifier depending on bit XTD. A standard identifier is stored into ID[28:18].

R1 Bit 31 - ANMF: Accepted Non-matching Frame

Acceptance of non-matching frames may be enabled via GFC.ANFS bits (GFC <5:4>) and GFC.ANFE bits (GFC <3:2>).

0 : Received frame matching filter index FIDX.

1 : Received frame did not match any Rx filter element.

R1 Bits 30:24 - FIDX[6:0]: Filter Index

0-127 : Index of matching Rx acceptance filter element (invalid if ANMF = '1').

Note: Range is 0 to SIDFC.LSS bits (SIDFC <23:16>) -1 for standard and 0 to XIDFC.LSE bits (XIDFC <22:16>) -1 for extended.

R1 Bits 23:22 - Reserved

R1 Bit 21 - FDF: FD Format

0 : Standard frame format.

1 : CAN FD frame format (new DLC-coding and CRC).

R1 Bit 20 - BRS: Bit Rate Switching

0 : Frame received without bit rate switching.

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1 : Frame received with bit rate switching.

R1 Bits 19:16 - DLC[3:0]: Data Length Code

0-8 : CAN + CAN FD: received frame has 0-8 data bytes.

9-15 : CAN: received frame has 8 data bytes.

9-15 : CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

R1 Bits 15:0 - RXTS[15:0]: Rx Timestamp

Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP bit (TSCC <19:16>).

R2 Bits 31:24 - DB3[7:0]: Data Byte 3

R2 Bits 23:16 - DB2[7:0]: Data Byte 2

R2 Bits 15:8 - DB1[7:0]: Data Byte 1

R2 Bits 7:0 - DB0[7:0]: Data Byte 0

R3 Bits 31:24 - DB7[7:0]: Data Byte 7

R3 Bits 23:16 - DB6[7:0]: Data Byte 6

R3 Bits 15:8 - DB5[7:0]: Data Byte 5

R3 Bits 7:0 - DB4[7:0]: Data Byte 4

...

Rn Bits 31:24 - DBm[7:0]: Data Byte m

Rn Bits 23:16 - DBm-1[7:0]: Data Byte m-1

Rn Bits 15:8 - DBm-2[7:0]: Data Byte m-2

Rn Bits 7:0 - DBm-3[7:0]: Data Byte m-3

WARNING Depending on the configuration of RXESC, between two and sixteen 32-bit words (Rn = 3 ... 17) are used for storage of a CAN message's data field.

43.6.8.3. Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO / Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO / Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler distinguishes between dedicated Tx Buffers and Tx FIFO / Tx Queue by evaluating the Tx Buffer configuration TXBC.TFQS bits (TXBC <29:24>) and TXBC.NDTB bits (TXBC <21:16>). The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via register TXESC.

Table 43-9. Tx Buffer Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T0	ESI	XTD	RTR	ID[28:0]																												
T1	MM[7:0]								EFC		FDF	BRS	DLC[3:0]																			
T2	DB3[7:0]								DB2[7:0]								DB1[7:0]								DB0[7:0]							
T3	DB7[7:0]								DB6[7:0]								DB5[7:0]								DB4[7:0]							

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Table 43-9. Tx Buffer Element (continued)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
...	...								...								...								...							
Tn	DBm[7:0]								DBm-1[7:0]								DBm-2[7:0]								DBm-3[7:0]							

T0 Bit 31 - ESI: Error State Indicator

0 : ESI bit in CAN FD format depends only on error passive flag.

1 : ESI bit in CAN FD format transmitted recessive.

Note: The ESI bit of the transmit buffer is OR'ed with the error passive flag to decide the value of the ESI bit in the transmitted FD frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the ESI bit recessive, but an error passive node will always transmit the ESI bit recessive.

T0 Bit 30 - XTD: Extended Identifier

0 : 11-bit standard identifier.

1 : 29-bit extended identifier.

T0 Bit 29 - RTR: Remote Transmission Request

0 : Transmit data frame.

1 : Transmit remote frame.

Note: When RTR = '1', the CAN transmits a remote frame according to ISO 11898-1, even if CCCR.FDOE enables the transmission in CAN FD format.

T0 Bits 28:0 - ID[28:0]: Identifier

Standard or extended identifier depending on bit XTD. A standard identifier is stored into ID[28:18].

T1 Bits 31:24 - MM[7:0]: Message Marker

Written by CPU during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status.

T1 Bit 23 - EFC: Event FIFO Control

0 : Don't store Tx events.

1 : Store Tx events.

T1 Bit 22 - Reserved

TR1 Bit 21 - FDF: FD Format

0 : Frame transmitted in Classic CAN format.

1 : Frame transmitted in CAN FD format.

T1 Bit 20 - BRS: Bit Rate Switching

0 : CAN FD frames transmitted without bit rate switching.

1 : CAN FD frames transmitted with bit rate switching.

Note: Bits ESI, FDF, and BRS are only evaluated when CAN FD operation is enabled CCCR.FDOE bit (CCCR <8>) = '1'. Bit BRS is only evaluated when in addition CCCR.BRSE bit (CCCR <9>) = '1'.

T1 Bits 19:16 - DLC[3:0]: Data Length Code

0-8 : CAN + CAN FD: received frame has 0-8 data bytes.

9-15 : CAN: received frame has 8 data bytes.

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9-15 : CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

T1 Bits 15:0 - Reserved

T2 Bits 31:24 - DB3[7:0]: Data Byte 3

T2 Bits 23:16 - DB2[7:0]: Data Byte 2

T2 Bits 15:8 - DB1[7:0]: Data Byte 1

T2 Bits 7:0 - DB0[7:0]: Data Byte 0

T3 Bits 31:24 - DB7[7:0]: Data Byte 7

T3 Bits 23:16 - DB6[7:0]: Data Byte 6

T3 Bits 15:8 - DB5[7:0]: Data Byte 5

T3 Bits 7:0 - DB4[7:0]: Data Byte 4

...

Tn Bits 31:24 - DBm[7:0]: Data Byte m

Tn Bits 23:16 - DBm-1[7:0]: Data Byte m-1

Tn Bits 15:8 - DBm-2[7:0]: Data Byte m-2

Tn Bits 7:0 - DBm-3[7:0]: Data Byte m-3

Note: Depending on the configuration of TXESC, between two and sixteen 32-bit words (Tn = 3 ... 17) are used for storage of a CAN message's data field.

43.6.8.4. Tx Event FIFO Element

Each element stores information about transmitted messages. By reading the Tx Event FIFO the Host CPU gets this information in the order the messages were transmitted. Status information about the Tx Event FIFO can be obtained from register TXEFS.

Table 43-10. Tx Event FIFO Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E0	ESI	XTD	RTR	ID[28:0]																												
E1	MM[7:0]								ET[1:0]		FDF	BRS	DLC[3:0]				TXTS[15:0]															

E0 Bit 31 - ESI: Error State Indicator

0 : Transmitting node is error active.

1 : Transmitting node is error passive.

E0 Bit 30 - XTD: Extended Identifier

0 : 11-bit standard identifier.

1 : 29-bit extended identifier.

E0 Bit 29 - RTR: Remote Transmission Request

0 : Received frame is a data frame.

1 : Received frame is a remote frame.

E0 Bits 28:0 - ID[28:0]: Identifier

Standard or extended identifier depending on bit XTD. A standard identifier is stored into ID[28:18].

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E1 Bits 31:24 - MM[7:0]: Message Marker

Copied from Tx Buffer into Tx Event FIFO element for identification of Tx message status.

E1 Bits 23:22 - ET[1:0]: Event Type

This field defines the event type.

Table 43-11. Event Type

Value	Name	Description
0x0 or 0x3	RES	Reserved
0x1	TXE	Tx event
0x2	TXC	Transmission in spite of cancellation (always set for transmission in DAR mode)

E1 Bit 21 - FDF: FD Format

0 : Standard frame format.

1 : CAN FD frame format (new DLC-coding and CRC).

E1 Bit 20 - BRS: Bit Rate Switching

0 : Frame received without bit rate switching.

1 : Frame received with bit rate switching.

E1 Bits 19:16 - DLC[3:0]: Data Length Code

0-8 : CAN + CAN FD: received frame has 0-8 data bytes.

9-15 : CAN: received frame has 8 data bytes.

9-15 : CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

E1 Bits 15:0 - TXTS[15:0]: Tx Timestamp

Timestamp Counter value captured on start of frame transmission. Resolution depending on configuration of the Timestamp Counter Prescaler TSCC.TCP bit (TSCC <19:16>).

43.6.8.5. Standard Message ID Filter Element

Up to 128 filter elements can be configured for 11-bit standard IDs. When accessing a Standard Message ID Filter element, its address is the Filter List Standard Start Address SIDFC.FLSSA bits (SIDFC <15:0>) plus the index of the filter element (0 ... 127).

Table 43-12. Standard Message ID Filter Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S0	SFT [1:0]		SFEC [2:0]			SFID1[10:0]																SFID2[10:0]										

Bits 31:30 - SFT[1:0]: Standard Filter Type

This field defines the standard filter type.

Table 43-13. Standard Filter Type

Value	Name	Description
0x0	RANGE	Range filter from SFID1 to SFID2 (SFID2 >= SFID1)
0x1	DUAL	Dual ID filter for SFID1 or SFID2
0x2	CLASSIC	Classic filter: SFID1 = filter, SFID2 = mask
0x3	RES	Reserved

Bits 29:27 - SFEC[2:0]: Standard Filter Element Configuration

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All enabled filter elements are used for acceptance filtering of standard frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If SFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM (IR <8>) and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match.

Table 43-14. Standard Filter Element Configuration

Value	Name	Description
0x0	DISABLE	Disable filter element
0x1	STF0M	Store in Rx FIFO 0 if filter matches
0x2	STF1M	Store in Rx FIFO 1 if filter matches
0x3	REJECT	Reject ID if filter matches
0x4	PRIORITY	Set priority if filter matches.
0x5	PRIF0M	Set priority and store in FIFO 0 if filter matches.
0x6	PRIF1M	Set priority and store in FIFO 1 if filter matches.
0x7	STRXBUF	Store into Rx Buffer or as debug message, configuration of SFT[1:0] ignored.

Bits 26:16 - SFID1[10:0]: Standard Filter ID 1

First ID of standard ID filter element.

When filtering for Rx Buffers or for debug messages this field defines the ID of a standard mesage to be stored. The received identifiers must match exactly, no masking mechanism is used.

Bits 15:11 - Reserved

Bits 10:0 - SFID2[10:0]: Standard Filter ID 2

This bit field has a different meaning depending on the configuration of SFEC.

1. SFEC = “001” ... “110”: Second ID of standard ID filter element.
2. SFEC = “111”: Filter for Rx Buffers or for debug messages.

SFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence.
00 = Store message into an Rx Buffer
01 = Debug Message A
10 = Debug Message B
11 = Debug Message C

SFID2[8:6] Reserved for future use

SFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA bits (RXBC <15:0>) for storage of a matching message.

43.6.8.6. Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address XIDFC.FLESA bits (XIDFC <15:0>) plus two times the index of the filter element (0...63).

Table 43-15. Extended Message ID Filter Element

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0	EFEC [2:0]			EFID1[28:0]																												
F1	EFT [1:0]			EFID2[28:0]																												

F0 Bits 31:29 - EFEC[2:0]: Extended Filter Element Configuration

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All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = “100”, “101”, or “110” a match sets interrupt flag IR.HPM (IR <8>) and, if enabled, an interrupt is generated. In this case register HPMS is updated with the status of the priority match.

Table 43-16. Extended Filter Element Configuration

Value	Name	Description
0x0	DISABLE	Disable filter element.
0x1	STF0M	Store in Rx FIFO 0 if filter matches.
0x2	STF1M	Store in Rx FIFO 1 if filter matches.
0x3	REJECT	Reject ID if filter matches.
0x4	PRIORITY	Set priority if filter matches.
0x5	PRIF0M	Set priority and store in FIFO 0 if filter matches.
0x6	PRIF1M	Set priority and store in FIFO 1 if filter matches.
0x7	STRXBUF	Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored.

F0 Bits 28:0 - EFID1[28:0]: Extended Filter ID 1

First ID of extended ID filter element.

When filtering for Rx Buffers or for debug messages this field defines the ID of a extended message to be stored. The received identifiers must match exactly, only XIDAM masking mechanism is used.

F1 Bits 31:30 - EFT[1:0]: Extended Filter Type

This field defines the extended filter type.

Table 43-17. Extended Filter Type

Value	Name	Description
0x0	RANGEM	Range filter from EFID1 to EFID2 (EFID2 >= EFID1).
0x1	DUAL	Dual ID filter for EFID1 or EFID2.
0x2	CLASSIC	Classic filter: EFID1 = filter, EFID2 = mask.
0x3	RANGE	Range filter from EFID1 to EFID2 (EFID2 >= EFID1), XIDAM mask not applied.

F1 Bits 28:0 - EFID2[28:0]: Extended Filter ID 2

This bit field has a different meaning depending on the configuration of EFEC.
1) EFEC = “001” ... “110” Second ID of standard ID filter element.
2) EFEC = “111” Filter for Rx Buffers or for debug messages.

EFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence.

00 = Store message into an Rx Buffer

01 = Debug Message A

10 = Debug Message B

11 = Debug Message C

EFID2[8:6] reserved for future use

EFID2[5:0] defines the offset to the Rx Buffer Start Address RXBC.RBSA bits (RXBC <15:0>) for storage of a matching message.

43.6.9. Interrupts

The CAN has the following interrupt sources:

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- Access to Reserved Address
- Protocol Errors (Data Phase / Arbitration Phase)
- Watchdog Interrupt
- “bus off” Status
- Error Warning & Passive
- Error Logging Overflow
- AHB Bus Error (BERR)
- Message stored to Dedicated Rx Buffer
- Timeout Occurred
- Message RAM Access Failure
- Timestamp Wraparound
- Tx Event FIFO statuses (Element Lost / Full / Watermark Reached / New Entry)
- Tx FIFO Empty
- Transmission Cancellation Finished
- Transmission Completed
- High Priority Message
- Rx FIFO 1 Statuses (Message Lost / Full / Watermark Reached / New Message)
- Rx FIFO 0 Statuses (Message Lost / Full / Watermark Reached / New Message)

Each interrupt source has an interrupt flag associated with it. The interrupt flag register (IR) is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing ‘1’ or disabled by writing ‘0’ to the corresponding bit in the interrupt enable register (IE). Each interrupt flag can be assigned to one of two interrupt service lines.

An interrupt request is generated when an interrupt flag is set, the corresponding interrupt enable is set, and the corresponding service line enable assigned to the interrupt is set. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, the service line is disabled, or the CAN is reset. Refer to the **[Required-Cleanup]:** register for details on how to clear interrupt flags. The interrupt request lines are connected to the Nested Vector Interrupt Controller (NVIC). All interrupt requests from the peripheral are sent to the *Nested vector Interrupt Controller NVIC*. Using the CAN FD interrupt requires the interrupt controller to be configured first. The user must read the IR register to determine which interrupt condition is present.

The CAN has one non-maskable interrupt source:

- AHB Bus Error (BERR)

The BERR bit (ERROR<0>) in the error interrupt flag register (ERROR) is set when the interrupt condition occurs. The bus error (BERR) interrupt flag is assigned to the ERROR interrupt service line.

The error interrupt request is generated when the BERR interrupt flag is set. The interrupt request remains active until the interrupt flag is cleared, or the CAN is reset. The interrupt request is sent to the NVIC.

Note: Interrupts must be globally enabled for interrupt requests to be generated.

43.6.10. Sleep Mode Operation

The CAN module can be configured to operate in any idle sleep mode if both AHB and GCLK clocks are available. In sleep mode system clock(AHB) will be off, hence the CAN interrupts are not generated and will not wake-up the device.

The CAN module has its own low power mode that may be used at any time without disabling this module. This is performed by writing one to the Clock Stop Request bit in the CC Control register

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(CCCR.CSR bit (CCCR <4>) = 1). Once all pending transactions are completed and the idle bus state is detected, the CAN will automatically set the Clock Stop Acknowledge bit (CCCR.CSA bit (CCCR <3>) = 1). The CAN then reverts back to its initial state (CCCR.INIT bit (CCCR <0>) = 1), blocking further transfers.

To exit low power mode, CCCR.CSR bit (CCCR<4>) in CCCR register must be written to 0. Afterwards, the application can restart CAN communication by resetting bit CCCR.INIT bit (CCCR <0>).

After reset, the GCLK_CANx and CLK_CANx_AHB clocks are not requested, except for each APB bus access. However, after the CAN initialization, both GCLK_CANx and CLK_CANx_AHB clocks are requested as long as Clock Stop Request bit in the CC Control register is cleared (CCCR.CSR (CCCR<4>)= 0), and stopped when Clock Stop Request bit in the CC Control register is set (CCCR.CSR (CCCR<4>) = 1) and the Clock Stop Acknowledge bit is set (CCCR.CSA (CCCR<3>)= 1). To limit the wake-up time latency, the CAN clock sources must be enabled in continuous mode (ONDEMAND of respective oscillator must be set zero). For further details, refer to the CRU chapter.

43.6.11. Synchronization

Due to the asynchronicity between the main clock domain (CLK_CANx_AHB) and the peripheral clock domain (GCLK_CANx) some registers are synchronized when written. When a write-synchronized register is written, the read back value will not be updated until the register has completed synchronization.

The following bits and registers are write-synchronized:

One Initialization bit in CC Control register (CCCR.INIT bit (CCCR <0>)).

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43.7. Register Summary

For descriptions and definitions of both register and bitfield properties, refer to the *Register Properties*.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x03	Reserved									
0x04	ENDN	7:0	ETV[7:0]							
		15:8	ETV[15:8]							
		23:16	ETV[23:16]							
		31:24	ETV[31:24]							
0x08	MRCFG	7:0								
		15:8								
		23:16	OFFSET[7:0]							
		31:24								
0x0C	DBTP	7:0		DTSEG2[3:0]			DSJW[3:0]			
		15:8				DTSEG1[4:0]				
		23:16	TDC			DBRP[4:0]				
		31:24								
0x10	TEST	7:0	RX	TX[1:0]		LBCK				
		15:8								
		23:16								
		31:24								
0x14	RWD	7:0	WDC[7:0]							
		15:8	WDV[7:0]							
		23:16								
		31:24								
0x18	CCCR	7:0	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
		15:8		TXP	EFBI	PXHD			BRSE	FDOE
		23:16								
		31:24								
0x1C	NBTP	7:0		NTSEG2[6:0]						
		15:8	NTSEG1[7:0]							
		23:16	NBRP[7:0]							
		31:24	NSJW[6:0]							NBRP[8]
0x20	TSCC	7:0							TSS[1:0]	
		15:8								
		23:16					TCP[3:0]			
		31:24								
0x24	TSCV	7:0	TSC[7:0]							
		15:8	TSC[15:8]							
		23:16								
		31:24								
0x28	TOCC	7:0						TOS[1:0]		ETOC
		15:8								
		23:16	TOP[7:0]							
		31:24	TOP[15:8]							
0x2C	TOCV	7:0	TOC[7:0]							
		15:8	TOC[15:8]							
		23:16								
		31:24								
0x30 ... 0x3F	Reserved									
0x40	ECR	7:0	TEC[7:0]							
		15:8	RP	REC[6:0]						
		23:16	CEL[7:0]							
		31:24								

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x44	PSR	7:0	BO	EW	EP	ACT[1:0]			LEC[2:0]	
		15:8		PXE	RFDF	RBRS	RESI		DLEC[2:0]	
		23:16		TDCV[6:0]						
		31:24								
0x48	TDCR	7:0		TDCF[6:0]						
		15:8		TDCO[6:0]						
		23:16								
		31:24								
0x4C ... 0x4F	Reserved									
0x50	IR	7:0	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
		15:8	TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
		23:16	EP	ELO			DRX	TOO	MRAF	TSW
		31:24			ARA	PED	PEA	WDI	BO	EW
0x54	IE	7:0	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
		15:8	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
		23:16	EPE	ELOE			DRXE	TOOE	MRAFE	TSWE
		31:24			ARAE	PEDE	PEAE	WDIE	BOE	EWE
0x58	ILS	7:0	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
		15:8	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
		23:16	EPL	ELOL			DRXL	TOOL	MRAFL	TSWL
		31:24			ARAL	PEDL	PEAL	WDIL	BOL	EWL
0x5C	ILE	7:0							EINT1	EINT0
		15:8								
		23:16								
		31:24								
0x60 ... 0x7F	Reserved									
0x80	GFC	7:0			ANFS[1:0]		ANFE[1:0]		RRFS	RRFE
		15:8								
		23:16								
		31:24								
0x84	SIDFC	7:0	FLSSA[7:0]							
		15:8	FLSSA[15:8]							
		23:16	LSS[7:0]							
		31:24								
0x88	XIDFC	7:0	FLESA[7:0]							
		15:8	FLESA[15:8]							
		23:16		LSE[6:0]						
		31:24								
0x8C ... 0x8F	Reserved									
0x90	XIDAM	7:0	EIDM[7:0]							
		15:8	EIDM[15:8]							
		23:16	EIDM[23:16]							
		31:24				EIDM[28:24]				
0x94	HPMS	7:0	MSI[1:0]		BIDX[5:0]					
		15:8	FLST	FIDX[6:0]						
		23:16								
		31:24								
0x98	NDAT1	7:0	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
		15:8	ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
		23:16	ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
		31:24	ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x9C	NDAT2	7:0	ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
		15:8	ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
		23:16	ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
		31:24	ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
0xA0	RXF0C	7:0	F0SA[7:0]							
		15:8	F0SA[15:8]							
		23:16		F0S[6:0]						
		31:24	F0OM	F0WM[6:0]						
0xA4	RXF0S	7:0		F0FL[6:0]						
		15:8			F0GI[5:0]					
		23:16			F0PI[5:0]					
		31:24							RF0L	F0F
0xA8	RXF0A	7:0			F0AI[5:0]					
		15:8								
		23:16								
		31:24								
0xAC	RXBC	7:0	RBSA[7:0]							
		15:8	RBSA[15:8]							
		23:16								
		31:24								
0xB0	RXF1C	7:0	F1SA[7:0]							
		15:8	F1SA[15:8]							
		23:16		F1S[6:0]						
		31:24	F1OM	F1WM[6:0]						
0xB4	RXF1S	7:0		F1FL[6:0]						
		15:8			F1GI[5:0]					
		23:16			F1PI[5:0]					
		31:24	DMS[1:0]						RF1L	F1F
0xB8	RXF1A	7:0			F1AI[5:0]					
		15:8								
		23:16								
		31:24								
0xBC	RXESC	7:0		F1DS[2:0]				F0DS[2:0]		
		15:8						RBDS[2:0]		
		23:16								
		31:24								
0xC0	TXBC	7:0	TBSA[7:0]							
		15:8	TBSA[15:8]							
		23:16			NDTB[5:0]					
		31:24		TFQM	TFQS[5:0]					
0xC4	TXFQS	7:0			TFFL[5:0]					
		15:8				TFGI[4:0]				
		23:16			TFQF	TFQPI[4:0]				
		31:24								
0xC8	TXESC	7:0						TBDS[2:0]		
		15:8								
		23:16								
		31:24								
0xCC	TXBRP	7:0	TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
		15:8	TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
		23:16	TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
		31:24	TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
0xD0	TXBAR	7:0	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
		15:8	AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
		23:16	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
		31:24	AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
0xD4	TXBCR	7:0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
		15:8	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
		23:16	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
		31:24	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xD8	TXBTO	7:0	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
		15:8	TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
		23:16	TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
		31:24	TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
0xDC	TXBCF	7:0	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
		15:8	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
		23:16	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
		31:24	CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
0xE0	TXBTIE	7:0	TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
		15:8	TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
		23:16	TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
		31:24	TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
0xE4	TXBCIE	7:0	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
		15:8	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
		23:16	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
		31:24	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
0xE8 ... 0xEF	Reserved									
0xF0	TXEFC	7:0	EFSA[7:0]							
		15:8	EFSA[15:8]							
		23:16			EFS[5:0]					
		31:24			EFWM[5:0]					
0xF4	TXEFS	7:0				EFFL[4:0]				
		15:8				EFGI[4:0]				
		23:16				EFPI[4:0]				
		31:24							TEFL	EFF
0xF8	TXEFA	7:0				EFAI[4:0]				
		15:8								
		23:16								
		31:24								
0xFC ... 0xFF	Reserved									
0x0100	ERROR	7:0								BERR
		15:8								
		23:16								
		31:24								

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43.7.1. Endian

Name: ENDN
Offset: 0x04
Reset: 0x87654321
Property: Read-only

Table 43-18. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ETV[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	0	0	0	1	1	1

Bit	23	22	21	20	19	18	17	16
	ETV[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	1	1	0	0	1	0	1

Bit	15	14	13	12	11	10	9	8
	ETV[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	1	0	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	ETV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	0	1

Bits 31:0 – ETV[31:0] Endianness Test Value
The endianness test value is 0x87654321

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43.7.2. Message RAM Configuration

Name: MRCFG
Offset: 0x08
Reset: 0x00000000
Property: Write-restricted

This register is writable only if CCCR.CCE bit (CCCR <1>) is set.

Table 43-19. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	OFFSET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 23:16 – OFFSET[7:0] Message RAM Base Address Offset
This bitfield value represents the 8 bits offset of the memory base address (bits [23:16]).
The base address is calculated following the formula: Base_Address = 0x20000000+OFFSET << 16.

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43.7.3. Data Bit Timing and Prescaler

Name: DBTP
Offset: 0x0C
Reset: 0x06000A03
Property: Write-restricted

This register is write-restricted and only writable if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

The CAN bit time may be programmed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 GCLK_CANx periods. time quantum (t_q) = (DBRP + 1) mtq. Therefore the length of the bit time is [DTSEG1 + DTSEG2 + 3] tq where DTSEG1 and DTSEG2 are programmed values in the DBTP register.

Note:
With a GCLK_CANx of 8MHz, the reset value 0x00000A33 configures the CAN for a fast bit rate of 500 kBits/s.

The bit rate configured for the CAN FD data phase via the DBTP register must be higher or equal to the bit rate configured for the arbitration phase via the NBTP register.

Table 43-20. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	TDC			DBRP[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				DTSEG1[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
	DTSEG2[3:0]				DSJW[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	0	0	1	1

Bit 23 – TDC Transceiver Delay Compensation

Value	Description
0	Transceiver Delay Compensation disabled.
1	Transceiver Delay Compensation enabled.

Bits 20:16 – DBRP[4:0] Data Baud Rate Prescaler

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Value	Description
0x00 – 0x1F	The value by which the GCLK_CANx is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

Bits 12:8 – DTSEG1[4:0] Fast time segment before sample point

Value	Description
0x00 – 0x1F	Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. DTSEG1 is the sum of PROPAGATION TIME SEGMENT (PROP_SEG) and PHASE BUFFER SEGMENT1 (PHASE_SEG1).

Bits 7:4 – DTSEG2[3:0] Data time segment after sample point

Value	Description
0x0 – 0xF	Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. DTSEG2 is PHASE BUFFER SEGMENT2 (PHASE_SEG2).

Bits 3:0 – DSJW[3:0] Data (Re)Syncronization Jump Width

Value	Description
0x0 – 0xF	Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.

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43.7.4. Test

Name: TEST
Offset: 0x10
Reset: 0x00000000
Property: Write-restricted

Table 43-21. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RX	TX[1:0]		LBCK				
Access	R	R/W	R/W	R/W				
Reset	0	0	0	0				

Bit 7 – RX Receive Pin
This bit reflects the actual value of pin CANx_RX. The read value can be interpret as follows.

Value	Description
0	The CAN bus is dominant (CANx_RX = 0).
1	The CAN bus is recessive (CANx_RX = 1).

Bits 6:5 – TX[1:0] Control of Transmit Pin
This field defines the control of the transmit pin.

Value	Name	Description
0x0	CORE	Reset value, CANx_TX controlled by CAN core, updated at the end of CAN bit time.
0x1	SAMPLE	Sample Point can be monitored at pin CANx_TX.
0x2	DOMINANT	Dominant (‘0’) level at pin CANx_TX.
0x3	RECESSIVE	Recessive (‘1’) level at pin CANx_TX.

Bit 4 – LBCK Loop Back Mode

Value	Description
0	Loop Back Mode is disabled.
1	Loop Back Mode is enabled.

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43.7.5. RAM Watchdog

Name: RWD
Offset: 0x14
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and writable only if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

The RAM Watchdog monitors the READY output of the Message RAM. A Message RAM access via the CAN's AHB Host Interface starts the Message RAM Watchdog Counter with the value configured by WDC bits (RWD <7:0>). The counter is reloaded with WDC bits (RWD <7:0>) when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt IR.WDI bit (IR<26>) is set.

Table 43-22. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	WDV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WDC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – WDV[7:0] Watchdog Value
Actual Message RAM Watchdog Counter Value.

Bits 7:0 – WDC[7:0] Watchdog Configuration
Start value of the Message RAM Watchdog Counter. With the reset value of 0x00 the counter is disabled.

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43.7.6. CC Control

Name: CCCR
Offset: 0x18
Reset: 0x00000001
Property: Write-restricted

Table 43-23. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		TXP	EFBI	PXHD			BRSE	FDOE
Access		R/W	R/W	R/W			R/W	R/W
Reset		0	0	0			0	0

Bit	7	6	5	4	3	2	1	0
	TEST	DAR	MON	CSR	CSA	ASM	CCE	INIT
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bit 14 – TXP Transmit Pause

This bit field is write-restricted and only writable if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Value	Description
0	Transmit pause disabled.
1	Transmit pause enabled. The CAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame.

Bit 13 – EFBI Edge Filtering during Bus Integration

Value	Description
0	Edge filtering is disabled.
1	Two consecutive dominant tq required to detect an edge for hard synchronization.

Bit 12 – PXHD Protocol Exception Handling Disable

Note: When protocol exception handling is disabled, the CAN will transmit an error frame when it detects a protocol exception condition.

Value	Description
0	Protocol exception handling enabled.
1	Protocol exception handling disabled.

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Bit 9 – BRSE Bit Rate Switch Enable

Note: When CAN FD operation is disabled (i.e.,CCCR.FDOE bit (CCCR <8>) = 0), BRSE is not evaluated.

Value	Description
0	Bit rate switching for transmissions disabled.
1	Bit rate switching for transmissions enabled.

Bit 8 – FDOE FD Operation Enable

Value	Description
0	FD operation disabled.
1	FD operation enabled.

Bit 7 – TEST Test Mode Enable

This bit field is write-restricted.
Writing a 0 to this field is always allowed.
Writing a 1 to this field is allowed only if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Value	Description
0	Normal operation. Register TEST holds reset values.
1	Test Mode, write access to register TEST enabled.

Bit 6 – DAR Disable Automatic Retransmission

This bit field is write-restricted and writable only if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Value	Description
0	Automatic retransmission of messages not transmitted successfully enabled.
1	Automatic retransmission disabled.

Bit 5 – MON Bus Monitoring Mode

This bit field is write-restricted.
Writing a 0 to this field is always allowed.
Writing a 1 to this field is allowed only both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Value	Description
0	Bus Monitoring Mode is disabled.
1	Bus Monitoring Mode is enabled.

Bit 4 – CSR Clock Stop Request

Value	Description
0	No clock stop is requested.
1	Clock stop requested. When clock stop is requested, first CCCR.INIT bit (CCCR <0>) and then the CCCR.CSA bit (CCCR <3>) will be set after all pending transfer requests have been completed and the CAN bus reached idle.

Bit 3 – CSA Clock Stop Acknowledge

Value	Description
0	No clock stop acknowledged.
1	CAN may be set in power down by stopping CLK_CANx_AHB and GCLK_CANx.

Bit 2 – ASM Restricted Operation Mode

This bit field is write-restricted.
Writing a 0 to this field is always allowed.

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Writing a 1 to this field is allowed only if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Value	Description
0	Normal CAN operation.
1	Restricted Operation Mode active.

Bit 1 – CCE Configuration Change Enable

This bit field is write-restricted and only writable if bit field CCCR.INIT bit (CCCR <0>) is set.

Value	Description
0	The CPU has no write access to the protected configuration registers.
1	The CPU has write access to the protected configuration registers (while CCCR.INIT bit (CCCR <0>) =1).

Bit 0 – INIT Initialization

Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to the INIT bit can be read back. The programmer has to assure that the previous value written to the INIT bit has been accepted by reading the INIT bit before setting the INIT bit to a new value.

Value	Description
0	Normal Operation.
1	Initialization is started.

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43.7.7. Nominal Bit Timing and Prescaler

Name: NBTP
Offset: 0x1C
Reset: 0x06000A33
Property: Write-restricted

This register is write-restricted and writable only if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

The CAN bit time may be programmed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 GCLK_CANx periods. tq = (NBRP + 1) mtq.

Therefore the length of the bit time is [NTSEG1 + NTSEG2 + 3] tq, where NTSEG1 and NTSEG2 are programmed values in the NBTP register.

Note: With a CAN clock (GCLK_CANx) of 8MHz, the reset value 0x06000A03 configures the CAN for a bit rate of 500 kBits/s.

Table 43-24. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NSJW[6:0]							NBRP[8]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	0

Bit	23	22	21	20	19	18	17	16
	NBRP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NTSEG1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
		NTSEG2[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	1	1

Bits 31:25 – NSJW[6:0] Nominal (Re)Syncronization Jump Width

Value	Description
0x00 – 0x7F	Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used.

Bits 24:16 – NBRP[8:0] Nominal Baud Rate Prescaler

Value	Description
0x000 – 0x1FF	The value by which the GCLK_CANx is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

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Bits 15:8 – NTSEG1[7:0] Nominal Time segment before sample point

Value	Description
0x00 – 0x7F	Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. NTSEG1 is the sum of PROPAGATION TIME SEGMENT (PROP_SEG) and PHASE BUFFER SEGMENT1 (PHASE_SEG1).

Bits 6:0 – NTSEG2[6:0] Time segment after sample point

Value	Description
0x00 – 0x7F	Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. NTSEG2 is PHASE BUFFER SEGMENT2 (PHASE_SEG2).

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43.7.8. Timestamp Counter Configuration

Name: TSCC
Offset: 0x20
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and writable only if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Table 43-25. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					TCP[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							TSS[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 19:16 – TCP[3:0] Timestamp Counter Prescaler

Value	Description
0x0 – 0xF	Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

Bits 1:0 – TSS[1:0] Timestamp Select
This field defines the timestamp counter selection.

Value	Name	Description
0x0 or 0x3	ZERO	Timestamp counter value always 0x0000.
0x1	INC	Timestamp counter value incremented by TCP.
0x2	EXT	External timestamp counter value used.

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43.7.9. Timestamp Counter Value

Name: TSCV
Offset: 0x24
Reset: 0x00000000
Property: Read-only

Notes:

1. A write access to TSCV clears the Timestamp Counter value.
2. A “wrap around” is a change of the Timestamp Counter value from non-zero to zero not caused by the write access to TSCV.

Table 43-26. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TSC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TSC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TSC[15:0] Timestamp Counter
The internal Timestamp Counter value is captured on start of frame (both Rx and Tx). When bitfield TSCC.TSS (TSCC<1:0>) = 0x1, the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of bitfield TSCC.TCP (TSCC<19:16>) . A wrap around sets interrupt flag IR.TSW (IR<16>) .

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43.7.10. Timeout Counter Configuration

Name: TOCC
Offset: 0x28
Reset: 0xFFFF0000
Property: Write-restricted

This register is write-restricted and writable if both CCCR.CCE bit (CCCR <1>) and CCCR.INIT bit (CCCR <0>) are set.

Table 43-27. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	TOP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	TOP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						TOS[1:0]		ETOC
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 31:16 – TOP[15:0] Timeout Period
Start value of the Timeout Counter (down-counter). Configures the Timeout Period.

Bits 2:1 – TOS[1:0] Timeout Select
When operating in Continuous mode, a write to TOCV register presets the counter to the value configured by bit TOCC.TOP (TOCC<31:16>) and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by bit TOCC.TOP (TOCC<31:16>). Down-counting is started when the first FIFO element is stored.

Value	Name	Description
0x0	CONT	Continuous operation.
0x1	TXEF	Timeout controlled by TX Event FIFO.
0x2	RXF0	Timeout controlled by Rx FIFO 0.
0x3	RXF1	Timeout controlled by Rx FIFO 1.

Bit 0 – ETOC Enable Timeout Counter

Value	Description
0	Timeout Counter disabled.

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Value	Description
1	Timeout Counter enabled.

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43.7.11. Timeout Counter Value

Name: TOCV
Offset: 0x2C
Reset: 0x0000FFFF
Property: -

Note: A write access to TOCV reloads the Timeout Counter with the value of bit TOCC.TOP (TOCC<31:16>).

Table 43-28. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TOC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	TOC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – TOC[15:0] Timeout Counter

The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of the TSCC.TCP bit (TSCC<19:16>). When decremented to zero, interrupt flag (IR.TOO bit (IR<18>)) is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS bit (TOCC<2:1>).

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43.7.12. Error Counter

Name: ECR
Offset: 0x40
Reset: 0x00000000
Property: Read-only

Note: When CCCR.ASM bit (CCCR<2>) is set, the CAN protocol controller does not increment TEC and REC when a CAN protocol error is detected, but CEL is still incremented.

Table 43-29. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CEL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RP	REC[6:0]						
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TEC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – CEL[7:0] CAN Error Logging
The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; and the next increment of TEC or REC sets interrupt flag IR.ELO bit (IR<22>).

Bit 15 – RP Receive Error Passive

Bits 14:8 – REC[6:0] Receive Error Counter
Actual state of the Receive Error Counter, values between 0 and 127.

Bits 7:0 – TEC[7:0] Transmit Error Counter
Actual state of the Transmit Error Counter, values between 0 and 255.

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43.7.13. Protocol Status

Name: PSR
Offset: 0x44
Reset: 0x00000707
Property: Read-only

Notes:

1. When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in PSR.DLEC bit field (PSR<10:8>) instead of LEC. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.
2. The 'bus off' recovery sequence (see CAN Specification Rev. 2.0 or ISO 11898-1) cannot be shortened by setting or resetting CCCR.INIT bit (CCCR <0>). If the device goes 'bus off', it will set CCCR.INIT bit (CCCR <0>) of its own accord, stopping all bus activities. Once CCCR.INIT bit (CCCR <0>) has been cleared by the CPU, the device will wait for 129 occurrences of Bus Idle (129 * 11 consecutive recessive bits) before resuming normal operation. At the end of the'bus off' recovery sequence, the Error Management Counters will be reset. During the wait time after the resetting of CCCR.INIT bit (CCCR <0>), each time a sequence of 11 recessive bits is monitored, a Bit0 Error code is written to PSR.LEC bit field (PSR <2:0>). This enables the CPU to readily check the status of CAN bus (whether bus is stuck at dominant level or continuously disturbed). ECR.REC bit-field (ECR<14:8>) is used to count these sequences.

Table 43-30. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		TDCV[6:0]						
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		PXE	RFDF	RBRS	RESI	DLEC[2:0]		
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	BO	EW	EP	ACT[1:0]		LEC[2:0]		
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	1	1

Bits 22:16 – TDCV[6:0] Transmitter Delay Compensation Value

Value	Description
0x00 – 0x7F	Position of the secondary sample point, defined by the sum of the measured delay from CANx_TX to CANx_RX and TDCR.TDCO bit-field (TDCR <14:8>). The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq.

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Bit 14 – PXE Protocol Exception Event

This field is cleared on read access. A recessive “reserved bit” following a recessive FDF bit is the example of Protocol Exception.

Value	Description
0	No protocol exception event occurred since last read access.
1	Protocol exception event occurred.

Bit 13 – RFDF Received a CAN FD Message

This field is cleared on read access.

Value	Description
0	Since this bit was reset by the CPU, no CAN FD message has been received.
1	Message in CAN FD format with FDF flag set has been received. This bit is set independent of acceptance filtering.

Bit 12 – RBRS BRS flag of last received CAN FD Message

This field is cleared on read access.

Value	Description
0	Last received CAN FD message did not have its BRS flag set.
1	Last received CAN FD message had its BRS flag set. This bit is set together with RFDF, independent of acceptance filtering.

Bit 11 – RESI ESI flag of last received CAN FD Message

This field is cleared on read access.

Value	Description
0	Last received CAN FD message did not have its ESI flag set.
1	Last received CAN FD message had its ESI flag set.

Bits 10:8 – DLEC[2:0] Data Last Error Code

Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.

Bit 7 – BO 'bus off' Status

Value	Description
0	The CAN is not 'bus off' state.
1	The CAN is in 'bus off' state.

Bit 6 – EW Error Warning Status

Value	Description
0	Both error counters are below the Error Warning limit of 96.
1	At least one of the error counter has reached the Error Warning limit of 96.

Bit 5 – EP Error Passive

Value	Description
0	The CAN is in the ‘error active’ state. It normally takes part in bus communication and sends an active error flag when an error has been detected.
1	The CAN is in the 'error passive' state.

Bits 4:3 – ACT[1:0] Activity

Monitors the module’s CAN communication state.

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Value	Name	Description
0x0	SYNC	Node is synchronizing on CAN communication.
0x1	IDLE	Node is neither receiver nor transmitter.
0x2	RX	Node is operating as receiver.
0x3	TX	Node is operating as transmitter.

Bits 2:0 – LEC[2:0] Last Error Code

The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error.
This field is set on read access.

Value	Name	Description
0x0	NONE	No Error: No error occurred since LEC has been reset by successful reception or transmission.
0x1	STUFF	Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.
0x2	FORM	Form Error: A fixed format part of a received frame has the wrong format.
0x3	ACK	Ack Error: The message transmitted by the CAN was not acknowledged by another node.
0x4	BIT1	Bit1 Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus was dominant.
0x5	BIT0	Bit0 Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value '0'), but the monitored bus value was recessive. During 'bus off' recovery this status is set each time a sequence of 11 recessive bits have been monitored. This enables the CPU to monitor the proceeding of the 'bus off' recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).
0x6	CRC	CRC Error: The CRC checksum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.
0x7	NC	No Change: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register.

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43.7.14. Transmitter Delay Compensation

Name: TDCR
Offset: 0x48
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-31. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		TDCO[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		TDCF[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 14:8 – TDCO[6:0] Transmitter Delay Compensation Offset

Value	Description
0x00 – 0x7F	Offset value defining the distance between the measured delay from CANx_TX to CANx_RX and the secondary sample point. Valid values are 0 to 127 mtq.

Bits 6:0 – TDCF[6:0] Transmitter Delay Compensation Filter Window Length

Value	Description
0x00 – 0x7F	Defines the minimum value for the SSP position, dominant edges on CANx_RX that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq.

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43.7.15. Interrupt

Name: IR
Offset: 0x50
Reset: 0x00000000
Property: -

Note: Interrupt flags must be cleared and then read back to confirm the clear before exiting the ISR to avoid double interrupts.

The flags are set when one of the listed conditions is detected (edge-sensitive). A flag is cleared by writing a 1 to the corresponding bit field. Writing a 0 has no effect. A hard reset will clear the register.

Table 43-32. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			ARA	PED	PEA	WDI	BO	EW
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EP	ELO			DRX	TOO	MRAF	TSW
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEFL	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RF1L	RF1F	RF1W	RF1N	RF0L	RF0F	RF0W	RF0N
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 29 – ARA Access to Reserved Address

Value	Description
0	No access to reserved address occurred.
1	Access to reserved address occurred.

Bit 28 – PED Protocol Error in Data Phase

Value	Description
0	No protocol error in data phase detected.
1	Protocol error in data phase detected (i.e., PSR.DLEC bits (PSR<10:8>) != 0 and PSR.DLEC bits (PSR<10:8>) != 0).

Bit 27 – PEA Protocol Error in Arbitration Phase

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Value	Description
0	No protocol error in arbitration phase detected.
1	Protocol error in arbitration phase detected (i.e., PSR.LEC bits (PSR<2:0>) != 0 and PSR.LEC bits (PSR<2:0>) != 0).

Bit 26 – WDI Watchdog Interrupt

Value	Description
0	No Message RAM Watchdog event occurred.
1	Message RAM Watchdog event due to missing READY.

Bit 25 – BO 'bus off' Status

Value	Description
0	'bus off' status unchanged.
1	'bus off' status changed.

Bit 24 – EW Error Warning Status

Value	Description
0	Error Warning status unchanged.
1	Error Warning status changed.

Bit 23 – EP Error Passive

Value	Description
0	Error Passive status unchanged.
1	Error Passive status changed.

Bit 22 – ELO Error Logging Overflow

Value	Description
0	CAN Error Logging Counter did not overflow.
1	Overflow of CAN Error Logging Counter occurred.

Bit 19 – DRX Message stored in a Dedicated Rx Buffer

The flag is set whenever a received message has been stored into a dedicated Rx Buffer.

Value	Description
0	No Rx Buffer updated.
1	At least one received message stored into a Rx Buffer.

Bit 18 – TOO Timeout Occurred

Value	Description
0	No timeout.
1	Timeout reached.

Bit 17 – MRAF Message RAM Access Failure

The flag is set, when the Rx Handler:

- has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message.
- was not able to write a message to the Message RAM. In this case message storage is aborted.

In both cases the FIFO put index is not updated. The New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location.

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The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the CAN is switched into Restricted Operation Mode. To leave Restricted Operation Mode, the Host CPU must clear CCCR.ASM bit (CCCR <2>).

Value	Description
0	No Message RAM access failure occurred.
1	Message RAM access failure occurred.

Bit 16 – TSW Timestamp Wraparound

Value	Description
0	No timestamp counter wrap-around.
1	Timestamp counter wrapped around.

Bit 15 – TEFL Tx Event FIFO Element Lost

Value	Description
0	No Tx Event FIFO element lost.
1	Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.

Bit 14 – TEFF Tx Event FIFO Full

Value	Description
0	Tx Event FIFO not full.
1	Tx Event FIFO full.

Bit 13 – TEFW Tx Event FIFO Watermark Reached

Value	Description
0	Tx Event FIFO fill level below watermark.
1	Tx Event FIFO fill level reached watermark.

Bit 12 – TEFN Tx Event FIFO New Entry

Value	Description
0	Tx Event FIFO unchanged.
1	Tx Handler wrote Tx Event FIFO element.

Bit 11 – TFE Tx FIFO Empty

Value	Description
0	Tx FIFO not-empty.
1	Tx FIFO empty.

Bit 10 – TCF Transmission Cancellation Finished

Value	Description
0	Transmission cancellation not finished.
1	Transmission cancellation finished.

Bit 9 – TC Transmission Completed

Value	Description
0	No transmission completed.
1	Transmission completed.

Bit 8 – HPM High Priority Message

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Value	Description
0	No high priority message received.
1	High priority message received.

Bit 7 – RF1L Rx FIFO 1 Message Lost

Value	Description
0	No Rx FIFO 1 message lost.
1	Rx FIFO 1 message lost. also set after write attempt to Rx FIFO 1 of size zero.

Bit 6 – RF1F Rx FIFO 1 Full

Value	Description
0	Rx FIFO 1 not full.
1	Rx FIFO 1 full.

Bit 5 – RF1W Rx FIFO 1 Watermark Reached

Value	Description
0	Rx FIFO 1 fill level below watermark.
1	Rx FIFO 1 fill level reached watermark.

Bit 4 – RF1N Rx FIFO 1 New Message

Value	Description
0	No new message written to Rx FIFO 1.
1	New message written to Rx FIFO 1.

Bit 3 – RF0L Rx FIFO 0 Message Lost

Value	Description
0	No Rx FIFO 0 message lost.
1	Rx FIFO 0 message lost. also set after write attempt to Rx FIFO 0 of size zero.

Bit 2 – RF0F Rx FIFO 0 Full

Value	Description
0	Rx FIFO 0 not full.
1	Rx FIFO 0 full.

Bit 1 – RF0W Rx FIFO 0 Watermark Reached

Value	Description
0	Rx FIFO 0 fill level below watermark.
1	Rx FIFO 0 fill level reached watermark.

Bit 0 – RF0N Rx FIFO 0 New Message

Value	Description
0	No new message written to Rx FIFO 0.
1	New message written to Rx FIFO 0.

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43.7.16. Interrupt Enable

Name: IE
Offset: 0x54
Reset: 0x00000000
Property: -

The settings in the Interrupt Enable register determine which status changes in the Interrupt Register will be signalled on an interrupt line.

Table 43-33. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			ARAE	PEDE	PEAE	WDIE	BOE	EWE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EPE	ELOE			DRXE	TOOE	MRAFE	TSWE
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 29 – ARAE Access to Reserved Address Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 28 – PEDE Protocol Error in Data Phase Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 27 – PEAE Protocol Error in Arbitration Phase Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 26 – WDIE Watchdog Interrupt Enable

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Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 25 – BOE 'bus off' Status Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 24 – EWE Error Warning Status Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 23 – EPE Error Passive Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 22 – ELOE Error Logging Overflow Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 19 – DRXE Message stored to Dedicated Rx Buffer Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 18 – TOOE Timeout Occurred Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 17 – MRAFE Message RAM Access Failure Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 16 – TSWE Timestamp Wraparound Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 15 – TEFLE Tx Event FIFO Event Lost Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 14 – TEFFE Tx Event FIFO Full Interrupt Enable

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Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 13 – TEFWE Tx Event FIFO Watermark Reached Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 12 – TEFNE Tx Event FIFO New Entry Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 11 – TFEE Tx FIFO Empty Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 10 – TCFE Transmission Cancellation Finished Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 9 – TCE Transmission Completed Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 8 – HPME High Priority Message Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 7 – RF1LE Rx FIFO 1 Message Lost Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 6 – RF1FE Rx FIFO 1 Full Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 5 – RF1WE Rx FIFO 1 Watermark Reached Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 4 – RF1NE Rx FIFO 1 New Message Interrupt Enable

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Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 3 – RF0LE Rx FIFO 0 Message Lost Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 2 – RF0FE Rx FIFO 0 Full Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 1 – RF0WE Rx FIFO 0 Watermark Reached Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

Bit 0 – RF0NE Rx FIFO 0 New Message Interrupt Enable

Value	Description
0	Interrupt disabled.
1	Interrupt enabled.

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43.7.17. Interrupt Line Select

Name: ILS
Offset: 0x58
Reset: 0x00000000
Property: -

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from IR to one of the two module interrupt lines.

Table 43-34. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			ARAL	PEDL	PEAL	WDIL	BOL	EWL
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EPL	ELOL			DRXL	TOOL	MRAFL	TSWL
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 29 – ARAL Access to Reserved Address Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 28 – PEDL Protocol Error in Data Phase Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 27 – PEAL Protocol Error in Arbitration Phase Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 26 – WDIL Watchdog Interrupt Line

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Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 25 – BOL 'bus off' Status Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 24 – EWL Error Warning Status Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 23 – EPL Error Passive Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 22 – ELOL Error Logging Overflow Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 19 – DRXL Message stored to Dedicated Rx Buffer Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 18 – TOOL Timeout Occurred Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 17 – MRAFL Message RAM Access Failure Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 16 – TSWL Timestamp Wraparound Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 15 – TEFLL Tx Event FIFO Event Lost Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 14 – TEFFL Tx Event FIFO Full Interrupt Line

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Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 13 – TEFWL Tx Event FIFO Watermark Reached Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 12 – TEFNL Tx Event FIFO New Entry Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 11 – TFEL Tx FIFO Empty Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 10 – TCFL Transmission Cancellation Finished Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 9 – TCL Transmission Completed Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 8 – HPML High Priority Message Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 7 – RF1LL Rx FIFO 1 Message Lost Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 6 – RF1FL Rx FIFO 1 Full Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 5 – RF1WL Rx FIFO 1 Watermark Reached Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 4 – RF1NL Rx FIFO 1 New Message Interrupt Line

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Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 3 – RF0LL Rx FIFO 0 Message Lost Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 2 – RF0FL Rx FIFO 0 Full Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 1 – RF0WL Rx FIFO 0 Watermark Reached Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

Bit 0 – RF0NL Rx FIFO 0 New Message Interrupt Line

Value	Description
0	Interrupt assigned to CAN interrupt line 0.
1	Interrupt assigned to CAN interrupt line 1.

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43.7.18. Interrupt Line Enable

Name: ILE
Offset: 0x5C
Reset: 0x00000000
Property: -

Table 43-35. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							EINT1	EINT0
Access							R/W	R/W
Reset							0	0

Bit 1 – EINT1 Enable Interrupt Line 1

Value	Description
0	CAN interrupt line 1 disabled.
1	CAN interrupt line 1 enabled.

Bit 0 – EINT0 Enable Interrupt Line 0

Value	Description
0	CAN interrupt line 0 disabled.
1	CAN interrupt line 0 enabled.

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43.7.19. Global Filter Configuration

Name: GFC
Offset: 0x80
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-36. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			ANFS[1:0]		ANFE[1:0]		RRFS	RRFE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:4 – ANFS[1:0] Accept Non-matching Frames Standard
Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated.

Value	Name	Description
0x0	RXF0	Accept in Rx FIFO 0.
0x1	RXF1	Accept in Rx FIFO 1.
0x1x	REJECT	Reject

Bits 3:2 – ANFE[1:0] Accept Non-matching Frames Extended
Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated.

Value	Name	Description
0x0	RXF0	Accept in Rx FIFO 0.
0x1	RXF1	Accept in Rx FIFO 1.
0x1x	REJECT	Reject

Bit 1 – RRFS Reject Remote Frames Standard

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Value	Description
0	Filter remote frames with 11-bit standard IDs.
1	Reject all remote frames with 11-bit standard IDs.

Bit 0 – RRFE Reject Remote Frames Extended

Value	Description
0	Filter remote frames with 29-bit extended IDs.
1	Reject all remote frames with 29-bit extended IDS.

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43.7.20. Standard ID Filter Configuration

Name: SIDFC
Offset: 0x84
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-37. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	LSS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FLSSA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLSSA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – LSS[7:0] List Size Standard

Value	Description
0	No standard Message ID filter.
1 – 128	Number of standard Message ID filter elements.
> 128	Values greater than 128 are interpreted as 128.

Bits 15:0 – FLSSA[15:0] Filter List Standard Start Address
Start address of standard Message ID filter list. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.21. Extended ID Filter Configuration

Name: XIDFC
Offset: 0x88
Reset: 0x00000000
Property: Write-restricted

Table 43-38. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		LSE[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FLESA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FLESA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:16 – LSE[6:0] List Size Extended

Value	Description
0	No extended Message ID filter.
1 – 64	Number of Extended Message ID filter elements.
> 64	Values greater than 64 are interpreted as 64.

Bits 15:0 – FLESA[15:0] Filter List Extended Start Address
Start address of extended Message ID filter list. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.22. Extended ID AND Mask

Name: XIDAM
Offset: 0x90
Reset: 0x1FFFFFFF
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-39. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
				EIDM[28:24]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	EIDM[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	EIDM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	EIDM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 28:0 – EIDM[28:0] Extended ID Mask
For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active.

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43.7.23. High Priority Message Status

Name: HPMS
Offset: 0x94
Reset: 0x00000000
Property: Read-only

This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Table 43-40. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FLST	FIDX[6:0]						
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MSI[1:0]		BIDX[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – FLST Filter List
Indicates the filter list of the matching filter element.

Value	Description
0	Standard Filter List.
1	Extended Filter List.

Bits 14:8 – FIDX[6:0] Filter Index
Index of matching filter element. Range is 0 to SIDFC.LSS bits (SIDFC <23:16>) bits (XIDFC <22:16>) - 1 (standard) or XIDFC.LSE bits (XIDFC <22:16>)- 1 (extended).

Bits 7:6 – MSI[1:0] Message Storage Indicator
This field defines the message storage information to a FIFO.

Value	Name	Description
0x0	NONE	No FIFO selected.
0x1	LOST	FIFO message lost.
0x2	FIFO0	Message stored in FIFO 0.

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Value	Name	Description
0x3	FIFO1	Message stored in FIFO 1.

Bits 5:0 – BIDX[5:0] Buffer Index
Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = 1.

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43.7.24. New Data 1

Name: NDAT1
Offset: 0x98
Reset: 0x00000000
Property: -

Table 43-41. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ND31	ND30	ND29	ND28	ND27	ND26	ND25	ND24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ND23	ND22	ND21	ND20	ND19	ND18	ND17	ND16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ND15	ND14	ND13	ND12	ND11	ND10	ND9	ND8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ND7	ND6	ND5	ND4	ND3	ND2	ND1	ND0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – NDn New Data n [n = 0..31]
The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register.

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43.7.25. New Data 2

Name: NDAT2
Offset: 0x9C
Reset: 0x00000000
Property: -

Table 43-42. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – NDn New Data [n = 32..63]
The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing 1 to the corresponding bit position. Writing a 0 has no effect. A hard reset will clear the register.

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43.7.26. Rx FIFO 0 Configuration

Name: RXF0C
Offset: 0xA0
Reset: 0x00000000
Property: Write-restricted

Table 43-43. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	F0OM	F0WM[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		F0S[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	F0SA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	F0SA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – F0OM FIFO 0 Operation Mode
FIFO 0 can be operated in blocking or in overwrite mode.

Value	Description
0	FIFO 0 blocking mode.
1	FIFO 0 overwrite mode.

Bits 30:24 – F0WM[6:0] Rx FIFO 0 Watermark

Value	Description
0	Watermark interrupt disabled.
1 – 64	Level for Rx FIFO 0 watermark interrupt (IR.RF0W bit (IR <1>)).
>64	Watermark interrupt disabled.

Bits 22:16 – F0S[6:0] Rx FIFO 0 Size
The Rx FIFO 0 elements are indexed from 0 to F0S - 1.

Value	Description
0	No Rx FIFO 0
1 – 64	Number of Rx FIFO 0 elements.
>64	Values greater than 64 are interpreted as 64.

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Bits 15:0 – F0SA[15:0] Rx FIFO 0 Start Address

Start address of Rx FIFO 0 in Message RAM. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.27. Rx FIFO 0 Status

Name: RXF0S
Offset: 0xA4
Reset: 0x00000000
Property: Read-only

Table 43-44. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
							RF0L	F0F
Access							R	R
Reset							0	0

Bit	23	22	21	20	19	18	17	16
			F0PI[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			F0GI[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		F0FL[6:0]						
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit 25 – RF0L Rx FIFO 0 Message Lost
This bit is a copy of interrupt flag IR.RF0L bit (IR <3>). When IR.RF0L bit (IR <3>) is reset, this bit is also reset.
Overwriting the oldest message when RXF0C.F0OM bit (RXF0C <31>) = '1' will not set this flag.

Value	Description
0	No Rx FIFO 0 message lost.
1	Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero.

Bit 24 – F0F Rx FIFO 0 Full

Value	Description
0	Rx FIFO 0 not full.
1	Rx FIFO 0 full.

Bits 21:16 – F0PI[5:0] Rx FIFO 0 Put Index
Rx FIFO 0 write index pointer, range 0 to 63.

Bits 13:8 – F0GI[5:0] Rx FIFO 0 Get Index
Rx FIFO 0 read index pointer, range 0 to 63.

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Bits 6:0 – F0FL[6:0] Rx FIFO 0 Fill Level
Number of elements stored in Rx FIFO 0, range 0 to 64.

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43.7.28. Rx FIFO 0 Acknowledge

Name: RXF0A
Offset: 0xA8
Reset: 0x00000000
Property: -

Table 43-45. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			F0AI[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – F0AI[5:0] Rx FIFO 0 Acknowledge Index
After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI bits (RXF0S <13:8>) to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL bit (RXF0S <25>).

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43.7.29. Rx Buffer Configuration

Name: RXBC
Offset: 0xAC
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-46. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RBSA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RBSA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RBSA[15:0] Rx Buffer Start Address
Configures the start address of the Rx Buffers section in the Message RAM. Also used to reference debug message A,B,C. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.30. Rx FIFO 1 Configuration

Name: RXF1C
Offset: 0xB0
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-47. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	F1OM	F1WM[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		F1S[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	F1SA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	F1SA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – F1OM FIFO 1 Operation Mode
FIFO 1 can be operated in blocking or in overwrite mode.

Value	Description
0	FIFO 1 blocking mode.
1	FIFO 1 overwrite mode.

Bits 30:24 – F1WM[6:0] Rx FIFO 1 Watermark

Value	Description
0	Watermark interrupt disabled.
1 – 64	Level for Rx FIFO 1 watermark interrupt (IR.RF1W bit (IR <5>)).
>64	Watermark interrupt disabled.

Bits 22:16 – F1S[6:0] Rx FIFO 1 Size
The Rx FIFO 1 elements are indexed from 0 to F1S - 1.

Value	Description
0	No Rx FIFO 1

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Value	Description
1 – 64	Number of Rx FIFO 1 elements.
>64	Values greater than 64 are interpreted as 64.

Bits 15:0 – F1SA[15:0] Rx FIFO 1 Start Address

Start address of Rx FIFO 1 in Message RAM. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.31. Rx FIFO 1 Status

Name: RXF1S
Offset: 0xB4
Reset: 0x00000000
Property: Read-only

Table 43-48. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	DMS[1:0]						RF1L	F1F
Access	R	R					R	R
Reset	0	0					0	0

Bit	23	22	21	20	19	18	17	16
			F1PI[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			F1GI[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		F1FL[6:0]						
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bits 31:30 – DMS[1:0] Debug Message Status
This field defines the debug message status.

Value	Name	Description
0x0	IDLE	Idle state, wait for reception of debug messages, DMA request is cleared.
0x1	DBGA	Debug message A received.
0x2	DBGB	Debug message A, B received.
0x3	DBGC	Debug message A, B, C received, DMA request is set.

Bit 25 – RF1L Rx FIFO 1 Message Lost
This bit is a copy of interrupt flag IR.RF1L bit (IR <7>). When IR.RF1L bit (IR <7>) is reset, this bit is also reset.
Overwriting the oldest message when RXF1C.F1OM bit (RXF1C <31>) = '1' will not set this flag.

Value	Description
0	No Rx FIFO 1 message lost.
1	Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero.

Bit 24 – F1F Rx FIFO 1 Full

Value	Description
0	Rx FIFO 1 not full.

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Value	Description
1	Rx FIFO 1 full.

Bits 21:16 – F1PI[5:0] Rx FIFO 1 Put Index
Rx FIFO 1 write index pointer, range 0 to 63.

Bits 13:8 – F1GI[5:0] Rx FIFO 1 Get Index
Rx FIFO 1 read index pointer, range 0 to 63.

Bits 6:0 – F1FL[6:0] Rx FIFO 1 Fill Level
Number of elements stored in Rx FIFO 1, range 0 to 64.

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43.7.32. Rx FIFO 1 Acknowledge

Name: RXF1A
Offset: 0xB8
Reset: 0x00000000
Property: -

Table 43-49. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			F1AI[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – F1AI[5:0] Rx FIFO 1 Acknowledge Index
After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI bits (RXF1S <13:8>) to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL bits (RXF1S <6:0>).

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43.7.33. Rx Buffer / FIFO Element Size Configuration

Name: RXESC
Offset: 0xBC
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Configures the number of data bytes belonging to an Rx Buffer / Rx FIFO element. Data field sizes >8 bytes are intended for CAN FD operation only.

Table 43-50. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						RBDS[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
		F1DS[2:0]				F0DS[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 10:8 – RBDS[2:0] Rx Buffer Data Field Size
In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer, only the number of bytes as configured by RXESC are stored to the Rx Buffer element. The rest of the frame's data field is ignored.

Value	Name	Description
0x0	DATA8	8 byte data field.
0x1	DATA12	12 byte data field.
0x2	DATA16	16 byte data field.
0x3	DATA20	20 byte data field.
0x4	DATA24	24 byte data field.
0x5	DATA32	32 byte data field.
0x6	DATA48	48 byte data field.
0x7	DATA64	64 byte data field.

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Bits 6:4 – F1DS[2:0] Rx FIFO 1 Data Field Size

In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx FIFO 1, only the number of bytes as configured by RXESC are stored to the Rx FIFO 1 element. The rest of the frame's data field is ignored.

Value	Name	Description
0x0	DATA8	8 byte data field.
0x1	DATA12	12 byte data field.
0x2	DATA16	16 byte data field.
0x3	DATA20	20 byte data field.
0x4	DATA24	24 byte data field.
0x5	DATA32	32 byte data field.
0x6	DATA48	48 byte data field.
0x7	DATA64	64 byte data field.

Bits 2:0 – F0DS[2:0] Rx FIFO 0 Data Field Size

In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx FIFO 0, only the number of bytes as configured by RXESC are stored to the Rx FIFO 0 element. The rest of the frame's data field is ignored.

Value	Name	Description
0x0	DATA8	8 byte data field.
0x1	DATA12	12 byte data field.
0x2	DATA16	16 byte data field.
0x3	DATA20	20 byte data field.
0x4	DATA24	24 byte data field.
0x5	DATA32	32 byte data field.
0x6	DATA48	48 byte data field.
0x7	DATA64	64 byte data field.

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43.7.34. Tx Buffer Configuration

Name: TXBC
Offset: 0xC0
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Note: Be aware that the sum of TFQS and NDTB may not be greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

Table 43-51. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
		TFQM	TFQS[5:0]					
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			NDTB[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TBSA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TBSA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 30 – TFQM Tx FIFO/Queue Mode

Value	Description
0	Tx FIFO operation.
1	Tx Queue operation.

Bits 29:24 – TFQS[5:0] Transmit FIFO/Queue Size

Value	Description
0	No Tx FIFO/Queue.
1 - 32	Number of Tx Buffers used for Tx FIFO/Queue.
>32	Values greater than 32 are interpreted as 32.

Bits 21:16 – NDTB[5:0] Number of Dedicated Transmit Buffers

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Value	Description
0	No Tx FIFO/Queue.
1 – 32	Number of Tx Buffers used for Tx FIFO/Queue.
>32	Values greater than 32 are interpreted as 32.

Bits 15:0 – TBSA[15:0] Tx Buffers Start Address

Start address of Tx Buffers section in Message RAM. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.35. Tx FIFO/Queue Status

Name: TXFQS
Offset: 0xC4
Reset: 0x00000000
Property: Read-only

Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indexes indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. Example: For a configuration of 12 dedicated Tx Buffers and a Tx FIFO of 20 Buffers a Put Index of 15 points to the fourth buffer of the Tx FIFO.

Table 43-52. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TFQF	TFQPI[4:0]				
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				TFGI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TFFL[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 21 – TFQF Tx FIFO/Queue Full

Value	Description
0	Tx FIFO/Queue not full.
1	Tx FIFO/Queue full.

Bits 20:16 – TFQPI[4:0] Tx FIFO/Queue Put Index
Tx FIFO/Queue write index pointer, range 0 to 31.

Bits 12:8 – TFGI[4:0] Tx FIFO/Queue Get Index
Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured (TXBC.TFQM bit (TXBC <30>) = '1').

Bits 5:0 – TFFL[5:0] Tx FIFO Free Level
Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM bit (TXBC <30>) = '1').

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43.7.36. Tx Buffer Element Size Configuration

Name: TXESC
Offset: 0xC8
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes >8 bytes are intended for CAN FD operation only.

Table 43-53. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						TBDS[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – TBDS[2:0] Tx Buffer Data Field Size
In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size TXESC.TBDS (TXESC <2:0>), the bytes not defined by the Tx Buffer are transmitted as “0xCC” (padding bytes).

Value	Name	Description
0x0	DATA8	8 byte data field.
0x1	DATA12	12 byte data field.
0x2	DATA16	16 byte data field.
0x3	DATA20	20 byte data field.
0x4	DATA24	24 byte data field.
0x5	DATA32	32 byte data field.
0x6	DATA48	48 byte data field.
0x7	DATA64	64 byte data field.

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43.7.37. Tx Buffer Request Pending

Name: TXBRP
Offset: 0xCC
Reset: 0x00000000
Property: Read-only

Note: TXBRP bits which are set while a Tx scan is in progress are not considered during this particular Tx scan. In case a cancellation is requested for such a Tx Buffer, this Add Request is canceled immediately, the corresponding TXBRP bit is reset.

Table 43-54. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	TRP31	TRP30	TRP29	TRP28	TRP27	TRP26	TRP25	TRP24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TRP23	TRP22	TRP21	TRP20	TRP19	TRP18	TRP17	TRP16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TRP15	TRP14	TRP13	TRP12	TRP11	TRP10	TRP9	TRP8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TRP7	TRP6	TRP5	TRP4	TRP3	TRP2	TRP1	TRP0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – TRPn Transmission Request Pending

Each Tx Buffer has its own Transmission Request Pending bit.
The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR.
TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).
A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset.
After a cancellation has been requested, a finished cancellation is signaled via TXBCF

- after successful transmission together with the corresponding TXBTO bit
- when the transmission has not yet been started at the point of cancellation
- when the transmission has been aborted due to lost arbitration

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- when an error occurred during frame transmission

In DAR mode all transmissions are automatically canceled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions.

Value	Description
0	No transmission request pending.
1	Transmission request pending.

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43.7.38. Tx Buffer Add Request

Name: TXBAR
Offset: 0xD0
Reset: 0x00000000
Property: -

Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding TXBRP bit is already set), this add request is ignored.

Table 43-55. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – ARn Add Request

Each Tx Buffer has its own Add Request bit.
Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed.

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43.7.39. Tx Buffer Cancellation Request

Name: TXBCR
Offset: 0xD4
Reset: 0x00000000
Property: -

Table 43-56. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	CR31	CR30	CR29	CR28	CR27	CR26	CR25	CR24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CR23	CR22	CR21	CR20	CR19	CR18	CR17	CR16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – CRn Cancellation Request

Each Tx Buffer has its own Cancellation Request bit.
Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset.

Value	Description
0	No cancellation pending.
1	Cancellation pending.

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43.7.40. Tx Buffer Transmission Occurred

Name: TXBTO
Offset: 0xD8
Reset: 0x00000000
Property: Read-only

Table 43-57. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – TOn Transmission Occurred

Each Tx Buffer has its own Transmission Occurred bit.
The bits are set when the corresponding TXBRP bit is cleared after a successful transmission.
The bits are reset when a new transmission is requested by writing '1' to the corresponding bit of register TXBAR.

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43.7.41. Tx Buffer Cancellation Finished

Name: TXBCF
Offset: 0xDC
Reset: 0x00000000
Property: Read-only

Table 43-58. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	CF31	CF30	CF29	CF28	CF27	CF26	CF25	CF24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CF23	CF22	CF21	CF20	CF19	CF18	CF17	CF16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CF15	CF14	CF13	CF12	CF11	CF10	CF9	CF8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CF7	CF6	CF5	CF4	CF3	CF2	CF1	CF0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – CFn Cancellation Finished

Each Tx Buffer has its own Cancellation Finished bit.
The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately.
The bits are reset when a new transmission is requested by writing '1' to the corresponding bit of register TXBAR.

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43.7.42. Tx Buffer Transmission Interrupt Enable

Name: TXBTIE
Offset: 0xE0
Reset: 0x00000000
Property: -

Table 43-59. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – TIEn Transmission Interrupt Enable

Each Tx Buffer has its own Transmission Interrupt Enable bit.

Value	Description
0	Transmission interrupt disabled.
1	Transmission interrupt enabled.

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43.7.43. Tx Buffer Cancellation Finished Interrupt Enable

Name: TXBCIE
Offset: 0xE4
Reset: 0x00000000
Property: -

Table 43-60. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – CFIEn Cancellation Finished Interrupt Enable

Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit.

Value	Description
0	Cancellation finished interrupt disabled.
1	Cancellation finished interrupt enabled.

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43.7.44. Tx Event FIFO Configuration

Name: TXEFC
Offset: 0xF0
Reset: 0x00000000
Property: Write-restricted

This register is write-restricted and only writable if bit fields CCCR.CCE bit (CCCR <1>) = 1 and CCCR.INIT bit (CCCR <0>) = 1.

Table 43-61. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			EFWM[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			EFS[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	EFSA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EFSA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 29:24 – EFWM[5:0] Event FIFO Watermark

Value	Description
0	Watermark interrupt disabled.
1 – 32	Level for Tx Event FIFO watermark interrupt (IR.TEFW bit (IR <13>)).
>32	Watermark interrupt disabled.

Bits 21:16 – EFS[5:0] Event FIFO Size
The Tx Event FIFO elements are indexed from 0 to EFS - 1.

Value	Description
0	Tx Event FIFO disabled
1 – 32	Number of Tx Event FIFO elements.
>32	Values greater than 32 are interpreted as 32.

Bits 15:0 – EFSA[15:0] Event FIFO Start Address
Start address of Tx Event FIFO in Message RAM. When the CAN module addresses the Message RAM it addresses 32-bit words, not single bytes. The configurable start addresses are 32-bit word

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addresses, i.e. only bits 15 to 2 are evaluated, the two least significant bits are ignored. Bits 1 to 0 will always be read back as “00”.

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43.7.45. Tx Event FIFO Status

Name: TXEFS
Offset: 0xF4
Reset: 0x00000000
Property: Read-only

Table 43-62. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
							TEFL	EFF
Access							R	R
Reset							0	0

Bit	23	22	21	20	19	18	17	16
				EFPI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				EFGI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				EFFL[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit 25 – TEFL Tx Event FIFO Element Lost
This bit is a copy of interrupt flag IR.TEFL bit (IR <15>). When IR.TEFL bit (IR <15>) is reset, this bit is also reset.

Value	Description
0	No Tx Event FIFO element lost.
1	Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.

Bit 24 – EFF Event FIFO Full

Value	Description
0	Tx Event FIFO not full.
1	Tx Event FIFO full.

Bits 20:16 – EFPI[4:0] Event FIFO Put Index
Tx Event FIFO write index pointer, range 0 to 31.

Bits 12:8 – EFGI[4:0] Event FIFO Get Index
Tx Event FIFO read index pointer, range 0 to 31.

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Bits 4:0 – EFFL[4:0] Event FIFO Fill Level
Number of elements stored in Tx Event FIFO, range 0 to 32.

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43.7.46. Tx Event FIFO Acknowledge

Name: TXEFA
Offset: 0xF8
Reset: 0x00000000
Property: -

Table 43-63. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EFAI[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – EFAI[4:0] Event FIFO Acknowledge Index
After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI bits (TXEFS <12:8>) to EFAI + 1 and update the FIFO 0 Fill Level TXEFS.EFFL bits (TXEFS <4:0>).

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43.7.47. Error Interrupt Flag

Name: ERROR
Offset: 0x100
Reset: 0x00000000
Property: -

Note: Interrupt flags must be cleared and then read back to confirm the clear before exiting the ISR to avoid double interrupts.

Table 43-64. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								BERR
Access								R/W
Reset								0

Bit 0 – BERR AHB Bus Error Detection
The flag is set when an AHB bus error is detected. The flag is cleared by writing a 1 to the corresponding bit field. Writing a 0 has no effect. A hard reset will clear the register. When the bit is set, the Error non-maskable interrupt is generated.

Value	Description
0	No bus error detection.
1	Bus error detection.

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44. Universal Serial Bus (USB)

44.1. Overview

The Universal Serial Bus (USB) module contains analog and digital components to provide a USB 2.0 full-speed and low-speed embedded host and full-speed device. This module in Host mode is intended for use as an embedded host and therefore does not implement a UHCI or OHCI controller.

The USB module consists of the following:

- Clock generator
- USB voltage comparators
- Transceiver
- Serial Interface Engine (SIE)
- USB DMA controller
- Pull-up and pull-down resistors
- Register interface

The interface diagram of the PIC32 USB module is illustrated in Figure 44-1. The clock generator provides the 48 MHz clock required for USB full-speed and low-speed communication. The voltage comparators monitor the voltage on the V BUS pin to determine the state of the bus. The transceiver provides the analog translation between the USB bus and the digital logic. The SIE is a state machine that transfers data to and from the endpoint buffers, and generates the hardware protocol for data transfers. The USB DMA controller transfers data between the data buffers in RAM and the SIE. The integrated pull-up and pull-down resistors eliminate the need for external signaling components. The register interface allows the CPU to configure and communicate with the module. To complement the information in this data sheet, refer to Section 27. USB On-The-Go (OTG).

44.2. Features

The PIC32 USB module has the following features:

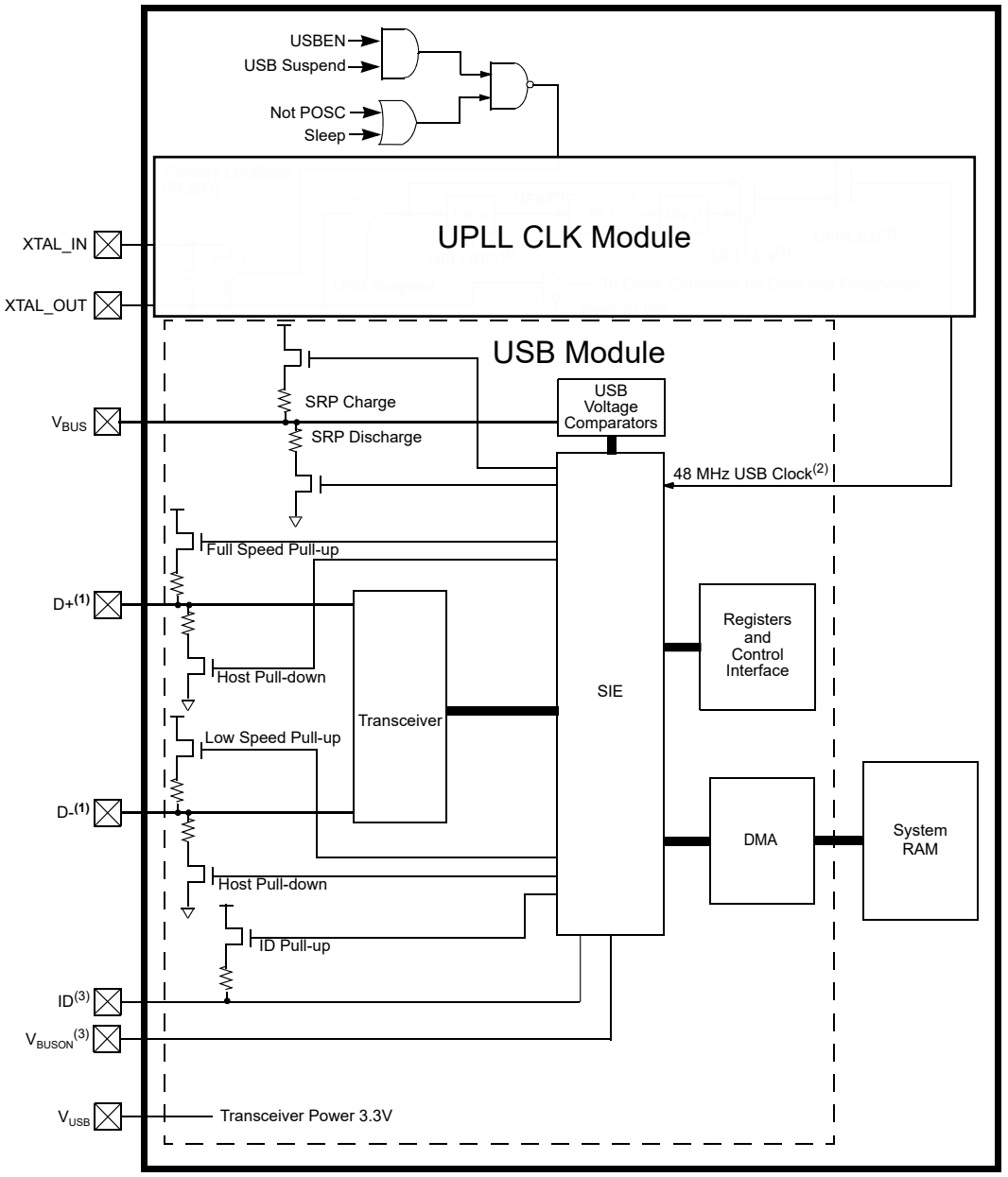
- USB full-speed support for host and device
- Low-speed host support
- USB support
- Integrated signaling resistors
- Integrated analog comparators for VBUS monitoring
- Integrated USB transceiver
- Transaction handshaking performed by hardware
- Endpoint buffering anywhere in system RAM
- Integrated DMA to access system RAM

Note: The implementation and use of the USB specifications, as well as other third-party specifications or technologies, may require licensing; including, but not limited to, USB Implementers Forum, Inc. (USB-IF). The user is fully responsible for investigating and satisfying any applicable licensing obligations.

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44.3. Block Diagram

Figure 44-1. PIC32 USB Interface Diagram



1. Pins can be used as digital inputs when USB is not enabled.
2. A 48 MHz clock is required for proper USB operation.
3. Pins can be used as GPIO when the USB module is disabled.
4. See *Clock and Reset Unit (CRU)* from Related Links for more details on clk generation.

Related Links

Clock and Reset Unit (CRU)

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44.4. USB OTG Control Registers

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See CLR, SET and INV Registers from Related Links.

Related Links

CLR, SET and INV Registers

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44.4.1. Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x403F	Reserved									
0x4040	UOTGIR	7:0	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF		VBUSVDIF
		15:8								
		23:16								
		31:24								
0x4044 ... 0x404F	Reserved									
0x4050	UOTGIE	7:0	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE		VBUSVDIE
		15:8								
		23:16								
		31:24								
0x4054 ... 0x405F	Reserved									
0x4060	UOTGSTAT	7:0	ID		LSTATE		SESVD	SESEND		VBUSVD
		15:8								
		23:16								
		31:24								
0x4064 ... 0x406F	Reserved									
0x4070	UOTGCON	7:0	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS
		15:8								
		23:16								
		31:24								
0x4074 ... 0x407F	Reserved									
0x4080	UPWRC	7:0	UACTPND			USLPGRD	USBBUSY		USUSPEND	USBPWR
		15:8								
		23:16								
		31:24								
0x4084 ... 0x41FF	Reserved									
0x4200	UIR	7:0	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF/ DETACHIF
		15:8								
		23:16								
		31:24								
0x4204 ... 0x420F	Reserved									
0x4210	UIE	7:0	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE/ DETACHIE
		15:8								
		23:16								
		31:24								
0x4214 ... 0x421F	Reserved									
0x4220	UEIR	7:0	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF		PIDEF
		15:8								
		23:16								
		31:24								

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x4224 ... 0x422F	Reserved									
0x4230	UEIE	7:0	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE/ EOFEE	PIDEE
		15:8								
		23:16								
		31:24								
0x4234 ... 0x423F	Reserved									
0x4240	USTAT	7:0	ENDPT[3:0]				DIR	PPBI		
		15:8								
		23:16								
		31:24								
0x4244 ... 0x424F	Reserved									
0x4250	UCON	7:0	JSTATE	SE0	PKTDIS/ TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN/ SOFEN
		15:8								
		23:16								
		31:24								
0x4254 ... 0x425F	Reserved									
0x4260	UADDR	7:0	LSPDEN	DEVADDR[6:0]						
		15:8								
		23:16								
		31:24								
0x4264 ... 0x426F	Reserved									
0x4270	UBDTP1	7:0	BDTPTRL[15:9]							
		15:8								
		23:16								
		31:24								
0x4274 ... 0x427F	Reserved									
0x4280	UFRML	7:0	FRML[7:0]							
		15:8								
		23:16								
		31:24								
0x4284 ... 0x428F	Reserved									
0x4290	UFRMH	7:0						FRML[2:0]		
		15:8								
		23:16								
		31:24								
0x4294 ... 0x429F	Reserved									
0x42A0	UTOK	7:0	PID[3:0]				EP[3:0]			
		15:8								
		23:16								
		31:24								
0x42A4 ... 0x42AF	Reserved									

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x42B0	USOF	7:0	CNT[7:0]							
		15:8								
		23:16								
		31:24								
0x42B4 ... 0x42BF	Reserved									
0x42C0	UBDTP2	7:0	BDTPTRH[23:16]							
		15:8								
		23:16								
		31:24								
0x42C4 ... 0x42CF	Reserved									
0x42D0	UBDTP3	7:0	BDTPTRU[31:24]							
		15:8								
		23:16								
		31:24								
0x42D4 ... 0x42DF	Reserved									
0x42E0	UCNFG1	7:0	UTEYE	UOEMON		USBSIDL				UASUSPND
		15:8								
		23:16								
		31:24								
0x42E4 ... 0x42FF	Reserved									
0x4300	UEP0	7:0	LSPD	RETRYDIS		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4304 ... 0x430F	Reserved									
0x4310	UEP1	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4314 ... 0x431F	Reserved									
0x4320	UEP2	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4324 ... 0x432F	Reserved									
0x4330	UEP3	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4334 ... 0x433F	Reserved									
0x4340	UEP4	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x4344 ... 0x434F	Reserved									
0x4350	UEP5	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4354 ... 0x435F	Reserved									
0x4360	UEP6	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4364 ... 0x436F	Reserved									
0x4370	UEP7	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4374 ... 0x437F	Reserved									
0x4380	UEP8	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4384 ... 0x438F	Reserved									
0x4390	UEP9	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x4394 ... 0x439F	Reserved									
0x43A0	UEP10	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x43A4 ... 0x43AF	Reserved									
0x43B0	UEP11	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x43B4 ... 0x43BF	Reserved									
0x43C0	UEP12	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x43C4 ... 0x43CF	Reserved									

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x43D0	UEP13	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x43D4 ... 0x43DF	Reserved									
0x43E0	UEP14	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								
0x43E4 ... 0x43EF	Reserved									
0x43F0	UEP15	7:0				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
		15:8								
		23:16								
		31:24								

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44.4.1.1. USB OTG Interrupt Status Register

Name: UOTGIR
Offset: 0x4040
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	IDIF	T1MSECIF	LSTATEIF	ACTVIF	SESVDIF	SESENDIF		VBUSVDIF
Access	R/K	R/K	R/K	R/K	R/K	R/K		R/K
Reset	0	0	0	0	0	0		0

Bit 7 – IDIF ID State Change Indicator bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Change in ID state detected
0	No change in ID state detected

Bit 6 – T1MSECIF 1 Millisecond Timer bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	1 millisecond timer has expired
0	1 millisecond timer has not expired

Bit 5 – LSTATEIF Line State Stable Indicator bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	USB line state is stable for 1 ms, but different from last time
0	USB line state is not stable for 1 ms

Bit 4 – ACTVIF Bus Activity Indicator bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Activity on the D+, D-, ID or V_{BUS} pins has caused the device to wake-up
0	Activity is not detected

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Bit 3 – SESVDIF Session Valid Change Indicator bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	V_{BUS} voltage has dropped below the session end level
0	V_{BUS} voltage has not dropped below the session end level

Bit 2 – SESENDIF B-Device V_{BUS} Change Indicator bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	A change on the session end input was detected
0	No change on the session end input was detected

Bit 0 – VBUSVDIF A-Device V_{BUS} Change Indicator bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	A change on the session end input was detected
0	No change on the session end input was detected

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44.4.1.2. USB OTG Interrupt Enable Register

Name: UOTGIE
Offset: 0x4050
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	IDIE	T1MSECIE	LSTATEIE	ACTVIE	SESVDIE	SESENDIE		VBUSVDIE
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0		0

Bit 7 – IDIE ID Interrupt Enable bit

Value	Description
1	ID interrupt enabled
0	ID interrupt disabled

Bit 6 – T1MSECIE 1 Millisecond Timer Interrupt Enable bit

Value	Description
1	1 millisecond timer interrupt enabled
0	1 millisecond timer interrupt disabled

Bit 5 – LSTATEIE Line State Interrupt Enable bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Line state interrupt enabled
0	Line state interrupt disabled

Bit 4 – ACTVIE Bus Activity Interrupt Enable bit

Value	Description
1	Bus activity interrupt enabled
0	Bus activity interrupt disabled

Bit 3 – SESVDIE Session Valid Interrupt Enable bit

Value	Description
1	Session valid interrupt enabled

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Value	Description
0	Session valid interrupt disabled

Bit 2 – SESENDIE B-Session End Interrupt Enable bit

Value	Description
1	B-session end interrupt enabled
0	B-session end interrupt disabled

Bit 0 – VBUSVDIE A-V_{BUS} Valid Interrupt Enable bit

Value	Description
1	A-V_{BUS} valid interrupt enabled
0	A-V_{BUS} valid interrupt disabled

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44.4.1.3. USB OTG Status Register

Name: UOTGSTAT
Offset: 0x4060
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ID		LSTATE		SESVD	SESEND		VBUSVD
Access	R		R		R	R		R
Reset	0		0		0	0		0

Bit 7 – ID ID Pin State Indicator bit

Value	Description
1	No cable is attached or a type B cable has been plugged into the USB receptacle
0	A “type A” OTG cable has been plugged into the USB receptacle

Bit 5 – LSTATE Line State Stable Indicator bit

Value	Description
1	USB line state (U1CON<SE0> and U1CON<JSTATE>) has been stable for the last 1 ms
0	USB line state (U1CON<SE0> and U1CON<JSTATE>) has not been stable for the last 1 ms

Bit 3 – SESVD Session Valid Change Indicator bit

Value	Description
1	V_{BUS} voltage is above Session Valid on the A or B device
0	V_{BUS} voltage is below Session Valid on the A or B device

Bit 2 – SESEND B-Session End Indicator bit

Value	Description
1	V_{BUS} voltage is below Session Valid on the B device
0	V_{BUS} voltage is above Session Valid on the B device

Bit 0 – VBUSVD A-V_{BUS} Valid Indicator bit

Value	Description
1	V_{BUS} voltage is below Session Valid on the A device
0	V_{BUS} voltage is above Session Valid on the A device

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44.4.1.4. USB OTG Control Register

Name: UOTGCON
Offset: 0x4070
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	DPPULUP	DMPULUP	DPPULDWN	DMPULDWN	VBUSON	OTGEN	VBUSCHG	VBUSDIS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – DPPULUP D+ Pull-Up Enable bit

Value	Description
1	D+ data line pull-up resistor is enabled
0	D+ data line pull-up resistor is disabled

Bit 6 – DMPULUP D- Pull-Up Enable bit

Value	Description
1	D- data line pull-up resistor is enabled
0	D- data line pull-up resistor is disabled

Bit 5 – DPPULDWN D+ Pull-Down Enable bit

Value	Description
1	D+ data line pull-down resistor is enabled
0	D+ data line pull-down resistor is disabled

Bit 4 – DMPULDWN D- Pull-Down Enable bit

Value	Description
1	D- data line pull-down resistor is enabled
0	D- data line pull-down resistor is disabled

Bit 3 – VBUSON V_{BUS} Power-on bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	V_{BUS} line is powered

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Value	Description
0	V_{BUS} line is not powered

Bit 2 – OTGEN OTG Functionality Enable bit

Value	Description
1	DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under software control
0	DPPULUP, DMPULUP, DPPULDWN and DMPULDWN bits are under USB hardware control

Bit 1 – VBUSCHG V_{BUS} Charge Enable bit

Value	Description
1	V_{BUS} line is charged through a pull-up resistor
0	V_{BUS} line is not charged through a resistor

Bit 0 – VBUSDIS V_{BUS} Discharge Enable bit

Value	Description
1	V_{BUS} line is discharged through a pull-down resistor
0	V_{BUS} line is not discharged through a resistor

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44.4.1.5. USB Power Control Register

Name: UPWRC
Offset: 0x4080
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	UACTPND			USLPGRD	USBBUSY		USUSPEND	USBPWR
Access	HS			R/W	R/W		R/W	R/K
Reset	0			0	0		0	0

Bit 7 – UACTPND USB Activity Pending bit

Value	Description
1	USB bus activity has been detected; but an interrupt is pending, it has not been generated yet
0	An interrupt is not pending

Bit 4 – USLPGRD USB Sleep Entry Guard bit

Value	Description
1	Sleep entry is blocked if USB bus activity is detected or if a notification is pending
0	USB OTG module does not block Sleep entry

Bit 3 – USBBUSY USB OTG module Busy bit

Note: When USBPWR = 0 and USBBUSY = 1, status from all other registers is invalid and writes to all USB OTG module registers produce undefined results.

Value	Description
1	USB OTG module is active or disabled, but not ready to be enabled
0	USB OTG module is not active and is ready to be enabled

Bit 1 – USUSPEND USB Suspend Mode bit

Value	Description
1	USB OTG module is placed in Suspend mode (The 48 MHz USB clock is gated off. The transceiver is placed in a low-power state.)
0	USB OTG module operates normally

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Bit 0 – USBPWR USB Operation Enable bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	USB OTG module is turned on
0	USB OTG module is disabled. Outputs held inactive, device pins not used by USB, analog features are shut down to reduce power consumption.

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44.4.1.6. USB Interrupt Register

Name: UIR
Offset: 0x4200
Reset: 0x0
Property: -

Notes:

1. This bit is valid only if the HOSTEN bit is set (see UCON register), there is no activity on the USB for 2.5 µs, and the current bus state is not SE0.
2. When not in Suspend mode, this interrupt should be disabled.
3. Clearing this bit will cause the STAT FIFO to advance.
4. Only error conditions enabled through the UEIE register will set this bit.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STALLIF	ATTACHIF	RESUMEIF	IDLEIF	TRNIF	SOFIF	UERRIF	URSTIF/ DETACHIF
Access	R/K	R/K	R/K	R/K	R/K	R/K	R/K	R/K
Reset	0	0	0	0	0	0	0	0

Bit 7 – STALLIF STALL Handshake Interrupt bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	In Host mode, a STALL handshake was received during the handshake phase of the transaction. In Device mode, a STALL handshake was transmitted during the handshake phase of the transaction.
0	STALL handshake has not been sent

Bit 6 – ATTACHIF Peripheral Attach Interrupt bit(1)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Peripheral attachment was detected by the USB OTG module
0	Peripheral attachment was not detected

Bit 5 – RESUMEIF Resume Interrupt bit(2)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	K-State is observed on the D+ or D- pin for 2.5 µs

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Value	Description
0	K-State is not observed

Bit 4 – IDLEIF Idle Detect Interrupt bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Idle condition is detected (constant Idle state of 3 ms or more)
0	No Idle condition is detected

Bit 3 – TRNIF Token Processing Complete Interrupt bit(3)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Processing of current token is complete; a read of the USTAT register provides endpoint information
0	Processing of current token is not complete

Bit 2 – SOFIF SOF Token Interrupt bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	SOF token received by the peripheral or the SOF threshold reached by the host
0	SOF token was not received nor threshold reached

Bit 1 – UERRIF USB Error Condition Interrupt bit(4)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Unmasked Error condition has occurred
0	Unmasked Error condition has not occurred

Bit 0 – URSTIF/DETACHIF URSTIF: USB Reset Interrupt bit (Device mode) DETACHIF: USB Detach Interrupt bit (Host mode)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	URSTIF: Valid USB Reset has occurred DETACHIF: Peripheral detachment was detected by the USB OTG module
0	URSTIF: No USB Reset has occurred DETACHIF: Peripheral detachment was not detected

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44.4.1.7. USB Interrupt Enable Register

Name: UIE
Offset: 0x4210
Reset: 0x0
Property: -

Note:

1. For an interrupt to propagate to the USBIF bit (IFS1<25>), the UERRIE bit (U1IE<1>) must be set.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	STALLIE	ATTACHIE	RESUMEIE	IDLEIE	TRNIE	SOFIE	UERRIE	URSTIE/ DETACHIE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – STALLIE STALL Handshake Interrupt Enable bit

Value	Description
1	STALL interrupt is enabled
0	STALL interrupt is disabled

Bit 6 – ATTACHIE ATTACH Interrupt Enable bit

Value	Description
1	ATTACH interrupt is enabled
0	ATTACH interrupt is disabled

Bit 5 – RESUMEIE RESUME Interrupt Enable bit

Value	Description
1	RESUME interrupt is enabled
0	RESUME interrupt is disabled

Bit 4 – IDLEIE Idle Detect Interrupt Enable bit

Value	Description
1	Idle interrupt is enabled
0	Idle interrupt is disabled

Bit 3 – TRNIE Token Processing Complete Interrupt Enable bit

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Value	Description
1	TRNIF interrupt is enabled
0	TRNIF interrupt is disabled

Bit 2 – SOFIE SOF Token Interrupt Enable bit

Value	Description
1	SOFIF interrupt is enabled
0	SOFIF interrupt is disabled

Bit 1 – UERRIE USB Error Interrupt Enable bit

Value	Description
1	SOFIF interrupt is enabled
0	SOFIF interrupt is disabled

Bit 0 – URSTIE/DETACHIE URSTIE: USB Reset Interrupt Enable bit (Device mode) DETACHIE: USB Detach Interrupt Enable bit (Host mode)

Value	Description
1	URSTIE: URSTIF interrupt is enabled DETACHIE: DATTCHIF interrupt is enabled
0	URSTIE: URSTIF interrupt is disabled DETACHIE: DATTCHIF interrupt is disabled

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44.4.1.8. USB Error Interrupt Status Register

Name: UEIR
Offset: 0x4220
Reset: 0x0
Property: -

Notes:

1. This type of error occurs when the module's request for the DMA bus is not granted in time to service the module's demand for memory, resulting in an overflow or underflow condition, and/or the allocated buffer size is not sufficient to store the received data packet causing it to be truncated.
2. This type of error occurs when more than 16-bit-times of Idle from the previous End-of-Packet (EOP) has elapsed.
3. This type of error occurs when the module is transmitting or receiving data and the SOF counter has reached zero.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BTSEF	BMXEF	DMAEF	BTOEF	DFN8EF	CRC16EF		PIDEF
Access	R/K	R/K	R/K	R/K	R/K	R/K		R/K
Reset	0	0	0	0	0	0		0

Bit 7 – BTSEF Bit Stuff Error Flag bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Packet is rejected due to a bit stuff error
0	Packet is accepted

Bit 6 – BMXEF Bus Matrix Error Flag bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	The base address of the BDT or the address of an individual buffer pointed to by a BDT entry, is invalid.
0	No address error

Bit 5 – DMAEF DMA Error Flag bit(1)
Write a '1' to this bit to clear the interrupt.

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Value	Description
1	USB DMA error condition detected
0	No DMA error

Bit 4 – BTOEF Bus Turnaround Time-Out Error Flag bit(2)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Bus turnaround time-out has occurred
0	No bus turnaround time-out

Bit 3 – DFN8EF Data Field Size Error Flag bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Data field received is not an integral number of bytes
0	Data field received is an integral number of bytes

Bit 2 – CRC16EF CRC16 Failure Flag bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	Data packet rejected due to CRC16 error
0	Data packet accepted

Bit 2 – CRC5EF/EOFEF CRC5EF: CRC5 Host Error Flag bit (Device mode)(3) EOFEF: EOF Error Flag bit (Host mode)
Write a '1' to this bit to clear the interrupt.

Value	Description
1	CRC5EF: Peripheral detachment was detected by the USB OTG module EOFEF: EOF error condition detected
0	CRC5EF: Peripheral detachment was not detected EOFEF: No EOF error condition

Bit 0 – PIDEF PID Check Failure Flag bit
Write a '1' to this bit to clear the interrupt.

Value	Description
1	PID check failed
0	PID check passed

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44.4.1.9. USB Error Interrupt Enable Register

Name: UEIE
Offset: 0x4230
Reset: 0x0
Property: -

Note:

1. For an interrupt to propagate USBIF bit (IFS1<25>), the UERRIE bit (U1IE<1>) must be set.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BTSEE	BMXEE	DMAEE	BTOEE	DFN8EE	CRC16EE	CRC5EE/ EOFEE	PIDEE
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – BTSEE Bit Stuff Error Interrupt Enable bit

Value	Description
1	BTSEF interrupt is enabled
0	BTSEF interrupt is disabled

Bit 6 – BMXEE Bus Matrix Error Interrupt Enable bit

Value	Description
1	BMXEF interrupt is enabled
0	BMXEF interrupt is disabled

Bit 5 – DMAEE DMA Error Interrupt Enable bit

Value	Description
1	DMAEF interrupt is enabled
0	DMAEF interrupt is disabled

Bit 4 – BTOEE Bus Turnaround Time-Out Error Interrupt Enable bit

Value	Description
1	BTOEF interrupt is enabled
0	BTOEF interrupt is disabled

Bit 3 – DFN8EE Data Field Size Error Interrupt Enable bit

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Value	Description
1	DFN8EF interrupt is enabled
0	DFN8EF interrupt is disabled

Bit 2 – CRC16EE CRC16 Failure Interrupt Enable bit

Value	Description
1	CRC16EF interrupt is enabled
0	CRC16EF interrupt is disabled

Bit 1 – CRC5EE/EOFEE CRC5EE: CRC5 Host Error Interrupt Enable bit (Device mode)(3) EOFEE: EOF Error Interrupt Enable bit (Host mode)

Value	Description
1	CRC5EE: CRC5EF interrupt is enabled EOFEE: EOF interrupt is enabled
0	CRC5EE: CRC5EF interrupt is disabled EOFEE: EOF interrupt is disabled

Bit 0 – PIDEE PID Check Failure Interrupt Enable bit

Value	Description
1	PIDEF interrupt is enabled
0	PIDEF interrupt is disabled

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44.4.1.10. USB Status Register

Name: USTAT
Offset: 0x4240
Reset: 0x0
Property: -

Note: The U1STAT register is a window into a 4 byte FIFO maintained by the USB OTG module. U1STAT value is only valid when the TRNIF bit (U1IR[3]) is active. Clearing the TRNIF bit (U1IR[3]) advances the FIFO. Data in register is invalid when the TRNIF bit (U1IR[3]) = 0.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ENDPT[3:0]				DIR	PPBI		
Access	R	R	R	R	R	R		
Reset	x	x	x	x	x	x		

Bits 7:4 – ENDPT[3:0] Encoded Number of Last Endpoint Activity bits
(Represents the number of the BDT, updated by the last USB transfer.)

Value	Description
1111	Endpoint 15
1110	Endpoint 14
...	
0001	Endpoint 1
0000	Endpoint 0

Bit 3 – DIR Last BD Direction Indicator bit

Value	Description
1	Last transaction was a TX
0	Last transaction was a RX

Bit 2 – PPBI Ping-pong BD Pointer Indicator bit

Value	Description
1	Last transaction was to the ODD BD bank
0	Last transaction was to the EVEN BD bank

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44.4.1.11. USB Control Register

Name: UCON
Offset: 0x4250
Reset: 0x0
Property: -

Notes:

1. Software is required to check this bit before issuing another token command to the UTOK register, see UTOK register.
2. All host control logic is reset any time the value of this bit is toggled.
3. Software must set RESUME for 10 ms if the part is a function, or for 25 ms if the part is a host, and then clear it to enable remote wake-up. In Host mode, the USB OTG module will append a low-speed EOP to the RESUME signaling when this bit is cleared.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	JSTATE	SE0	PKTDIS/ TOKBUSY	USBRST	HOSTEN	RESUME	PPBRST	USBEN/ SOFEN
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – JSTATE Live Differential Receiver JSTATE flag bit

Value	Description
1	JSTATE is detected on the USB
0	JSTATE is not detected

Bit 6 – SE0 Live Single-Ended Zero flag bit

Value	Description
1	Single-Ended Zero detected on the USB
0	No Single-Ended Zero detected

Bit 5 – PKTDIS/TOKBUSY PKTDIS: Packet Transfer Disable bit (Device mode) TOKBUSY: Token Busy Indicator bit (Host mode)(1)

Value	Description
1	PKTDIS: Token and packet processing disabled (set upon SETUP token received) TOKBUSY: Token and packet processing enabled

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Value	Description
0	PKTDIS: Token being executed by the USB OTG module TOKBUSY: No token being executed

Bit 4 – USBRST Module Reset bit (Host mode)

Value	Description
1	USB Reset is generated
0	USB Reset is terminated

Bit 3 – HOSTEN Host Mode Enable bit(2)

Value	Description
1	USB host capability is enabled
0	USB host capability is disabled

Bit 2 – RESUME RESUME Signaling Enable bit(3)

Value	Description
1	RESUME signaling is activated
0	RESUME signaling is disabled

Bit 1 – PPBRST Ping-Pong Buffers Reset bit

Value	Description
1	Reset all Even/Odd buffer pointers to the EVEN BD banks
0	Even/Odd buffer pointers not being Reset

Bit 0 – USBEN/SOFEN USBEN: USB OTG Module Enable bit (Device mode) SOFEN: SOF Enable bit (Host mode)

Value	Description
1	USBEN: USB OTG module and supporting circuitry are enabled SOFEN: SOF token sent every 1 ms
0	USBEN: USB OTG module and supporting circuitry are disabled SOFEN: SOF token is disabled

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44.4.1.12. USB Address Register

Name: UADDR
Offset: 0x4260
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	LSPDEN	DEVADDR[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – LSPDEN Low-Speed Enable Indicator bit

Value	Description
1	Next token command to be executed at low-speed
0	Next token command to be executed at full-speed

Bits 6:0 – DEVADDR[6:0] 7-bit USB Device Address bits

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44.4.1.13. USB BDT Register

Name: UBDTP1
Offset: 0x4270
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BDTPTRL[15:9]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bits 7:1 – BDTPTRL[15:9] BDT Base Address Low bits
This 7-bit value provides address bits 15 through 9 of the BDT base address, which defines the BDT's starting location in the system memory.
The 32-bit BDT base address is 512 byte aligned.

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44.4.1.14. USB Frame Number Low Register

Name: UFRML
Offset: 0x4280
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	FRML[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – FRML[7:0] 11-bit Frame Number Lower bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

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44.4.1.15. USB Frame Number High Register

Name: UFRMH
Offset: 0x4290
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						FRML[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – FRML[2:0] Upper 3 bits of the Frame Number bits
The register bits are updated with the current frame number whenever a SOF TOKEN is received.

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44.4.1.16. USB Token Register

Name: UTOK
Offset: 0x42A0
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PID[3:0]				EP[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:4 – PID[3:0] Token Type Indicator bits
Note: All other values are reserved and must not be used.

Value	Description
0001	OUT (TX) token type transaction
1001	IN (RX) token type transaction
1101	SETUP (TX) token type transaction

Bits 3:0 – EP[3:0] Token Command Endpoint Address bits
The four bit value must specify a valid endpoint.

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44.4.1.17. USB SOF Threshold Register

Name: USOF
Offset: 0x42B0
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CNT[7:0] SOF Threshold Value bits

Value	Description
0100 1010	64-byte packet
0010 1010	32-byte packet
0001 1010	16-byte packet
0001 0010	8-byte packet

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44.4.1.18. USB BDT Page 2 Register

Name: UBDTP2
Offset: 0x42C0
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BDTPTRH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BDTPTRH[23:16] BDT Base Address High bits
This 8-bit value provides address bits 23 through 16 of the BDT base address, which defines the BDT's starting location in the system memory.
The 32-bit BDT base address is 512 byte aligned.

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44.4.1.19. USB BDT Page 3 Register

Name: UBDTP3
Offset: 0x42D0
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BDTPTRU[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BDTPTRU[31:24] BDT Base Address Upper bits
This 8-bit value provides address bits 31 through 24 of the BDT base address, which defines the BDT's starting location in the system memory.
The 32-bit BDT base address is 512 byte aligned.

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44.4.1.20. USB Configuration 1 Register

Name: UCNFG1
Offset: 0x42E0
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	UTEYE	UOEMON		USBSIDL				UASUSPND
Access	R/W	R/W		R/W				R/W
Reset	0	0		0				0

Bit 7 – UTEYE USB Eye-Pattern Test Enable bit

Value	Description
1	Eye-Pattern test is enabled
0	Eye-Pattern test is disabled

Bit 6 – UOEMON USB $\overline{OE}$ Monitor Enable bit

Value	Description
1	OE signal is active; it indicates intervals during which the D+/D- lines are driving
0	OE signal is inactive

Bit 4 – USBSIDL Stop in Idle Mode bit

Value	Description
1	Discontinue module operation when device enters Idle mode
0	Continue module operation in Idle mode

Bit 0 – UASUSPND Automatic Suspend Enable bit

Value	Description
1	USB OTG module automatically suspends upon entry to Sleep mode. See the USUSPEND bit (U1PWRC[1]) in register UTOK **TBD**.
0	USB OTG module does not automatically suspend upon entry to Sleep mode. Software must use the USUSPEND bit (U1PWRC[1]) to suspend the module, including the USB 48 MHz clock.

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44.4.1.21. USB Endpoint Control 0 Register

Name: UEP0
Offset: 0x4300
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	LSPD	RETRYDIS		EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	0	0	0

Bit 7 – LSPD Low-Speed Direct Connection Enable bit (Host mode)

Value	Description
1	Direct connection to a low-speed device is enabled
0	Direct connection to a low-speed device is disabled; hub required with PRE_PID

Bit 6 – RETRYDIS Retry Disable bit (Host mode)

Value	Description
1	Retry NAK'd transactions are disabled
0	Retry NAK'd transactions are enabled; retry done in hardware

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN=1:

Value	Description
1	Disable endpoint 0 for control transfers; only TX and RX transfers are allowed
0	Enable endpoint 0 for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint 0 receive is enabled
0	Endpoint 0 receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint 0 transmit is enabled

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Value	Description
0	Endpoint 0 transmit is disabled

Bit 1 – EPSTALL Endpoint Stall Status bit

Value	Description
1	Endpoint 0 is stalled
0	Endpoint 0 is not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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44.4.1.22. USB Endpoint Control n Register (n=1...15)

Name: UEPn
Offset: 0x4310 + (n-1)*0x10 [n=1..15]
Reset: 0x0
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				EPCONDIS	EPRXEN	EPTXEN	EPSTALL	EPHSHK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – EPCONDIS Bidirectional Endpoint Control bit
If EPTXEN = 1 and EPRXEN=1:

Value	Description
1	Disable endpoint n for control transfers; only TX and RX transfers are allowed
0	Enable endpoint n for control (SETUP) transfers; TX and RX transfers are also allowed

Bit 3 – EPRXEN Endpoint Receive Enable bit

Value	Description
1	Endpoint n receive is enabled
0	Endpoint n receive is disabled

Bit 2 – EPTXEN Endpoint Transmit Enable bit

Value	Description
1	Endpoint n transmit is enabled
0	Endpoint n transmit is disabled

Bit 1 – EPSTALL Endpoint Stall Status bit

Value	Description
1	Endpoint n is stalled
0	Endpoint n is not stalled

Bit 0 – EPHSHK Endpoint Handshake Enable bit

Value	Description
1	Endpoint handshake is enabled

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Value	Description
0	Endpoint handshake is disabled (typically used for isochronous endpoints)

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45. Ethernet Media Access Controller (ETH)

45.1. Overview

The Ethernet Media Access Controller (ETH) module implements a 10/100 Mbps Ethernet MAC, compatible with the IEEE 802.3 standard. The ETH can operate in either half or full duplex mode at all supported speeds.

45.2. Features

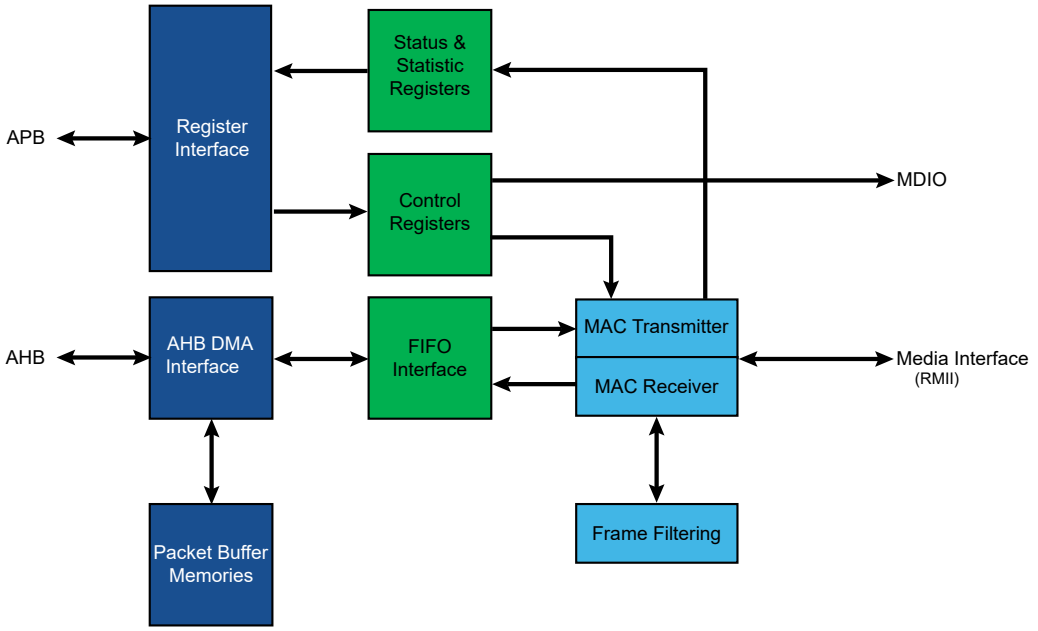
The following are key features of the ETH module:

- Compatible with IEEE Standard 802.3
- 10 and 100 Mbps Operation
- Full and Half Duplex Operation at all Supported Speeds of Operation
- Statistics Counter Registers for RMON/MIB
- RMII Interfaces to the Physical Layer
- Direct Memory Access (DMA) Interface to External Memory
- Support for 5 Priority Queues in DMA
- Programmable Burst Length and Endianism for DMA
- Interrupt Generation to Signal Receive and Transmit Completion, Errors or Other Events
- Automatic Pad and Cyclic Redundancy Check (CRC) Generation on Transmitted Frames
- Automatic Discard of Frames Received with Errors
- Receive and Transmit IP, TCP and UDP Checksum Offload. Both IPv4 and IPv6 Packet Types Supported.
- Address Checking Logic for Four Specific 48-bit Addresses, Four Type IDs, Promiscuous Mode, Hash Matching of Unicast and Multicast Destination Addresses and Wake-on-LAN
- Management Data Input/Output (MDIO) Interface for Physical Layer Management
- Support for Jumbo Frames Up To 3840 Bytes
- Full Duplex Flow Control With Recognition of Incoming Pause Frames and Hardware Generation of Transmitted Pause Frames
- Half Duplex Flow Control By Forcing Collisions on Incoming Frames
- Support for 802.1Q VLAN Tagging With Recognition of Incoming VLAN and Priority Tagged Frames
- Programmable Inter Packet Gap (IPG) Stretch
- Recognition of IEEE 1588 PTP Frames
- IEEE 1588 Time Stamp Unit (TSU)
- Support for 802.1AS Timing and Synchronization
- Support for 802.3az Energy Efficient Ethernet

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45.3. Block Diagram

Figure 45-1. Block Diagram



Note: For EPLL configuration, refer *Clock and Reset Unit (CRU)* from Related Links.

Related Links

Clock and Reset Unit (CRU)

45.4. Signal Interface

The ETH Controller module includes the following signal interfaces:

- RMII to an external PHY
- MDIO interface for external PHY management
- Client APB interface for accessing ETH registers
- Host AHB interface for memory access
- TSUCOMP signal for TSU timer count value comparison

Table 45-1. Ethernet MAC Connections in RMII Modes

Signal Name	Function	RMII
ETH_TXCK1[1]	Transmit Clock or Reference Clock	REFCK
ETH_TXEN	Transmit Enable	TXEN
Tx[1:0] and Rx[1:0]	Transmit Data	TXD[1:0]
ETH_TXER	Transmit Coding Error	Not Used
ETH_RXCK	Receive Clock	Not Used
ETH_RXDV	Receive Data Valid	CRSDV
Tx[1:0] and Rx[1:0]	Receive Data	RXD[1:0]
ETH_RXER	Receive Error	RXER
ETH_CRS	Carrier Sense and Data Valid	Not Used
ETH_COL	Collision Detect	Not Used
ETH_MDC	Management Data Clock	MDC
ETH_MDIO	Management Data Input/Output	MDIO

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Note:

1. Input only. ETH_TXCK1 must be provided with a 50 MHz clock for RMII interfaces, respectively.

45.5. Functional Description

45.5.1. Media Access Controller

The Transmit Block of the Media Access Controller (MAC) takes data from FIFO, adds preamble, checks and adds padding and frame check sequence (FCS). Both half duplex and full duplex Ethernet modes of operation are supported.

When operating in half duplex mode, the MAC Transmit Block generates data according to the Carrier Sense Multiple Access with Collision Detect (CSMA/CD) protocol. The start of transmission is deferred if Carrier Sense (CRS) is active. If Collision (COL) is detected during transmission, a jam sequence is asserted and the transmission is retried after a random back off. The CRS and COL signals have no effect in full duplex mode.

The Receive Block of the MAC checks for valid preamble, FCS, alignment and length, and presents received frames to the MAC address checking block and FIFO. Software can configure the ETH to receive jumbo frames of up to 3840 Bytes. It can optionally strip CRC (Cyclic Redundancy Check) from the received frame before transferring it to FIFO.

The Address Checker recognizes four specific 48-bit addresses, can recognize four different types of ID values, and contains a 64-bit Hash register for matching multicast and unicast addresses as required. It can recognize the broadcast address *all-'1'* (0xFFFFFFFFFFFF) and copy all frames. The MAC can also reject all frames that are not VLAN tagged, and can recognize Wake on LAN events.

The MAC Receive Block supports offloading of IP, TCP and UDP checksum calculations (both IPv4 and IPv6 packet types supported), and can automatically discard bad checksum frames.

45.5.2. IEEE 1588 Time Stamp Unit

The IEEE 1588 time stamp unit (TSU) is implemented as a 102-bit timer.

- The 48 upper bits [93:46] of the timer count seconds and are accessible in the ETH 1588 Timer Seconds High Register" (TSH) and ETH 1588 Timer Seconds Low Register (TSL)
- The 30 lower bits [45:16] of the timer count nanoseconds and are accessible in the ETH 1588 Timer Nanoseconds Register (TN)
- TISUBN register specifies the increment value in sub nanoseconds for every clock

The 46 lower bits roll over when they have counted to 1s. The timer increments by a programmable period (to approximately 15.2 femtosecond resolution) with each CLK_ETH_TSU period and can also be adjusted in 1ns resolution (incremented or decremented) through APB register accesses.

45.5.3. AHB Direct Memory Access Interface

The ETH DMA controller is connected to the MAC FIFO interface and provides a scatter-gather type capability for packet data storage.

The DMA implements packet buffering where dual-port memories are used to buffer multiple frames.

45.5.3.1. Packet Buffer DMA

- Easier to guarantee maximum line rate due to the ability to store multiple frames in the packet buffer, where the number of frames is limited by the amount of packet buffer memory and Ethernet frame size
- Full store and forward, or partial store and forward programmable options (partial store will cater for shorter latency requirements)
- Support for Transmit TCP/IP checksum offload

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- When a collision on the line occurs during transmission, the packet will be automatically replayed directly from the packet buffer memory rather than having to re-fetch through the AHB (full store and forward ONLY)
- Received erroneous packets are automatically dropped before any of the packet is presented to the AHB (full store and forward ONLY), therefore reducing AHB activity
- Supports manual RX packet flush capabilities
- Optional RX packet flush when there is lack of AHB resource

45.5.3.2. Partial Store and Forward Using Packet Buffer DMA

The DMA uses SRAM-based packet buffers, and can be programmed into a low latency mode, known as Partial Store and Forward. This mode allows for a reduced latency as the full packet is not buffered before forwarding.
Note: This option is only available when the device is configured for full duplex operation.

This feature is enabled via the programmable TX and RX Partial Store and Forward registers (TPSF and RPSF). When the transmit Partial Store and Forward mode is activated, the transmitter will only begin to forward the packet to the MAC when there is enough packet data stored in the packet buffer. Likewise, when the receive Partial Store and Forward mode is activated, the receiver will only begin to forward the packet to the AHB when enough packet data is stored in the packet buffer. The amount of packet data required to activate the forwarding process is programmable via watermark registers. These registers are located at the same address as the partial store and forward enable bits.
Note: The minimum operational value for the TX partial store and forward watermark is 20. There is no operational limit for the RX partial store and forward watermark.

Enabling Partial Store and Forward is a useful means to reduce latency, but there are performance implications. The ETH DMA uses separate transmit and receive lists of buffer descriptors, with each descriptor describing a buffer area in memory. This allows Ethernet packets to be broken up and scattered around the AHB memory space.

45.5.3.3. Receive AHB Buffers

Received frames, optionally including FCS, are written to receive AHB buffers stored in memory. The receive buffer depth is programmable in the range of 64 Bytes to 10 KBytes through the DMA Configuration register (DCFGR), with the default being 128 Bytes.

The start location for each receive AHB buffer is stored in memory in a list of receive buffer descriptors at an address location pointed to by the receive buffer queue pointer. The base address for the receive buffer queue pointer is configured in software using the Receive Buffer Queue Base Address register (RBQB).

Each list entry consists of two words. The first is the address of the receive AHB buffer and the second the receive status.

If the length of a receive frame exceeds the AHB buffer length, the status word for the used buffer is written with zeroes except for the “Start of Frame” bit, which is always set for the first buffer in a frame.

Bit zero of the address field is written to 1 to show that the buffer has been used. The receive buffer manager then reads the location of the next receive AHB buffer and fills that with the next part of the received frame data. AHB buffers are filled until the frame is complete and the final buffer descriptor status word contains the complete frame status. See the following table for details of the receive buffer descriptor list.

Table 45-2. Receive Buffer Descriptor Entry

Bit	Function
Word 0	
31:2	Address of beginning of buffer

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Table 45-2. Receive Buffer Descriptor Entry (continued)

Bit	Function
1	Wrap—marks last descriptor in receive buffer descriptor list.
0	Ownership—needs to be zero for the ETH to write data to the receive buffer. The ETH sets this to one once it has successfully written a frame to memory. Software has to clear this bit before the buffer can be used again.
Word 1	
31	Global all ones broadcast address detected
30	Multicast hash match
29	Unicast hash match
28	–
27	Specific Address Register match found, bit 25 and bit 26 indicate which Specific Address Register causes the match.
26:25	Specific Address Register match. Encoded as follows: 00: Specific Address Register 1 match 01: Specific Address Register 2 match 10: Specific Address Register 3 match 11: Specific Address Register 4 match If more than one specific address is matched only one is indicated with priority 4 down to 1.
24	This bit has a different meaning depending on whether RX checksum offloading is enabled. With RX checksum offloading disabled: (bit 24 clear in Network Configuration Register) Type ID register match found, bit 22 and bit 23 indicate which type ID register causes the match. With RX checksum offloading enabled: (bit 24 set in Network Configuration Register) 0: The frame was not SNAP encoded and/or had a VLAN tag with the Canonical Format Indicator (CFI) bit set. 1: The frame was SNAP encoded and had either no VLAN tag or a VLAN tag with the CFI bit not set.
23:22	This bit has a different meaning depending on whether RX checksum offloading is enabled. With RX checksum offloading disabled: (bit 24 clear in Network Configuration) Type ID register match. Encoded as follows: 00: Type ID register 1 match 01: Type ID register 2 match 10: Type ID register 3 match 11: Type ID register 4 match If more than one Type ID is matched only one is indicated with priority 4 down to 1. With RX checksum offloading enabled: (bit 24 set in Network Configuration Register) 00: Neither the IP header checksum nor the TCP/UDP checksum was checked. 01: The IP header checksum was checked and was correct. Neither the TCP nor UDP checksum was checked. 10: Both the IP header and TCP checksum were checked and were correct. 11: Both the IP header and UDP checksum were checked and were correct.
21	VLAN tag detected—type ID of 0x8100. For packets incorporating the stacked VLAN processing feature, this bit will be set if the second VLAN tag has a type ID of 0x8100
20	Priority tag detected—type ID of 0x8100 and null VLAN identifier. For packets incorporating the stacked VLAN processing feature, this bit will be set if the second VLAN tag has a type ID of 0x8100 and a null VLAN identifier.
19:17	VLAN priority—only valid if bit 21 is set.
16	Canonical format indicator (CFI) bit (only valid if bit 21 is set).
15	End of frame—when set the buffer contains the end of a frame. If end of frame is not set, then the only valid status bit is start of frame (bit 14).
14	Start of frame—when set the buffer contains the start of a frame. If both bits 15 and 14 are set, the buffer contains a whole frame.

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Table 45-2. Receive Buffer Descriptor Entry (continued)

Bit	Function
13	This bit has a different meaning depending on whether jumbo frames and ignore FCS modes are enabled. If neither mode is enabled this bit will be zero. With jumbo frame mode enabled: (bit 3 set in Network Configuration Register) Additional bit for length of frame (bit[13]), that is concatenated with bits[12:0] With ignore FCS mode enabled and jumbo frames disabled: (bit 26 set in Network Configuration Register and bit 3 clear in Network Configuration Register) This indicates per frame FCS status as follows: 0: Frame had good FCS 1: Frame had bad FCS, but was copied to memory as ignore FCS enabled.
12:0	These bits represent the length of the received frame which may or may not include FCS depending on whether FCS discard mode is enabled. With FCS discard mode disabled: (bit 17 clear in Network Configuration Register) Least significant 12 bits for length of frame including FCS. If jumbo frames are enabled, these 12 bits are concatenated with bit[13] of the descriptor above. With FCS discard mode enabled: (bit 17 set in Network Configuration Register) Least significant 12 bits for length of frame excluding FCS. If jumbo frames are enabled, these 12 bits are concatenated with bit[13] of the descriptor above.

Each receive AHB buffer start location is a word address. The start of the first AHB buffer in a frame can be offset by up to three Bytes, depending on the value written to bits 14 and 15 of the Network Configuration register (NCFGR). If the start location of the AHB buffer is offset, the available length of the first AHB buffer is reduced by the corresponding number of Bytes.

To receive frames, the AHB buffer descriptors must be initialized by writing an appropriate address to bits 31:2 in the first word of each list entry. Bit 0 must be written with zero. Bit 1 is the wrap bit and indicates the last entry in the buffer descriptor list.

The start location of the receive buffer descriptor list must be written with the receive buffer queue base address before reception is enabled (receive enable in the Network Control register NCR). Once reception is enabled, any writes to the Receive Buffer Queue Base Address register (RBQB) are ignored. When read, it will return the current pointer position in the descriptor list, though this is only valid and stable when receive is disabled.

If the filter block indicates that a frame should be copied to memory, the receive data DMA operation starts writing data into the receive buffer. If an error occurs, the buffer is recovered.

An internal counter within the ETH represents the receive buffer queue pointer and it is not visible through the CPU interface. The receive buffer queue pointer increments by two words after each buffer has been used. It re-initializes to the receive buffer queue base address if any descriptor has its wrap bit set.

As receive AHB buffers are used, the receive AHB buffer manager sets bit zero of the first word of the descriptor to logic one indicating the AHB buffer has been used.

Software should search through the “used” bits in the AHB buffer descriptors to find out how many frames have been received, checking the start of frame and end of frame bits.

When the DMA is configured in the packet buffer Partial Store And Forward mode, received frames are written out to the AHB buffers as soon as enough frame data exists in the packet buffer. For both cases, this may mean several full AHB buffers are used before some error conditions can be detected. If a receive error is detected the receive buffer currently being written will be recovered. Previous buffers will not be recovered. As an example, when receiving frames with cyclic redundancy check (CRC) errors or excessive length, it is possible that a frame fragment might be stored in a sequence of AHB receive buffers. Software can detect this by looking for start of frame bit set in a buffer following a buffer with no end of frame bit set.

To function properly, a 10/100 Ethernet system should have no excessive length frames or frames greater than 128 Bytes with CRC errors. Collision fragments will be less than 128 Bytes long,

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therefore it will be a rare occurrence to find a frame fragment in a receive AHB buffer, when using the default value of 128 Bytes for the receive buffers size.

When in packet buffer full store and forward mode, only good received frames are written out of the DMA, so no fragments will exist in the AHB buffers due to MAC receiver errors. There is still the possibility of fragments due to DMA errors, for example used bit read on the second buffer of a multi-buffer frame.

If bit zero of the receive buffer descriptor is already set when the receive buffer manager reads the location of the receive AHB buffer, the buffer has been already used and cannot be used again until software has processed the frame and cleared bit zero. In this case, the “buffer not available” bit in the receive status register is set and an interrupt triggered. The receive resource error statistics register is also incremented.

When the DMA is configured in the packet buffer full store and forward mode, the user can optionally select whether received frames should be automatically discarded when no AHB buffer resource is available. This feature is selected via the DMA Discard Receive Packets bit in the DMA Configuration register (DCFGR.DDRP). By default, the received frames are not automatically discarded. If this feature is off, then received packets will remain to be stored in the SRAM-based packet buffer until AHB buffer resource next becomes available. This may lead to an eventual packet buffer overflow if packets continue to be received when bit zero (used bit) of the receive buffer descriptor remains set.
Note: After a used bit has been read, the receive buffer manager will re-read the location of the receive buffer descriptor every time a new packet is received. When the DMA is not configured in the packet buffer full store and forward mode and a used bit is read, the frame currently being received will be automatically discarded.

When the DMA is configured in the packet buffer full store and forward mode, a receive overrun condition occurs when the receive SRAM-based packet buffer is full, or because HRESP was not OK. In all other modes, a receive overrun condition occurs when either the AHB bus was not granted quickly enough, or because HRESP was not OK, or because a new frame has been detected by the receive block, but the status update or write back for the previous frame has not yet finished. For a receive overrun condition, the receive overrun interrupt is asserted and the buffer currently being written is recovered. The next frame that is received whose address is recognized reuses the buffer.

In any packet buffer mode, writing a '1' to the Flush Next Package bit in the NCR register (NCR.FNP) will force a packet from the external SRAM-based receive packet buffer to be flushed. This feature is only acted upon when the RX DMA is not currently writing packet data out to AHB, i.e., it is in an IDLE state. If the RX DMA is active, NCR.FNP=1 is ignored.

45.5.3.4. Transmit AHB Buffers

Frames to transmit are stored in one or more transmit AHB buffers. Transmit frames can be between 1 and 10240 Bytes long, so it is possible to transmit frames longer than the maximum length specified in the IEEE 802.3 standard. It should be noted that zero length AHB buffers are allowed and that the maximum number of buffers permitted for each transmit frame is 128.

The start location for each transmit AHB buffer is stored in memory in a list of transmit buffer descriptors at a location pointed to by the transmit buffer queue pointer. The base address for this queue pointer is set in software using the Transmit Buffer Queue Base Address register. Each list entry consists of two words. The first is the Byte address of the transmit buffer and the second containing the transmit control and status. For the packet buffer DMA, the start location for each AHB buffer is a Byte address, the bottom bits of the address being used to offset the start of the data from the data-word boundary (i.e., bits 2,1 and 0 are used to offset the address for 64-bit data paths).

Frames can be transmitted with or without automatic Cyclic Redundancy Checksum (CRC) generation. If CRC is automatically generated, pad will also be automatically generated to take frames to a minimum length of 64 Bytes. When CRC is not automatically generated (as defined in

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word 1 of the transmit buffer descriptor), the frame is assumed to be at least 64 Bytes long and pad is not generated.

An entry in the transmit buffer descriptor list is described in this table:

Table 45-3. Transmit Buffer Descriptor Entry

Bit	Function
Word 0	
31:0	Byte address of buffer
Word 1	
31	Used—must be zero for the ETH to read data to the transmit buffer. The ETH sets this to one for the first buffer of a frame once it has been successfully transmitted. Software must clear this bit before the buffer can be used again.
30	Wrap—marks last descriptor in transmit buffer descriptor list. This can be set for any buffer within the frame.
29	Retry limit exceeded, transmit error detected
28	Transmit underrun—occurs when the start of packet data has been written into the FIFO and either HRESP is not OK, the transmit data could not be fetched in time, or when buffers are exhausted.
27	Transmit frame corruption due to AHB error—set if an error occurs while midway through reading transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame (if the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and TXER asserted). Also set if single frame is too large for configured packet buffer memory size.
26	Late collision, transmit error detected.
25:23	Reserved
22:20	Transmit IP/TCP/UDP checksum generation offload errors: 000: No Error. 001: The Packet was identified as a VLAN type, but the header was not fully complete, or had an error in it. 010: The Packet was identified as a SNAP type, but the header was not fully complete, or had an error in it. 011: The Packet was not of an IP type, or the IP packet was invalidly short, or the IP was not of type IPv4/IPv6. 100: The Packet was not identified as VLAN, SNAP or IP. 101: Non supported packet fragmentation occurred. For IPv4 packets, the IP checksum was generated and inserted. 110: Packet type detected was not TCP or UDP. TCP/UDP checksum was therefore not generated. For IPv4 packets, the IP checksum was generated and inserted. 111: A premature end of packet was detected and the TCP/UDP checksum could not be generated.
19:17	Reserved
16	No CRC to be appended by MAC. When set, this implies that the data in the buffers already contains a valid CRC, therefore no CRC or padding is to be appended to the current frame by the MAC. This control bit must be set for the first buffer in a frame and will be ignored for the subsequent buffers of a frame. Note that this bit must be clear when using the transmit IP/TCP/UDP checksum generation offload, otherwise checksum generation and substitution will not occur.
15	Last buffer, when set this bit will indicate the last buffer in the current frame has been reached.
14	Reserved
13:0	Length of buffer

To transmit frames, the buffer descriptors must be initialized by writing an appropriate Byte address to bits [31:0] of the first word of each descriptor list entry.

The second word of the transmit buffer descriptor is initialized with control information that indicates the length of the frame, whether or not the MAC is to append CRC and whether the buffer is the last buffer in the frame.

After transmission the status bits are written back to the second word of the first buffer along with the used bit. Bit 31 is the used bit which must be zero when the control word is read if transmission is to take place. It is written to '1' once the frame has been transmitted. Bits[29:20] indicate various transmit error conditions. Bit 30 is the wrap bit which can be set for any buffer within a frame. If no wrap bit is encountered the queue pointer continues to increment.

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The Transmit Buffer Queue Base Address register can only be updated while transmission is disabled or halted; otherwise any attempted write will be ignored. When transmission is halted the transmit buffer queue pointer will maintain its value. Therefore when transmission is restarted the next descriptor read from the queue will be from immediately after the last successfully transmitted frame. As long as transmit is disabled by writing a '0' to the Transmit Enable bit in the Network Control register (NCR.TXEN), the transmit buffer queue pointer resets to point to the address indicated by the Transmit Buffer Queue Base Address register (TBQB).
Note: Disabling receive does not have the same effect on the receive buffer queue pointer.

Once the transmit queue is initialized, transmit is activated by writing a '1' to the Start Transmission bit of the Network Control register (NCR.TSTART). Transmit is halted when a buffer descriptor with its used bit set is read, a transmit error occurs, or by writing to the Transmit Halt bit of the Network Control register (NCR.THALT). Transmission is suspended if a pause frame is received while the Transmit Pause Frame bit is '1' in the Network Configuration register (NCR.TXPF). Rewriting the Start bit (NCR.TSTART) while transmission is active is allowed. This is implemented by the Transmit Go variable which is readable in the Transmit Status register (TSR.TXGO). The TXGO variable is reset when:

- Transmit is disabled
- A buffer descriptor with its ownership bit set is read
- Bit 10, THALT, of the Network Control register is written
- There is a transmit error such as too many retries, or a transmit underrun

To set TXGO, write a '1' to NCR.TSTART. Transmit halt does not take effect until any ongoing transmit finishes.

The DMA transmission will automatically restart from the first buffer of the frame.

If the DMA is configured for packet buffer Partial Store and Forward mode and a collision occurs during transmission of a multi-buffer frame, transmission will automatically restart from the first buffer of the frame. For packet buffer mode, the entire contents of the frame are read into the transmit packet buffer memory, so the retry attempt will be replayed directly from the packet buffer memory rather than having to re-fetch through the AHB.

If a used bit is read midway through transmission of a multi-buffer frame, this is treated as a transmit error. Transmission stops, TXER is asserted and the FCS will be bad.

If transmission stops due to a transmit error or a used bit being read, transmission restarts from the first buffer descriptor of the frame being transmitted when the transmit start bit is rewritten.

45.5.3.5. DMA Bursting on the AHB

The DMA will always use SINGLE, or INCR type AHB accesses for buffer management operations. When performing data transfers, the AHB burst length is selected by the Fixed Burst Length for DMA Data Operations bit field in the DMA Configuration register (DCFGR.FBLDO) so that either SINGLE or fixed length incrementing bursts (INCR4, INCR8 or INCR16) are used where possible:

When there is enough space and enough data to be transferred, the programmed fixed length bursts will be used. If there is not enough data or space available, for example when at the beginning or the end of a buffer, SINGLE type accesses are used. Also SINGLE type accesses are used at 1024 Byte boundaries, so that the 1 KByte boundaries are not burst over as per AHB requirements.

The DMA will not terminate a fixed length burst early, unless an error condition occurs on the AHB or if receive or transmit are disabled in the Network Control register (NCR).

45.5.3.6. DMA Packet Buffer

The DMA uses packet buffers for both transmit and receive paths. This mode allows multiple packets to be buffered in both transmit and receive directions. This allows the DMA to withstand far

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greater access latencies on the AHB and make more efficient use of the AHB bandwidth. There are two modes of operation—Full Store and Forward and Partial Store and Forward.

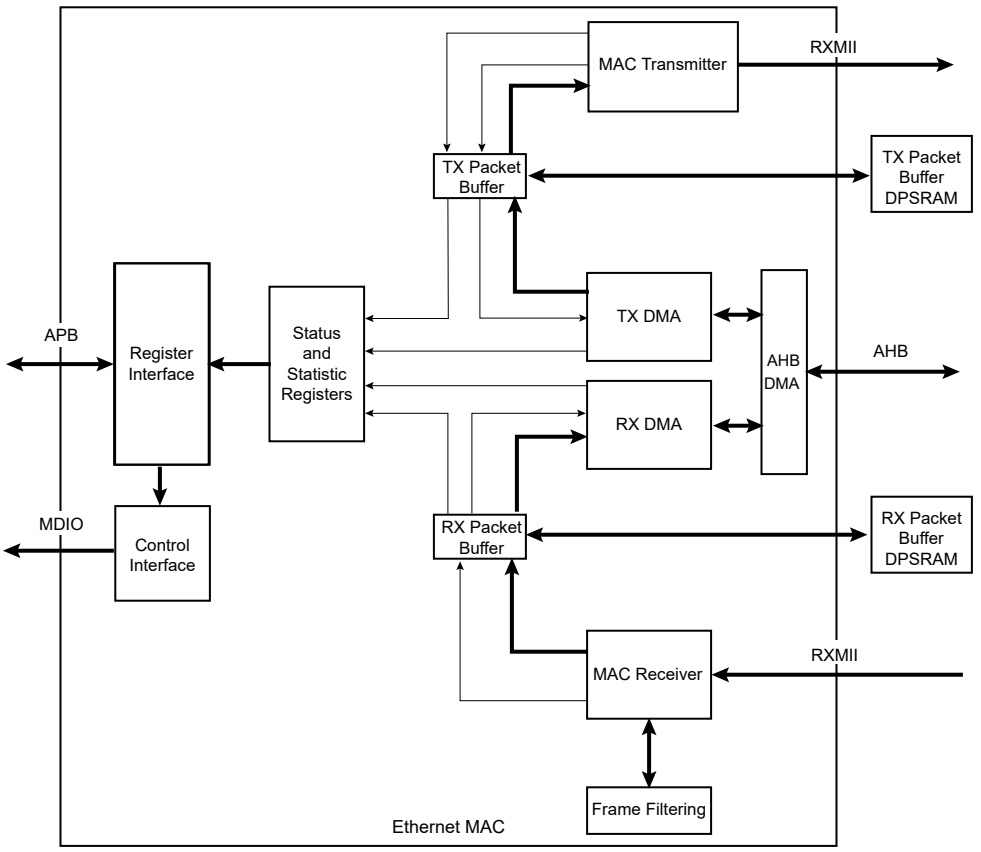
As described above, the DMA can be programmed into a low latency mode, known as Partial Store and Forward. For more details of this mode, see *Direct Memory Access Controller (DMAC)* from Related Links.

When the DMA is in full store and forward mode, full packets are buffered which provides the possibility to:

- Discard packets with error on the receive path before they are partially written out of the DMA, therefore saving AHB bus bandwidth and driver processing overhead,
- Retry collided transmit frames from the buffer, therefore saving AHB bus bandwidth,
- Implement transmit IP/TCP/UDP checksum generation offload.

With the packet buffers included, the structure of the ETH data paths is shown in this image:

Figure 45-2. Data Paths with Packet Buffers Included



Related Links

Direct Memory Access Controller (DMAC)

45.5.3.7. Transmit Packet Buffer

The transmitter packet buffer will continue attempting to fetch frame data from the AHB system memory until the packet buffer itself is full, at which point it will attempt to maintain its full level.

To accommodate the status and statistics associated with each frame, two or four words (configured in 64-bit data path mode) are reserved at the end of the packet data. If the packet is bad and requires to be dropped, the status and statistics are the only information held on that packet. Storing the status in the DPRAM is required in order to decouple the DMA interface of the buffer

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from the MAC interface, to update the MAC status/statistics and to generate interrupts in the order in which the packets that they represent were fetched from the AHB memory.

If any errors occur on the AHB while reading the transmit frame, the fetching of packet data from AHB memory is halted. The MAC transmitter will continue to fetch packet data, thereby emptying the packet buffer and allowing any good (non-erroneous) frames to be transmitted successfully. Once these have been fully transmitted, the status/statistics for the erroneous frame will be updated and software will be informed via an interrupt that an AHB error occurred. This way, the error is reported in the correct packet order.

The transmit packet buffer will only attempt to read more frame data from the AHB when space is available in the packet buffer memory. If space is not available it must wait until the a packet fetched by the MAC completes transmission and is subsequently removed from the packet buffer memory.
Note: If full store and forward mode is active and if a single frame is fetched that is too large for the packet buffer memory, the frame is flushed and the DMA halted with an error status. This is because a complete frame must be written into the packet buffer before transmission can begin, and therefore the minimum packet buffer memory size should be chosen to satisfy the maximum frame to be transmitted in the application.

In full store and forward mode, once the complete transmit frame is written into the packet buffer memory, a trigger is sent across to the MAC transmitter, which will then begin reading the frame from the packet buffer memory. Since the whole frame is present and stable in the packet buffer memory an underflow of the transmitter is not possible. The frame is kept in the packet buffer until notification is received from the MAC that the frame data has either been successfully transmitted or can no longer be retransmitted (too many retries in half duplex mode). When this notification is received the frame is flushed from memory to make room for a new frame to be fetched from AHB system memory.

In Partial Store and Forward mode, a trigger is sent across to the MAC transmitter as soon as sufficient packet data is available, which will then begin fetching the frame from the packet buffer memory. If, after this point, the MAC transmitter is able to fetch data from the packet buffer faster than the AHB DMA can fill it, an underflow of the transmitter is possible. In this case, the transmission is terminated early, and the packet buffer is completely flushed. Transmission can only be restarted by writing a '1' to the Transmit Start bit in the Network Control register (NCR.TSTART).

In half duplex mode, the frame is kept in the packet buffer until notification is received from the MAC that the frame data has either been successfully transmitted or can no longer be retransmitted (too many retries in half duplex mode). When this notification is received the frame is flushed from memory to make room for a new frame to be fetched from AHB system memory.

In full duplex mode, the frame is removed from the packet buffer on the fly.

Other than underflow, the only MAC related errors that can occur are due to collisions during half duplex transmissions. When a collision occurs the frame still exists in the packet buffer memory so can be retried directly from there. After sixteen failed transmit attempts, the frame will be flushed from the packet buffer.

45.5.3.8. Receive Packet Buffer

The receive packet buffer stores frames from the MAC receiver along with their status and statistics. Frames with errors are flushed from the packet buffer memory, while good frames are pushed onto the DMA AHB interface.

The receiver packet buffer monitors the FIFO write interface from the MAC receiver and translates the FIFO pushes into packet buffer writes. At the end of the received frame the status and statistics are buffered so that the information can be used when the frame is read out. When programmed in full store and forward mode and the frame has an error, the frame data is immediately flushed from the packet buffer memory allowing subsequent frames to utilize the freed up space. The status and statistics for bad frames are still used to update the ETH registers.

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To accommodate the status and statistics associated with each frame, two or four words (configured in 64-bit data path mode) are reserved at the end of the packet data. If the packet is bad and requires to be dropped, the status and statistics are the only information held on that packet.

The receiver packet buffer will also detect a full condition so that an overflow condition can be detected. If this occurs, subsequent packets are dropped and an RX overflow interrupt is raised.

For full store and forward, the DMA only begins packet fetches once the status and statistics for a frame are available. If the frame has a bad status due to a frame error, the status and statistics are passed on to the ETH registers. If the frame has a good status, the information is used to read the frame from the packet buffer memory and burst onto the AHB using the DMA buffer management protocol. Once the last frame data has been transferred to the packet buffer, the status and statistics are updated to the ETH registers.

If Partial Store and Forward mode is active, the DMA will begin fetching the packet data before the status is available. As soon as the status becomes available, the DMA will fetch this information as soon as possible before continuing to fetch the remainder of the frame. Once the last frame data has been transferred to the packet buffer, the status and statistics are updated to the ETH registers.

45.5.4. MAC Transmit Block

The MAC transmitter can operate in either half duplex or full duplex mode and transmits frames in accordance with the Ethernet IEEE 802.3 standard. In half duplex mode, the CSMA/CD protocol of the IEEE 802.3 specification is followed.

A small input buffer receives data through the FIFO interface which, depending on the DMA bus width control bits in the Network Configuration register, will extract data in 32-bit or 64-bit form. All subsequent processing prior to the final output is performed in bytes.

Transmit data can be output using the RMII interface.

Frame assembly starts by adding preamble and the start frame delimiter. Data is taken from the transmit FIFO interface a word at a time. Transmit data to the PHY is two bit wide and least significant bits first using TXD[1:0] with TXD[7:2] being unused tied to logic 0.

If necessary, padding is added to take the frame length to 60 bytes. CRC is calculated using an order 32-bit polynomial. This is inverted and appended to the end of the frame taking the frame length to a minimum of 64 bytes. If the no CRC bit is set in the second word of the last buffer descriptor of a transmit frame, neither pad nor CRC are appended. The no CRC bit can also be set through the FIFO interface.

In full duplex mode (at all data rates), frames are transmitted immediately. Back to back frames are transmitted at least 96 bit times apart to guarantee the interframe gap.

In half duplex mode, the transmitter checks carrier sense. If asserted, the transmitter waits for the signal to become inactive, and then starts transmission after the interframe gap of 96 bit times. If the collision signal is asserted during transmission, the transmitter will transmit a jam sequence of 32 bits taken from the data register and then retry transmission after the back off time has elapsed. If the collision occurs during either the preamble or Start Frame Delimiter (SFD), then these fields will be completed prior to generation of the jam sequence.

The back off time is based on an XOR of the 10 least significant bits of the data coming from the transmit FIFO interface and a 10-bit pseudo random number generator. The number of bits used depends on the number of collisions seen. After the first collision 1 bit is used, then the second 2 bits and so on up to the maximum of 10 bits. All 10 bits are used above ten collisions. An error will be indicated and no further attempts will be made if 16 consecutive attempts cause collision. This operation is compliant with the description in Clause 4.2.3.2.5 of the IEEE 802.3 standard which refers to the truncated binary exponential back off algorithm.

Both collisions and late collisions are treated identically, and back off and retry will be performed up to 16 times. This condition is reported in the transmit buffer descriptor word 1 (late collision, bit 26)

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and also in the Transmit Status register (late collision, bit 7). An interrupt can also be generated (if enabled) when this exception occurs, and bit 5 in the Interrupt Status register will be set.

By setting when bit 28 is set in the Network Configuration register, the Inter Packet Gap (IPG) may be stretched beyond 96 bits depending on the length of the previously transmitted frame and the value written to the IPG Stretch register (IPGS). The least significant 8 bits of the IPG Stretch register multiply the previous frame length (including preamble). The next significant 8 bits (+1 so as not to get a divide by zero) divide the frame length to generate the IPG. IPG stretch only works in full duplex mode and when bit 28 is set in the Network Configuration register. The IPG Stretch register cannot be used to shrink the IPG below 96 bits.

If the back pressure bit is set in the Network Control register, the transmit block transmits 64 bits of data, which can consist of 16 nibbles of 1011 or in bit rate mode 64 1s, whenever it sees an incoming frame to force a collision. This provides a way of implementing flow control in half duplex mode.

45.5.5. MAC Receive Block

All processing within the MAC receive block is implemented using a 16-bit data path. The MAC receive block checks for valid preamble, FCS, alignment and length, presents received frames to the FIFO interface and stores the frame destination address for use by the address checking block.

If, during the frame reception, the frame is found to be too long, a bad frame indication is sent to the FIFO interface. The receiver logic ceases to send data to memory as soon as this condition occurs.

At end of frame reception the receive block indicates to the DMA block whether the frame is good or bad. The DMA block will recover the current receive buffer if the frame was bad.

Ethernet frames are normally stored in DMA memory complete with the FCS. Setting the FCS remove bit in the network configuration (bit 17) causes frames to be stored without their corresponding FCS. The reported frame length field is reduced by four bytes to reflect this operation.

The receive block signals to the register block to increment the alignment, CRC (FCS), short frame, long frame, jabber or receive symbol errors when any of these exception conditions occur.

If bit 26 is set in the network configuration, CRC errors will be ignored and CRC errored frames will not be discarded, though the Frame Check Sequence Errors statistic register will still be incremented. Additionally, if not enabled for jumbo frames mode, then bit[13] of the receiver descriptor word 1 will be updated to indicate the FCS validity for the particular frame. This is useful for applications such as EtherCAT whereby individual frames with FCS errors must be identified.

Received frames can be checked for length field error by setting the length field error frame discard bit of the Network Configuration register (bit-16). When this bit is set, the receiver compares a frame's measured length with the length field (bytes 13 and 14) extracted from the frame. The frame is discarded if the measured length is shorter. This checking procedure is for received frames between 64 bytes and 1518 bytes in length.

Each discarded frame is counted in the 10-bit length field error statistics register. Frames where the length field is greater than or equal to 0x0600 hex will not be checked.

45.5.6. Checksum Offload for IP, TCP and UDP

The ETH can be programmed to perform IP, TCP and UDP checksum offloading in both receive and transmit directions, which is enabled by setting bit 24 in the Network Configuration register (NCFGR.RXCOEN =1) for receive and bit 11 in the DMA Configuration register (DCFGR.TXCOEN =1) for transmit.

IPv4 packets contain a 16-bit checksum field, which is the 16-bit 1’s complement of the 1’s complement sum of all 16-bit words in the header. TCP and UDP packets contain a 16-bit checksum field, which is the 16-bit 1’s complement of the 1’s complement sum of all 16-bit words in the header, the data and a conceptual IP pseudo header.

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To calculate these checksums in software requires each byte of the packet to be processed. For TCP and UDP this can use a large amount of processing power. Offloading the checksum calculation to hardware can result in significant performance improvements.

For IP, TCP or UDP checksum offload to be useful, the operating system containing the protocol stack must be aware that this offload is available so that it can make use of the fact that the hardware can either generate or verify the checksum.

45.5.6.1. Receiver Checksum Offload

When receive checksum offloading is enabled in the ETH Network Configuration Register (NCFGR.RXCOEN), the IPv4 header checksum is checked as per RFC 791, where the packet meets the following criteria:

- If present, the VLAN header must be four octets long and the CFI bit must not be set
- Encapsulation must be RFC 894 Ethernet Type Encoding or RFC 1042 SNAP Encoding
- IPv4 packet
- IP header is of a valid length

The ETH also checks the TCP checksum as per RFC 793, or the UDP checksum as per RFC 768, if the following criteria are met:

- IPv4 or IPv6 packet
- Good IP header checksum (if IPv4)
- No IP fragmentation
- TCP or UDP packet

When an IP, TCP or UDP frame is received, the receive buffer descriptor gives an indication if the ETH was able to verify the checksums. There is also an indication if the frame had SNAP encapsulation. These indication bits will replace the type ID match indication bits when the receive checksum offload is enabled. For details of these indication bits refer to “Receive Buffer Description Entry”.

If any of the checksums are verified as incorrect by the ETH, the packet is discarded and the appropriate statistics counter incremented.

45.5.6.2. Transmitter Checksum Offload

The transmitter checksum offload is only available if the full store and forward mode is enabled. This is because the complete frame to be transmitted must be read into the packet buffer memory before the checksum can be calculated and written back into the headers at the beginning of the frame.

Transmitter checksum offload is enabled by setting bit [11] in the DMA Configuration register (DCFGR.TXCOEN =1). When enabled, it will monitor the frame as it is written into the transmitter packet buffer memory to automatically detect the protocol of the frame. Protocol support is identical to the receiver checksum offload.

For transmit checksum generation and substitution to occur, the protocol of the frame must be recognized and the frame must be provided without the FCS field, by making sure that bit [16] of the transmit descriptor word 1 is clear. If the frame data already had the FCS field, this would be corrupted by the substitution of the new checksum fields.

If these conditions are met, the transmit checksum offload engine will calculate the IP, TCP and UDP checksums as appropriate. Once the full packet is completely written into packet buffer memory, the checksums will be valid and the relevant DPRAM locations will be updated for the new checksum fields as per standard IP/TCP and UDP packet structures.

If the transmitter checksum engine is prevented from generating the relevant checksums, bits [22:20] of the transmitter DMA writeback status will be updated to identify the reason for the error.

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Note that the frame will still be transmitted but without the checksum substitution, as typically the reason that the substitution did not occur was that the protocol was not recognized.

45.5.7. MAC Filtering Block

The filter block determines which frames should be written to the FIFO interface and on to the DMA.

Whether a frame is passed depends on what is enabled in the Network Configuration register, the state of the external matching pins, the contents of the specific address, type and Hash registers and the frame's destination address and type field.

If bit 25 of the Network Configuration register (NCFGR.EFRHD) is not set, a frame will not be copied to memory if the ETH is transmitting in half duplex mode at the time a destination address is received.

Ethernet frames are transmitted a byte at a time, least significant bit first. The first six bytes (48 bits) of an Ethernet frame make up the destination address. The first bit of the destination address, which is the LSB of the first byte of the frame, is the group or individual bit. This is one for multicast addresses and zero for unicast. The all ones address is the broadcast address and a special case of multicast.

The ETH supports recognition of four specific addresses. Each specific address requires two registers, Specific Address register Bottom and Specific Address register Top. Specific Address register Bottom stores the first four bytes of the destination address and Specific Address register Top contains the last two bytes. The addresses stored can be specific, group, local or universal.

The destination address of received frames is compared against the data stored in the Specific Address registers once they have been activated. The addresses are deactivated at reset or when their corresponding Specific Address register Bottom is written. They are activated when Specific Address register Top is written. If a receive frame address matches an active address, the frame is written to the FIFO interface and on to DMA memory.

Frames may be filtered using the type ID field for matching. Four type ID registers exist in the register address space and each can be enabled for matching by writing a one to the MSB (bit 31) of the respective register. When a frame is received, the matching is implemented as an OR function of the various types of match.

The contents of each type ID register (when enabled) are compared against the length/type ID of the frame being received (e.g., bytes 13 and 14 in non-VLAN and non-SNAP encapsulated frames) and copied to memory if a match is found. The encoded type ID match bits (Word 0, Bit 22 and Bit 23) in the receive buffer descriptor status are set indicating which type ID register generated the match, if the receive checksum offload is disabled.

The reset state of the type ID registers is zero, therefore each is initially disabled.

The following example illustrates the use of the address and type ID match registers for a MAC address of 21:43:65:87:A9:CB:

Preamble	55
SFD	D5
DA (Octet 0 - LSB)	21
DA (Octet 1)	43
DA (Octet 2)	65
DA (Octet 3)	87
DA (Octet 4)	A9
DA (Octet 5 - MSB)	CB
SA (LSB)	00 (see **Note**)
SA	00(see **Note**)
SA	00(see **Note**)

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SA	00(see **Note**)
SA	00(see **Note**)
SA (MSB)	00(see **Note**)
Type ID (MSB)	43
Type ID (LSB)	21

Note: Contains the address of the transmitting device.

The previous sequence shows the beginning of an Ethernet frame. Byte order of transmission is from top to bottom, as shown. For a successful match to specific address 1, the following address matching registers must be set up:

Specific Address 1 Bottom register (SAB1) (Address 0x088) 0x87654321

Specific Address 1 Top register (SAT1) (Address 0x08C) 0x0000CBA9

For a successful match to the type ID, the following Type ID Match 1 register must be set up:

Type ID Match 1 register (TIDM1) (Address 0x0A8) 0x80004321

45.5.8. Broadcast Address

Frames with the broadcast address of 0xFFFFFFFFFFFF are stored to memory only if the 'no broadcast' bit in the Network Configuration register is set to zero.

45.5.9. Hash Addressing

The hash address register is 64 bits long and takes up two locations in the memory map. The least significant bits are stored in Hash Register Bottom and the most significant bits in Hash Register Top.

The unicast hash enable and the multicast hash enable bits in the Network Configuration register enable the reception of hash matched frames. The destination address is reduced to a 6-bit index into the 64-bit Hash register using the following hash function: The hash function is an XOR of every sixth bit of the destination address.

hash_index[05] = da[05] ^ da[11] ^ da[17] ^ da[23] ^ da[29] ^ da[35] ^ da[41] ^ da[47]

hash_index[04] = da[04] ^ da[10] ^ da[16] ^ da[22] ^ da[28] ^ da[34] ^ da[40] ^ da[46]

hash_index[03] = da[03] ^ da[09] ^ da[15] ^ da[21] ^ da[27] ^ da[33] ^ da[39] ^ da[45]

hash_index[02] = da[02] ^ da[08] ^ da[14] ^ da[20] ^ da[26] ^ da[32] ^ da[38] ^ da[44]

hash_index[01] = da[01] ^ da[07] ^ da[13] ^ da[19] ^ da[25] ^ da[31] ^ da[37] ^ da[43]

hash_index[00] = da[00] ^ da[06] ^ da[12] ^ da[18] ^ da[24] ^ da[30] ^ da[36] ^ da[42]

da[0] represents the least significant bit of the first byte received, that is, the multicast/unicast indicator, and da[47] represents the most significant bit of the last byte received.

If the hash index points to a bit that is set in the Hash register then the frame will be matched according to whether the frame is multicast or unicast.

A multicast match will be signaled if the multicast hash enable bit is set, da[0] is logic 1 and the hash index points to a bit set in the Hash register.

A unicast match will be signaled if the unicast hash enable bit is set, da[0] is logic 0 and the hash index points to a bit set in the Hash register.

To receive all multicast frames, the Hash register should be set with all ones and the multicast hash enable bit should be set in the Network Configuration register.

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45.5.10. Copy all Frames (Promiscuous Mode)

If the Copy All Frames bit is set in the Network Configuration register then all frames (except those that are too long, too short, have FCS errors or have RXER asserted during reception) will be copied to memory. Frames with FCS errors will be copied if bit 26 is set in the Network Configuration register.

45.5.11. Disable Copy of Pause Frames

Pause frames can be prevented from being written to memory by setting the disable copying of pause frames control bit 23 in the Network Configuration register. When set, pause frames are not copied to memory regardless of the Copy All Frames bit, whether a hash match is found, a type ID match is identified or if a destination address match is found.

45.5.12. VLAN Support

The following table describes an Ethernet encoded 802.1Q VLAN tag.

Table 45-4. 802.1Q VLAN Tag

TPID (Tag Protocol Identifier) 16 bits	TCI (Tag Control Information) 16 bits
0x8100	First 3 bits priority, then CFI bit, last 12 bits VID

The VLAN tag is inserted at the 13th byte of the frame adding an extra four bytes to the frame. To support these extra four bytes, the ETH can accept frame lengths up to 1536 bytes by setting bit 8 in the Network Configuration register.

If the VID (VLAN identifier) is null (0x000) this indicates a priority-tagged frame.

The following bits in the receive buffer descriptor status word give information about VLAN tagged frames:

- Bit 21 set if receive frame is VLAN tagged (i.e., type ID of 0x8100)
- Bit 20 set if receive frame is priority tagged (i.e., type ID of 0x8100 and null VID) (If bit 20 is set, bit 21 will be set also)
- Bit 19, 18 and 17 set to priority if bit 21 is set
- Bit 16 set to CFI if bit 21 is set

The ETH can be configured to reject all frames except VLAN tagged frames by setting the discard non-VLAN frames bit in the Network Configuration register.

45.5.13. Wake on LAN Support

The receive block supports Wake on LAN by detecting the following events on incoming receive frames:

- Magic packet
- Address Resolution Protocol (ARP) request to the device IP address
- Specific address 1 filter match
- Multicast hash filter match

These events can be individually enabled through bits [19:16] of the Wake on LAN register. Also, for Wake on LAN detection to occur, receive enable must be set in the Network Control register, however a receive buffer does not have to be available.

In case of an ARP request, specific address 1 or multicast filter events will occur even if the frame is errored. For magic packet events, the frame must be correctly formed and error free.

A magic packet event is detected if all of the following are true:

- Magic packet events are enabled through bit 16 of the Wake on LAN register

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- The frame's destination address matches specific address 1
- The frame is correctly formed with no errors
- The frame contains at least 6 bytes of 0xFF for synchronization
- There are 16 repetitions of the contents of Specific Address 1 register immediately following the synchronization

An ARP request event is detected if all of the following are true:

- ARP request events are enabled through bit 17 of the Wake on LAN register
- Broadcasts are allowed by bit 5 in the Network Configuration register
- The frame has a broadcast destination address (bytes 1 to 6)
- The frame has a type ID field of 0x0806 (bytes 13 and 14)
- The frame has an ARP operation field of 0x0001 (bytes 21 and 22)
- The least significant 16 bits of the frame's ARP target protocol address (bytes 41 and 42) match the value programmed in bits[15:0] of the Wake on LAN register

The decoding of the ARP fields adjusts automatically if a VLAN tag is detected within the frame. The reserved value of 0x0000 for the Wake on LAN target address value will not cause an ARP request event, even if matched by the frame.

A specific address 1 filter match event will occur if all of the following are true:

- Specific address 1 events are enabled through bit 18 of the Wake on LAN register
- The frame's destination address matches the value programmed in the Specific Address 1 registers

A multicast filter match event will occur if all of the following are true:

- Multicast hash events are enabled through bit 19 of the Wake on LAN register
- Multicast hash filtering is enabled through bit 6 of the Network Configuration register
- The frame destination address matches against the multicast hash filter
- The frame destination address is not a broadcast

45.5.14. IEEE 1588 Support

IEEE 1588 is a standard for precision time synchronization in local area networks. It works with the exchange of special Precision Time Protocol (PTP) frames. The PTP messages can be transported over IEEE 802.3/Ethernet, over Internet Protocol Version 4 or over Internet Protocol Version 6 as described in the annex of IEEE P1588.D2.1.

The ETH indicates the message time-stamp point (asserted on the start packet delimiter and de-asserted at end of frame) for all frames and the passage of PTP event frames (asserted when a PTP event frame is detected and de-asserted at end of frame).

IEEE 802.1AS is a subset of IEEE 1588. One difference is that IEEE 802.1AS uses the Ethernet multicast address 0180C200000E for sync frame recognition whereas IEEE 1588 does not. ETH is designed to recognize sync frames with both IEEE 802.1AS and IEEE 1588 addresses and so can support both 1588 and 802.1AS frame recognition simultaneously.

Synchronization between host and client clocks is a two stage process.

First, the offset between the host and client clocks is corrected by the host sending a sync frame to the client with a follow up frame containing the exact time the sync frame was sent. Hardware assist modules at the host and client side detect exactly when the sync frame was sent by the host and received by the client. The client then corrects its clock to match the host clock.

Second, the transmission delay between the host and client is corrected. The client sends a delay request frame to the host which sends a delay response frame in reply. Hardware assist modules

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at the host and client side detect exactly when the delay request frame was sent by the client and received by the host. The client will now have enough information to adjust its clock to account for delay. For example, if the client was assuming zero delay, the actual delay will be half the difference between the transmit and receive time of the delay request frame (assuming equal transmit and receive times) because the client clock will be lagging the host clock by the delay time already.

The time-stamp is taken when the message time-stamp point passes the clock time-stamp point. This can generate an interrupt if enabled (IER). However, MAC Filtering configuration is needed to actually 'copy' the message to memory. For Ethernet, the message time-stamp point is the SFD and the clock time-stamp point is the MII interface. (The IEEE 1588 specification refers to sync and delay_req messages as event messages as these require time-stamping. These events are captured in the registers TSSx, EFTx, and EFRx, respectively. Follow up, delay response and management messages do not require time-stamping and are referred to as general messages.)

1588 version 2 defines two additional PTP event messages. These are the peer delay request (Pdelay_Req) and peer delay response (Pdelay_Resp) messages. These events are captured in the registers PEFTx and PEFRx, respectively. These messages are used to calculate the delay on a link. Nodes at both ends of a link send both types of frames (regardless of whether they contain a host or client clock). The Pdelay_Resp message contains the time at which a Pdelay_Req was received and is itself an event message. The time at which a Pdelay_Resp message is received is returned in a Pdelay_Resp_Follow_Up message.

1588 version 2 introduces transparent clocks of which there are two kinds, peer-to-peer (P2P) and end-to-end (E2E). Transparent clocks measure the transit time of event messages through a bridge and amend a correction field within the message to allow for the transit time. P2P transparent clocks additionally correct for the delay in the receive path of the link using the information gathered from the peer delay frames. With P2P transparent clocks delay_req messages are not used to measure link delay. This simplifies the protocol and makes larger systems more stable.

The ETH recognizes four different encapsulations for PTP event messages:

1. 1588 version 1 (UDP/IPv4 multicast)
2. 1588 version 2 (UDP/IPv4 multicast)
3. 1588 version 2 (UDP/IPv6 multicast)
4. 1588 version 2 (Ethernet multicast)

Table 45-5. Example of Sync Frame in 1588 Version 1 Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–32)	E00001
IP DA (Octet 33)	81 or 82 or 83 or 84
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–42)	—
Version PTP (Octet 43)	01
Other stuff (Octets 44–73)	—
Control (Octet 74)	00
Other stuff (Octets 75–168)	—

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Table 45-6. Example of Delay Request Frame in 1588 Version 1 Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–32)	E00001
IP DA (Octet 33)	81 or 82 or 83 or 84
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–42)	—
Version PTP (Octet 43)	01
Other stuff (Octets 44–73)	—
Control (Octet 74)	01
Other stuff (Octets 75–168)	—

For 1588 version 1 messages, sync and delay request frames are indicated by the ETH if the frame type field indicates TCP/IP, UDP protocol is indicated, the destination IP address is 224.0.1.129/130/131 or 132, the destination UDP port is 319 and the control field is correct.

The control field is 0x00 for sync frames and 0x01 for delay request frames.

For 1588 version 2 messages, the type of frame is determined by looking at the message type field in the first byte of the PTP frame. Whether a frame is version 1 or version 2 can be determined by looking at the version PTP field in the second byte of both version 1 and version 2 PTP frames.

In version 2 messages sync frames have a message type value of 0x0, delay_req have 0x1, Pdelay_Req have 0x2 and Pdelay_Resp have 0x3.

Table 45-7. Example of Sync Frame in 1588 Version 2 (UDP/IPv4) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–33)	E0000181
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–41)	—
Message type (Octet 42)	00
Version PTP (Octet 43)	02

Table 45-8. Example of Pdelay_Req Frame in 1588 Version 2 (UDP/IPv4) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5

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Table 45-8. Example of Pdelay_Req Frame in 1588 Version 2 (UDP/IPv4) Format (continued)

Frame Segment	Value
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–33)	E000006B
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–41)	—
Message type (Octet 42)	02
Version PTP (Octet 43)	02

Table 45-9. Example of Sync Frame in 1588 Version 2 (UDP/IPv6) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	86dd
IP stuff (Octets 14–19)	—
UDP (Octet 20)	11
IP stuff (Octets 21–37)	—
IP DA (Octets 38–53)	FF0X00000000018
Source IP port (Octets 54–55)	—
Dest IP port (Octets 56–57)	013F
Other stuff (Octets 58–61)	—
Message type (Octet 62)	00
Other stuff (Octets 63–93)	—
Version PTP (Octet 94)	02

Table 45-10. Example of Pdelay_Resp Frame in 1588 Version 2 (UDP/IPv6) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	86dd
IP stuff (Octets 14–19)	—
UDP (Octet 20)	11
IP stuff (Octets 21–37)	—
IP DA (Octets 38–53)	FF0200000000006B
Source IP port (Octets 54–55)	—
Dest IP port (Octets 56–57)	013F
Other stuff (Octets 58–61)	—
Message type (Octet 62)	03
Other stuff (Octets 63–93)	—
Version PTP (Octet 94)	02

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For the multicast address 011B19000000 sync and delay request frames are recognized depending on the message type field, 00 for sync and 01 for delay request.

Table 45-11. Example of Sync Frame in 1588 Version 2 (Ethernet Multicast) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	011B19000000
SA (Octets 6–11)	—
Type (Octets 12–13)	88F7
Message type (Octet 14)	00
Version PTP (Octet 15)	02

Pdelay request frames need a special multicast address so they can pass through ports blocked by the spanning tree protocol. For the multicast address 0180C200000E sync, Pdelay_Req and Pdelay_Resp frames are recognized depending on the message type field, 00 for sync, 02 for pdelay request and 03 for pdelay response.

Table 45-12. Example of Pdelay_Req Frame in 1588 Version 2 (Ethernet Multicast) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	0180C200000E
SA (Octets 6–11)	—
Type (Octets 12–13)	88F7
Message type (Octet 14)	00
Version PTP (Octet 15)	02

45.5.15. Time Stamp Unit

Overview

The TSU consists of a timer and registers to capture the time at which PTP event frames cross the message timestamp point. An interrupt is issued when a capture register is updated.

The 1588 time stamp unit (TSU) is implemented as a 94-bit timer.

- The 48 upper bits [93:46] of the timer count seconds and are accessible in the ETH 1588 Timer Seconds High Register" (TSH) and ETH 1588 Timer Seconds Low Register (TSL)
- The 30 lower bits [45:16] of the timer count nanoseconds and are accessible in the ETH 1588 Timer Nanoseconds Register (TN)
- The lowest 16 bits [15:0] of the timer count sub-nanoseconds

The 46 lower bits roll over when they have counted to 1s. An interrupt is generated when the seconds increment. The timer increments by a programmable period (to approximately 15.2fs resolution) with each MCK period. The timer value can be read, written and adjusted with 1ns resolution (incremented or decremented) through the APB interface.

Timer Adjustment

The amount by which the timer increments each clock cycle is controlled by the Timer Increment register (TI). Bits [7:0] are the default increment value in nanoseconds. Additional 16 bits of sub-nanosecond resolution are available using the Timer Increment Sub-Nanoseconds register (TISUBN). If the rest of the register is written with zero, the timer increments by the value in [7:0], plus the value of the TISUBN for each clock cycle.

The TISUBN allows a resolution of approximately 15fs.

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Bits [15:8] of the increment register are the alternative increment value in nanoseconds, and bits [23:16] are the number of increments after which the alternative increment value is used. If [23:16] are zero the alternative increment value will never be used.

> Taking the example of 10.2MHz, there are 102 cycles every 10µs or 51 cycles every 5µs. So a timer with a 10.2MHz clock source is constructed by incrementing by 98ns for fifty cycles and then incrementing by 100ns (98ns × 50 + 100ns = 5000ns). This is programmed by writing the value 0x00326462 to the Timer Increment register (TI).

> In a second example, a 49.8 MHz clock source requires 20ns for 248 cycles, followed by an increment of 40ns (20ns × 248 + 40ns = 5000ns). This is programmed by writing the value 0x00F82814 to the TI register.

The Number of Increments bit field in the TI register is 8 bit in size, so frequencies up to 50 MHz are supported with 200 kHz resolution.

Without the alternative increment field the period of the clock would be limited to an integer number of nanoseconds, resulting in supported clock frequencies of 8, 10, 20, 25, 40, 50, 100, 125, 200 and 250 MHz.

There are eight additional 80-bit registers that capture the time at which PTP event frames are transmitted and received. An interrupt is issued when these registers are updated. The TSU timer count value can be compared to a programmable comparison value. For the comparison, the 48 bits of the seconds value and the upper 22 bits of the nanoseconds value are used. A signal (TSUCOMP) is output from the core to indicate when the TSU timer count value is equal to the comparison value stored in the TSU timer comparison value registers (NSC, SCL, and SCH). An interrupt can also be generated (if enabled) when the TSU timer count value and comparison value are equal, mapped to bit 29 of the interrupt status register.

45.5.16. MAC 802.3 Pause Frame Support

Note: Refer to the Clause 31, and Annex 31A and 31B of the IEEE standard 802.3 for a full description of MAC 802.3 pause operation.

The following table shows the start of a MAC 802.3 pause frame.

Table 45-13. Start of an 802.3 Pause Frame

Address		Type (MAC Control Frame)	Pause	
Destination	Source		Opcode	Time
0x0180C2000001	6 bytes	0x8808	0x0001	2 bytes

The ETH supports both hardware controlled pause of the transmitter, upon reception of a pause frame, and hardware generated pause frame transmission.

45.5.16.1. 802.3 Pause Frame Reception

Bit 13 of the Network Configuration register is the pause enable control for reception. If this bit is set, transmission will pause if a non zero pause quantum frame is received.

If a valid pause frame is received then the Pause Time register is updated with the new frame's pause time, regardless of whether a previous pause frame is active or not. An interrupt (either bit 12 or bit 13 of the Interrupt Status register) is triggered when a pause frame is received, but only if the interrupt has been enabled (bit 12 and bit 13 of the Interrupt Mask register). Pause frames received with non zero quantum are indicated through the interrupt bit 12 of the Interrupt Status register. Pause frames received with zero quantum are indicated on bit 13 of the Interrupt Status register.

Once the Pause Time register is loaded and the frame currently being transmitted has been sent, no new frames are transmitted until the pause time reaches zero. The loading of a new pause time, and therefore the pausing of transmission, only occurs when the ETH is configured for full duplex

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operation. If the ETH is configured for half duplex there will be no transmission pause, but the pause frame received interrupt will still be triggered. A valid pause frame is defined as having a destination address that matches either the address stored in Specific Address register 1 or if it matches the reserved address of 0x0180C2000001. It must also have the MAC control frame type ID of 0x8808 and have the pause opcode of 0x0001.

Pause frames that have frame check sequence (FCS) or other errors will be treated as invalid and will be discarded. 802.3 Pause frames that are received after Priority-based Flow Control (PFC) has been negotiated will also be discarded. Valid pause frames received will increment the pause frames received statistic register.

The pause time register decrements every 512 bit times once transmission has stopped. For test purposes, the retry test bit can be set (bit 12 in the Network Configuration register) which causes the Pause Time register to decrement every TXCK cycle once transmission has stopped.

The interrupt (bit 13 in the Interrupt Status register) is asserted whenever the Pause Time register decrements to zero (assuming it has been enabled by bit 13 in the Interrupt Mask register). This interrupt is also set when a zero quantum pause frame is received.

45.5.16.2. 802.3 Pause Frame Transmission

Automatic transmission of pause frames is supported through the transmit pause frame bits of the Network Control register. If either bit 11 (NCR.TXPF) or bit 12 (NCR.TXZQPF) of the Network Control register is written with logic 1, an 802.3 pause frame will be transmitted, providing full duplex is selected in the Network Configuration register and the transmit block is enabled in the Network Control register.

Pause frame transmission will happen immediately if transmit is inactive or if transmit is active between the current frame and the next frame due to be transmitted.

Transmitted pause frames comprise the following:

- A destination address of 01-80-C2-00-00-01
- A source address taken from Specific Address register 1
- A type ID of 88-08 (MAC control frame)
- A pause opcode of 00-01
- A pause quantum register
- Fill of 00 to take the frame to minimum frame length
- Valid FCS

The pause quantum used in the generated frame will depend on the trigger source for the frame as follows:

- If bit 11 (NCR.TXPF) is written with a '1', the pause quantum will be taken from the Transmit Pause Quantum register. The Transmit Pause Quantum register resets to a value of 0xFFFF giving maximum pause quantum as default.
- If bit 12 (NCR.TXZQPF) is written with a '1', the pause quantum will be zero.

After transmission, a pause frame transmitted interrupt will be generated (bit 14 (ISR.PFTR) of the Interrupt Status register) and the only statistics register that will be incremented will be the Pause Frames Transmitted register.

Pause frames can also be transmitted by the MAC using normal frame transmission methods.

45.5.17. MAC PFC Priority-based Pause Frame Support

Note: Refer to the 802.1Qbb standard for a full description of priority-based pause operation.

The following table shows the start of a Priority-based Flow Control (PFC) pause frame.

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Table 45-14. Start of a PFC Pause Frame

Address		Type (Mac Control Frame)	Pause Opcode	Priority Enable Vector	Pause Time
Destination	Source				
0x0180C2000001	6 bytes	0x8808	0x1001	2 bytes	8 × 2 bytes

The ETH supports PFC priority-based pause transmission and reception. Before PFC pause frames can be received, bit 16 of the Network Control register must be set (NCR.ENPBPR =1).

45.5.17.1. PFC Pause Frame Reception

The ability to receive and decode priority-based pause frames is enabled by setting bit 16 (NCR.ENPBPR) of the Network Control register. When this bit is set, the ETH will match either classic 802.3 pause frames or PFC priority-based pause frames. Once a priority-based pause frame has been received and matched, then from that moment on the ETH will only match on priority-based pause frames (this is an 802.1Qbb requirement, known as PFC negotiation). Once priority-based pause has been negotiated, any received 802.3x format pause frames will not be acted upon.

If a valid priority-based pause frame is received then the ETH will decode the frame and determine which, if any, of the eight priorities require to be paused. Up to eight Pause Time registers are then updated with the eight pause times extracted from the frame regardless of whether a previous pause operation is active or not. An interrupt (either bit 12 or bit 13 of the Interrupt Status register) is triggered when a pause frame is received, but only if the interrupt has been enabled (bit 12 and bit 13 of the Interrupt Mask register). Pause frames received with non zero quantum are indicated through the interrupt bit 12 of the Interrupt Status register. Pause frames received with zero quantum are indicated on bit 13 of the Interrupt Status register. The loading of a new pause time only occurs when the ETH is configured for full duplex operation. If the ETH is configured for half duplex, the pause time counters will not be loaded, but the pause frame received interrupt will still be triggered. A valid pause frame is defined as having a destination address that matches either the address stored in Specific Address register 1 or if it matches the reserved address of 0x0180C2000001. It must also have the MAC control frame type ID of 0x8808 and have the pause opcode of 0x0101.

Pause frames that have frame check sequence (FCS) or other errors will be treated as invalid and will be discarded. Valid pause frames received will increment the Pause Frames Received Statistic register.

The Pause Time registers decrement every 512 bit times immediately following the PFC frame reception. For test purposes, the retry test bit can be set (bit 12 in the Network Configuration register) which causes the Pause Time register to decrement every RXCK cycle once transmission has stopped.

The interrupt (bit 13 in the Interrupt Status register) is asserted whenever the Pause Time register decrements to zero (assuming it has been enabled by bit 13 in the Interrupt Mask register). This interrupt is also set when a zero quantum pause frame is received.

45.5.18. Energy Efficient Ethernet Support

Features

- Energy Efficient Ethernet according to IEEE 802.3az
- A system's transmit path can enter a low power mode if there is nothing to transmit.
- A PHY can detect whether its link partner's transmit path is in low power mode, and configure its own receive path to enter low power mode.
- Link remains up during lower power mode and no frames are dropped.
- Asymmetric, one direction can be in low power mode while the other is transmitting normally.
- LPI (Low Power Idle) signaling is used to control entry and exit to and from low power modes.
  Note: LPI signaling can only take place if both sides have indicated support for it through auto-negotiation.

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Operation

- Low power control is done at the RMII (reconciliation sublayer).
- As an architectural convenience in writing the 802.3az it is assumed that transmission is deferred by asserting carrier sense - in practice it will not be done this way. This system will know when it has nothing to transmit and only enter low power mode when it is not transmitting.
- LPI should not be requested unless the link has been up for at least one second.
- LPI is signaled on the RMII transmit path by asserting 0x01 on TXD with TX_EN low and TX_ER high.
- A PHY on seeing LPI requested on the RMII will send the sleep signal before going quiet. After going quiet it will periodically emit refresh signals.
- The sleep, quiet and refresh periods are defined in 802.3az, Table 78-2.
- LPI mode ends by transmitting normal idle for the wake time. There is a default time for this but it can be adjusted in software using the Link Layer Discovery Protocol (LLDP) described in 802.3az, Clause 79.
- LPI is indicated at the receive side when sleep and refresh signaling has been detected.

45.5.19. LPI Operation in the EMAC

It is best to use firmware to control LPI. LPI operation happens at the system level. Firmware gives maximum control and flexibility of operation. LPI operation is straightforward and firmware should be capable of responding within the required timeframes.

Autonegotiation:

1. Indicate EEE capability using next page autonegotiation.

For the transmit path:

1. If the link has been up for 1 second and there is nothing being transmitted, write to the TXLPIEN bit in the Network Control register.
2. Wake up by clearing the TXLPIEN bit in the Network Control register.

For the receive path:

1. Enable RXLPISBC bit in IER. The bit RXLPIS is set in Network Status Register triggering an interrupt.
2. Wait for an interrupt to indicate that LPI has been received.
3. Disable relevant parts of the receive path if desired.
4. The RXLPIS bit in Network Status Register gets cleared to indicate that regular idle has been received. This triggers an interrupt.
5. Re-enable the receive path.

45.5.20. PHY Interface

The Ethernet MAC supports RMII PHY interface. The RMII interface is provided for 10/100 operation and uses TXD[1:0] and RXD[1:0].

45.5.21. Jumbo Frames

The jumbo frames enable bit in the Network Configuration register allows the ETH, in its default configuration, to receive jumbo frames up to 3840 bytes in size. This operation does not form part of the IEEE 802.3 specification and is normally disabled. When jumbo frames are enabled, frames received with a frame size greater than 3840 bytes are discarded.

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45.6. Programming Interface

45.6.1. Initialization

45.6.1.1. Configuration

Initialization of the ETH configuration (i.e., loop back mode, frequency ratios) must be done while the transmit and receive circuits are disabled. See the description of the Network Control register and Network Configuration register earlier in this document.

To change loop back mode, the following sequence of operations must be followed:

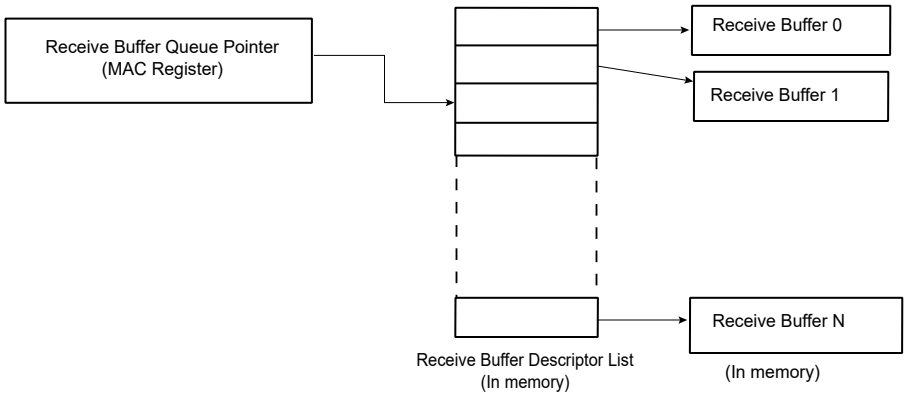
1. Write to Network Control register to disable transmit and receive circuits.
2. Write to Network Control register to change loop back mode.
3. Write to Network Control register to re-enable transmit or receive circuits.
   Note: These writes to the Network Control register cannot be combined in any way.

45.6.1.2. Receive Buffer List

Receive data is written to areas of data (i.e., buffers) in system memory. These buffers are listed in another data structure that also resides in main memory. This data structure (receive buffer queue) is a sequence of descriptor entries as defined in the table “Receive Buffer Description Entry”.

The Receive Buffer Queue Pointer register points to this data structure.

Figure 45-3. Receive Buffer List



To create the list of buffers:

1. Allocate a number (N) of buffers of X bytes in system memory, where X is the DMA buffer length programmed in the DMA Configuration register.
2. Allocate an area 8N (16N if Timestamp is included) bytes for the receive buffer descriptor list in system memory and create N entries in this list. Mark all entries in this list as owned by ETH, i.e., bit 0 of word 0 set to 0.
3. Mark the last descriptor in the queue with the wrap bit (bit 1 in word 0 set to 1).
4. Write address of receive buffer descriptor list and control information to ETH register receive buffer queue pointer
5. The receive circuits can then be enabled by writing to the address recognition registers and the Network Control register.

Note: The queue pointers must be initialized and point to USED descriptors for all queues including those not intended for use.

45.6.1.3. Transmit Buffer List

Transmit data is read from areas of data (the buffers) in system memory. These buffers are listed in another data structure that also resides in main memory. This data structure (Transmit Buffer

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Queue) is a sequence of descriptor entries as defined in the table “Transmit Buffer Description Entry”.

The Transmit Buffer Queue Pointer register points to this data structure.

To create this list of buffers:

1. Allocate a number (N) of buffers of between 1 and 10240 bytes of data to be transmitted in system memory which is up to 32768 bytes. Up to 128 buffers per frame are allowed.
2. Allocate an area 8N (16N if Timestamp is included) bytes for the transmit buffer descriptor list in system memory and create N entries in this list. Mark all entries in this list as owned by ETH, i.e., bit 31 of word 1 set to 0.
3. Mark the last descriptor in the queue with the wrap bit (bit 30 in word 1 set to 1).
4. Write address of transmit buffer descriptor list and control information to ETH register transmit buffer queue pointer.
5. The transmit circuits can then be enabled by writing to the Network Control register.

Note: The queue pointers must be initialized and point to USED descriptors for all queues including those not intended for use.

45.6.1.4. Address Matching

The ETH Hash register pair and the four Specific Address register pairs must be written with the required values. Each register pair comprises of a bottom register and top register, with the bottom register being written first. The address matching is disabled for a particular register pair after the bottom register has been written and re-enabled when the top register is written. Each register pair may be written at any time, regardless of whether the receive circuits are enabled or disabled.

As an example, to set Specific Address register 1 to recognize destination address 21:43:65:87:A9:CB, the following values are written to Specific Address register 1 bottom and Specific Address register 1 top:

- Specific Address register 1 bottom bits 31:0 (0x98): 0x8765_4321
- Specific Address register 1 top bits 31:0 (0x9C): 0x0000_CBA9

45.6.1.5. PHY Maintenance

The PHY Maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit two is set in the Network Status register (about 2000 MCK cycles later when bits 18:16 are set to 010 in the Network Configuration register). An interrupt is generated as this bit is set.

During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each Management Data Clock (MDC) cycle. This causes the transmission of a PHY management frame on MDIO. See section 22.2.4.5 of the IEEE 802.3 standard.

Reading during the shift operation will return the current contents of the shift register. At the end of the management operation the bits will have shifted back to their original locations. For a read operation the data bits are updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced.

The Management Data Clock (MDC) should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3 standard. MDC is generated by dividing down MCK. Three bits in the Network Configuration register determine by how much MCK should be divided to produce MDC.

45.6.1.6. Interrupts

There are multiple interrupt conditions that are detected within the ETH. The conditions are ORed to make multiple interrupts. Each queue has its own interrupt vector. There are 6 interrupt lines connected to the NVIC correspondence to each queue. On receipt of the interrupt signal, the CPU

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enters the interrupt handler. Refer to the NVIC chapter to find more information about ETH Queue Interrupts.

At reset all interrupts are disabled. To enable an interrupt, write to Interrupt Enable register with the pertinent interrupt bit set to 1. To disable an interrupt, write to Interrupt Disable register with the pertinent interrupt bit set to 1. To check whether an interrupt is enabled or disabled, read Interrupt Mask register. If the bit is set to 1, the interrupt is disabled.

45.6.1.7. Transmitting Frames

The procedure to set up a frame for transmission is the following:

1. Enable transmit in the Network Control register.
2. Allocate an area of system memory for transmit data. This does not have to be contiguous, varying byte lengths can be used if they conclude on byte borders.
3. Set-up the transmit buffer list by writing buffer addresses to word zero of the transmit buffer descriptor entries and control and length to word one.
4. Write data for transmission into the buffers pointed to by the descriptors.
5. Write the address of the first buffer descriptor to transmit buffer descriptor queue pointer.
6. Enable appropriate interrupts.
7. Write to the transmit start bit (TSTART) in the Network Control register.

45.6.1.8. Receiving Frames

When a frame is received and the receive circuits are enabled, the ETH checks the address and, in the following cases, the frame is written to system memory:

- If it matches one of the four Specific Address registers
- If it matches one of the four type ID registers
- If it matches the hash address function
- If it is a broadcast address (0xFFFFFFFFFFFF) and broadcasts are allowed
- If the ETH is configured to “copy all frames”

The register receive buffer queue pointer points to the next entry in the receive buffer descriptor list and the ETH uses this as the address in system memory to write the frame to.

Once the frame has been completely and successfully received and written to system memory, the ETH then updates the receive buffer descriptor entry (see Receive Buffer Description Entry) with the reason for the address match and marks the area as being owned by software. Once this is complete, a receive complete interrupt is set. Software is then responsible for copying the data to the application area and releasing the buffer (by writing the ownership bit back to 0).

If the ETH is unable to write the data at a rate to match the incoming frame, then a receive overrun interrupt is set. If there is no receive buffer available, i.e., the next buffer is still owned by software, a receive buffer not available interrupt is set. If the frame is not successfully received, a statistics register is incremented and the frame is discarded without informing software.

45.6.2. Statistics Registers

Statistics registers are described in the user interface beginning with ETH Octets Transmitted Low Register and ending with ETH UDP Checksum Errors Register.

The statistics register block begins at 0x1100 and runs to 0x11B0, and comprises the registers listed below.

Octets Transmitted Low Register	Broadcast Frames Received Register
Octets Transmitted High Register	Multicast Frames Received Register
Frames Transmitted Register	Pause Frames Received Register

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Broadcast Frames Transmitted Register	64 Byte Frames Received Register
Multicast Frames Transmitted Register	65 to 127 Byte Frames Received Register
Pause Frames Transmitted Register	128 to 255 Byte Frames Received Register
64 Byte Frames Transmitted Register	256 to 511 Byte Frames Received Register
65 to 127 Byte Frames Transmitted Register	512 to 1023 Byte Frames Received Register
128 to 255 Byte Frames Transmitted Register	1024 to 1518 Byte Frames Received Register
256 to 511 Byte Frames Transmitted Register	1519 to Maximum Byte Frames Received Register
512 to 1023 Byte Frames Transmitted Register	Undersize Frames Received Register
1024 to 1518 Byte Frames Transmitted Register	Oversize Frames Received Register
Greater Than 1518 Byte Frames Transmitted Register	Jabbers Received Register
Transmit Underruns Register	Frame Check Sequence Errors Register
Single Collision Frames Register	Length Field Frame Errors Register
Multiple Collision Frames Register	Receive Symbol Errors Register
Excessive Collisions Register	Alignment Errors Register
Late Collisions Register	Receive Resource Errors Register
Deferred Transmission Frames Register	Receive Overrun Register
Carrier Sense Errors Register	IP Header Checksum Errors Register
Octets Received Low Register	TCP Checksum Errors Register
Octets Received High Register	UDP Checksum Errors Register
Frames Received Register	

These registers reset to zero on a read and stick at all ones when they count to their maximum value. They should be read frequently enough to prevent loss of data.

The receive statistics registers are only incremented when the receive enable bit (RXEN) is set in the Network Control register.

Once a statistics register has been read, it is automatically cleared. When reading the Octets Transmitted and Octets Received registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

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45.7. Register Summary

For descriptions and definitions of both Register and bitfield properties, refer to **[Required-Cleanup]:** .

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0		RUNSTDBY					ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x04	CTRLB	7:0	TSUINC[1:0]		TSUMS			TSUCLKREQ		
		15:8								
		23:16								
		31:24								
0x08 ... 0x0B	Reserved									
0x0C	EVCTRL	7:0								CMPEO
		15:8								
		23:16								
		31:24								
0x10 ... 0x1F	Reserved									
0x20	SYNCB	7:0							ENABLE	
		15:8								
		23:16								
		31:24								
0x24 ... 0x0FFF	Reserved									
0x1000	NCR	7:0	WESTAT	INCSTAT	CLRSTAT	MPE	TXEN	RXEN	LBL	
		15:8	SRTSM			TXZQPF	TXPF	THALT	TSTART	BP
		23:16					LPI	FNP	TXPBPF	ENPBPR
		31:24								
0x1004	NCFGR	7:0	UNIHEN	MTIHEN	NBC	CAF	JFRAME	DNVLAN	FD	SPD
		15:8	RXBUFO[1:0]		PEN	RTY				MAXFS
		23:16	DCPF	DBW[1:0]		CLK[2:0]			RFCS	LFERD
		31:24		IRXER	RXBP	IPGSEN		IRXFCS	EFRHD	RXCOEN
0x1008	NSR	7:0						IDLE	MDIO	
		15:8								
		23:16								
		31:24								
0x100C	UR	7:0								MII
		15:8								
		23:16								
		31:24								
0x1010	DCFGR	7:0	ESPA	ESMA		FBLDO[4:0]				
		15:8					TXCOEN	TXPBMS	RXBMS[1:0]	
		23:16	DRBS[7:0]							
		31:24								DDRP
0x1014	TSR	7:0		UND	TXCOMP	TFC	TXGO	RLE	COL	UBR
		15:8								HRESP
		23:16								
		31:24								
0x1018	RBQB	7:0	ADDR[5:0]							
		15:8	ADDR[13:6]							
		23:16	ADDR[21:14]							
		31:24	ADDR[29:22]							
0x101C	TBQB	7:0	ADDR[5:0]							
		15:8	ADDR[13:6]							
		23:16	ADDR[21:14]							
		31:24	ADDR[29:22]							

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x101C	TBFT127	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x1020	RSR	7:0					HNO	RXOVR	REC	BNA
		15:8								
		23:16								
		31:24								
0x1024	ISR	7:0	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
		15:8		PFTR	PTZ	PFNZ	HRESP	ROVR		
		23:16	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
		31:24			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
0x1028	IER	7:0	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
		15:8	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
		23:16	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
		31:24			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
0x102C	IDR	7:0	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
		15:8	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
		23:16	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
		31:24			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
0x1030	IMR	7:0	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
		15:8	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
		23:16	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
		31:24			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
0x1034	MAN	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	PHYA[0]	REGA[4:0]					WTN[1:0]	
		31:24	WZO	CLTTO	OP[1:0]		PHYA[4:1]			
0x1038	RPQ	7:0	RPQ[7:0]							
		15:8	RPQ[15:8]							
		23:16								
		31:24								
0x103C	TPQ	7:0	TPQ[7:0]							
		15:8	TPQ[15:8]							
		23:16								
		31:24								
0x1040	TPSF	7:0	TPB1ADR[7:0]							
		15:8					TPB1ADR[11:8]			
		23:16								
		31:24	ENTXP							
0x1044	RPSF	7:0	RPB1ADR[7:0]							
		15:8					RPB1ADR[11:8]			
		23:16								
		31:24	ENRXP							
0x1048	RJFML	7:0	FML[7:0]							
		15:8			FML[13:8]					
		23:16								
		31:24								
0x104C ... 0x107F	Reserved									
0x1080	HRB	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x1084	HRT	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1088	SAB1	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x108C ... 0x108F	Reserved									
0x1090	SAB2	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x1094 ... 0x1097	Reserved									
0x1098	SAB3	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x109C ... 0x109F	Reserved									
0x10A0	SAB4	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x10A4 ... 0x10A7	Reserved									
0x10A8	SAB5	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x10A8	TIDM1	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0x10AC	TIDM2	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0x10B0	TIDM3	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0x10B4	TIDM4	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0x10B8	WOL	7:0	IP[7:0]							
		15:8	IP[15:8]							
		23:16					MTI	SA1	ARP	MAG
		31:24								
0x10BC	IPGS	7:0	FL[7:0]							
		15:8	FL[15:8]							
		23:16								
		31:24								
0x10C0	SVLAN	7:0	VLAN_TYPE[7:0]							
		15:8	VLAN_TYPE[15:8]							
		23:16								
		31:24	ESVLAN							

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x10C4	TPFCP	7:0	PEV[7:0]							
		15:8	PQ[7:0]							
		23:16								
		31:24								
0x10C8	SAMB1	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x10CC	SAMT1	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16								
		31:24								
0x10D0 ... 0x10DB	Reserved									
0x10DC	NSC	7:0	NANOSEC[7:0]							
		15:8	NANOSEC[15:8]							
		23:16			NANOSEC[21:16]					
		31:24								
0x10E0	SCL	7:0	SEC[7:0]							
		15:8	SEC[15:8]							
		23:16	SEC[23:16]							
		31:24	SEC[31:24]							
0x10E4	SCH	7:0	SEC[7:0]							
		15:8	SEC[15:8]							
		23:16								
		31:24								
0x10E8	EFTSH	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16								
		31:24								
0x10EC	EFRSH	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16								
		31:24								
0x10F0	PEFTSH	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16								
		31:24								
0x10F4	PEFRSH	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16								
		31:24								
0x10F8 ... 0x10FF	Reserved									
0x1100	OTLO	7:0	TXO[7:0]							
		15:8	TXO[15:8]							
		23:16	TXO[23:16]							
		31:24	TXO[31:24]							
0x1104	OTHI	7:0	TXO[7:0]							
		15:8	TXO[15:8]							
		23:16								
		31:24								
0x1108	FT	7:0	FTX[7:0]							
		15:8	FTX[15:8]							
		23:16	FTX[23:16]							
		31:24	FTX[31:24]							

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x110C	BCFT	7:0	BFTX[7:0]							
		15:8	BFTX[15:8]							
		23:16	BFTX[23:16]							
		31:24	BFTX[31:24]							
0x1110	MFT	7:0	MFTX[7:0]							
		15:8	MFTX[15:8]							
		23:16	MFTX[23:16]							
		31:24	MFTX[31:24]							
0x1114	PFT	7:0	PFTX[7:0]							
		15:8	PFTX[15:8]							
		23:16								
		31:24								
0x1118	BFT64	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x111C ... 0x111F	Reserved									
0x1120	TBFT255	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x1124	TBFT511	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x1128	TBFT1023	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x112C	TBFT1518	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x1130	GTBFT1518	7:0	NFTX[7:0]							
		15:8	NFTX[15:8]							
		23:16	NFTX[23:16]							
		31:24	NFTX[31:24]							
0x1134	TUR	7:0	TXUNR[7:0]							
		15:8							TXUNR[9:8]	
		23:16								
		31:24								
0x1138	SCF	7:0	SCOL[7:0]							
		15:8	SCOL[15:8]							
		23:16							SCOL[17:16]	
		31:24								
0x113C	MCF	7:0	MCOL[7:0]							
		15:8	MCOL[15:8]							
		23:16							MCOL[17:16]	
		31:24								
0x1140	EC	7:0	XCOL[7:0]							
		15:8							XCOL[9:8]	
		23:16								
		31:24								
0x1144	LC	7:0	LCOL[7:0]							
		15:8							LCOL[9:8]	
		23:16								
		31:24								

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1148	DTF	7:0	DEFT[7:0]							
		15:8	DEFT[15:8]							
		23:16							DEFT[17:16]	
		31:24								
0x114C	CSE	7:0	CSR[7:0]							
		15:8							CSR[9:8]	
		23:16								
		31:24								
0x1150	ORLO	7:0	RXO[7:0]							
		15:8	RXO[15:8]							
		23:16	RXO[23:16]							
		31:24	RXO[31:24]							
0x1154	ORHI	7:0	RXO[7:0]							
		15:8	RXO[15:8]							
		23:16								
		31:24								
0x1158	FR	7:0	FRX[7:0]							
		15:8	FRX[15:8]							
		23:16	FRX[23:16]							
		31:24	FRX[31:24]							
0x115C	BCFR	7:0	BFRX[7:0]							
		15:8	BFRX[15:8]							
		23:16	BFRX[23:16]							
		31:24	BFRX[31:24]							
0x1160	MFR	7:0	MFRX[7:0]							
		15:8	MFRX[15:8]							
		23:16	MFRX[23:16]							
		31:24	MFRX[31:24]							
0x1164	PFR	7:0	PFRX[7:0]							
		15:8	PFRX[15:8]							
		23:16								
		31:24								
0x1168	BFR64	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x116C	TBFR127	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x1170	TBFR255	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x1174	TBFR511	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x1178	TBFR1023	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x117C	TBFR1518	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							
0x1180	TMXBFR	7:0	NFRX[7:0]							
		15:8	NFRX[15:8]							
		23:16	NFRX[23:16]							
		31:24	NFRX[31:24]							

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1184	UFR	7:0	UFRX[7:0]							
		15:8							UFRX[9:8]	
		23:16								
		31:24								
0x1188	OFR	7:0	OFRX[7:0]							
		15:8							OFRX[9:8]	
		23:16								
		31:24								
0x118C	JR	7:0	JRX[7:0]							
		15:8							JRX[9:8]	
		23:16								
		31:24								
0x1190	FCSE	7:0	FCKR[7:0]							
		15:8							FCKR[9:8]	
		23:16								
		31:24								
0x1194	LFFE	7:0	LFER[7:0]							
		15:8							LFER[9:8]	
		23:16								
		31:24								
0x1198	RSE	7:0	RXSE[7:0]							
		15:8							RXSE[9:8]	
		23:16								
		31:24								
0x119C	AE	7:0	AER[7:0]							
		15:8							AER[9:8]	
		23:16								
		31:24								
0x11A0	RRE	7:0	RXRER[7:0]							
		15:8	RXRER[15:8]							
		23:16							RXRER[17:16]	
		31:24								
0x11A4	ROE	7:0	RXOVR[7:0]							
		15:8							RXOVR[9:8]	
		23:16								
		31:24								
0x11A8	IHCE	7:0	HCKER[7:0]							
		15:8								
		23:16								
		31:24								
0x11AC	TCE	7:0	TCKER[7:0]							
		15:8								
		23:16								
		31:24								
0x11B0	UCE	7:0	UCKER[7:0]							
		15:8								
		23:16								
		31:24								
0x11B4 ... 0x11BB	Reserved									
0x11BC	TISUBN	7:0	LSBTIR[7:0]							
		15:8	LSBTIR[15:8]							
		23:16								
		31:24								
0x11C0	TSH	7:0	TCS[7:0]							
		15:8	TCS[15:8]							
		23:16								
		31:24								

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x11C4 ... 0x11C7	Reserved									
0x11C8	TSSSL	7:0	VTS[7:0]							
		15:8	VTS[15:8]							
		23:16	VTS[23:16]							
		31:24	VTS[31:24]							
0x11CC	TSSSN	7:0	VTN[7:0]							
		15:8	VTN[15:8]							
		23:16	VTN[23:16]							
		31:24	VTN[31:24]							
0x11D0	TSL	7:0	TCS[7:0]							
		15:8	TCS[15:8]							
		23:16	TCS[23:16]							
		31:24	TCS[31:24]							
0x11D4	TN	7:0	TNS[7:0]							
		15:8	TNS[15:8]							
		23:16	TNS[23:16]							
		31:24			TNS[29:24]					
0x11D8	TA	7:0	ITDT[7:0]							
		15:8	ITDT[15:8]							
		23:16	ITDT[23:16]							
		31:24	ADJ		ITDT[29:24]					
0x11DC	TI	7:0	CNS[7:0]							
		15:8	ACNS[7:0]							
		23:16	NIT[7:0]							
		31:24								
0x11E0	EFTSL	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24	RUD[31:24]							
0x11E4	EFTN	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24			RUD[29:24]					
0x11E8	EFRSL	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24	RUD[31:24]							
0x11EC	EFRN	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24			RUD[29:24]					
0x11F0	PEFTSL	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24	RUD[31:24]							
0x11F4	PEFTN	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24			RUD[29:24]					
0x11F8	PEFRSL	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24	RUD[31:24]							
0x11FC	PEFRN	7:0	RUD[7:0]							
		15:8	RUD[15:8]							
		23:16	RUD[23:16]							
		31:24			RUD[29:24]					

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x1200 ... 0x126F	Reserved									
0x1270	RLPITR	7:0				RLPITR[7:0]				
		15:8				RLPITR[15:8]				
		23:16								
		31:24								
0x1274	RLPITI	7:0				RLPITI[7:0]				
		15:8				RLPITI[15:8]				
		23:16				RLPITI[23:16]				
		31:24								
0x1278	TLPITR	7:0				TLPITR[7:0]				
		15:8				TLPITR[15:8]				
		23:16				TLPITR[23:16]				
		31:24								
0x127C	TLPITI	7:0				TLPITI[7:0]				
		15:8				TLPITI[15:8]				
		23:16				TLPITI[23:16]				
		31:24								
0x1280 ... 0x01008B	Reserved									
0x01008C	SAT1	7:0				ADDR[7:0]				
		15:8				ADDR[15:8]				
		23:16								
		31:24								
0x010090 ... 0x010093	Reserved									
0x010094	SAT2	7:0				ADDR[7:0]				
		15:8				ADDR[15:8]				
		23:16								
		31:24								
0x010098 ... 0x01009B	Reserved									
0x01009C	SAT3	7:0				ADDR[7:0]				
		15:8				ADDR[15:8]				
		23:16								
		31:24								
0x0100A0 ... 0x0100A3	Reserved									
0x0100A4	SAT4	7:0				ADDR[7:0]				
		15:8				ADDR[15:8]				
		23:16								
		31:24								
0x0100A8 ... 0x0100AB	Reserved									
0x0100AC	SAT5	7:0				ADDR[7:0]				
		15:8				ADDR[15:8]				
		23:16								
		31:24								

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45.7.1. ETH Control A Register

Name: CTRLA
Offset: 0x0000
Reset: 0x00000000
Property: PAC Write Protected

Table 45-15. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access		R/W					R/W	R/S/HC
Reset		0					0	0

Bit 6 – RUNSTDBY Run in Standby
This bit is used to keep the ETH running in standby mode.

Value	Description
0	The ETH module is disabled in Standby Sleep mode, clock requests are de-asserted after any pending bus transactions or requests are complete.
1	The ETH module continues to run in Standby Sleep mode.

Bit 1 – ENABLE ETH Clock Enable
Changing the state of this bit from '0' to '1' or '1' to '0' sets the SYNCBUSY.ENABLE bit to 1. The SYNCBUSY.ENABLE bit stays asserted until the module is either completely enabled or completely disabled.
Note: If the ETH is enabled the user should ensure the ETH finishes all tasks before writing this bit to '0'.

Value	Description
0	Disable module. System clock is only requested for bus transactions. GCLK is never requested, turn off module, disable clocks, disable interrupt event generation.
1	Enable module by allowing both the generic clock and system clock requests based on the incoming clock requests.

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Bit 0 – SWRST Software Reset Busy bit

Synchronizing Busy bit for CTRLA.SWRST

This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.

This bit is set when the synchronization of SWRST bit between clock domains is started.

Notes:

1. When the CTRLA.SWRST is written, the user should poll SYNCB.SWRST bit to know when the reset operation is complete.
2. During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST is cleared by hardware.

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45.7.2. ETH Control B Register

Name: CTRLB
Offset: 0x0004
Reset: 0x000000C0
Property: PAC Write Protected, Enable Write-Protected

Table 45-16. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	TSUINC[1:0]		TSUMS			TSUCLKREQ		
Access	R/W	R/W	R/W			R/W		
Reset	0	1	0			0		

Bits 7:6 – TSUINC[1:0] Timer Adjust Mode
An alternative way of controlling the way the timer increment register
2'b11 = timer register increments as normal
2'b10 = timer register increments by an additional nanosecond
2'b01 = timer increments by a nanosecond less.
2'b00 = uses TSUINC

Bit 5 – TSUMS Timer Adjust

Value	Description
0	The timer register increments as normal, but the timer value is copied to the sync strobe register
1	The "nanoseconds" timer register is cleared and the "seconds" timer register is incremented with each clock cycle.

Bit 2 – TSUCLKREQ TSU GCLK Request

Value	Description
0	no clock request.
1	GCLK_ETH_TSU clock request

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45.7.3. Event Control Register

Name: EVCTRL
Offset: 0x000C
Reset: 0x00000000
Property: PAC Write Protected, Enable Write-Protected

Table 45-17. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								CMPEO
Access								R/W
Reset								0

Bit 0 – CMPEO Enable the Output of the Time Stamp Compare Event

Value	Description
0	Not Enabled
1	Enabled

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45.7.4. SYNCBUSY Register

Name: SYNCB
Offset: 0x0020
Reset: 0x00000000
Property: -

Table 45-18. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							ENABLE	
Access							R/HS/HC	
Reset							0	

Bit 1 – ENABLE Module Enable Synchronization Busy

Value	Description
0	Enable synchronization is not busy
1	Enable synchronization is busy

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45.7.5. Network Control Register

Name: NCR
Offset: 0x1000
Reset: 0x00000000
Property: Read/Write

Table 45-19. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					LPI	FNP	TXPBPF	ENPBPR
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SRTSM			TXZQPF	TXPF	THALT	TSTART	BP
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WESTAT	INCSTAT	CLRSTAT	MPE	TXEN	RXEN	LBL	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	

Bit 19 – LPI Low Power Idle Transmission Enable
When this bit is set, LPI (low power idle) is immediately transmitted. LPI is transmitted even if transmit enable bit NCR.TXEN is disabled.
Setting this bit also sends a pause signal to the transmit datapath.

Bit 18 – FNP Flush Next Packet
Writing a '1' to this bit will flush the next packet from the System RAM. Flushing the next packet will only take effect if the DMA is not currently writing a packet already stored in the DPRAM to memory.

Bit 17 – TXPBPF Transmit PFC Priority-based Pause Frame
Takes the values stored in the Transmit PFC Pause Register.

Bit 16 – ENPBPR Enable PFC Priority-based Pause Reception
Writing a '1' to this bit enables PFC Priority Based Pause Reception capabilities, enabling PFC negotiation and recognition of priority-based pause frames.

Value	Description
0	Normal operation
1	PFC Priority-based Pause frames are recognized.

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Bit 15 – SRTSM Store Receive Time Stamp to Memory
Writing a '1' to this bit causes the CRC of every received frame to be replaced with the value of the nanoseconds field of the 1588 timer that was captured as the receive frame passed the message time stamp point.
Note that bit RFCS in register NCFGR may not be set to 1 when the timer should be captured.

Value	Description
0	Normal operation
1	All received frames' CRC is replaced with a time stamp.

Bit 12 – TXZQPF Transmit Zero Quantum Pause Frame
Writing a '1' to this bit causes a pause frame with zero quantum to be transmitted.
Writing a '0' to this bit has no effect.

Bit 11 – TXPF Transmit Pause Frame
Writing one to this bit causes a pause frame to be transmitted.
Writing a '0' to this bit has no effect.

Bit 10 – THALT Transmit Halt
Writing a '1' to this bit halts transmission as soon as any ongoing frame transmission ends.
Writing a '0' to this bit has no effect.

Bit 9 – TSTART Start Transmission
Writing a '1' to this bit starts transmission.
Writing a '0' to this bit has no effect.

Bit 8 – BP Back Pressure
In 10M or 100M half duplex mode, writing a '1' to this bit forces collisions on all received frames.

Value	Description
0	Frame collisions are not forced.
1	Frame collisions are forced in 10M and 100M half duplex mode.

Bit 7 – WESTAT Write Enable for Statistics Registers
Writing a '1' to this bit makes the statistics registers writable for functional test purposes.

Value	Description
0	Statistics Registers are write-protected.
1	Statistics Registers are write-enabled.

Bit 6 – INCSTAT Increment Statistics Registers
Writing a '1' to this bit increments all Statistics Registers by one for test purposes.
Writing a '0' to this bit has no effect.
This bit will always read '0'.

Bit 5 – CLRSTAT Clear Statistics Registers
Writing a '1' to this bit clears the Statistics Registers.
Writing a '0' to this bit has no effect.
This bit will always read '0'.

Bit 4 – MPE Management Port Enable
Writing a '1' to this bit enables the Management Port.
Writing a '0' to this bit disables the Management Port, and forces MDIO to high impedance state and MDC to low impedance.

Value	Description
0	Management Port is disabled.

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Value	Description
1	Management Port is enabled.

Bit 3 – TXEN Transmit Enable

Writing a '1' to this bit enables the ETH transmitter to send data.
Writing a '0' to this bit stops transmission immediately, the transmit pipeline and control registers is cleared, and the Transmit Queue Pointer Register will be set to point to the start of the transmit descriptor list.

Value	Description
0	Transmit is disabled.
1	Transmit is enabled.

Bit 2 – RXEN Receive Enable

Writing a '1' to this bit enables the ETH to receive data.
Writing a '0' to this bit stops frame reception immediately, and the receive pipeline is cleared. The Receive Queue Pointer Register is not affected.

Value	Description
0	Receive is disabled.
1	Receive is enabled.

Bit 1 – LBL Loop Back Local

Writing '1' to this bit connects ETH_GTX to ETH_GRX, ETH_GTXEN to ETH_GRXDV, and forces full duplex mode.
ETH_GRXCK and ETH_GTXCK may malfunction as the ETH is switched into and out of internal loop back. It is important that receive and transmit circuits have already been disabled when making the switch into and out of internal loop back.

Value	Description
0	Loop back local is disabled.
1	Loop back local is enabled.

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45.7.6. ETH Network Configuration Register

Name: NCFGR
Offset: 0x1004
Reset: 0x00080000
Property: Read/Write

Table 45-20. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
		IRXER	RXBP	IPGSEN		IRXFCS	EFRHD	RXCOEN
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	DCPF	DBW[1:0]		CLK[2:0]			RFCS	LFERD
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	0	0

Bit	15	14	13	12	11	10	9	8
	RXBUFO[1:0]		PEN	RTY				MAXFS
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit	7	6	5	4	3	2	1	0
	UNIHEN	MTIHEN	NBC	CAF	JFRAME	DNVLAN	FD	SPD
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 30 – IRXER Ignore IPG GRXER
When this bit is written to '1', the Receive Error signal (ETH_GRXER) has no effect on the ETH operation when Receive Data Valid signal (ETH_GRXDV) is low.

Bit 29 – RXBP Receive Bad Preamble
When written to '1', frames with non-standard preamble are not rejected.

Bit 28 – IPGSEN IP Stretch Enable
Writing a '1' to this bit allows the transmit IPG to increase above 96 bit times, depending on the previous frame length using the IPG Stretch Register.

Bit 26 – IRXFCS Ignore RX FCS
For normal operation this bit must be written to zero.
When this bit is written to '1', frames with FCS/CRC errors will not be rejected. FCS error statistics will still be collected for frames with bad FCS, and FCS status will be recorded in the DMA descriptor of the frame.

Bit 25 – EFRHD Enable Frames Received in half-duplex
Writing a '1' to this bit enables frames to be received in half-duplex mode while transmitting.

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Bit 24 – RXCOEN Receive Checksum Offload Enable
Writing a '1' to this bit enables the receive checksum engine, and frames with bad IP, TCP or UDP checksums are discarded.

Bit 23 – DCPF Disable Copy of Pause Frames
Writing a '1' to this bit prevents valid pause frames from being copied to memory. Pause frames are not copied regardless of the state of the Copy All Frames (CAF) bit, whether a hash match is found or whether a type ID match is identified.
If a destination address match is found, the pause frame will be copied to memory. Note that valid pause frames received will still increment pause statistics and pause the transmission of frames, as required.

Bits 22:21 – DBW[1:0] Data Bus Width
Should always be written to '1'.

Value	Name	Description
0	DBW32	32-bit data bus width
1	DBW64	64-bit data bus width

Bits 20:18 – CLK[2:0] MDC Clock Division
These bits must be set according to MCK speed, and determine the number MCK will be divided by to generate Management Data Clock (MDC). For conformance with the 802.3 specification, MDC must not exceed 2.5MHz.
Note: MDC is only active during MDIO read and write operations.

Value	Name	Description
0	MCK_8	MCK divided by 8 (MCK up to 20MHz)
1	MCK_16	MCK divided by 16 (MCK up to 40MHz)
2	MCK_32	MCK divided by 32 (MCK up to 80MHz)
3	MCK_48	MCK divided by 48 (MCK up to 120MHz)
4	MCK_64	MCK divided by 64 (MCK up to 160MHz)
5	MCK_96	MCK divided by 96 (MCK up to 240MHz)
6	MCK_128	MCK divided by 128 (MCK up to 320MHz)
7	MCK_224	MCK divided by 224 (MCK up to 560MHz)

Bit 17 – RFCS Remove FCS
Writing this bit to '1' will cause received frames to be written to memory without their frame check sequence (last 4 bytes). The indicated frame length will be reduced by four bytes in this mode.

Bit 16 – LFERD Length Field Error Frame Discard
Writing a '1' to this bit discards frames with a measured length shorter than the extracted length field (as indicated by bytes 13 and 14 in a non-VLAN tagged frame). This only applies to frames with a length field less than 0x0600.

Bits 15:14 – RXBUFO[1:0] Receive Buffer Offset
These bits determine the number of bytes by which the received data is offset from the start of the receive buffer.

Bit 13 – PEN Pause Enable
When written to '1', transmission will pause if a non-zero 802.3 classic pause frame is received and PFC has not been negotiated.

Bit 12 – RTY Retry Test
This bit must be written to '0' for normal operation.

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When writing a '1' to this bit, the back-off between collisions will always be one slot time. This setting helps testing the too many retries condition. This setting is also useful for pause frame tests by reducing the pause counter's decrement time from "512 bit times" to "every GRXCK cycle".

Bit 8 – MAXFS 1536 Maximum Frame Size
Writing a '1' to this bit increases the maximum accepted frame size to 1536 bytes in length. When written to '0', any frame above 1518 bytes in length is rejected.

Bit 7 – UNIHEN Unicast Hash Enable
When writing a '1' to this bit, unicast frames will be accepted when the 6-bit hash function of the destination address points to a bit that is set in the Hash Register.
Writing a '0' to this bit disables unicast hashing.

Bit 6 – MTIHEN Multicast Hash Enable
When writing a '1' to this bit, multicast frames will be accepted when the 6-bit hash function of the destination address points to a bit that is set in the Hash Register.
Writing a '0' to this bit disables multicast hashing.

Bit 5 – NBC No Broadcast
Writing a '1' to this bit will reject frames addressed to the broadcast address 0xFFFFFFFFFFFF (all '1').
Writing a '0' to this bit allows broadcasting to 0xFFFFFFFFFFFF.

Bit 4 – CAF Copy All Frames
When writing a '1' to this bit, all valid frames will be accepted.

Bit 3 – JFRAME Jumbo Frame Size
Writing a '1' to this bit enables jumbo frames of up to 10240 bytes to be accepted. The default length is 10240 bytes.

Bit 2 – DNVLAN Discard Non-VLAN Frames
Writing a '1' to this bit allows only VLAN-tagged frames to pass to the address matching logic.
Writing a '0' to this bit allows both VLAN_tagged and untagged frames to pass to the address matching logic.

Bit 1 – FD Full Duplex
Writing a '1' enables full duplex operation, so the transmit block ignores the state of collision and carrier sense and allows receive while transmitting.
Writing a '0' disables full duplex operation.

Bit 0 – SPD Speed
Writing a '1' selects 100Mbps operation.
Writing a '0' to this bit selects 10Mbps operation.

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45.7.7. ETH Network Status Register

Name: NSR
Offset: 0x1008
Reset: 0x000001X0
Property: Read-only

Table 45-21. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						IDLE	MDIO	
Access						R	R	
Reset						1	0	

Bit 2 – IDLE PHY Management Logic Idle
The PHY management logic is idle (i.e., has completed).

Bit 1 – MDIO MDIO Input Status
Returns status of the MDIO pin.

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45.7.8. ETH User Register

Name: UR
Offset: 0x100C
Reset: 0x00000000
Property: -

Table 45-22. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								MII
Access								R/W
Reset								0

Bit 0 – MII Reduced MII Mode

Value	Description
0	RMII mode is selected
1	MII mode is selected

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45.7.9. ETH DMA Configuration Register

Name: DCFGR
Offset: 0x1010
Reset: 0x00020004
Property: Read/Write

Table 45-23. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
								DDRP
Access								R/W
Reset								0

Bit	23	22	21	20	19	18	17	16
	DRBS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bit	15	14	13	12	11	10	9	8
					TXCOEN	TXPBMS	RXBMS[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	1	1	1

Bit	7	6	5	4	3	2	1	0
	ESPA	ESMA		FBLDO[4:0]				
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W
Reset	0	0		0	0	1	0	0

Bit 24 – DDRP DMA Discard Receive Packets
A write to this bit is ignored if the DMA is not configured in the packet buffer full store and forward mode.

Value	Description
0	Received packets are stored in the SRAM based packet buffer until next AHB buffer resource becomes available.
1	Receive packets from the receiver packet buffer memory are automatically discarded when no AHB resource is available.

Bits 23:16 – DRBS[7:0] DMA Receive Buffer Size
These bits defined by these bits determines the size of buffer to use in main AHB system memory when writing received data.
The value is defined in multiples of 64 bytes. For example:

- 0x02: 128 bytes
- 0x18: 1536 bytes (1 × max length frame/buffer)
- 0xA0: 10240 bytes (1 × 10K jumbo frame/buffer)

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WARNING Do not write 0x00 to this bit field.

Bit 11 – TXCOEN Transmitter Checksum Generation Offload Enable
Transmitter IP, TCP and UDP checksum generation offload enable.

Value	Description
0	Frame data is unaffected.
1	The transmitter checksum generation engine calculates and substitutes checksums for transmit frames.

Bit 10 – TXPBMS Transmitter Packet Buffer Memory Size Select
When written to zero, the amount of memory used for the transmit packet buffer is reduced by 50%. This reduces the amount of memory used by the ETH.
It is important to write this bit to '1' if the full configured physical memory is available. The value in parentheses represents the size that would result for the default maximum configured memory size of 4 KBytes.

Value	Description
0	Top address bits not used. (2KByte used.)
1	Full configured addressable space (4KBytes) used.

Bits 9:8 – RXBMS[1:0] Receiver Packet Buffer Memory Size Select
The default receive packet buffer size is FULL=8 Kbytes. The table below shows how to configure this memory to FULL, HALF, QUARTER or EIGHTH of the default size.

Value	Name	Description
0	EIGHTH	8/8 Kbyte Memory Size
1	QUARTER	8/4 Kbytes Memory Size
2	HALF	8/2 Kbytes Memory Size
3	FULL	8 Kbytes Memory Size

Bit 7 – ESPA Endian Swap Mode Enable for Packet Data Accesses

Value	Description
0	Little endian mode for AHB transfers selected.
1	Big endian mode for AHB transfers selected.

Bit 6 – ESMA Endian Swap Mode Enable for Management Descriptor Accesses

Value	Description
0	Little endian mode for AHB transfers selected.
1	Big endian mode for AHB transfers selected.

Bits 4:0 – FBLDO[4:0] Fixed Burst Length for DMA Data Operations
Selects the burst length to attempt to use on the AHB when transferring frame data. Not used for DMA management operations and only used where space and data size allow. Otherwise SINGLE type AHB transfers are used.
One-hot priority encoding enforced automatically on register writes as follows. 'x' represents don't care.

Value	Name	Description
0	-	Reserved
1	SINGLE	00001: Always use SINGLE AHB bursts
2	-	Reserved
4	INCR4	001xx: Attempt to use INCR4 AHB bursts (Default)

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Value	Name	Description
8	INCR8	01xxx: Attempt to use INCR8 AHB bursts
16	INCR16	1xxxx: Attempt to use INCR16 AHB bursts

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45.7.10. ETH Transmit Status Register

Name: TSR
Offset: 0x1014
Reset: 0x00000000
Property: -

Table 45-24. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
								HRESP
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
		UND	TXCOMP	TFC	TXGO	RLE	COL	UBR
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 8 – HRESP HRESP Not OK
Set when the DMA block sees HRESP not OK.
This bit is cleared by writing a '1' to it.

Bit 6 – UND Transmit Underrun
This bit is set if the transmitter was forced to terminate a frame that it had already began transmitting due to further data being unavailable. This bit is set if a transmitter status write back has not completed when another status write back is attempted. When using the DMA interface configured for internal FIFO mode, this bit is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB not OK response was returned, or because a used bit was read. When using the DMA interface configured for packet buffer mode, this bit will never be set.

Bit 5 – TXCOMP Transmit Complete
Set when a frame has been transmitted.
This bit is cleared by writing a '1' to it.

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Bit 4 – TFC Transmit Frame Corruption Due to AHB Error

This bit is set when an error occurs during reading transmit frame from the AHB. Error causes include HRESP errors and buffers exhausted mid frame. (If the buffers run out during transmission of a frame then transmission stops, FCS shall be bad and TXER asserted).
In DMA packet buffer mode, this bit is also set if a single frame is too large for the configured packet buffer memory size.
This bit is cleared by writing a '1' to it.

Bit 3 – TXGO Transmit Go

This bit is '1' when transmit is active. When using the DMA interface this bit represents the TXGO variable as specified in the transmit buffer description.

Bit 2 – RLE Retry Limit Exceeded

This bit is cleared by writing a '1' to it.

Bit 1 – COL Collision Occurred

When operating in 10/100Mbps mode, this bit is set by the assertion of either a collision or a late collision.
This bit is cleared by writing a '1' to it.

Bit 0 – UBR Used Bit Read

This bit is set when a transmit buffer descriptor is read with its used bit set.
This bit is cleared by writing a '1' to it.

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45.7.11. ETH Receive Buffer Queue Base Address Register

Name: RBQB
Offset: 0x1018
Reset: 0x00000000
Property: Read/Write

This register holds the start address of the receive buffer queue (receive buffers descriptor list). The receive buffer queue base address must be initialized before receive is enabled through bit 2 of the Network Control Register. Once reception is enabled, any write to the Receive Buffer Queue Base Address Register is ignored. Reading this register returns the location of the descriptor currently being accessed. This value increments as buffers are used. Software should not use this register for determining where to remove received frames from the queue as it constantly changes as new frames are received. Software should instead work its way through the buffer descriptor queue checking the “used” bits.

In terms of AMBA AHB operation, the descriptors are read from memory using a single 32-bit AHB access. The descriptors should be aligned at 32-bit boundaries and the descriptors are written to using two individual non sequential accesses.

Table 45-25. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADDR[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	ADDR[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	ADDR[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	ADDR[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bits 31:2 – ADDR[29:0] Receive Buffer Queue Base Address
Written with the address of the start of the receive queue.

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45.7.12. ETH Transmit Buffer Queue Base Address Register

Name: TBQB
Offset: 0x101C
Reset: 0x00000000
Property: -

This register holds the start address of the transmit buffer queue (transmit buffers descriptor list). The Transmit Buffer Queue Base Address Register must be initialized before transmit is started through bit 9 of the Network Control Register. Once transmission has started, any write to the Transmit Buffer Queue Base Address Register is illegal and therefore ignored.

Note that due to clock boundary synchronization, it takes a maximum of four MCK cycles from the writing of the transmit start bit before the transmitter is active. Writing to the Transmit Buffer Queue Base Address Register during this time may produce unpredictable results.

Reading this register returns the location of the descriptor currently being accessed. Since the DMA handles two frames at once, this may not necessarily be pointing to the current frame being transmitted.

In terms of AMBA AHB operation, the descriptors are written to memory using a single 32-bit AHB access. The descriptors should be aligned at 32-bit boundaries and the descriptors are read from memory using two individual non sequential accesses.

Table 45-26. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADDR[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bits 31:2 – ADDR[29:0] Transmit Buffer Queue Base Address
Written with the address of the start of the transmit queue.

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45.7.13. ETH Receive Status Register

Name: RSR
Offset: 0x1020
Reset: 0x00000000
Property: -

This register, when read, provides receive status details. Once read, individual bits may be cleared by writing a '1' to them. It is not possible to set a bit to '1' by writing to this register.

Table 45-27. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					HNO	RXOVR	REC	BNA
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – HNO HRESP Not OK
This bit is set when the DMA block sees HRESP not OK.
This bit is cleared by writing a '1' to it.

Bit 2 – RXOVR Receive Overrun
This bit is set if the receive status was not taken at the end of the frame. The buffer will be recovered if an overrun occurs.
This bit is cleared by writing a '1' to it.

Bit 1 – REC Frame Received
This bit is set to when one or more frames have been received and placed in memory.
This bit is cleared by writing a '1' to it.

Bit 0 – BNA Buffer Not Available
When this bit is set, an attempt was made to get a new buffer and the pointer indicated that it was owned by the processor. The DMA will re-read the pointer each time an end of frame is received until a valid pointer is found. This bit is set following each descriptor read attempt that fails, even if consecutive pointers are unsuccessful and software has in the mean time cleared the status flag.

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This bit is cleared by writing a '1' to it.

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45.7.14. ETH Interrupt Status Register

Name: ISR
Offset: 0x1024
Reset: 0x00000000
Property: Write to Clear

This register indicates the source of the interrupt. An interrupt source must be enabled in the mask register first so the corresponding bits of this register will be set and the ETH interrupt signal will be asserted in the system.

Note: Interrupt flags must be cleared and then read back to confirm the clear before exiting the ISR to avoid double interrupts.

Table 45-28. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	R	R	R	R	R	R		
Reset	0	0	0	0	0	0		

Bit	15	14	13	12	11	10	9	8
		PFTR	PTZ	PFNZ	HRESP	ROVR		
Access		R	R	R	R	R		
Reset		0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 29 – TSUTIMCMP TSU Timer Comparison
Indicates when TSU timer count value is equal to programmed value.
Cleared on read.

Bit 28 – WOL Wake On LAN
WOL interrupt. Indicates a WOL message has been received.

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.
Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment
Indicates the register has incremented.
Cleared on read.

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Bit 25 – PDRSFT PDelay Response Frame Transmitted
Indicates a PTP pdelay_resp frame has been transmitted.
Cleared on read.

Bit 24 – PDRQFT PDelay Request Frame Transmitted
Indicates a PTP pdelay_req frame has been transmitted.
Cleared on read.

Bit 23 – PDRSFR PDelay Response Frame Received
Indicates a PTP pdelay_resp frame has been received.
Cleared on read.

Bit 22 – PDRQFR PDelay Request Frame Received
Indicates a PTP pdelay_req frame has been received.
Cleared on read.

Bit 21 – SFT PTP Sync Frame Transmitted
Indicates a PTP sync frame has been transmitted.
Cleared on read.

Bit 20 – DRQFT PTP Delay Request Frame Transmitted
Indicates a PTP delay_req frame has been transmitted.
Cleared on read.

Bit 19 – SFR PTP Sync Frame Received
Indicates a PTP sync frame has been received.
Cleared on read.

Bit 18 – DRQFR PTP Delay Request Frame Received
Indicates a PTP delay_req frame has been received.
Cleared on read.

Bit 14 – PFTR Pause Frame Transmitted
Indicates a pause frame has been successfully transmitted after being initiated from the Network Control Register.
Cleared on read.

Bit 13 – PTZ Pause Time Zero
Set when either the Pause Time Register at address 0x1038 decrements to zero, or when a valid pause frame is received with a zero pause quantum field.
Cleared on read.

Bit 12 – PFNZ Pause Frame with Non-zero Pause Quantum Received
Indicates a valid pause has been received that has a non-zero pause quantum field.
Cleared on read.

Bit 11 – HRESP HRESP Not OK
Set when the DMA block sees HRESP not OK.
Cleared on read.

Bit 10 – ROVR Receive Overrun
Set when the receive overrun status bit is set.
Cleared on read.

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Bit 7 – TCOMP Transmit Complete
Set when a frame has been transmitted.
Cleared on read.

Bit 6 – TFC Transmit Frame Corruption Due to AHB Error
Transmit frame corruption due to AHB error. Set if an error occurs during reading a transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame.

Bit 5 – RLEX Retry Limit Exceeded
Retry Limit Exceeded Transmit error.
Cleared on read.

Bit 4 – TUR Transmit Underrun
This interrupt is set if the transmitter was forced to terminate an ongoing frame transmission due to further data being unavailable.
This interrupt is also set if a transmitter status write back has not completed when another status write back is attempted.
This interrupt is also set when the transmit DMA has written the SOP data into the FIFO and either the AHB bus was not granted in time for further data, or because an AHB not OK response was returned, or because the used bit was read.

Bit 3 – TXUBR TX Used Bit Read
Set when a transmit buffer descriptor is read with its used bit set.
Cleared on read.

Bit 2 – RXUBR RX Used Bit Read
Set when a receive buffer descriptor is read with its used bit set.
Cleared on read.

Bit 1 – RCOMP Receive Complete
A frame has been stored in memory.
Cleared on read.

Bit 0 – MFS Management Frame Sent
The PHY Maintenance Register has completed its operation.
Cleared on read.

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45.7.15. ETH Interrupt Enable Register

Name: IER
Offset: 0x1028
Reset: –
Property: Write-only

This register is write-only and will always return zero.

The following values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Table 45-29. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			W	W	R	W	W	W
Reset			-	-	-	-	-	-

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	W	W	W	W	W	W		
Reset	-	-	-	-	-	-		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	W	W	W	W	W	W		
Reset	-	-	-	-	-	-		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	W	W	W	W	W	W	W	W
Reset	-	-	-	-	-	-	-	-

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.
Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

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Bit 23 – PDRSFR PDelay Response Frame Received

Bit 22 – PDRQFR PDelay Request Frame Received

Bit 21 – SFT PTP Sync Frame Transmitted

Bit 20 – DRQFT PTP Delay Request Frame Transmitted

Bit 19 – SFR PTP Sync Frame Received

Bit 18 – DRQFR PTP Delay Request Frame Received

Bit 15 – EXINT External Interrupt

Bit 14 – PFTR Pause Frame Transmitted

Bit 13 – PTZ Pause Time Zero

Bit 12 – PFNZ Pause Frame with Non-zero Pause Quantum Received

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

Bit 6 – TFC Transmit Frame Corruption Due to AHB Error

Bit 5 – RLEX Retry Limit Exceeded or Late Collision

Bit 4 – TUR Transmit Underrun

Bit 3 – TXUBR TX Used Bit Read

Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

Bit 0 – MFS Management Frame Sent

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45.7.16. ETH Interrupt Disable Register

Name: IDR
Offset: 0x102C
Reset: –
Property: Write-only

This register is write-only and will always return zero.

The following values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Table 45-30. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			W	W	R	W	W	W
Reset			-	-	-	-	-	-

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	W	W	W	W	W	W		
Reset	-	-	-	-	-	-		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	W	W	W	W	W	W		
Reset	-	-	-	-	-	-		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	W	W	W	W	W	W	W	W
Reset	-	-	-	-	-	-	-	-

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.
Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

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Bit 23 – PDRSFR PDelay Response Frame Received

Bit 22 – PDRQFR PDelay Request Frame Received

Bit 21 – SFT PTP Sync Frame Transmitted

Bit 20 – DRQFT PTP Delay Request Frame Transmitted

Bit 19 – SFR PTP Sync Frame Received

Bit 18 – DRQFR PTP Delay Request Frame Received

Bit 15 – EXINT External Interrupt

Bit 14 – PFTR Pause Frame Transmitted

Bit 13 – PTZ Pause Time Zero

Bit 12 – PFNZ Pause Frame with Non-zero Pause Quantum Received

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

Bit 6 – TFC Transmit Frame Corruption Due to AHB Error

Bit 5 – RLEX Retry Limit Exceeded or Late Collision

Bit 4 – TUR Transmit Underrun

Bit 3 – TXUBR TX Used Bit Read

Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

Bit 0 – MFS Management Frame Sent

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45.7.17. ETH Interrupt Mask Register

Name: IMR
Offset: 0x1030
Reset: 0x07FFFFFF
Property: Read/Write

This register is a read-only register indicating which interrupts are masked. All bits are set at Reset and can be reset individually by writing to the Interrupt Enable Register (IER), or set individually by writing to the Interrupt Disable Register (IDR).

For test purposes there is a write-only function to this register that allows the bits in the Interrupt Status Register to be set or cleared, regardless of the state of the mask register. A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

The following values are valid for all listed bit names of this register when read:

0: The corresponding interrupt is enabled.

1: The corresponding interrupt is not enabled.

Table 45-31. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	1	1	1

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	1	1	1	1	1	1		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	1	1	1	1	1	1		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.
Cleared on read.

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Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

Bit 23 – PDRSFR PDelay Response Frame Received

Bit 22 – PDRQFR PDelay Request Frame Received

Bit 21 – SFT PTP Sync Frame Transmitted

Bit 20 – DRQFT PTP Delay Request Frame Transmitted

Bit 19 – SFR PTP Sync Frame Received

Bit 18 – DRQFR PTP Delay Request Frame Received

Bit 15 – EXINT External Interrupt

Bit 14 – PFTR Pause Frame Transmitted

Bit 13 – PTZ Pause Time Zero

Bit 12 – PFNZ Pause Frame with Non-zero Pause Quantum Received

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

Bit 6 – TFC Transmit Frame Corruption Due to AHB Error

Bit 5 – RLEX Retry Limit Exceeded

Bit 4 – TUR Transmit Underrun

Bit 3 – TXUBR TX Used Bit Read

Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

Bit 0 – MFS Management Frame Sent

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45.7.18. ETH PHY Maintenance Register

Name: MAN
Offset: 0x1034
Reset: 0x00000000
Property: Read/Write

This register is a shift register. Writing to it starts a shift operation which is signaled completed when bit 2 is set in the Network Status Register (NSR). It takes about 2000 MCK cycles to complete, when MDC is set for MCK divide by 32 in the Network Configuration Register. An interrupt is generated upon completion.

During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each MDC cycle. This causes transmission of a PHY management frame on MDIO. Refer also to section 22.2.4.5 of the IEEE 802.3 standard.

Reading during the shift operation returns the current contents of the shift register. At the end of management operation, the bits will have shifted back to their original locations. For a read operation, the data bits are updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced.

The MDIO interface can read IEEE 802.3 clause 45 PHYs, as well as clause 22 PHYs. To read clause 45 PHYs, bit 30 should be written with a '0' rather than a '1'. To write clause 45 PHYs, bits 31:28 should be written as 0x1:

PHY	Access	Bit Value			
		WZO	CLTTO	OP[1]	OP[0]
Clause 22	Read	0	1	1	0
	Write	0	1	0	1
Clause 45	Read	0	0	1	1
	Write	0	0	0	1
	Read + Address	0	0	1	0

For a description of MDC generation, see also the 'ETH Network Configuration Register' (NCR) description.

Table 45-32. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

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Bit	31	30	29	28	27	26	25	24
	WZO	CLTTO	OP[1:0]		PHYA[4:1]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PHYA[0]	REGA[4:0]					WTN[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – WZO Write ZERO
Must be written to '0'.

Value	Description
0	Mandatory
1	Reserved

Bit 30 – CLTTO Clause 22 Operation

Value	Description
0	Clause 45 operation
1	Clause 22 operation

Bits 29:28 – OP[1:0] Operation

Value	Description
01	Write
10	Read
Other	Reseved

Bits 27:23 – PHYA[4:0] PHY Address

Bits 22:18 – REGA[4:0] Register Address
Specifies the register in the PHY to access.

Bits 17:16 – WTN[1:0] Write Ten
Must be written to '10'.

Value	Description
10	Mandatory
Other	Reserved

Bits 15:0 – DATA[15:0] PHY Data
For a write operation, this field is written with the data to be written to the PHY.
After a read operation, this field contains the data read from the PHY.

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45.7.19. ETH Receive Pause Quantum Register

Name: RPQ
Offset: 0x1038
Reset: 0x00000000
Property: -

Table 45-33. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RPQ[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RPQ[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RPQ[15:0] Received Pause Quantum
Stores the current value of the Receive Pause Quantum Register which is decremented every 512 bit times.

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45.7.20. ETH Transmit Pause Quantum Register

Name: TPQ
Offset: 0x103C
Reset: 0x0000FFFF
Property: -

Table 45-34. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TPQ[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	TPQ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:0 – TPQ[15:0] Transmit Pause Quantum
Written with the pause quantum value for pause frame transmission.

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45.7.21. ETH TX Partial Store and Forward Register

Name: TPSF
Offset: 0x1040
Reset: 0x000003FF
Property: -

Table 45-35. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ENTXP							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					TPB1ADR[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	1	1

Bit	7	6	5	4	3	2	1	0
	TPB1ADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 31 – ENTXP Enable TX Partial Store and Forward Operation

Bits 11:0 – TPB1ADR[11:0] Transmit Partial Store and Forward Address Watermark value.
This value must be ≥ 0x14.

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45.7.22. ETH RX Partial Store and Forward Register

Name: RPSF
Offset: 0x1044
Reset: 0x000003FF
Property: -

Table 45-36. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ENRXP							
Access	R							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RPB1ADR[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	1	1

Bit	7	6	5	4	3	2	1	0
	RPB1ADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 31 – ENRXP Enable RX Partial Store and Forward Operation

Bits 11:0 – RPB1ADR[11:0] Receive Partial Store and Forward Address Watermark value. Reset = 1.

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45.7.23. ETH RX Jumbo Frame Max Length Register

Name: RJFML
Offset: 0x1048
Reset: 0x00002800
Property: Read/Write

Table 45-37. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			FML[13:8]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
	FML[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 13:0 – FML[13:0] Frame Max Length
Rx jumbo frame maximum length.

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45.7.24. ETH Hash Register Bottom

Name: HRB
Offset: 0x1080
Reset: 0x00000000
Property: Read/Write

The unicast hash enable (UNIHEN) and the multicast hash enable (MITIHEN) bits in the Network Configuration Register (NCFGR) enable the reception of hash matched frames.

Table 45-38. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Hash Address
The first 32 bits of the Hash Address Register.

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45.7.25. ETH Hash Register Top

Name: HRT
Offset: 0x1084
Reset: 0x00000000
Property: Read/Write

The Unicast Hash Enable (UNIHEN) and the Multicast Hash Enable (MITIHEN) bits in the Network Configuration Register (NCFGR) enable the reception of hash matched frames.

Table 45-39. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Hash Address
Bits 63 to 32 of the Hash Address Register.

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45.7.26. GMAC Specific Address n Bottom Register

Name: SABx
Offset: 0x1088 + (x-1)*0x08 [x=1..5]
Reset: 0x00000000
Property: Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

Table 45-40. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Specific Address n
Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.
Note: The SABx and SATx registers must be initialized from the FCCFG72 (FMAC_31_0) and FCCFG72 (FMAC_47_32) locations in OTPCAL.

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45.7.27. GMAC Specific Address n Top Register

Name: SATx
Offset: 0x01008C + (x-1)*0x08 [x=1..5]
Reset: 0x00000000
Property: Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

Table 45-41. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADDR[15:0] Specific Address n
The most significant bits of the destination address, that is, bits 47:32.
Note: The SABx and SATx registers must be initialized from the FCCFG72 (FMAC_31_0) and FCCFG72 (FMAC_47_32) locations in OTPCAL.

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45.7.28. ETH Type ID Match n Register

Name: TIDMx
Offset: 0x10A8 + (x-1)*0x04 [x=1..4]
Reset: 0x00000000
Property: Read/Write

Table 45-42. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ENIDn							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TID[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – ENIDn Enable Copying of TID Matched Frames

Value	Description
0	TID n is not part of the comparison match.
1	TID n is processed for the comparison match.

Bits 15:0 – TID[15:0] Type ID Match n
For use in comparisons with received frames type ID/length frames.

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45.7.29. ETH Wake on LAN Register

Name: WOL
Offset: 0x10B8
Reset: 0x00000000
Property: -

Table 45-43. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					MTI	SA1	ARP	MAG
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 19 – MTI Multicast Hash Event Enable

Value	Description
0	Wake on LAN multicast hash Event disabled
1	Wake on LAN multicast hash Event enabled

Bit 18 – SA1 Specific Address Register 1 Event Enable

Value	Description
0	Wake on Specific Address Register 1 Event disabled
1	Wake on Specific Address Register 1 Event enabled

Bit 17 – ARP ARP Request Event Enable

Value	Description
0	Wake on LAN ARP request Event disabled
1	Wake on LAN ARP request Event enabled

Bit 16 – MAG Magic Packet Event Enable

Value	Description
0	Wake on LAN magic packet Event disabled

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Value	Description
1	Wake on LAN magic packet Event enabled

Bits 15:0 – IP[15:0] ARP Request IP Address

Wake on LAN ARP request IP address. Written to define the 16 least significant bits of the target IP address that is matched to generate a Wake on LAN event.

Value	Description
0x0000	No Event generated, even if matched by the received frame.
0x0001-0xFFFF	Wake on LAN Event generated for matching LSB of the target IP address.

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45.7.30. ETH IPG Stretch Register

Name: IPGS
Offset: 0x10BC
Reset: 0x00000000
Property: -

Table 45-44. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FL[15:0] Frame Length

Bits FL[7:0] are multiplied with the previously transmitted frame length (including preamble), and divided by FL[15:8]+1 (adding 1 to prevent division by zero). $\mathrm{RESULT} = \frac{\mathrm{FL[7:0]}}{\mathrm{F[15+8]+1}}$

If RESULT > 96 and the IP Stretch Enable bit in the Network Configuration Register (NCFGR.IPGSEN) is written to '1', RESULT is used for the transmit inter-packet-gap.

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45.7.31. ETH Stacked VLAN Register

Name: SVLAN
Offset: 0x10C0
Reset: 0x00000000
Property: -

Table 45-45. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ESVLAN							
Access	-							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	VLAN_TYPE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VLAN_TYPE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – ESVLAN Enable Stacked VLAN Processing Mode
0: Disable the stacked VLAN processing mode
1: Enable the stacked VLAN processing mode

Value	Description
0	Stacked VLAN Processing disabled
1	Stacked VLAN Processing enabled

Bits 15:0 – VLAN_TYPE[15:0] User Defined VLAN_TYPE Field
When Stacked VLAN is enabled (ESVLAN=1), the first VLAN tag in a received frame will only be accepted if the VLAN type field is equal to this user defined VLAN_TYPE, OR equal to the standard VLAN type (0x8100).
Note: The second VLAN tag of a Stacked VLAN packet will only be matched correctly if its VLAN_TYPE field equals 0x8100.

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45.7.32. ETH Transmit PFC Pause Register

Name: TPFCP
Offset: 0x10C4
Reset: 0x00000000
Property: -

Table 45-46. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PQ[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PEV[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – PQ[7:0] Pause Quantum
When the Remove FCS bit in the ETH Network Configuration register (NCFGR.RFCS) is written to '1', and one or more bits in this bit field are written to '0', the associated PFC pause frame's pause quantum field value is taken from the Transmit Pause Quantum register (TPQ).
For each entry equal to '1' in this bit field, the pause quantum associated with that entry will be zero.

Bits 7:0 – PEV[7:0] Priority Enable Vector
When the Remove FCS bit in the ETH Network Configuration register (NCFGR.RFCS) is written to '1', the priority enable vector of the PFC priority-based pause frame is set to the value stored in this bit field.

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45.7.33. ETH Specific Address 1 Mask Bottom

Name: SAMB1
Offset: 0x10C8
Reset: 0x00000000
Property: -

Table 45-47. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Specific Address 1 Mask
Setting a bit to '1' masks the corresponding bit in the Specific Address 1 Bottom register (SAB1).

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45.7.34. ETH Specific Address Mask 1 Top

Name: SAMT1
Offset: 0x10CC
Reset: 0x00000000
Property: -

Table 45-48. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADDR[15:0] Specific Address 1 Mask
Setting a bit to '1' masks the corresponding bit in the Specific Address 1 register SAT1.

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45.7.35. ETH 1588 Timer Nanosecond Comparison Register

Name: NSC
Offset: 0x10DC
Reset: 0x00000000
Property: -

Table 45-49. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			NANOSEC[21:16]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NANOSEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NANOSEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 21:0 – NANOSEC[21:0] 1588 Timer Nanosecond Comparison Value
Value is compared to the bits [45:24] of the TSU timer count value (upper 22 bits of nanosecond value).

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45.7.36. ETH 1588 Timer Second Comparison Low Register

Name: SCL
Offset: 0x10E0
Reset: 0x00000000
Property: -

Table 45-50. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	SEC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SEC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SEC[31:0] 1588 Timer Second Comparison Value
Value is compared to seconds value bits [31:0] of the TSU timer count value.

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45.7.37. ETH 1588 Timer Second Comparison High Register

Name: SCH
Offset: 0x10E4
Reset: 0x00000000
Property: -

Table 45-51. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SEC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SEC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – SEC[15:0] 1588 Timer Second Comparison Value
Value is compared to the top 16 bits (most significant 16 bits [47:32] of seconds value) of the TSU timer count value.

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45.7.38. ETH PTP Event Frame Transmitted Seconds High Register

Name: EFTSH
Offset: 0x10E8
Reset: 0x00000000
Property: Read-only

Table 45-52. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RUD[15:0] Register Update

The register is updated with the value that the IEEE 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.39. ETH PTP Event Frame Received Seconds High Register

Name: EFRSH
Offset: 0x10EC
Reset: 0x00000000
Property: Read-only

Table 45-53. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RUD[15:0] Register Update

The register is updated with the value that the IEEE 1588 timer seconds register held when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.40. ETH PTP Peer Event Frame Transmitted Seconds High Register

Name: PEFTSH
Offset: 0x10F0
Reset: 0x00000000
Property: -

Table 45-54. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RUD[15:0] Register Update

The register is updated with the value that the IEEE 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.41. ETH PTP Peer Event Frame Received Seconds High Register

Name: PEFRSH
Offset: 0x10F4
Reset: 0x00000000
Property: -

Table 45-55. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RUD[15:0] Register Update

The register is updated with the value that the 1588 timer seconds register held when the SFD of a PTP transmit peer event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.42. ETH Octets Transmitted Low Register

Name: OTLO
Offset: 0x1100
Reset: 0x00000000
Property: Read-Only(Cleared on Read)

When reading the Octets Transmitted and Octets Received Registers, bits [31:0] should be read prior to bits [47:32] to ensure reliable operation.

Table 45-56. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	TXO[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TXO[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TXO[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXO[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TXO[31:0] Transmitted Octets
Transmitted octets in valid frames of any type without errors, bits [31:0]. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames.

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45.7.43. ETH Octets Transmitted High Register

Name: OTHI
Offset: 0x1104
Reset: 0x00000000
Property: Read-Only(Cleared on Read)

When reading the Octets Transmitted and Octets Received Registers, bits [31:0] should be read prior to bits [47:32] to ensure reliable operation.

Table 45-57. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TXO[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXO[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TXO[15:0] Transmitted Octets
Transmitted octets in valid frames of any type without errors, bits [47:32]. This counter is 48-bits, and is read through two registers. This count does not include octets from automatically generated pause frames.

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45.7.44. ETH Frames Transmitted

Name: FT
Offset: 0x1108
Reset: 0x00000000
Property: Read-only(Cleared on Read)

Table 45-58. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	FTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – FTX[31:0] Frames Transmitted without Error
Frames transmitted without error. This register counts the number of frames successfully transmitted, i.e., no underrun and not too many retries. Excludes pause frames.

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45.7.45. ETH Broadcast Frames Transmitted Register

Name: BCFT
Offset: 0x110C
Reset: 0x00000000
Property: Read-only(Cleared on Read)

Table 45-59. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	BFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BFTX[31:0] Broadcast Frames Transmitted without Error
This register counts the number of broadcast frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

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45.7.46. ETH Multicast Frames Transmitted Register

Name: MFT
Offset: 0x1110
Reset: 0x00000000
Property: Read-Only(Cleared on Read)

Table 45-60. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	MFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MFTX[31:0] Multicast Frames Transmitted without Error
This register counts the number of multicast frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

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45.7.47. ETH Pause Frames Transmitted Register

Name: PFT
Offset: 0x1114
Reset: 0x00000000
Property: -

Table 45-61. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PFTX[15:0] Pause Frames Transmitted Register
This register counts the number of pause frames transmitted. Only pause frames triggered by the register interface or through the external pause pins are counted as pause frames. Pause frames received through the FIFO interface are counted in the frames transmitted counter.

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45.7.48. ETH 64-Byte Frames Transmitted Register

Name: BFT64
Offset: 0x1118
Reset: 0x00000000
Property: Read-only

Table 45-62. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 64-Byte Frames Transmitted without Error
This register counts the number of 64-byte frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

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45.7.49. ETH 65 to 127 Byte Frames Transmitted Register

Name: TBFT127
Offset: 0x101C
Reset: 0x00000000
Property: -

Table 45-63. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 65 to 127 Byte Frames Transmitted without Error
This register counts the number of 65 to 127 byte frames successfully transmitted without error, i.e., no underrun and not too many retries. Excludes pause frames.

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45.7.50. ETH 128 to 255 Byte Frames Transmitted Register

Name: TBFT255
Offset: 0x1120
Reset: 0x00000000
Property: -

Table 45-64. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 128 to 255 Byte Frames Transmitted without Error
This register counts the number of 128 to 255 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

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45.7.51. ETH 256 to 511 Byte Frames Transmitted Register

Name: TBFT511
Offset: 0x1124
Reset: 0x00000000
Property: -

Table 45-65. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 256 to 511 Byte Frames Transmitted without Error
This register counts the number of 256 to 511 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

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45.7.52. ETH 512 to 1023 Byte Frames Transmitted Register

Name: TBFT1023
Offset: 0x1128
Reset: 0x00000000
Property: -

Table 45-66. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 512 to 1023 Byte Frames Transmitted without Error
This register counts the number of 512 to 1023 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

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45.7.53. ETH 1024 to 1518 Byte Frames Transmitted Register

Name: TBFT1518
Offset: 0x112C
Reset: 0x00000000
Property: -

Table 45-67. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 1024 to 1518 Byte Frames Transmitted without Error
This register counts the number of 1024 to 1518 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

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45.7.54. ETH Greater Than 1518 Byte Frames Transmitted Register

Name: GTBFT1518
Offset: 0x1130
Reset: 0x00000000
Property: Read-only

Table 45-68. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] Greater than 1518 Byte Frames Transmitted without Error
This register counts the number of 1518 or above byte frames successfully transmitted without error i.e., no underrun and not too many retries.

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45.7.55. ETH Transmit Underruns Register

Name: TUR
Offset: 0x1134
Reset: 0x00000000
Property: -

Table 45-69. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							TXUNR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	TXUNR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – TXUNR[9:0] Transmit Underruns
This register counts the number of frames not transmitted due to a transmit underrun. If this register is incremented then no other statistics register is incremented.

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45.7.56. ETH Single Collision Frames Register

Name: SCF
Offset: 0x1138
Reset: 0x00000000
Property: -

Table 45-70. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							SCOL[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	SCOL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – SCOL[17:0] Single Collision
This register counts the number of frames experiencing a single collision before being successfully transmitted i.e., no underrun.

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45.7.57. ETH Multiple Collision Frames Register

Name: MCF
Offset: 0x113C
Reset: 0x00000000
Property: -

Table 45-71. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							MCOL[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	MCOL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – MCOL[17:0] Multiple Collision

This register counts the number of frames experiencing between two and fifteen collisions prior to being successfully transmitted, i.e., no underrun and not too many retries.

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45.7.58. ETH Excessive Collisions Register

Name: EC
Offset: 0x1140
Reset: 0x00000000
Property: Read-only

Table 45-72. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							XCOL[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	XCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – XCOL[9:0] Excessive Collisions
This register counts the number of frames that failed to be transmitted because they experienced 16 collisions.

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45.7.59. ETH Late Collisions Register

Name: LC
Offset: 0x1144
Reset: 0x00000000
Property: -

Table 45-73. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							LCOL[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	LCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – LCOL[9:0] Late Collisions
This register counts the number of late collisions occurring after the slot time (512 bits) has expired. In 10/100 mode, late collisions are counted twice i.e., both as a collision and a late collision.

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45.7.60. ETH Deferred Transmission Frames Register

Name: DTF
Offset: 0x1148
Reset: 0x00000000
Property: Read-only

Table 45-74. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							DEFT[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	DEFT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DEFT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – DEFT[17:0] Deferred Transmission

This register counts the number of frames experiencing deferral due to carrier sense being active on their first attempt at transmission. Frames involved in any collision are not counted nor are frames that experienced a transmit underrun.

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45.7.61. ETH Carrier Sense Errors Register

Name: CSE
Offset: 0x114C
Reset: 0x00000000
Property: Read-only

Table 45-75. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							CSR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	CSR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – CSR[9:0] Carrier Sense Error
This register counts the number of frames transmitted with carrier sense was not seen during transmission or where carrier sense was de-asserted after being asserted in a transmit frame without collision (no underrun). Only incremented in half duplex mode. The only effect of a carrier sense error is to increment this register. The behavior of the other statistics registers is unaffected by the detection of a carrier sense error.

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45.7.62. ETH Octets Received Low Register

Name: ORLO
Offset: 0x1150
Reset: 0x00000000
Property: Read-Only(Cleared on read)

When reading the Octets Transmitted and Octets Received Registers, bits [31:0] should be read prior to bits [47:32] to ensure reliable operation.

Table 45-76. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	RXO[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RXO[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RXO[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RXO[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RXO[31:0] Received Octets
Received octets in frame without errors [31:0]. The number of octets received in valid frames of any type. This counter is 48-bits and is read through two registers. This count does not include octets from pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.63. ETH Octets Received High Register

Name: ORHI
Offset: 0x1154
Reset: 0x00000000
Property: Read-only(Cleared on Read)

When reading the Octets Transmitted and Octets Received Registers, bits 31:0 should be read prior to bits 47:32 to ensure reliable operation.

Table 45-77. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RXO[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RXO[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RXO[15:0] Received Octets
Received octets in frame without errors [47:32]. The number of octets received in valid frames of any type. This counter is 48-bits and is read through two registers. This count does not include octets from pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.64. ETH Frames Received Register

Name: FR
Offset: 0x1158
Reset: 0x00000000
Property: Read-only(Cleared on Read)

Table 45-78. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	FRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	FRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – FRX[31:0] Frames Received without Error
This bit field counts the number of frames successfully received, excluding pause frames. It is only incremented if the frame is successfully filtered and copied to memory.

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45.7.65. ETH Broadcast Frames Received Register

Name: BCFR
Offset: 0x115C
Reset: 0x00000000
Property: Read-only(Cleared on Read)

Table 45-79. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	BFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BFRX[31:0] Broadcast Frames Received without Error
Broadcast frames received without error. This bit field counts the number of broadcast frames successfully received. This excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.66. ETH Multicast Frames Received Register

Name: MFR
Offset: 0x1160
Reset: 0x00000000
Property: Read-only(Cleared on Read)

Table 45-80. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	MFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MFRX[31:0] Multicast Frames Received without Error
This register counts the number of multicast frames successfully received without error, excluding pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.67. ETH Pause Frames Received Register

Name: PFR
Offset: 0x1164
Reset: 0x00000000
Property: -

Table 45-81. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PFRX[15:0] Pause Frames Received Register
This register counts the number of pause frames received without error.

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45.7.68. ETH 64-Byte Frames Received Register

Name: BFR64
Offset: 0x1168
Reset: 0x00000000
Property: Read-only

Table 45-82. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 64-Byte Frames Received without Error
This bit field counts the number of 64-byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.69. ETH 65 to 127 Byte Frames Received Register

Name: TBFR127
Offset: 0x116C
Reset: 0x00000000
Property: -

Table 45-83. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 65 to 127 Byte Frames Received without Error
This bit field counts the number of 65 to 127 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.70. ETH 128 to 255 Byte Frames Received Register

Name: TBFR255
Offset: 0x1170
Reset: 0x00000000
Property: -

Table 45-84. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 128 to 255 Byte Frames Received without Error
This bit field counts the number of 128 to 255 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.71. ETH 256 to 511 Byte Frames Received Register

Name: TBFR511
Offset: 0x1174
Reset: 0x00000000
Property: -

Table 45-85. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 256 to 511 Byte Frames Received without Error
This bit fields counts the number of 256 to 511 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.72. ETH 512 to 1023 Byte Frames Received Register

Name: TBFR1023
Offset: 0x1178
Reset: 0x00000000
Property: -

Table 45-86. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 512 to 1023 Byte Frames Received without Error
This bit field counts the number of 512 to 1023 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.73. ETH 1024 to 1518 Byte Frames Received Register

Name: TBFR1518
Offset: 0x117C
Reset: 0x00000000
Property: -

Table 45-87. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 1024 to 1518 Byte Frames Received without Error
This bit field counts the number of 1024 to 1518 byte frames successfully received without error, i.e., no underrun and not too many retries.

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45.7.74. ETH 1519 to Maximum Byte Frames Received Register

Name: TMXBFR
Offset: 0x1180
Reset: 0x00000000
Property: -

Table 45-88. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 1519 to Maximum Byte Frames Received without Error
This bit field counts the number of 1519 Byte or above frames successfully received without error. Maximum frame size is determined by the Maximum Frame Size bit (MAXFS, 1536 Bytes) or Jumbo Frame Size bit (JFRAME, 10240 Bytes) in the Network Configuration Register (NCFGR). Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

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45.7.75. ETH Undersized Frames Received Register

Name: UFR
Offset: 0x1184
Reset: 0x00000000
Property: -

Table 45-89. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							UFRX[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	UFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – UFRX[9:0] Undersize Frames Received
This bit field counts the number of frames received less than 64 bytes in length (10/100 mode, full duplex) that do not have either a CRC error or an alignment error.

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45.7.76. ETH Oversized Frames Received Register

Name: OFR
Offset: 0x1188
Reset: 0x00000000
Property: -

Table 45-90. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							OFRX[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	OFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – OFRX[9:0] Oversized Frames Received
This pit field counts the number of frames received exceeding 1518 Bytes in length (1536 Bytes if NCFGR.MAXFS is written to '1') but do not have either a CRC error, an alignment error, nor a receive symbol error.

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45.7.77. ETH Jabbers Received Register

Name: JR
Offset: 0x118C
Reset: 0x00000000
Property: -

Table 45-91. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							JRX[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	JRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – JRX[9:0] Jabbers Received
This bit field counts the number of frames received exceeding 1518 Bytes in length (1536 Bytes if NCFGR.MAXFS is written to '1') and have either a CRC error, an alignment error or a receive symbol error.

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45.7.78. ETH Frame Check Sequence Errors Register

Name: FCSE
Offset: 0x1190
Reset: 0x00000000
Property: Read-only

Table 45-92. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							FCKR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	FCKR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – FCKR[9:0] Frame Check Sequence Errors
The register counts frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 Bytes if NCFGR.MAXFS is written to '1'). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes.
This register is incremented for a frame with bad FCS, regardless of whether it is copied to memory due to ignore FCS mode (enabled by writing NCFGR.IRXFCS=1).

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45.7.79. ETH Length Field Frame Errors Register

Name: LFFE
Offset: 0x1194
Reset: 0x00000000
Property: -

Table 45-93. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							LFER[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	LFER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – LFER[9:0] Length Field Frame Errors
This bit field counts the number of frames received that have a measured length shorter than that extracted from the length field (Bytes 13 and 14). This condition is only counted if the value of the length field is less than 0x0600, the frame is not of excessive length and checking is enabled by writing a '1' to the Length Field Error Frame Discard bit in the Network Configuration Register (NCFGR.LFERD).

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45.7.80. ETH Receive Symbol Errors Register

Name: RSE
Offset: 0x1198
Reset: 0x00000000
Property: Read-only

Table 45-94. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							RXSE[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RXSE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – RXSE[9:0] Receive Symbol Errors
This bit field counts the number of frames that had GRXER asserted during reception. For 10/100 mode symbol errors are counted regardless of frame length checks.

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45.7.81. ETH Alignment Errors Register

Name: AE
Offset: 0x119C
Reset: 0x00000000
Property: Read-only

Table 45-95. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							AER[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	AER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – AER[9:0] Alignment Errors
This bit field counts the frames that are not an integral number of bytes long and have bad CRC when their length is truncated to an integral number of Bytes and are between 64 and 1518 Bytes in length (1536 if NCFGR.MAXFS=1). This register is also incremented if a symbol error is detected and the frame is of valid length and does not have an integral number of bytes.

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45.7.82. ETH Receive Resource Errors Register

Name: RRE
Offset: 0x11A0
Reset: 0x00000000
Property: -

Table 45-96. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RXRER[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	RXRER[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RXRER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – RXRER[17:0] Receive Resource Errors

This bit field counts frames that are not an integral number of bytes long and have bad CRC when their length is truncated to an integral number of Bytes and are between 64 and 1518 Bytes in length (1536 if NCFGR.MAXFS=1). This bit field is also incremented if a symbol error is detected and the frame is of valid length and does not have an integral number of Bytes.

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45.7.83. ETH Receive Overruns Register

Name: ROE
Offset: 0x11A4
Reset: 0x00000000
Property: -

Table 45-97. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							RXOVR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RXOVR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – RXOVR[9:0] Receive Overruns
This bit field counts the number of frames that are address recognized but were not copied to memory due to a receive overrun.

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45.7.84. ETH IP Header Checksum Errors Register

Name: IHCE
Offset: 0x11A8
Reset: 0x00000000
Property: -

Table 45-98. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	HCKER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – HCKER[7:0] IP Header Checksum Errors
This register counts the number of frames discarded due to an incorrect IP header checksum, but are between 64 and 1518 Bytes (1536 Bytes if NCFGR.MAXFS=1) and do not have a CRC error, an alignment error, nor a symbol error.

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45.7.85. ETH TCP Checksum Errors Register

Name: TCE
Offset: 0x11AC
Reset: 0x00000000
Property: -

Table 45-99. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	TCKER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TCKER[7:0] TCP Checksum Errors
This register counts the number of frames discarded due to an incorrect TCP checksum, but are between 64 and 1518 Bytes (1536 Bytes if NCFGR.MAXFS=1) and do not have a CRC error, an alignment error, nor a symbol error.

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45.7.86. ETH UDP Checksum Errors Register

Name: UCE
Offset: 0x11B0
Reset: 0x00000000
Property: -

Table 45-100. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	UCKER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – UCKER[7:0] UDP Checksum Errors
This register counts the number of frames discarded due to an incorrect UDP checksum, but are between 64 and 1518 Bytes (1536 Bytes if NCFGR.MAXFS=1) and do not have a CRC error, an alignment error, nor a symbol error.

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45.7.87. ETH 1588 Timer Increment Sub-nanoseconds Register

Name: TISUBN
Offset: 0x11BC
Reset: 0x00000000
Property: -

Table 45-101. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LSBTIR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LSBTIR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – LSBTIR[15:0] Lower Significant Bits of Timer Increment Register
Lower significant bits of Timer Increment Register [15:0], giving a 24-bit timer_increment counter. These bits are the sub-ns value which the 1588 timer will be incremented each clock cycle. Bit n = $2^{(n-16)}$ ns giving a resolution of approximately 15.2E^{-15} sec.

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45.7.88. ETH 1588 Timer Seconds High Register

Name: TSH
Offset: 0x11C0
Reset: 0x00000000
Property: -

Table 45-102. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TCS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TCS[15:0] Timer Count in Seconds
This register is writable. It increments by 1 when the IEEE 1588 nanoseconds counter counts to one second. It may also be incremented when the Timer Adjust Register is written.

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45.7.89. ETH 1588 Timer Sync Strobe Seconds Low Register

Name: TSSSL
Offset: 0x11C8
Reset: 0x00000000
Property: -

Table 45-103. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	VTS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	VTS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	VTS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VTS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – VTS[31:0] Value of Timer Seconds Register Capture
The lowest significant 32-bit value of the Timer Seconds register captured when both CTRLB.TSUINCand CTRLB.TSUMS are zero.

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45.7.90. ETH 1588 Timer Sync Strobe Nanoseconds Register

Name: TSSSN
Offset: 0x11CC
Reset: 0x00000000
Property: -

Table 45-104. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	VTN[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	VTN[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	VTN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VTN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – VTN[31:0] Value of Timer Nanoseconds Register Capture
The value of the Timer Nanoseconds register captured when both CTRLB.TSUINCand CTRLB.TSUMS are zero.

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45.7.91. ETH 1588 Timer Seconds Low Register

Name: TSL
Offset: 0x11D0
Reset: 0x00000000
Property: -

Table 45-105. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	TCS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TCS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TCS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TCS[31:0] Timer Count in Seconds
This register is writable. It increments by 1 when the IEEE 1588 nanoseconds counter counts to one second. It may also be incremented when the Timer Adjust Register is written.

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45.7.92. ETH 1588 Timer Nanoseconds Register

Name: TN
Offset: 0x11D4
Reset: 0x00000000
Property: -

Table 45-106. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			TNS[29:24]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TNS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TNS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TNS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – TNS[29:0] Timer Count in Nanoseconds
This register is writable. It can also be adjusted by writes to the IEEE 1588 Timer Adjust Register. It increments by the value of the IEEE 1588 Timer Increment Register each clock cycle.

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45.7.93. ETH 1588 Timer Adjust Register

Name: TA
Offset: 0x11D8
Reset: 0x00000000
Property: -

Table 45-107. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	ADJ		ITDT[29:24]					
Access	W		W	W	W	W	W	W
Reset	0		0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ITDT[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ITDT[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ITDT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit 31 – ADJ Adjust 1588 Timer
Write as '1' to subtract from the 1588 timer. Write as '0' to add to it.

Bits 29:0 – ITDT[29:0] Increment/Decrement
The number of nanoseconds to increment or decrement the IEEE 1588 Timer Nanoseconds Register. If necessary, the IEEE 1588 Seconds Register will be incremented or decremented.

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45.7.94. ETH IEEE 1588 Timer Increment Register

Name: TI
Offset: 0x11DC
Reset: 0x00000000
Property: -

Table 45-108. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	NIT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ACNS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – NIT[7:0] Number of Increments
The number of increments after which the alternative increment is used.

Bits 15:8 – ACNS[7:0] Alternative Count Nanoseconds
Alternative count of nanoseconds by which the 1588 Timer Nanoseconds Register will be incremented each clock cycle.

Bits 7:0 – CNS[7:0] Count Nanoseconds
A count of nanoseconds by which the IEEE 1588 Timer Nanoseconds Register will be incremented each clock cycle.

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45.7.95. ETH PTP Event Frame Transmitted Seconds Low Register

Name: EFTSL
Offset: 0x11E0
Reset: 0x00000000
Property: Read-only

Table 45-109. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	RUD[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RUD[31:0] Register Update

The register is updated with the value that the IEEE 1588 Timer Seconds Register holds when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.96. ETH PTP Event Frame Transmitted Nanoseconds Register

Name: EFTN
Offset: 0x11E4
Reset: 0x00000000
Property: Read-only

Table 45-110. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			RUD[29:24]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – RUD[29:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Nanoseconds Register holds when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the bit field is updated.

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45.7.97. ETH PTP Event Frame Received Seconds Low Register

Name: EFRSL
Offset: 0x11E8
Reset: 0x00000000
Property: Read-only

Table 45-111. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	RUD[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RUD[31:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Seconds Register holds when the SFD of a PTP receive primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.98. ETH PTP Event Frame Received Nanoseconds Register

Name: EFRN
Offset: 0x11EC
Reset: 0x00000000
Property: Read-only

Table 45-112. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			RUD[29:24]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – RUD[29:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Nanoseconds Register holds when the SFD of a PTP receive primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.99. ETH PTP Peer Event Frame Transmitted Seconds Low Register

Name: PEFTSL
Offset: 0x11F0
Reset: 0x00000000
Property: -

Table 45-113. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	RUD[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RUD[31:0] Register Update

The register is updated with the value that the IEEE 1588 Timer Seconds Register holds when the SFD of a PTP transmit peer event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.100. ETH PTP Peer Event Frame Transmitted Nanoseconds Register

Name: PEFTN
Offset: 0x11F4
Reset: 0x00000000
Property: -

Table 45-114. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			RUD[29:24]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – RUD[29:0] Register Update

The register is updated with the value that the 1588 Timer Nanoseconds Register holds when the SFD of a PTP transmit peer event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.101. ETH PTP Peer Event Frame Received Seconds Low Register

Name: PEFRSL
Offset: 0x11F8
Reset: 0x00000000
Property: -

Table 45-115. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
	RUD[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RUD[31:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Seconds Register holds when the SFD of a PTP receive primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.102. ETH PTP Peer Event Frame Received Nanoseconds Register

Name: PEFRN
Offset: 0x11FC
Reset: 0x00000000
Property: -

Table 45-116. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
			RUD[29:24]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – RUD[29:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Nanoseconds Register holds when the SFD of a PTP receive primary event crosses the MII interface. An interrupt is issued when the register is updated.

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45.7.103. Received LPI Transitions

Name: RLPITR
Offset: 0x1270
Reset: 0x00000000
Property: Read-only

Table 45-117. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RLPITR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RLPITR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RLPITR[15:0] Count of Received LPI Transitions
A count of the number of times there is a transition from receiving normal idle to receiving low power idle.
Cleared on read.

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45.7.104. Received LPI Time

Name: RLPITI
Offset: 0x1274
Reset: 0x00000000
Property: Read-only

Table 45-118. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	RLPITI[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RLPITI[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RLPITI[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – RLPITI[23:0] Time in LPI

This field increments once every 16 MCK cycles when the bit RXLPIS (LPI Indication (bit 7)) is set in the NSR.
Cleared on read.

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45.7.105. Transmit LPI Transitions

Name: TLPITR
Offset: 0x1278
Reset: 0x00000000
Property: Read-only

Table 45-119. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	TLPITR[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TLPITR[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TLPITR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – TLPITR[23:0] Count of LIP Transitions
A count of the number of times the bit TXLPIEN (Enable LPI Transmission (bit 19)) goes from low to high in the NCR.
Cleared on read.

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45.7.106. Transmit LPI Time

Name: TLPITI
Offset: 0x127C
Reset: 0x00000000
Property: Read-only

Table 45-120. Register Bit Attribute Legend

Symbol	Description	Symbol	Description	Symbol	Description
R	Readable bit	**HC**	Cleared by Hardware	(Grey cell)	Unimplemented
W	Writable bit	**HS**	Set by Hardware	**X**	Bit is unknown at Reset
K	Write to clear	**S**	Software settable bit	—	—

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	TLPITI[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TLPITI[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TLPITI[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – TLPITI[23:0] Time in LPI

This field increments once every 16 MCK cycles when the bit TXLPIEN (Enable LPI Transmission (bit 19)) is set in NCR.
Cleared on read.

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46. Quadrature Encoder Interface (QEI)

46.1. Overview

The Quadrature Encoder Interface (QEI) module provides the interface to incremental encoders for obtaining mechanical position data and velocity. Quadrature encoders, also known as incremental encoders or optical encoders, detect position and speed of rotating motion systems. Quadrature encoders enable closed-loop control of motor control applications, such as Switched Reluctance (SR) and AC Induction Motors (ACIM).

A typical quadrature encoder includes a slotted wheel attached to the shaft of the motor and an emitter/detector module that senses the slots in the wheel. Typically, four output channels, Phase A (QEAx), Phase B (QEBx) and Index (INDXx) and Home (HOME) provide information on the movement of the motor shaft, including distance and direction.

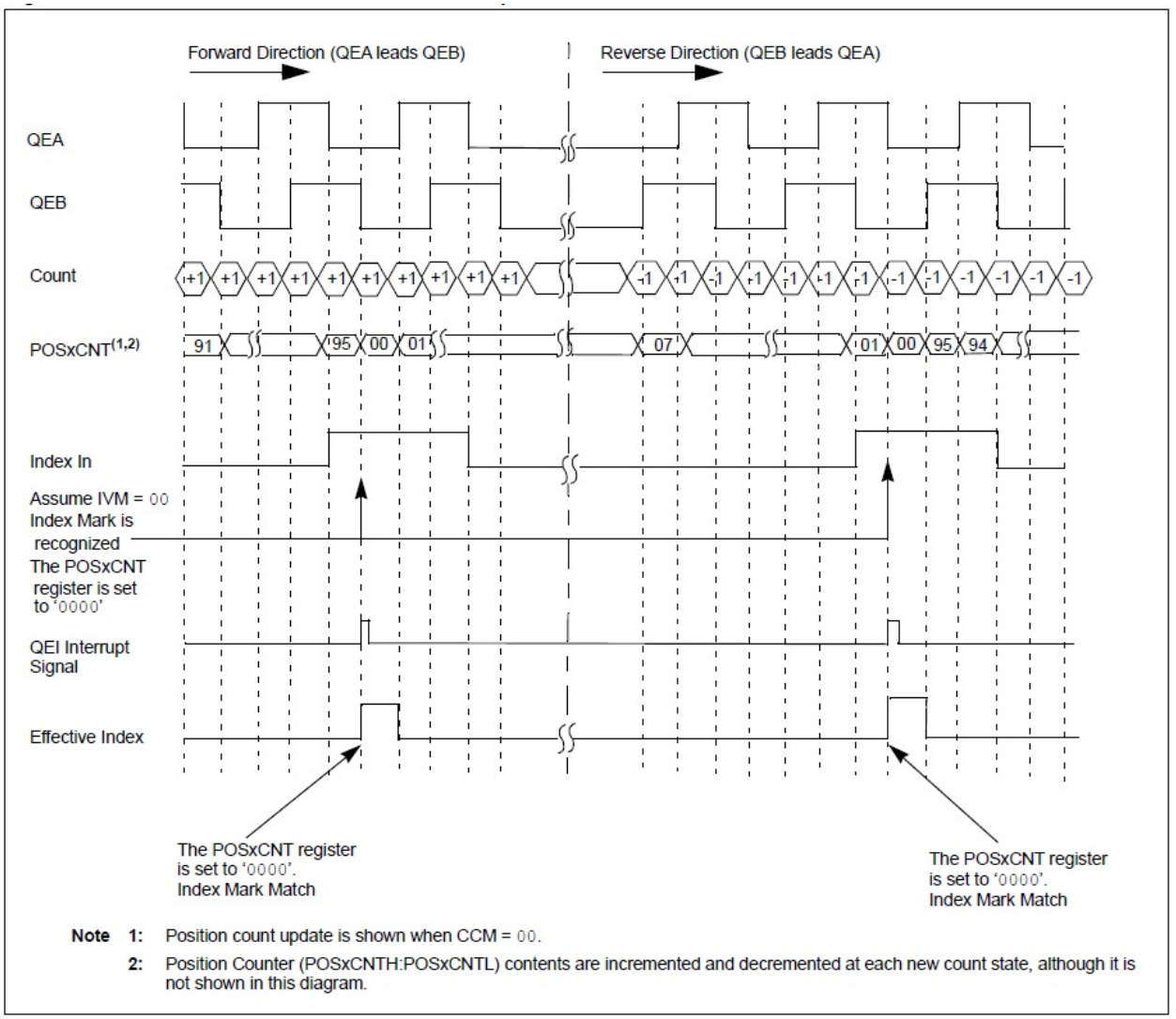
The two channels, Phase A (QEA) and Phase B (QEB), are typically 90º out of phase with respect to each other. The Phase A and Phase B channels have a unique relationship. If Phase A leads Phase B, the direction of the motor is deemed positive or forward. If Phase A lags Phase B, the direction of the motor is deemed negative or reverse. The Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position. The following figure illustrates the Quadrature Encoder Interface signals. On power-up, the machine needs to orient itself to a known reference point. The QEIIC register is loaded with the “home” position. The position counter is configured via the PIMOD bits to initialize the position counter on the first index event following a home event. The home and index events occur and the contents of the QEIIC register are loaded into the Position Counter (POSCNT) register.

The quadrature signals from the encoder can have four unique states (‘01’, ‘00’, ‘10’ and ‘11’) that reflect the relationship between QEA and QEB. The following figure illustrates these states for one count cycle. The order of the states get reversed when the direction of travel changes.

The quadrature decoder increments or decrements the 32-bit up/down Position Counter (POSxCNT) for each Change-of-State (COS). The counter increments when QEA leads QEB and decrements when QEB leads QEA.

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Figure 46-1. Quadrature Encoder Interface Signals



The following table shows the truth table that describes how the quadrature signals are decoded.

Table 46-1. Truth Table for Quadrature Encoder

Current Quadrature State		Previous Quadrature State		Action
QEA	QEB	QEA	QEB	
1	1	1	1	No count or direction change
1	1	1	0	Count up
1	1	0	1	Count down
1	1	0	0	Invalid state change, ignore
1	0	1	1	Count down
1	0	1	0	No count or direction change
1	0	0	1	Invalid state change, ignore
1	0	0	0	Count up
0	1	1	1	Count up
0	1	1	0	Invalid state change, ignore
0	1	0	1	No count or direction change

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Table 46-1. Truth Table for Quadrature Encoder (continued)

Current Quadrature State		Previous Quadrature State		Action
QEA	QEB	QEA	QEB	
0	1	0	0	Count down
0	0	1	1	Invalid state change, ignore
0	0	1	0	Count down
0	0	0	1	Count up
0	0	0	0	No count or direction change

Block Diagram illustrates the simplified block diagram of the QEI module. The QEI module consists of decoder logic to interpret the Phase A (QEA) and Phase B (QEB) signals, and an Up/Down Counter to accumulate the count. The counter pulses are generated when the quadrature state changes. The count direction information must be maintained in a register until a direction change is detected. The module also includes digital noise filters, which condition the input signal.

46.2. Features

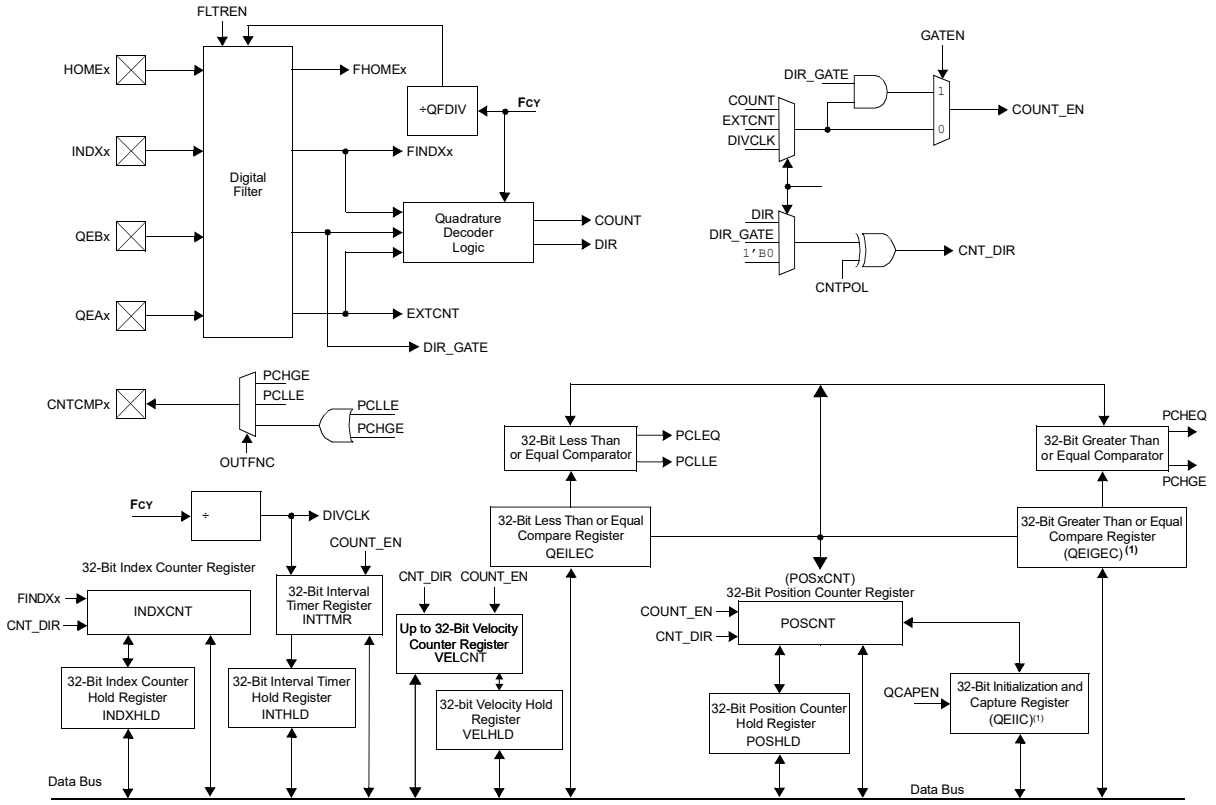
The QEI module consists of the following major features:

- 32-bit Position Counter
- 32-bit Index Pulse Counter
- 32-bit Interval Timer
- 32-bit Velocity Counter
- 32-bit Position Initialization/Capture/Compare High Register
- 32-bit Position Compare Low Register
- 4x Quadrature Count Mode
- External Up/Down Count Mode
- External Gated Count Mode
- External Gated Timer mode
- Interval Timer Mode

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46.3. Block Diagram

Figure 46-2. Quadrature Encoder Interface (QEI) Module Block Diagram



Note:

1. These registers map to the same memory location.

46.4. Module Description

46.4.1. Position Counter

The position counter is 32 bits wide and is contained in the POSxCNT register. The counter counts the number of pulses generated by an encoder.

If the POSOVIEN bit (QEIxSTAT<8>) is set, and the position counter rolls over from 0x7FFFFFFF to 0x80000000, or from 0x80000000 to 0x7FFFFFFF, an interrupt will be generated.

The operating mode of the position counter is controlled by the CCM<1:0> bits (QEIxCON<1:0>). The position counter supports the following operating modes:

- Quadrature Count Mode
- External Count with External Up/Down Mode
- External Count with External Gate Mode
- Internal Timer with External Gate Mode

46.4.1.1. Quadrature Count Mode

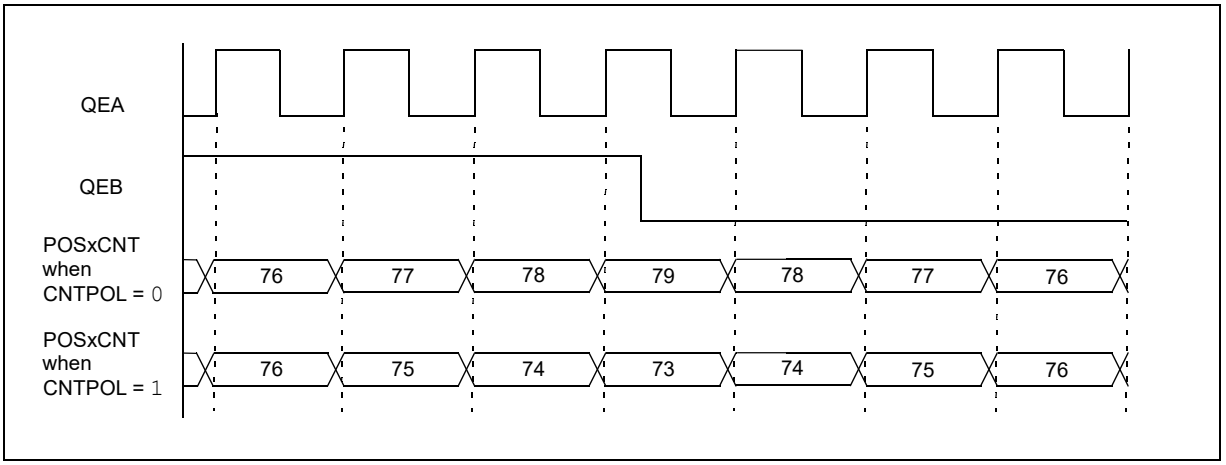
In this mode, the QEA/EXTCNT and QEB/DIR/GATE inputs are decoded to generate count pulses and direction information to control the POSxCNT and VELxCNT registers. The INDXxCNTregister counts when a valid edge is detected on INDX input. Figure 46-1 illustrates the timing diagram of the Quadrature Count mode operation.

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46.4.1.2. External Count with External Up/Down Mode

In this mode, the QEA/EXTCNT input is considered as an external count signal, and the QEB/DIR/GATE input provides the count direction information. The count direction is positive unless overridden by the CNTPOL bit (QEIxCON<3>). The following figure illustrates the timing diagram of an External Count with External Up/Down mode operation.

Figure 46-3. External Count with External Up/Down Mode

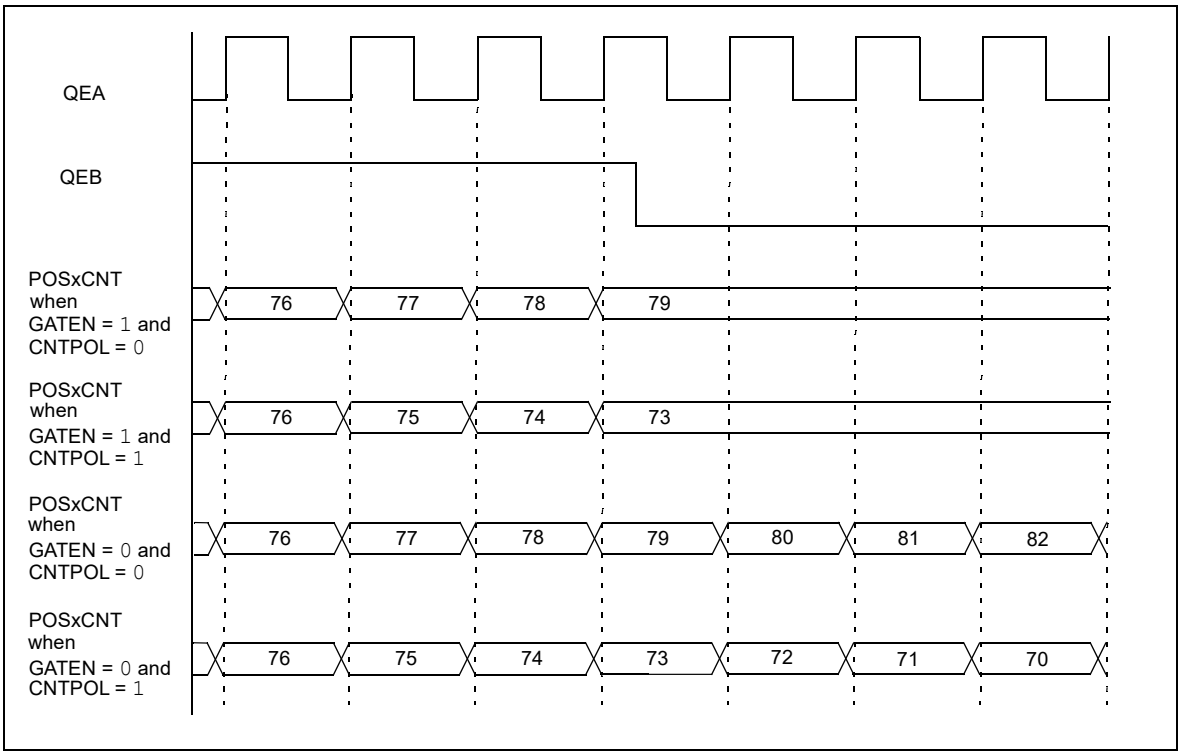


46.4.1.3. External Count with External Gate Mode

In this mode, the QEA/EXTCNT input is considered as an external count signal. If the GATEN bit (QEIxCON<2>) is set, and QEB/DIR/GATE = 0, the QEB/DIR/GATE input will inhibit the counter signal. If the GATEN bit is cleared, the gate signal does not affect the counter operation. The default count direction is positive. If the CNTPOL bit (QEIxCON<3>) is set, the count direction is negative. The following figure illustrates the timing diagram of an External Count with External Gate mode operation.

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Figure 46-4. External Count with External Gate Mode

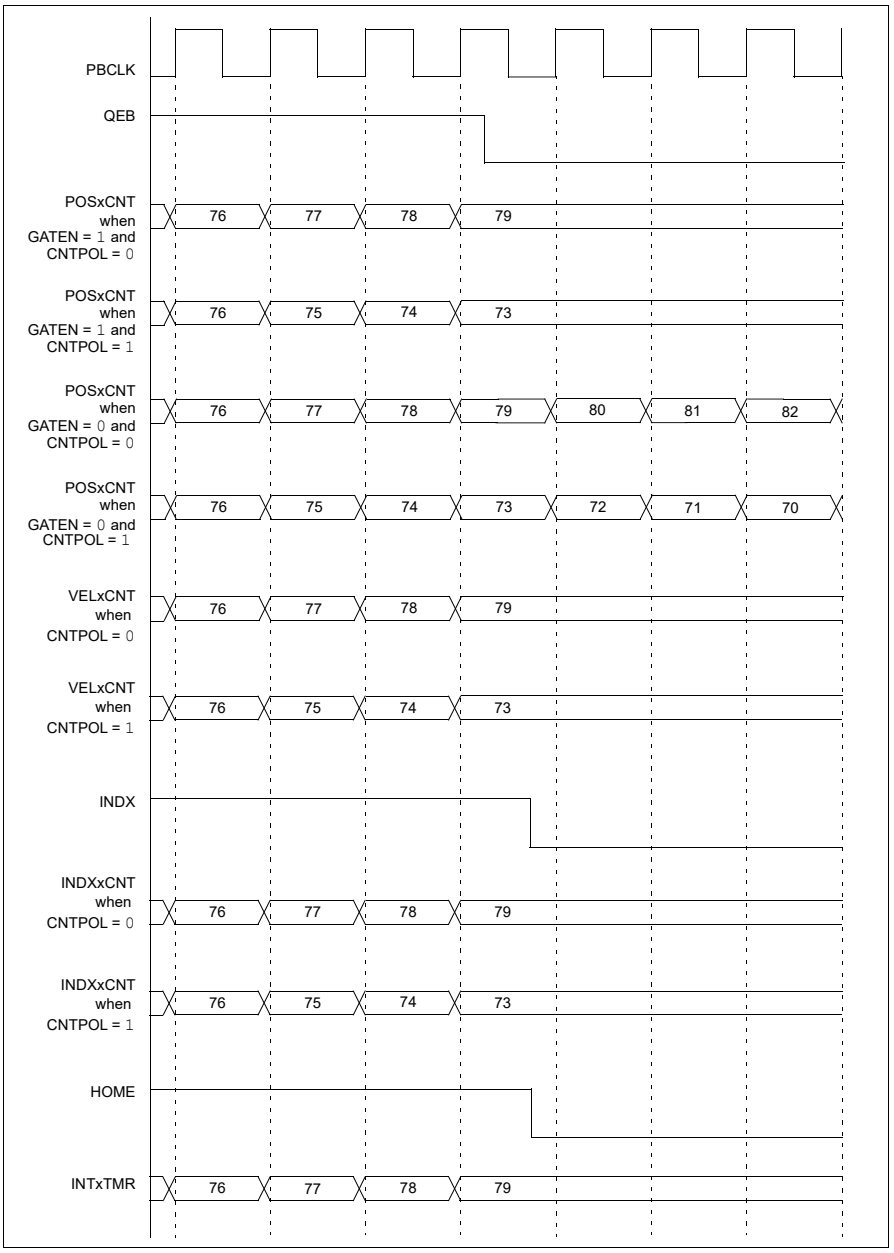


46.4.1.4. Internal Timer with External Gate Mode

In this mode, the velocity, index and interval counter of the position counter uses an internal clock as the count source. The internal clock is divided by the clock divider using the INTDIV<2:0> bits (QEIxCON<6:4>). If the GATEN bit (QEIxCON<2>) is set, and QEB/DIR/GATE = 0, the QEB/DIR/GATE input will inhibit the counter signal. If the GATEN bit is cleared, the gate signal does not affect the operation of the counter. The default count direction is positive. If the CNTPOL bit (QEIxCON<3>) is set, the count direction is negative. The following figure illustrates the timing diagram of an Internal Timer mode operation.

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Figure 46-5. Internal Timer Mode



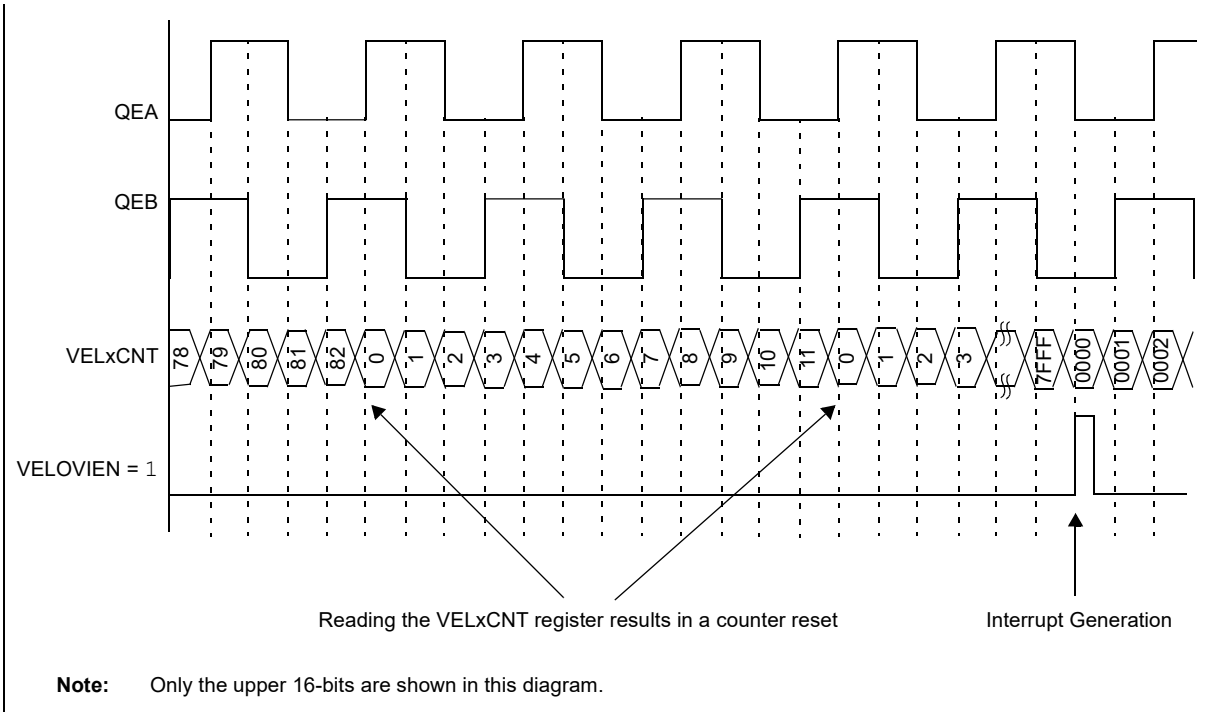
46.4.2. Velocity Counter

The 32-bit wide Velocity Counter (VELxCNT) register increments or decrements based on the signal from the quadrature decoder logic. Reading this register resets the register. The index input or any of the modes specified by the PIMOD<2:0> bits (QEIxCON<12:10>) does not affect the operation of the velocity counter. If the velocity counter rolls over from 0x7FFFFFFF to 0x80000000, or from 0x80000000 to 0x7FFFFFFF, and the VELOVIEN bit (QEIxSTAT<4>) is set, an interrupt will be generated. The following figure illustrates the timing diagram of the Velocity Counter operation

Note: The velocity counter specifies the distance traveled between the time interval of each sample. Reading the VELxCNT register results in counter reset. The user application should read the velocity counter at a rate of 1 kHz to 4 kHz.

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Figure 46-6. Velocity Counter



Note: Only the upper 16-bits are shown in this diagram.

46.4.3. Index Counter

The 32-bit wide Index Counter (INDXxCNT) register counts index events. It is incremented or decremented based on the direction output of the quadrature logic decoder (see Figure 46-2). For more information, refer to Index Event.

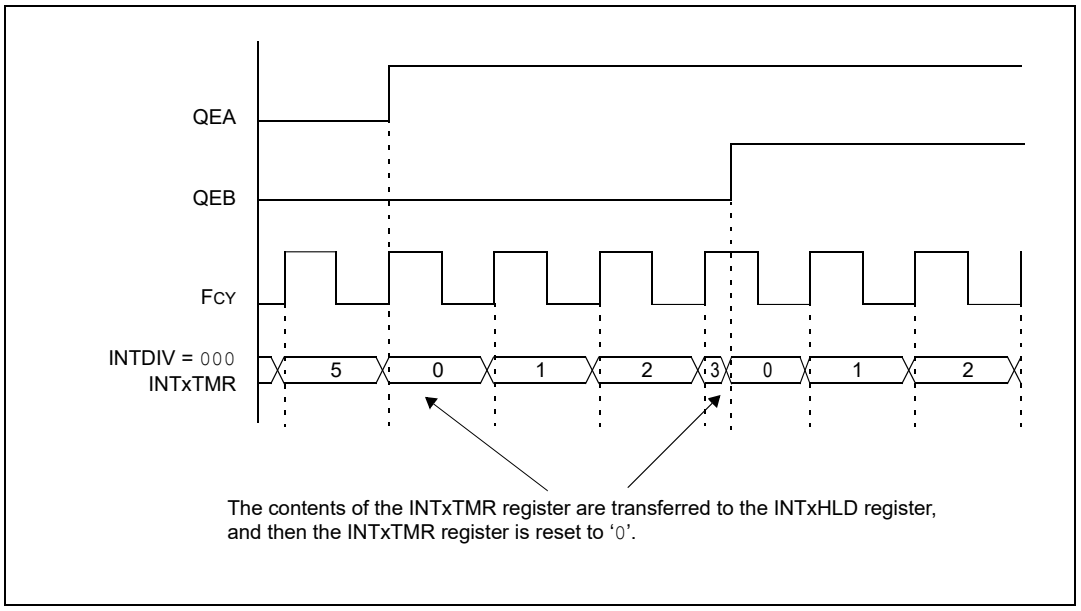
46.4.4. Interval Timer

When a motor runs at a very low speed, the encoder does not generate enough pulses for accurate speed measurement. Therefore, instead of counting the number of pulses, the pulse duration can be measured. The 32-bit Interval Timer (INTxTMR) register is used to measure the time interval between each decoded quadrature count pulse when the motor operates at a very low speed. The timer counts at a rate specified by the INTDIV<2:0> bits (QEIxCON<6:4>). The interval timer is cleared when the first count pulse is detected. When the next count pulse is detected, the current contents of the interval timer are transferred to the Interval Timer Hold (INTxHLD) register, the interval timer is cleared, and then the process repeats. The interval timer hold registers always contain the most recent completed timing measurements. The following figure illustrates the timing diagram of the Interval Timer operation.

Note: If the INTxHLD register is read when a new position count pulse is detected, the contents of the INTxHLD register are not updated to avoid incoherent data reading.

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Figure 46-7. Interval Timer



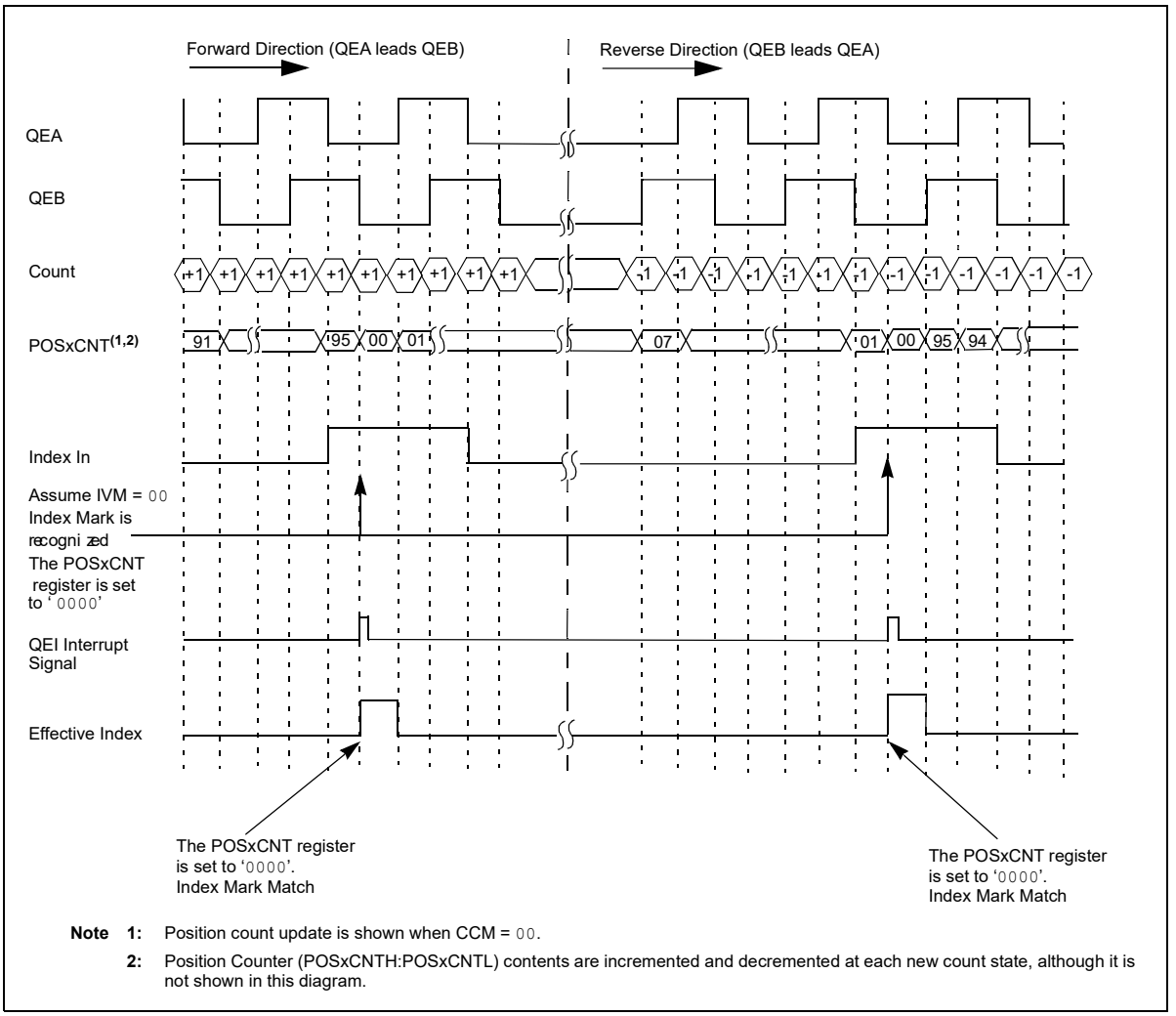
46.4.5. Initialization/Capture Register

The 32-bit general purpose Initialization/Capture (QEIxIC) register can be used to initialize the position counter and capture the contents of the position counter. The QEIxIC register can perform only one of these tasks at a time, but the mode of operation may be changed during operation. Typical application examples include:

- On power-up, the machine needs to orient itself to a known reference point. The QEIxIC register is loaded with the "home" position. The position counter is configured via the PIMOD bits to initialize the position counter on the first index event following a home event. The home and index events occur and the contents of the QEIxIC register are loaded into the Position Counter (POSxCNT) register.
- A user connects a "Touch Probe" to the machine via the "HOME" input to measure a previously machined item. The machine scans the item in a pattern, constantly moving the machine until a probe contact occurs. The probe contact causes the QEIxIC register to capture the position. The position information is then relayed to another computer for analysis.

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Figure 46-8. Index Reset Position Counter Operation



Note 1: Position count update is shown when CCM = 00.

2: Position Counter (POSxCNTH:POSxCNTL) contents are incremented and decremented at each new count state, although it is not shown in this diagram.

46.4.6. Position Comparator

The QEIxCMPL and QEIxICC registers and the associated comparator provide the ability to compare the contents of the Position Counter (POSxCNT) register to a specified value. The comparator provides two outputs: equality detect, and less than or greater than detect. The comparator equality output can be enabled to generate interrupts via the PCLEQIEN bit (QEIxSTAT<10>). The less than or equal, or greater than or equal output can be output on a device pin. The selection is made by setting the OUTFNC<1:0> bits (QEIxIOC<10:9>). The comparator output can be used to detect an illegal move operation by an end user and the comparator output can be connected to appropriate external circuitry to prevent the illegal move.

Sometimes, the potential for costly damage to a part, or a machine due to an operator, programming,or a machine failure is too much to accept. The QEIxCMPL and QEIxICC registers can be configured to define a bounds of travel beyond which a Fault is generated. The values in these registers are continually compared to the position counter. The comparator output can be directed to a device pin. This Fault detected signal can be used to shut down the machine operation to prevent damage or injury.

The comparator can also be used to reset the position counter when a match is detected. Figure 46-8, on the previous page, illustrates the index reset position counter operation.

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46.4.7. Index Event

The IMV<1:0> bits (QEIxCON<9:8>) specify the state of the QEA and QEB input signals required to acknowledge an index event. An index event is accepted when an index pulse occurs while the value of the QEA and QEB inputs match the condition set in the IMV<1:0> bits. This prevents further index events from being accepted until the index input signal is deasserted, and ensures that only one index event occurs for each index input pulse. Figure 46-8, on the previous page, illustrates the index reset position counter operation.

46.4.8. Position Counter Initialization Modes

By using the PIMOD<2:0> bits (QEIxCON<12:10>), the user application can specify how the position counter is initialized during the module operation.

- **Mode0** – The position counter is unaffected by the index input.
- **Mode1** –The position counter is cleared whenever an index input event is detected.
- **Mode2** –The position counter is initialized with the contents of the QEIxICC register on the next detected index input event. When the index event occurs, the PIMOD<2:0> bits are cleared, and then the counter operates in Mode 0.
- **Mode3** –The position counter is initialized with the contents of the QEIxICC register on the next detected index input event following the assertion of the home input. When an index event occurs following the home event, the PIMOD<2:0> bits are cleared, and then the counter operates in Mode 0.
- **Mode4** –The position counter is initialized with the contents of the QEIxICC register on the second detected index input event following the assertion of the home input. When the second index event occurs following the home event, the PIMOD<2:0> bits are cleared, and then the counter operates in Mode 0.
- **Mode5** –The position counter is cleared when the position counter value equals the QEIxICC register value.
- **Mode6** –The position counter is loaded with the contents of the QEIxCMPL register when the position counter value equals the QEIxICC register value and a count up pulse is detected. The counter is loaded with the contents of the QEIxICC register when the position counter value equals the QEIxCMPL register value and a count down pulse is detected.
- **Mode7** – Same as mode 6, with the additional feature of the position counter being cleared whenever an index input event is detected

46.4.9. Digital Input Filter

The QEI module uses digital noise filters to reject noise on the incoming index and quadrature phase signals. These filters reject low-level noise and large, short duration noise spikes that typically occur in motor systems.

The filtered output signals can change only after an input level has the same value for three consecutive rising clock edges. The result is that short noise spikes between rising clock edges are ignored, and pulses shorter than two clock periods are rejected.

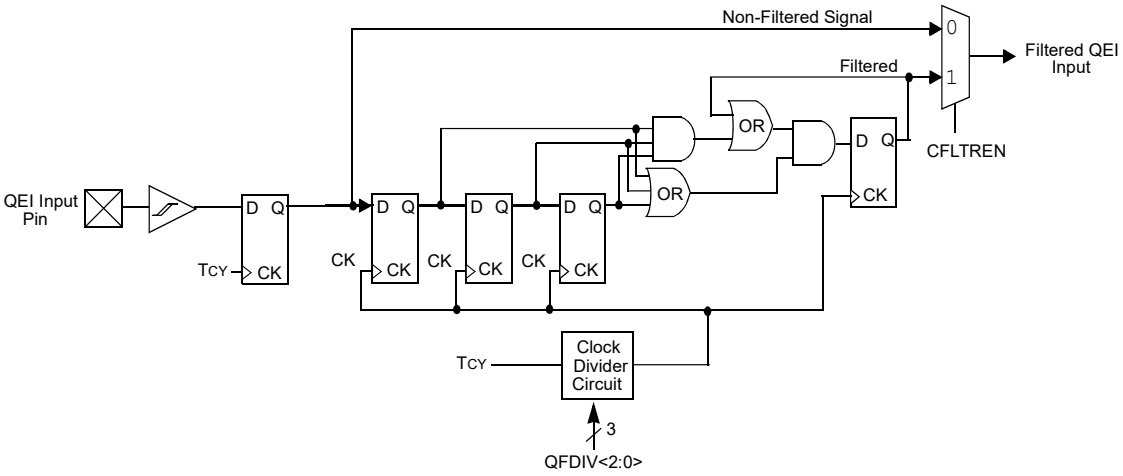
The filter clocks rate determines the low passband of the filter. A slower filter clock results in a passband rejecting lower frequencies.

The digital filter is enabled by setting the FLTREN bit (QEIxIOC<14>). The QFDIV<2:0> bits (QEIxIOC<13:11>) select the filter clock divider ratio for the clock signal.

The following figure illustrates the simplified block diagram of the digital noise filter.

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Figure 46-9. Block Diagram of Digital Noise Filter



Note: The digital filter clock frequency should be at least eight times greater than the maximum count rate.

46.4.10. Interrupts

The following are the sources of QEI interrupts:

- Position counter overflow or underflow event
- Velocity counter overflow or underflow event
- Position counter initialization process complete
- Position counter greater than or equal compare interrupt
- Position counter less than or equal compare interrupt
- Index event interrupt
- Home event interrupt

The QEIx Status (QEIxSTAT) register contains the individual interrupt enable bits and the corresponding interrupt status bits for each interrupt source. A status bit indicates that an interrupt request has occurred. The module reduces all of the QEI interrupts to a single interrupt signal to the interrupt controller module.

46.5. QEI Operation in Power-Saving Modes

46.5.1. Sleep Mode

When the device enters Sleep mode, QEI operations cease. The POSxCNT register stops at the current value. The QEI does not respond to active signals on the QEA, QEB or INDX pins. The QEIxCON register remains unchanged.

46.5.2. Idle Mode

When the device enters Idle mode, the QEISIDL bit (QEIxCON<13>) determines whether the QEI module stops in Idle mode or continues to operate in Idle mode.

If QEISIDL = 1, the QEI module enters into a power-saving mode and performs the same functions as in Sleep mode. If QEISIDL = 0, the module does not enter into a power-saving mode and continues operation in Idle mode.

46.6. QEI Registers

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46.6.1. Register Summary

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See CLR, SET, and INV Registers from Related Links.

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	QEICON	7:0			INTDIV[2:0]		CNTPOL	GATEN	CCM[1:0]	
		15:8	QEIEN		QEISIDL		PIMOD[2:0]		IMV[1:0]	
		23:16								
		31:24								
0x04 ... 0x0F	Reserved									
0x10	QEIIOC	7:0	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
		15:8	QCAPEN	FLTREN	QFDIV[2:0]			OUTFNC[1:0]		SWPAB
		23:16								HCAPEN
		31:24								
0x14 ... 0x1F	Reserved									
0x20	QEISTAT	7:0	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
		15:8			PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
		23:16								
		31:24								
0x24 ... 0x2F	Reserved									
0x30	POSCNT	7:0	POSCNT[7:0]							
		15:8	POSCNT[15:8]							
		23:16	POSCNT[23:16]							
		31:24	POSCNT[31:24]							
0x34 ... 0x3F	Reserved									
0x40	POSHLD	7:0	POSHLD[7:0]							
		15:8	POSHLD[15:8]							
		23:16	POSHLD[23:16]							
		31:24	POSHLD[31:24]							
0x44 ... 0x4F	Reserved									
0x50	VELCNT	7:0	VELCNT[7:0]							
		15:8	VELCNT[15:8]							
		23:16	VELCNT[23:16]							
		31:24	VELCNT[31:24]							
0x54 ... 0x5F	Reserved									
0x60	VELHLD	7:0	VEL_HLD[7:0]							
		15:8	VEL_HLD[15:8]							
		23:16	VEL_HLD[23:16]							
		31:24	VEL_HLD[31:24]							
0x64 ... 0x6F	Reserved									
0x70	INTTMR	7:0	INTTMR[7:0]							
		15:8	INTTMR[15:8]							
		23:16	INTTMR[23:16]							
		31:24	INTTMR[31:24]							
0x74 ... 0x7F	Reserved									

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Register Summary (continued)

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x80	INTHLD	7:0	INTHLD[7:0]							
		15:8	INTHLD[15:8]							
		23:16	INTHLD[23:16]							
		31:24	INTHLD[31:24]							
0x84 ... 0x8F	Reserved									
0x90	INDXCNT	7:0	INDXCNT[7:0]							
		15:8	INDXCNT[15:8]							
		23:16	INDXCNT[23:16]							
		31:24	INDXCNT[31:24]							
0x94 ... 0x9F	Reserved									
0xA0	INDXHLD	7:0	INDXHLD[7:0]							
		15:8	INDXHLD[15:8]							
		23:16	INDXHLD[23:16]							
		31:24	INDXHLD[31:24]							
0xA4 ... 0xAF	Reserved									
0xB0	QEIICC	7:0	ICCH[7:0]							
		15:8	ICCH[15:8]							
		23:16	ICCH[23:16]							
		31:24	ICCH[31:24]							
0xB4 ... 0xBF	Reserved									
0xC0	QEICMPL	7:0	CMPL[7:0]							
		15:8	CMPL[15:8]							
		23:16	CMPL[23:16]							
		31:24	CMPL[31:24]							

Related Links

CLR, SET and INV Registers

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46.6.1.1. QEI Control Register

Name: QEICON
Offset: 0x00000000
Reset: 0x00000000

Notes:

1. When CCMx = 01, CCMx = 10 or CCMx = 11, all of the QEI Counters operate as timers and the PIMOD[2:0] bits are ignored.
2. When CCMx = 00, and QEA and QEB values match the Index Match Value (IMV), the POSxCNTH and POSxCNTL registers are reset.
3. The selected clock rate should be at least twice the expected maximum quadrature count rate.
4. The QCAPEN and HCAPEN bits must be cleared during PIMOD modes 2 though 7 to insure proper functionality.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	QEIEN		QEISIDL	PIMOD[2:0]			IMV[1:0]	
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		INTDIV[2:0]			CNTPOL	GATEN	CCM[1:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit 15 – QEIEN Quadrature Encoder Interface Module Counter Enable bit

Value	Description
1	Module counters are enabled
0	Module counters are disabled, but SFRs can be read or written

Bit 13 – QEISIDL QEI Stop in Idle Mode bit

Value	Description
1	Discontinues module operation when device enters Idle mode
0	Continues module operation in Idle mode

Bits 12:10 – PIMOD[2:0] Position Counter Initialization Mode Select bits(1)

Value	Description
111	Modulo Count mode for position counter and every Index input event resets the position counter
110	Modulo Count mode for position counter
101	Position counter equals ICC register resets the position counter
100	Second Index event after Home event initializes position counter with contents of QEIxIC register

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Value	Description
011	First Index event after Home event initializes position counter with contents of QEIxIC register
010	Next index input event initializes the position counter with contents of QEIxIC register
001	Every index input event resets the position counter
000	Index input event does not affect position counter

Bits 9:8 – IMV[1:0] Index Match Value bits(2)

Value	Description
11	Index match occurs when QEB = 1 and QEA = 1
10	Index match occurs when QEB = 1 and QEA = 0
01	Index match occurs when QEB = 0 and QEA = 1
00	Index match occurs when QEB = 0 and QEA = 0

Bits 6:4 – INTDIV[2:0] Timer Input Clock Prescale Select bits(3)
(Interval Timer, Main Timer (Position Counter), Velocity Counter and Index Counter internal clock divider select)

Value	Description
111	1:128 prescale value
110	1:64 prescale value
101	1:32 prescale value
100	1:16 prescale value
011	1:8 prescale value
010	1:4 prescale value
001	1:2 prescale value
000	1:1 prescale value

Bit 3 – CNTPOL Position and Index Counter/Timer Direction Select bit

Value	Description
1	Counter direction is negative unless modified by external up/down signal
0	Counter direction is positive unless modified by external up/down signal

Bit 2 – GATEN External Count Gate Enable bit

Value	Description
1	External gate signal controls Position Counter operation
0	External gate signal does not affect Position Counter/timer operation

Bits 1:0 – CCM[1:0] Counter Control Mode Selection bits

Value	Description
11	Internal Timer mode
10	External Clock Count with External Gate mode
01	External Clock Count with External Up/Down mode
00	Quadrature Encoder mode

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46.6.1.2. QEI I/O Control Register

Name: QEIIOC
Offset: 0x10
Reset: 0x00000000
Property: RW

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								R/W
Reset								0

Bit	15	14	13	12	11	10	9	8
	QCAPEN	FLTREN	QFDIV[2:0]			OUTFNC[1:0]		SWPAB
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	HOMPOL	IDXPOL	QEBPOL	QEAPOL	HOME	INDEX	QEB	QEA
Access	R/W	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 16 – HCAPEN Position Counter Input Capture by Home Event Enable bit

Value	Description
1	HOMEx input event (positive edge) triggers a position capture event
0	HOMEx input event (positive edge) does not trigger a position capture event

Bit 15 – QCAPEN Position Counter Input Capture Enable bit

Value	Description
1	Positive edge detect of Home input triggers position capture function
0	Home input event (positive edge) does not trigger a capture even

Bit 14 – FLTREN QEA/QEB/INDX/HOMEx Digital Filter Enable bit

Value	Description
1	Input pin digital filter is enabled
0	Input pin digital filter is disabled (bypassed)

Bits 13:11 – QFDIV[2:0] QEA/QEB/INDX/HOMEx Digital Input Filter Clock Divide Select bits

Value	Description
111	1:128 clock divide
110	1:64 clock divide
101	1:32 clock divide
100	1:16 clock divide
011	1:8 clock divide
010	1:4 clock divide
001	1:2 clock divide

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Value	Description
000	1:1 clock divide

Bits 10:9 – OUTFNC[1:0] QEI Module Output Function Mode Select bits

Value	Description
11	The CNTCMPx pin goes high when POSxCNT ≤ QEIxCMPL or POSxCNT ≥ QEIxICCH
10	The CNTCMPx pin goes high when POSxCNT ≤ QEIxCMPL
01	The CNTCMPx pin goes high when POSxCNT ≥ QEIxICCH
00	Output is disabled

Bit 8 – SWPAB Swap QEA and QEB Inputs bit

Value	Description
1	QEAx and QEBx are swapped prior to quadrature decoder logic
0	QEAx and QEBx are not swapped

Bit 7 – HOMPOL HOME Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 6 – IDXPOL INDX Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 5 – QEBPOL QEB Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 4 – QEAPOL QEA Input Polarity Select bit

Value	Description
1	Input is inverted
0	Input is not inverted

Bit 3 – HOME Status of HOME Input Pin After Polarity Control bit (read-only)

Value	Description
1	Pin is at logic '1', if HOMPOL bit is set to '0' Pin is at logic '0', if HOMPOL bit is set to '1'
0	Pin is at logic '0', if HOMPOL bit is set to '0' Pin is at logic '1', if HOMPOL bit is set to '1'

Bit 2 – INDEX Status of INDX Input Pin After Polarity Control bit (read-only)

Value	Description
1	Pin is at logic '1', if IDXPOL bit is set to '0' Pin is at logic '0', if IDXPOL bit is set to '1'
0	Pin is at logic '0', if IDXPOL bit is set to '0' Pin is at logic '1', if IDXPOL bit is set to '1'

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Bit 1 – QEB Status of QEB Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)

Value	Description
1	Physical pin QEBx is at logic '1', if QEBPOL bit is set to '0' and SWPAB bit is set to '0'
	Physical pin QEBx is at logic '0', if QEBPOL bit is set to '1' and SWPAB bit is set to '0'
	Physical pin QEAx is at logic '1', if QEBPOL bit is set to '0' and SWPAB bit is set to '1'
	Physical pin QEAx is at logic '0', if QEBPOL bit is set to '1' and SWPAB bit is set to '1'
0	Physical pin QEBx is at logic '0', if QEBPOL bit is set to '0' and SWPAB bit is set to '0'
	Physical pin QEBx is at logic '1', if QEBPOL bit is set to '1' and SWPAB bit is set to '0'
	Physical pin QEAx is at logic '0', if QEBPOL bit is set to '0' and SWPAB bit is set to '1'
	Physical pin QEAx is at logic '1', if QEBPOL bit is set to '1' and SWPAB bit is set to '1'

Bit 0 – QEA Status of QEA Input Pin After Polarity Control and SWPAB Pin Swapping bit (read-only)

Value	Description
1	Physical pin QEAx is at logic '1', if QEAPOL bit is set to '0' and SWPAB bit is set to '0'
	Physical pin QEAx is at logic '0', if QEAPOL bit is set to '1' and SWPAB bit is set to '0'
	Physical pin QEBx is at logic '1', if QEAPOL bit is set to '0' and SWPAB bit is set to '1'
	Physical pin QEBx is at logic '0', if QEAPOL bit is set to '1' and SWPAB bit is set to '1'
0	Physical pin QEAx is at logic '0', if QEAPOL bit is set to '0' and SWPAB bit is set to '0'
	Physical pin QEAx is at logic '1', if QEAPOL bit is set to '1' and SWPAB bit is set to '0'
	Physical pin QEBx is at logic '0', if QEAPOL bit is set to '0' and SWPAB bit is set to '1'
	Physical pin QEBx is at logic '1', if QEAPOL bit is set to '1' and SWPAB bit is set to '1'

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46.6.1.3. QEI Status Register

Name: QEISTAT
Offset: 0x20
Reset: 0x00000000
Property: R/W

Note:

1. This status bit is only applicable to PIMOD[2:0] modes, '011' and '100'.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
Access			RC	R/W	RC	R/W	RC	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PCIIRQ	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 13 – PCHEQIRQ Position Counter Greater Than or Equal Compare Status bit

Value	Description
1	POSxCNT > QEIxICCH
0	POSxCNT ≤ QEIxICCH

Bit 12 – PCHEQIEN Position Counter Greater Than or Equal Compare Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 11 – PCLEQIRQ Position Counter Less Than or Equal Compare Status bit

Value	Description
1	POSxCNT < QEIxCMPL
0	POSxCNT ≥ QEIxCMPL

Bit 10 – PCLEQIEN Position Counter Less Than or Equal Compare Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 9 – POSOVIRQ Position Counter Overflow Status bit

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Value	Description
1	Overflow has occurred
0	No overflow has occurred

Bit 8 – POSOVIEN Position Counter Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 7 – PCIIRQ Position Counter (Homing) Initialization Process Complete Status bit(1)

Value	Description
1	POSxCNT was reinitialized
0	POSxCNT was not reinitialized

Bit 6 – PCIIEN Position Counter (Homing) Initialization Process Complete Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 5 – VELOVIRQ Velocity Counter Overflow Status bit

Value	Description
1	Overflow has occurred
0	No overflow has occurred

Bit 4 – VELOVIEN Velocity Counter Overflow Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 3 – HOMIRQ Status Flag for Home Event Status bit

Value	Description
1	Home event has occurred
0	No Home event has occurred

Bit 2 – HOMIEN Home Input Event Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

Bit 1 – IDXIRQ Status Flag for Index Event Status bit

Value	Description
1	Index event has occurred
0	No Index event has occurred

Bit 0 – IDXIEN Index Input Event Interrupt Enable bit

Value	Description
1	Interrupt is enabled
0	Interrupt is disabled

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46.6.1.4. Position Counter Word Register

Name: POSCNT
Offset: 0x30
Reset: 0x00000000
Property: RW

Bit	31	30	29	28	27	26	25	24
	POSCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POSCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POSCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POSCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POSCNT[31:0] 32-Bit Position Counter Register (POSxCNT) bits
The Operating mode of the position counter is controlled by the CCM bit in the QEIxCON register.
Quadrature Count mode: The QEA and QEB inputs are decoded to generate count pulses and direction information for controlling the position counter operation.
External Count with External Up/Down mode: The QEA/EXTCNT input is treated as an external count signal, and the QEB/DIR/GATE input provides the count direction information.
External Count with External Gate mode: The QEA/EXTCNT input is treated as an external count signal. If the GATEN bit in the QEIxCON register is equal to '1', the QEB/DIR/GATE input will gate the counter signal.
Internal Timer mode: The position counter uses PBCLK2 divided by the clock divider INTDIV as the count source.

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46.6.1.5. Position Counter Hold Register

Name: POSHLD
Offset: 0x40
Reset: 0x00000000
Property: RW

Bit	31	30	29	28	27	26	25	24
	POSHLD[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	POSHLD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	POSHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	POSHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – POSHLD[31:0] Hold Register for Reading and Writing Position Counter Register (POSxCNT) bits

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46.6.1.6. Velocity Counter Register

Name: VELCNT
Offset: 0x50
Reset: 0x00000000
Property: RW

Bit	31	30	29	28	27	26	25	24
	VELCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	VELCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	VELCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VELCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – VELCNT[31:0] 32-bit Velocity Counter bits

The velocity counter is automatically cleared after every processor read of the velocity counter. It is not reset by the index input or otherwise affected by any of the PIMOD[2:0] specified modes. The contents of the counter represents the distance traveled during the time between samples. Velocity equals the distance traveled per unit of time. The velocity counter can save the application software the trouble of performing 32-bit math operations between current and previous position counter values to calculate velocity. If the velocity counter rolls over from 0x7FFFFFFF to 0x80000000, or from 0x80000000 to 0x7FFFFFFF, an overflow/underflow condition is detected. If the VELOVIEN bit is set in the QEISTAT register, an interrupt will be generated.

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46.6.1.7. Velocity Counter Holding Register

Name: VELHLD
Offset: 0x60
Reset: 0x00000000
Property: RW

Bit	31	30	29	28	27	26	25	24
	VEL_HLD[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	VEL_HLD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	VEL_HLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VEL_HLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – VEL_HLD[31:0] 32-bit Velocity Counter
This register is loaded for any read of VEL_CNT[7:0]. This allows coherent 8 bit / 16 bit reads of VEL_CNT.

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46.6.1.8. Interval Timer Register

Name: INTTMR
Offset: 0x70
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
	INTTMR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INTTMR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INTTMR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTTMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INTTMR[31:0] 32-bit Interval Timer Counter bits

The INTxTMR register provides a means to measure the time between each decoded quadrature count pulse to yield improved velocity information. The interval timer should be set to run at a frequency chosen such that the counter does not overflow at the expected minimum operating speed of the motor. The interval timer is automatically cleared when a count pulse is detected. The timer then counts at the specified rate based on the setting of the INTDIV bit in the QEIxCON register.

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46.6.1.9. Interval Timer Hold Register

Name: INTHLD
Offset: 0x80
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
	INTHLD[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INTHLD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INTHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INTHLD[31:0] 32-bit Index Counter Hold bits
When the next count pulse is detected, the current contents of the interval timer (INTxTMR) are transferred to the Interval Hold register (INTxHLD) and the interval timer is cleared and the process repeats.

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46.6.1.10. Index Counter Register

Name: INDXCNT
Offset: 0x90
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
	INDXCNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INDXCNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INDXCNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INDXCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INDXCNT[31:0] 32-bit Index Counter bits

Note: This counter counts in a bidirectional manner (in two's complete format). The sign for counting is derived from the current position count direction.

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46.6.1.11. Index Counter Hold Register

Name: INDXHLD
Offset: 0xA0
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
	INDXHLD[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INDXHLD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INDXHLD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INDXHLD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – INDXHLD[31:0] Hold Register for Reading/Writing Index Counter bits

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46.6.1.12. QEI Initialize/Capture/Compare Register

Name: QEIICC
Offset: 0xB0
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
	ICCH[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ICCH[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ICCH[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ICCH[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ICCH[31:0] 32-bit Initialize/Capture/Compare High bits

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46.6.1.13. QEI Initialize/Capture/Compare Low Register

Name: QEICMPL
Offset: 0xC0
Reset: 0x00000000
Property: R/W

Bit	31	30	29	28	27	26	25	24
	CMPL[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CMPL[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CMPL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CMPL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CMPL[31:0] 32-bit Compare Low Value bits

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47. Electrical Characteristics

This chapter provides the electrical specifications and characteristics of the PIC32CX-BZ6 and the PIC32WM-BZ6 Module across the operating temperature range of the device.

Note: All the electrical specifications of the PIC32CX-BZ6 apply to the PIC32WM-BZ6 Module as well unless specified explicitly.

47.1. Absolute Maximum Ratings

Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Table 47-1. Absolute Maximum Ratings

Parameter	Value
Ambient temperature under bias (PIC32CX-BZ6)(1)	-40°C to +125°C
Ambient temperature under bias (PIC32WM-BZ6)(1)	-40°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD33}/V_{DDIO}/AV_{DD} with respect to GND	-0.3V to +4.0V
Voltage on any Non-5V tolerant pin(s), with respect to GND(3,4,5)	-0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to GND when $V_{DD} \geq 1.9V$(3,4)	-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to GND when $V_{DD} < 1.9V$(3,4)	-0.3V to +(V_{DD}+3.6V)
Voltage on D+ or D- pin with respect to GND(5)	-0.3V to (V_{DD}+0.3V)
Voltage on VBUS with respect to GND	-0.4V to +5.5V
Maximum current out of GND pins	200 mA
Maximum current into V_{DD33} pins(2)	200 mA
Maximum current sunk by all ports	120 mA
Maximum current sourced by all ports(2)	120 mA
Maximum Junction Temperature	+135°C
ESD Qualification	
Human Body Model (HBM) per JESD22-A114	±2000V
Charged Device Model (CDM) (ANSI/ESD STM 5.3.1)...(All pins)	±500V

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. Maximum allowable current is a function of the device's maximum power dissipation (see the *Thermal Operating Conditions* table in the *Thermal Specifications* from Related Links).
3. See the pin mapping tables___ for the 5V tolerant pins.
4. When applying higher or lower voltage than those specified on IO pins, please refer to DI_19 / DI_21 to respect the maximum injection current specification.
5. The max voltage applied on the Pin is limited to +4V.

Related Links

Thermal Specifications

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47.2. DC Electrical Characteristics

Table 47-2. Operating Frequency VS. Voltage

Param. No.	V_{DD}/V_{DDIO}, AV_{DD} Range	Temp. Range (in °C)	Max. MCU Frequency	Comments
DC_5	—	-40°C to +85°C	128 MHz	Industrial
DC_6	—	-40°C to +105°C	128 MHz	V-Temp
DC_7	—	-40°C to +125°C	128 MHz	Extended

47.3. Thermal Specifications

Table 47-3. Thermal Operating Conditions

Rating	Symbol	Min.	Typ	Max.	Unit
Industrial Temperature Devices:					
Operating ambient temperature range	T_A	-40	—	+85	°C
Operating junction temperature range	T_J	—	—	+95	°C
V-temp Temperature Devices:					
Operating ambient temperature range	T_A	-40	—	+105	°C
Operating junction temperature range	T_J	—	—	+115	°C
Extended Temperature Range:					
Operating ambient temperature range	T_A	-40	—	+125	°C
Operating junction temperature range	T_J	—	—	+135	°C
Power Dissipation: Internal Chip Power Dissipation: P_{INT} = (VDDIOx x (IDD –∑ IOH)) I/O Pin Power Dissipation: $P_{I/O}$ = ∑ (({VDDIO – VOH} x IOH) + ∑ (VOL x IOL))	P_D	$P_{INT} + P_{I/O}$			W
Maximum allowed power dissipation	P_{DMAX}	$(T_J - T_A)/\Theta_{JA}$			W

Table 47-4. Thermal Packaging Characteristics

Characteristics	Symbol	Typ	Max.	Unit
Thermal Resistance, 132-pin DQFN (10 mm x 10 mm x 0.9 mm) Package	Θ_{JA}	21.7	—	°C/W
Thermal Resistance, 64-pin VQFN (9 mm x 9 mm x 0.9 mm) Package	Θ_{JA}	19.7	—	°C/W
Thermal Resistance, 48-pin QFN (7 mm x 7 mm x 0.9 mm) Package	Θ_{JA}	21.6	—	°C/W
Note: The junction-to-ambient thermal resistance, Θ_{JA}, numbers are achieved by package simulations.				

47.4. Power Supply DC Module Electrical Specifications

DC Characteristics			Standard Operating Conditions: $V_{DD33} = V_{DDIO} = AV_{DD}$ = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_2	VDD33_CIN(1)	VDD33 Input Bypass parallel Capacitor pair	—	10	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature

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Power Supply DC Module Electrical Specifications (continued)

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_3	PMU_VDDIO_CIN(1)	PMU_VDDIO Input Bypass parallel Capacitor pair	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_4	PMU_VDDP_CIN(1)	PMU_VDDP Input Bypass parallel Capacitor pair	—	10	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_5	FAVDD_CIN(1)	FAVDD Input Bypass parallel Capacitor pair	—	10	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic X7R/X5R with ESR <0.5Ω depending on temperature
REG_6	AVDD_CIN(1)	AVDD Input Bypass parallel Capacitor pair	—	10	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_7	VUSB_C_{IN}(1)	USB Power pin bypass capacitance	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_8	BUCK_PA_CIN(1)	BUCK_PA Input Bypass Capacitor	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_9	CLDO_BUCK_CIN(1)	CLDO_BUCK Input Bypass Capacitor	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_10	CLDO_IN_CIN(1)	CLDO_IN Input Bypass parallel Capacitor pair	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_11	CLDO_OUT_CIN(1)	CLDO_OUT Input Bypass parallel Capacitor pair	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature

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Power Supply DC Module Electrical Specifications (continued)

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_12	VDD_RF_CIN(1)	VDD_RF Input Bypass parallel Capacitor pair	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_13	RF_LDO_OUT_CIN(1)	RF_LDO_OUT Input Bypass parallel Capacitor pair	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_14	SOC_LDO_IN_CIN(1)	SOC_LDO, PLL_VDD Input Bypass parallel Capacitor pair	—	1	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_15	AVDD_LEXT(3)	AVDD series Ferrite Bead DCR (DC Resistance)	—	—	0.15	Ω	≥600Ω at 100 MHz
REG_16		Ferrite Bead current Rating	700	—	—	mA	
REG_17	VBUCK_LEXT (4,5)	Buck Regulator Inductor Inductance	—	4.7	—	µH	Shielded Inductor ONLY
REG_18		Inductor DCR (DC Resistance)	—	—	0.275	Ω	—
REG_21	VBUCK_CEXT	Buck Regulator Bulk Capacitor Capacitance	—	10	—	µF	—
REG_22		Capacitor ESR	—	—	0.01	Ω	—
REG_23	CLDO_LEXT	BUCK_PA/CLDO_BUCK Ferrite Bead DCR (DC Resistance)	—	—	0.15	Ω	≥600Ω at 100 MHz
REG_24		Ferrite Bead current Rating	700	—	—	mA	
REG_25	CLDO_OUT_LEXT	CLDO_OUT Ferrite Bead DCR (DC Resistance)	—	—	0.15	Ω	≥600Ω at 100 MHz
REG_26		Ferrite Bead current Rating	700	—	—	mA	
REG_27	SOC_LDO_LEXT	SOC_LDO_IN/PLL_VDD_IN Ferrite Bead DCR (DC Resistance)	—	—	0.15	Ω	≥600Ω at 100 MHz
REG_28		Ferrite Bead current Rating	700	—	—	mA	
REG_37	VDD33/ VDDIO (2)	VDD/VDDIO Input Voltage Range	1.9	3.3	3.6	V	—

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Power Supply DC Module Electrical Specifications (continued)

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_39	AVDD (2)	AVDD Input Voltage Range	>= 1.9 VDD33-0.3	—	VDD33+0.3 <= 3.6	V	—
REG_41	VUSB3V3	VUSB3V3 Input Voltage Range	3	—	3.6	V	—
PMU Specification (MLDO Mode)							
REG_43	MLDO_V_{OUT}	Output Voltage Range	1.3	1.35	1.4	V	—
REG_45	MLDO_V_{IN}	Input Voltage Range (Same as VDD/VDDIO)	1.9	3.3	3.6	V	—
PMU Specification (Buck Mode)							
REG_67	BUCK_V_{OUT}	Output Voltage Range	1.3	1.35	1.4	V	—
REG_69	BUCK_V_{IN}	Input Voltage Range (Same as VDD/VDDIO)	2.4	3.3	3.6	V	—
CLDO Specification							
REG_93	CLDO_V_{IN}	Input Voltage Range (Output from PMU)	1.3	1.35	1.4	V	—
REG_94	CLDO_V_{OUT}	Output Voltage Range	1.1	1.2	1.26	V	—
POR,BOR,RESET Specification							
REG_105	SVDD_R	VDD Rise Ramp Rate to Ensure Internal Power-on Reset Signal	—	—	4	mV/µs	Failure to meet this specification may lead to start-up or unexpected behaviors
REG_107	SVDD_F	VDD Falling Ramp Rate to Ensure Internal Power-on Reset Signal	—	—	4	mV/µs	Failure to meet this specification may cause the device to not detect reset
REG_109	VPOR+	Power-on Reset (Voltage threshold Level on VDD rising)	1.55	1.55	1.59	V	VDD33/VDDIO voltage must remain at VSS for a minimum of 200 us to ensure POR. VDDIO Power-up/Power-down (See Param REG_105, VDDIO Ramp Rate)
REG_111	VPOR-	Power-on Reset (Voltage threshold Level on VDD falling)	1.55	1.55	1.59	V	VDD33/VDDIO voltage must remain at VSS for a minimum of 200 us to ensure POR. VDDIO Power-up/Power-down (See Param REG_107, VDDIO Ramp Rate)
REG_113	VBOR33	BOR33 Voltage on VDD transition high to low	1.756	1.802	1.855	V	—
REG_115	$VBOR33_{LH}$	BOR33 Voltage on VDD transition low to high	1.756	1.834	1.855	V	—
REG_119	$VBOR33_{HYS}$	Brown-out Hysteresis	—	32	—	mV	—
REG_121	VBOR12	BOR12 (1.2V) Voltage transition high to low	1.067	1.1	1.104	V	—
REG_123	$VBOR12_{LH}$	BOR12 Voltage transition low to high	1.067	1.104	1.104	V	—
REG_125	$VBOR12_{HYS}$	Brown-out Hysteresis	—	4	—	mV	—
REG_127	VZPBOR33	Zero Power BOR (high to low)	1.66	1.787	1.98	V	—

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Power Supply DC Module Electrical Specifications (continued)

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
REG_128	$VZPBOR33_{LH}$	Zero Power BOR (low to high)	1.66	1.85	1.98	V	—
REG_129	T_{PU}	Power-up Period (Internal regulator enabled)	—	650		µs	Time till PMU, CLDO output are available
REG_135	T_{SYSDLY}	System Delay Period (Without Security)	—	4	—	ms	Before CPU start executing instruction from Flash. Includes Reload Device Configuration Fuses, Boot ROM execution time with authentication disable
REG_139	T_{RST}	External RESET valid active pulse width (low)	3	—	—	µs	Minimum reset active time to guarantee MCU reset for the SoC. No filter circuit
			13	—	—	µs	Minimum reset active time to guarantee MCU reset for the PIC32WM-BZ6 module. Reset filter circuit inside Module

Notes:

1. All bypass caps should be located immediately adjacent to pin(s) and on the same side of the PCB as the MCU. Each primary power supply group VDDIO, AVDD must have one bulk capacitor and all power pins everywhere a 100 nF bypass cap.
2. VDD33/VDDIO and AVDD must be at the same voltage level.
3. Ferrite Bead ISAT(min) ≥ (IDD(max) * 1.15).
4. User must select either MLDO or BUCK Mode. The modes are exclusive of each other.
5. Buck Inductor ISAT(min) ≥ ((ICAPACITOR + IVDDCORE_MAX) * 1.2) when BUCK mode enabled (Shielded inductor only).
6. Given:
   BUCK VSW output pin impedance = ~4Ω
   Buck Inductor DCR = ~0.2Ω (Check Inductor Mfg spec)
   C= VDDCORE Bypass Capacitance
   RVSW = VSW output pin impedance + Buck Inductor DCR
   e = 2.71828
   Recommended Inductor ISAT margin 25%
   VDDCORE bypass bulk capacitor charging current through inductor:
   ICAPACITOR = (VDDCORE / RVSW) e-t/RC
   where, t=0 is worst case
   Therefore:
   Inductor ISAT(max) = ((ICAPACITOR + IVDDCORE_PEAK_SURGE) * 1.25)
   = (((VDDCORE / RVSW) e-t/RC + IVDDCORE_PEAK_SURGE) * 1.25)

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47.5. Active Current Consumption DC Electrical Specifications

Table 47-5. Active Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp			
Param. No.	**Symbol**	**Characteristics**	**Clock/Freq**	**Typ.**	**Max.**	**Units**	**Conditions**
APWR_1	IDD_ACTIVE (1,2)	MCU IDD in run mode w/MLDO mode selected	PLL 128 MHz	185.7		µA/MHz	VDD = AVDD = 3.3V
APWR_9			FRC 8 MHz	3.9		mA	VDD = AVDD = 3.3V
APWR_13		MCU IDD in run mode w/BUCK mode selected	PLL 128 MHz	99.9		µA/MHz	VDD = AVDD = 3.3V
APWR_21			FRC 8 MHz	2.85		mA	VDD = AVDD = 3.3V

Notes:

1. Conditions:
   - No peripheral modules are operating (in other words: all peripherals are inactive)
   - Disable the JTAG port
   - RF System OFF
   - CMCC is disabled
   - MCU is running on Flash with automatic wait state
   - PreFetch Cache is enabled
   - All GPIO are input and pulled up
   - PB1, PB2, PB4, PB5 Clocks divided by 2, PB3 clock is divided by 20
   - PMU 1MHz Clock from FRC divided by 8
   - LPRC set as LPCLK
   - SOSC is disabled
   - WDT and RTCC are disabled
   - WCM memories configured in Retention + NAP mode
   - DSU is disconnected
2. MCU Running while(1) loop with 50 NOP instructions.

47.6. Idle Current Consumption DC Electrical Specifications

Table 47-6. Idle Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	**Symbol**	**Characteristics**	**Clock/Freq**	**Typ.**	**Max.**	**Units**	**Conditions**
IPWR_1	IDD_IDLE (1,2)	MCU IDD in IDLE mode w/ MLDO mode selected	PLL 128 Mhz	110.4		µA/MHz	VDD = AVDD = 3.3V
IPWR_9			FRC 8 MHz	3.3		mA	VDD = AVDD = 3.3V
IPWR_13		MCU IDD in IDLE mode w/ BUCK mode selected	PLL 128 Mhz	57.5		µA/MHz	VDD = AVDD = 3.3V
IPWR_21			FRC 8 MHz	2.47	—	mA	VDD = AVDD = 3.3V

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Table 47-6. Idle Current Consumption DC Electrical Specifications (continued)

DC Characteristics				Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.	Max.	Units	Conditions

Notes:

1. Conditions:
   - All Peripherals disabled with PMD bits (except EIC for external interrupt)
   - Disable the JTAG Port
   - RF System OFF
   - CMCC Disable
   - PreFetch Cache Disable
   - All GPIO are input and pulled up
   - PB1, PB2, PB4, PB5 Clocks divided by 2, PB3 clock is divided by 20
   - PMU 1MHz Clock from FRC div by 8
   - LPRC set as LPCLK
   - SOSC is disabled
   - RTCC is enabled as wake-up source
   - WCM memories configured in Retention + NAP mode
   - DSU is disconnected
2. Entry to sleep mode disabled and WFI instruction executed:
   - On Exit by RTCC timeout, Verified RCON status to ensure System was in IDLE mode

47.7. Standby/Sleep Current Consumption DC Electrical Specifications

Table 47-7. Standby/Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.	Max.	Units	Conditions
SPWR_1	IDD_STANDBY (1)	MCU IDD in STANDBY/SLEEP mode w/MLDO mode selected	3.3V	1.23		mA	16 MHz XTAL = OFF SOSC = OFF LP_CLK = LPRC RTC running on LPRC Full System RAM retained (Retention + NAP mode)
SPWR_17			3.3V	1.66		mA	16 MHz XTAL = ON SOSC = OFF LP_CLK = LPRC RTC running o n LPRC Full System RAM retained (Retention + NAP mode)
SPWR_29		MCU IDD in STANDBY/SLEEP mode w/BUCK mode (SLEEP mode = PSM) selected	3.3V	0.82		mA	16 MHz XTAL = OFF SOSC = OFF LP_CLK = LPRC RTC running on LPRC Full System RAM retained (Retention + NAP mode)
SPWR_45			3.3V	1.01		mA	16 MHz XTAL = ON SOSC = OFF LP_CLK = POSC RTC running on LPRC Full System RAM retained (Retention + NAP mode)

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Table 47-7. Standby/Sleep Current Consumption DC Electrical Specifications (continued)

DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.	Max.	Units	Conditions

Notes:

1. Conditions:
   - All Peripherals disabled with PMD bits
   - Disable the JTAG Port
   - RF System OFF
   - CMCC Disable
   - PreFetch Cache Enable
   - All GPIO are input and pulled up except
   - PB1, PB2, PB4, PB5 Clocks divided by 2, PB3 clock is divided by 20
   - WCM memories configured in Retention + NAP mode
   - DSU is disconnected
   - RF System in power down configuration
2. Entry to sleep mode enabled and WFI instruction executed
   - On Exit by Wake-up source (RTCC), Verified RCON status to ensure System was in Sleep mode
   - In XTAL ON mode : PMU Buck Clock is derived from POSC 16MHz and scaled to 1MHz. FRC is OFF
   - In XTAL OFF Mode : PMU is clocked from FRC and divided by 8 and POSC 16MHz clock is disabled

47.8. Deep Sleep Current Consumption DC Electrical Specifications

Table 47-8. Deep Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.	Max.	Units	Conditions
BPWR_1	IDD_DS (1,2)	MCU IDD in Deep Sleep mode powered from VDD	3.3V	1.44		µA	16 MHz XTAL = OFF SOSC = OFF RTC = ON LP_CLK = LPRC DSWDT = OFF FlexRAM is completely powered OFF (WCMSIZ.SRAM1_SIZ[1:0] = 0x0)
BPWR_5			3.3V	2.32		µA	16 MHz XTAL = OFF SOSC = OFF RTC = ON LP_CLK = LPRC DSWDT = OFF 16 KB FlexRAM retention (WCMSIZ.SRAM1_SIZ[1:0] = 0x1)

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Table 47-8. Deep Sleep Current Consumption DC Electrical Specifications (continued)

DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.	Max.	Units	Conditions

Notes:

1. Conditions:
   - All Peripherals disabled with PMD bits
   - Disable the JTAG Port
   - RF System OFF
   - CMCC is disabled
   - CPU is OFF
   - PreFetch Cache is enabled
   - All GPIO are input and pulled up
   - All PB Clocks are set OFF
   - DSU is disconnected
   - RF System set in power down configuration
2. Deep Sleep Entry configured and WFI instruction executed:
   - On Exit by RTC interrupt, verified RCON status to ensure system was in Deep Sleep mode.

47.9. XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

Table 47-9. XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.	Max.	Units	Conditions
OPWR_1	IDD_XDS (1,2)	Extreme Deep Sleep Mode Current	3.3V	180	—	nA	In Off mode, the device is entirely powered-off and subsequent execution of the WFI instruction. **Note:** This mode is left by pulling the RESET pin low or INT0 pin, or when a power Reset is done.

Notes:

1. Conditions:
   - All GPIO are input and pulled up except PB9 for INT0 wakeup source
   - All Peripherals disabled with PMD bits
   - DSU is disconnected
   - RF System in power down configuration
   - DSWDT disabled
   - RTCC, POSC, SOSC disabled
   - FlexRAM is completely powered OFF (WCMSIZ.SRAM1_SIZ[1:0] = 0x0)
2. Extreme Deep Sleep Entry Configured and WFI instruction executed.

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47.10. Wake-Up Timing from Low Power Modes AC Electrical Specifications

Table 47-10. Wake-Up Timing from Low Power Modes AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
WKUP_1	WKUP_IDLE	Wake from IDLE mode	—	0.5	—	µs	Wake-up Source: EIC Time measurement between toggle of EIC pin and IO pin set at the first instruction after wake-up (in wake-up source interrupt handler)
WKUP_3	WKUP_STDBY	Wake from STANDBY/SLEEP Mode	—	28	—	µs	
WKUP_13	WKUP_BCKUP	Wake from Deep Sleep Mode	—	4	—	ms	Wake-up Source: INT0/ NMCLR Time measurement between Set of INT0/ NMCLR pin and IO pin set at the first instruction executed from Flash (in reset handler). Includes Boot up time, Reload Device Configuration Fuses, Boot ROM execution time with authentication disable
WKUP_15	WKUP_OFF	Wake from Extreme Deep Sleep Mode	—	4	—	ms	
Note: VDD = 3.3 V, CPU clock = 128 MHz, 4 wait states, PCache enabled = __, Temperature = 25°C.							

47.11. I/O PIN AC/DC Electrical Specifications

Table 47-11. I/O PIN AC/DC Electrical Specifications

AC - DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
DI_1	VIL	Input voltage low (Drive Strength 4x pins)	GND	—	0.2*VDDIO	V	VDDIO(min) -to-VDDIO(max)
		Input voltage low (Drive Strength 8x pins)	GND	—	0.2*VDDIO	V	VDDIO(min) -to-VDDIO(max)
		Input voltage low (Drive Strength 12x pins)	GND	—	0.2*VDDIO	V	VDDIO(min) -to-VDDIO(max)
DI_3	VIH	Input High Voltage Non-5v tolerant I/O Pins (Drive Strength 4x pins)	0.65*VDDIO	—	VDDIO	V	VDDIO(min) -to-VDDIO(max)
		Input High Voltage Non-5v tolerant I/O Pins (Drive Strength 8x pins)	0.65*VDDIO	—	VDDIO	V	VDDIO(min) -to-VDDIO(max)
		Input High Voltage Non-5v tolerant I/O Pins (Drive Strength 12x pins)	0.65*VDDIO	—	VDDIO	V	VDDIO(min) -to-VDDIO(max)
		Input High Voltage 5V-tolerant I/O Pins (Drive Strength 4x pins)	0.65*VDDIO	—	5.5	V	VDDIO(min) -to- 5.5V
		Input High Voltage 5V-tolerant I/O Pins (Drive Strength 8x pins)	0.65*VDDIO	—	5.5	V	VDDIO(min) -to- 5.5V
		Input High Voltage 5V-tolerant I/O Pins (Drive Strength 12x pins)	0.65*VDDIO	—	5.5	V	VDDIO(min) -to- 5.5V

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Table 47-11. I/O PIN AC/DC Electrical Specifications (continued)

AC - DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
DI_5	VOL	4x Drive Strength I/O pins (Output Low)	—	—	0.4	V	IOL= 8 mA
		8x Drive Strength I/O pins (Output Low)	—	—	0.4		IOL= 14 mA
		12x Drive Strength I/O pins (Output Low)	—	—	0.4		IOL= 20 mA
DI_9	VOH	4x Drive Strength I/O pins (Output High)	vdd-0.6	—	—	V	IOH= 9 mA
		8x Drive Strength I/O pins (Output High)	vdd-0.6	—	—		IOH= 16 mA
		12x Drive Strength I/O pins (Output High)	vdd-0.7	—	—		IOH= 28 mA
DI_13	$IIL^{(6,7)}$	Input pin leakage current	-1	—	1	uA	GND ≤ VPIN ≤ VDDIO(max) (VPIN = Voltage present on Pin)
DI_15	R_{PDWN}	Internal Pull-Down (4x Drive Strength I/O pins)	14	18	50	kΩ	VDDIO(min) - VDDIO(max)
		Internal Pull-Down (8x Drive Strength I/O pins)	14	20	50	kΩ	
		Internal Pull-Down (12x Drive Strength I/O pins)	14	20	50	kΩ	
DI_17	R_{PUP}	Internal Pull-Up (4x Drive Strength I/O pins)	10	13	35	kΩ	
		Internal Pull-Up (8x Drive Strength I/O pins)	10	17	35	kΩ	
		Internal Pull-Up (12x Drive Strength I/O pins)	10	17	35	kΩ	
DI_19	$I_{ICL}^{(1,4,5)}$	Input Low Injection Current	-5	—	0	mA	This parameter applies to all I/O pins. Except VDD, VSS, AVDD,AVSS, NMCLR
DI_21	$I_{ICH}^{(2,3,4,5)}$	Input High Injection Current	0	—	5	mA	This parameter applies to all pins, with the exception of VDD, VSS, AVDD, AVSS, NMCLR and 5V tolerant I/O pins
DI_23	$\sum I_{ICT}$	Total Input Injection Current (sum of all I/O and control pins) Absolute value of $\lvert \sum I_{ICT} \rvert$	-20	—	20	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins. (| IICL | + | IICH |) ≤ ∑IICT

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Table 47-11. I/O PIN AC/DC Electrical Specifications (continued)

AC - DC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
DI_25	T_{RISE}	I/O pin Rise Time (4x Drive Strength, High Load)	—	—	9.5	ns	VDDIO(min), C_{LOAD} = 50 $pf_{(MAX)}$
		I/O pin Rise Time (8x Drive Strength, High Load)	—	—	8	ns	
		I/O pin Rise Time (12x Drive Strength, High Load)	—	—	4	ns	
		I/O pin Rise Time (4x Drive Strength, Standard Load)	—	—	6	ns	VDDIO(min), C_{LOAD} = 20 pf
		I/O pin Rise Time (8x Drive Strength, Standard Load)	—	—	6	ns	
		I/O pin Rise Time (12x Drive Strength, Standard Load)	—	—	3	ns	
DI_27	T_{FALL}	I/O pin Fall Time (4x Drive Strength, High Load)	—	—	9.5	ns	VDDIO(min), C_{LOAD} = 50 $pf_{(MAX)}$
		I/O pin Fall Time (8x Drive Strength, High Load)	—	—	8	ns	
		I/O pin Fall Time (12x Drive Strength, High Load)	—	—	5.5	ns	
		I/O pin Fall Time (4x Drive Strength, Standard Load)	—	—	6	ns	VDDIO(min), C_{LOAD} = 20 pf
		I/O pin Fall Time (8x Drive Strength, Standard Load)	—	—	6	ns	
		I/O pin Fall Time (12x Drive Strength, Standard Load)	—	—	3	ns	

Notes:

1. VIL source < (GND - 0.3). Characterized but not tested.
2. VIH source > (VDDIO + 0.3) for non-5V tolerant pins only. On USB, “D+” & “D-“ VIH source > (VUSB+0.3). Characterized but not tested.
3. Digital 5V tolerant pins do not have an internal high side Diode to VDDIO , and therefore, cannot tolerate any “positive” input injection current (i.e. positive injection current, VIH source > (VDDIO+0.3)).
4. If the sum of all injection currents are > | ∑IICT | it can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDDIO + 0.3) or VIL source < (GND - 0.3)).
5. Any number and the combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified ∑IICT limit. To limit the injection current the user must insert a resistor in series RSERIES, (i.e. RS), between input source voltage and device pin. The resistor value is calculated according to:
   - For negative Input voltages less than (GND-0.3): RS ≥ absolute value of | ((VIL source - (GND - 0.3)) / IICL) |
   - For positive input voltages greater than (VDDIO +0.3): RS ≥ ((VIH source - (VDDIO +0.3))/ IICH)
   - For Vpin voltages >VDDIO +0.3 and <GND-0.3 then RS = the larger of the values calculated above
6. The leakage current on the pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
7. Negative current is defined as current sourced by the pin.

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47.12. Maximum Clock Frequencies Electrical Specifications

Table 47-12. Maximum Clock Frequencies Electrical Specifications

AC Characteristics		Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp		
Param. No.	Symbol	Characteristics	Max	Units
FCLK_1	FCY	MCU clock frequency	128	MHz
FCLK_3	fAHB	AHB clock frequency	128	MHz
FCLK_5a	fAPBn	PB1, PB2, PB4 clock frequency	128	MHz
FCLK_5b	fAPBn	PB3 clock frequency	8	MHz
FCLK_5b	fAPBn	PB5 clock frequency	64	MHz
FCLK_6	fREFO[0:5]	Reference clock frequency	128	MHz
FCLK_7a	fSPLL1	SPLL1 clock frequency	128	MHz
FCLK_9a	fEPLL1	EPLL clock frequency	50	MHz
FCLK_9b	fEPLL2	EPLL clock frequency	80	MHz
FCLK_11a	fUPLL	UPLL clock frequency	96	MHz
FCLK_13	fGCLK_EIC	EIC input clock frequency	128	MHz
FCLK_15	fGCLK_FREQM_MSR	FREQM Measure clock frequency	128	MHz
FCLK_17	fGCLK_FREQM_REF	FREQM Reference clock frequency	64	MHz
FCLK_19	fGCLK_EVSYS_CHANNELx	EVSYS channel x input clock frequency	128	MHz
FCLK_21	fGCLK_SERCOMx_SLOW	Common SERCOM slow input clock frequency	32	khz
FCLK_23	fGCLK_SERCOMx_CORE	SERCOMx input clock frequency	128	MHz
FCLK_25	fGCLK_CANx	CAN input clock frequency (SPLL)	128	MHz
FCLK_25a		CAN input clock frequency (EPLL2)	80	MHz
FCLK_27	f_USB	USB input clock frequency	48	MHz
FCLK_35	fGCLK_TCCx	TCCx input clock frequency	128	MHz
FCLK_37	fGCLK_TCx	TCx input clock frequency	128	MHz
FCLK_41	fGCLK_QEI	QEI input clock frequency	128	MHz
FCLK_43	fGCLK_CCL	CCL input clock frequency	128	MHz
FCLK_45a	fREFI	External REFO input clock frequency	64	MHz
FCLK_49	fGCLK_AC	Analog comparator peripheral module clock frequency	128	MHz
FCLK_51	f_ADCx	ADC Controller clock frequency	64	MHz
FCLK_53	f_DAC	DAC input clock frequency	100	khz
FCLK_56	fGCLK_CVD	CVD input clock frequency	64	MHz
FCLK_61	f_ETH	Ethernet input clock frequency	50	MHz
FCLK_61a	fGCLK_ETH_TSU	Ethernet Time-Stamping Unit Clock	128	MHz
FCLK_67	fGCLK_SPI	SERCOM SPI internal GCLK frequency	128	MHz
FCLK_69	fGCLK_I2C	SERCOM I2C internal GCLK frequency	128	MHz
FCLK_71	fGCLK_USART	SERCOM USART internal GCLK frequency (Asynchronous Mode)	128	MHz
		SERCOM USART internal GCLK frequency (Synchronous Mode, DIRECT pin)	128	MHz
		SERCOM USART internal GCLK frequency (Synchronous Mode, PPS pin)	128	MHz

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Table 47-12. Maximum Clock Frequencies Electrical Specifications (continued)

AC Characteristics		Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp		
Param. No.	Symbol	Characteristics	Max	Units
FCLK_73	fXCK_USART	SERCOM USART external XCK frequency (Asynchronous Mode, DIRECT)	64	MHz
		SERCOM USART external XCK freq (Asynchronous Mode, PPS)	32	MHz
		SERCOM USART external XCK freq (Synchronous Mode, DIRECT pin)	16	MHz
		SERCOM USART external XCK freq (Synchronous Mode, PPS pin)	10.67	MHz

Note: To achieve reliable IEEE 1588 function, fGCLK_ETH_TSU must be less than the fAHB clock.

47.13. External XTAL and Clock (POSC) AC Electrical Specifications

Table 47-13. External XTAL and Clock (POSC) AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
XOSC_1	FOSC_XOSC	XOSC Crystal Frequency	—	16	—	MHz	XIN, XOUT Primary Osc. ± 20 ppm
XOSC_1A	TOSC	TOSC = 1/ FOSC_XOSC	—	62.5	—	ns	See parameter XOSC1 for FOSC_XOSC value
XOSC_2	XOSC_ST (2)	XOSC Crystal Start-up Time	—	1.25	2.5	ms	Crystal stabilization time+Oscillator Ready
XOSC_3	C_{XIN}	XOSC X_{IN} parasitic pin capacitance	—	0.35	—	pF	—
XOSC_5	C_{XOUT}	XOSC X_{OUT} parasitic pin capacitance	—	0.35	—	pF	—
XOSC_11	C_{LOAD}(3)	Crystal load capacitance FOSC = 16 MHz	—	8		pF	—
XOSC_21	ESR	Crystal Frequency FOSC = 16 MHz	—	—	100	Ω	
XOSC_31	IDD_{XOSC}	Oscillator Current (XOSC)	—	264	750	µA	XTAL_OSC power consumption at its resonance frequency
XOSC_33	D_{LEVEL}	MCU Crystal Osc Power Drive Level	—	100		µW	—
XOSC_34	Gm(4)	XOSC Transconductance	14	—	—	mA/V	—

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Table 47-13. External XTAL and Clock (POSC) AC Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions

Notes:

1. Typical value tested but not characterized.
2. This is for guidance only. A major component of crystal start-up time is based on the second party crystal MFG parasitics that are outside the scope of this specification. If this is a major concern, the customer must characterize this based on their design choices.
3. The test conditions for the crystal load capacitor calculation are as follows:
   - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W = 0.175 mm, H = 36 µm, T = 113 µm).
   - Xtal PCB capacitance typical; therefore, ~= 2.5 pF for a tight PCB xtal layout
   - For CXIN and CXOUT within 4 pF of each other, assume CXTAL_EFF = ((CXIN+CXOUT)/2).
     Note: Averaging CXIN and CXOUT will affect the final calculated CLOAD value by less than 0.25 pF.

   Equation 47-1. Equation 1:

   $$MFG\ \ CLOAD\ Spec = \{([CXIN + C1] * [CXOUT + C2])/[CXIN + C1 + C2 + CXOUT]\} + estimated\ oscillator\ PCB\ stray\ capacitance$$

   Assuming C1 = C2 and CXin ~= CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

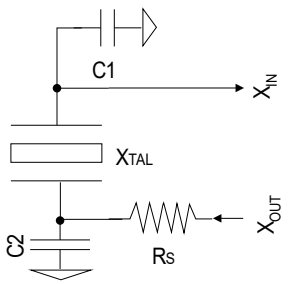
   Equation 47-2. Equation 2 (In other words: Simplified Equation 1)

   $$C1 = C2 = ((2 * MFG\ \ CLOAD\ Spec) - CXTAL\_EFF - (2 * PCB\ \ capacitance))$$

   Example:
   - XTAL Mfg CLOAD Data Sheet Spec = 12 pF
   - PCB XTAL trace Capacitance = 2.5 pF
   - CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF; therefore, CXTAL_EFF = ((CXIN+CXOUT) / 2)

   CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 pF
   C1 = C2 = ((2 * MFG Cload spec) – CXTAL_EFF – (2 * PCB capacitance))
   C1 = C2 = (24 - 5.5 – (2 * 2.5))
   C1 = C2 = 13.5 pF (Always rounded down)
   C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)
   User C1 = C2 = 13 pF CLOAD (max) spec
4. For guaranteed crystal start-up, XOSC Auto Gain disabled:
   MCU Gm (spec) / Gm_crit >= 5; MCU Gm at specified XOSC Gain level
   Gm_crit = 4*ESR(max)*(2π*F)2*(C0+CL)2; Calculated Crystal Gm
   F = Crystal Freq, C0 = Crystal Shunt Capacitance , CL = C1 = C2 = Calculated CLOAD of circuit

Figure 47-1. External XTAL and Clock Diagram



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47.14. XOSC32 (SOSC) AC Electrical Specifications

Table 47-14. XOSC32 (SOSC) AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
XOSC32_1	F_{OSC}_XOSC32	XOSC32 oscillator crystal frequency	—	32.764	—	kHz	XIN32, XOUT32 secondary oscillator
XOSC32_1	FOSC_XOSC32	XOSC32 Oscillator Crystal Frequency	—	32.768	—	kHz	XIN32, XOUT32 Secondary Osc ± 250ppm
XOSC32_3	C_{XIN32}	XOSC32 XIN32 parasitic pin capacitance (PIC32CX-BZ6)	—	4.6	—	pF	—
		XOSC32 XIN32 parasitic pin capacitance (WBZ)	—	5.2	—	pF	—
XOSC32_5	C_{XOUT32}	XOSC32 XOUT32 parasitic pin capacitance (PIC32CX-BZ6)	—	4.3	—	pF	—
		XOSC32 XOUT32 parasitic pin capacitance (WBZ)	—	5.1	—	pF	—
XOSC32_11	C_{LOAD_X32}(3)	32.768kz Crystal Load Capacitance	—	11	—	pF	—
XOSC32_12			—	—	—	pF	—
XOSC32_13	ESR_X32	32.768 kz Crystal ESR	—	75	100	KΩ	—
XOSC32_14			—	—	—	Ω	—
XOSC32_15	TOSC32	TOSC32 = 1/ FOSC_XOSC32	—	30.518	—	µs	See parameter XOSC32_1 for FOSC_XOSC32 value
XOSC32_17	XOSC32_ST (2)	XOSC32 Crystal Start-up Time	—	206	—	ms	From clock request to Oscillator Ready

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Table 47-14. XOSC32 (SOSC) AC Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions

Notes:

1. Typical value tested but not characterized.
2. This is for guidance only. A major component of crystal start-up time is based on the second party crystal MFG parasitic that is outside the scope of this specification. If this is a major concern, the customer might need to characterize this based on their design choices.
3. The test conditions for the crystal load capacitor calculation are as follows:
   - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W = 0.175 mm, H = 36 µm, T = 113 µm)
   - Xtal PCB capacitance typical; therefore, ~= 2.5 pF for a tight PCB xtal layout
   - For CXIN and CXOUT within 4 pF of each other, assume CXTAL_EFF = ((CXIN / 2)
   - **Note:** Averaging CXIN and CXOUT will affect the final calculated CLOAD value by less than the tolerance of the capacitor selection.

   Equation 1:

   $$MFG\ \ CLOAD\ Spec = \{([CXIN + C1] * [CXOUT + C2])/[CXIN + C1 + C2 + CXOUT]\} + estimated\ oscillator\ PCB\ stray\ capacitance$$

   Assuming C1 = C2 and CXin ~= CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

   Equation 47-3. Equation 2 (In other words: Simplified Equation 1)

   $$C1 = C2 = ((2 * MFG\ \ CLOAD\ Spec) - CXTAL\_EFF - (2 * PCB\ \ capacitance))$$

   Example:
   - XTAL Mfg CLOAD Data Sheet Spec = 12 pF
   - PCB XTAL trace Capacitance = 2.5 pF
   - CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF therefore CXTAL_EFF = ((CXIN / 2)

   CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 pF

   C1 = C2 = ((2 * MFG Cload spec) – CXTAL_EFF – (2 * PCB capacitance))

   C1 = C2 = (24 – 5.5 – (2 * 2.5))

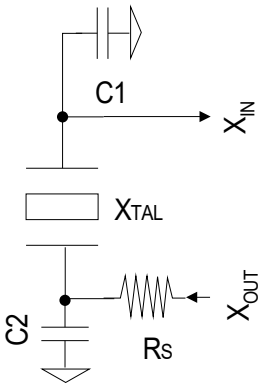
   C1 = C2 = (24 – 5.5 – 5)

   C1 = C2 = 13.5 pF (Always rounded down)

   C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)

   User C1 = C2 = 13 pF ≤ CLOAD_X32 (max.) spec
4. User selectable in OSC32KCTRL.STARTUP.

Figure 47-2. XOSC32 Block Diagram



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47.15. Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

Table 47-15. Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
LP32K_1	FOSC_LPRC32K	Output Frequency	—	32.768	—	kHz	-40°C ≤ T_A ≤ +85°C (i.e. Factory Default Calibration)
LP32K_3	LPRC32K_ACC	Accuracy from factory calibration	—	—	—	kHz	-40°C ≤ T_A ≤ +125°C
LP32K_9	RC32K_Duty	LPRC32K OSC Duty Cycle	—	50	—	%	—

47.16. FRC AC Electrical Specifications

Table 47-16. FRC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
FRC1	FINTFREQ	Internal FRC Frequency	—	8	—	MHz	—
FRC3	TSUFRC	Start-up time of internal FRC	—	11.12	—	us	—
FRC5	FACCU	FRC Accuracy	—	—	—	%	—
FRC7	DUTY_CYCLE	FRC Duty Cycle	—	50	—	%	—
FRC9	C_USE	FRC User Tune	TBD	TBD	TBD	%	Maximum Frequency drift possible by using the Frequency trim bits (OSCTRIM register)
FRC11	C_USER_STEP_SIZE	FRC User Tune Step size	—	0.047	—	%	Change in frequency with incremental trim bit (OSCTRIM register)

47.17. RFPLL (RF/System Phase Locked Loop) AC Electrical Specifications

Table 47-17. RFPLL (RF/System Phase Locked Loop) AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
RFPLL_1	RFPLL_F_{IN}(1)	RFPLL Input Frequency Range	—	16	—	MHz	—
RFPLL_3	RFPLL_FOUT(1)	RFPLL Output Clock Frequency	—	128	—	MHz	—
RFPLL_5	RFPLL_Jitter	RFPLL Period Jitter Pk-to-Pk	—	—	500	ps	—
RFPLL_7	RFPLL_RFRT	RFPLL Start-Up / Lock Time	—	32	75	µs	—

Note:

1. Input clock source for RFPLL, UPLL (USB), EPLL (Ethernet) is XOSC (POSC).

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Table 47-18. EPLL (Ethernet Phase Locked Loop) AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
EPLL_1	PLL_F_{IN}(1)	PLL Input Frequency Range	—	16	—	MHz	—
EPLL_3	PLL_FOUT	PLL Output Clock Frequency (EPLL1)	—	80	—	MHz	—
		PLL Output Clock Frequency (EPLL2)	—	50	—	MHz	—
EPLL_5	PLL_VCO	PLL VCO Frequency Range	800	—	1600	MHz	—
EPLL_11	PLL_RFRT	PLL Start-Up / Lock Time Time	—	17	50	µs	—

Note:

1. Input clock source for RFPLL, UPLL (USB), EPLL (Ethernet) is XOSC (POSC).

Table 47-19. UPLL (USB Phase Locked Loop) AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
UPLL_1	PLL_F_{IN}(1)	PLL Input Frequency Range	—	16	—	MHz	—
UPLL_3	PLL_FOUT	PLL Output Clock Frequency	—	96	—	MHz	—
UPLL_5	PLL_VCO	PLL VCO Frequency Range	1152	—	1536	MHz	—
UPLL_11	PLL_RFRT	PLL Start-Up / Lock Time	—	10	50	µs	—

Note:

1. Input clock source for RFPLL, UPLL (USB), EPLL (Ethernet) is XOSC (POSC).

47.18. DAC Module Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
DAC_1	DRES	DAC Resolution	—	—	7	Bits	—
DAC_3	DCLK	Internal DAC Clock Frequency	—	—	FCLK_53	MHz	AVDD(min)
DAC_7	VOUT	Output Voltage Linear Range	AVSS+	—	AVDD-	V	VREF = AVDD
DAC_9	VREF	DAC Reference Input Option		—	AVDD	V	—
DAC_11	CLOAD	DAC Out max load to meet VOUT and TSET	—	—	40	pf	—
DAC_13	RLOAD	DAC Out max load to meet VOUT and TSET	33	—	—	KΩ	—

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DAC Module Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
DAC_15	Tset	DAC Settling Time (10LSB step)	TBD	TBD	10	µs	±2 LSB of final value for step size ≤ 10 Lsb at CLOAD and RLOAD w/ AVDD = 3.3V
DAC_17	Tset_FS	DAC Full Scale Settling Time	TBD	TBD	20	µs	±2 LSB of final value for step size from 10% to 90% at CLOAD and RLOAD w/ AVDD = 3.3V
Single Ended Mode							
SDAC_19	INL	Integral Non Linearity	TBD	±2	TBD	LSB	VREF = AVDD = 3.3V
SDAC_21	DNL	Differential Non Linearity	TBD	±3	TBD	LSB	
SDAC_23	GERR	Gain Error	TBD	TBD	TBD	LSB	VREF = AVDD = 3.3V
SDAC_25	EOFF	Offset Error	TBD	TBD	TBD	LSB	VREF = AVDD = 3.3V

47.19. ADC Electrical Specifications

Table 47-20. ADC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
Device Supply							
ADC_1	AVDD	ADC Module Supply	AVDD(min)	—	AVDD(max)	V	—
Reference Inputs							
ADC_3	VREF	ADC Reference Voltage	—	—	AVDD	V	Internal Reference
Analog Input Range							
ADC_7	AFS	Full-Scale Analog Input Signal Range	AVSS	—	VREF	V	Single-Ended Mode

Table 47-21. Single-Ended Mode ADC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
Single-Ended Mode ADC Accuracy							
SADC_11	Res	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 bit Resolution Ranges
SADC_13	ENOB	Effective Number of bits	TBD	10.5	TBD	bits	2 MSPS, 12-bit Resolution mode VREF = AVDD = VDDIO = 3.3V
SADC_19	INL	Integral Nonlinearity	TBD	±3	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
SADC_25	DNL	Differential Nonlinearity	TBD	±1	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
SADC_31	GERR	Gain Error	TBD	±8	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V

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Table 47-21. Single-Ended Mode ADC AC Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
SADC_37	EOFF	Offset Error	TBD	±4	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
Single-Ended Mode ADC Dynamic Performance							
SADC_49	SINAD	Signal to Noise and Distortion	TBD	65	TBD	dB	VREF = AVDD = VDDIO = 3.3V at 12bit max sampling rate
SADC_51	SNR	Signal to Noise ratio	TBD	TBD	TBD		
SADC_53	SFDR	Spurious Free Dynamic Range	TBD	65	TBD		
SADC_55	THD	Total Harmonic Distortion	TBD	-65	TBD		

Table 47-22. Differential Mode ADC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
Differential Mode ADC Accuracy							
DADC_11	Res	Resolution	6	—	12	bits	Selectable 6, 8, 10, 12 bit Resolution Ranges
DADC_13	ENOB	Effective Number of bits	TBD	TBD	TBD	bits	2 MSPS, 12-bit Resolution mode VREF = AVDD = VDDIO = 3.3V
DADC_19	INL	Integral Nonlinearity	TBD	TBD	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
DADC_25	DNL	Differential Nonlinearity	TBD	TBD	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
DADC_31	GERR	Gain Error	TBD	TBD	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
DADC_37	EOFF	Offset Error	TBD	TBD	TBD	LSB	2 MSPS, VREF = AVDD = VDDIO = 3.3V
DADC_43	TUE	Total Unadjusted Error	TBD	TBD	TBD	LSB	1 MSPS, Internal VREF - 0.___, AVDD = VDDIO = 3.3V
Differential Mode ADC Dynamic Performance							
DADC_49	SINAD	Signal to Noise and Distortion	TBD	TBD	TBD	dB	VREF = AVDD = VDDIO = 3.3V at 12bit max sampling rate
DADC_51	SNR	Signal to Noise ratio	TBD	TBD	TBD		
DADC_53	SFDR	Spurious Free Dynamic Range	TBD	TBD	TBD		
DADC_55	THD	Total Harmonic Distortion	TBD	TBD	TBD		

Table 47-23. ADC Conversion and Sample AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
ADC Clock Requirements							

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Table 47-23. ADC Conversion and Sample AC Electrical Requirements (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
ADC_57	TQ	ADC Controller Clock Period	1/ fADC_TQ	—	—	ns	—
ADC_57a	TAD	ADC Core Clock Period	1/ fADC_TAD	—	1/ fADC_TAD	ns	—
ADC_58	fADC_TQ	ADC Controller Clock freq		—	FCLK_51	MHz	—
ADC_58a	fADC_TAD	ADC Core Clock Frequency	0.14	—	32	MHz	—
ADC Single-Ended Throughput Rates							
ADC_59	F_{TP} (1) (Single-Ended Mode)	ADC0-Throughput Rate (Sampling rate) (Single-Ended)	TBD	TBD	1	MSPS	12-bit resolution, Rsource Impedance ≤ 200 Ω, SAMC=0
		ADC-SHR -Throughput Rate (Sampling rate) (Single-Ended)	TBD	TBD	1		12-bit resolution, Rsource Impedance ≤ 200 Ω, SAMC=0
ADC Conversion and Sample time							
ADC_63	TSAMP	ADC Sample Time (ADC0)	2.5	TBD	TBD	TAD	12 bit TAD(min), Ext Analog Input Rsource ≤ 200 Ω, Max ADC Clock, SAMC=0
		ADC Sample Time (ADC-SHR)	2.5	TBD	TBD		12 bit TAD(min), Ext Analog Input Rsource ≤ 200 Ω, Max ADC Clock
		ADC Sample Time (ADC-SHR with with ADCCON1.CVDEN bit = 1)	TBD	TBD	TBD		12 bit TAD(min), Ext Analog Input Rsource ≤ 200 Ω, ADCCON2.CVDCPL[2:0] = 111
ADC_65	TCNV	Conversion Time (Single-Ended Mode)	12.5			TAD	12-bit resolution
			12				10-bit resolution
			10				8-bit resolution
			8				6-bit resolution

Note:

1. ADC Throughput Rate FTP = ((1 / ((TSAMP + TCNV) * TAD)) / (# of user active analog inputs in use on specific target ADC module)). Specification values assume only one AINx channel in use.

47.20. Analog Comparator AC Electrical Specifications

Table 47-24. Analog Comparator AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
CMP_1	VIOFF_00	Input Offset Voltage	-16	—	16	mV	Comparator ref voltage = AVDD/2COMPCTRLx<HYST> = 0x0, COMPCTRLn.HYSTEN = 1

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Table 47-24. Analog Comparator AC Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
CMP_4	VIN	Input Voltage Range	AVSS	—	AVDD	mV	With respect to GND and AVDD
CMP_5	VHYST_00	Input Hysteresis Voltage	—	15	—	mV	Comparator ref voltage = AVDD/ 2COMPCTRLx<HYST> = 0x0
CMP_15	TRESPSS(2)	Small Signal Response Time	—	140	160	ns	Comparator ref voltage = AVDD/2, COMPCTRLx<HYST> = 0x3, input step of 50 mV with Input overdrive = ± 15 mV
CMP_19	COUTVAL	Comparator Enabled to Output Valid	—	—	10	ms	Comparator module is configured before enabling it
CMP_21	ACIREF	Comparator Internal Band Gap Voltage Reference	—	1.2	—	V	AVDD = 3.3V, T = 25°C
CMP_23	CVREFRNG	Comparator Voltage Reference Input Range	(1)	—	(1)	V	—
CMP_25	FGCLK_AC	Analog comparator peripheral module clock freq	—	—	FCLK_49	MHz	—

Notes:

1. Comparator Ref voltage cannot exceed: (VIN(max) - VIOFF(max) - CMP_5(max) - 50 mV) ≥CMP_23 ≥ (VIN(min) + abs(VIOFF(min)) + CMP_5(max) + 50 mV).
2. TRESP is measured from VIN transition to ACOUT toggle (AC direct output accessible by setting COMPCTRLn.OUT[1:0]). It takes into account only analog propagation delay.

47.21. SPI Module Electrical Specifications

Table 47-25. SPI Module Host Mode Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MSP_1	FSCK	SCK Frequency	—	—	16	MHz	VDDIO=3.3V, C_{LOAD}=30 $pF_{(MAX)}$ DIRECT pins
			—	—	10.67		VDDIO=3.3V, C_{LOAD}=30 $pF_{(MAX)}$ Remappable pins
			—	—	16		VDDIO=1.9V, C_{LOAD}=30 $pF_{(MAX)}$ DIRECT pins
			—	—	10.67		VDDIO=1.9V, C_{LOAD}=30 $pF_{(MAX)}$ Remappable pins
MSP_3	TSCL	SCK Output Low Time	—	1/(2*FSCK)	—	ns	—
MSP_5	TSCH	SCK Output High Time	—	1/(2*FSCK)	—	ns	—

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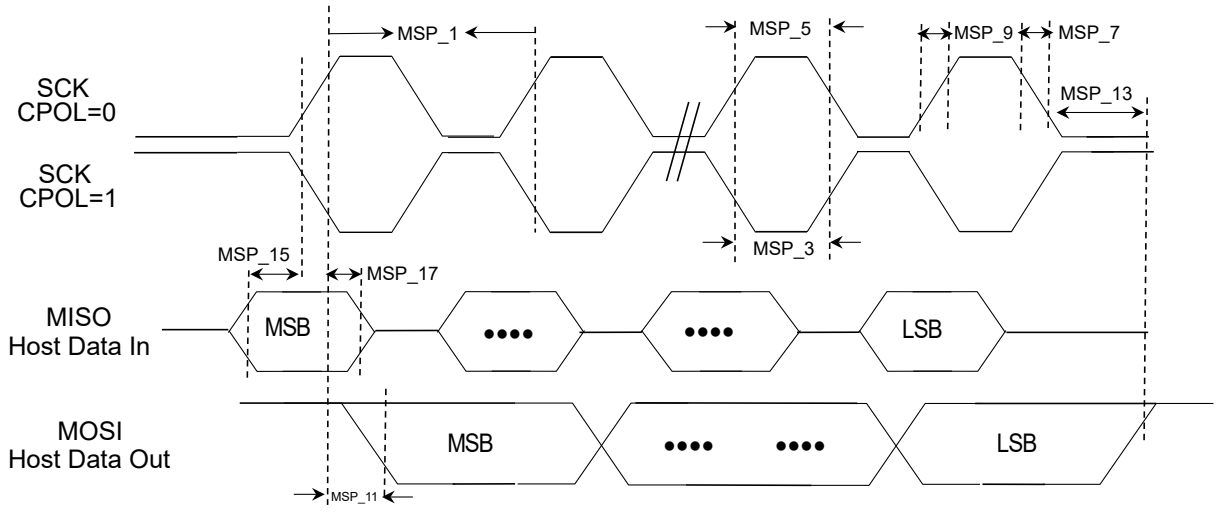
Table 47-25. SPI Module Host Mode Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MSP_7	TSCF	SCK & MOSI Output Fall Time	—	—	DI27	ns	See parameter DI27 I/O spec
MSP_9	TSCR	SCK & MOSI Output Rise Time	—	—	DI25	ns	See parameter DI25 I/O spec
MSP_11	TMOV	MOSI Data Output Valid after SCK	—	—	7	ns	DIRECT pins
			—	—	13	ns	Remappable/ PPS pins
MSP_13	TMOH	MOSI hold after SCK	5	—	—	ns	—
MSP_15	TMIS	MISO Setup Time of Data Input to SCK	27	—	—	ns	DIRECT pins
			35	—	—	ns	Remappable/ PPS pins
MSP_17	TMIH	MISO Hold Time of Data Input to SCK	0	—	—	ns	—
MSP_19	SPI_GCLK	SERCOM SPI input clk freq, GCLK_SPI	—	—	FCLK_67	MHz	—

Notes:

1. Assumes VDDIOx(min) and 30pF external load on all SPIx pins unless otherwise noted.
2. These parameters are characterized, but not tested in manufacturing

Figure 47-3. SPI Host Module CPHA = 0 Timing Diagrams



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Figure 47-4. SPI Host Module CPHA = 1 Timing Diagrams

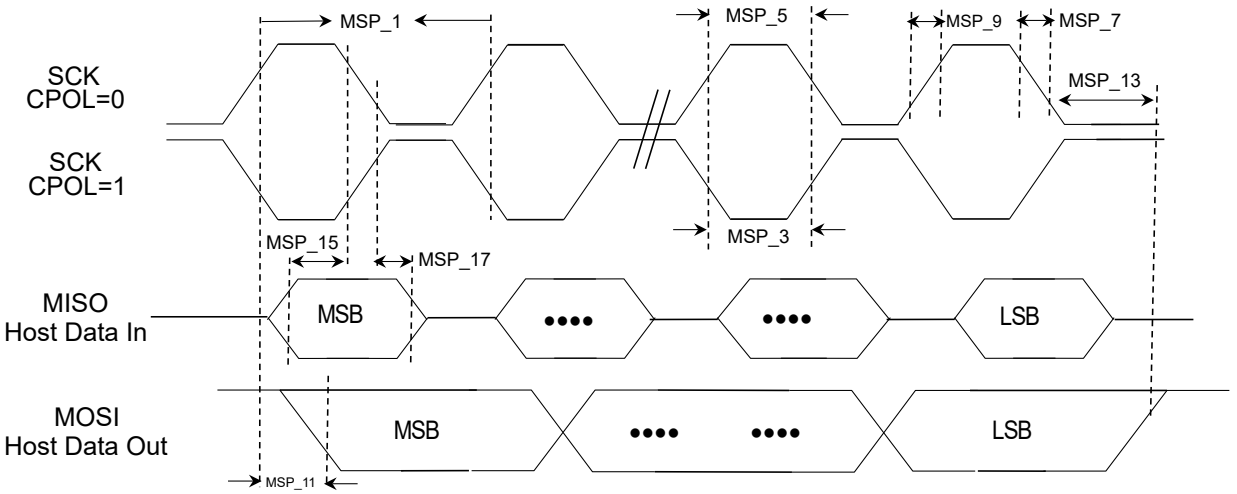


Table 47-26. SPI Module Client Mode Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	**Symbol**	**Characteristics(1, 2)**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
SSP_1	FSCK	SCK Frequency	—	—	16	MHz	VDDIO=3.3V, C_{LOAD}=30 $pF_{(MAX)}$ DIRECT pins
			—	—	10.67		VDDIO=3.3V, C_{LOAD}=30 $pF_{(MAX)}$ Remappable pins
			—	—	16		VDDIO=1.9V, C_{LOAD}=30 $pF_{(MAX)}$ DIRECT pins
			—	—	10.67		VDDIO=1.9V, C_{LOAD}=30 $pF_{(MAX)}$ Remappable pins
SSP_3	TSCL	SCK Output Low Time	—	1/(2*FSCK)	—	ns	—
SSP_5	TSCH	SCK Output High Time	—	1/(2*FSCK)	—	ns	—
SSP_7	TSCF	MISO Output Fall Time	—	—	DI27	ns	See parameter DI27 I/O spec
SSP_9	TSCR	MISO Output Rise Time	—	—	DI25	ns	See parameter DI25 I/O spec
SSP_11	TSOV	MISO Data Output Valid after SCK	—	—	24	ns	DIRECT pins
			—	—	34	ns	Remappable/ PPS pins
SSP_13	TSOH	MISO hold after SCK	0	—	—	ns	
SSP_15	TSIS	MOSI Setup Time of Data Input to SCK	6	—	—	ns	DIRECT pins
			7	—	—	ns	Remappable/ PPS pins
SSP_17	TSIH	MOSI Hold Time of Data Input to SCK	1	—	—	ns	DIRECT pins
			2	—	—	ns	Remappable/ PPS pins
SSP_19	TSSS	SS setup to SCK (PRELOADEN=1)	TSCK+13	—	—	ns	
		SS setup to SCK (PRELOADEN=0)	TSCK	—	—	ns	
SSP_21	TSSH	SS hold after SCK Client	TSIH-1	—	—	ns	
SSP_23	SPI_GCLK	SERCOM SPI input clk freq, GCLK_SPI	—	—	FCLK_67	MHz	

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Table 47-26. SPI Module Client Mode Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics(1, 2)	Min.	Typical	Max.	Units	Conditions

Notes:

1. Assumes VDDIOx(min) and 30 pF external load on all SPIx pins unless otherwise noted.
2. These parameters are characterized, but not tested in manufacturing.

Figure 47-5. SPI Client Module CPHA = 0 Timing Diagrams

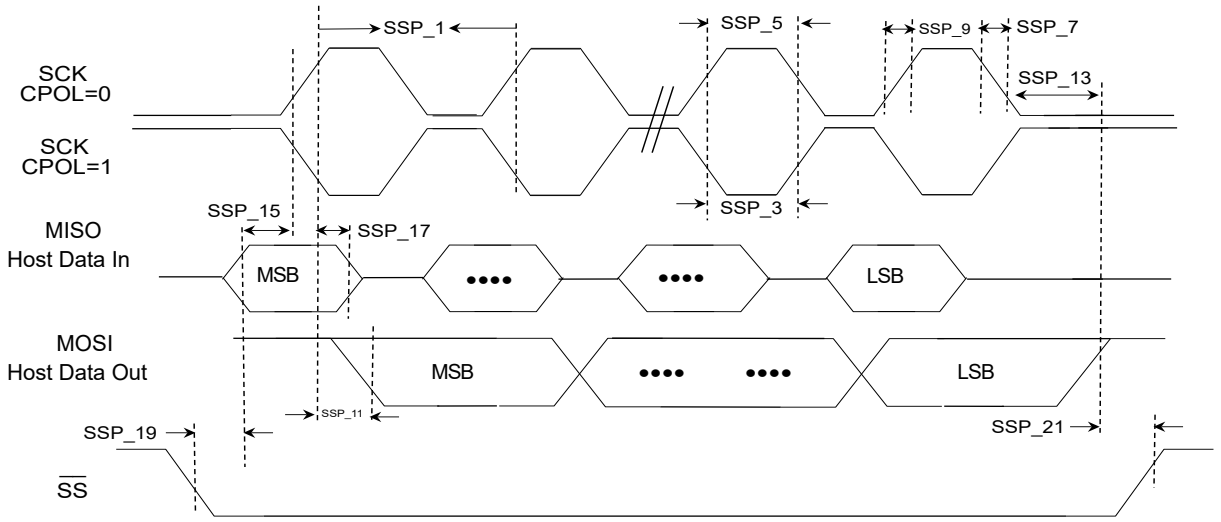
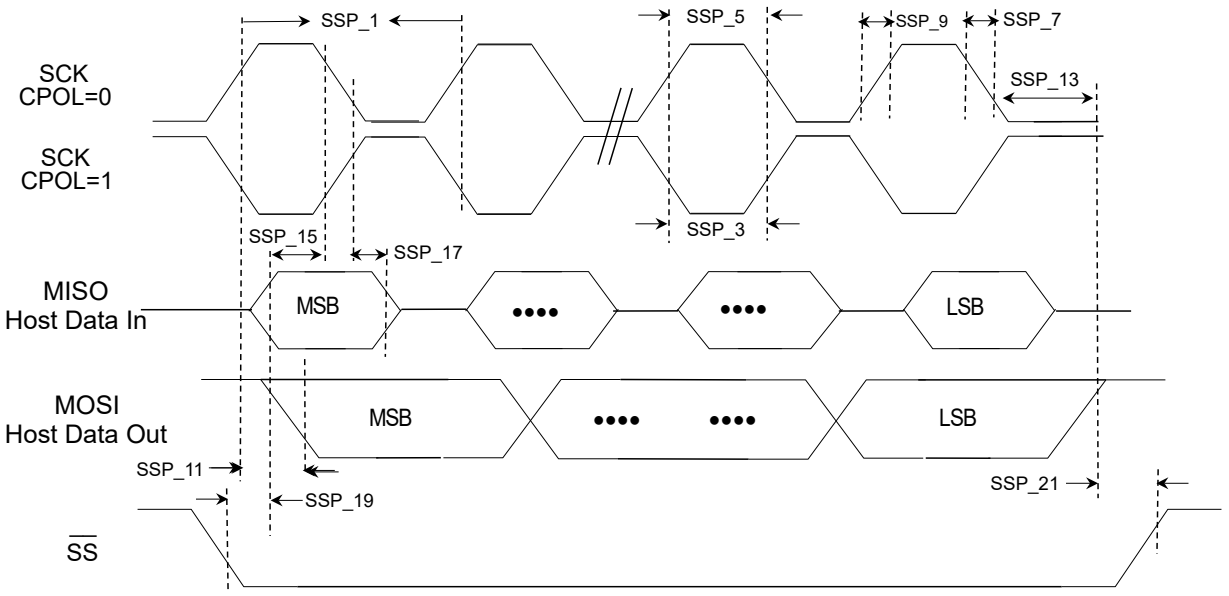


Figure 47-6. SPI Client Module CPHA = 1 Timing Diagrams



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47.22. UART AC Electrical Specifications

Table 47-27. UART AC Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics		Min.	Typical	Max.	Units	Conditions
UT_1	FBRATE	Baud Rate	Asynchronous SAMPR = 16x mode (Internal)	—	—	FCLK_71/16	Mbps	—
			Asynchronous SAMPR = 16x mode (External)	—	—	FCLK_73/16	Mbps	—
UT_3			Asynchronous SAMPR = 8x mode (Internal)	—	—	FCLK_71/8	Mbps	—
			Asynchronous SAMPR = 8x mode (External)	—	—	FCLK_73/8	Mbps	—
UT_5			Asynchronous SAMPR = 3x mode (Internal)	—	—	FCLK_71/3	Mbps	Max Baud Rate is limited to 21.33 Mbps
			Asynchronous SAMPR = 3x mode (External)	—	—	FCLK_73/3	Mbps	—
UT_19			Synchronous Host Mode (Internal clock)	—	—	16	Mbps	DIRECT Pins
				—	—	10.67	Mbps	Remappable (PPS) Pins
UT_21			Synchronous Client Mode (External clock)	—	—	10	Mbps	DIRECT Pins
				—	—	10.67	Mbps	Remappable (PPS) Pins
UT_23	FUSART	USART max GCLK_SERCOM		—	—	FCLK_71	MHz	—
UT_25	FXCK	USART External Clock Input		—	—	FCLK_73	MHz	—

Note: These parameters are characterized but not tested in manufacturing.

47.23. I²C Module Electrical Specifications

Table 47-28. I²C Module Host Mode Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
I2CM_23	TBF:SDA	Bus free time(1)	400 kHz mode	TL0:SCL	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pf
I2CM_1	TL0:SCL	Host Clock Low Time	100 kHz mode	4.7	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_3	THI:SCL	Host Clock High Time	100 kHz mode	4	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF

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Table 47-28. I^2C Module Host Mode Electrical Specifications (continued)

AC Characteristics				Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
I2CM_5	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	TBD	300	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	TBD	300	ns	
			1 MHz mode	TBD	120	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_7	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	TBD	1000	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	TBD	300	ns	
			1 MHz mode	TBD	120	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_9	TSU:DAT	Data Setup Time	100 kHz mode	250	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	100	—	ns	
			1 MHz mode	50	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_11	THD:DAT	Data Hold Time (1)	100 kHz mode	300	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	300	—	ns	
			1 MHz mode	0	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_13	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_15	THD:STA	Start Condition Hold Time	100 kHz mode	4	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_17	TSU:ST0	Stop Condition Setup Time	100 kHz mode	4	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_21	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3.45	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	—	0.9	µs	
			1 MHz mode	—	0.45	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_23	TBF:SDA	Bus Free Time (2)	100 kHz mode	4.7	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF

Notes:

1. Longest delay between data hold timing based on CFGI2C.I2CDSEL for 100 kHz/400 kHz mode.
2. The amount of time the bus must be free before a new transmission can start (STOP condition to START condition).

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Figure 47-7. I²C Start/Stop Bits Host Mode AC Timing Diagram

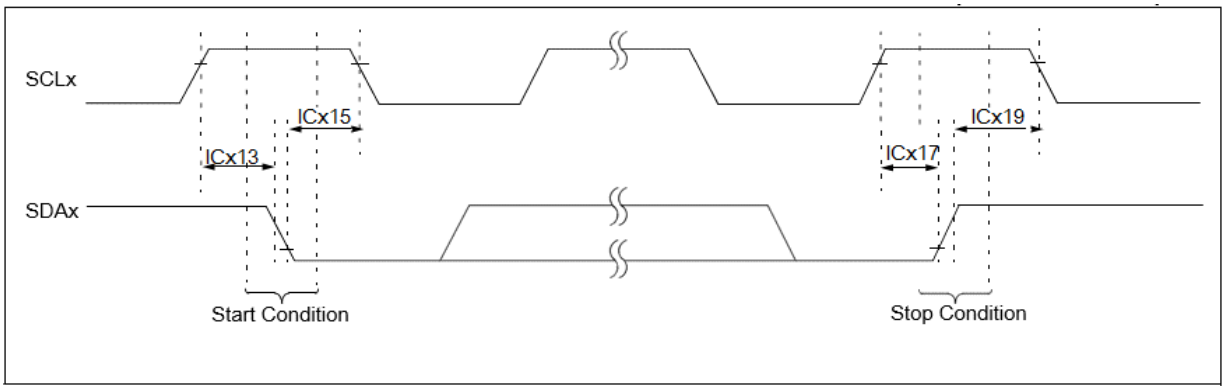


Figure 47-8. I²C Bus Data Host Mode AC Timing Diagram

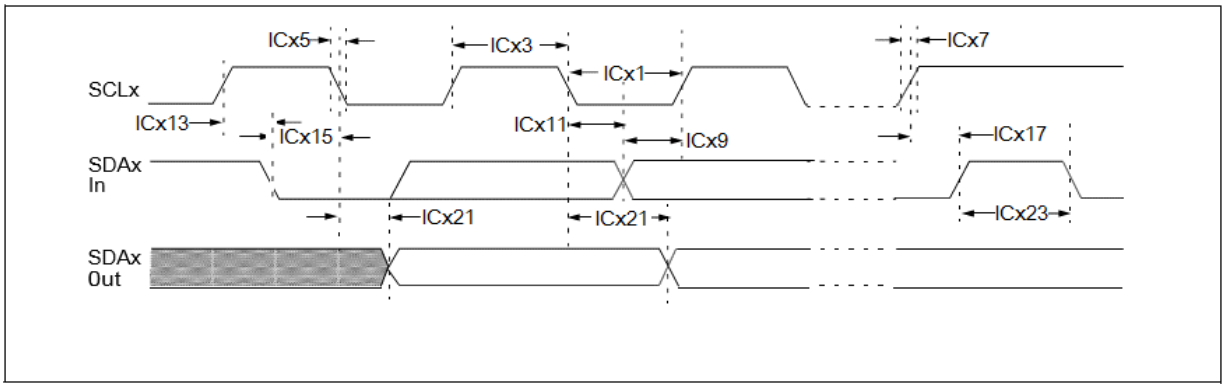


Table 47-29. I²C Module Client Mode Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	**Symbol**	**Characteristics**		**Min.**	**Max.**	**Units**	**Conditions**
I2CS_1	TL0:SCL	Client Clock Low Time	100 kHz mode	4.7	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_3	THI:SCL	Client Clock High Time	100 kHz mode	4	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_5	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	—	300	ns	
			1 MHz mode	—	120	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_7	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	—	300	ns	
			1 MHz mode	—	120	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF

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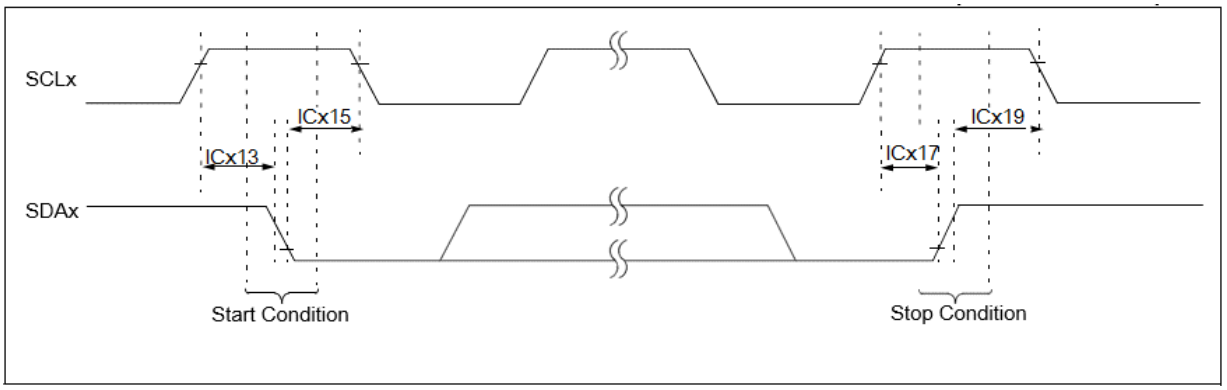
Table 47-29. I²C Module Client Mode Electrical Specifications (continued)

AC Characteristics				Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
I2CS_9	TSU:DAT	Data Setup Time	100 kHz mode	250	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	100	—	ns	
			1 MHz mode	50	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_11	THD:DAT	Data Hold Time (1)	100 kHz mode	300	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	300	—	ns	
			1 MHz mode	0	—	ns	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_13	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_15	THD:STA	Start Condition Hold Time	100 kHz mode	4	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_17	TSU:ST0	Stop Condition Setup Time	100 kHz mode	4	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	0.6	—	µs	
			1 MHz mode	0.26	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_21	TAA:SCL	Output Valid from Clock	100 kHz mode	—	3.45	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	—	0.9	µs	
			1 MHz mode	—	0.45	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF
I2CS_23	TBF:SDA	Bus Free Time (1)	100 kHz mode	4.7	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 3 mA, CLOAD = 400 pF
			400 kHz mode	1.3	—	µs	
			1 MHz mode	0.5	—	µs	VDDIOx = 3.3V, $I_{PULL-UP}$ = 20 mA, CLOAD = 550 pF

Notes:

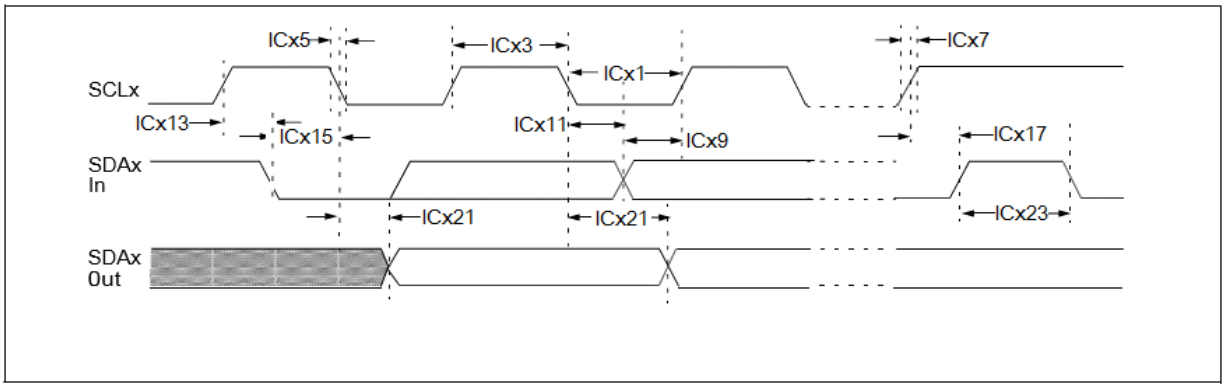
1. Longest delay between data hold timing based on CFGI2C.I2CDSEL for 100 kHz/400 kHz mode.
2. The amount of time the bus must be free before a new transmission can start (STOP condition to START condition).

Figure 47-9. I²C Start/Stop Bits Client Mode AC Timing Diagram



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Figure 47-10. I²C Bus Data Client Mode AC Timing Diagram



47.24. QSPI Module Electrical Specifications

Table 47-30. QSPI Module Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions(2)
QSPI_1	FCLK	QSPI Serial Clock Frequency (DIRECT)	—	—	32	MHz	Host SDR Transfer mode 0 and 3 VDDIOx = 3.3V, C_{LOAD} = 20 $pF_{(MAX)}$
			—	—	32	MHz	Host SDR Transfer mode 0 and 3 VDDIOx = 1.9V, C_{LOAD} = 20 pF(MAX)
			—	—	16	MHz	Host DDR Transfer mode 0 in Read only (BAUD.CPHA=0, BAUD.CPOL=0) VDDIOx = 3.3V, C_{LOAD} = 20 $pF_{(MAX)}$
			—	—	16	MHz	Host DDR Transfer mode 0 in Read only (BAUD.CPHA=0, BAUD.CPOL=0) VDDIOx = 1.9V, C_{LOAD} = 20 $pF_{(MAX)}$
	FCLK	QSPI Serial Clock Frequency(Remappable PPS)	—	—	16	MHz	Host SDR Transfer mode 0 and 3 VDDIOx = 3.3V, C_{LOAD} = 20 $pF_{(MAX)}$
			—	—	16	MHz	Host SDR Transfer mode 0 and 3 VDDIOx = 1.9V, C_{LOAD} = 20 pF(MAX)
			—	—	8	MHz	Host DDR Transfer mode 0 in Read only (BAUD.CPHA=0, BAUD.CPOL=0) VDDIOx = 3.3V, C_{LOAD} = 20 $pF_{(MAX)}$
			—	—	8	MHz	Host DDR Transfer mode 0 in Read only (BAUD.CPHA=0, BAUD.CPOL=0) VDDIOx = 1.9V, C_{LOAD} = 20 $pF_{(MAX)}$
QSPI_3	TSCKH	Serial Clock High Time	—	1/(2*FCLK)	—	ns	—
QSPI_5	TSCKL	Serial Clock Low Time	—	1/(2*FCLK)	—	ns	—
QSPI_7	TSCKR	Serial Clock Rise Time	—	—	DI27	ns	See parameter DI27 I/O spec
QSPI_9	TSCKF	Serial Clock Fall Time	—	—	DI25	ns	See parameter DI25 I/O spec

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Table 47-30. QSPI Module Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions(2)
QSPI_11	TCSS	CS Active Setup Time	5	—	—	ns	Configurable using BAUD.DLYBS register Min time at BAUD.DLYBS = 0 and Max QSPI peripheral Clock Frequency
QSPI_13	TCSH	CS Active Hold Time	5	—	—	ns	Configurable using CTRLB.DLYBCT register Min time at CTRLB.DLYBCT = 0 and Max QSPI peripheral Clock Frequency
QSPI_19	TDIS	Data In Setup Time	2.799	—	—	ns	Host SDR mode
			2.8	—	—	ns	Host DDR mode, SCLK Rise
			3.67	—	—	ns	Host DDR mode, SCLK Fall
QSPI_21	TDIH	Data In Hold Time	0.794	—	—	ns	Host SDR mode
			0.428	—	—	ns	Host DDR mode, SCLK Rise
			0.793	—	—	ns	Host DDR mode, SCLK Fall
QSPI_23	TDOH	Data Out Hold	0.376	—	—	ns	Host SDR mode
QSPI_25	TDOV	Data Out Valid	—	—	8.025	ns	Host SDR mode

Notes:

1. Assumes $V_{DDIOx\,(min)}$ and 30 pF external load on all QSPI pins unless otherwise noted.
2. These parameters are characterized, but not tested in manufacturing.

Table 47-31. QSPI Maximum Frequency Example

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp		
QSPI Mode	CLK_QSPI2X_AHB	CLK_QSPI_AHB	Max.fCPU	Max.QSPI Serial Clock Frequency(2)	Conditions
SDR	x	128 MHz	128 MHz	32 MHz	BAUD.BAUD[7:0] must be greater than 2 to ensure QSPI clock frequency. DIRECT Pin Configuration
	x	128 MHz	128 MHz	16 MHz	BAUD.BAUD[7:0] must be greater than 6 to ensure QSPI clock frequency. Remappable Pin Configuration
DDR	128	64 MHz	64 MHz	16 MHz	BAUD.BAUD[7:0] must be greater than 6 to ensure QSPI clock frequency. DIRECT Pin Configuration
	128	64 MHz	64 MHz	8 MHz	BAUD.BAUD[7:0] must be greater than 14 to ensure QSPI clock frequency. Remappable Pin Configuration

Notes:

1. Examples shown do not supersede the electrical specification shown in TABLE ____: QSPI MODULE ELECTRICAL SPECIFICATIONS.
2. Refer to QSPI_1 for maximum QSPI Serial Clock Frequency (FCLK) in SDR and DDR modes.

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47.25. CANx Module AC Electrical Specifications

Table 47-32. CANx Module AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics(1)	Min.	Typ	Max.	Units	Conditions
CAN_1	CANRATE	CAN data rate	—	—	10	Mbps	VDDIOx = 3.3V, C_{LOAD} = 30 $pF_{(MAX)}$.Note 3
			—	—	10		VDDIOx = 1.9V, C_{LOAD} = 30 $pF_{(MAX)}$. Note 3
CAN_3	CANFALL	Port 0utput Fall Time	—	—	DI_27 (1)	ns	See parameter DI27 I/O spec
CAN_4	CANRISE	Port 0utput Rise Time	—	—	DI_25 (1)	ns	See parameter DI25 I/O spec
CAN_7	fCAN_GCLK	CANx Input clk freq, GCLK_CAN	—	—	FCLK_25	MHz	—

Notes:

1. Assumes VDDIOx(min) and 30 pF external load on all CAN pins unless otherwise noted.
2. These parameters are characterized, but not tested in manufacturing.
3. The Max data rate is achieved using EPLL2 Max Frequency

CANx Module AC Timing Diagram

47.26. TCx Timer Capture Module AC Electrical Specifications

Table 47-33. TCx Timer Capture Module AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
TC_1	TC_{INLOW}	Capture TCx Input Low Time	2/128MHz	—	—	ns	VDDIOx(min) and meet TC_5 spec
TC_3	TC_{INHIGH}	Capture TCx Input High Time	2/128MHz	—	—	ns	VDDIOx(min) and meet TC_5 spec
TC_5	$TC_{INPERIOD}$	Capture Input Period	4/128MHz	—	—	ns	VDDIOx(min)
TC_7	TC_{OUTLOW}	Compare TCx Output Low Time	2/128MHz	—	—	ns	VDDIOx(min) and meet TC_11 spec
TC_9	$TC_{OUTHIGH}$	Compare TCx Output High Time	2/128MHz	—	—	ns	VDDIOx(min) and meet TC_11 spec
TC_11	$TC_{OUTPERIOD}$	Compare Output Period	TC_7+TC_9	—	—	ns	VDDIOx(min)
TC_13	fGCLK_TCx	TC peripheral module clock frequency	—	—	FCLK_37	MHz	VDDIOx(min)

Note: These parameters are characterized but not tested in manufacturing.

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Figure 47-11. TCx Timer Capture Input Module AC Timing Diagram

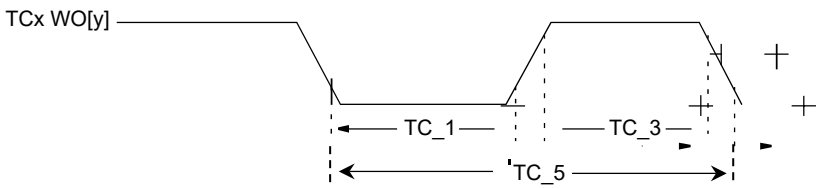
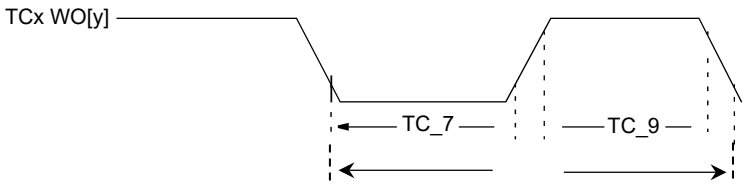


Figure 47-12. TCx Timer Capture Output Module AC Timing Diagram



47.27. TCCx Timer Capture Module AC Electrical Specifications

Table 47-34. TCCx Timer Capture Module AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions
TCC_1	TCCINLOW	Capture TCCx Input Low Time	2/128 MHz	—	—	ns	VDDIOx(min) and meet TCC_5 spec
TCC_3	TCCINHIGH	Capture TCCx Input High Time	2/128 MHz	—	—	ns	VDDIOx(min) and meet TCC_5 spec
TCC_5	TCCINPERIOD	Capture Input Period	4/128 MHz	—	—	ns	VDDIOx(min)
TCC_7	TCCOUTLOW	Compare TCCx Output Low Time	2/128 MHz	—	—	ns	VDDIOx(min) and meet TCC_11 spec
TCC_9	TCCOUTHIGH	Compare TCCx Output High Time	2/128 MHz	—	—	ns	VDDIOx(min) and meet TCC_11 spec
TCC_11	TCCOUTPERIOD	Compare Output Period	TCC_7+TCC_9	—	—	ns	VDDIOx(min)
TCC_13	fGCLK_TCCx	TCC peripheral module clock frequency	—	—	FCLK_35	MHz	
TCC_15	TCCFD	Fault Input to I/O Pin Change	—	—	63	ns	
TCC_17	TCCFLT	Fault Input Pulse Width	10	—	—	ns	

Note: These parameters are characterized but not tested in manufacturing.

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Figure 47-13. TCCx Timer Capture Input Module AC Timing Diagram

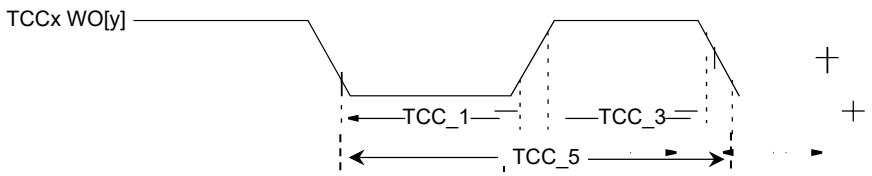


Figure 47-14. TCCx Timer Capture Output Module AC Timing Diagram

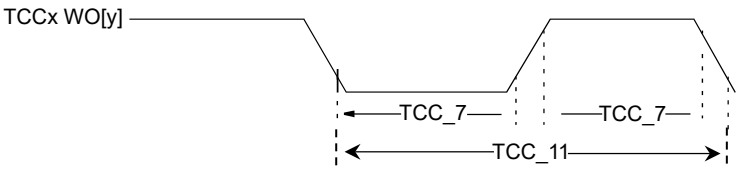
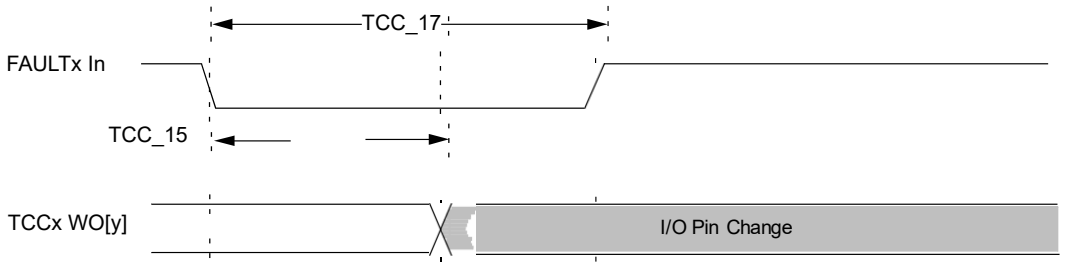


Figure 47-15. TCC_x Timer Compare Fault Output Module AC Timing Diagram



47.28. USB AC Electrical Specifications

Table 47-35. USB AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics(2)	Min.	Typ	Max.	Units	Conditions
USB_1	VDDUSB	USB Transceiver Voltage	3	—	3.6	V	Voltage on VDDIOx must be in this range for proper USB operation
VBUS Supply							
USB_7	VILUSB	Input Low Voltage for USB Buffer	—	—	DI_1	V	—
USB_9	VIHUSB	Input High Voltage for USB Buffer	DI_3	—	—	V	—
USB_11	VDIFS	Differential Input Sensitivity	0.2	—	—	V	The difference between D+ and D- must exceed this value while VCM is met
USB_13	VCM	Differential Common Mode Range	0.8	—	2.5	V	VUSB = 3.0V-to-3.6V
USB_15	ZOUT	Driver Output Impedance	28	—	44	W	—
USB_17	VOLUSB	Voltage Output Low	—	—	DI_5	V	1.425 kW load connected to VUSB = 3.6V

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Table 47-35. USB AC Electrical Specifications (continued)

AC Characteristics			Standard Operating Conditions: V_{DD} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics(2)	Min.	Typ	Max.	Units	Conditions
USB_19	VOHUSB	Voltage Output High	DI_9	—	—	V	14.25 kW load connected to ground w/VUSB = 3.0V
USB_21	VBUS	USB VBUS Input range		TBD	5.5	V	—
USB_23	USBCLKS(1)	USB Clock Source (1)GCLK_USB of 48 MHz	—	48	—	MHz	fUPLL = 96 MHz(1)

Notes:

1. External Crystal oscillator (POSC) as input clock source to UPLL for fUPLL of 96 MHz which is divided by 2 to get USBCLKS = 48 MHz. Required clock accuracy: High Speed = ±0.05%, Full Speed = ±0.25% (2500 ppm), Low Speed = ±1.5% (15000 ppm).
2. These parameters are characterized, but not tested in manufacturing.

47.29. FLASH NVM AC Electrical Specifications

Table 47-36. FLASH NVM AC Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics		Min.	Typical	Max.	Units	Conditions
NVM_1	FRETEN	Flash Data Retention		20	—	—	Yrs	Under all conditions less than Absolute Maximum Ratings specifications
NVM_3	EP	Cell Endurance (Flash Erase and Wite Operation)		20k	—	—	Cycles	
		Cell Endurance (Flash Erase/ Retry and Write Operation)		100k	—	—	Cycles	
NVM_5	FREAD	Flash Read	0 Wait States	—	—	25.6	MHz	VDDIO = 1.9V, CHECON.PFMWS[3:0]
			1 Wait States	—	—	51.2		
			2 Wait States	—	—	76.8		
			3 Wait States	—	—	102.4		
			4 Wait States	—	—	128		
			0 Wait States	—	—	64	MHz	VDDIO = 1.9V, CHECON.ADRWS
			1 Wait States	—	—	128		
NVM_7	TFPW	Program Cycle Time	Write Row	—	—	2.6	ms	—
NVM_9	TCE		Erase Chip	—	—	20	ms	—
NVM_11	TFEB		Erase Page	—	—	1.25	ms	20K Endurance
			Erase Page	—	—	8	ms	100K Endurance with Erase/ Retry

Note:

1. Maximum FLASH operating frequencies are given in the table above, but are limited by the Embedded Flash access time when the processor is fetching code out of it. This field defines the number of Wait states required to access the Embedded Flash Memory.

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47.30. GMAC Electrical Specifications

Table 47-37. RMII ETHERNET Module AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MDC/MDIO AC Timing Requirements							
ET_1a	$tMDIO_{SU}$	MDIO Set-up Time	22	—	—	ns	VDDIO = 1.9V with CLOAD = 10 pF
ET_3a	$tMDIO_{HOLD}$	MDIO Hold Time	0	—	—	ns	
ET_5a	$tMDIO_{VAL}$	MDIO OUTPUT Valid Time	0.4	—	9.2	ns	
ET_6	tMDCcyc	MDC CLK period(1)	400	—	—	ns	
RMII AC Timing Requirements							
ET_29	$tREF_{CLK}$	Reference Clock Frequency	—	50	—	MHz	For 100/10 BASE with CLOAD = 10 pF
ET_31	$tREF_{CLKIH}$	Reference Clock High Time	—	tREFCLK / 2	—	ns	VDDIO = 1.9V with CLOAD = 10 pF
ET_33	$tREF_{CLKIL}$	Reference Clock Low Time	—	tREFCLK / 2	—	ns	
ET_35	REF_{CLKDC}	Reference Clock Duty Cycle	—	50	—	%	
ET_37	$REF_{CLKJITTER}$	Reference Clock Jitter	—	TBD		ps	
ET_41	$tRX[1:0]_{SU}$ $tRXER_{SU}$	RXD[1:0], RXER Set-up time	4	—	—	ns	
ET_43	$tRX[1:0]_{HOLD}$ $tRXER_{HOLD}$	RXD[1:0], RXER hold time	2.5	—	—	ns	
ET_45	$tTX[1:0]_{VAL}$ $tTXEN_{VAL}$	TX[1:0], TXEN output valid time	5	—	12	ns	

Note:
1. The max MDC Clock is achieved using 80 MHz EPLL clock as system clock.

47.31. Frequency Meter AC Electrical Specifications

Table 47-38. Frequency Meter AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics(1)	Min.	Typical	Max.	Units	Conditions
FM_1	FMLOW	REFI Input Low Time	5	—	—	ns	VDDIOx(min) and meet FM5 spec
FM_3	FMHIGH	REFI Input High Time	5	—	—	ns	
FM_5	FMPERIOD	REFI Input Period	1/64MHz	—	—	ns	VDDIOx(min)
FM_7	fGCLK_FREQM_REF	FREQM Reference	—	—	FCLK_17	MHz	
FM_9	fGCLK_FREQM_MSR	FREQM Measure	—	—	FCLK_15	MHz	

Note:
1. These parameters are characterized, but not tested in manufacturing.

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47.32. Quadrature Encoder Interface AC Electrical Specifications

Table 47-39. Quadrature Encoder Interface AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
PDEC_1	TtPH	TQCK high time	1.5/fGCLK_QEI	—	—	ns	VDDIOx(min) -to-VDDIOx(max)
PDEC_3	TtPL	TQCK low time	1.5/fGCLK_QEI	—	—	ns	
PDEC_5	TtPP	TQCK input period	3/fGCLK_QEI	—	—	ns	
PDEC_7	TCKEXTDLY	Delay from External TxCK Clock Edge to counter Increment		—	5/fGCLK_QEI	ns	
PDEC_11	TPDH	QE Input High Time (Digital Filter Disabled)	6/fGCLK_QEI	—	—	ns	
		QE Input High Time (Digital Filter Enabled)	6*N/fGCLK_QEI	—	—	ns	N = 1, 2, 4, 8, 16, 32, 64, 128
PDEC_13	TPDL	QE Input Low Time (Digital Filter Disabled)	6/fGCLK_QEI	—	—	ns	—
		QE Input Low Time (Digital Filter Enabled)	6*N/fGCLK_QEI	—	—	ns	N = 1, 2, 4, 8, 16, 32, 64, 128
PDEC_15	TPDIN	QE Input Period (Digital Filter Disabled)	12/fGCLK_QEI	—	—	ns	—
		QE Input Period (Digital Filter Enabled)	12*N/fGCLK_QEI	—	—	ns	N = 1, 2, 4, 8, 16, 32, 64, 128
PDEC_17	TPDP	QE Phase Period (Digital Filter Disabled)	3/fGCLK_QEI	—	—	ns	
		QE Phase Period (Digital Filter Enabled)	3*N/fGCLK_QEI	—	—	ns	N = 1, 2, 4, 8, 16, 32, 64, 128
PDEC_19	TPDIDX	Index Pulse Width, Digital Filter Disabled	3/fGCLK_QEI	—	15/fGCLK_QEI	ns	—
		Index Pulse Width, Digital Filter Enabled	3*N/fGCLK_QEI	—	15*N/fGCLK_QEI	ns	N = 1, 2, 4, 8, 16, 32, 64, 128
PDEC_21	TPDFH	Filter Time to Recognize High, with Digital Filter	6/fGCLK_QEI	—	—	ns	—
PDEC_23	TPDFL	Filter Time to Recognize Low, with Digital Filter	6/fGCLK_QEI	—	—	ns	—
PDEC_24	fGCLK_QEI	CLK_QEI	—	—	FCLK_41	MHz	—

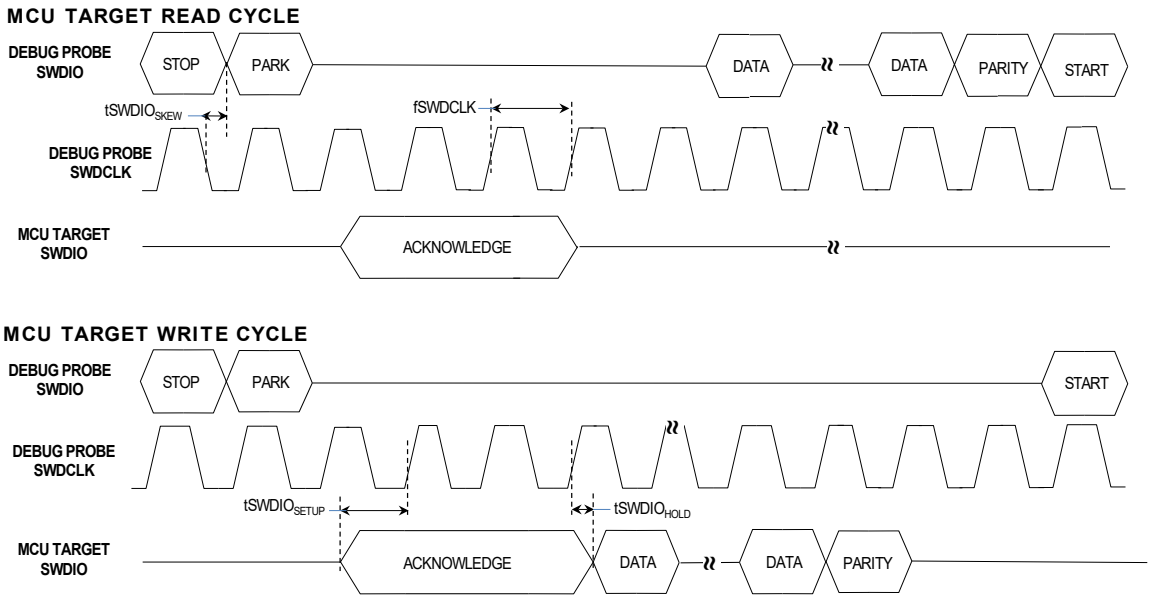
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47.33. SWD 2-Wire AC Electrical Specifications

Table 47-40. SWD 2-Wire AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
SWD_1	fSWDCLK	SWDCLK Clock Frequency	—	—	25	MHz	VDDIO(min) - VDDIO(max)
SWD_3	$tSWDCLK_{HIGH}$	SWDCLK Clock High Time	—	1 / (2 * fSWDCLK)	—	ns	
SWD_5	$tSWDCLK_{LOW}$	SWDCLK Clock Low Time	—	1 / (2 * fSWDCLK)	—	ns	
SWD_7	$tSWDIO_{SKEW}$	SWDIO Output Skew	-5	—	5	ns	
SWD_9	$tSWDIO_{SETUP}$	SWDIO Setup Time (Target Output)	4	—	—	ns	
SWD_11	$tSWDIO_{HOLD}$	SWDIO Hold Time (Target Output)	1	—	—	ns	

Figure 47-16. SWD 2-Wire Read/Write AC Timing Diagram



47.34. Bluetooth Low Energy RF Characteristics

Table 47-41. sBluetooth Low Energy RF Characteristics

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
BTG1	FREQ	Frequency Range of operation	2402	—	2480	MHz	—
BTTX1	TXPWR:PA	Bluetooth Transmit Power PA	—	11	—	dBm	—

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Table 47-41. sBluetooth Low Energy RF Characteristics (continued)

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
BTX2	TXIB:1MBPS	In-band emission for FTX±2 MHz	—	-42	—	dBm	—
		In-band emission for FTX±(3+N) MHz	—	-48	—	dBm	—
BTX3	TXIB:2MBPS	In-band emission for FTX±4 MHz	—	-49	—	dBm	—
		In-band emission for FTX±5 MHz	—	-52	—	dBm	—
		In-band emission for FTX±(6+N) MHz	—	-55	—	dBm	—
BTRX1	RXSENSE	Receiver Sensitvity at 1 Mbps	—	-99	—	dBm	—
		Receiver Sensitvity at 2 Mbps	—	-96	—	dBm	—
		Receiver Sensitvity at S=8	—	-108	—	dBm	—
		Receiver Sensitvity at S=2	—	-103	—	dBm	
BTRX2	MAXINSIG	Maximum Input signal level at 1 Mbps	—	0	—	dBm	—
		Maximum Input signal level at 2 Mbps	—	0	—	dBm	—
		Maximum Input signal level at S=2	—	0	—	dBm	—
		Maximum Input signal level at S=8	—	0	—	dBm	—
BTRX3	CI1M:COCH	C/I Co channel Rejection	—	13	—	dB	—
	CI1M:±1 MHz	C/I Adjacent Channel Rejection	—	15	—	dB	—
	CI1M:±2 MHz	C/I Adjacent Channel Rejection	—	7	—	dB	—
	CI1M:ADJ(3+n)	C/I Alternate Channel Rejection	—	6	—	dB	—
	CI1M:IMG	C/I Image Frequency Rejection	—	11	—	dB	—
	CI1M:IMG±1 MHz	C/I Adjacent Channel to Image Freq Rejection	—	12	—	dB	—
BTRX4	CIS2:COCH	C/I Co channel Rejection	—	11	—	dB	—
	CIS2:±1 MHz	C/I Adjacent Channel Rejection	—	19	—	dB	—
	CIS2:±2 MHz	C/I Adjacent Channel Rejection	—	18	—	dB	—
	CIS2:ADJ(3+n)	C/I Alternate Channel Rejection	—	7	—	dB	—
	CIS2:IMG	C/I Image Frequency Rejection	—	18	—	dB	—
	CIS2:IMG±1 MHz	C/I Adjacent Channel to Image Freq Rejection	—	13	—	dB	—

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Table 47-41. sBluetooth Low Energy RF Characteristics (continued)

DC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
BTRX5	CIS8:COCH	C/I Co channel Rejection	—	3	—	dB	—
	CIS8:±1 MHz	C/I Adjacent Channel Rejection	—	20	—	dB	—
	CIS8:±2 MHz	C/I Adjacent Channel Rejection	—	14	—	dB	—
	CIS8:ADJ(3+n)	C/I Alternate Channel Rejection	—	3	—	dB	—
	CIS8:IMG	C/I Image Frequency Rejection	—	14	—	dB	—
	CIS2:IMG±1 MHz	C/I Adjacent Channel to Image Freq Rejection	—	15	—	dB	—
BTRX6	CI2M:COCH	C/I Co channel Rejection	—	12	—	dB	—
	CI2M:±2 MHz	C/I Adjacent Channel Rejection	—	14	—	dB	—
	CI2M:±4 MHz	C/I Adjacent Channel Rejection	—	12	—	dB	—
	CI2M:ADJ(6+2n)	C/I Alternate Channel Rejection	—	14	—	dB	—
	CI2M:IMG	C/I Image Frequency Rejection	—	13	—	dB	—
	CI2M:IMG±2 MHz	C/I Adjacent Channel to Image Freq Rejection	—	14	—	dB	—
BTRX7	BLOCK1M:<2 GHZ	Blocking performance from 30 MHz to 2 GHz	—	20	—	dB	—
	BLOCK1M:2 GHZ<SIG<2399 MHz	Blocking performance from 2003 MHzto 2399 MHz	—	20	—	dB	—
	BLOCK1M:2484 MHZ<SIG<2977 MHz	Blocking performance between 2484 MHz to 2997 MHz	—	20	—	dB	—
	BLOCK1M:3 GHZ<SIG<12.75 GHz	Blocking Performance between 3 GHz to 12.5 GHz	—	20	—	dB	—
BTRX8	BLE1M:INTERMOD	Inter modulation performance for BLEM	—	8.5	—	dB	—
	BLE2M:INTERMOD	Inter modulation performance for BLEM	—	9.5	—	dB	—

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Table 47-42. Bluetooth Low Energy RF Current Consumption

DC Characteristics					Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	RF Power	CPU Frequency	Min.	Typ	Max.	Units	Conditions
IBLETX_1	IDDTXPA1M	Current Consumption with TX in MLDO mode at 1 Mbps	+11 dBm	128 MHz	—	61.4	—	mA	VDD = 3.3V; Temp=25°C CPU Consumption included
			+11 dBm	64 MHz	—	50.6	—	mA	
			+11 dBm	32 MHz	—	45.1	—	mA	
			0 dBm	128 MHz	—	36.7	—	mA	
			0 dBm	64 MHz	—	25.7	—	mA	
			0 dBm	32 MHz	—	20.2	—	mA	
IBLETX_3	IDDTXPA1B	Current Consumption with TX in Buck mode at1 Mbps	+11 dBm	128 MHz	—	31.2	—	mA	
			+11 dBm	64 MHz	—	25.8	—	mA	
			+11 dBm	32 MHz	—	23.1	—	mA	
			0 dBm	128 MHz	—	19.2	—	mA	
			0 dBm	64 MHz	—	13.9	—	mA	
			0 dBm	32 MHz	—	11.3	—	mA	
IBLERX_1	IDDRXBLE1M	Current consumption at Rx signal MLDO mode at1 Mbps	-80 dBm	128 MHz	—	31.1	—	mA	
			-80 dBm	64 MHz	—	20.1	—	mA	
			-80 dBm	32 MHz	—	14.5	—	mA	
IBLERX_3	IDDRXBLE1B	Current consumption at Rx signal BUCK mode at1 Mbps	-80 dBm	128 MHz	—	16.6	—	mA	
			-80 dBm	64 MHz	—	11.4	—	mA	
			-80 dBm	32 MHz	—	8.7	—	mA	

47.35. 802.15.4 RF Characteristics

Table 47-43. 802.15.4 RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
ZBG1	FREQ	Frequency Range	2405	—	2480	MHz	—
ZBG2	FCH	Channel Spacing	—	5	—	MHz	—
ZBG3	PSDU	Bit rate	—	250	2000	kbps	—
ZBT1	TXOPPA	Transmit Output Power PA	—	11	—	dBm	—
ZBT2	POWERRANGE	Output Power Range	-12	—	11	dBm	—
ZBT3	EVM	Error Vector Magnitude	—	4.5	—	%RMS	—
ZBT4	MPA2HAR	Second Harmonic from MPA	—	-47	—	dBm	—
ZBT5	MPA3HAR	Third Harmonic from MPA	—	-45	—	dBm	—

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Table 47-43. 802.15.4 RF Characteristics (continued)

AC Characteristics			Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
ZBRX1	SENS	Receiver Sensitivity in 250 kbs	—	-103	—	dBm	—
		Receiver Sensitivity in 500 kbps	—	-100	—	dBm	—
		Receiver Sensitivity in 1 Mbps	—	-97	—	dBm	—
		Receiver Sensitivity in 2 Mbps	—	-91	—	dBm	—
ZBRX2	PMAX	Maximum Input Level	—	0	—	dBm	—
ZBRX3	PACRP	Adjacent Channel Rejection +5MHz	—	20	—	dB	—
ZBRX4	PACRN	Adjacent Channel Rejection -5 MHz	—	18	—	dB	—
ZBRX5	PALRP	Alternate Channel Rejection +10 MHz	—	15	—	dB	—
ZBRX6	PALRN	Alternate Channel Rejection -10 MHz	—	13	—	dB	—
ZBRX7	RSSIRANGE	Dynamic Range of RSSI	—	80	—	dB	—
ZBRX8	RSSIRES	Resolution of RSSI	—	1	—	dB	—
ZBRX9	RSSIBASEVAL	Minimum value of RSSI	—	-100	—	dBm	—

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Table 47-44. 802.15.4 RF Current Characteristics

AC Characteristics					Standard Operating Conditions: V_{DD33} = V_{DDIO} = AV_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	RF Power	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IZBTX_1	IDDTX	TX Current Consumption in MLDO mode at 250 kbps	+11 dBm	128 MHz	—	62.1	—	mA	VDD = 3.3V; Temp = 25°C CPU Consumption included
			+11 dBm	64 MHz	—	50.8	—	mA	
			+11 dBm	32 MHz	—	44.9	—	mA	
			10 dBm	128 MHz	—	56.5	—	mA	
			10 dBm	64 MHz	—	45.2	—	mA	
			10 dBm	32 MHz	—	39.2	—	mA	
			1 dBm	128 MHz	—	37.7	—	mA	
			1 dBm	64 MHz	—	26.5	—	mA	
			1 dBm	32 MHz	—	20.7	—	mA	
IZBTX_3	IDDTX	TX Current Consumption in BUCK mode at 250 kbps	+11 dBm	128 MHz	—	31.5	—	mA	
			+11 dBm	64 MHz	—	25.8	—	mA	
			+11 dBm	32 MHz	—	23	—	mA	
			10 dBm	128 MHz	—	28.7	—	mA	
			10 dBm	64 MHz	—	23.1	—	mA	
			10 dBm	32 MHz	—	20.2	—	mA	
			1 dBm	128 MHz	—	19.6	—	mA	
			1 dBm	64 MHz	—	14.2	—	mA	
			1 dBm	32 MHz	—	11.5	—	mA	
IZBRX_1	IDDRXZB	Current consumption in MLDO mode at 250 kbps	-95 dBm	128 MHz	—	32	—	mA	
			-95 dBm	64 MHz	—	21	—	mA	
			-95 dBm	32 MHz	—	15.3	—	mA	
	IDDRXZBRPC		—	128 MHz	—	29.9	—	mA	
			—	64 MHz	—	19	—	mA	
			—	32 MHz	—	13.4	—	mA	
IZBRX_3	IDDRXZB	Current consumption in BUCK mode at 50 kbps	-95 dBm	128 MHz	—	17	—	mA	
			-95 dBm	64 MHz	—	11.7	—	mA	
			-95 dBm	32 MHz	—	9.1	—	mA	
	IDDRXZBRPC		—	128 MHz	—	16	—	mA	
			—	64 MHz	—	10.8	—	mA	
			—	32 MHz	—	8.2	—	mA	

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