

RX23W Group

User's Manual: Hardware

RENESAS 32-Bit MCU
RX Family / RX200 Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.

This manual is organized in the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI, take all points to note into account. Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

The following documents have been prepared for the RX23W Group. Before using any of the documents, please visit our website to verify that you have the most up-to-date available version of the document.

Document Type	Contents	Document Title	Document No.
Datasheet	Overview of hardware and electrical characteristics	RX23W Group Datasheet	R01DS0342EJ
User's Manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, and timing charts) and descriptions of operation	RX23W Group User's Manual: Hardware	This User's manual
User's Manual: Software	Detailed descriptions of the CPU and instruction set	RX Family RXv2 Instruction Set Architecture User's Manual: Software	R01US0071EJ
Application Note	Notes on Printed Circuit Board Patterns	RX Family Hardware Design Guide	R01AN1411EJ
	Examples of register initial setting	—	—
	Examples of applications and sample programs	—	—
Renesas Technical Update	Preliminary report on the specifications of a product, document, etc.	—	—

2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

X.X.X ... Register

Address(es): xxxx xxxh

b7	b6	b5	b4	b3	b2	b1	b0
—	...[1:0]	...4	—	—	—	—	...0
Value after reset:	x	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	...0		0: 1: (Setting prohibited) (3)	R/W (1)
b3 to b1	—	(Reserved) (2)	These bits are read as 0. The write value should be 0.	R/W
b4	...4		0: 1:	R
b6, b5	...[1:0]		0 0: 0 1: (Settings other than above are prohibited.) (3)	R/(W)*1
b7	—	Reserved	The read value is undefined. Writing to this bit has no effect.	R

- (1) R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit or field is readable. Writing to this bit or field has no effect.
- (2) Reserved.
Use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.
- (3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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54-MHz 32-bit RX MCUs, built-in FPU, 88.56 DMIPS, up to 512-KB flash memory, *Bluetooth*® 5.0, various communication functions including USB 2.0 full-speed host/function/OTG, CAN, SD host interface, serial sound interface, capacitive touch sensing unit, 12-bit A/D converter, 12-bit D/A converter, RTC, Encryption functions

Features

■ 32-bit RXv2 CPU core

- Max. operating frequency: 54 MHz
Capable of 88.56 DMIPS in operation at 54 MHz
- Enhanced DSP: 32-bit multiply-accumulate and 16-bit multiply-subtract instructions supported
- Built-in FPU: 32-bit single-precision floating point (compliant to IEEE754)
- Divider (fastest instruction execution takes two CPU clock cycles)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit
- Memory protection unit (MPU) supported

■ Low power design and architecture

- Operation from a single 1.8-V to 3.6-V supply
- RTC capable of operating on the battery backup power supply
- Three low power consumption modes
- Low power timer (LPT) that operates during the software standby state

■ On-chip flash memory for code

- 384- to 512-Kbyte capacities
- On-board or off-board user programming
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory

- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states

- 64-Kbyte size capacities

■ Data transfer functions

- DMAC: Incorporates four channels
- DTC: Four transfer modes

■ ELC

- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

■ Reset and supply management

- Eight types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions

- Main clock oscillator frequency: 1 to 20 MHz
- External clock input frequency: Up to 20 MHz
- Sub-clock oscillator frequency: 32.768 kHz
- Frequency of Bluetooth-dedicated clock oscillator: 32 MHz
- PLL circuit input: 4 MHz to 12.5 MHz
- On-chip low- and high-speed oscillators, dedicated on-chip low-speed oscillator for the IWDt
- USB-dedicated PLL circuit: 4, 6, 8, or 12 MHz
54 MHz can be set for the system clock and 48 MHz for the USB clock
- Generation of a dedicated 32.768-kHz clock for the RTC
- Clock frequency accuracy measurement circuit (CAC)

■ Realtime clock

- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable
- Time capture function
- Time capture on event-signal input through external pins

■ Independent watchdog timer

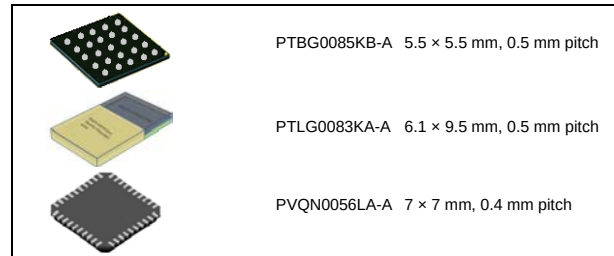
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDt operation.

■ Useful functions for IEC60730 compliance

- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.

■ Capacitive touch sensing unit

- Self-capacitance method: A single pin configures a single key, supporting up to 12 keys
- Mutual capacitance method: Matrix configuration with 12 pins, supporting up to 36 keys



■ Up to 12 communication functions

- Bluetooth Low Energy (1 channel)
An RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification
LE 1M PHY, LE 2M PHY, LE Coded PHY (125 kbps and 500 kbps), and LE Advertising extension support
On-chip Bluetooth-dedicated AES-CCM (128-bit blocks) encryption circuit
The 83-pin LGA product has been certified as compliant with radio-related laws (in Japan, North America, and Europe).
The 83-pin LGA product includes a small PCB trace antenna.
- USB 2.0 host/function/On-The-Go (OTG) (one channel), full-speed = 12 Mbps, low-speed = 1.5 Mbps, isochronous transfer, and BC (Battery Charger) supported
- CAN (one channel) compliant to ISO11898-1:
Transfer at up to 1 Mbps
- SCI with many useful functions (up to 4 channels)
Asynchronous mode, clock synchronous mode, smart card interface
Reduction of errors in communications using the bit modulation function
- IrDA interface (one channel, in cooperation with the SCI5)
- I²C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPi (one channel): Transfer at up to 16 Mbps
- Serial sound interface (one channel)
- SD host interface (optional: one channel) SD memory/ SDIO 1-bit or 4-bit SD bus supported

■ Up to 19 extended-function timers

- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (five channels)
- 16-bit TPU: input capture, output compare, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (four channels)

■ 12-bit A/D converter

- Capable of conversion within 0.83 μs
- 14 channels
- Sampling time can be set for each channel
- Self-diagnostic function and analog input disconnection detection assistance function

■ 12-bit D/A converter

- Two channels

■ Analog comparator

- Two channels × one unit

■ General I/O ports

- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Encryption functions (TSIP-Lite)

- Unauthorized access to the encryption engine is disabled and imposture and falsification of information are prevented
- Safe management of keys
- 128- or 256-bit key length of AES for ECB, CBC, GCM, others
- True random number generator

■ Temperature sensor

■ Operating temperature range

- -40 to +85°C

■ Applications

- 85-pin BGA, 56-pin QFN: General industrial and consumer equipment
- 83-pin LGA: Consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.

Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/5)

Classification	Module/Function	Description
CPU	CPU	- Maximum operating frequency: 54 MHz 32-bit RX CPU (RX v2) - Minimum instruction execution time: One instruction per clock cycle - Address space: 4-Gbyte linear - Register set - General purpose: Sixteen 32-bit registers - Control: Ten 32-bit registers - Accumulator: Two 72-bit registers - Basic instructions: 75 (variable-length instruction format) - Floating-point instructions: 11 - DSP instructions: 23 - Addressing modes: 10 - Data arrangement - Instructions: Little endian - Data: Selectable as little endian or big endian - On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit - On-chip divider: 32-bit ÷ 32-bit → 32 bits - Barrel shifter: 32 bits - Memory protection unit (MPU)
	FPU	- Single precision (32-bit) floating point - Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	- Capacity: 384/512 Kbytes - Up to 32 MHz: No-wait memory access 32 to 54 MHz: Wait state required. No wait state if the instruction is served by a ROM accelerator hit. - Programming/erasing method: - Serial programming (asynchronous serial communication/USB communication), self-programming
	RAM	- Capacity: 64 Kbytes 54 MHz, no-wait memory access
	E2 DataFlash	- Capacity: 8 Kbytes - Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	- Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, USB-dedicated PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator, Bluetooth-dedicated clock oscillator, Bluetooth-dedicated low-speed on-chip oscillator - Oscillation stop detection: Available - Clock frequency accuracy measurement circuit (CAC) - Independent settings for the system clock (ICKL), peripheral module clock (PCLK), and FlashIF clock (FCLK) - The CPU and system sections such as other bus masters run in synchronization with the system clock (ICKL): 54 MHz (at max.) - MTU2a runs in synchronization with the PCLKA: 54 MHz (at max.) - The ADCLK for the S12AD runs in synchronization with the PCLKD: 54 MHz (at max.) - Peripheral modules other than MTU2a and S12ADE run in synchronization with the PCLKB: 32 MHz (at max.) - The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	- When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. - Voltage detection circuit 0 is capable of selecting the detection voltage from 3 levels - Voltage detection circuit 1 is capable of selecting the detection voltage from 10 levels

Table 1.1 Outline of Specifications (2/5)

Classification	Module/Function	Description
Low power consumption	Low power consumption functions	- Module stop function - Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode - Low power timer that operates during the software standby state
	Function for lower operating power consumption	Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	- Interrupt vectors: 148 - External interrupts: 7 (NMI, IRQ0, IRQ1, IRQ4 to IRQ7 pins) - Non-maskable interrupts: 6 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, WDT interrupt, IWDI interrupt, and VBATT power monitoring interrupt) 16 levels specifiable for the order of priority
DMA	DMA controller (DMACA)	4 channels - Three transfer modes: Normal transfer, repeat transfer, and block transfer - Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	- Transfer modes: Normal transfer, repeat transfer, and block transfer - Activation sources: Interrupts - Chain transfer function
I/O ports	General I/O ports	85-pin/83-pin/56-pin I/O: 43/43/29 - Input: 1/1/1 Pull-up resistors: 43/43/29 - Open-drain outputs: 31/31/24 5-V tolerance: 5/5/4
Event link controller (ELC)		- Event signals of 59 types can be directly connected to the module - Operations of timer modules are selectable at event input - Capable of event link operation for port B and port E
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	16-bit timer pulse unit (TPUa)	(16 bits × 6 channels) × 1 unit - Maximum of 10 pulse-input/output possible - Select from among seven or eight counter-input clock signals for each channel - Supports the input capture/output compare function - Output of PWM waveforms in up to 9 phases in PWM mode - Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade connected operation (32 bits × 2 channels) depending on the channel. - Capable of generating conversion start triggers for the A/D converters - Signals from the input capture pins are input via a digital filter - Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	(16 bits × 5 channels) × 1 unit - Up to 15 pulse-input/output lines are available based on the six 16-bit timer channels - Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD). - Input capture function 18 output compare/input capture registers - Pulse output mode - Complementary PWM output mode - Reset synchronous PWM mode - Phase-counting mode - Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	(16 bits × 2 channels) × 2 units - Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDTA)	14 bits × 1 channel - Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)

Table 1.1 Outline of Specifications (3/5)

Classification	Module/Function	Description
Timers	Independent watchdog timer (IWDtA)	14 bits × 1 channel - Count clock: Dedicated low-speed on-chip oscillator for the IWDtA Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTcE)	- Clock source: Sub-clock - Time/calendar - Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt - Time-capture facility for two values
	Low power timer (LPT)	16 bits × 1 channel - Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDtA Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	(8 bits × 2 channels) × 2 units - Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected - Pulse output and PWM output with any duty cycle are available - Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SClG, SClH)	4 channels (channel 1, 5, 8: SClG, channel 12: SClH) - SClG - Serial communications modes: Asynchronous, clock synchronous, and smart-card interface - Multi-processor function - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Average transfer rate clock can be input from TMR timers for SCl5, and SCl12 - Start-bit detection: Level or edge detection is selectable. - Simple I²C - Simple SPI 9-bit transfer mode - Bit rate modulation - Event linking by the ELC (only on channel 5) - SClH (The following functions are added to SClG) - Supports the serial communications protocol, which contains the start frame and information frame - Supports the LIN format
	IrDA interface (IrDA)	1 channel (SCl5 used) - Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I ² C bus interface (RIICa)	1 channel - Communications formats: I²C bus format/SMBus format - Master mode or slave mode selectable - Supports fast mode
	Serial peripheral interface (RSPiA)	1 channel - Transfer facility - Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPi clock) enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) - Capable of handling serial transfer as a master or slave - Data formats - Choice of LSB-first or MSB-first transfer - The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception - Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) - Double buffers for both transmission and reception
	USB 2.0 host/function module (USBc)	- USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. - Host/function module: 1 port - Compliant with USB version 2.0 - Transfer speed: Full-speed (12 Mbps), low-speed (1.5 Mbps) - OTG (ON-The-Go) is supported. - Isochronous transfer is supported. - BC1.2 (Battery Charging Specification Revision 1.2) is supported.
	CAN module (RSCAN)	1 channel - Compliance with the ISO11898-1 specification (standard frame and extended frame) 16 Message boxes

Table 1.1 Outline of Specifications (4/5)

Classification	Module/Function	Description
Communication functions	Serial Sound Interface (SSI)	• 1 channel • Capable of duplex communications • Various serial audio formats supported • Master/slave function supported • Programmable word clock or bit clock generation function • 8/16/18/20/22/24/32-bit data formats supported • On-chip 8-stage FIFO for transmission/reception • Supports WS continue mode in which the SSIWS signal is not stopped.
	SD Host Interface (SDHIA)	• 1 channel • Transfer speed: Default speed mode (8MB/s) • SD memory card interface (1 bit / 4bits SD bus) • MMC, eMMC Backward-compatible are supported. • SD Specifications - Part 1: Compliant with Physical Layer Specification Ver.3.01 (Not support DDR) - Part E1: SDIO Specification Ver. 3.00 • Error check function: CRC7 (command), CRC16 (data) • Interrupt Source: Card access interrupt, SDIO access interrupt, Card detection interrupt, SD buffer access interrupt • DMA transfer sources: SD_BUF write, SD_BUF read • Card detection, Write protection
	Bluetooth low energy (BLE)	• On-chip RF transceiver and link layer compliant with the Bluetooth 5.0 Low Energy specification • Bit rates: 1 Mbps, 2 Mbps, 500 kbps, and 125 kbps • LE Advertising extension support • Includes an RF transceiver power supply (selectable as a DC-to-DC converter or linear regulator) • On-chip matching circuit to help reduce the number of external parts • Transmission power: +4 dBm support • Small PCB trace antenna • Certified as compliant with radio-related laws • Bluetooth-dedicated clock oscillator
Encryption functions		• Access management circuit • Encryption engine 128- or 256-bit key sizes of AES - Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Prevention from illicit copying of a key
12-bit A/D converter (S12ADE)		• 12 bits (14 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 0.83 μs per channel when the ADCLK is operating at 54 MHz • Operating modes - Scan mode (single scan mode, continuous scan mode, and group scan mode) - Group A priority control (only for group scan mode) • Sampling variable - Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • A/D conversion start conditions - A software trigger, a trigger from a timer (MTU, TPU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
12-bit D/A converter (R12DAA)		• 2 channels • 12-bit resolution • Output voltage: 0.4 to AVCC0-0.5V
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels × 1 unit • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSU)		Detection pin: 12 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 3.6 V: 54 MHz
Operating temperature range		D version: -40 to +85°C

Table 1.1 **Outline of Specifications (5/5)**

Classification	Module/Function	Description
Packages		85-pin BGA (PTBG0085KB-A) 5.5 × 5.5 mm, 0.5 mm pitch 83-pin LGA (PTLG0083KA-A) 6.1 × 9.5 mm, 0.5 mm pitch 56-pin QFN (PVQN0056LA-A) 7 × 7 mm, 0.4 mm pitch
Debugging interfaces		FINE interface

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX23W Group		
		56 Pins	83 Pins	85 Pins
External bus	External bus	Not supported		
Interrupts	External interrupts	NMI, IRQ0, IRQ1, IRQ4 to IRQ7		
DMA	DMA controller	4 channels (DMAC0 to DMAC3)		
	Data transfer controller	Available		
Timers	16-bit timer pulse unit	5 channels (TPU0 to TPU3, TPU5)	6 channels (TPU0 to TPU5)	
	Multi-function timer pulse unit 2	5 channels (MTU0 to MTU4)		
	Port output enable 2	POE0#, POE8#	POE0#, POE1#, POE3#, POE8#	
	8-bit timer	2 channels × 2 units		
	Compare match timer	2 channels × 2 units		
	Low power timer	1 channel		
	Realtime clock	Available		
	Watchdog timer	Available		
	Independent watchdog timer	Available		
Communication functions	Serial communications interfaces (SCIg)	3 channels (SCI1, 5, 8)		
	IrDA interface	1 channel (SCI5)		
	Serial communications interfaces (SCIh)	Not supported	1 channel (SCI12)	
	I ² C bus interface	1 channel		
	CAN module	1 channel		
	Serial peripheral interface	1 channel		
	USB 2.0 host/function module	1 channel		
	Serial sound interface	1 channel		
	SD Host Interface	Not supported	1 channel	
	Bluetooth low energy	An RF transceiver and link layer compliant with Bluetooth 5.0 low energy specification		
Capacitive touch sensing unit		9 channels	12 channels	
12-bit A/D converter (including high-precision channels)		8 channels (4 channels)	14 channels (8 channels)	
Temperature sensor		Available		
D/A converter		1 channel	2 channels	
CRC calculator		Available		
Event link controller		Available		
Comparator B		2 channels		
RF transceiver power supply		DC-to-DC converter and linear regulator are selectable	Linear regulator	DC-to-DC converter and linear regulator are selectable
Small PCB trace antenna		Not supported	Included	Not supported
Bluetooth-dedicated clock oscillator		Not supported	Included	Not supported
Certificates of compliance with radio-related laws (technical standards, FCC, ISED, and CE)		—	Confirmed	—
Packages		56-pin QFN	83-pin LGA	85-pin BGA

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products: D Version ($T_a = -40$ to $+85^\circ\text{C}$)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency	Security Function	Antenna	Operating Temperature
RX23W	R5F523W8ADBL	R5F523W8ADBL#20	PTBG0085KB-A	512 Kbytes	64 Kbytes	8 Kbytes	54 MHz	Not available	Not included	−40 to +85°C
	R5F523W8CDLN	R5F523W8CDLN#U0	PTLG0083KA-A					Not available	Included	
	R5F523W8ADNG	R5F523W8ADNG#30	PVQN0056LA-A					Not available	Not included	
	R5F523W8BDBL	R5F523W8BDBL#20	PTBG0085KB-A					Available	Not included	
	R5F523W8DDLN	R5F523W8DDLN#U0	PTLG0083KA-A					Available	Included	
	R5F523W8BDNG	R5F523W8BDNG#30	PVQN0056LA-A					Available	Not included	
	R5F523W7ADBL	R5F523W7ADBL#20	PTBG0085KB-A	384 Kbytes				Not available	Not included	
	R5F523W7ADNG	R5F523W7ADNG#30	PVQN0056LA-A					Not available	Not included	
	R5F523W7BDBL	R5F523W7BDBL#20	PTBG0085KB-A					Available	Not included	
	R5F523W7BDNG	R5F523W7BDNG#30	PVQN0056LA-A					Available	Not included	

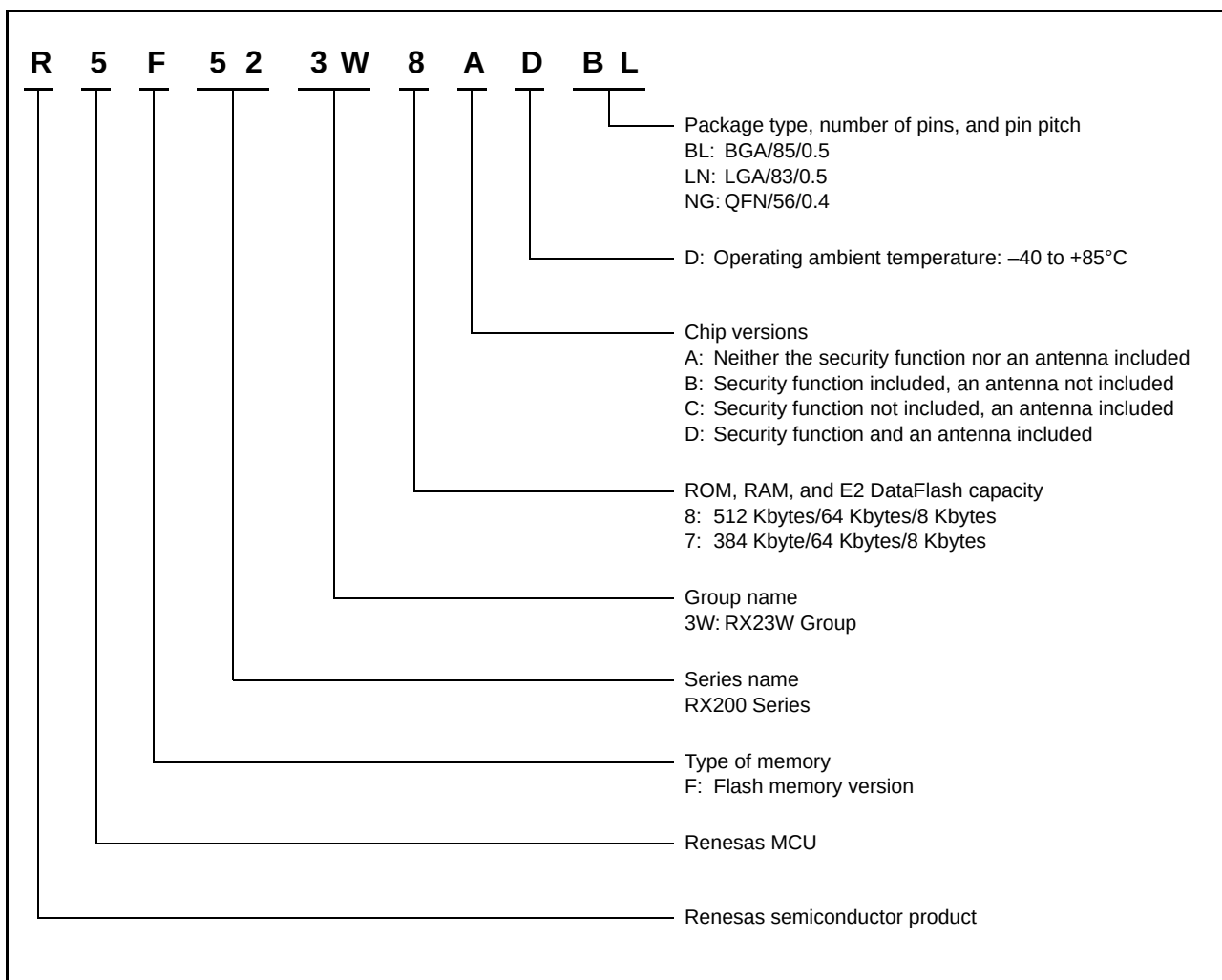


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram for the 85-pin BGA or 56-pin QFN product.

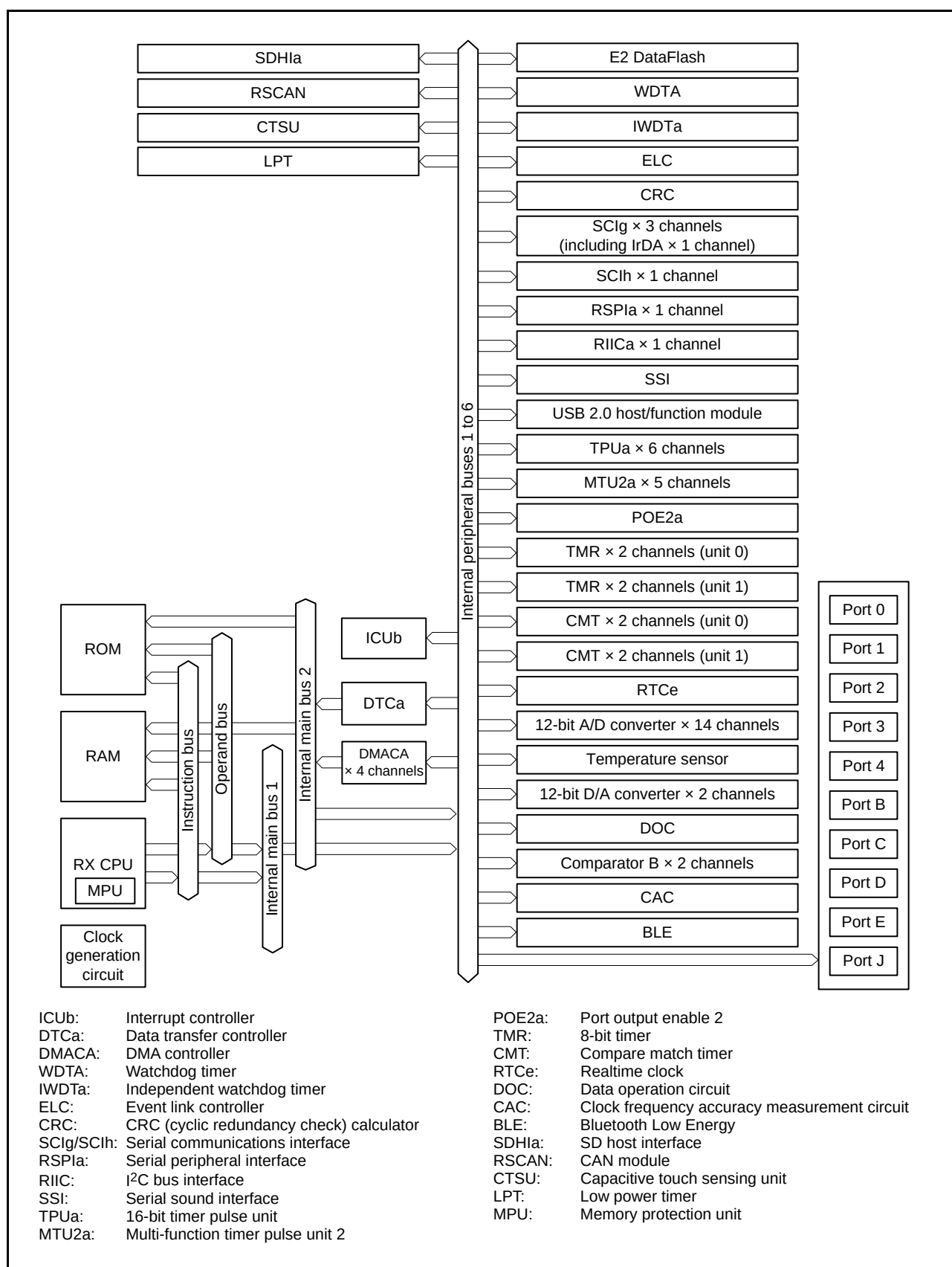


Figure 1.2 Block Diagram (85-Pin BGA, 56-Pin QFN)

Figure 1.3 shows a block diagram for the 83-pin LGA product.

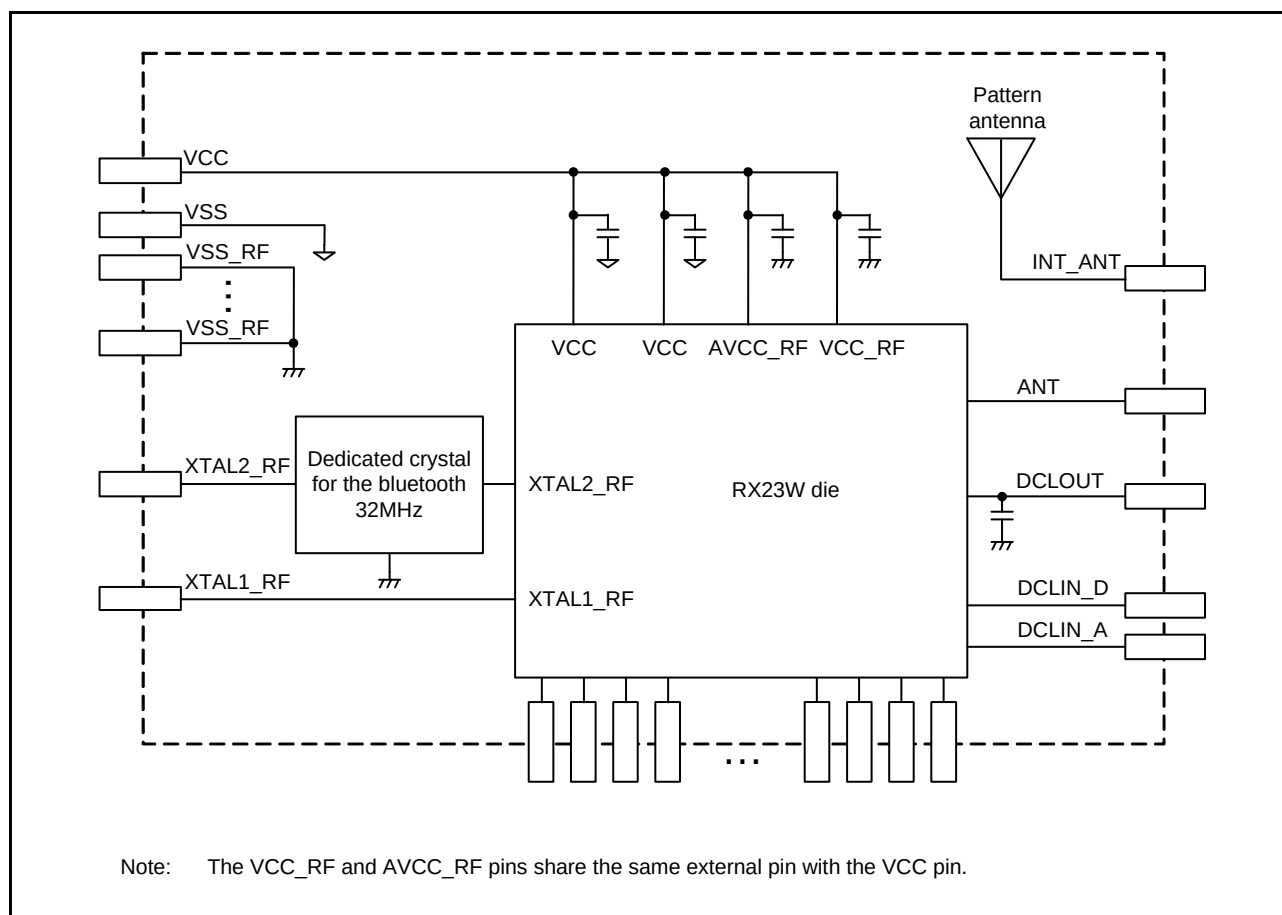


Figure 1.3 Block Diagram (83-Pin LGA)

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via a 4.7 μ F smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT_RF	Output	Bluetooth-dedicated clock output pin for output of a 1-, 2-, or 4-MHz signal
	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. Connect a 32-MHz oscillator to these pins. The 83-pin LGA product includes a 32-MHz crystal resonator. XTAL1_RF and XTAL2_R should thus be externally connected to each other.
	XTAL2_RF	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
	UB	Input	Pin used for boot mode (USB interface).
	UPSEL	Input	Pin used for boot mode (USB interface).
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0, IRQ1, IRQ4 to IRQ7	Input	Interrupt request pins.
16-bit timer pulse unit	TIOCB0	I/O	The TGRB0 inputs capture input/output compare output/PWM output pins.
	TIOCB1	I/O	The TGRB1 inputs capture input/output compare output/PWM output pins.
	TIOCB2	I/O	The TGRB2 inputs capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCB5	I/O	The TGRB5 inputs capture input/output compare output/PWM output pins.
	TCLKA, TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.

Table 1.4 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
Port output enable 2	POE0#, POE1#, POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
	RTCIC0, RTCIC1	Input	Time capture event input pins.
8-bit timer	TMO0 to TMO2	Output	Compare match output pins.
	TMCIO to TMCi3	Input	Input pins for the external clock to be input to the counter.
	TMRI1 to TMRI3	Input	Counter reset input pins.
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK8	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD8	Input	Input pins for received data.
	TXD1, TXD5, TXD8	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS8#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS8#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL1, SSCL5, SSCL8	I/O	Input/output pins for the I ² C clock.
	SSDA1, SSDA5, SSDA8	I/O	Input/output pins for the I ² C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK8	I/O	Input/output pins for the clock.
	SMISO1, SMISO5, SMISO8	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI8	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS8#	Input	Slave-select input pins.
IrDA interface	IRTXD5	Output	Data output pin in the IrDA format.
	IRRXD5	Input	Data input pin in the IrDA format.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pin for the I ² C clock.
	SSDA12	I/O	Input/output pin for the I ² C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I ² C bus interface	SCL	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output.

Table 1.4 Pin Functions (3/4)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1, SSLA3	Output	Output pins to select the slave for the RSPI.
Serial sound interface	SSISCK0	I/O	SSI serial bit clock pin.
	SSIWS0	I/O	Word selection pin.
	SSITXD0	Output	Serial data output pin.
	SSIRXD0	Input	Serial data input pin.
	AUDIO_MCLK	Input	Master clock pin for audio.
CAN module	CRXD0	Input	Input pin
	CTXD0	Output	Output pin
SD host interface	SDHI_CLK	Output	SD clock output pin
	SDHI_CMD	I/O	SD command output, response input signal pin
	SDHI_D3 to SDHI_D0	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
USB 2.0 host/function module	VCC_USB	Input	Power supply pin for USB. Connect this pin to VCC or connect this pin to VSS via a 0.33 μ F smoothing capacitor for stabilizing the internal power supply.
	VSS_USB	Input	Ground pin for USB. Connect this pin to VSS.
	USB0_DP	I/O	D+ I/O pin of the USB on-chip transceiver.
	USB0_DM	I/O	D- I/O pin of the USB on-chip transceiver.
	USB0_VBUS	Input	USB cable connection monitor pin.
	USB0_EXICEN	Output	Low-power control signal for the OTG chip.
	USB0_VBUSEN	Output	VBUS (5 V) supply enable signal for the OTG chip.
	USB0_OVRCURA, USB0_OVRCURB	Input	External overcurrent detection pins.
	USB0_ID	Input	Mini-AB connector ID input pin during operation in OTG mode.
12-bit A/D converter	AN000 to AN007, AN016 to AN020, AN027	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
12-bit D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB2, CMPB3	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB2, CVREFB3	Input	Analog reference voltage supply pin for comparator B.
	CMPOB2, CMPOB3	Output	Output pin for comparator B.
CTSU	TS2 to TS4, TS7, TS8, TS12, TS13, TS22, TS23, TS27, TS30, TS35	Output	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	Output	LPF connection pin.
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.

Table 1.4 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
I/O ports	P03, P05, P07	I/O	3-bit input/output pins.
	P14 to P17	I/O	4-bit input/output pins.
	P21, P22, P25 to P27	I/O	5-bit input/output pins.
	P30, P31, P35 to P37	I/O	5-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	PB0, PB1, PB3, PB5, PB7	I/O	5-bit input/output pins.
	PC0, PC2 to PC7	I/O	7-bit input/output pins.
	PD3	I/O	1-bit input/output pins.
	PE0 to PE4	I/O	5-bit input/output pins.
	PJ3	I/O	1-bit input/output pin.
Bluetooth low energy	ANT	I/O	RF single I/O pin for RF transceiver Set the impedance of the signal line to 50 Ω.
	INT_ANT	I/O	Internal antenna connection pin Externally connect this pin to the ANT pin.
	DCLOUT	Output	RF transceiver power-supply output pin
	DCLIN_A, DCLIN_D	Input	RF transceiver power-supply output connection pin In the case of an 83-pin LGA product, these pins should be externally connected to the DCLOUT pin.
	VCC_RF	Input	RF transceiver power supply pin
	AVCC_RF	Input	RF transceiver power supply pin
	VSS_RF	Input	RF transceiver ground pin

1.5 Pin Assignments

1.5.1 85-Pin BGA

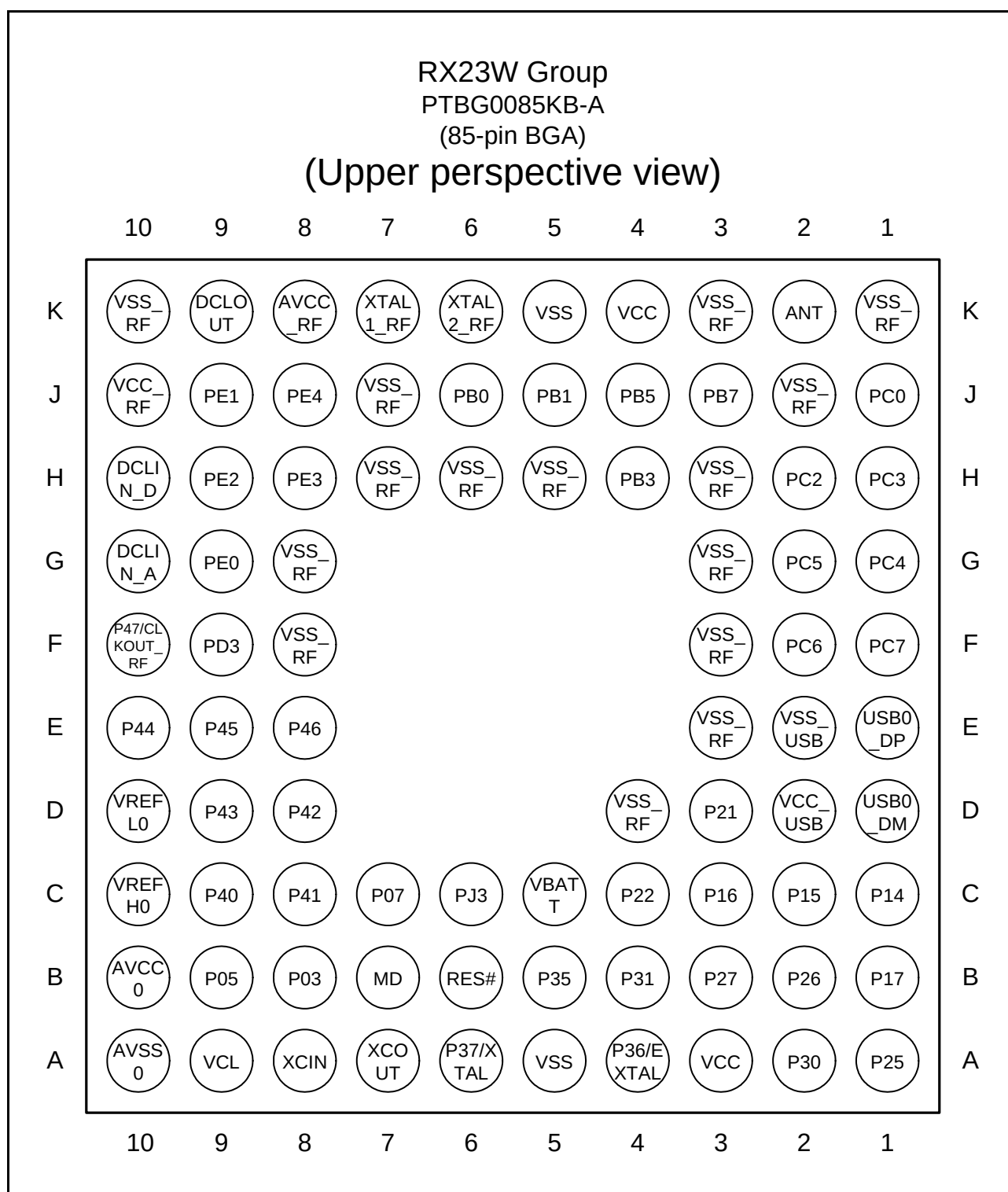


Figure 1.4 Pin Assignments of the 85-Pin BGA

RX23W Group
PTLG0083KA-A
(83-pin LGA)
(Upper perspective view)

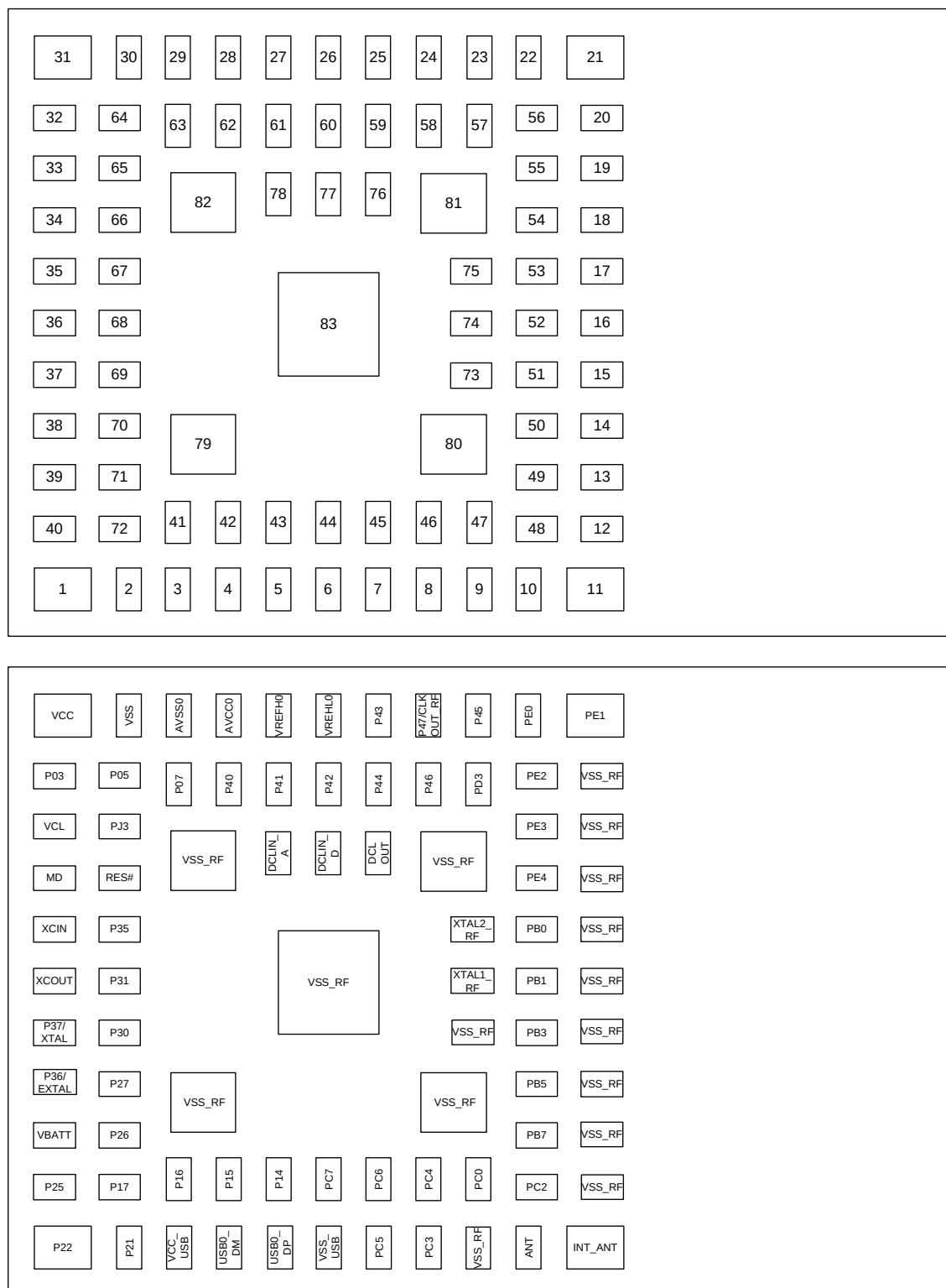


Figure 1.5 Pin Assignments of the 83-Pin LGA

1.5.3 56-Pin QFN

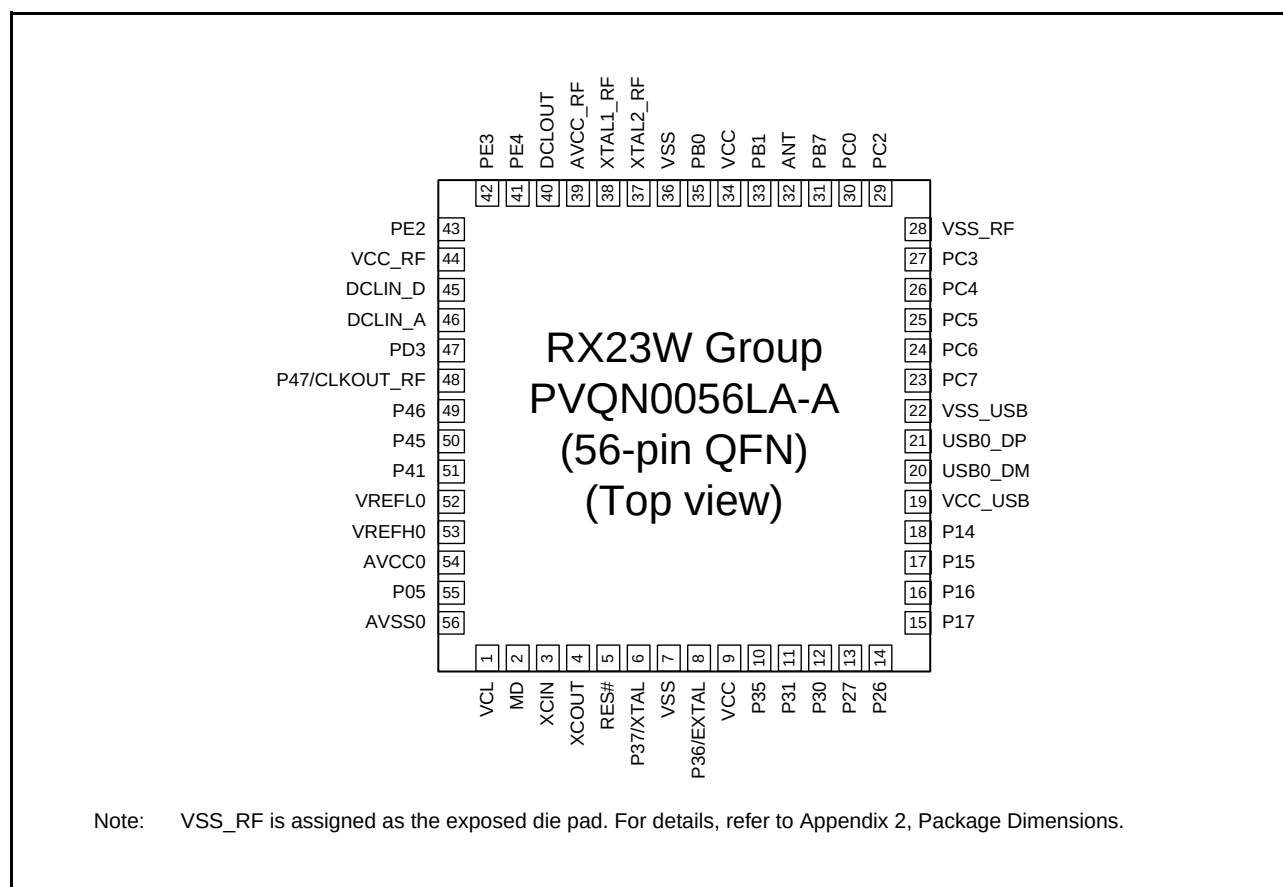


Figure 1.6 Pin Assignments of the 56-Pin QFN

1.6 List of Pins and Pin Functions

1.6.1 85-Pin BGA

Table 1.5 List of Pins and Pin Functions (85-Pin BGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
A1		P25	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
A2		P30	MTIOC4B/TMRI3/POE8#/ RTCIC0	RXD1/SMISO1/SSCL1/ AUDIO_MCLK			IRQ0/CMPOB3
A3	VCC						
A4	EXTAL	P36					
A5	VSS						
A6	XTAL	P37					
A7	XCOU						
A8	XCIN						
A9	VCL						
A10	AVSS0						
B1		P17	MTIOC3A/MTIOC3B/TMO1/ POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
B2		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0/ USB0_VBUSEN		TS3	CMPB3
B3		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
B4		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
B5	UPSEL	P35					NMI
B6	RES#						
B7	MD						FINED
B8		P03					DA0
B9		P05					DA1
B10	AVCC0						
C1		P14	MTIOC3A/MTCLKA/TMRI2/ TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/ USB0_OVRCURA		TS13	IRQ4/ CVREFB2
C2		P15	MTIOC0B/MTCLKB/TMCI2/ TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
C3		P16	MTIOC3C/MTIOC3D/TMO2/ TIOCB1/TCLKC/RTCOU	TXD1/SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB			IRQ6/ ADTRG0#
C4		P22	MTIOC3B/MTCLKC/TMO0/ TIOCC3	USB0_OVRCURB/AUDIO_MCLK		TS7	
C5	VBATT						
C6		PJ3	MTIOC3C				
C7		P07					ADTRG0#
C8		P41					AN001
C9		P40					AN000
C10	VREFH0						
D1				USB0_DM			
D2	VCC_USB						
D3		P21	MTIOC1B/TMCI0/TIOCA3	USB0_EXICEN/SSIWS0		TS8	
D4	VSS_RF						
D8		P42					AN002
D9		P43					AN003
D10	VREFL0						
E1				USB0_DP			
E2	VSS_USB						
E3	VSS_RF						
E8		P46					AN006
E9		P45					AN005
E10		P44					AN004
F1	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF

Table 1.5 List of Pins and Pin Functions (85-Pin BGA) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
F2		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
F3	VSS_RF						
F8	VSS_RF						
F9		PD3	POE8#				AN027
F10		P47					AN007/ CLKOUT_RF
G1		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	CTS8#/RTS8#/SS8#/SSLA0/SCK5	SDHI_D1	TSCAP	
G2		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
G3	VSS_RF						
G8	VSS_RF						
G9		PE0		SCK12			AN016
G10	DCLIN_A						
H1		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
H2		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	SDHI_D3	TS30	
H3	VSS_RF						
H4		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#/TIOC3/TCLKD		SDHI_WP		
H5	VSS_RF						
H6	VSS_RF						
H7	VSS_RF						
H8		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/ AUDIO_MCLK			AN019/ CLKOUT
H9		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018
H10	DCLIN_D						
J1		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
J2	VSS_RF						
J3		PB7	MTIOC3B/TIOCB5		SDHI_D2		
J4		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#/TIOCB4	USB0_VBUS	SDHI_CD		
J5		PB1	MTIOC0C/MTIOC4C/TMCI0/ TIOCB3		SDHI_CLK		IRQ4
J6		PB0	TIOCA3	RSPCKA	SDHI_CMD		
J7	VSS_RF						
J8		PE4	MTIOC4D/MTIOC1A				AN020/ CLKOUT
J9		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/ SSDA12			AN017
J10	VCC_RF						
K1	VSS_RF						
K2							ANT
K3	VSS_RF						
K4	VCC						
K5	VSS						
K6	XTAL2_RF						
K7	XTAL1_RF						
K8	AVCC_RF						
K9	DCLOUT						
K10	VSS_RF						

1.6.2 83-Pin LGA

Table 1.6 List of Pins and Pin Functions (83-Pin LGA) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
1		P22	MTIOC3B/MTCLKC/TMO0/TIOCC3	USB0_OVRCURB/AUDIO_MCLK		TS7	
2		P21	MTIOC1B/TMCI0/TIOCA3	USB0_EXICEN/SSIWS0		TS8	
3	VCC_USB						
4				USB0_DM			
5				USB0_DP			
6	VSS_USB						
7		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID		TS23	
8		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	SDHI_D0	TS27	
9	VSS_RF						
10							ANT
11							INT_ANT
12	VSS_RF						
13	VSS_RF						
14	VSS_RF						
15	VSS_RF						
16	VSS_RF						
17	VSS_RF						
18	VSS_RF						
19	VSS_RF						
20	VSS_RF						
21		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12			AN017
22		PE0		SCK12			AN016
23		P45					AN005
24		P47					AN007/ CLKOUT_RF
25		P43					AN003
26	VREFL0						
27	VREFH0						
28	AVCC0						
29	AVSS0						
30	VSS						
31	VCC						
32		P03					DA0
33	VCL						
34	MD						FINED
35	XCIN						
36	XCOUT						
37	XTAL	P37					
38	EXTAL	P36					
39	VBATT						
40		P25	MTIOC4C/MTCLKB/TIOCA4			TS4	ADTRG0#
41		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTCOU	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB			IRQ6/ ADTRG0#
42		P15	MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0		TS12	IRQ5/CMPB2
43		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA		TS13	IRQ4/ CVREFB2
44	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA			CACREF
45		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN		TS22	
46		PC4	MTIOC3D/MTCLKC/TMCI1/POE0#	CTS8#/RTS8#/SS8#/SSLA0/SCK5	SDHI_D1	TSCAP	

Table 1.6 List of Pins and Pin Functions (83-Pin LGA) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, IIC, RSCAN, USB, SSI)	Memory Interface (SDHI)	Touch sensing	Others
47		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1		TS35	
48		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	SDHI_D3	TS30	
49		PB7	MTIOC3B/TIOCB5		SDHI_D2		
50		PB5	MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4	USB0_VBUS	SDHI_CD		
51		PB3	MTIOC0A/MTIOC4A/TMO0/POE3#/TIOC03/TCLKD		SDHI_WP		
52		PB1	MTIOC0C/MTIOC4C/TMCI0/TIOCB3		SDHI_CLK		IRQ4
53		PB0	TIOCA3	RSPCKA	SDHI_CMD		
54		PE4	MTIOC4D/MTIOC1A				AN020/CLKOUT
55		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/AUDIO_MCLK			AN019/CLKOUT
56		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12			IRQ7/AN018
57		PD3	POE8#				AN027
58		P46					AN006
59		P44					AN004
60		P42					AN002
61		P41					AN001
62		P40					AN000
63		P07					ADTRG0#
64		P05					DA1
65		PJ3	MTIOC3C				
66	RES#						
67	UPSEL	P35					NMI
68		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0			IRQ1
69		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK			IRQ0/CMPOB3
70		P27	MTIOC2B/TMCI3	SCK1/SSIWS0		TS2	CVREFB3
71		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0/USB0_VBUSEN		TS3	CMPB3
72		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOC03/TCLKD	SCK1/MISOA/SDA/SSITXD0			IRQ7/CMPOB2
73	VSS_RF						
74	XTAL1_RF						
75	XTAL2_RF						
76	DCLOUT						
77	DCLIN_D						
78	DCLIN_A						
79	VSS_RF						
80	VSS_RF						
81	VSS_RF						
82	VSS_RF						
83	VSS_RF						

1.6.3 56-Pin QFN

Table 1.7 List of Pins and Pin Functions (56-Pin QFN) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Touch sensing	Others
1	VCL					
2	MD					FINED
3	XCIN					
4	XCOUT					
5	RES#					
6	XTAL	P37				
7	VSS					
8	EXTAL	P36				
9	VCC					
10	UPSEL	P35				NMI
11		P31	MTIOC4D/TMCI2/RTCIC1	CTS1#/RTS1#/SS1#/SSISCK0		IRQ1
12		P30	MTIOC4B/TMRI3/POE8#/RTCIC0	RXD1/SMISO1/SSCL1/AUDIO_MCLK		IRQ0/CMPOB3
13		P27	MTIOC2B/TMCI3	SCK1/SSIWS0	TS2	CVREFB3
14		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/SSIRXD0/USB0_VBUSEN	TS3	CMPB3
15		P17	MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/TCLKD	SCK1/MISOA/SDA/SSITXD0		IRQ7/CMPOB2
16		P16	MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/RTXCOUT	TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
17		P15	MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB	RXD1/SMISO1/SSCL1/CRXD0	TS12	IRQ5/CMPB2
18		P14	MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA	CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA	TS13	IRQ4/CVREFB2
19	VCC_USB					
20				USB0_DM		
21				USB0_DP		
22	VSS_USB					
23	UB	PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA		CACREF
24		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA/USB0_EXICEN	TS22	
25		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA/USB0_ID	TS23	
26		PC4	MTIOC3D/MTCLKC/TMCI1/POE0#	CTS8#/RTS8#/SS8#/SSLA0/SCK5	TSCAP	
27		PC3	MTIOC4D/TCLKB	TXD5/SMOSI5/SSDA5/IRTXD5	TS27	
28	VSS_RF					
29		PC2	MTIOC4B/TCLKA	RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	TS30	
30		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/SS5#/SSLA1	TS35	
31		PB7	MTIOC3B/TIOCB5			
32						ANT
33		PB1	MTIOC0C/MTIOC4C/TMCI0/TIOCB3			IRQ4
34	VCC					
35		PB0	TIOCA3	RSPCKA		
36	VSS					
37	XTAL2_RF					
38	XTAL1_RF					
39	AVCC_RF					
40	DCLOUT					
41		PE4	MTIOC4D/MTIOC1A			AN020/CLKOUT
42		PE3	MTIOC4B/POE8#	AUDIO_MCLK		AN019/CLKOUT
43		PE2	MTIOC4A			IRQ7/AN018
44	VCC_RF					
45	DCLIN_D					
46	DCLIN_A					
47		PD3	POE8#			AN027

Table 1.7 List of Pins and Pin Functions (56-Pin QFN) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TPU, TMR, RTC, CMT, POE, CAC)	Communications (SCI, RSPI, RIIC, RSCAN, USB, SSI)	Touch sensing	Others
48		P47				AN007/ CLKOUT_RF
49		P46				AN006
50		P45				AN005
51		P41				AN001
52	VREFL0					
53	VREFH0					
54	AVCC0					
55		P05				DA1
56	AVSS0					

Note: VSS_RF is assigned as the exposed die pad. For details, refer to Appendix 2, Package Dimensions.

2. CPU

The RXv2 instruction set architecture (RXv2) has upward compatibility with the RXv1 instruction set architecture (RXv1).

- Adoption of variable-length instruction format
As with RXv1, the RXv2 CPU has short formats for frequently used instructions, facilitating the development of efficient programs that take up less memory.
- Powerful instruction set
The RXv2 supports 109 selected instructions. Moreover, DSP instructions and floating-point operation instructions are added, thus realizing high-speed arithmetic processing.
- Versatile addressing modes
The RXv2 CPU has 11 versatile addressing modes, with register-register operations, register-memory operations, and bitwise operations included. Data transfer between memory locations is also possible.

2.1 Features

- Minimum instruction execution rate: One clock cycle
- Address space: 4-Gbyte linear addresses
- Register set of the CPU
General purpose: Sixteen 32-bit registers
Control: Ten 32-bit registers
Accumulator: Two 72-bit registers
- Variable-length instruction format (lengths from one to eight bytes)
- 109 instructions/11 addressing modes
Basic instructions: 75
Floating-point operation instructions: 11
DSP instructions: 23
- Processor modes
Supervisor mode and user mode
- Vector tables
Exception vector table and interrupt vector table
- Memory protection unit
- Data arrangement
Selectable as little endian or big endian

2.2 Register Set of the CPU

The RXv2 CPU has sixteen general-purpose registers, ten control registers, and two accumulator used for DSP instructions.

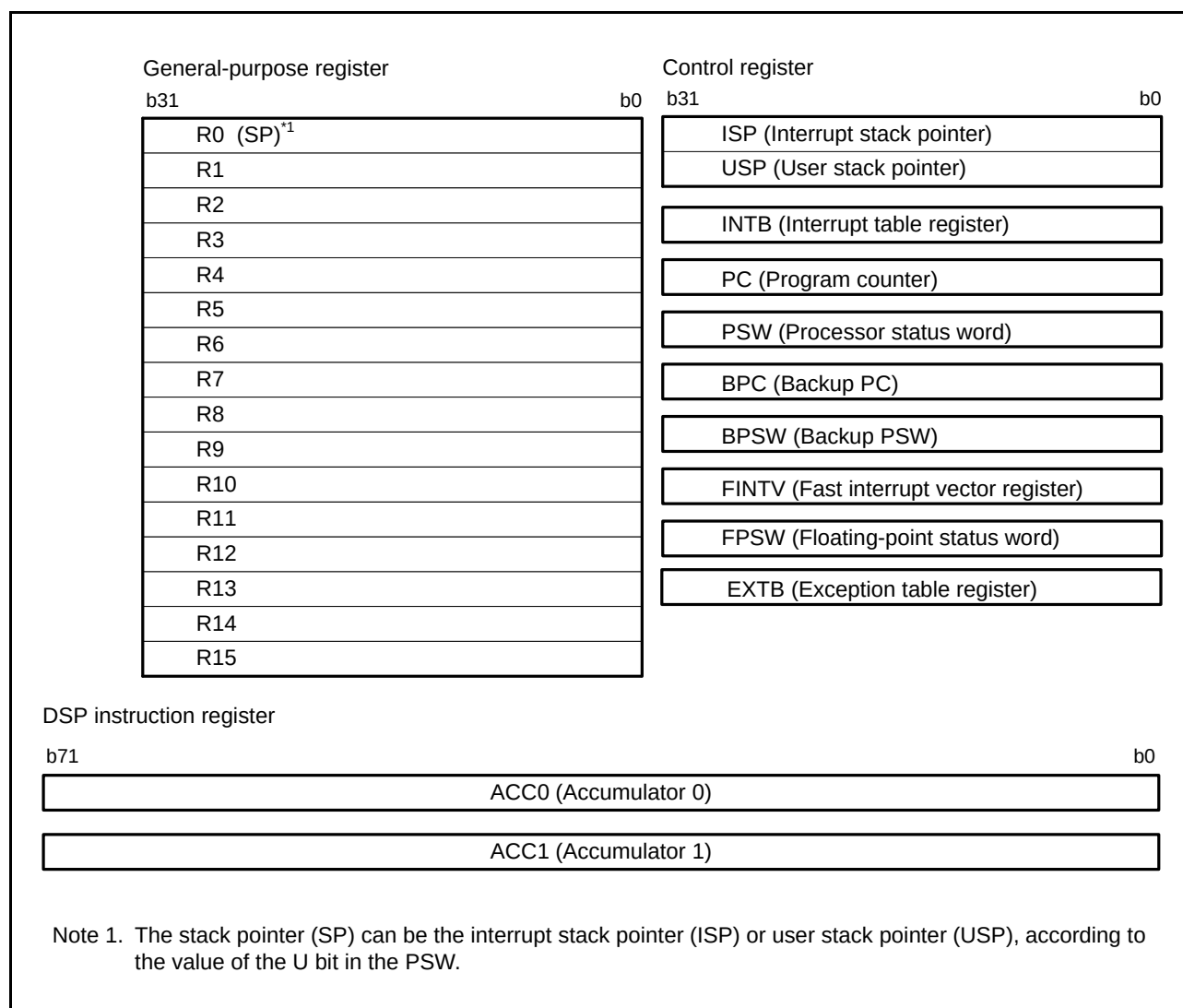


Figure 2.1 Register Set of the CPU

2.2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP).

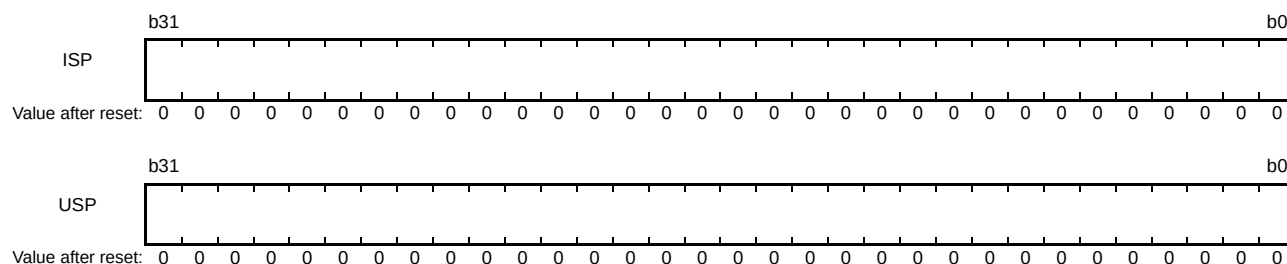
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2.2 Control Registers

This CPU has the following ten control registers.

- Interrupt stack pointer (ISP)
- User stack pointer (USP)
- Exception table register (EXTB)
- Interrupt table register (INTB)
- Program counter (PC)
- Processor status word (PSW)
- Backup PC (BPC)
- Backup PSW (BPSW)
- Fast interrupt vector register (FINTV)
- Floating-point status word (FPSW)

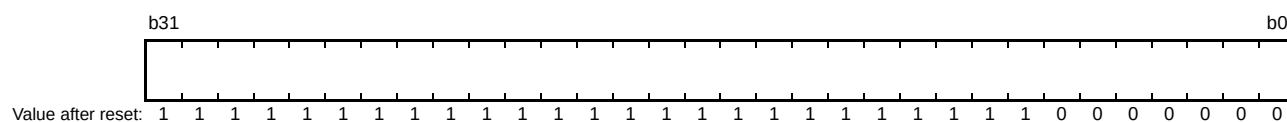
2.2.2.1 Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)



The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

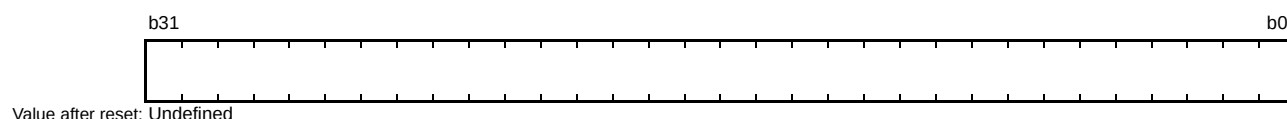
2.2.2.2 Exception Table Register (EXTB)



The exception table register (EXTB) specifies the address where the exception vector table starts.

Set the EXTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

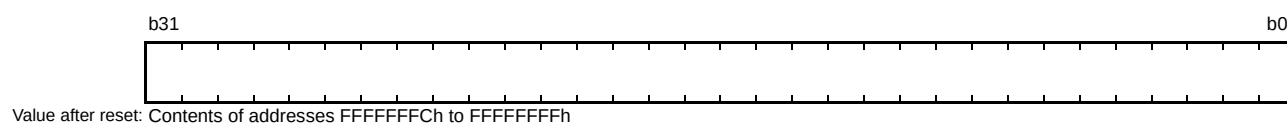
2.2.2.3 Interrupt Table Register (INTB)



The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

Set the INTB to a multiple of 4 to reduce the number of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

2.2.2.4 Program Counter (PC)



The program counter (PC) indicates the address of the instruction being executed.

2.2.2.5 Processor Status Word (PSW)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	IPL[3:0]				—	—	—	PM	—	—	U	I
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	—	—	—	—	O	S	Z	C
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C	Carry Flag	0: No carry has occurred. 1: A carry has occurred.	R/W
b1	Z	Zero Flag	0: Result is non-zero. 1: Result is 0.	R/W
b2	S	Sign Flag	0: Result is a positive value or 0. 1: Result is a negative value.	R/W
b3	O	Overflow Flag	0: No overflow has occurred. 1: An overflow has occurred.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	I*1	Interrupt Enable	0: Interrupt disabled. 1: Interrupt enabled.	R/W
b17	U*1	Stack Pointer Select	0: Interrupt stack pointer (ISP) is selected. 1: User stack pointer (USP) is selected.	R/W
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	PM*1, *2, *3	Processor Mode Select	0: Supervisor mode is selected. 1: User mode is selected.	R/W
b23 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b24	IPL[3:0]*1	Processor Interrupt Priority Level	b27 b24 0 0 0 0: Priority level 0 (lowest) 0 0 0 1: Priority level 1 0 0 1 0: Priority level 2 0 0 1 1: Priority level 3 0 1 0 0: Priority level 4 0 1 0 1: Priority level 5 0 1 1 0: Priority level 6 0 1 1 1: Priority level 7 1 0 0 0: Priority level 8 1 0 0 1: Priority level 9 1 0 1 0: Priority level 10 1 0 1 1: Priority level 11 1 1 0 0: Priority level 12 1 1 0 1: Priority level 13 1 1 1 0: Priority level 14 1 1 1 1: Priority level 15 (highest)	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In user mode, writing to the IPL[3:0], PM, U, and I bits by an MVTC or a POPC instruction is ignored. Writing to the IPL[3:0] bits by an MVTIPL instruction generates a privileged instruction exception.

Note 2. In supervisor mode, writing to the PM bit by an MVTC or a POPC instruction is ignored, but writing to the other bits is possible.

Note 3. Switching from supervisor mode to user mode requires execution of an RTE instruction after having set the PSW.PM bit saved on the stack to 1 or executing an RTFI instruction after having set the BPSW.PM bit to 1.

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

C Flag (Carry Flag)

This flag retains the state of the bit after a carry, borrow, or shift-out has occurred.

Z Flag (Zero Flag)

This flag is set to 1 if the result of an operation is 0; otherwise its value is cleared to 0.

S Flag (Sign Flag)

This flag is set to 1 if the result of an operation is negative; otherwise its value is cleared to 0.

O Flag (Overflow Flag)

This flag is set to 1 if the result of an operation overflows; otherwise its value is cleared to 0.

I Bit (Interrupt Enable)

This bit enables interrupt requests. When a WAIT instruction is executed, the value of this bit becomes 1. It becomes 0 when an exception is accepted.

U Bit (Stack Pointer Select)

This bit specifies the stack pointer as either the ISP or USP. When an exception request is accepted, this bit is set to 0. When the processor mode is switched from supervisor mode to user mode, this bit is set to 1.

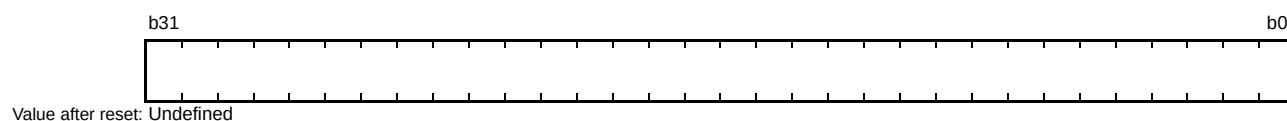
PM Bit (Processor Mode Select)

This bit specifies the processor mode. When an exception is accepted, the value of this bit becomes 0.

IPL[3:0] Bits (Processor Interrupt Priority Level)

The IPL[3:0] bits specify the processor interrupt priority level as one of sixteen levels from zero to fifteen, wherein priority level zero is the lowest and priority level fifteen the highest. When the priority level of a requested interrupt is higher than the processor interrupt priority level, the interrupt is enabled. Setting the IPL[3:0] bits to level fifteen (Fh) disables all interrupt requests. The IPL[3:0] bits are set to level fifteen (Fh) when a non-maskable interrupt is generated. When interrupts in general are generated, the bits are set to the priority levels of accepted interrupts.

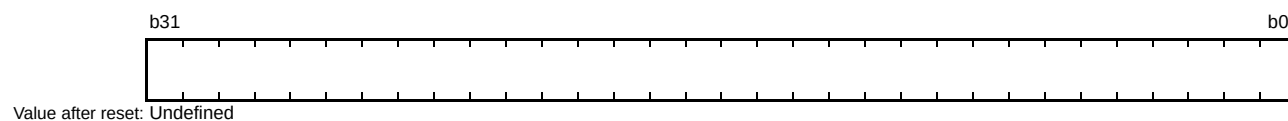
2.2.2.6 Backup PC (BPC)



The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

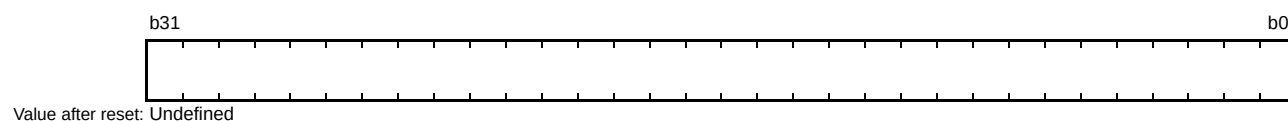
2.2.2.7 Backup PSW (BPSW)



The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

2.2.2.8 Fast Interrupt Vector Register (FINTV)



The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.2.2.9 Floating-Point Status Word (FPSW)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FS	FX	FU	FZ	FO	FV	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	EX	EU	EZ	EO	EV	—	DN	CE	CX	CU	CZ	CO	CV	RM[1:0]	—
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	RM[1:0]	Floating-Point Rounding-Mode Setting	b1 b0 0 0: Rounding towards the nearest value 0 1: Rounding towards 0 1 0: Rounding towards $+\infty$ 1 1: Rounding towards $-\infty$	R/W
b2	CV	Invalid Operation Cause Flag	0: No invalid operation has been encountered. 1: Invalid operation has been encountered.	R/(W) *1
b3	CO	Overflow Cause Flag	0: No overflow has occurred. 1: Overflow has occurred.	R/(W) *1
b4	CZ	Division-by-Zero Cause Flag	0: No division-by-zero has occurred. 1: Division-by-zero has occurred.	R/(W) *1
b5	CU	Underflow Cause Flag	0: No underflow has occurred. 1: Underflow has occurred.	R/(W) *1
b6	CX	Inexact Cause Flag	0: No inexact exception has been generated. 1: Inexact exception has been generated.	R/(W) *1
b7	CE	Unimplemented Processing Cause Flag	0: No unimplemented processing has been encountered. 1: Unimplemented process has been encountered.	R/(W) *1
b8	DN	0 Flush Bit of Denormalized Number	0: A denormalized number is handled as a denormalized number. 1: A denormalized number is handled as 0.*2	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	EV	Invalid Operation Exception Enable	0: Invalid operation exception is masked. 1: Invalid operation exception is enabled.	R/W
b11	EO	Overflow Exception Enable	0: Overflow exception is masked. 1: Overflow exception is enabled.	R/W
b12	EZ	Division-by-Zero Exception Enable	0: Division-by-zero exception is masked. 1: Division-by-zero exception is enabled.	R/W
b13	EU	Underflow Exception Enable	0: Underflow exception is masked. 1: Underflow exception is enabled.	R/W
b14	EX	Inexact Exception Enable	0: Inexact exception is masked. 1: Inexact exception is enabled.	R/W
b25 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26	FV*3	Invalid Operation Flag	0: No invalid operation has been encountered. 1: Invalid operation has been encountered.*8	R/W
b27	FO*4	Overflow Flag	0: No overflow has occurred. 1: Overflow has occurred.*8	R/W
b28	FZ*5	Division-by-Zero Flag	0: No division-by-zero has occurred. 1: Division-by-zero has occurred.*8	R/W
b29	FU*6	Underflow Flag	0: No underflow has occurred. 1: Underflow has occurred.*8	R/W
b30	FX*7	Inexact Flag	0: No inexact exception has been generated. 1: Inexact exception has been generated.*8	R/W

Bit	Symbol	Bit Name	Description	R/W
b31	FS	Floating-Point Error Summary Flag	This bit reflects the logical OR of the FU, FZ, FO, and FV flags.	R

Note 1. Writing 0 to the bit clears it. Writing 1 to the bit does not affect its value.

Note 2. Positive denormalized numbers are treated as +0, negative denormalized numbers as -0.

Note 3. When the EV bit is set to 0, the FV flag is enabled.

Note 4. When the EO bit is set to 0, the FO flag is enabled.

Note 5. When the EZ bit is set to 0, the FZ flag is enabled.

Note 6. When the EU bit is set to 0, the FU flag is enabled.

Note 7. When the EX bit is set to 0, the FX flag is enabled.

Note 8. Once the bit has been set to 1, this value is retained until it is cleared to 0 by software.

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

RM[1:0] Bits (Floating-Point Rounding-Mode Setting)

These bits specify the floating-point rounding-mode.

Explanation of Floating-Point Rounding Modes

- Rounding towards the nearest value (the default behavior) : An inexact result is rounded to the available value that is closest to the result which would be obtained with an infinite number of digits. If two available values are equally close, rounding is to the even alternative.
- Rounding towards 0 : An inexact result is rounded to the smallest available absolute value, i.e. in the direction of zero (simple truncation).
- Rounding towards $+\infty$: An inexact result is rounded to the nearest available value in the direction of positive infinity.
- Rounding towards $-\infty$: An inexact result is rounded to the nearest available value in the direction of negative infinity.

(1) Rounding to the nearest value is specified as the default mode and returns the most accurate value.

(2) Modes such as rounding towards 0, rounding towards $+\infty$, and rounding towards $-\infty$ are used to ensure precision when interval arithmetic is employed.

CV Flag (Invalid Operation Cause Flag), CO Flag (Overflow Cause Flag), CZ Flag (Division-by-Zero Cause Flag), CU Flag (Underflow Cause Flag), CX Flag (Inexact Cause Flag), and CE Flag (Unimplemented Processing Cause Flag)

Floating-point exceptions include the five specified in the IEEE754 standard, namely overflow, underflow, inexact, division-by-zero, and invalid operation. For a further floating-point exception that is generated upon detection of unimplemented processing, the corresponding flag (CE) is set to 1.

- The bit that has been set to 1 is cleared to 0 when the FPU instruction is executed.
- When 0 is written to the bit by the MVTC and POPC instructions, the bit is set to 0; the bit retains the previous value when 1 is written by the instruction.

DN Flag (0 Flush Bit of Denormalized Number)

When this bit is set to 0, a denormalized number is handled as a denormalized number. When this bit is set to 1, a denormalized number is handled as 0.

EV Bit (Invalid Operation Exception Enable), EO Bit (Overflow Exception Enable), EZ Bit (Division-by-Zero Exception Enable), EU Bit (Underflow Exception Enable), and EX Bit (Inexact Exception Enable)

When any of five floating-point exceptions specified in the IEEE754 standard is generated by the floating-point

operation instruction, the bit decides whether the CPU will start handling the exception. When the bit is set to 0, the exception handling is masked; when the bit is set to 1, the exception handling is enabled.

FV Flag (Invalid Operation Flag), FO Flag (Overflow Flag), FZ Flag (Division-by-Zero Flag), FU Flag (Underflow Flag), and FX Flag (Inexact Flag)

While the exception handling enable bit (Ej) is 0 (exception handling is masked), if any of five floating-point exceptions specified in the IEEE754 standard is generated, the corresponding bit is set to 1.

- When Ej is 1 (exception handling is enabled), the value of the flag remains.
- When the corresponding flag is set to 1, it remains 1 until it is cleared to 0 by software. (accumulation flag)

FS Flag (Floating-Point Error Summary Flag)

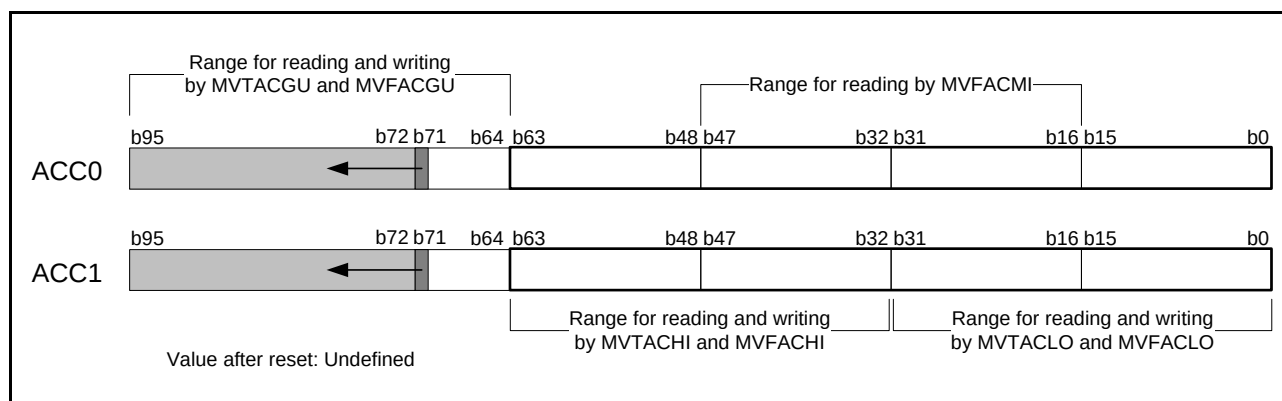
This bit reflects the logical OR of the FU, FZ, FO, and FV flags.

2.2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 31 to 0), and the lower-order 32 bits (bits 31 to 0), respectively.



Note: The value of bit 71 is sign extended for bits 95 to 72 and the extended value is always read. Writing to this area is ignored.

2.3 Processor Mode

The RXv2 CPU supports two processor modes, supervisor and user. These processor modes and the memory protection function enable the realization of a hierarchical CPU resource protection and memory protection mechanism. Each processor mode imposes a level on rights of access to memory and the instructions that can be executed. Supervisor mode carries greater rights than user mode. The initial state after a reset is supervisor mode.

2.3.1 Supervisor Mode

In supervisor mode, all CPU resources are accessible and all instructions are available. However, writing to the processor mode select bit (PM) in the processor status word (PSW) by executing an MVTC or a POPC instruction will be ignored. For details on how to write to the PM bit, refer to section 2.2.2.5, Processor Status Word (PSW).

2.3.2 User Mode

In user mode, write access to the CPU resources listed below is restricted. The restriction applies to any instruction capable of write access.

- Some bits (bits IPL[3:0], PM, U, and I) in the processor status word (PSW)
- Interrupt stack pointer (ISP)
- Exception table register (EXTB)
- Interrupt table register (INTB)
- Backup PSW (BPSW)
- Backup PC (BPC)
- Fast interrupt vector register (FINTV)

2.3.3 Privileged Instruction

Privileged instructions can only be executed in supervisor mode. Executing a privileged instruction in user mode produces a privileged instruction exception. Privileged instructions include the RTFI, MVTIPL, RTE, and WAIT instructions.

2.3.4 Switching Between Processor Modes

Manipulating the processor mode select bit (PM) in the processor status word (PSW) switches the processor mode. However, rewriting to the PM bit by executing an MVTC or a POPC instruction is prohibited. Switch the processor mode by following the procedures described below.

(1) Switching from user mode to supervisor mode

After an exception has been generated, the PSW.PM bit is set to 0 and the CPU switches to supervisor mode. The hardware pre-processing is executed in supervisor mode. The state of the processor mode before the exception was generated is retained in the copy of PSW.PM bit is saved on the stack.

(2) Switching from supervisor mode to user mode

Executing an RTE instruction when the value of the copy of the PSW.PM bit that has been preserved on the stack is 1 or an RTFI instruction when the value of the copy of the PSW.PM bit that has been preserved in the backup PSW (BPSW) is 1 causes a transition to user mode. In the transition to user mode, the value of the stack pointer designation bit (the U bit in the PSW) becomes 1.

2.4 Data Types

The RXv2 CPU can handle four types of data: integer, floating-point, bit, and string.

For details, refer to RX Family RXv2 Instruction Set Architecture User's Manual: Software.

2.4.1 Integer

An integer can be signed or unsigned. For signed integers, negative values are represented by two's complements.

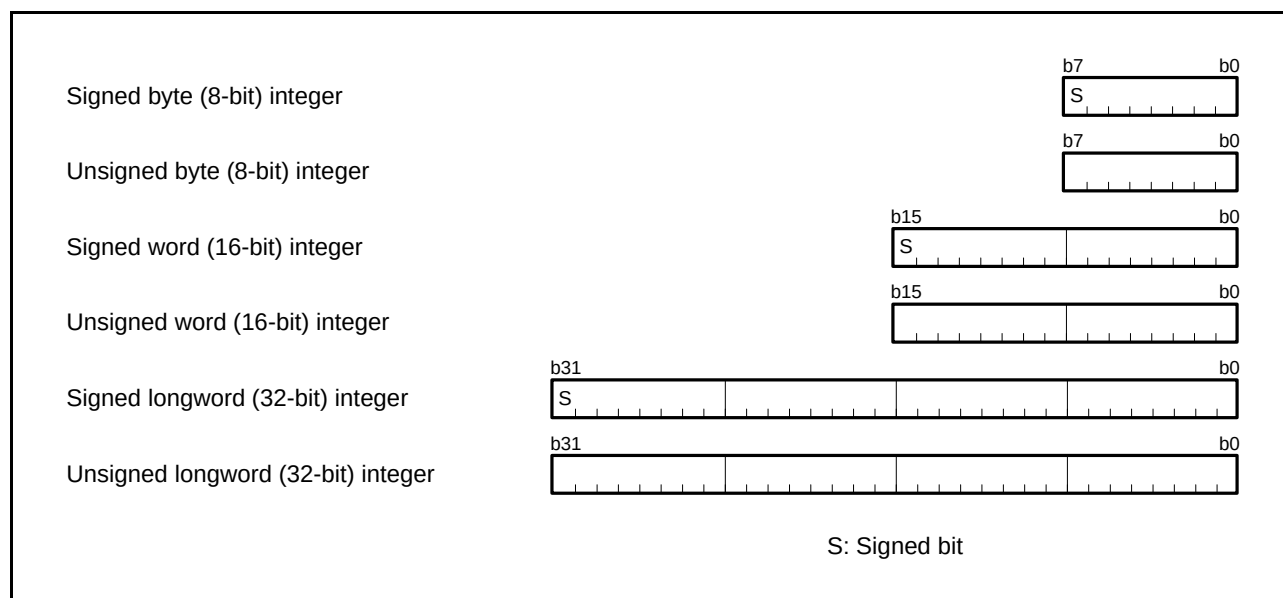


Figure 2.2 Integer

2.4.2 Floating-Points

Floating-point support is for the single-precision floating-point type specified in the IEEE754 standard; operands of this type can be used in eleven floating-point operation instructions: FADD, FCMP, FDIV, FMUL, FSQRT, FSUB, FTOI, FTOU, ITOF, ROUND, and UTOF.

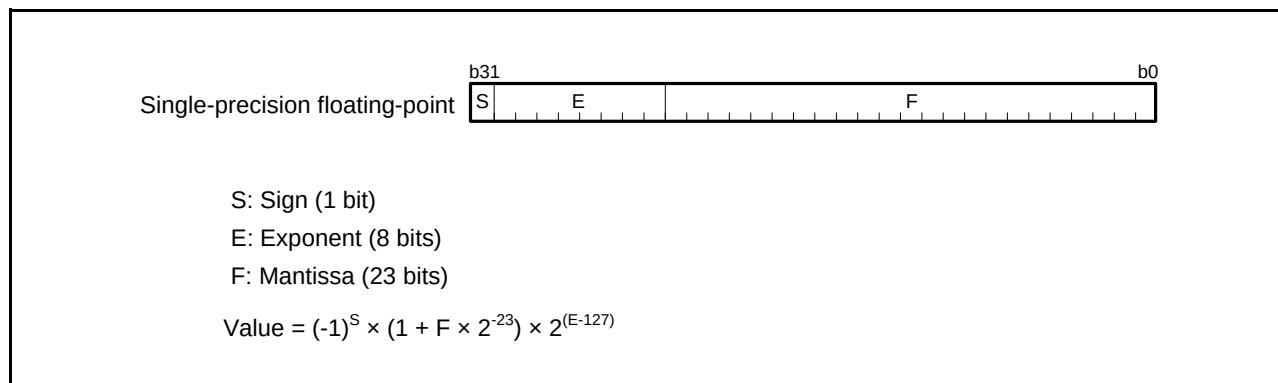


Figure 2.3 Floating-Point

The floating-point format supports the values listed below.

- 0 < E < 255 (normal numbers)
- E = 0 and F = 0 (signed zero)
- E = 0 and F > 0 (denormalized numbers)*1
- E = 255 and F = 0 (infinity)
- E = 255 and F > 0 (NaN: Not-a-Number)

Note 1. The number is treated as 0 when the FPSW.DN bit is 1. When the DN bit is 0, an unimplemented processing exception is generated.

2.4.3 Bitwise Operations

Five bit-manipulation instructions are provided for bitwise operations: BCLR, BMCnd, BNOT, BSET, and BTST.

A bit in a register is specified as the destination register and a bit number in the range from 31 to 0.

A bit in memory is specified as the destination address and a bit number from 7 to 0. The addressing modes available to specify addresses are register indirect and register relative.

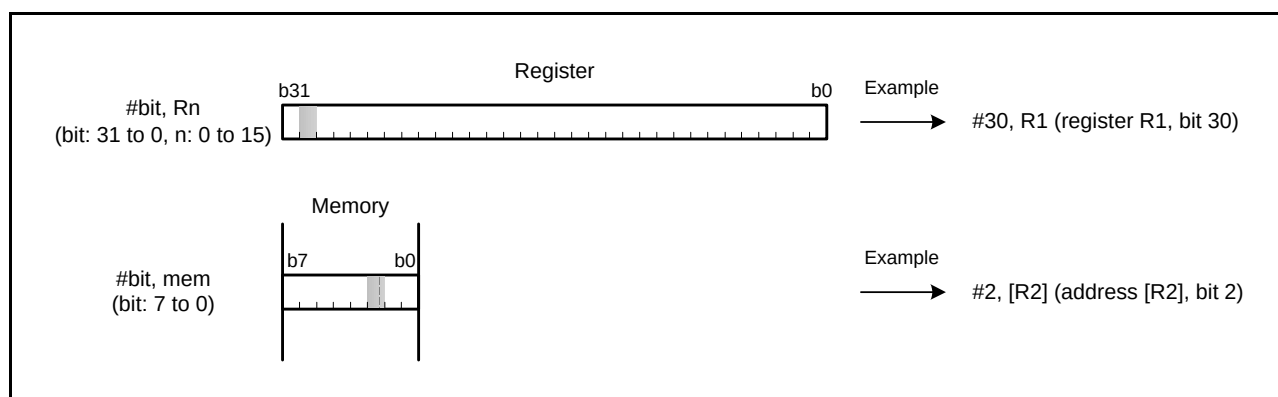


Figure 2.4 Bit

2.4.4 Strings

The string data type consists of an arbitrary number of consecutive byte (8-bit), word (16-bit), or longword (32-bit) units. Seven string manipulation instructions are provided for use with strings: SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE.

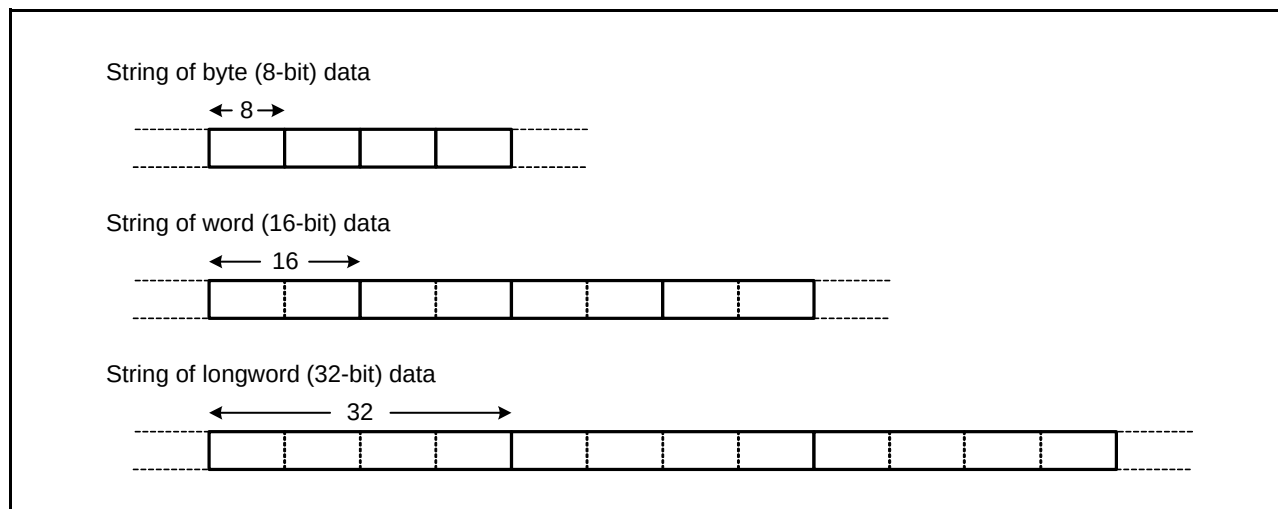


Figure 2.5 String

2.5 Endian

For the RXv2 CPU, instructions are little endian, but the treatment of data is selectable as little or big endian.

2.5.1 Switching the Endian

As arrangements of bytes, this MCU supports both big endian, where the higher-order byte (MSB) is at location 0, and little endian, where the lower-order byte (LSB) is at location 0.

For details on the endian setting, see section 3, Operating Modes.

Operations for access differ according to the endian setting and, depending on the instruction, whether 8-, 16- or 32-bit access has been selected. Operations for access in the various possible cases are described in Table 2.1 to Table 2.12.

In the tables,

LL indicates bits D7 to D0 of the general-purpose register,

LH indicates bits D15 to D8 of the general-purpose register,

HL indicates bits D23 to D16 of the general-purpose register, and

HH indicates bits D31 to D24 of the general-purpose register.

	D31 to D24	D23 to D16	D15 to D8	D7 to D0
General purpose register: Rm	HH	HL	LH	LL

Table 2.1 32-Bit Read Operations when Little Endian has been Selected

Operation Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to LL	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—
Address 2	Transfer to HL	Transfer to LH	Transfer to LL	—	—
Address 3	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL	—
Address 4	—	Transfer to HH	Transfer to HL	Transfer to LH	Transfer to LL
Address 5	—	—	Transfer to HH	Transfer to HL	Transfer to LH
Address 6	—	—	—	Transfer to HH	Transfer to HL
Address 7	—	—	—	—	Transfer to HH

Table 2.2 32-Bit Read Operations when Big Endian has been Selected

Operation Address of src	Reading a 32-bit unit from address 0	Reading a 32-bit unit from address 1	Reading a 32-bit unit from address 2	Reading a 32-bit unit from address 3	Reading a 32-bit unit from address 4
Address 0	Transfer to HH	—	—	—	—
Address 1	Transfer to HL	Transfer to HH	—	—	—
Address 2	Transfer to LH	Transfer to HL	Transfer to HH	—	—
Address 3	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH	—
Address 4	—	Transfer to LL	Transfer to LH	Transfer to HL	Transfer to HH
Address 5	—	—	Transfer to LL	Transfer to LH	Transfer to HL
Address 6	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	Transfer to LL

Table 2.3 32-Bit Write Operations when Little Endian has been Selected

Operation Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from LL	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—
Address 2	Transfer from HL	Transfer from LH	Transfer from LL	—	—
Address 3	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL	—
Address 4	—	Transfer from HH	Transfer from HL	Transfer from LH	Transfer from LL
Address 5	—	—	Transfer from HH	Transfer from HL	Transfer from LH
Address 6	—	—	—	Transfer from HH	Transfer from HL
Address 7	—	—	—	—	Transfer from HH

Table 2.4 32-Bit Write Operations when Big Endian has been Selected

Operation Address of dest	Writing a 32-bit unit to address 0	Writing a 32-bit unit to address 1	Writing a 32-bit unit to address 2	Writing a 32-bit unit to address 3	Writing a 32-bit unit to address 4
Address 0	Transfer from HH	—	—	—	—
Address 1	Transfer from HL	Transfer from HH	—	—	—
Address 2	Transfer from LH	Transfer from HL	Transfer from HH	—	—
Address 3	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH	—
Address 4	—	Transfer from LL	Transfer from LH	Transfer from HL	Transfer from HH
Address 5	—	—	Transfer from LL	Transfer from LH	Transfer from HL
Address 6	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	Transfer from LL

Table 2.5 16-Bit Read Operations when Little Endian has been Selected

Operation Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LL	—	—	—	—	—	—
Address 1	Transfer to LH	Transfer to LL	—	—	—	—	—
Address 2	—	Transfer to LH	Transfer to LL	—	—	—	—
Address 3	—	—	Transfer to LH	Transfer to LL	—	—	—
Address 4	—	—	—	Transfer to LH	Transfer to LL	—	—
Address 5	—	—	—	—	Transfer to LH	Transfer to LL	—
Address 6	—	—	—	—	—	Transfer to LH	Transfer to LL
Address 7	—	—	—	—	—	—	Transfer to LH

Table 2.6 16-Bit Read Operations when Big Endian has been Selected

Operation Address of src	Reading a 16-bit unit from address 0	Reading a 16-bit unit from address 1	Reading a 16-bit unit from address 2	Reading a 16-bit unit from address 3	Reading a 16-bit unit from address 4	Reading a 16-bit unit from address 5	Reading a 16-bit unit from address 6
Address 0	Transfer to LH	—	—	—	—	—	—
Address 1	Transfer to LL	Transfer to LH	—	—	—	—	—
Address 2	—	Transfer to LL	Transfer to LH	—	—	—	—
Address 3	—	—	Transfer to LL	Transfer to LH	—	—	—
Address 4	—	—	—	Transfer to LL	Transfer to LH	—	—
Address 5	—	—	—	—	Transfer to LL	Transfer to LH	—
Address 6	—	—	—	—	—	Transfer to LL	Transfer to LH
Address 7	—	—	—	—	—	—	Transfer to LL

Table 2.7 16-Bit Write Operations when Little Endian has been Selected

Operation Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LL	—	—	—	—	—	—
Address 1	Transfer from LH	Transfer from LL	—	—	—	—	—
Address 2	—	Transfer from LH	Transfer from LL	—	—	—	—
Address 3	—	—	Transfer from LH	Transfer from LL	—	—	—
Address 4	—	—	—	Transfer from LH	Transfer from LL	—	—
Address 5	—	—	—	—	Transfer from LH	Transfer from LL	—
Address 6	—	—	—	—	—	Transfer from LH	Transfer from LL
Address 7	—	—	—	—	—	—	Transfer from LH

Table 2.8 16-Bit Write Operations when Big Endian has been Selected

Operation Address of dest	Writing a 16-bit unit to address 0	Writing a 16-bit unit to address 1	Writing a 16-bit unit to address 2	Writing a 16-bit unit to address 3	Writing a 16-bit unit to address 4	Writing a 16-bit unit to address 5	Writing a 16-bit unit to address 6
Address 0	Transfer from LH	—	—	—	—	—	—
Address 1	Transfer from LL	Transfer from LH	—	—	—	—	—
Address 2	—	Transfer from LL	Transfer from LH	—	—	—	—
Address 3	—	—	Transfer from LL	Transfer from LH	—	—	—
Address 4	—	—	—	Transfer from LL	Transfer from LH	—	—
Address 5	—	—	—	—	Transfer from LL	Transfer from LH	—
Address 6	—	—	—	—	—	Transfer from LL	Transfer from LH
Address 7	—	—	—	—	—	—	Transfer from LL

Table 2.9 8-Bit Read Operations when Little Endian has been Selected

Operation Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.10 8-Bit Read Operations when Big Endian has been Selected

Operation Address of src	Reading an 8-bit unit from address 0	Reading an 8-bit unit from address 1	Reading an 8-bit unit from address 2	Reading an 8-bit unit from address 3
Address 0	Transfer to LL	—	—	—
Address 1	—	Transfer to LL	—	—
Address 2	—	—	Transfer to LL	—
Address 3	—	—	—	Transfer to LL

Table 2.11 8-Bit Write Operations when Little Endian has been Selected

Operation Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

Table 2.12 8-Bit Write Operations when Big Endian has been Selected

Operation Address of dest	Writing an 8-bit unit to address 0	Writing an 8-bit unit to address 1	Writing an 8-bit unit to address 2	Writing an 8-bit unit to address 3
Address 0	Transfer from LL	—	—	—
Address 1	—	Transfer from LL	—	—
Address 2	—	—	Transfer from LL	—
Address 3	—	—	—	Transfer from LL

2.5.2 Access to I/O Registers

The addresses of I/O registers are fixed, and this is regardless of whether the setting is for little endian or big endian. Accordingly, changes to the endian do not affect access to I/O registers. For the arrangements of I/O registers, refer to the descriptions of registers in the relevant sections.

2.5.3 Notes on Access to I/O Registers

Ensure that access to I/O registers is in accord with the following rules.

- With I/O registers for which a bus width of eight bits is indicated, use instructions having operands of the same width (eight bits). That is, access these registers by using instructions with .B as the size specifier (.size), or with .B or .UB as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 16 bits is indicated, use instructions having operands of the same width (16 bits). That is, access these registers by using instructions with .W as the size specifier (.size), or with .W or .UW as the size-extension specifier (.memex).
- With I/O registers for which a bus width of 32 bits is indicated, use instructions having operands of the same width (32 bits). That is, access these registers by using instructions with .L as the size specifier (.size), or with .L size-extension specifier (.memex).

2.5.4 Data Arrangement

2.5.4.1 Data Arrangement in Registers

Figure 2.6 shows the relation between the sizes of registers and bit numbers.

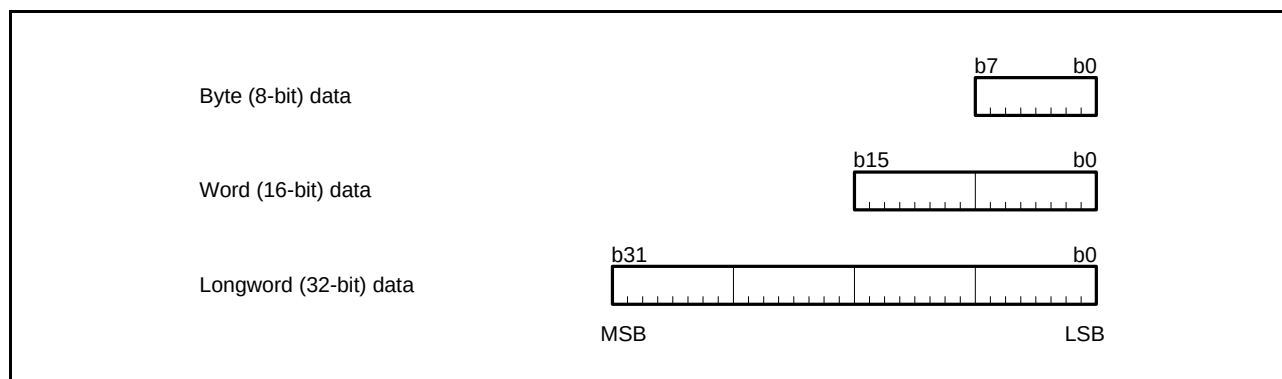


Figure 2.6 Data Arrangement in Registers

2.5.4.2 Data Arrangement in Memory

Data in memory have three sizes: byte (8-bit), word (16-bit), and longword (32-bit). The data arrangement is selectable as little endian or big endian. Figure 2.7 shows the arrangement of data in memory.

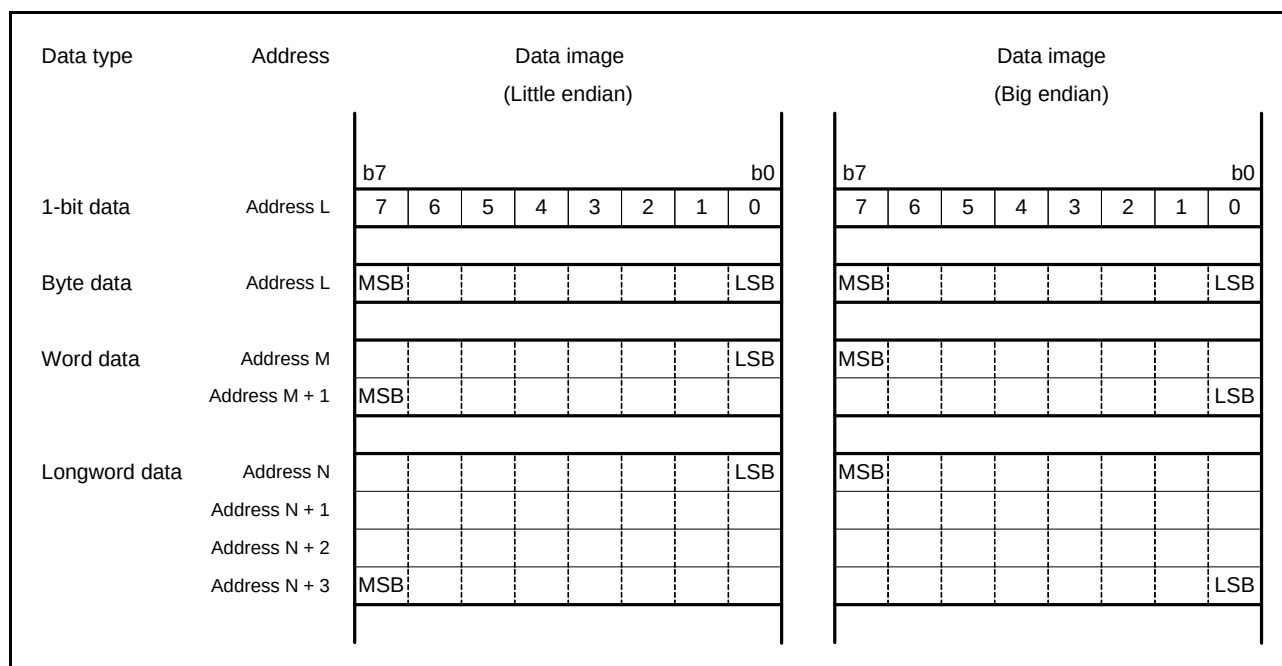


Figure 2.7 Data Arrangement in Memory

2.5.5 Notes on the Allocation of Instruction Codes

The allocation of instruction codes to an external space where the endian differs from that of the chip is prohibited. If the instruction codes are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.

2.6 Vector Table

There are two types of vector table: exception and interrupt. Each vector in the vector table consists of four bytes and specifies the address where the corresponding exception handling routine starts.

2.6.1 Exception Vector Table

In the exception vector table, the individual vectors for the privileged instruction exception, access exception, undefined instruction exception, floating-point exception, and non-maskable interrupt are allocated to the 124-byte area where the value indicated by the exception table register (EXTB) is used as the starting address (ExtBase). The reset vector is always allocated to FFFFFFFCh, regardless of the value of the exception vector table.

Figure 2.8 shows the exception vector table.

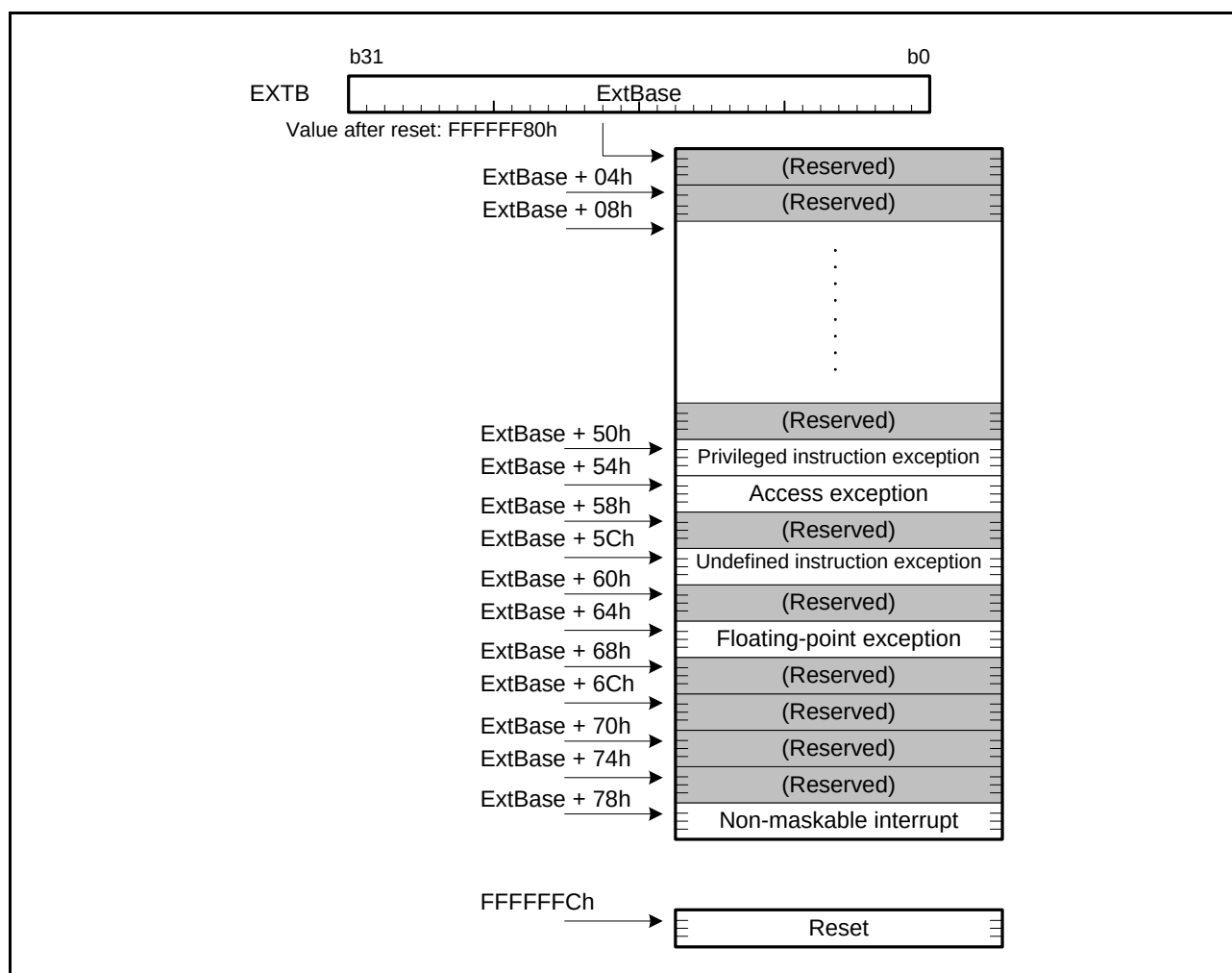


Figure 2.8 Exception Vector Table

2.6.2 Interrupt Vector Table

The address where the interrupt vector table is placed can be adjusted. The table is a 1,024-byte region that contains all vectors for unconditional traps and interrupts and starts at the address (IntBase) specified in the interrupt table register (INTB). Figure 2.9 shows the interrupt vector table.

Each vector in the interrupt vector table has a vector number from 0 to 255. Each of the INT instructions, which act as the sources of unconditional traps, is allocated to the vector that has the same number as is specified as the operand of the instruction itself (from 0 to 255). The BRK instruction is allocated to the vector with number 0. Furthermore, vector numbers (from 0 to 255) are allocated to interrupt requests in a fixed way for each product. For more on interrupt vector numbers, see section 15.3.1, Interrupt Vector Table.

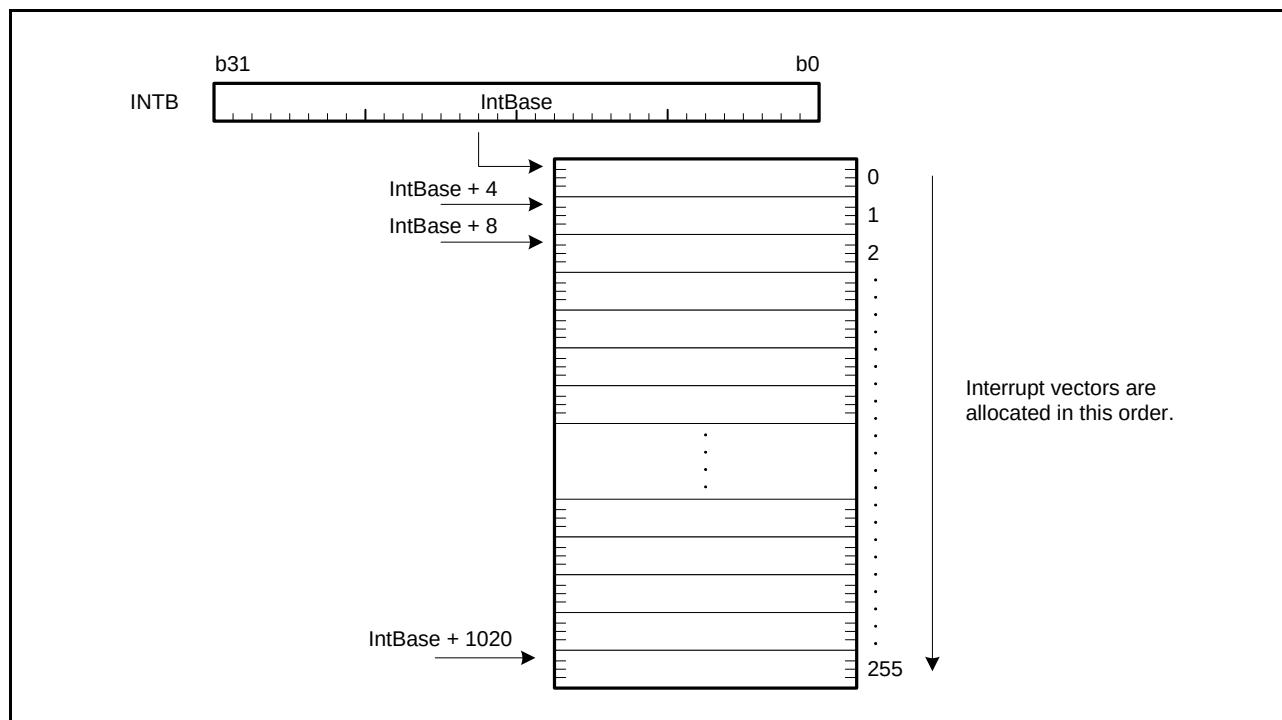


Figure 2.9 Interrupt Vector Table

2.7 Operation of Instructions

2.7.1 Restrictions on RMPA and String-Manipulation Instructions

2.7.1.1 Transfer Size and Data Prefetching

The RMPA instruction and the string-manipulation instructions (SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions) transfer data in longword units to speed up the reading of data from and writing of data to the memory. If the last of the data to be processed is less than a longword, data transfer proceeds with the sizes described below:

- RMPA, SSTR, SUNTIL, and SWHILE instructions: Size specified by the size specifier
- SCMPU, SMOVB, SMOVF, and SMOVU instructions: Byte

Additionally, in the above processing, the RMPA instruction and the string-manipulation instructions other than the SSTR instruction (that is, the SCMPU, SMOVB, SMOVF, SMOVU, SUNTIL, and SWHILE instructions) prefetch data when reading data from the memory. Data is prefetched from the prefetching start position with three bytes as the upper limit. The prefetching start positions of each operation are shown below.

- RMPA instruction: The multiplicand address specified by R1, and the multiplier address specified by R2
- SCMPU instruction: The source address specified by R1 for comparison, and the destination address specified by R2 for comparison
- SUNTIL and SWHILE instructions: The destination address specified by R1 for comparison
- SMOVB, SMOVF, and SMOVU instructions: The source address specified by R2 for transfer

2.7.1.2 Access to the External Space

Although the external space has a per-area ending-switching facility (only for data), the allocation of data to be handled by RMPA or string-manipulation instructions (SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions) to an area where the endian differs from that of the chip is prohibited, and operation is not guaranteed if this restriction is not observed. If data to be handled by RMPA or string-manipulation instructions are allocated to the external space, they must be allocated to areas where the endian setting is the same as that for the chip.

2.7.1.3 Access to I/O Registers

The allocation of data to be handled by RMPA or string-manipulation instructions (SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions) to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

2.8 Number of Cycles

2.8.1 Instruction and Number of Cycle

Table 2.13 to Table 2.20 show the number of cycles in operation of each instruction. The listed numbers of cycles for access to memory are the numbers of cycles during no-wait access. The operands in the table below indicate the following meanings.

#IMM: Immediate

flag: bit, flag

Rs, Rs2, Rd, Rd2, Ri, Rb: General-purpose register

As, Ad: Accumulator

CR: Control register

dsp: displacement

pcdsp: displacement

Table 2.13 Number of Cycles for Arithmetic/logic Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Arithmetic/logic instructions (register-register, immediate- register)	• {ABS, NEG, NOT} "Rd"/"Rs, Rd" • {ADC, MAX, MIN, ROTL, ROTR, XOR} "#IMM, Rd"/"Rs, Rd" • ADD "#IMM, Rd"/"Rs, Rd"/"#IMM, Rs, Rd"/"Rs, Rs2, Rd" • {AND, MUL, OR, SUB} "#IMM, Rd"/"Rs, Rd"/"Rs, Rs2, Rd" • {CMP, TST} "#IMM, Rs"/"Rs, Rs2" • NOP • {ROL, ROR, SAT} "Rd" • SBB "Rs, Rd" • {SHAR, SHLL, SHLR} "#IMM, Rd"/"Rs, Rd"/"#IMM, Rs, Rd"	1
	• DIV "#IMM, Rd"/"Rs, Rd"	3 to 20 ¹
	• DIVU "#IMM, Rd"/"Rs, Rd"	2 to 18 ¹
	• {EMUL, EMULU} "#IMM, Rd"/"Rs, Rd"	2
	• SATR	3
	Arithmetic/logic instructions (memory source operand)	3
	• {ADC, ADD, AND, MAX, MIN, MUL, OR, SBB, SUB, XOR} "[Rs], Rd"/"dsp[Rs], Rd" • {CMP, TST} "[Rs], Rs2"/"dsp[Rs], Rs2"	
	• DIV "[Rs], Rd / dsp[Rs], Rd"	5 to 22
	• DIVU "[Rs], Rd / dsp[Rs], Rd"	4 to 20
	• {EMUL, EMULU} "[Rs], Rd"/"dsp[Rs], Rd"	4
	• RMPA.B	6+7×floor(n/4)+4×(n%4) n: Number of processing bytes*2
	• RMPA.W	6+5×floor(n/2)+4×(n%2) n: Number of processing words*2
	• RMPA.L	6+4n n: Number of processing longwords*2

Note 1. The number of cycles for the dividing instruction varies according to the divisor and dividend.

Note 2. floor (x): Max. integer that is smaller than x.

Table 2.14 Number of Cycles for Transfer Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Transfer instructions (register-register, immediate-register)	• MOV “#IMM, Rd”/“Rs, Rd” • {MOVU, REVL, REVW} “Rs, Rd” • SCCnd “Rd” • {STNZ, STZ} “#IMM, Rd”/ “Rs, Rd”	1
	• XCHG “Rs, Rd”	2
Transfer instructions (load operation)	• {MOV, MOVU} “[Rs], Rd”/“dsp[Rs], Rd”/“[Rs+], Rd”/“[-Rs], Rd”/“[Ri, Rb], Rd” • MOVL “[Rs], Rd” • POP “Rd”	Throughput: 1 Latency: 2*1
	• POPC “CR”	Throughput: 3 Latency: 4*1
	• POPM “Rd-Rd2”	Throughput: n Latency: n+1 n: Number of registers*1, *2
Transfer instructions (store operation)	• MOV “Rs, [Rd]”/“Rs, dsp[Rd]”/“Rs, [Rd+]”/“Rs, [-Rd]”/“Rs, [Ri, Rb]”/“#IMM, dsp[Rd]”/“#IMM, [Rd]” • PUSH “Rs” • PUSHC “CR” • SCCnd “[Rd]”/“dsp[Rd]” • MOVCO “Rs, [Rd]”	1
	• PUSHM “Rs-Rs2”	n n: Number of registers*3
Transfer instructions (memory-register)	• XCHG “[Rs], Rd”/“dsp[Rs], Rd”	2
Transfer instructions (memory-memory)	• MOV “[Rs], [Rd]”/“dsp[Rs], [Rd]”/“[Rs], dsp[Rd]”/“dsp[Rs], dsp[Rd]” • PUSH “[Rs]”/“dsp[Rs]”	3

Note 1. When the load data is used by the subsequent instruction, the number of cycles described as “latency” is counted as the number of cycles for the memory load instruction. For the cycles other than the memory load instruction, the number of cycles described as “throughput” is counted.

Note 2. The POPM instruction is converted into multiple load operations. The processing is the same as the one for the load operations of the MOV instruction, where the operation is repeated for the number of specified registers.

Note 3. The PUSHM instruction is converted into multiple store operations. The processing is the same as the one for the store operations of the MOV instruction, where the operation is repeated for the number of specified registers.

Table 2.15 Number of Cycles for Bit Manipulation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Bit manipulation instructions (register)	• {BCLR, BNOT, BSET} “#IMM, Rd”/“Rs, Rd” • BMCnd “#IMM, Rd” • BTST “#IMM, Rs”/“Rs, Rs2”	1
Bit manipulation instructions (memory source operand)	• {BCLR, BNOT, BSET} “#IMM, [Rd]”/“#IMM, dsp[Rd]”/“Rs, [Rd]”/“Rs, dsp[Rd]” • BMCnd “#IMM, [Rd]”/“#IMM, dsp[Rd]” • BTST “#IMM, [Rs]”/“#IMM, dsp[Rs]”/“Rs, [Rs2]”/“Rs, dsp[Rs2]”	3

Table 2.16 Number of Cycles for Branch Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Branch instructions	• BCnd "pcdsp" • {BRA, BSR} "pcdsp"/"Rs" • {JMP, JSR} "Rs"	Branch taken: 3 Branch not taken: 1
	• RTE	6
	• RTFI	3
	• RTS	5
	• RTSD "#IMM"	5
	• RTSD "#IMM, Rd-Rd2"	Throughput: $n < 5?5:1+n$ Latency: $n < 4?5:2+n$ n: Number of registers*1

?: Conditional operator

Note 1. When the load data is used by the subsequent instruction, the number of cycles described as "latency" is counted as the number of cycles for the memory load instruction. For the cycles other than the memory load instruction, the number of cycles described as "throughput" is counted.

Table 2.17 Number of Cycles for Floating-Point Operation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
Floating-point operation instructions (register-register, immediate-register)	• {FADD, FSUB} "#IMM, Rd"/"Rs, Rd"/"Rs, Rs2, Rd"	2
	• FCMP "#IMM, Rs"/"Rs, Rs2"	1
	• FDIV "#IMM, Rd"/"Rs, Rd"	16
	• FMUL "#IMM, Rd"/"Rs, Rd" / "Rs, Rs2, Rd"	2
	• FSQRT "Rs, Rd"	16
	• {FTOI, ROUND, ITOF} "Rs, Rd"	2
	• {FTOU, UTOF} "Rs, Rd"	2
Floating-point operation instructions (memory source operand)	• {FADD, FSUB} "[Rs], Rd"/"dsp[Rs], Rd"	4
	• FCMP "[Rs], Rs2"/"dsp[Rs], Rs2"	3
	• FDIV "[Rs], Rd"/"dsp[Rs], Rd"	18
	• FMUL "[Rs], Rd"/"dsp[Rs], Rd"	4
	• FSQRT "[Rs], Rd"/"dsp[Rs], Rd"	18
	• {FTOI, ROUND, ITOF} "[Rs], Rd"/"dsp[Rs], Rd"	4
	• {FTOU, UTOF} "[Rs], Rd"/"dsp[Rs], Rd"	4

Table 2.18 Number of Cycles for DSP Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
DSP instructions	• {EMULA, EMACA, EMSBA, MULLH, MULHI, MULLO, MACLH, MACHI, MACLO, MSBLH, MSBHI, MSBLO} "Rs, Rs2, Ad" • {MVFACHI, MVFACMI, MVFACLO, MVFACGU} "#IMM, As, Rd" • {MVTACHI, MVTACLO, MVTACGU} "As, Rd" • {RDACW, RDACL, RACW, RACL} "#IMM, Ad"	1

Table 2.19 Number of Cycles for String Manipulation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
String manipulation instructions* ¹	• SCMPU	$2+4\times\text{floor}(n/4)+4\times(n\%4)$ n: Number of comparison bytes* ²
	• SMOVB	$n>3?6+3\times\text{floor}(n/4)+3\times(n\%4):2+3n$ n: Number of transfer bytes* ²
	• SMOVF, SMOVU	$2+3\times\text{floor}(n/4)+3\times(n\%4)$ n: Number of transfer bytes* ²
	• SSTR.B	$2+\text{floor}(n/4)+n\%4$ n: Number of transfer bytes* ²
	• SSTR.W	$2+\text{floor}(n/2)+n\%2$ n: Number of transfer words* ²
	• SSTR.L	$2+n$ n: Number of transfer longwords
	• SUNTIL.B, SWHILE.B	$3+3\times\text{floor}(n/4)+3\times(n\%4)$ n: Number of comparison bytes* ²
	• SUNTIL.W, SWHILE.W	$3+3\times\text{floor}(n/2)+3\times(n\%2)$ n: Number of comparison words* ²
	• SUNTIL.L, SWHILE.L	$3+3\times n$ n: Number of comparison longwords

?: Conditional operator

Note 1. Each of the SCMPU, SMOVU, SWHILE, and SUNTIL instructions ends the execution regardless of the specified cycles, if the end condition is satisfied during execution.

Note 2. floor (x): Max. integer that is smaller than x.

Table 2.20 Number of Cycles for System Manipulation Instructions

Instruction	Mnemonic (indicates the common operation when the size is omitted)	Number of Cycles
System manipulation instructions	• {CLRPSW, SETPSW}*flag" • MVTC "#IMM, CR"/"Rs, CR" • MVFC "CR, Rd" • MVTIPL "#IMM"	1
	• RTE	6
	• RTFI	3

2.8.2 Numbers of Cycles for Response to Interrupts

Table 2.21 lists numbers of cycles taken by processing for response to interrupts.

Table 2.21 Numbers of Cycles for Response to Interrupts

Type of Interrupt Request/Details of Processing	Fast Interrupt	Other Interrupts
ICU Judgment of priority order	2 cycles	
CPU Number of cycles from notification to acceptance of the interrupt request	N cycles (varies with the instruction being executed at the time the interrupt was received)	
CPU Pre-processing by hardware Saving the current PC and PSW values in RAM (or in control registers in the case of the fast interrupt) Reading of the vector Branching to the start of the exception handling routine	4 cycles	6 cycles

Times calculated from the values in Table 2.21 will be applicable when access to memory from the CPU is processed with no waiting. The RAM and code flash memory in this MCU allow such access. Numbers of cycles for response to interrupts can be minimized by placing program code (and vectors) in code flash memory and the stack in RAM.

Furthermore, place the addresses where the exception handling routine start on 8-byte boundaries.

For information on the number of cycles from notification to acceptance of the interrupt request, indicated by N in the table above, see Table 2.13 to Table 2.20.

The timing of interrupt acceptance depends on the execution state of the instruction. For more information on this, see section 14.3.1, Acceptance Timing and Saved PC Value.

3. Operating Modes

3.1 Operating Mode Types and Selection

There are two types of operating-mode selection: one is selected by the level on pins at the time of release from the reset state, and the other is selected by software after release from the reset state.

Table 3.1 shows the relationship between levels on the mode-setting pins (MD, UB) on release from the reset state and the operating mode selected at that time. For details on each of the operating modes, see section 3.3, Details of Operating Modes.

Table 3.1 Selection of Operating Modes by the Mode-Setting Pins

Mode-Setting Pin		Operating Mode
MD*1	UB	
Low	High	Boot mode (USB Interface)
Low	Low	Boot mode (SCI)
High	—	Single-chip mode

Note 1. Do not change the level on the MD pin while the MCU is operating.

The endian is selectable in single-chip mode. Endian is set by the MDE.MDE[2:0] bits in the option-setting memory. For the correspondence between the setting and endian, see Table 3.2.

Table 3.2 Selection of Endian

MDE.MDE[2:0] Bit Setting	Endian
000b	Big endian
111b	Little endian

3.2 Register Descriptions

3.2.1 Mode Monitor Register (MDMONR)

Address(es): 0008 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MD
Value after reset:	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit Name	Description	R/W
b0	MD	MD Pin Status Flag	0: The MD pin is low. 1: The MD pin is high.	R
b7 to b1	—	Reserved	These bits are read as 0.	R
b8	—	Reserved	The read value is undefined.	R
b15 to b9	—	Reserved	These bits are read as 0.	R

Note 1. This affects the level on the MD pin at the time of release from the reset state.

3.2.2 System Control Register 1 (SYSCR1)

Address(es): 0008 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RAME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RAME	RAM Enable	0: The RAM is disabled. 1: The RAM is enabled.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

RAME Bit (RAM Enable)

The RAME bit enables or disables the RAM.

A 0 should not be written to this bit during access to the RAM. When accessing the RAM immediately after changing the RAME bit from 0 (RAM disabled) to 1 (RAM enabled), make sure that the RAME bit is 1 before the access.

Even when the RAME bit is cleared to 0, the RAM retains its value. To retain the value in the RAM, keep the specified RAM standby voltage (VRAM). For details, see section 51, Electrical Characteristics.

3.3 Details of Operating Modes

3.3.1 Single-Chip Mode

In this mode, all I/O ports can be used as general input/output ports, peripheral function input/output, or interrupt input pins.

The chip starts up in single-chip mode if the high level is on the MD pin on release from the reset state.

3.3.2 Boot Mode

In this mode, the on-chip flash memory modifying program (boot program) stored in a dedicated area within the MCU operates. The on-chip flash memory (ROM and E2 DataFlash) can be modified from outside the MCU by using a USB or universal asynchronous receiver/transmitter (SCI1). For details, see [section 50, Flash Memory \(FLASH\)](#).

When a reset is released while the MD pin is low, boot mode is selected.

3.3.2.1 Boot Mode (USB Interface)

When a reset is released while the MD pin is low and the UB pin is high, boot mode (USB interface) is selected. For details on boot mode (USB interface), refer to [section 50.8.1, Boot Mode \(USB Interface\)](#).

3.3.2.2 Boot Mode (SCI)

When a reset is released while the MD pin is low and the UB pin is low, boot mode (SCI) is selected. For details on boot mode (SCI), refer to [section 50.8.2, Boot Mode \(SCI Interface\)](#).

3.4 Transitions of Operating Modes

3.4.1 Operating Mode Transitions Determined by the Mode-Setting Pins

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin and the UB pin.

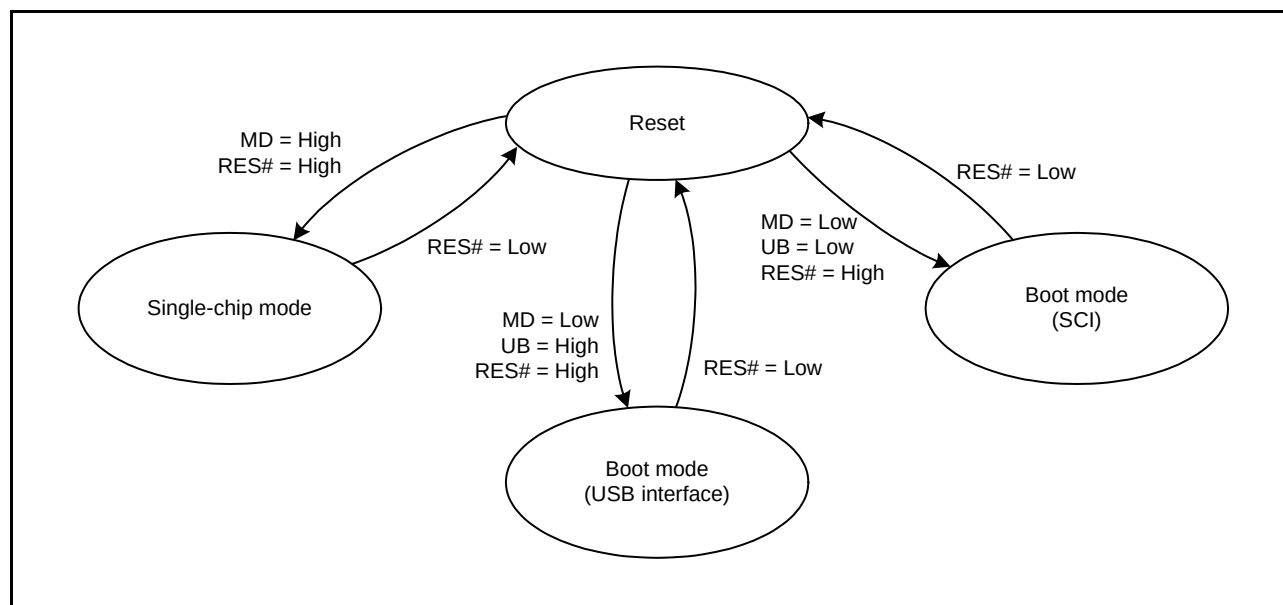


Figure 3.1 Mode-Setting Pin Levels and Operating Modes

4. Address Space

4.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 4.1 shows the memory maps in the respective operating modes.

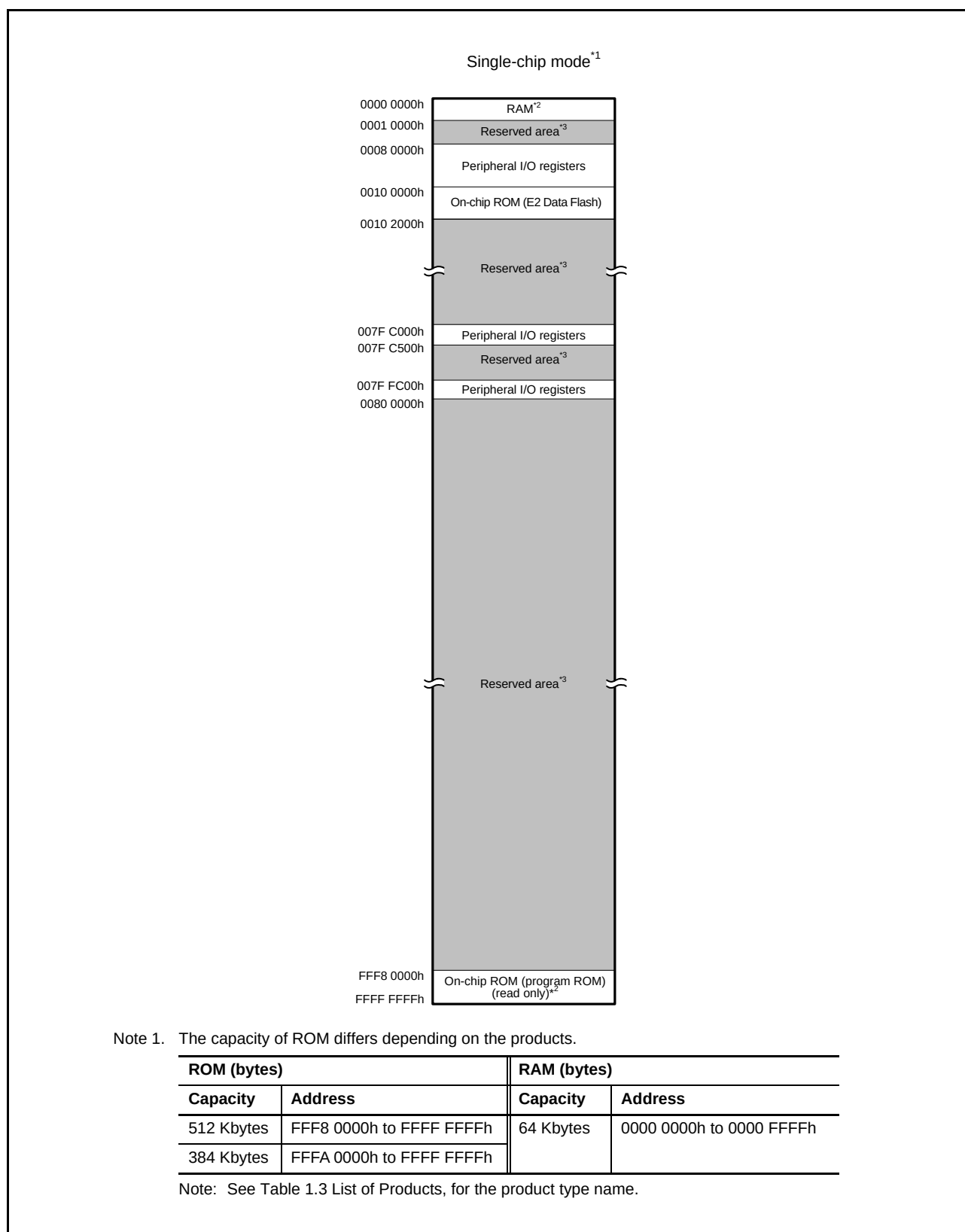


Figure 4.1 Memory Map in Each Operating Mode

5. I/O Registers

This section provides information on the on-chip I/O register addresses and bit configuration. The information is given as shown below. Notes on writing to registers are also given below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Numbers of cycles for access indicate numbers of cycles of the given base clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For numbers of clock cycles for access to I/O registers, see Table 5.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral bus 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access cycles shown in Table 5.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

(5) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order)).

5.1 I/O Register Addresses (Address Order)

Table 5.1 List of I/O Registers (Address Order) (1/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		section 3.
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK		section 3.
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		section 11.
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK		section 11.
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK		section 11.
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK		section 11.
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK		section 11.
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		section 9.
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK		section 9.
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK		section 9.
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK		section 9.
0008 002Ch	SYSTEM	USB-dedicated PLL Control Register	UPLLCR	16	16	3 ICLK		section 9.
0008 002Eh	SYSTEM	USB-dedicated PLL Control Register 2	UPLLCR2	8	8	3 ICLK		section 9.
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK		section 9.
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK		section 9.
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK		section 9.
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK		section 9.
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK		section 9.
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK		section 9.
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK		section 9.
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK		section 9.
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK		section 9.
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK		section 9.
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK		section 9.
0008 0060h	SYSTEM	Low-Speed On-Chip Oscillator Trimming Register	LOCOTRR	8	8	3 ICLK		section 9.
0008 0064h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Trimming Register	ILOCOTRR	8	8	3 ICLK		section 9.
0008 0068h	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 0	HOCOTRR0	8	8	3 ICLK		section 9.
0008 006Bh	SYSTEM	High-Speed On-Chip Oscillator Trimming Register 3	HOCOTRR3	8	8	3 ICLK		section 9.
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK		section 11.
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK		section 11.
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK		section 9.
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK		section 11.
0008 00B0h	LPT	Low-Power Timer Control Register 1	LPTCR1	8	8	3 ICLK		section 29.
0008 00B1h	LPT	Low-Power Timer Control Register 2	LPTCR2	8	8	3 ICLK		section 29.
0008 00B2h	LPT	Low-Power Timer Control Register 3	LPTCR3	8	8	3 ICLK		section 29.
0008 00B4h	LPT	Low-Power Timer Period Setting Register	LPTPRD	16	16	3 ICLK		section 29.
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK		section 29.
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK		section 29.
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		section 6.
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK		section 6.
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		section 8.
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK		section 8.
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		section 13.
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		section 16.
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK		section 16.
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK		section 16.
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK		section 16.
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK		section 16.
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		section 18.

Table 5.1 List of I/O Registers (Address Order) (2/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2	ICLK	section 18.
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	section 18.
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	section 18.
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	section 18.
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	section 18.
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2	ICLK	section 18.
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2	ICLK	section 18.
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	section 18.
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2	ICLK	section 18.
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2	ICLK	section 18.
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2	ICLK	section 18.
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2	ICLK	section 18.
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2	ICLK	section 18.
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	section 18.
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	section 18.
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	section 18.
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	section 18.
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2	ICLK	section 18.
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	section 18.
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2	ICLK	section 18.
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2	ICLK	section 18.
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2	ICLK	section 18.
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2	ICLK	section 18.
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2	ICLK	section 18.
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	section 18.
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	section 18.
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	section 18.
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	section 18.
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2	ICLK	section 18.
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	section 18.
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2	ICLK	section 18.
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2	ICLK	section 18.
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2	ICLK	section 18.
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2	ICLK	section 18.
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2	ICLK	section 18.
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2	ICLK	section 18.
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2	ICLK	section 18.
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2	ICLK	section 18.
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2	ICLK	section 18.
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2	ICLK	section 18.
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2	ICLK	section 18.
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2	ICLK	section 18.
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2	ICLK	section 18.
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2	ICLK	section 18.
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2	ICLK	section 18.
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2	ICLK	section 19.
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2	ICLK	section 19.
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2	ICLK	section 19.
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2	ICLK	section 19.
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2	ICLK	section 19.
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1	ICLK	section 17.
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1	ICLK	section 17.

Table 5.1 List of I/O Registers (Address Order) (3/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32		1 ICLK	section 17.
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32		1 ICLK	section 17.
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32		1 ICLK	section 17.
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32		1 ICLK	section 17.
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32		1 ICLK	section 17.
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32		1 ICLK	section 17.
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32		1 ICLK	section 17.
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32		1 ICLK	section 17.
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32		1 ICLK	section 17.
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32		1 ICLK	section 17.
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32		1 ICLK	section 17.
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32		1 ICLK	section 17.
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32		1 ICLK	section 17.
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32		1 ICLK	section 17.
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32		1 ICLK	section 17.
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32		1 ICLK	section 17.
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32		1 ICLK	section 17.
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32		1 ICLK	section 17.
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32		1 ICLK	section 17.
0008 6520h	MPU	Region Search Address Register	MPSA	32	32		1 ICLK	section 17.
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16		1 ICLK	section 17.
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16		1 ICLK	section 17.
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32		1 ICLK	section 17.
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32		1 ICLK	section 17.
0008 7010h to 0008 70FFh	ICU	Interrupt Request Register 016 to Interrupt Request Register 255	IR016 to IR255	8	8		2 ICLK	section 15.
0008 711Bh to 0008 71FFh	ICU	DTC Activation Enable Register 027 to DTC Activation Enable Register 255	DTCER027 to DTCER255	8	8		2 ICLK	section 15.
0008 7202h to 0008 721Fh	ICU	Interrupt Request Enable Register 02 to Interrupt Request Enable Register 1F	IER02 to IER1F	8	8		2 ICLK	section 15.
0008 72E0h	ICU	Software Interrupt Generation Register	SWINTR	8	8		2 ICLK	section 15.
0008 72F0h	ICU	Fast Interrupt Set Register	FIR	16	16		2 ICLK	section 15.
0008 7300h to 0008 73FFh	ICU	Interrupt Source Priority Register 000 to Interrupt Source Priority Register 255	IPR000 to IPR255	8	8		2 ICLK	section 15.
0008 7400h	ICU	DMAC Trigger Select Register 0	DMRSR0	8	8		2 ICLK	section 15.
0008 7404h	ICU	DMAC Trigger Select Register 1	DMRSR1	8	8		2 ICLK	section 15.
0008 7408h	ICU	DMAC Trigger Select Register 2	DMRSR2	8	8		2 ICLK	section 15.
0008 740Ch	ICU	DMAC Trigger Select Register 3	DMRSR3	8	8		2 ICLK	section 15.
0008 7500h to 0008 7507h	ICU	IRQ Control Register 0 to IRQ Control Register 7	IRQCR0 to IRQCR7	8	8		2 ICLK	section 15.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8		2 ICLK	section 15.
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16		2 ICLK	section 15.
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8		2 ICLK	section 15.
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8		2 ICLK	section 15.
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8		2 ICLK	section 15.
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8		2 ICLK	section 15.
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8		2 ICLK	section 15.
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8		2 ICLK	section 15.
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK	section 27.

Table 5.1 List of I/O Registers (Address Order) (4/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB	2 ICLK	section 27.
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2 or 3 PCLKB	2 ICLK	section 30.
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2 or 3 PCLKB	2 ICLK	section 30.
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2 or 3 PCLKB	2 ICLK	section 30.
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2 or 3 PCLKB	2 ICLK	section 30.
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB	2 ICLK	section 31.
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB	2 ICLK	section 31.
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB	2 ICLK	section 31.
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB	2 ICLK	section 31.
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB	2 ICLK	section 31.
0008 8040h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB	2 ICLK	section 45.
0008 8042h	DA	D/A Data Register 1	DADR1	16	16	2 or 3 PCLKB	2 ICLK	section 45.
0008 8044h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB	2 ICLK	section 45.
0008 8045h	DA	Data Register Format Select Register	DADPR	8	8	2 or 3 PCLKB	2 ICLK	section 45.
0008 8046h	DA	D/A A/D Synchronous Start Control Register	DAADSCR	8	8	2 or 3 PCLKB	2 ICLK	section 45.
0008 8047h	DA	D/A VREF Control Register	DAVREFCR	8	8	2 or 3 PCLKB	2 ICLK	section 45.
0008 8100h	TPU	Timer Start Register	TSTR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8101h	TPU	Timer Synchronous Register	TSYR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8111h	TPU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8112h	TPU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8114h	TPU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8115h	TPU0	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8116h	TPU0	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8118h	TPU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 811Ah	TPU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 811Ch	TPU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 811Eh	TPU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8120h	TPU1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8121h	TPU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8122h	TPU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8124h	TPU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8125h	TPU1	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8126h	TPU1	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8128h	TPU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 812Ah	TPU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK	section 25.

Table 5.1 List of I/O Registers (Address Order) (5/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 8130h	TPU2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8131h	TPU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8132h	TPU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8134h	TPU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8135h	TPU2	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8136h	TPU2	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8138h	TPU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 813Ah	TPU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8140h	TPU3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8141h	TPU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8142h	TPU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8143h	TPU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8144h	TPU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8145h	TPU3	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8146h	TPU3	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8148h	TPU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 814Ah	TPU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 814Ch	TPU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 814Eh	TPU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8150h	TPU4	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8151h	TPU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8152h	TPU4	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8154h	TPU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8155h	TPU4	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8156h	TPU4	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8158h	TPU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 815Ah	TPU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8160h	TPU5	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8161h	TPU5	Timer Mode Register	TMDR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8162h	TPU5	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8164h	TPU5	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8165h	TPU5	Timer Status Register	TSR	8	8	2 or 3 PCLKB	2 ICLK	section 25.
0008 8166h	TPU5	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8168h	TPU5	Timer General Register A	TGRA	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 816Ah	TPU5	Timer General Register B	TGRB	16	16	2 or 3 PCLKB	2 ICLK	section 25.
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8204h	TMR01	Time Constant Register A	TCORA	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB	2 ICLK	section 26.
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8206h	TMR01	Time Constant Register B	TCORB	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB	2 ICLK	section 26.
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8208h	TMR01	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB	2 ICLK	section 26.
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 820Ah	TMR01	Timer Counter Control Register	TCCR	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB	2 ICLK	section 26.
0008 820Ch	TMR0	Timer Counter Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK	section 26.

Table 5.1 List of I/O Registers (Address Order) (6/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8214h	TMR23	Time Constant Register A	TCORA	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK	section 26.
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8216h	TMR23	Time Constant Register B	TCORB	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK	section 26.
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8218h	TMR23	Timer Counter	TCNT	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 8219h	TMR3	Timer Counter	TCNT	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK	section 26.
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 821Ah	TMR23	Timer Counter Control Register	TCCR	16	16	2 or 3 PCLKB	2 ICLK	section 26.
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8 ^{*1}	2 or 3 PCLKB	2 ICLK	section 26.
0008 821Ch	TMR2	Timer Counter Start Register	TCSTR	8	8	2 or 3 PCLKB	2 ICLK	section 26.
0008 8280h	CRC	CRC Control Register	CRCCR	8	8	2 or 3 PCLKB	2 ICLK	section 39.
0008 8281h	CRC	CRC Data Input Register	CRCDIR	8	8	2 or 3 PCLKB	2 ICLK	section 39.
0008 8282h	CRC	CRC Data Output Register	CRCDOR	16	16	2 or 3 PCLKB	2 ICLK	section 39.
0008 8300h	RIIC0	I ² C-bus Control Register 1	ICCR1	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8301h	RIIC0	I ² C-bus Control Register 2	ICCR2	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8302h	RIIC0	I ² C-bus Mode Register 1	ICMR1	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8303h	RIIC0	I ² C-bus Mode Register 2	ICMR2	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8304h	RIIC0	I ² C-bus Mode Register 3	ICMR3	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8305h	RIIC0	I ² C-bus Function Enable Register	ICFER	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8306h	RIIC0	I ² C-bus Status Enable Register	ICSER	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8307h	RIIC0	I ² C-bus Interrupt Enable Register	ICIER	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8308h	RIIC0	I ² C-bus Status Register 1	ICSR1	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8309h	RIIC0	I ² C-bus Status Register 2	ICSR2	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8310h	RIIC0	I ² C-bus Bit Rate Low-Level Register	ICBRL	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8311h	RIIC0	I ² C-bus Bit Rate High-Level Register	ICBRH	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8312h	RIIC0	I ² C-bus Transmit Data Register	ICDRT	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8313h	RIIC0	I ² C-bus Receive Data Register	ICDRR	8	8	2 or 3 PCLKB	2 ICLK	section 35.
0008 8380h	RSPI0	RSPI Control Register	SPCR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 8381h	RSPI0	RSPI Slave Select Polarity Register	SSLP	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 8382h	RSPI0	RSPI Pin Control Register	SPPCR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 8383h	RSPI0	RSPI Status Register	SPSR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 8384h	RSPI0	RSPI Data Register	SPDR	32	16, 32	2 or 3 PCLKB	2 ICLK	section 38.
0008 8388h	RSPI0	RSPI Sequence Control Register	SPSCR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 8389h	RSPI0	RSPI Sequence Status Register	SPSSR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 838Ah	RSPI0	RSPI Bit Rate Register	SPBR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 838Bh	RSPI0	RSPI Data Control Register	SPDCR	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 838Ch	RSPI0	RSPI Clock Delay Register	SPCKD	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 838Dh	RSPI0	RSPI Slave Select Negation Delay Register	SSLND	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 838Eh	RSPI0	RSPI Next-Access Delay Register	SPND	8	8	2 or 3 PCLKB	2 ICLK	section 38.

Table 5.1 List of I/O Registers (Address Order) (7/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK ≥ PCLK	ICLK < PCLK	
0008 838Fh	RSPi0	RSPi Control Register 2	SPCR2	8	8	2 or 3 PCLKB	2 ICLK	section 38.
0008 8390h	RSPi0	RSPi Command Register 0	SPCMD0	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 8392h	RSPi0	RSPi Command Register 1	SPCMD1	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 8394h	RSPi0	RSPi Command Register 2	SPCMD2	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 8396h	RSPi0	RSPi Command Register 3	SPCMD3	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 8398h	RSPi0	RSPi Command Register 4	SPCMD4	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 839Ah	RSPi0	RSPi Command Register 5	SPCMD5	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 839Ch	RSPi0	RSPi Command Register 6	SPCMD6	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 839Eh	RSPi0	RSPi Command Register 7	SPCMD7	16	16	2 or 3 PCLKB	2 ICLK	section 38.
0008 8410h	IRDA	IrDA Control Register	IRCR	8	8	2 or 3 PCLKB	2 ICLK	section 34.
0008 8900h	POE	Input Level Control/Status Register 1	ICSR1	16	8, 16	2 or 3 PCLKB	2 ICLK	section 24.
0008 8902h	POE	Output Level Control/Status Register 1	OCSR1	16	8, 16	2 or 3 PCLKB	2 ICLK	section 24.
0008 8908h	POE	Input Level Control/Status Register 2	ICSR2	16	8, 16	2 or 3 PCLKB	2 ICLK	section 24.
0008 890Ah	POE	Software Port Output Enable Register	SPOER	8	8	2 or 3 PCLKB	2 ICLK	section 24.
0008 890Bh	POE	Port Output Enable Control Register 1	POECR1	8	8	2 or 3 PCLKB	2 ICLK	section 24.
0008 890Ch	POE	Port Output Enable Control Register 2	POECR2	8	8	2 or 3 PCLKB	2 ICLK	section 24.
0008 890Eh	POE	Input Level Control/Status Register 3	ICSR3	16	8, 16	2 or 3 PCLKB	2 ICLK	section 24.
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Select Register 0	ADADS0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Select Register 1	ADADS1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9012h	S12AD	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9042h	S12AD	A/D Data Register 17	ADDR17	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9044h	S12AD	A/D Data Register 18	ADDR18	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9046h	S12AD	A/D Data Register 19	ADDR19	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9048h	S12AD	A/D Data Register 20	ADDR20	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9056h	S12AD	A/D Data Register 27	ADDR27	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 907Dh	S12AD	A/D Event Link Control Register	ADELCCR	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 908Ah	S12AD	A/D High-Potential/Low-Potential Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB	2 ICLK	section 44.

Table 5.1 List of I/O Registers (Address Order) (8/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 908Ch	S12AD	A/D Compare Function Window A/B Status Monitor Register	ADWINMON	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 9090h	S12AD	A/D Compare Function Control Register	ADCMPCR	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9092h	S12AD	A/D Compare Function Window A Extended Input Select Register	ADCMPSER	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 9093h	S12AD	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	ADCMPLER	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 9094h	S12AD	A/D Compare Function Window A Channel Select Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9096h	S12AD	A/D Compare Function Window A Channel Select Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 9098h	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 0	ADCMPLR0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 909Ah	S12AD	A/D Compare Function Window A Comparison Condition Setting Register 1	ADCMPLR1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 909Ch	S12AD	A/D Compare Function Window A Lower-Side Level Setting Register	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 909Eh	S12AD	A/D Compare Function Window A Upper-Side Level Setting Register	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90A0h	S12AD	A/D Compare Function Window A Channel Status Register 0	ADCMPSR0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90A2h	S12AD	A/D Compare Function Window A Channel Status Register 1	ADCMPSR1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90A4h	S12AD	A/D Compare Function Window A Extended Input Channel Status Register	ADCMPSER	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90A6h	S12AD	A/D Compare Function Window B Channel Select Register	ADCMPSNR	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90A8h	S12AD	A/D Compare Function Window B Lower-Side Level Setting Register	ADWINLLB	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90AAh	S12AD	A/D Compare Function Window B Upper-Side Level Setting Register	ADWINULB	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90ACh	S12AD	A/D Compare Function Window B Channel Status Register	ADCMPSR	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90B0h	S12AD	A/D Data Storage Buffer Register 0	ADBUF0	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90B2h	S12AD	A/D Data Storage Buffer Register 1	ADBUF1	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90B4h	S12AD	A/D Data Storage Buffer Register 2	ADBUF2	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90B6h	S12AD	A/D Data Storage Buffer Register 3	ADBUF3	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90B8h	S12AD	A/D Data Storage Buffer Register 4	ADBUF4	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90BAh	S12AD	A/D Data Storage Buffer Register 5	ADBUF5	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90BCh	S12AD	A/D Data Storage Buffer Register 6	ADBUF6	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90BEh	S12AD	A/D Data Storage Buffer Register 7	ADBUF7	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90C0h	S12AD	A/D Data Storage Buffer Register 8	ADBUF8	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90C2h	S12AD	A/D Data Storage Buffer Register 9	ADBUF9	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90C4h	S12AD	A/D Data Storage Buffer Register 10	ADBUF10	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90C6h	S12AD	A/D Data Storage Buffer Register 11	ADBUF11	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90C8h	S12AD	A/D Data Storage Buffer Register 12	ADBUF12	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90CAh	S12AD	A/D Data Storage Buffer Register 13	ADBUF13	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90CCh	S12AD	A/D Data Storage Buffer Register 14	ADBUF14	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90CEh	S12AD	A/D Data Storage Buffer Register 15	ADBUF15	16	16	2 or 3 PCLKB	2 ICLK	section 44.
0008 90D0h	S12AD	A/D Data Storage Buffer Enable Register	ADBUFEN	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90D2h	S12AD	A/D Data Storage Buffer Pointer Register	ADBUFPTR	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90DEh	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90DFh	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E4h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E5h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 90E6h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB	2 ICLK	section 44.

Table 5.1 List of I/O Registers (Address Order) (9/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 90E7h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB	2 ICLK	section 44.
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A020h	SMCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A022h	SMCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A024h	SMCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A026h	SMCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A029h	SCI1	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A02Ah	SCI1	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A02Bh	SCI1	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A02Ch	SCI1	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A02Eh	SCI1	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 A02Eh	SCI1	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A02Fh	SCI1	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A030h	SCI1	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 A030h	SCI1	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A031h	SCI1	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A032h	SCI1	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A0h	SMCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A2h	SMCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A4h	SMCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A6h	SMCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0A9h	SCI5	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0AAh	SCI5	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0ABh	SCI5	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0ACh	SCI5	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0AEh	SCI5	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 A0AEh	SCI5	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.

Table 5.1 List of I/O Registers (Address Order) (10/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 A100h	SMCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A102h	SMCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A104h	SMCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A106h	SMCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A109h	SCI8	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A10Ah	SCI8	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A10Bh	SCI8	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A10Ch	SCI8	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A10Eh	SCI8	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 A10Eh	SCI8	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A10Fh	SCI8	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A110h	SCI8	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 A110h	SCI8	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A111h	SCI8	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A112h	SCI8	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 A500h	SSI0	Control Register	SSICR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 A504h	SSI0	Status Register	SSISR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 A510h	SSI0	FIFO Control Register	SSIFCR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 A514h	SSI0	FIFO Status Register	SSIFSR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 A518h	SSI0	Transmit FIFO Data Register	SSIFTDR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 A51Ch	SSI0	Receive FIFO Data Register	SSIFRDR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 A520h	SSI0	TDM Mode Register	SSITDMR	32	32	2 or 3 PCLKB	2 ICLK	section 37.
0008 AC00h	SDHI	Command Register	SDCMD	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC08h	SDHI	Argument Register	SDARG	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC10h	SDHI	Data Stop Register	SDSTOP	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC14h	SDHI	Block Count Register	SDBLKCNT	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC18h	SDHI	Response Register 10	SDRSP10	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.

Table 5.1 List of I/O Registers (Address Order) (11/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK ≥ PCLK	ICLK < PCLK	
0008 AC20h	SDHI	Response Register 32	SDRSP32	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC28h	SDHI	Response Register 54	SDRSP54	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC30h	SDHI	Response Register 76	SDRSP76	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC38h	SDHI	SD Status Register 1	SDSTS1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC3Ch	SDHI	SD Status Register 2	SDSTS2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC40h	SDHI	SD Interrupt Mask Register 1	SDIMSK1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC44h	SDHI	SD Interrupt Mask Register 2	SDIMSK2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC48h	SDHI	SDHI Clock Control Register	SDCLKCR	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC4Ch	SDHI	Transfer Data Size Register	SDSIZE	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC50h	SDHI	Card Access Option Register	SDOPT	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC58h	SDHI	SD Error Status Register 1	SDERSTS1	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC5Ch	SDHI	SD Error Status Register 2	SDERSTS2	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC60h	SDHI	SD Buffer Register	SDBUFR	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.

Table 5.1 List of I/O Registers (Address Order) (12/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 AC68h	SDHI	SDIO Mode Control Register	SDIOMD	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC6Ch	SDHI	SDIO Status Register	SDIOSTS	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 AC70h	SDHI	SDIO Interrupt Mask Register	SDIOIMSK	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 ADB0h	SDHI	DMA Transfer Enable Register	SDDMAEN	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 ADC0h	SDHI	SDHI Software Reset Register	SDRST	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 ADE0h	SDHI	Swap Control Register	SDSWAP	32	32	3 or 4 PCLKB cycles when reading, 2 or 3 PCLKB cycles when writing	3 ICLK cycles when reading, 2 ICLK cycles when writing	section 40.
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB	2 ICLK	section 10.
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB	2 ICLK	section 10.
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB	2 ICLK	section 10.
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB	2 ICLK	section 10.
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB	2 ICLK	section 10.
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB	2 ICLK	section 10.
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB	2 ICLK	section 10.
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB	2 ICLK	section 10.
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB	2 ICLK	section 48.
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB	2 ICLK	section 48.
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB	2 ICLK	section 48.
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B109h	ELC	Event Link Setting Register 8	ELSR8	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2 or 3 PCLKB	2 ICLK	section 20.

Table 5.1 List of I/O Registers (Address Order) (13/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B11Eh	ELC	Event Link Setting Register 29	ELSR29	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB	2 ICLK	section 20.
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B300h	SMCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B302h	SMCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B304h	SMCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B306h	SMCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B30Eh	SCI12	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 B30Eh	SCI12	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B30Fh	SCI12	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B310h	SCI12	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB	2 ICLK	section 33.
0008 B310h	SCI12	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B311h	SCI12	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B312h	SCI12	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.

Table 5.1 List of I/O Registers (Address Order) (14/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 or 3 PCLKB	2 ICLK	section 33.
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C00Ch	PORTC	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C012h	PORTJ	Port Direction Register	PDR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C021h	PORT1	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C022h	PORT2	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C023h	PORT3	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C024h	PORT4	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C02Bh	PORTB	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C02Ch	PORTC	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C02Dh	PORTD	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C02Eh	PORTE	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C032h	PORTJ	Port Output Data Register	PODR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C040h	PORT0	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C041h	PORT1	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C042h	PORT2	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C043h	PORT3	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C044h	PORT4	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C04Bh	PORTB	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C04Ch	PORTC	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C04Dh	PORTD	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C04Eh	PORTE	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C052h	PORTJ	Port Input Data Register	PIDR	8	8	3 or 4 PCLKB	3 ICLK	section 21.
0008 C060h	PORT0	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C061h	PORT1	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C064h	PORT4	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.

Table 5.1 List of I/O Registers (Address Order) (15/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0A4h	PORTJ	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0CCh	PORTC	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0D2h	PORTJ	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0ECh	PORTC	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C0F2h	PORTJ	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C120h	PORT	Port Switching Register B	PSRB	8	8	2 or 3 PCLKB	2 ICLK	section 21.
0008 C143h	MPC	P03 Pin Function Control Register	P03PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C145h	MPC	P05 Pin Function Control Register	P05PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C147h	MPC	P07 Pin Function Control Register	P07PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C14Ch	MPC	P14 Pin Function Control Register	P14PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C14Dh	MPC	P15 Pin Function Control Register	P15PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C14Eh	MPC	P16 Pin Function Control Register	P16PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C14Fh	MPC	P17 Pin Function Control Register	P17PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C155h	MPC	P25 Pin Function Control Register	P25PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C156h	MPC	P26 Pin Function Control Register	P26PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.

Table 5.1 List of I/O Registers (Address Order) (16/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C198h	MPC	PB0 Pin Function Control Register	PB0PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C199h	MPC	PB1 Pin Function Control Register	PB1PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C19Bh	MPC	PB3 Pin Function Control Register	PB3PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C19Dh	MPC	PB5 Pin Function Control Register	PB5PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C19Fh	MPC	PB7 Pin Function Control Register	PB7PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A0h	MPC	PC0 Pin Function Control Register	PC0PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A2h	MPC	PC2 Pin Function Control Register	PC2PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A3h	MPC	PC3 Pin Function Control Register	PC3PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A4h	MPC	PC4 Pin Function Control Register	PC4PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A5h	MPC	PC5 Pin Function Control Register	PC5PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A6h	MPC	PC6 Pin Function Control Register	PC6PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1A7h	MPC	PC7 Pin Function Control Register	PC7PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1ABh	MPC	PD3 Pin Function Control Register	PD3PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1B0h	MPC	PE0 Pin Function Control Register	PE0PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1B1h	MPC	PE1 Pin Function Control Register	PE1PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1B2h	MPC	PE2 Pin Function Control Register	PE2PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1B3h	MPC	PE3 Pin Function Control Register	PE3PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1B4h	MPC	PE4 Pin Function Control Register	PE4PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C1D3h	MPC	PJ3 Pin Function Control Register	PJ3PFS	8	8	2 or 3 PCLKB	2 ICLK	section 22.
0008 C290h	SYSTEM	Reset Status Register 0	RSTSR0	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 6.
0008 C291h	SYSTEM	Reset Status Register 1	RSTSR1	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 6.
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 9.
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 8.
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVL	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 8.
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 8.
0008 C29Dh	SYSTEM	VBATT Control Register	VBATTCR	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 12.
0008 C29Eh	SYSTEM	VBATT Status Register	VBATTSR	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 12.
0008 C29Fh	SYSTEM	VBATT Pin Voltage Drop Detection Interrupt Control Register	VBTLVDICR	8	8	4 or 5 PCLKB	2 or 3 ICLK	section 12.
0008 C400h	RTC	64-Hz Counter	R64CNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C402h	RTC	Second Counter	RSECCNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C408h	RTC	Day-of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB	2 ICLK	section 28.
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB	2 ICLK	section 28.

Table 5.1 List of I/O Registers (Address Order) (17/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLKB	ICLK $<$ PCLKB	
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB	2 ICLK	section 28.
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB	2 ICLK	section 28.
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C440h	RTC	Time Capture Control Register 0	RTCCR0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C442h	RTC	Time Capture Control Register 1	RTCCR1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C452h	RTC	Second Capture Register 0	RSECCP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C452h	RTC	BCNT0 Capture Register 0	BCNT0CP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C454h	RTC	Minute Capture Register 0	RMINCP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C454h	RTC	BCNT1 Capture Register 0	BCNT1CP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C456h	RTC	Hour Capture Register 0	RHRCP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C456h	RTC	BCNT2 Capture Register 0	BCNT2CP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C45Ah	RTC	Date Capture Register 0	RDAYCP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C45Ah	RTC	BCNT3 Capture Register 0	BCNT3CP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C45Ch	RTC	Month Capture Register 0	RMONCP0	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C462h	RTC	Second Capture Register 1	RSECCP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C462h	RTC	BCNT0 Capture Register 1	BCNT0CP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C464h	RTC	Minute Capture Register 1	RMINCP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C464h	RTC	BCNT1 Capture Register 1	BCNT1CP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C466h	RTC	Hour Capture Register 1	RHRCP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C466h	RTC	BCNT2 Capture Register 1	BCNT2CP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C46Ah	RTC	Date Capture Register 1	RDAYCP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C46Ah	RTC	BCNT3 Capture Register 1	BCNT3CP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C46Ch	RTC	Month Capture Register 1	RMONCP1	8	8	2 or 3 PCLKB	2 ICLK	section 28.
0008 C5A0h	CMPB	Comparator B1 Control Register 1	CPB1CNT1	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A1h	CMPB	Comparator B1 Control Register 2	CPB1CNT2	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A2h	CMPB	Comparator B1 Flag Register	CPB1FLG	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A3h	CMPB	Comparator B1 Interrupt Control Register	CPB1INT	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A4h	CMPB	Comparator B1 Filter Select Register	CPB1F	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A5h	CMPB	Comparator B1 Mode Select Register	CPB1MD	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A6h	CMPB	Comparator B1 Reference Input Voltage Select Register	CPB1REF	8	8	2 or 3 PCLKB	2 ICLK	section 47.
0008 C5A7h	CMPB	Comparator B1 Output Control Register	CPB1OCR	8	8	2 or 3 PCLKB	2 ICLK	section 47.
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$	section 32.
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^2$	section 32.
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3, 4 PCLKB	2 ICLK	section 32.

Table 5.1 List of I/O Registers (Address Order) (18/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLKB	ICLK $<$ PCLKB	
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3, 4 PCLKB	2 ICLK	section 32.
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0036h	USB0	BRDY Interrupt Enable Register	BRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0038h	USB0	NRDY Interrupt Enable Register	NRDYENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 003Ah	USB0	BEMP Interrupt Enable Register	BEMPENB	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 003Ch	USB0	SOF Output Configuration Register	SOFCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0040h	USB0	Interrupt Status Register 0	INTSTS0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0042h	USB0	Interrupt Status Register 1	INTSTS1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0046h	USB0	BRDY Interrupt Status Register	BRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0048h	USB0	NRDY Interrupt Status Register	NRDYSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 004Ah	USB0	BEMP Interrupt Status Register	BEMPSTS	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 004Ch	USB0	Frame Number Register	FRMNUM	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0054h	USB0	USB Request Type Register	USBREQ	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.

Table 5.1 List of I/O Registers (Address Order) (19/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 0056h	USB0	USB Request Value Register	USBVAL	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0058h	USB0	USB Request Index Register	USBINDX	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 005Ah	USB0	USB Request Length Register	USBLENG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 005Ch	USB0	DCP Configuration Register	DCPCFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 005Eh	USB0	DCP Maximum Packet Size Register	DCPMAXP	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0060h	USB0	DCP Control Register	DCPCTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0064h	USB0	Pipe Window Select Register	PIPESEL	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0068h	USB0	Pipe Configuration Register	PIPECFG	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 006Ch	USB0	Pipe Maximum Packet Size Register	PIPEMAXP	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 006Eh	USB0	Pipe Cycle Control Register	PIPEPERI	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0070h	USB0	Pipe1 Control Register	PIPE1CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0072h	USB0	Pipe2 Control Register	PIPE2CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0074h	USB0	Pipe3 Control Register	PIPE3CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0076h	USB0	Pipe4 Control Register	PIPE4CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0078h	USB0	Pipe5 Control Register	PIPE5CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 007Ah	USB0	Pipe6 Control Register	PIPE6CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.

Table 5.1 List of I/O Registers (Address Order) (20/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 007Ch	USB0	Pipe7 Control Register	PIPE7CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 007Eh	USB0	Pipe8 Control Register	PIPE8CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0080h	USB0	Pipe9 Control Register	PIPE9CTR	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0090h	USB0	Pipe1 Transaction Counter Enable Register	PIPE1TRE	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0092h	USB0	Pipe1 Transaction Counter Register	PIPE1TRN	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0094h	USB0	Pipe2 Transaction Counter Enable Register	PIPE2TRE	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0096h	USB0	Pipe2 Transaction Counter Register	PIPE2TRN	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0098h	USB0	Pipe3 Transaction Counter Enable Register	PIPE3TRE	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 009Ah	USB0	Pipe3 Transaction Counter Register	PIPE3TRN	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 009Ch	USB0	Pipe4 Transaction Counter Enable Register	PIPE4TRE	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 009Eh	USB0	Pipe4 Transaction Counter Register	PIPE4TRN	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00A0h	USB0	Pipe5 Transaction Counter Enable Register	PIPE5TRE	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00A2h	USB0	Pipe5 Transaction Counter Register	PIPE5TRN	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00B0h	USB0	BC Control Register 0	USBBCCTRL0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00CCh	USB0	USB Module Control Register	USBMC	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00D0h	USB0	Device Address 0 Configuration Register	DEVADD0	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.

Table 5.1 List of I/O Registers (Address Order) (21/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 00D2h	USB0	Device Address 1 Configuration Register	DEVADD1	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00D4h	USB0	Device Address 2 Configuration Register	DEVADD2	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00D6h	USB0	Device Address 3 Configuration Register	DEVADD3	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00D8h	USB0	Device Address 4 Configuration Register	DEVADD4	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 00DAh	USB0	Device Address 5 Configuration Register	DEVADD5	16	16	9 PCLKB or more	Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*2}	section 32.
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Control Register	CTSUSST	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0908h	CTSU	CTSU Channel Enable Control Register 2	CTSUCHAC2	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0909h	CTSU	CTSU Channel Enable Control Register 3	CTSUCHAC3	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 090Ah	CTSU	CTSU Channel Enable Control Register 4	CTSUCHAC4	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 090Dh	CTSU	CTSU Channel Transmit/Receive Control Register 2	CTSUCHTRC2	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 090Eh	CTSU	CTSU Channel Transmit/Receive Control Register 3	CTSUCHTRC3	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 090Fh	CTSU	CTSU Channel Transmit/Receive Control Register 4	CTSUCHTRC4	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	2 or 3 PCLKB	2 ICLK	section 43.
000A 0912h	CTSU	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	CTSUSSC	16	16	2 or 3 PCLKB	2 ICLK	section 43.
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	2 or 3 PCLKB	2 ICLK	section 43.
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	2 or 3 PCLKB	2 ICLK	section 43.
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	2 or 3 PCLKB	2 ICLK	section 43.
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	2 or 3 PCLKB	2 ICLK	section 43.
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	2 or 3 PCLKB	2 ICLK	section 43.
000A 8300h	RSCAN0	Bit Configuration Register L	CFGL	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8302h	RSCAN0	Bit Configuration Register H	CFGH	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8304h	RSCAN0	Control Register L	CTRL	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8306h	RSCAN0	Control Register H	CTRH	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8308h	RSCAN0	Status Register L	STSL	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 830Ah	RSCAN0	Status Register H	STSH	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 830Ch	RSCAN0	Error Flag Register L	ERFLL	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 830Eh	RSCAN0	Error Flag Register H	ERFLH	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8322h	RSCAN	Global Configuration Register L	GCFGL	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8324h	RSCAN	Global Configuration Register H	GCFGH	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8326h	RSCAN	Global Control Register L	GCTRL	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (22/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 8328h	RSCAN	Global Control Register H	GCTRH	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 832Ah	RSCAN	Global Status Register	GSTS	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 832Ch	RSCAN	Global Error Flag Register	GERFLL	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 832Eh	RSCAN	Timestamp Register	GTSC	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8330h	RSCAN	Receive Rule Number Configuration Register	GAFLCFG	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8332h	RSCAN	Receive Buffer Number Configuration Register	RMNB	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8334h	RSCAN	Receive Buffer Receive Complete Flag Register	RMND0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8338h	RSCAN	Receive FIFO Control Register 0	RFCC0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 833Ah	RSCAN	Receive FIFO Control Register 1	RFCC1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8340h	RSCAN	Receive FIFO Status Register 0	RFSTS0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8342h	RSCAN	Receive FIFO Status Register 1	RFSTS1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8348h	RSCAN	Receive FIFO Pointer Control Register 0	RFPCTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 834Ah	RSCAN	Receive FIFO Pointer Control Register 1	RFPCTR1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8350h	RSCAN0	Transmit/Receive FIFO Control Register 0L	CFCCLO	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8352h	RSCAN0	Transmit/Receive FIFO Control Register 0H	CFCH0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8358h	RSCAN0	Transmit/Receive FIFO Status Register 0	CFSTS0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 835Ch	RSCAN0	Transmit/Receive FIFO Pointer Control Register 0	CFPCTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8360h	RSCAN	Receive FIFO Message Lost Status Register	RFMSTS	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8361h	RSCAN0	Transmit/Receive FIFO Message Lost Status Register	CFMSTS	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8362h	RSCAN	Receive FIFO Interrupt Status Register	RFISTS	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8363h	RSCAN	Transmit/Receive FIFO Receive Interrupt Status Register	CFISTS	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8364h	RSCAN0	Transmit Buffer Control Register 0	TMC0	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8365h	RSCAN0	Transmit Buffer Control Register 1	TMC1	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8366h	RSCAN0	Transmit Buffer Control Register 2	TMC2	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8367h	RSCAN0	Transmit Buffer Control Register 3	TMC3	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 836Ch	RSCAN0	Transmit Buffer Status Register 0	TMSTS0	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1	TMSTS1	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2	TMSTS2	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3	TMSTS3	8	8	2 or 3 PCLKB	2 ICLK	section 36.
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register	TMTRSTS	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register	TMTCTS	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register	TMTASTS	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register	TMIEC	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 837Ch	RSCAN0	Transmit History Buffer Control Register	THLCC0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8380h	RSCAN0	Transmit History Buffer Status Register	THLSTS0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register	THLPCTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8388h	RSCAN	Global Transmit Interrupt Status Register	GTINTSTS	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 838Ah	RSCAN	Global RAM Window Control Register	GRWCR	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 838Ch	RSCAN	Global Test Configuration Register	GTSTCFG	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 838Eh	RSCAN	Global Test Control Register	GTSTCTRL	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8394h	RSCAN	Global Test Protection Unlock Register	GLOCKK	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL	GAFLIDLO	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A0h	RSCAN	Receive Buffer Register 0AL	RMIDLO	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH	GAFLIDHO	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A2h	RSCAN	Receive Buffer Register 0AH	RMIDHO	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL	GAFLML0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A4h	RSCAN	Receive Buffer Register 0BL	RMTS0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH	GAFLMH0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A6h	RSCAN	Receive Buffer Register 0BH	RMPTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL	GAFLPL0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83A8h	RSCAN	Receive Buffer Register 0CL	RMDFO0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH	GAFLPH0	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (23/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 83AAh	RSCAN	Receive Buffer Register 0CH	RMDF10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL	GAFLIDL1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83ACH	RSCAN	Receive Buffer Register 0DL	RMDF20	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH	GAFLIDH1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83AEh	RSCAN	Receive Buffer Register 0DH	RMDF30	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL	GAFLML1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B0h	RSCAN	Receive Buffer Register 1AL	RMIDL1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH	GAFLMH1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B2h	RSCAN	Receive Buffer Register 1AH	RMIDH1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL	GAFLPL1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B4h	RSCAN	Receive Buffer Register 1BL	RMTS1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH	GAFLPH1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B6h	RSCAN	Receive Buffer Register 1BH	RMPTR1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL	GAFLIDL2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83B8h	RSCAN	Receive Buffer Register 1CL	RMDF01	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH	GAFLIDH2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83BAh	RSCAN	Receive Buffer Register 1CH	RMDF11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL	GAFLML2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83BCh	RSCAN	Receive Buffer Register 1DL	RMDF21	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH	GAFLMH2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83BEh	RSCAN	Receive Buffer Register 1DH	RMDF31	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL	GAFLPL2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C0h	RSCAN	Receive Buffer Register 2AL	RMIDL2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH	GAFLPH2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C2h	RSCAN	Receive Buffer Register 2AH	RMIDH2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL	GAFLIDL3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C4h	RSCAN	Receive Buffer Register 2BL	RMTS2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C6h	RSCAN	Receive Rule Entry Register 3AH	GAFLIDH3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C6h	RSCAN	Receive Buffer Register 2BH	RMPTR2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C8h	RSCAN	Receive Rule Entry Register 3BL	GAFLML3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83C8h	RSCAN	Receive Buffer Register 2CL	RMDF02	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83CAh	RSCAN	Receive Rule Entry Register 3BH	GAFLMH3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83CAh	RSCAN	Receive Buffer Register 2CH	RMDF12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83CCh	RSCAN	Receive Rule Entry Register 3CL	GAFLPL3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83CCh	RSCAN	Receive Buffer Register 2DL	RMDF22	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83CEh	RSCAN	Receive Rule Entry Register 3CH	GAFLPH3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83CEh	RSCAN	Receive Buffer Register 2DH	RMDF32	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D0h	RSCAN	Receive Rule Entry Register 4AL	GAFLIDL4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D0h	RSCAN	Receive Buffer Register 3AL	RMIDL3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D2h	RSCAN	Receive Rule Entry Register 4AH	GAFLIDH4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D2h	RSCAN	Receive Buffer Register 3AH	RMIDH3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D4h	RSCAN	Receive Rule Entry Register 4BL	GAFLML4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D4h	RSCAN	Receive Buffer Register 3BL	RMTS3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D6h	RSCAN	Receive Rule Entry Register 4BH	GAFLMH4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D6h	RSCAN	Receive Buffer Register 3BH	RMPTR3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D8h	RSCAN	Receive Rule Entry Register 4CL	GAFLPL4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83D8h	RSCAN	Receive Buffer Register 3CL	RMDF03	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83DAh	RSCAN	Receive Rule Entry Register 4CH	GAFLPH4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83DAh	RSCAN	Receive Buffer Register 3CH	RMDF13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83DCh	RSCAN	Receive Rule Entry Register 5AL	GAFLIDL5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83DCh	RSCAN	Receive Buffer Register 3DL	RMDF23	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83DEh	RSCAN	Receive Rule Entry Register 5AH	GAFLIDH5	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (24/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 83DEh	RSCAN	Receive Buffer Register 3DH	RMDF33	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E0h	RSCAN	Receive Rule Entry Register 5BL	GAFLML5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E0h	RSCAN	Receive Buffer Register 4AL	RMIDL4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E2h	RSCAN	Receive Rule Entry Register 5BH	GAFLMH5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E2h	RSCAN	Receive Buffer Register 4AH	RMIDH4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E4h	RSCAN	Receive Rule Entry Register 5CL	GAFLPL5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E4h	RSCAN	Receive Buffer Register 4BL	RMTS4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E6h	RSCAN	Receive Rule Entry Register 5CH	GAFLPH5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E6h	RSCAN	Receive Buffer Register 4BH	RMPTR4	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E8h	RSCAN	Receive Rule Entry Register 6AL	GAFLIDL6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83E8h	RSCAN	Receive Buffer Register 4CL	RMDF04	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83EAh	RSCAN	Receive Rule Entry Register 6AH	GAFLIDH6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83EAh	RSCAN	Receive Buffer Register 4CH	RMDF14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83ECh	RSCAN	Receive Rule Entry Register 6BL	GAFLML6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83ECh	RSCAN	Receive Buffer Register 4DL	RMDF24	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83EEh	RSCAN	Receive Rule Entry Register 6BH	GAFLMH6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83EEh	RSCAN	Receive Buffer Register 4DH	RMDF34	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F0h	RSCAN	Receive Rule Entry Register 6CL	GAFLPL6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F0h	RSCAN	Receive Buffer Register 5AL	RMIDL5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F2h	RSCAN	Receive Rule Entry Register 6CH	GAFLPH6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F2h	RSCAN	Receive Buffer Register 5AH	RMIDH5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F4h	RSCAN	Receive Rule Entry Register 7AL	GAFLIDL7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F4h	RSCAN	Receive Buffer Register 5BL	RMTS5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F6h	RSCAN	Receive Rule Entry Register 7AH	GAFLIDH7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F6h	RSCAN	Receive Buffer Register 5BH	RMPTR5	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F8h	RSCAN	Receive Rule Entry Register 7BL	GAFLML7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83F8h	RSCAN	Receive Buffer Register 5CL	RMDF05	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83FAh	RSCAN	Receive Rule Entry Register 7BH	GAFLMH7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83FAh	RSCAN	Receive Buffer Register 5CH	RMDF15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83FCh	RSCAN	Receive Rule Entry Register 7CL	GAFLPL7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83FCh	RSCAN	Receive Buffer Register 5DL	RMDF25	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83FEh	RSCAN	Receive Rule Entry Register 7CH	GAFLPH7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 83FEh	RSCAN	Receive Buffer Register 5DH	RMDF35	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8400h	RSCAN	Receive Rule Entry Register 8AL	GAFLIDL8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8400h	RSCAN	Receive Buffer Register 6AL	RMIDL6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8402h	RSCAN	Receive Rule Entry Register 8AH	GAFLIDH8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8402h	RSCAN	Receive Buffer Register 6AH	RMIDH6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8404h	RSCAN	Receive Rule Entry Register 8BL	GAFLML8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8404h	RSCAN	Receive Buffer Register 6BL	RMTS6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8406h	RSCAN	Receive Rule Entry Register 8BH	GAFLMH8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8406h	RSCAN	Receive Buffer Register 6BH	RMPTR6	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8408h	RSCAN	Receive Rule Entry Register 8CL	GAFLPL8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8408h	RSCAN	Receive Buffer Register 6CL	RMDF06	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 840Ah	RSCAN	Receive Rule Entry Register 8CH	GAFLPH8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 840Ah	RSCAN	Receive Buffer Register 6CH	RMDF16	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 840Ch	RSCAN	Receive Rule Entry Register 9AL	GAFLIDL9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 840Ch	RSCAN	Receive Buffer Register 6DL	RMDF26	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 840Eh	RSCAN	Receive Rule Entry Register 9AH	GAFLIDH9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 840Eh	RSCAN	Receive Buffer Register 6DH	RMDF36	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8410h	RSCAN	Receive Rule Entry Register 9BL	GAFLML9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8410h	RSCAN	Receive Buffer Register 7AL	RMIDL7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8412h	RSCAN	Receive Rule Entry Register 9BH	GAFLMH9	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (25/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 8412h	RSCAN	Receive Buffer Register 7AH	RMIDH7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8414h	RSCAN	Receive Rule Entry Register 9CL	GAFLPL9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8414h	RSCAN	Receive Buffer Register 7BL	RMTS7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8416h	RSCAN	Receive Rule Entry Register 9CH	GAFLPH9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8416h	RSCAN	Receive Buffer Register 7BH	RMPTR7	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8418h	RSCAN	Receive Rule Entry Register 10AL	GAFLIDL10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8418h	RSCAN	Receive Buffer Register 7CL	RMDF07	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 841Ah	RSCAN	Receive Rule Entry Register 10AH	GAFLIDH10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 841Ah	RSCAN	Receive Buffer Register 7CH	RMDF17	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 841Ch	RSCAN	Receive Rule Entry Register 10BL	GAFLML10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 841Ch	RSCAN	Receive Buffer Register 7DL	RMDF27	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 841Eh	RSCAN	Receive Rule Entry Register 10BH	GAFLMH10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 841Eh	RSCAN	Receive Buffer Register 7DH	RMDF37	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8420h	RSCAN	Receive Rule Entry Register 10CL	GAFLPL10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8420h	RSCAN	Receive Buffer Register 8AL	RMIDL8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8422h	RSCAN	Receive Rule Entry Register 10CH	GAFLPH10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8422h	RSCAN	Receive Buffer Register 8AH	RMIDH8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8424h	RSCAN	Receive Rule Entry Register 11AL	GAFLIDL11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8424h	RSCAN	Receive Buffer Register 8BL	RMTS8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8426h	RSCAN	Receive Rule Entry Register 11AH	GAFLIDH11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8426h	RSCAN	Receive Buffer Register 8BH	RMPTR8	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8428h	RSCAN	Receive Rule Entry Register 11BL	GAFLML11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8428h	RSCAN	Receive Buffer Register 8CL	RMDF08	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 842Ah	RSCAN	Receive Rule Entry Register 11BH	GAFLMH11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 842Ah	RSCAN	Receive Buffer Register 8CH	RMDF18	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 842Ch	RSCAN	Receive Rule Entry Register 11CL	GAFLPL11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 842Ch	RSCAN	Receive Buffer Register 8DL	RMDF28	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH	GAFLPH11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 842Eh	RSCAN	Receive Buffer Register 8DH	RMDF38	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8430h	RSCAN	Receive Rule Entry Register 12AL	GAFLIDL12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8430h	RSCAN	Receive Buffer Register 9AL	RMIDL9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8432h	RSCAN	Receive Rule Entry Register 12AH	GAFLIDH12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8432h	RSCAN	Receive Buffer Register 9AH	RMIDH9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8434h	RSCAN	Receive Rule Entry Register 12BL	GAFLML12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8434h	RSCAN	Receive Buffer Register 9BL	RMTS9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8436h	RSCAN	Receive Rule Entry Register 12BH	GAFLMH12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8436h	RSCAN	Receive Buffer Register 9BH	RMPTR9	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8438h	RSCAN	Receive Rule Entry Register 12CL	GAFLPL12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8438h	RSCAN	Receive Buffer Register 9CL	RMDF09	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH	GAFLPH12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 843Ah	RSCAN	Receive Buffer Register 9CH	RMDF19	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL	GAFLIDL13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 843Ch	RSCAN	Receive Buffer Register 9DL	RMDF29	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH	GAFLIDH13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 843Eh	RSCAN	Receive Buffer Register 9DH	RMDF39	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8440h	RSCAN	Receive Rule Entry Register 13BL	GAFLML13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8440h	RSCAN	Receive Buffer Register 10AL	RMIDL10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8442h	RSCAN	Receive Rule Entry Register 13BH	GAFLMH13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8442h	RSCAN	Receive Buffer Register 10AH	RMIDH10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8444h	RSCAN	Receive Rule Entry Register 13CL	GAFLPL13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8444h	RSCAN	Receive Buffer Register 10BL	RMTS10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8446h	RSCAN	Receive Rule Entry Register 13CH	GAFLPH13	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (26/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 8446h	RSCAN	Receive Buffer Register 10BH	RMPTR10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8448h	RSCAN	Receive Rule Entry Register 14AL	GAFLIDL14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8448h	RSCAN	Receive Buffer Register 10CL	RMDF010	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH	GAFLIDH14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 844Ah	RSCAN	Receive Buffer Register 10CH	RMDF110	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL	GAFLML14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 844Ch	RSCAN	Receive Buffer Register 10DL	RMDF210	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH	GAFLMH14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 844Eh	RSCAN	Receive Buffer Register 10DH	RMDF310	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8450h	RSCAN	Receive Rule Entry Register 14CL	GAFLPL14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8450h	RSCAN	Receive Buffer Register 11AL	RMIDL11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8452h	RSCAN	Receive Rule Entry Register 14CH	GAFLPH14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8452h	RSCAN	Receive Buffer Register 11AH	RMIDH11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8454h	RSCAN	Receive Rule Entry Register 15AL	GAFLIDL15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8454h	RSCAN	Receive Buffer Register 11BL	RMTS11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8456h	RSCAN	Receive Rule Entry Register 15AH	GAFLIDH15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8456h	RSCAN	Receive Buffer Register 11BH	RMPTR11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8458h	RSCAN	Receive Rule Entry Register 15BL	GAFLML15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8458h	RSCAN	Receive Buffer Register 11CL	RMDF011	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 845Ah	RSCAN	Receive Rule Entry Register 15BH	GAFLMH15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 845Ah	RSCAN	Receive Buffer Register 11CH	RMDF111	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 845Ch	RSCAN	Receive Rule Entry Register 15CL	GAFLPL15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 845Ch	RSCAN	Receive Buffer Register 11DL	RMDF211	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 845Eh	RSCAN	Receive Rule Entry Register 15CH	GAFLPH15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 845Eh	RSCAN	Receive Buffer Register 11DH	RMDF311	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8460h	RSCAN	Receive Buffer Register 12AL	RMIDL12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8462h	RSCAN	Receive Buffer Register 12AH	RMIDH12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8464h	RSCAN	Receive Buffer Register 12BL	RMTS12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8466h	RSCAN	Receive Buffer Register 12BH	RMPTR12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8468h	RSCAN	Receive Buffer Register 12CL	RMDF012	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 846Ah	RSCAN	Receive Buffer Register 12CH	RMDF112	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 846Ch	RSCAN	Receive Buffer Register 12DL	RMDF212	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 846Eh	RSCAN	Receive Buffer Register 12DH	RMDF312	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8470h	RSCAN	Receive Buffer Register 13AL	RMIDL13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8472h	RSCAN	Receive Buffer Register 13AH	RMIDH13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8474h	RSCAN	Receive Buffer Register 13BL	RMTS13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8476h	RSCAN	Receive Buffer Register 13BH	RMPTR13	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8478h	RSCAN	Receive Buffer Register 13CL	RMDF013	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 847Ah	RSCAN	Receive Buffer Register 13CH	RMDF113	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 847Ch	RSCAN	Receive Buffer Register 13DL	RMDF213	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 847Eh	RSCAN	Receive Buffer Register 13DH	RMDF313	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8480h	RSCAN	Receive Buffer Register 14AL	RMIDL14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8482h	RSCAN	Receive Buffer Register 14AH	RMIDH14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8484h	RSCAN	Receive Buffer Register 14BL	RMTS14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8486h	RSCAN	Receive Buffer Register 14BH	RMPTR14	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8488h	RSCAN	Receive Buffer Register 14CL	RMDF014	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 848Ah	RSCAN	Receive Buffer Register 14CH	RMDF114	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 848Ch	RSCAN	Receive Buffer Register 14DL	RMDF214	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 848Eh	RSCAN	Receive Buffer Register 14DH	RMDF314	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8490h	RSCAN	Receive Buffer Register 15AL	RMIDL15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8492h	RSCAN	Receive Buffer Register 15AH	RMIDH15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8494h	RSCAN	Receive Buffer Register 15BL	RMTS15	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (27/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK ≥ PCLK	ICLK < PCLK	
000A 8496h	RSCAN	Receive Buffer Register 15BH	RMPTR15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8498h	RSCAN	Receive Buffer Register 15CL	RMDF015	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 849Ah	RSCAN	Receive Buffer Register 15CH	RMDF115	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 849Ch	RSCAN	Receive Buffer Register 15DL	RMDF215	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 849Eh	RSCAN	Receive Buffer Register 15DH	RMDF315	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8580h to 000A 859Fh	RSCAN	RAM Test Register 0 to RAM Test Register 15	RPGACC0 to RPGACC15	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A0h	RSCAN	Receive FIFO Access Register 0AL	RFIDL0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A0h	RSCAN	RAM Test Register 16	RPGACC16	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A2h	RSCAN	Receive FIFO Access Register 0AH	RFIDH0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A2h	RSCAN	RAM Test Register 17	RPGACC17	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A4h	RSCAN	Receive FIFO Access Register 0BL	RFTS0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A4h	RSCAN	RAM Test Register 18	RPGACC18	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A6h	RSCAN	Receive FIFO Access Register 0BH	RFPTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A6h	RSCAN	RAM Test Register 19	RPGACC19	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A8h	RSCAN	Receive FIFO Access Register 0CL	RFDF00	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85A8h	RSCAN	RAM Test Register 20	RPGACC20	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85AAh	RSCAN	Receive FIFO Access Register 0CH	RFDF10	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85AAh	RSCAN	RAM Test Register 21	RPGACC21	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85ACh	RSCAN	Receive FIFO Access Register 0DL	RFDF20	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85ACh	RSCAN	RAM Test Register 22	RPGACC22	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85AEh	RSCAN	Receive FIFO Access Register 0DH	RFDF30	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85AEh	RSCAN	RAM Test Register 23	RPGACC23	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B0h	RSCAN	Receive FIFO Access Register 1AL	RFIDL1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B0h	RSCAN	RAM Test Register 24	RPGACC24	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B2h	RSCAN	Receive FIFO Access Register 1AH	RFIDH1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B2h	RSCAN	RAM Test Register 25	RPGACC25	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B4h	RSCAN	Receive FIFO Access Register 1BL	RFTS1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B4h	RSCAN	RAM Test Register 26	RPGACC26	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B6h	RSCAN	Receive FIFO Access Register 1BH	RFPTR1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B6h	RSCAN	RAM Test Register 27	RPGACC27	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B8h	RSCAN	Receive FIFO Access Register 1CL	RFDF01	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85B8h	RSCAN	RAM Test Register 28	RPGACC28	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85BAh	RSCAN	Receive FIFO Access Register 1CH	RFDF11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85BAh	RSCAN	RAM Test Register 29	RPGACC29	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85BCh	RSCAN	Receive FIFO Access Register 1DL	RFDF21	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85BCh	RSCAN	RAM Test Register 30	RPGACC30	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85BEh	RSCAN	Receive FIFO Access Register 1DH	RFDF31	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85BEh	RSCAN	RAM Test Register 31	RPGACC31	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85C0h to 000A 85DEh	RSCAN	RAM Test Register 32 to RAM Test Register 47	RPGACC32 to RPGACC47	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E0h	RSCAN0	Transmit/Receive FIFO Access Register 0AL	CFIDL0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E0h	RSCAN	RAM Test Register 48	RPGACC48	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E2h	RSCAN0	Transmit/Receive FIFO Access Register 0AH	CFIDH0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E2h	RSCAN	RAM Test Register 49	RPGACC49	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E4h	RSCAN0	Transmit/Receive FIFO Access Register 0BL	CFTS0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E4h	RSCAN	RAM Test Register 50	RPGACC50	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E6h	RSCAN0	Transmit/Receive FIFO Access Register 0BH	CFPTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E6h	RSCAN	RAM Test Register 51	RPGACC51	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E8h	RSCAN0	Transmit/Receive FIFO Access Register 0CL	CFDF00	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85E8h	RSCAN	RAM Test Register 52	RPGACC52	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85EAh	RSCAN0	Transmit/Receive FIFO Access Register 0CH	CFDF10	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (28/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 85EAh	RSCAN	RAM Test Register 53	RPGACC53	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85ECh	RSCAN0	Transmit/Receive FIFO Access Register 0DL	CFDF20	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85ECh	RSCAN	RAM Test Register 54	RPGACC54	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85EEh	RSCAN0	Transmit/Receive FIFO Access Register 0DH	CFDF30	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85EEh	RSCAN	RAM Test Register 55	RPGACC55	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 85F0h to 000A 85FEh	RSCAN	RAM Test Register 56 to RAM Test Register 63	RPGACC56 to RPGACC63	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8600h	RSCAN0	Transmit Buffer Register 0AL	TMIDL0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8600h	RSCAN	RAM Test Register 64	RPGACC64	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8602h	RSCAN0	Transmit Buffer Register 0AH	TMIDH0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8602h	RSCAN	RAM Test Register 65	RPGACC65	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8604h	RSCAN	RAM Test Register 66	RPGACC66	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8606h	RSCAN0	Transmit Buffer Register 0BH	TMPTR0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8606h	RSCAN	RAM Test Register 67	RPGACC67	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8608h	RSCAN0	Transmit Buffer Register 0CL	TMDFO0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8608h	RSCAN	RAM Test Register 68	RPGACC68	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 860Ah	RSCAN0	Transmit Buffer Register 0CH	TMDFO1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 860Ah	RSCAN	RAM Test Register 69	RPGACC69	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 860Ch	RSCAN0	Transmit Buffer Register 0DL	TMDFO2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 860Ch	RSCAN	RAM Test Register 70	RPGACC70	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 860Eh	RSCAN0	Transmit Buffer Register 0DH	TMDFO3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 860Eh	RSCAN	RAM Test Register 71	RPGACC71	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8610h	RSCAN0	Transmit Buffer Register 1AL	TMIDL1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8610h	RSCAN	RAM Test Register 72	RPGACC72	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8612h	RSCAN0	Transmit Buffer Register 1AH	TMIDH1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8612h	RSCAN	RAM Test Register 73	RPGACC73	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8614h	RSCAN	RAM Test Register 74	RPGACC74	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8616h	RSCAN0	Transmit Buffer Register 1BH	TMPTR1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8616h	RSCAN	RAM Test Register 75	RPGACC75	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8618h	RSCAN0	Transmit Buffer Register 1CL	TMDFO1	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8618h	RSCAN	RAM Test Register 76	RPGACC76	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 861Ah	RSCAN0	Transmit Buffer Register 1CH	TMDFO11	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 861Ah	RSCAN	RAM Test Register 77	RPGACC77	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 861Ch	RSCAN0	Transmit Buffer Register 1DL	TMDFO21	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 861Ch	RSCAN	RAM Test Register 78	RPGACC78	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 861Eh	RSCAN0	Transmit Buffer Register 1DH	TMDFO31	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 861Eh	RSCAN	RAM Test Register 79	RPGACC79	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8620h	RSCAN0	Transmit Buffer Register 2AL	TMIDL2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8620h	RSCAN	RAM Test Register 80	RPGACC80	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8622h	RSCAN0	Transmit Buffer Register 2AH	TMIDH2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8622h	RSCAN	RAM Test Register 81	RPGACC81	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8624h	RSCAN	RAM Test Register 82	RPGACC82	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8626h	RSCAN0	Transmit Buffer Register 2BH	TMPTR2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8626h	RSCAN	RAM Test Register 83	RPGACC83	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8628h	RSCAN0	Transmit Buffer Register 2CL	TMDFO2	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8628h	RSCAN	RAM Test Register 84	RPGACC84	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 862Ah	RSCAN0	Transmit Buffer Register 2CH	TMDFO12	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 862Ah	RSCAN	RAM Test Register 85	RPGACC85	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 862Ch	RSCAN0	Transmit Buffer Register 2DL	TMDFO22	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 862Ch	RSCAN	RAM Test Register 86	RPGACC86	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 862Eh	RSCAN0	Transmit Buffer Register 2DH	TMDFO32	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 862Eh	RSCAN	RAM Test Register 87	RPGACC87	16	16	2 or 3 PCLKB	2 ICLK	section 36.

Table 5.1 List of I/O Registers (Address Order) (29/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000A 8630h	RSCAN0	Transmit Buffer Register 3AL	TMIDL3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8630h	RSCAN	RAM Test Register 88	RPGACC88	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8632h	RSCAN0	Transmit Buffer Register 3AH	TMIDH3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8632h	RSCAN	RAM Test Register 89	RPGACC89	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8634h	RSCAN	RAM Test Register 90	RPGACC90	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8636h	RSCAN0	Transmit Buffer Register 3BH	TMPTR3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8636h	RSCAN	RAM Test Register 91	RPGACC91	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8638h	RSCAN0	Transmit Buffer Register 3CL	TMDFO3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8638h	RSCAN	RAM Test Register 92	RPGACC92	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 863Ah	RSCAN0	Transmit Buffer Register 3CH	TMDFI3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 863Ah	RSCAN	RAM Test Register 93	RPGACC93	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 863Ch	RSCAN0	Transmit Buffer Register 3DL	TMDFI3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 863Ch	RSCAN	RAM Test Register 94	RPGACC94	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 863Eh	RSCAN0	Transmit Buffer Register 3DH	TMDFI3	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 863Eh	RSCAN	RAM Test Register 95	RPGACC95	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8640h to 000A 867Eh	RSCAN	RAM Test Register 96 to RAM Test Register 127	RPGACC96 to RPGACC127	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000A 8680h	RSCAN0	Transmit History Buffer Access Register	THLACC0	16	16	2 or 3 PCLKB	2 ICLK	section 36.
000D 0A00h	MTU3	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A01h	MTU4	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A02h	MTU3	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A03h	MTU4	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A04h	MTU3	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A05h	MTU3	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A06h	MTU4	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A07h	MTU4	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A08h	MTU3	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A09h	MTU4	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A0Ah	MTU	Timer Output Master Enable Register	TOER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A0Dh	MTU	Timer Gate Control Register	TGCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A0Eh	MTU	Timer Output Control Register 1	TOCR1	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A0Fh	MTU	Timer Output Control Register 2	TOCR2	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A10h	MTU3	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A12h	MTU4	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A14h	MTU	Timer Cycle Data Register	TCDR	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A16h	MTU	Timer Dead Time Data Register	TDDR	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A18h	MTU3	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A1Ah	MTU3	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A1Ch	MTU4	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A1Eh	MTU4	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A20h	MTU	Timer Subcounter	TCNTS	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A22h	MTU	Timer Cycle Buffer Register	TCBR	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A24h	MTU3	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A26h	MTU3	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A28h	MTU4	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A2Ah	MTU4	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A2Ch	MTU3	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A2Dh	MTU4	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A30h	MTU	Timer Interrupt Skipping Set Register	TITCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A31h	MTU	Timer Interrupt Skipping Counter	TITCNT	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A32h	MTU	Timer Buffer Transfer Set Register	TBTER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A34h	MTU	Timer Dead Time Enable Register	TDER	8	8	2 or 3 PCLKA	2 ICLK	section 23.

Table 5.1 List of I/O Registers (Address Order) (30/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
000D 0A36h	MTU	Timer Output Level Buffer Register	TOLBR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A38h	MTU3	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A39h	MTU4	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A40h	MTU4	Timer A/D Converter Start Request Control Register	TADCR	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A44h	MTU4	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A46h	MTU4	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A48h	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A4Ah	MTU4	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A60h	MTU	Timer Waveform Control Register	TWCR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A80h	MTU	Timer Start Register	TSTR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A81h	MTU	Timer Synchronous Register	TSYR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A84h	MTU	Timer Read/Write Enable Register	TRWER	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A90h	MTU0	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A91h	MTU1	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A92h	MTU2	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A93h	MTU3	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0A94h	MTU4	Noise Filter Control Register	NFCR	8	8, 16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B00h	MTU0	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B01h	MTU0	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B02h	MTU0	Timer I/O Control Register H	TIORH	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B03h	MTU0	Timer I/O Control Register L	TIORL	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B04h	MTU0	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B05h	MTU0	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B06h	MTU0	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B08h	MTU0	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B0Ah	MTU0	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B0Ch	MTU0	Timer General Register C	TGRC	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B0Eh	MTU0	Timer General Register D	TGRD	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B20h	MTU0	Timer General Register E	TGRE	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B22h	MTU0	Timer General Register F	TGRF	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B24h	MTU0	Timer Interrupt Enable Register 2	TIER2	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B26h	MTU0	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B80h	MTU1	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B81h	MTU1	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B82h	MTU1	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B84h	MTU1	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B85h	MTU1	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B86h	MTU1	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B88h	MTU1	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B8Ah	MTU1	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0B90h	MTU1	Timer Input Capture Control Register	TICCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C00h	MTU2	Timer Control Register	TCR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C01h	MTU2	Timer Mode Register	TMDR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C02h	MTU2	Timer I/O Control Register	TIOR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C04h	MTU2	Timer Interrupt Enable Register	TIER	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C05h	MTU2	Timer Status Register	TSR	8	8	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C06h	MTU2	Timer Counter	TCNT	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C08h	MTU2	Timer General Register A	TGRA	16	16	2 or 3 PCLKA	2 ICLK	section 23.
000D 0C0Ah	MTU2	Timer General Register B	TGRB	16	16	2 or 3 PCLKA	2 ICLK	section 23.
007F C090h	FLASH	E2 DataFlash Control Register	DFLCTL	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C0ACh	TEMPSA	Temperature Sensor Calibration Data Register L	TSCDRL	8	8	2 or 3 PCLKA	2 ICLK	section 46.

Table 5.1 List of I/O Registers (Address Order) (31/31)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Reference Section
						ICLK $\geq$ PCLK	ICLK $<$ PCLK	
007F C0ADh	TEMPSA	Temperature Sensor Calibration Data Register H	TSCDRH	8	8	2 or 3 PCLKA	2 ICLK	section 46.
007F C100h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C104h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C108h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C110h	FLASH	Flash Processing Start Address Register H	FSARH	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C114h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C118h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C120h	FLASH	Flash Processing End Address Register H	FEARH	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C124h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C12Ch	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C130h	FLASH	Flash Write Buffer Register 0	FWB0	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C138h	FLASH	Flash Write Buffer Register 1	FWB1	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C140h	FLASH	Flash Write Buffer Register 2	FWB2	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C144h	FLASH	Flash Write Buffer Register 3	FWB3	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C180h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C184h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C1C0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C1C8h	FLASH	Flash Access Window Start Address Monitor Register	FAWSMR	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C1D0h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C1D8h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C1DCh	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C1E0h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK	2 ICLK	section 50.
007F C1E8h	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C1F0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK	2 ICLK	section 50.
007F C350h	FLASHCON ST	Unique ID Register 0	UIDR0	32	32	2 or 3 FCLK	2 ICLK	section 50.
007F C354h	FLASHCON ST	Unique ID Register 1	UIDR1	32	32	2 or 3 FCLK	2 ICLK	section 50.
007F C358h	FLASHCON ST	Unique ID Register 2	UIDR2	32	32	2 or 3 FCLK	2 ICLK	section 50.
007F C35Ch	FLASHCON ST	Unique ID Register 3	UIDR3	32	32	2 or 3 FCLK	2 ICLK	section 50.
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK	2 ICLK	section 50.

Note 1. Odd addresses cannot be accessed in 16-bit units. Table 26.4 lists register allocation for 16-bit access.

Note 2. When the register is accessed while the USB is operating, a delay may be generated in accessing.

6. Resets

6.1 Overview

The following resets are implemented: RES# pin reset, power-on reset, voltage monitoring 0 reset, voltage monitoring 1 reset, independent watchdog timer reset, watchdog timer reset, and software reset.

Table 6.1 lists the reset names and sources.

Table 6.1 Reset Names and Sources

Reset Name	Source
RES# pin reset	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)* ¹
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)* ¹
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)* ¹
Independent watchdog timer reset	The independent watchdog timer underflows, or a refresh error occurs.
Watchdog timer reset	The watchdog timer underflows, or a refresh error occurs.
Software reset	Register setting

Note 1. For the voltages to be monitored (VPOR, Vdet0, and Vdet1), see section 8, Voltage Detection Circuit (LVDAb) and section 51, Electrical Characteristics.

The internal state and pins are initialized by a reset.

Table 6.2 lists the reset targets to be initialized.

Table 6.2 Targets Initialized by Each Reset Source

Target to be Initialized	Reset Source						
	RES# Pin Reset	Power-On Reset	Voltage Monitoring 0 Reset	Independent Watchdog Timer Reset	Watchdog Timer Reset	Voltage Monitoring 1 Reset	Software Reset
The power-on reset detect flag (RSTSR0.PORF)	✓	—	—	—	—	—	—
Register related to the cold start/warm start determination flag (RSTSR1.CWSF)	—*1	✓	—	—	—	—	—
Voltage monitoring 0 reset detect flag (RSTSR0.LVD0RF)	✓	✓	—	—	—	—	—
Registers related to the battery backup function (VBATTCR, VBATTSR, VBTLDICR)	✓	✓	—	—	—	—	—
The independent watchdog timer reset detect flag (RSTSR2.IWDTRF)	✓	✓	✓	—	—	—	—
Registers related to the independent watchdog timer (IWDTRR, IWDTCR, IWDTSR, IWDTRCR, IWDTCSTPR, ILOCOCR)	✓	✓	✓	—	—	—	—
The watchdog timer reset detect flag (RSTSR2.WDTRF)	✓	✓	✓	✓	—	—	—
Registers related to the watchdog timer (WDTRR, WDTCSR, WDTSR, WDTRCR)	✓	✓	✓	✓	—	—	—
The voltage monitoring 1 reset detect flag (RSTSR0.LVD1RF)	✓	✓	✓	✓	✓	—	—
Registers related to voltage monitor function 1 (LVD1CR0, LVCMPCCR.LVD1E, LVDLVLRLVD1LVL[3:0])	✓	✓	✓	✓	✓	—	—
(LVD1CR1, LVD1SR)	✓	✓	✓	✓	✓	—	—
The software reset detect flag (RSTSR2.SWRF)	✓	✓	✓	✓	✓	✓	—
Register related to the realtime clock*2	—	—	—	—	—	—	—
Registers other than the above, CPU, and internal state	✓	✓	✓	✓	✓	✓	✓

✓: Targets to be initialized, —: No change occurs.

Note 1. Initialized at a power-on.

Note 2. Some control bits (RCR1.CIE, RCR1.RTCOS, RCR2.RTCOE, ADJ30, and RESET) are initialized by all types of reset. For details on the target bits, refer to section 28, Realtime Clock (RTCe).

When a reset is canceled, the reset exception handling starts. For the reset exception handling, see section 14, Exception Handling.

Table 6.3 lists the pin related to the reset.

Table 6.3 Pin Related to Reset

Pin Name	I/O	Function
RES#	Input	Reset pin

6.2 Register Descriptions

6.2.1 Reset Status Register 0 (RSTSR0)

Address(es): 0008 C290h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	LVD1R F	LVD0R F	PORF
Value after reset:	0	0	0	0	0*1	0*1	0*1

Bit	Symbol	Bit Name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected. 1: Power-on reset detected.	R(W) *2
b1	LVD0RF	Voltage Monitoring 0 Reset Detect Flag	0: Voltage monitoring 0 reset not detected. 1: Voltage monitoring 0 reset detected.	R(W) *2
b2	LVD1RF	Voltage Monitoring 1 Reset Detect Flag	0: Voltage monitoring 1 reset not detected. 1: Voltage monitoring 1 reset detected.	R(W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.

Note 2. Only 0 can be written to clear the flag.

PORF Flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset has occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When resets shown in Table 6.2 occur.
- When PORF is read as 1 and then 0 is written to PORF.

LVD0RF Flag (Voltage Monitoring 0 Reset Detect Flag)

The LVD0RF flag indicates that VCC voltage has fallen below Vdet0.

[Setting condition]

- When Vdet0-level VCC voltage is detected.

[Clearing conditions]

- When resets listed in Table 6.2 occur.
- When LVD0RF is read as 1 and then 0 is written to LVD0RF.

LVD1RF Flag (Voltage Monitoring 1 Reset Detect Flag)

The LVD1RF flag indicates that VCC voltage has fallen below Vdet1.

[Setting condition]

- When Vdet1-level VCC voltage is detected.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When LVD1RF is read as 1 and then 0 is written to LVD1RF.

6.2.2 Reset Status Register 1 (RSTSR1)

Address(es): 0008 C291h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	CWSF
0	0	0	0	0	0	0	0/1*1

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start	R/(W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.

Note 2. Only 1 can be written to set the flag.

RSTSR1 determines whether a power-on reset has caused the reset processing (cold start) or a reset signal input during operation has caused the reset processing (warm start).

CWSF Flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing: cold start or warm start.

The CWSF flag is initialized at a power-on.

[Setting condition]

- When 1 is written through programming; it is not set to 0 even when 0 is written.

[Clearing condition]

- When a reset listed in Table 6.2 occurs.

6.2.3 Reset Status Register 2 (RSTSR2)

Address(es): 0008 00C0h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	SWRF	WDTRF	IWDTRF
0	0	0	0	0	0*1	0*1	0*1

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent watchdog timer reset not detected. 1: Independent watchdog timer reset detected.	R(W) *2
b1	WDTRF	Watchdog Timer Reset Detect Flag	0: Watchdog timer reset not detected. 1: Watchdog timer reset detected.	R(W) *2
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected. 1: Software reset detected.	R(W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.

Note 2. Only 0 can be written to clear the flag.

IWDTRF Flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset has occurred.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When IWDTRF is read as 1 and then 0 is written to IWDTRF.

WDTRF Flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset has occurred.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When WDTRF is read as 1 and then 0 is written to WDTRF.

SWRF Flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset has occurred.

[Setting condition]

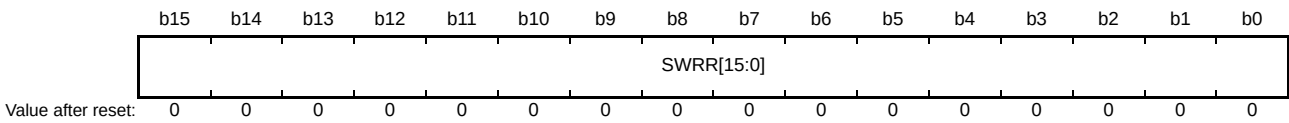
- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs.
- When SWRF is read as 1 and then 0 is written to SWRF.

6.2.4 Software Reset Register (SWRR)

Address(es): 0008 00C2h



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	SWRR[15:0]	Software Reset	Writing A501h resets the MCU. These bits are read as 0000h.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

6.3 Operation

6.3.1 RES# Pin Reset

This is a reset generated by the RES# pin.

When the RES# pin is driven low, all the processing in progress is aborted and the LSI enters a reset state.

In order to unfailingly reset the LSI, the RES# pin should be held low for the specified power supply stabilization time at a power-on.

When the RES# pin is driven high from low, the internal reset is canceled after the post-RES# cancellation wait time (tRESWT) has elapsed, and then the CPU starts the reset exception handling.

For details, see section 51, Electrical Characteristics.

6.3.2 Power-On Reset and Voltage Monitoring 0 Reset

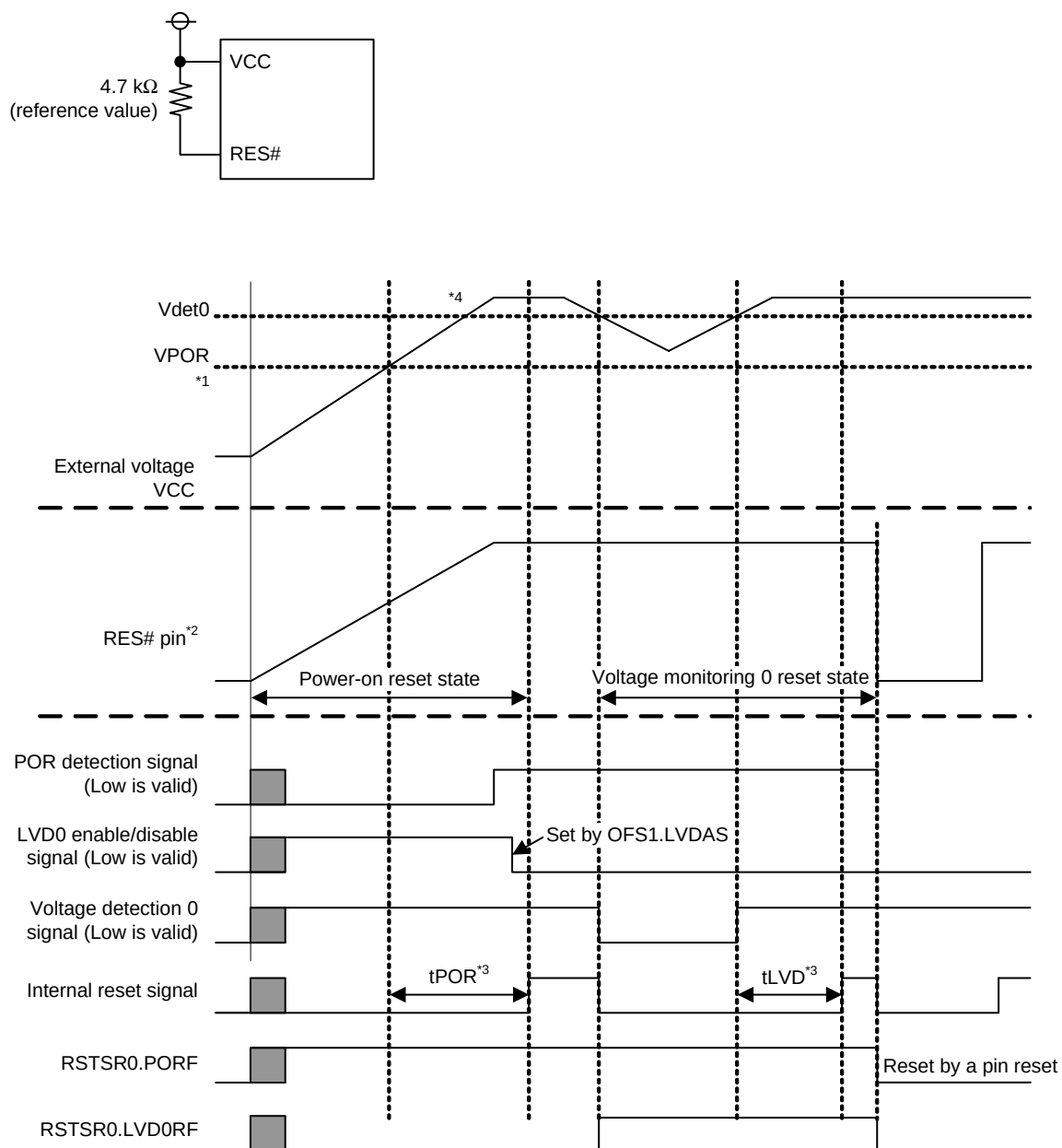
The power-on reset is an internal reset generated by the power-on reset circuit. A power-on reset is generated when power is supplied to the RES# pin while it is connected to VCC via a resistor. When connecting a capacitor to the RES# pin, also ensure that the voltage on the RES# pin is always at least VIH. For details on VIH, refer to section 51, Electrical Characteristics. After VCC has exceeded VPOR and the specified period (power-on reset time) has elapsed, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is a stabilization period for the external power supply and the MCU circuit. After a power-on reset has been generated, the PORF flag in RSTSR0 is set to 1. The PORF flag is initialized by RES# pin reset.

The voltage monitoring 0 reset is an internal reset generated by the voltage monitoring circuit. If the voltage detection circuit 0 start bit (LVDAS) in option function select register 1 (OFS1) is 0 (voltage monitoring 0 reset is enabled after a reset) and VCC falls below Vdet0, the RSTSR0.LVD0RF flag becomes 1 and the voltage detection circuit generates voltage monitoring 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitoring 0 reset is to be used.

Release from the voltage monitoring 0 reset state occurs when VCC rises above Vdet0 and the LVD0 reset time (tLVD0) elapses, and then the CPU starts the reset exception handling.

Figure 6.1 shows operations during a power-on reset and voltage monitoring 0 reset.

For details on voltage monitoring 0 reset, refer to section 8, Voltage Detection Circuit (LVDAb).



Note: For details on the electrical characteristics, see the Electrical Characteristics section.

Note 1. Vdet0 indicates the detection level for a voltage monitoring 0 reset and VPOR indicates the detection level for a power-on reset.

Note 2. Ensure that the voltage on the RES# pin is always at least VIH.

Note 3. tPOR indicates the period of a power-on reset and tLVD0 indicates the period of a voltage monitoring 0 reset.

Note 4. At the time the power-supply voltage rises, VCC must rise to at least the minimum guaranteed voltage before release from the POR reset state.

Figure 6.1 Operation Examples During a Power-On Reset and Voltage Monitoring 0 Reset

6.3.3 Voltage Monitoring 1 Reset

The voltage monitoring 1 reset is internal resets generated by the voltage monitoring circuit.

When the voltage monitoring 1 interrupt/reset enable bit (LVD1RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the voltage monitoring 1 circuit mode select bit (LVD1RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in the voltage monitoring 1 circuit control register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage-detection circuit generates a voltage monitoring 1 reset if VCC falls to or below Vdet1.

Timing for release from the voltage monitoring 1 reset state is selectable with the voltage monitoring 1 reset negation select bit (LVD1RN) in the LVD1CR0 register. When the LVD1CR0.LVD1RN bit is 0 and VCC has fallen to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling once the voltage monitoring 1 reset time (tLVD1) has elapsed after VCC has risen above Vdet1. When the LVD1CR0.LVD1RN bit is 1 and VCC has fallen to or below Vdet1, the CPU is released from the internal reset state and starts reset exception handling once the voltage monitoring 1 reset time (tLVD1) has elapsed.

Detection levels Vdet1 can be changed by settings in the voltage detection level select register (LVDLVLRL).

Figure 6.2 shows examples of operations during voltage monitoring 1 reset.

For details on the voltage monitoring 1 reset, refer to section 8, Voltage Detection Circuit (LVDAb).

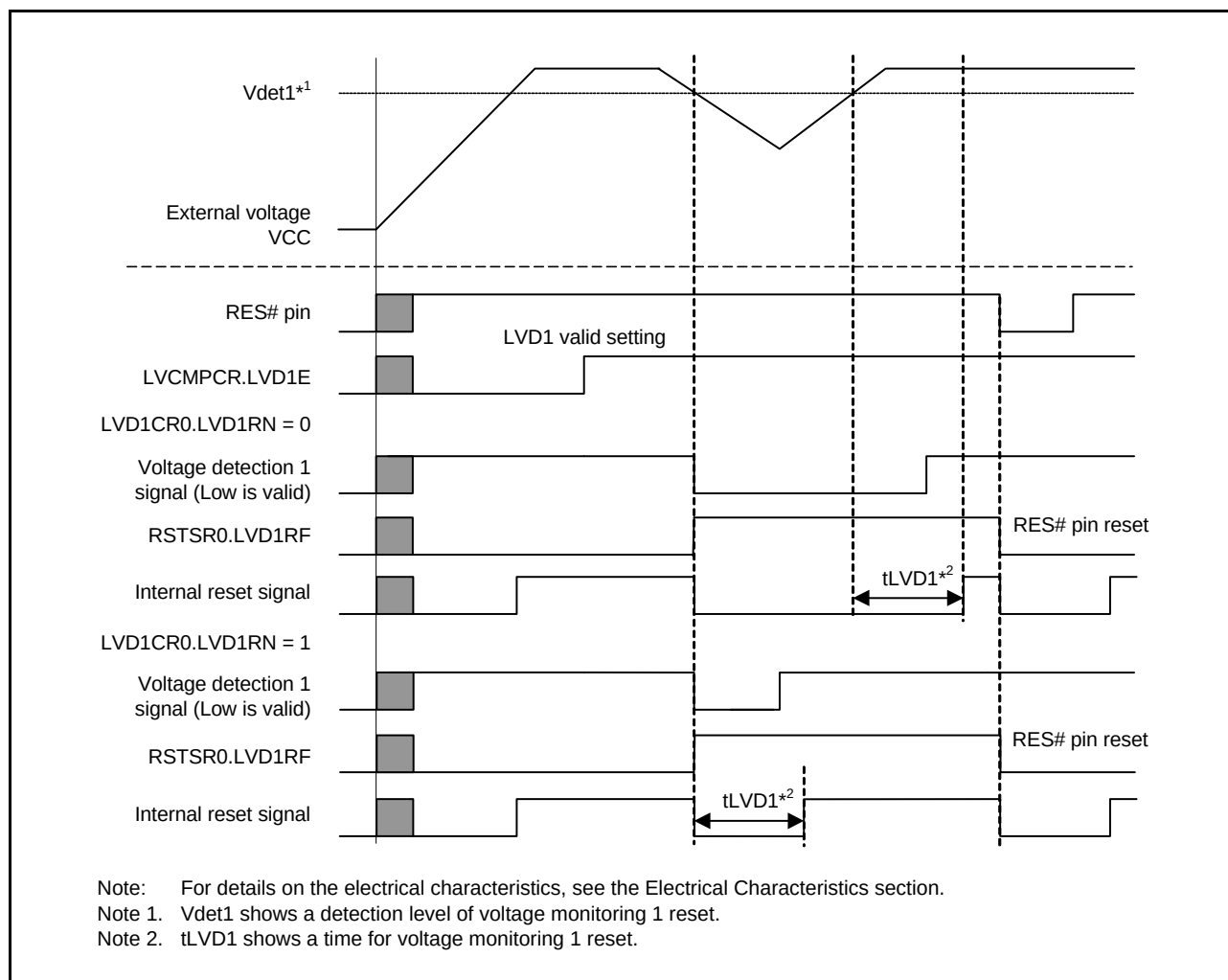


Figure 6.2 Operation Examples During Voltage Monitoring 1 Reset

6.3.4 Independent Watchdog Timer Reset

Independent watchdog timer reset is an internal reset generated by the independent watchdog timer.

Output of the independent watchdog timer reset from the independent watchdog timer can be selected by setting the IWDTR reset control register (IWDTRCR) and option function select register 0 (OFS0).

When output of the independent watchdog timer reset is selected, an independent watchdog timer reset is generated if the independent watchdog timer underflows, or if data is written outside the refresh-permitted period. When the internal reset time (tRESW2) has elapsed after the independent watchdog timer reset has been generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 31, Independent Watchdog Timer (IWDTa).

6.3.5 Watchdog Timer Reset

The watchdog-timer reset is an internal reset from the watchdog timer.

Output of the independent watchdog timer reset from the independent watchdog timer can be selected by setting the WDT reset control register (WDTRCR) and option function select register 0 (OFS0).

When output of the independent watchdog timer reset is selected, a watchdog timer reset is generated if the watchdog timer underflows, or if data is written outside the refresh-permitted period. When the internal reset time (tRESW2) has elapsed after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details, see section 30, Watchdog Timer (WDTA).

6.3.6 Software Reset

The software reset is an internal reset generated by the software reset circuit.

When A501h is written to SWRR, a software reset is generated. When the internal reset time (tRESW2) has elapsed after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

6.3.7 Determination of Cold/Warm Start

By reading the CWSF flag in RSTSR1, the type of reset processing caused can be identified; that is, whether a power-on reset has caused the reset processing (cold start) or a reset signal input during operation has caused the reset processing (warm start).

The CWSF flag in RSTSR1 is set to 0 when a power-on reset occurs (cold start); otherwise the flag is not set to 0. The flag is set to 1 when 1 is written to it through programming; it is not set to 0 even when 0 is written.

Figure 6.3 shows an example of cold/warm start determination operation.

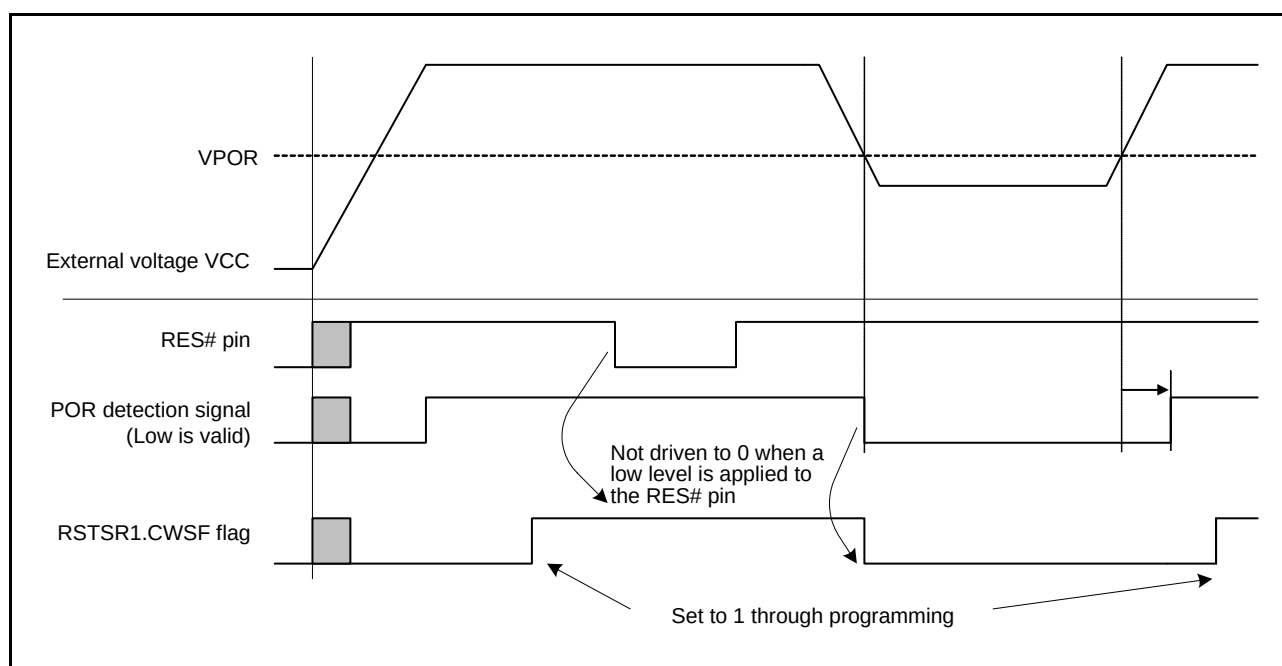


Figure 6.3 Example of Cold/Warm Start Determination Operation

6.3.8 Determination of Reset Generation Source

Reading RSTSR0 and RSTSR2 determines which reset was used to execute the reset exception handling.

Figure 6.4 shows an example of the flow to identify a reset generation source.

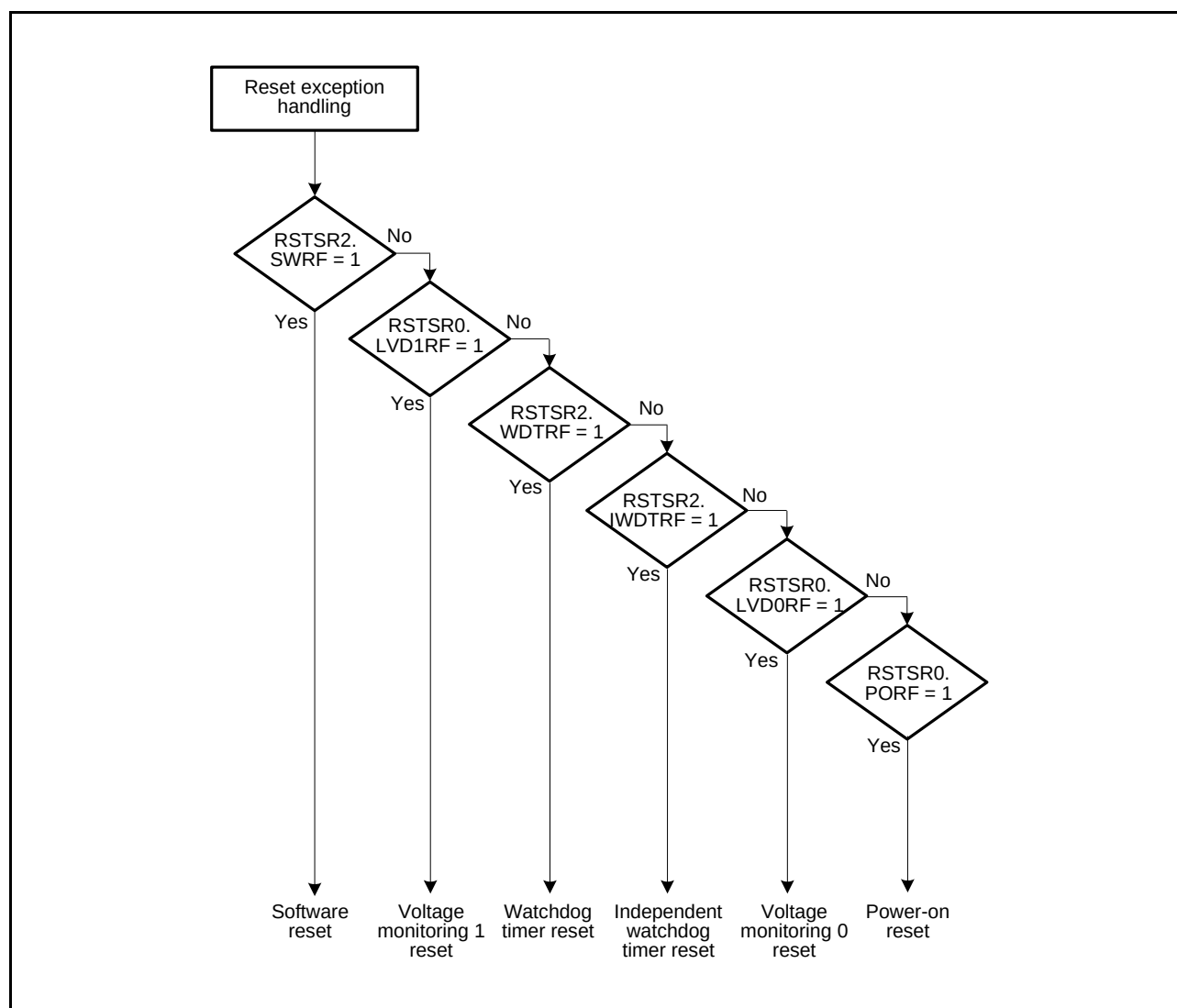


Figure 6.4 Example of Reset Generation Source Determination Flow

7. Option-Setting Memory (OFSM)

7.1 Overview

Option-setting memory (OFSM) refers to a set of registers that are provided for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the ROM.

Figure 7.1 shows the option-setting memory area.

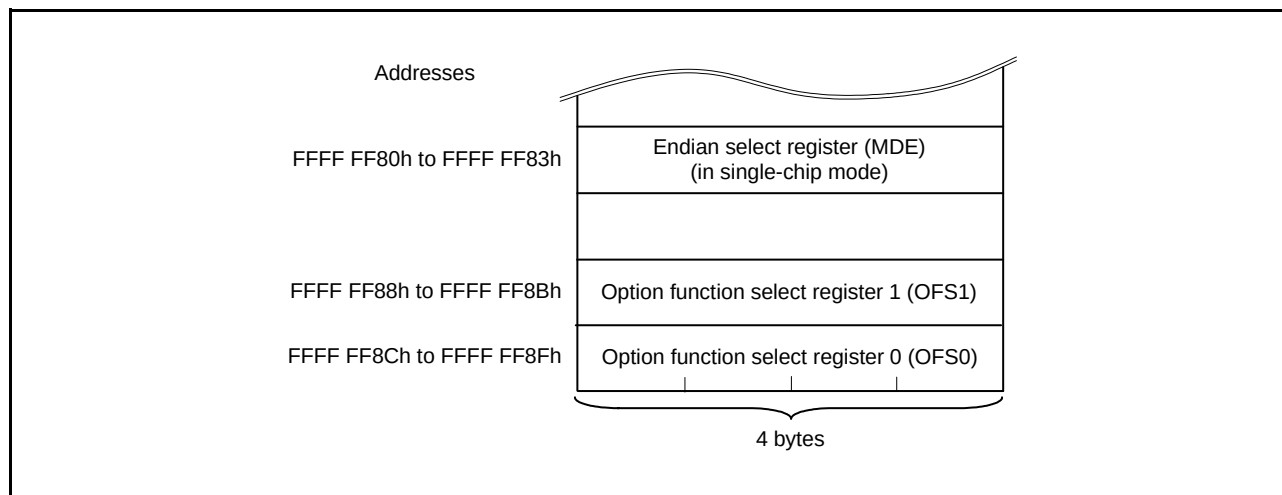


Figure 7.1 Option-Setting Memory Area

7.2 Register Descriptions

7.2.1 Option Function Select Register 0 (OFS0)

Address(es): OFSM.OFS0 FFFF FF8Ch

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	WDTRS TIRQS	WDTRPSS[1:0]	WDTRPES[1:0]			WDTCKS[3:0]				WDTTOPS[1:0]	WDTST RT	—	

Value after reset:

The value set by the user*1

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	IWDTSLCSTP	—	IWDTSTRIRQS	WDTRPSS[1:0]	WDTRPES[1:0]			WDTCKS[3:0]				WDTTOPS[1:0]	IWDTST TRT	—	

Value after reset:

The value set by the user*1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	When reading, this bit returns the value written by the user. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: IWDT is automatically activated in auto-start mode after a reset 1: IWDT is halted after a reset	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Select	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)	R
b7 to b4	IWDTCKS[3:0]	IWDT Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: No division 0 0 1 0: Divide-by-16 0 0 1 1: Divide-by-32 0 1 0 0: Divide-by-64 1 1 1 1: Divide-by-128 0 1 0 1: Divide-by-256 Settings other than above are prohibited.	R
b9, b8	IWDRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting)	R
b11, b10	IWDRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting)	R
b12	IWDTSTRIRQS	IWDT Reset Interrupt Request Select	0: Non-maskable interrupt request is enabled 1: Reset is enabled	R
b13	—	Reserved	When reading, this bit returns the value written by the user. The write value should be 1.	R
b14	IWDTSLCSTP	IWDT Sleep Mode Count Stop Control	0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	R
b16, b15	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R
b17	WDTSTRT	WDT Start Mode Select	0: WDT is automatically activated in auto-start mode after a reset 1: WDT is stopped after a reset	R

Bit	Symbol	Bit Name	Description	R/W
b19, b18	WDTTOPS[1:0]	WDT Timeout Period Select	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	R
b23 to b20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	b23 b20 0 0 0 1: Divide-by-4 0 1 0 0: Divide-by-64 1 1 1 1: Divide-by-128 0 1 1 0: Divide-by-512 0 1 1 1: Divide-by-2048 1 0 0 0: Divide-by-8192 Settings other than above are prohibited.	R
b25, b24	WDRPES[1:0]	WDT Window End Position Select	b25 b24 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting)	R
b27, b26	WDRPSS[1:0]	WDT Window Start Position Select	b27 b26 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting)	R
b28	WDRSTIRQS	WDT Reset Interrupt Request Select	0: Non-maskable interrupt request is enabled 1: Reset is enabled	R
b31 to b29	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. This register is set to a specified value after programming of the flash memory with the user program.

The OFS0 register is allocated in the ROM. Set this register at the same time as writing the program. After writing to the OFS0 register once, do not write to it again.

When erasing the block including the OFS0 register, the OFS0 register value becomes FFFF FFFFh.

The setting in the OFS0 register is ignored in boot mode, and this register functions similarly when it is set to FFFF FFFFh.

IWDTSTRT Bit (IWDT Start Mode Select)

This bit selects the mode in which the IWDT is activated after a reset (stopped state or activated in auto-start mode). When activated in auto-start mode, the OFS0 register setting for the IWDT is effective.

IWDTTOPS[1:0] Bits (IWDT Timeout Period Select)

These bits select the timeout period, i.e. the time it takes for the down-counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set by the IWDTCKS[3:0] bits. The time (number of IWDT-dedicated clock cycles) it takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] bits and IWDTTOPS[1:0] bits.

For details, see section 31, Independent Watchdog Timer (IWDTa).

IWDTCKS[3:0] Bits (IWDT Clock Frequency Division Ratio Select)

These bits select, from 1/1, 1/16, 1/32, 1/64, 1/128, and 1/256, the division ratio of the prescaler to divide the frequency of the IWDT-dedicated clock. Using the setting of these bits together with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 128 to 524288 IWDT-dedicated clock cycles.

For details, see section 31, Independent Watchdog Timer (IWDTa).

IWDRPES[1:0] Bits (IWDT Window End Position Select)

These bits select the position of the end of the window for the down-counter as 0%, 25%, 50%, or 75% of the value being

counted by the counter. The value of the window end position must be smaller than the value of the window start position (window start position > window end position). If the value for the window end position is greater than the value for the window start position, only the value for the window start position is effective.

The counter values corresponding to the settings for the start and end positions of the window in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits vary with the setting of the IWDTTOPS[1:0] bits.

For details, refer to section 31, Independent Watchdog Timer (IWDTa).

IWDTRPSS[1:0] Bits (IWDT Window Start Position Select)

These bits select the position where the window for the down-counter starts as 25%, 50%, 75%, or 100% of the value being counted (the point at which counting starts is 100% and the point at which an underflow occurs is 0%). The interval between the positions where the window starts and ends becomes the period in which refreshing is possible, and refreshing is not possible outside this period.

For details, refer to section 31, Independent Watchdog Timer (IWDTa).

IWDRSTIRQS Bit (IWDT Reset Interrupt Request Select)

The setting of this bit selects the operation on an underflow of the down-counter or generation of a refresh error. Either an independent watchdog timer reset or a non-maskable interrupt request is selectable.

For details, refer to section 31, Independent Watchdog Timer (IWDTa).

IWDTSLCSTP Bit (IWDT Sleep Mode Count Stop Control)

This bit selects whether to stop counting when entering sleep, software standby, or deep sleep mode.

For details, see section 31, Independent Watchdog Timer (IWDTa).

WDTSTRT Bit (WDT Start Mode Select)

This bit selects the mode in which the WDT is activated after a reset (stopped state or activated in auto-start mode).

When activated in auto-start mode, the OFS0 register setting for the WDT is effective.

WDDTOPS[1:0] Bits (WDT Timeout Period Select)

These bits select the timeout period, i.e. the time it takes for the down-counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set by the WDTCKS[3:0] bits. The time (number of PCLKB cycles) it takes to underflow after a refresh operation is determined by a combination of the WDTCKS[3:0] bits and WDDTOPS[1:0] bits.

For details, see section 30, Watchdog Timer (WDTA).

WDTCKS[3:0] Bits (WDT Clock Frequency Division Ratio Select)

These bits select, from 1/4, 1/64, 1/128, 1/512, 1/2048, and 1/8192, the division ratio of the prescaler to divide the frequency of PCLKB. Using the setting of these bits together with the WDDTOPS[1:0] bit setting, the WDT counting period can be set from 4096 to 134217728 PCLKB cycles.

For details, see section 30, Watchdog Timer (WDTA).

WDRPES[1:0] Bits (WDT Window End Position Select)

These bits select the position of the end of the window on the down-counter as 0%, 25%, 50%, or 75% of the value being counted by the counter. The value of the window end position must be smaller than the value of the window start position (window start position > window end position). If the value for the window end position is greater than the value for the window start position, only the value for the window start position is effective.

The counter values corresponding to the settings for the start and end positions of the window in the WDRPSS[1:0] and WDRPES[1:0] bits vary with the setting of the WDDTOPS[1:0] bits.

For details, refer to section 30, Watchdog Timer (WDTA).

WDTRPSS[1:0] Bits (WDT Window Start Position Select)

These bits select the position where the window for the down-counter starts as 25%, 50%, 75%, or 100% of the value being counted (the point at which counting starts is 100% and the point at which an underflow occurs is 0%). The interval between the positions where the window starts and ends becomes the period in which refreshing is possible, and refreshing is not possible outside this period.

For details, refer to section 30, Watchdog Timer (WDTA).

WDTRSTIRQS Bit (WDT Reset Interrupt Request Select)

The setting of this bit selects the operation on an underflow of the down-counter or generation of a refresh error. Either a watchdog timer reset or a non-maskable interrupt request is selectable.

For details, refer to section 30, Watchdog Timer (WDTA).

7.2.2 Option Function Select Register 1 (OFS1)

Address(es): OFSM.OFS1 FFFF FF88h, (FFFF 7F88h)*1

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Value after reset: The value set by the user*2

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	HOCO EN	—	—	—	—	FASTS TUP	LVDAS	VDSEL[1:0]	—

Value after reset: The value set by the user*2

Bit	Symbol	Bit Name	Description	R/W
b1, b0	VDSEL[1:0]	Voltage Detection 0 Level Select	b1 b0 0 0: Settings prohibited 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Voltage monitoring 0 reset is enabled after a reset 1: Voltage monitoring 0 reset is disabled after a reset	R
b3	FASTSTUP	Power-On Fast Startup Time	0: Fast startup time at power on 1: Normal startup	R
b7 to b4	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R
b8	HOCOEN	HOCO Oscillation Enable	0: HOCO oscillation is enabled after a reset 1: HOCO oscillation is disabled after a reset	R
b31 to b9	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R

Note 1. Set the same value to this address when using start-up program protection.

Note 2. The value of the blank product is FFFF FFFFh. This register is set to a specified value after programming of the flash memory with the user program.

The OFS1 register is allocated in the ROM. Set this register at the same time as writing the program. After writing, do not write additions to this register.

When erasing the block including the OFS1 register, the OFS1 register value becomes FFFF FFFFh.

The setting in the OFS1 register is ignored in boot mode, and this register functions similarly when it is set to FFFF FFFFh.

VDSEL[1:0] Bits (Voltage Detection 0 Level Select)

These bits select the voltage detection level to be monitored by the voltage detection 0 circuit.

Set the voltage detection 0 level to 2.51 V (set VDSEL[1:0] bits to 10b) before using the battery backup function (setting the VBATTCCR.VBATTDIS bit to 0).

LVDAS Bit (Voltage Detection 0 Circuit Start)

This bit selects whether the voltage monitoring 0 reset is enabled or disabled after a reset.

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by the VDSEL[1:0] bits.

FASTSTUP Bit (Power-On Fast Startup Time)

The startup time can be reduced by setting this bit to 0 (fast startup time at power on) when it is possible to meet the power-on VCC rising gradient (during fast startup time) shown in Electrical Characteristics. Do not set this bit to 0 when it is not possible to meet the power-on VCC rising gradient (during fast startup time).

HOCOEN Bit (HOCO Oscillation Enable)

This bit selects whether the HOCO oscillation is effective or not after a reset.

Setting the HOCOEN bit to 0 allows the HOCO oscillation to be started before the CPU starts operation, and therefore reduces the wait time for oscillation stabilization.

Note that even if the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is switched to HOCO only by modifying the clock source select bits (SCKCR3.CKSEL[2:0]) from the CPU.

Also, when the HOCOEN bit is set to 0, the HOCO oscillation stabilization time (tHOCO) is secured by hardware, so the clock with the accuracy of the HOCO oscillation frequency (fHOCO) shown in Electrical Characteristics is supplied after release from the CPU reset state.

7.2.3 Endian Select Register (MDE)

Address(es): OFSM.MDE FFFF FF80h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset: The value set by the user*1															
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	—	—	—	—	—	MDE[2:0]		
Value after reset: The value set by the user*1															

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MDE[2:0]	Endian Select	b2 b0 0 0 0: Big endian 1 1 1: Little endian Settings other than above are prohibited.	R
b31 to b3	—	Reserved	When reading, these bits return the value written by the user. The write value should be 1.	R

Note 1. The value of the blank product is FFFF FFFFh. This register is set to a specified value after programming of the flash memory with the user program.

The MDE register selects the endian for the CPU. In single-chip mode, the endian select register (MDE) at address FFFF FF80h is used to select the endian.

MDE is allocated in the ROM. Set the register at the same time as writing the program. After writing to the register once, do not write to it again.

When erasing the block including the MDE register, the MDE register value becomes FFFF FFFFh.

MDE[2:0] Bits (Endian Select)

These bits select little endian or big endian for the CPU.

The endian is determined by the value at address FFFF FF80h in the user area when operating in single-chip mode.

7.3 Usage Note

7.3.1 Setting Example of Option-Setting Memory

Since the option-setting memory is allocated in the ROM, values cannot be written by executing instructions. Write appropriate values when writing the program. Examples of the settings are shown below.

- To set FFFF FFF8h in the OFS0 register

```
.ORG    0FFFFFFF8CH  
.LWORD  0FFFFFFF8H
```

- To set FFFF FEF0h in the OFS1 register

```
.ORG    0FFFFFFF88H  
.LWORD  0FFFFFFEF0H  
.ORG    0FFFF7F88H  
.LWORD  0FFFFFFEF0H
```

When neither the voltage monitoring 0 reset nor power-on fast startup time is used, the value set in the address FFFF 7F88h can be FFFF FFFh.

Note: Programming formats vary depending on the compiler. Refer to the compiler manual for details.

8. Voltage Detection Circuit (LVDAb)

The voltage detection circuit (LVD) monitors the voltage level input to the VCC pin using a program.

8.1 Overview

In voltage detection 0, the detection voltage can be selected from three levels using option function select register 1 (OFS1).

In voltage detection 1, the detection voltage can be selected from 10 levels using the voltage detection level select register (LVDLVLR).

Voltage monitoring 0 reset and voltage monitoring 1 reset/interrupt can be used.

Table 8.1 lists the specifications of the voltage detection circuit. Figure 8.1 is a block diagram of the voltage detection circuit. Figure 8.2 is a block diagram of the voltage monitoring 1 interrupt/reset circuit.

Table 8.1 LVD Specifications

Item		Voltage Monitoring 0	Voltage Monitoring 1
VCC monitoring	Monitored voltage	Vdet0	Vdet1
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1
	Detection voltage	Voltage selectable from four levels using OFS1	Voltage selectable from 10 levels using the LVDLVLR.LVD1LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1 LVD1SR.LVD1DET flag: Vdet1 passage detection
Process upon voltage detection	Reset	Voltage monitoring 0 reset Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Voltage monitoring 1 reset Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC
	Interrupt	Not available	Voltage monitoring 1 interrupt Non-maskable or maskable interrupt is selectable Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either
Event link function		Not available	Available Vdet1 passage detection event output

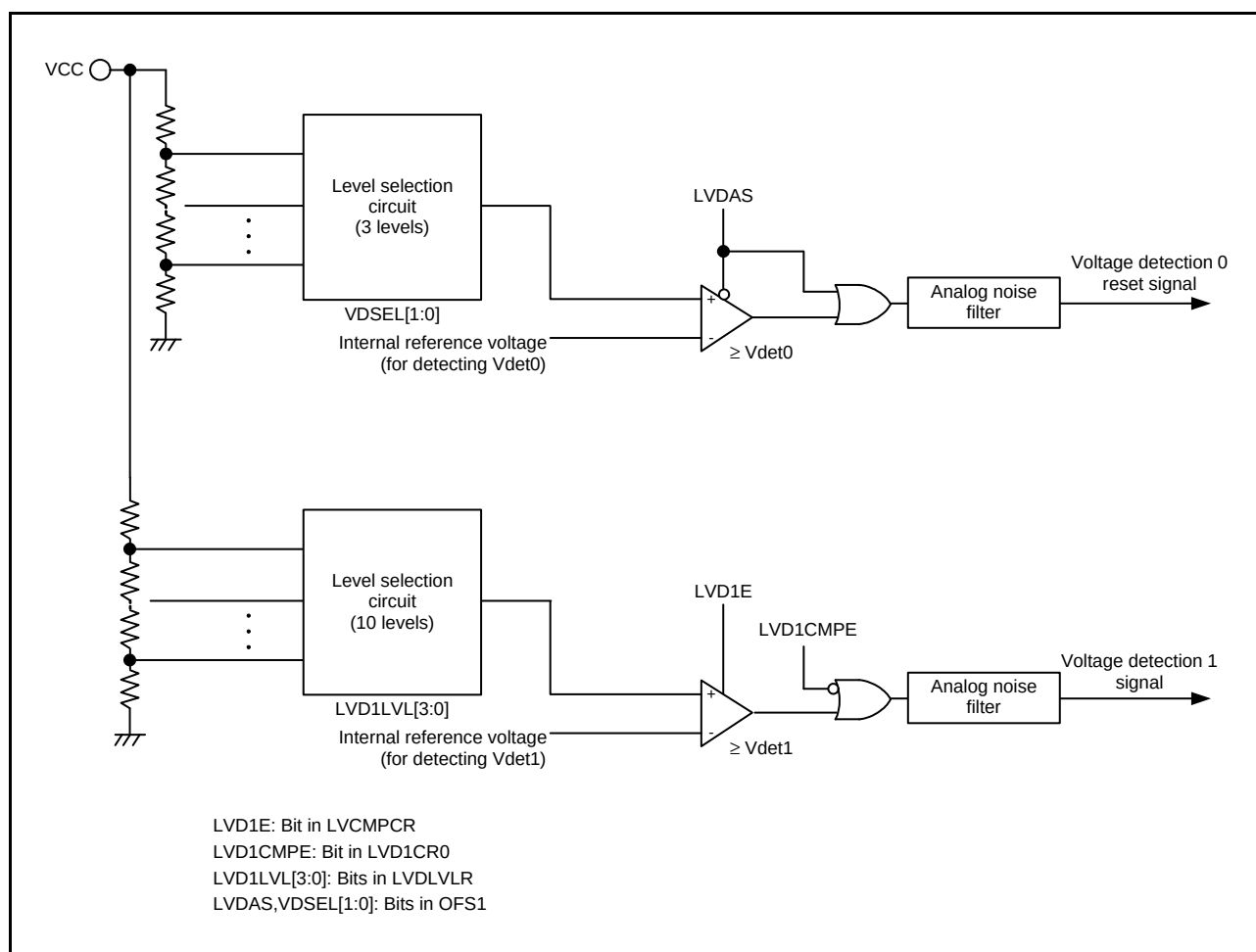


Figure 8.1 Block Diagram of the LVD

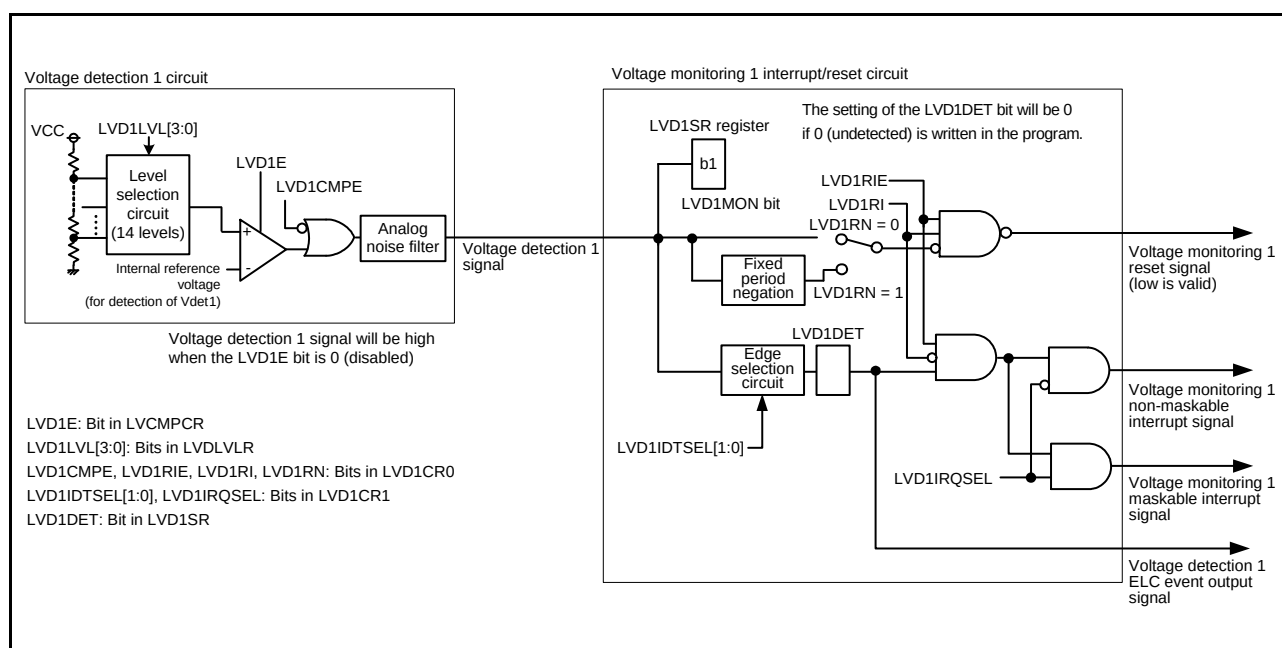


Figure 8.2 Block Diagram of Voltage Monitoring 1 Interrupt/Reset Circuit

8.2 Register Descriptions

8.2.1 Voltage Monitoring 1 Circuit Control Register 1 (LVD1CR1)

Address(es): 0008 00E0h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	LVD1IRQSEL	LVD1IDTSEL[1:0]	1
Value after reset:	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LVD1IDTSEL [1:0]	Voltage Monitoring 1 Interrupt ELC Event Generation Condition Select	b1 b0 0 0: When $VCC \geq V_{det1}$ (rise) is detected 0 1: When $VCC < V_{det1}$ (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited	R/W
b2	LVD1IRQSEL	Voltage Monitoring 1 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.2 Voltage Monitoring 1 Circuit Status Register (LVD1SR)

Address(es): 0008 00E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LVD1MON	LVD1DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LVD1DET	Voltage Monitoring 1 Voltage Change Detection Flag	0: Not detected 1: Vdet1 passage detection	R/(W) *1
b1	LVD1MON	Voltage Monitoring 1 Signal Monitor Flag	0: VCC < Vdet1 1: VCC ≥ Vdet1 or LVD1MON circuit is disabled	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

Note 1. Only 0 can be written to this bit. After writing 0 to this bit, it takes two system clock cycles for the bit to be read as 0.

LVD1DET Flag (Voltage Monitoring 1 Voltage Change Detection Flag)

The LVD1DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.LVD1CMPE bit is 1 (voltage monitoring 1 circuit comparison result output enabled).

The LVD1DET flag should be set to 0 after LVD1CR0.LVD1RIE is set to 0 (disabled). LVD1CR0.LVD1RIE can be set to 1 (enabled) again after a period of two or more cycles of PCLKB has elapsed.

With read access to an I/O register which access cycle number is defined by PCLKB, two or more cycles of PCLKB may have to be secured as waiting time.

LVD1MON Flag (Voltage Monitoring 1 Signal Monitor Flag)

The LVD1MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.LVD1CMPE bit is 1 (voltage monitoring 1 circuit comparison result output enabled).

8.2.3 Voltage Monitoring Circuit Control Register (LVCMPCR)

Address(es): 0008 C297h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

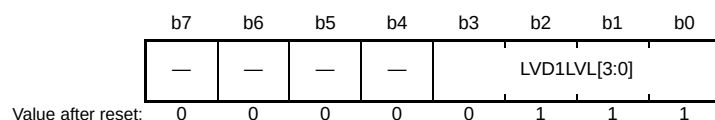
Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1E Bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.LVD1MON flag, set the LVD1E bit to 1. The voltage detection 1 circuit starts once $td(E-A)$ passes after the LVD1E bit value is changed from 0 to 1.

8.2.4 Voltage Detection Level Select Register (LVDLVL[R])

Address(es): 0008 C298h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	LVD1LVL[3:0]	Voltage Detection 1 Level Select (Standard voltage during drop in voltage)	b3 b0 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than those listed above are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

When changing the LVDLVL[R] register, first set the LVCMP[R].LVD1E bit to 0 (voltage detection 1 circuit disabled).
For details on the voltage detection level range, refer to section 51, Electrical Characteristics.

8.2.5 Voltage Monitoring 1 Circuit Control Register 0 (LVD1CR0)

Address(es): 0008 C29Ah

b7	b6	b5	b4	b3	b2	b1	b0
LVD1RN	LVD1RI	—	—	—	LVD1CMPE	—	LVD1RIE
Value after reset:	1	0	0	0	X	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	LVD1RIE	Voltage Monitoring 1 Interrupt/Reset Enable	0: Disabled 1: Enabled	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	LVD1CMPE	Voltage Monitoring 1 Circuit Comparison Result Output Enable	0: Voltage monitoring 1 circuit comparison results output disabled 1: Voltage monitoring 1 circuit comparison results output enabled	R/W
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LVD1RI	Voltage Monitoring 1 Circuit Mode Select	0: Voltage monitoring 1 interrupt occurs when the voltage passes Vdet1 1: Voltage monitoring 1 reset occurs when the voltage falls below Vdet1	R/W
b7	LVD1RN	Voltage Monitoring 1 Reset Negation Select	0: Negation follows a stabilization time (tLVD1) after VCC > Vdet1 is detected. 1: Negation follows a stabilization time (tLVD1) after assertion of the voltage monitoring 1 reset.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

LVD1RIE Bit (Voltage Monitoring 1 Interrupt/Reset Enable)

The LVD1RIE bit is enabled when the LVCMPCR.LVD1E bit is set to 1 (voltage detection 1 circuit enabled) and the LVD1CMPE bit is set to 1 (voltage monitoring 1 circuit comparison results output enabled).

Ensure that neither a voltage monitoring 1 reset nor a voltage monitoring 1 non-maskable interrupt is generated during programming or erasure of the flash memory.

LVD1RN Bit (Voltage Monitoring 1 Reset Negation Select)

If the LVD1RN bit is to be set to 1 (negation follows a stabilization time after assertion of the voltage monitoring 1 reset), set the LOCOCR.LCSTP bit to 0 (LOCO is operating). Furthermore, if a transition to software standby mode, the only possible value for the LVD1RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the LVD1RN bit to 1 (negation follows a stabilization time after assertion of the voltage monitoring 1 reset).

8.3 VCC Input Voltage Monitor

8.3.1 Monitoring Vdet0

Monitoring Vdet0 is not possible.

8.3.2 Monitoring Vdet1

After making the following settings, the LVD1SR.LVD1MON flag can be used to monitor the results of comparison by voltage monitor 1.

- (1) Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).
- (2) Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).
- (3) After waiting for $t_d(E-A)$, set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).

8.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the voltage detection 0 circuit start bit (OFS1.LVDAS) to 0 (enabling the voltage monitor 0 reset after a reset).

Figure 8.3 shows an example of operations for a voltage monitoring 0 reset.

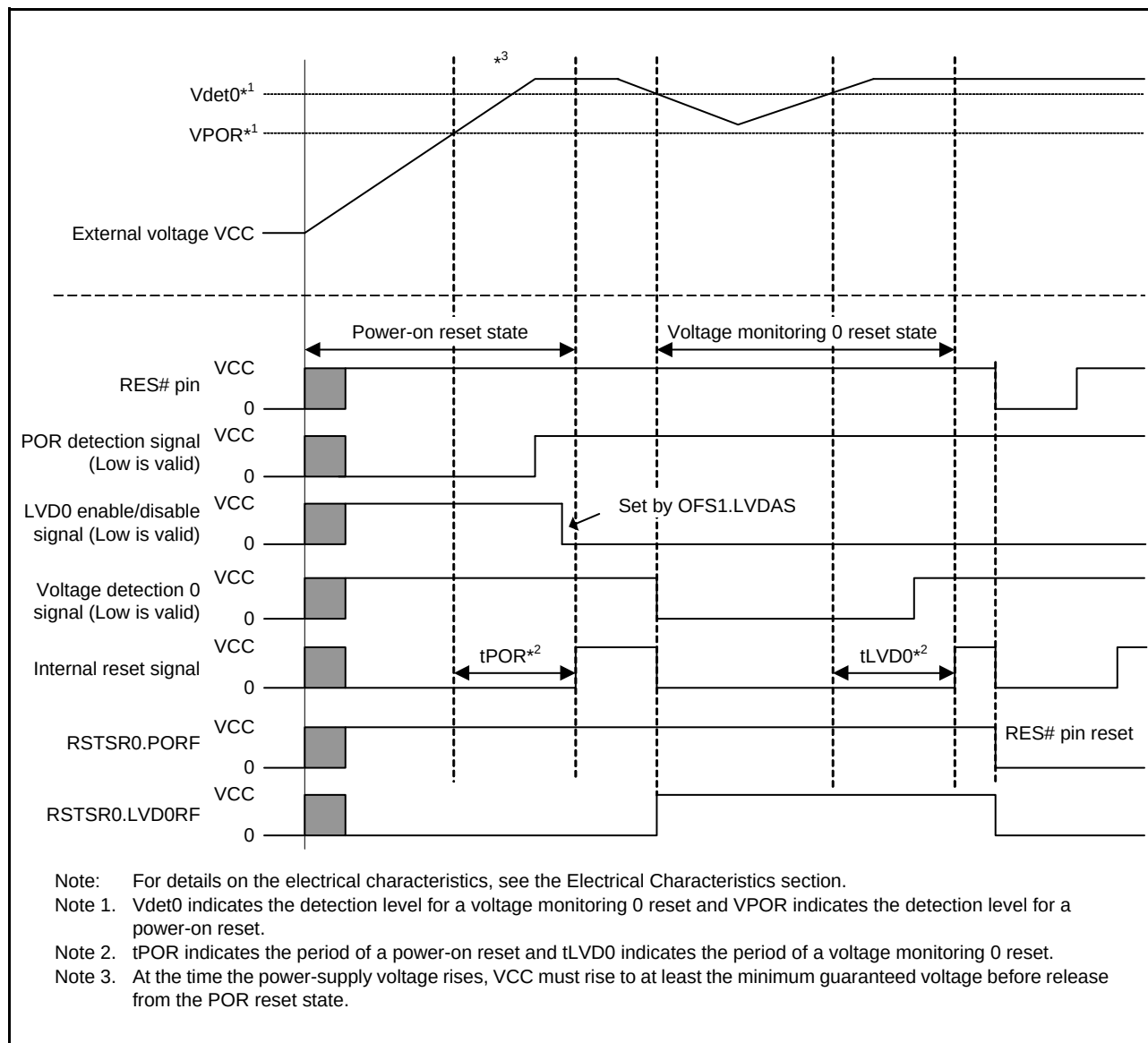


Figure 8.3 Example of Voltage Monitoring 0 Reset Operation

8.5 Interrupt and Reset from Voltage Monitoring 1

Table 8.2 shows the procedures for setting bits related to the voltage monitoring 1 interrupt and voltage monitoring 1 reset. Table 8.3 shows the procedures for stopping bits related to the voltage monitoring 1 interrupt and voltage monitoring 1 reset. Figure 8.4 shows an example of operations for a voltage monitoring 1 interrupt. For the operation of the voltage monitoring 1 reset, see Figure 6.2 in section 6, Resets.

Table 8.2 Procedures for Setting Bits Related to the Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Step	Voltage Monitoring 1 Interrupt, Voltage Monitoring 1 ELC Event Output	Voltage Monitoring 1 Reset
1 ^{*1}	Select the detection voltage by setting the LVD1LVR.LVD1LVL[3:0] bits.	
2 ^{*1}	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.
3	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	—
4	—	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).
5 ^{*1}	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	
6 ^{*1}	Wait for at least $t_d(E-A)$.	
7	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison results output enabled).	
8	Wait for at least 2 μs .	—
9	Set the LVD1SR.LVD1DET bit to 0.	—
10	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	—

Note 1. Steps 1, 2, 5, and 6 are not required if operation is with the setting to select the voltage monitoring 1 interrupt (LVD1CR0.LVD1RI = 0) and operation can be restarted by simply changing the settings of the LVD1CR1.LVD1IRQSEL and LVD1IDTSEL[1:0] bits after monitoring is stopped or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitoring 1 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 10.

Table 8.3 Procedures for Stopping Bits Related to the Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Step	Voltage Monitoring 1 Interrupt, Voltage Monitoring 1 ELC Event Output	Voltage Monitoring 1 Reset
1	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).	—
2	Set the LVD1CR0.LVD1CMPE bit to 0 (voltage monitoring 1 circuit comparison results output disabled).	
3 ^{*1}	Set the LVCMPCR.LVD1E bit to 0 (voltage detection 1 circuit disabled).	
4	—	Set the LVD1CR0.LVD1RIE bit to 0 (voltage monitoring 1 interrupt/reset disabled).
5	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	

Note 1. Step 3 is not required if operation is with the setting to select the voltage monitoring 1 interrupt (LVD1CR0.LVD1RI = 0) and operation can be restarted by simply changing the settings of the LVD1CR1.LVD1IRQSEL and LVD1IDTSEL[1:0] bits after monitoring is stopped or if restarting is in a case where the settings related to the voltage-detection circuit were not changed after monitoring was stopped. When changes are to be made and operation is with the setting to select the voltage monitoring 1 reset (LVD1CR0.LVD1RI = 1), proceed through all steps from 1 to 5.

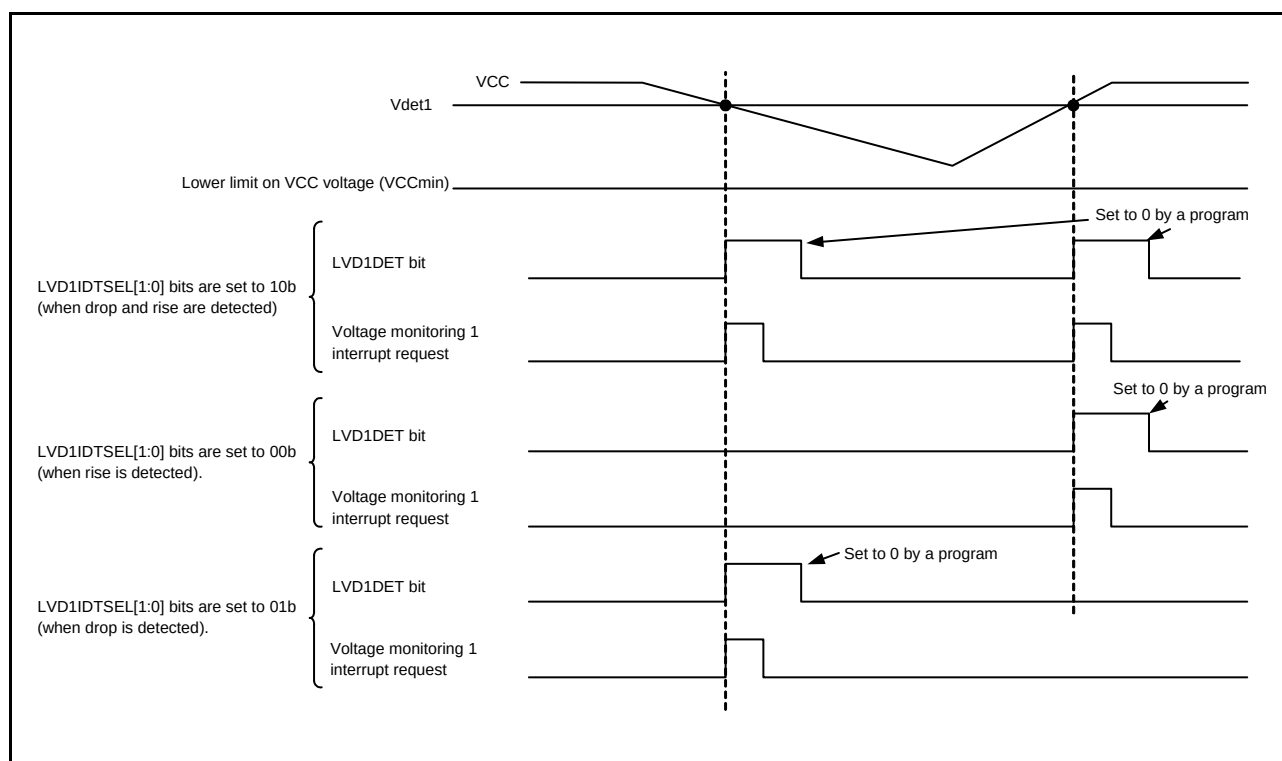


Figure 8.4 Example of Voltage Monitoring 1 Interrupt Operation

8.6 Event Link Output

The LVD can output the event signals to the event link controller (ELC).

(1) Vdet1 passage detection event output

The LVD outputs the event signal when it is detected that the voltage has passed the Vdet1 voltage while both the voltage detection 1 circuit and the voltage monitoring 1 circuit comparison result output are enabled.

When enabling the LVD's event link output function, be sure to make settings for enabling the LVD before enabling the LVD event link function of the ELC. To stop the LVD's event link output function, be sure to make settings for stopping the LVD after disabling the LVD event link function of the ELC.

8.6.1 Interrupt Handling and Event Linking

The LVD has the bits to separately enable or disable the voltage monitoring 1 interrupt. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt request signal is output to the CPU.

On the contrary, as soon as an interrupt source is generated, the event link signal is output as the event signal to the other module via the ELC regardless of the state of the interrupt enable bit.

It is possible to output voltage monitoring 1 interrupt in software standby. The event signal for the ELC, however, is output as follows:

- When the event of passing Vdet1 is detected in software standby mode, no event signals are generated for the ELC because no clock is presented in software standby mode. Since the Vdet1 passage detection flag is preserved, however, when the supply of the clock is resumed after restoring from software standby mode, the event signal for the ELC is output according to the state of the Vdet1 passage detection flag.

9. Clock Generation Circuit

9.1 Overview

This MCU incorporates a clock generation circuit.

Table 9.1 lists the specifications of the clock generation circuit. Figure 9.1 and Figure 9.2 show a block diagram of the clock generation circuit.

Table 9.1 Specifications of Clock Generation Circuit (1/2)

Item	Specification
Uses	- Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. - Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU2, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for other modules. - Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. - Generates the USB clock (UCLK) to be supplied to the USB. - Generates the CAC clock (CACCLK) to be supplied to the CAC. - Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. - Generates the IWDTC-dedicated low-speed clock (IWDTCCLK) to be supplied to the IWDTC. - Generates the CAN clock (CANMCLK) to be supplied to the RSCAN. - Generates the SSI clock (SSISCK) to be supplied to the SSI. - Generates the LPT clock (LPTCLK) to be supplied to the LPT. - Generation of Bluetooth-dedicated clock (BLECK) - Generation of Bluetooth-dedicated low speed clock (BLELOCO)
Operating frequencies*1	- ICLK: 54 MHz (max) - PCLKA: 54 MHz (max) - PCLKB: 32 MHz (max) - PCLKD: 54 MHz (max) - FCLK: 1 to 32 MHz (for programming and erasing the ROM and E2 DataFlash) 32 MHz (max) (for reading from the E2 DataFlash) - UCLK: 48 MHz - CACCLK: Same frequency as each oscillator - RTCSCLK: 32.768 kHz - IWDTCCLK: 15 kHz - CANMCLK: 20 MHz (max) - SSISCK: 20 MHz (max) - LPTCLK: The same frequency as that of the selected oscillator - BLECK: 32 MHz - BLELOCO: 32.768 kHz
Main clock oscillator*2	- Resonator frequency: 1 to 20 MHz ($V_{CC} \geq 2.4$ V), 1 to 8 MHz ($V_{CC} < 2.4$ V) - External clock input frequency: 20 MHz (max) - Connectable resonator or additional circuit: ceramic resonator, crystal - Connection pins: EXTAL, XTAL - Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU output can be forcedly driven to high-impedance. - Drive capacity switching function
Sub-clock oscillator	- Resonator frequency: 32.768 kHz - Connectable resonator or additional circuit: crystal - Connection pin: XCIN, XCOU - Drive capacity switching function
PLL circuit*3	- Input clock source: Main clock - Input pulse frequency division ratio: Selectable from 1, 2, and 4 - Input frequency: 4 to 12.5 MHz - Frequency multiplication ratio: Selectable from 4 to 13.5 (increments of 0.5) - VCO oscillation frequency: 24 to 54 MHz ($V_{CC} \geq 2.4$ V)
USB-dedicated PLL circuit*3	- Input clock source: Main clock - Input pulse frequency division ratio: Selectable from 1, 2, and 4 - Input frequency: 4, 6, 8, and 12 MHz - Frequency multiplication ratio: Selectable from 4, 6, 8, and 12 - VCO oscillation frequency: 48 MHz ($V_{CC} \geq 2.4$ V)

Table 9.1 Specifications of Clock Generation Circuit (2/2)

Item	Specification
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 and 54 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz
Bluetooth-dedicated clock oscillator	- Frequency of oscillation: 32 MHz - Connectable resonator: Crystal (The 83-pin LGA package product includes a crystal resonator.) - Connection pin: XTAL1_RF, and XTAL2_RF
Bluetooth-dedicated low-speed on-chip oscillator	Frequency of oscillation: 32.768 kHz

Note 1. The maximum operating frequency in high-speed operating mode. For the maximum operating frequency in the other operating modes, refer to section 11.2.6, Operating Power Control Register (OPCCR).

Note 2. When oscillating USB-dedicated PLL at 48 MHz and the PLL at 54 MHz, the frequency of the main clock oscillator should be set to 4, 6, 8, or 12 MHz.

Note 3. The PLL and USB-dedicated PLL can be used when the external voltage (VCC) is 2.4 V or above.

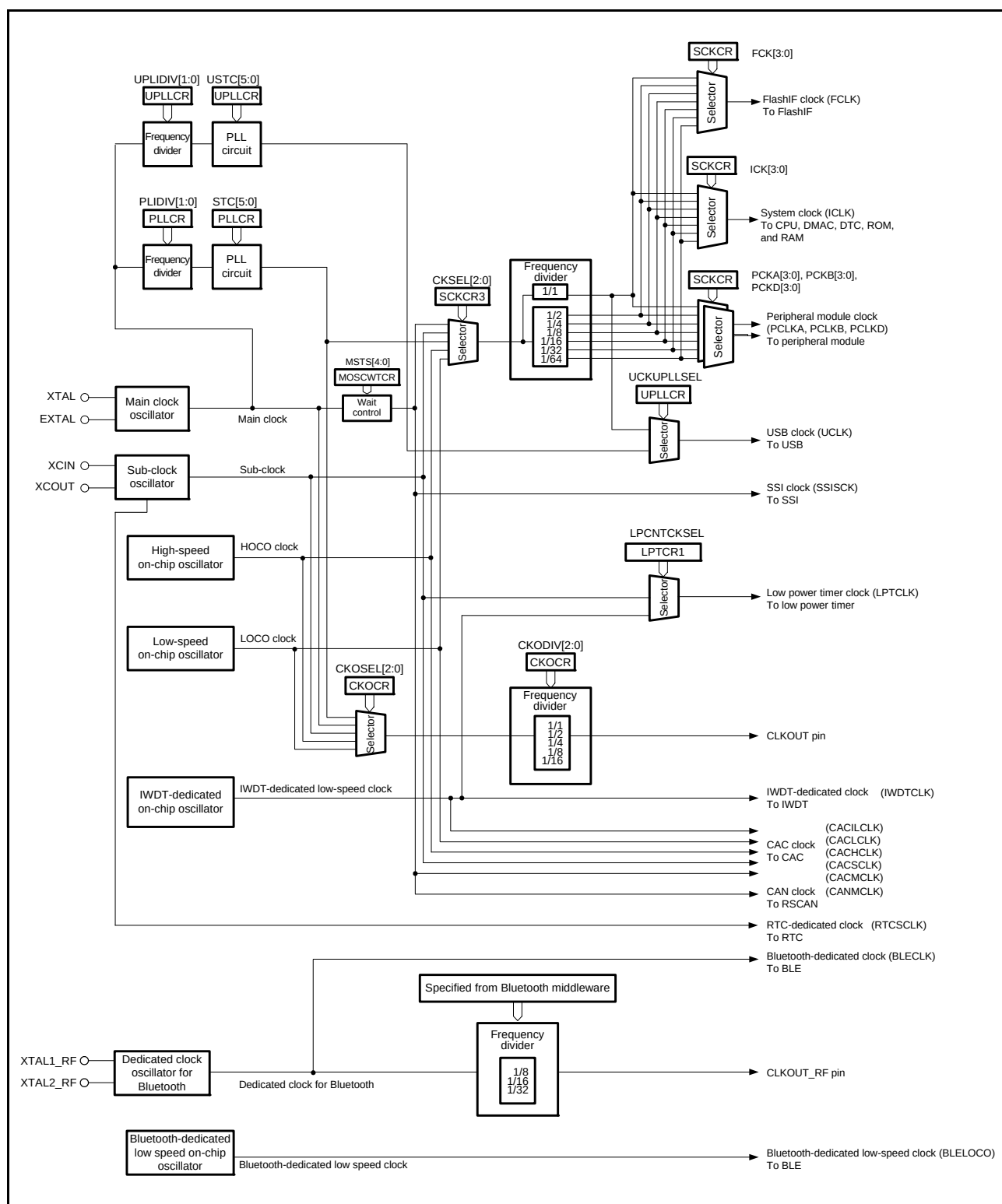


Figure 9.1 Block Diagram of Clock Generation Circuit (85-Pin BGA, 56-Pin QFN)

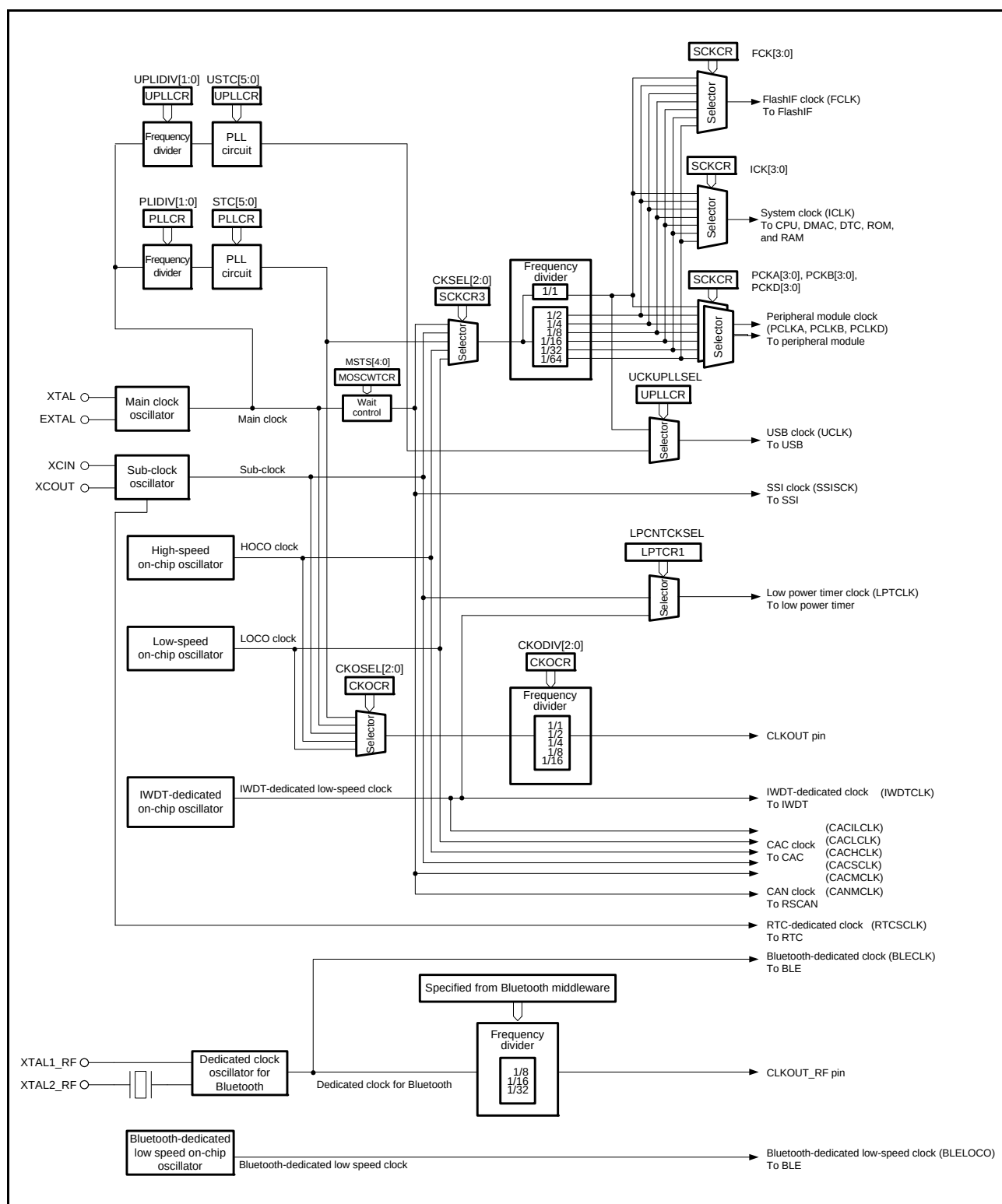


Figure 9.2 Block Diagram of Clock Generation Circuit (83-Pin LGA)

Table 9.2 lists the I/O pins of the clock generation circuit.

Table 9.2 I/O Pins of Clock Generation Circuit

Pin Name	I/O	Description
XTAL	Output	These pins are used to connect a crystal. The EXTAL pin can also be used to input an external clock. For details, refer to section 9.3.2, External Clock Input.
EXTAL	Input	
XCIN	Input	These pins are used to connect a 32.768-kHz crystal.
XCOU	Output	
CLKOUT	Output	Clock output pin
XTAL1_RF	Input	Connect a 32-MHz oscillator. The 83-pin LGA product incorporates a 32-MHz crystal.
XTAL2_RF	Output	
CLKOUT_RF	Output	Bluetooth-dedicated clock output pin

9.2 Register Descriptions

9.2.1 System Clock Control Register (SCKCR)

Address(es): 0008 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FCK[3:0]				ICK[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PCKA[3:0]				PCKB[3:0]				—	—	—	—	PCKD[3:0]			
Value after reset:	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PCKD[3:0]	Peripheral Module Clock D (PCLKD) Select	b3 b0 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	PCKB[3:0]	Peripheral Module Clock B (PCLKB) Select	b11 b8 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W
b15 to b12	PCKA[3:0]	Peripheral Module Clock A (PCLKA) Select	b15 b12 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W
b19 to b16	—	Reserved	Set the value to whichever is greater of the values of the ICK[3:0] and PCKB[3:0] bits.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b24	ICK[3:0] *1	System Clock (ICLK) Select	b27 b24 0 0 0 0: ×1 0 0 0 1: ×1/2 0 0 1 0: ×1/4 0 0 1 1: ×1/8 0 1 0 0: ×1/16 0 1 0 1: ×1/32 0 1 1 0: ×1/64 Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b28	FCK[3:0]	FlashIF Clock (FCLK) Select	b31b28 0000: ×1 0001: ×1/2 0010: ×1/4 0011: ×1/8 0100: ×1/16 0101: ×1/32 0110: ×1/64 Settings other than above are prohibited.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. Do not set the frequency division ratio of ICLK = 1 when a clock of frequency higher than 32 MHz is selected by the SCKCR3.CKSEL[2:0] bits and MEMWAIT.MEMWAIT = 0.

This register cannot be rewritten while the flash memory is being programmed or erased.

When an instruction for writing to SCKCR or SCKCR3 is to follow writing to the SCKCR register, do so in accord with the procedure below.

1. Write to the SCKCR register.
2. Confirm that the value has actually been written to the SCKCR register.
3. Proceed to the next step.

PCKD[3:0] Bits (Peripheral Module Clock D (PCLKD) Select)

These bits select the frequency of peripheral module clock D (PCLKD).

PCKB[3:0] Bits (Peripheral Module Clock B (PCLKB) Select)

These bits select the frequency of peripheral module clock B (PCLKB).

PCKA[3:0] Bits (Peripheral Module Clock A (PCLKA) Select)

These bits select the frequency of peripheral module clock A (PCLKA).

ICK[3:0] Bits (System Clock (ICLK) Select)

These bits select the frequency of the system clock (ICLK).

FCK[3:0] Bits (FlashIF Clock (FCLK) Select)

These bits select the frequency of the FlashIF clock (FCLK).

9.2.2 System Clock Control Register 3 (SCKCR3)

Address(es): 0008 0026h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	CKSEL[2:0]		—	—	—	—	—	—	—	—	—
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CKSEL[2:0] *1	Clock Source Select	b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. Do not select a clock of frequency higher than 32 MHz when divided by 1 is selected by SCKCR.ICK and MEMWAIT.MEMWAIT = 0.

This register cannot be rewritten while the flash memory is being programmed or erased.

CKSEL[2:0] Bits (Clock Source Select)

These bits select the source of the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, and PCLKD), FlashIF clock (FCLK), and USB clock (UCLK) from low-speed on-chip oscillator (LOCO), high-speed on-chip oscillator (HOCO), the main clock oscillator, the sub-clock oscillator, and the PLL circuit.

Transitions to clock sources which are not in operation are prohibited.

9.2.3 PLL Control Register (PLLCR)

Address(es): 0008 0028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—							—	—	—	—	—	—		
Value after reset:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select	b1 b0 0 0: ×1 0 1: ×1/2 1 0: ×1/4 1 1: Setting prohibited	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	STC[5:0]	Frequency Multiplication Factor Select	b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 Settings other than above are prohibited.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Writing to the PLLCR is prohibited when the PLLCR2.PLEN bit is 0 (PLL is operating).

PLIDIV[1:0] Bits (PLL Input Frequency Division Ratio Select)

These bits select the frequency division ratio of the PLL clock source.

Set these bits so that the frequency of PLL input signal is within the range of 4 MHz to 12.5 MHz.

STC[5:0] Bits (Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the PLL circuit.

Set these bits so that the PLL oscillation frequency is within the range of 24 MHz to 54 MHz.

9.2.4 PLL Control Register 2 (PLLCR2)

Address(es): 0008 002Ah

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	PLLEN
0	0	0	0	0	0	0	1

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	PLLEN	PLL Stop Control	0: PLL is operating. 1: PLL is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

PLLEN Bit (PLL Stop Control)

This bit runs or stops the PLL circuit.

After setting the PLLEN bit to 0 (PLL is operating), confirm that the OSCOVFSR.PLOVF bit is 1 before switching the system clock to the PLL clock.

That is, a fixed time for stabilization is required after the setting for PLL operation. A fixed time is also required for oscillation to stop after the setting to stop PLL operation. Accordingly, take note of the following limitations when starting and stopping PLL operation.

- After stopping the PLL, confirm that the OSCOVFSR.PLOVF bit is 0 before restarting the PLL.
- Confirm that the PLL is operating and that the OSCOVFSR.PLOVF bit is 1 before stopping the PLL.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.PLOVF bit is 1 before executing a WAIT instruction to place the MCU in software standby mode.
- After stopping the PLL, confirm that the OSCOVFSR.PLOVF bit is 0 and execute a WAIT instruction before entering software standby mode.

When the PLL clock is selected by the SCKCR3.CKSEL[2:0] bits, do not set the PLLEN bit (PLL is stopped) to 1.

When the external voltage (VCC) is below 2.4 V or low-speed operating mode is selected by the SOPCCR.SOPCM bit, do not set the PLLEN bit to 0 (PLL is operating).

9.2.5 USB-dedicated PLL Control Register (UPLLCR)

Address(es): 0008 002Ch

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—							—	—	—	UCKUPLSEL	—	—		UPLDIV[1:0]
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b1, b0	UPLDIV[1:0]	USB-dedicated PLL Input Frequency Division Ratio Select	b1 b0 0 0: $\times 1$ 0 1: $\times 1/2$ 1 0: $\times 1/4$ Settings other than above are prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	UCKUPLSEL	UCLK Source USB-Dedicated PLL Select	0: System clock is selected as UCLK 1: USB-dedicated PLL is selected as UCLK	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	USTC[5:0]	Frequency Multiplication Factor Select	b13 b8 0 0 0 1 1 1: $\times 4$ 0 0 1 0 1 1: $\times 6$ 0 0 1 1 1 1: $\times 8$ 0 1 0 1 1 1: $\times 12$ Settings other than above are prohibited.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Writing to the UPLLCR is prohibited when the UPLLCR2.UPLLEN bit is 0 (USB-dedicated PLL is operating).

UPLDIV[1:0] Bits (USB-dedicated PLL Input Frequency Division Ratio Select)

These bits select the input frequency division ratio of the USB-dedicated PLL clock source.

Set these bits so that the input frequency of the USB-dedicated PLL input is 4, 6, 8, 12 MHz.

UCKUPLSEL Bit (UCLK Source USB-Dedicated PLL Select)

This bit selects the USB-dedicated PLL clock. When this bit is set to 1, the USB-dedicated PLL (48 MHz) is supplied to the UCLK, and the clock of the oscillator (up to 54 MHz) selected by the SCKCR3.CKSEL[2:0] bits is supplied to the system clock.

When setting this bit to change the UCLK source clock, set the MSTPCRB.MSTPB19 bit (this module clock is disabled) and wait for at least three cycles of the clock before the change.

USTC[5:0] Bits (Frequency Multiplication Factor Select)

These bits select the frequency multiplication factor of the USB-dedicated PLL circuit.

Set these bits so that the USB-dedicated PLL oscillation frequency is 48 MHz.

9.2.6 USB-dedicated PLL Control Register 2 (UPLLCR2)

Address(es): 0008 002Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	UPLLEN
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	UPLLEN	USB-dedicated PLL Stop Control	0: USB-dedicated PLL is operating. 1: USB-dedicated PLL is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

The UPLLCR2 register runs or stops the USB-dedicated PLL circuit.

UPLLEN Bit (USB-dedicated PLL Stop Control)

This bit runs or stops the USB-dedicated PLL circuit.

After setting the UPLLEN bit to 0 (USB-dedicated PLL is operating), read the OSCOVFSR.UPLOVF flag to confirm that it has become 1, and then start using the USB-dedicated PLL clock.

That is, a fixed time for stabilization is required after the setting for USB-dedicated PLL operation. A fixed time is also required for oscillation to stop after the setting to stop USB-dedicated PLL operation. Accordingly, take note of the following limitations when starting and stopping USB-dedicated PLL operation.

- After stopping the USB-dedicated PLL, confirm that the OSCOVFSR.UPLOVF bit is 0 before restarting the USB-dedicated PLL.
- Confirm that the USB-dedicated PLL is operating and that the OSCOVFSR.UPLOVF bit is 1 before stopping the USB-dedicated PLL.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.UPLOVF bit is 1 before executing a WAIT instruction to place the MCU in software standby mode.
- After stopping the USB-dedicated PLL, confirm that the OSCOVFSR.UPLOVF bit is 0 and execute a WAIT instruction before entering software standby mode.

When the external voltage (VCC) is below 2.4 V or low-speed operating mode is selected by the SOPCCR.SOPCM bit, do not set the UPLLEN bit to 0 (USB-dedicated PLL is operating).

When the USB-dedicated PLL is selected by the UPLLCR.UCKUPLLSEL bit and the MSTPCRB.MSTPB19 bit is set to 0 (this module clock is enabled), do not set the UPLLEN bit to 1 (USB-dedicated PLL is stopped).

9.2.7 Main Clock Oscillator Control Register (MOSCCR)

Address(es): 0008 0032h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	MOSTP
0	0	0	0	0	0	0	1

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Main clock oscillator is operating. 1: Main clock oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Set this register after setting up the main clock oscillator wait control register.

MOSTP Bit (Main Clock Oscillator Stop)

This bit runs or stops the main clock oscillator.

After setting the MOSTP bit to 0 (main clock oscillator is operating), read the OSCOVFSR.MOOVF bit to confirm that it has become 1, and then use the main clock.

For the main clock oscillator, a fixed time is required for oscillation to become stable after the settings for operation have been made. Furthermore, a fixed time is required for oscillation to actually stop after the settings to stop oscillation have been made. Accordingly, take note of the following limitations when starting and stopping operation.

- After stopping the main clock oscillator, confirm that the OSCOVFSR.MOOVF bit is 0 before restarting the main clock oscillator.
- Confirm that the main clock oscillator is operating and that the OSCOVFSR.MOOVF bit is 1 before stopping the main clock oscillator.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.MOOVF bit is 1 and execute a WAIT instruction in order to operate the main clock oscillator and place the MCU in software standby mode.
- After stopping the main clock oscillator, confirm that the OSCOVFSR.MOOVF bit is 0 and execute a WAIT instruction before entering software standby mode.

Do not set the MOSTP bit to 1 when one of the following condition is met.

- When the main clock is selected as the clock source for the system clock (SCKCR3.CKSEL[2:0] = 010b)
- When the PLL clock is selected as the clock source for the system clock (SCKCR3.CKSEL[2:0] = 100b)
- When the PLL is operating (PLLCR2.PLEN = 0)
- When the USB-dedicated PLL is operating (UPLLCR2.PLEN = 0)

Do not set the MOSTP bit to 0 when the following condition is met.

- When low-speed operating mode is selected by the SOPCCR.SOPCM bit

9.2.8 Sub-Clock Oscillator Control Register (SOSCCR)

Address(es): 0008 0033h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	SOSTP
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	SOSTP	Sub-Clock Oscillator Stop	0: Sub-clock oscillator is operating. 1: Sub-clock oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

SOSTP Bit (Sub-Clock Oscillator Stop)

This bit runs or stops the sub-clock oscillator.

The SOSTP bit and the sub-clock oscillator control bit in RTC control register 3 (RCR3.RTCEN) controls whether to operate or stop the sub-clock oscillator. If one of these bits is set so as to enable the operation, the sub-clock oscillator runs.

When changing the value of the SOSTP bit or RCR3.RTCEN bit, execute subsequent instructions after reading the bit and checking that its value has actually been updated (refer to (2), Notes on writing to I/O registers, in section 5, I/O Registers).

After the setting of the SOSTP bit or the RCR3.RTCEN bit has been changed so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization time (t_{SUBOSC}) has elapsed.

That is, a fixed time for stabilization is required after the setting for sub-clock oscillator operation. A fixed time is also required for oscillation to stop after the setting to stop the oscillator. Accordingly, take note of the following limitations when starting and stopping the oscillator.

- When restarting the sub-clock oscillator after it has been stopped, allow at least five cycles of the sub-clock as an interval over which it is still stopped.
- Ensure that oscillation by the sub-clock oscillator is stable when making the setting to stop the sub-clock oscillator.
- Regardless of whether or not it is selected as the system clock, ensure that oscillation by the sub-clock oscillator is stable before executing a WAIT instruction to place the chip on software standby.
- When a transition to software standby mode is to follow the setting to stop the sub-clock oscillator, wait for at least two cycles of the sub-clock oscillator after the setting to stop the sub-clock oscillator and before executing the WAIT instruction.

While the sub-clock oscillator is selected by the SCKCR3.CKSEL[2:0] bits, do not set the SOSTP bit to 1 (sub-clock oscillator is stopped).

9.2.9 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): 0008 0034h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	LCSTP
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	LCSTP	LOCO Stop	0: LOCO is operating. 1: LOCO is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

LCSTP Bit (LOCO Stop)

This bit runs or stops the LOCO.

After the setting of the LCSTP bit has been changed so that the LOCO operates, only start using the LOCO clock after the LOCO clock oscillation stabilization time (t_{LOCO}) has elapsed.

That is, a fixed time for stabilization of oscillation is required after the setting for LOCO operation. A fixed time is also required for oscillation to stop after the setting to stop the oscillator. Accordingly, take note of the following limitations when starting and stopping the oscillator.

- When restarting the LOCO after it has been stopped, allow at least five cycles of the LOCO as an interval over which it is still stopped.
- Ensure that oscillation by the LOCO is stable when making the setting to stop the LOCO.
- Regardless of whether or not it is selected as the system clock, ensure that oscillation by the LOCO is stable before executing a WAIT instruction to place the chip on software standby.
- When a transition to software standby mode is to follow the setting to stop the LOCO, wait for at least three cycles of the LOCO after the setting to stop the LOCO and before executing the WAIT instruction.

While the LOCO is selected by the SCKCR3.CKSEL[2:0] bits, do not set the LCSTP bit to 1 (LOCO is stopped).

While low-speed operating mode is selected by the SOPCCR.SOPCM bit, do not set the LCSTP bit to 0 (LOCO is operating).

9.2.10 IWDT-Dedicated On-Chip Oscillator Control Register (ILOCOCR)

Address(es): 0008 0035h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	ILCSTP
0	0	0	0	0	0	0	1

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	ILCSTP	IWDT-Dedicated On-Chip Oscillator Stop	0: IWDT-dedicated on-chip oscillator is operating. 1: IWDT-dedicated on-chip oscillator is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

When the IWDT start mode select bit in option function select register 0 (OFS0.IWDTSTRT) is 0 (IWDT is operating), the setting of this register is invalid; it is valid only when the OFS0.IWDTSTRT bit is set to 1 (IWDT is stopped). The ILCSTP bit cannot be changed from 0 (IWDT-dedicated on-chip oscillator is operating) to 1 (IWDT-dedicated on-chip oscillator is stopped) while ILOCOCR is valid.

ILCSTP Bit (IWDT-Dedicated On-Chip Oscillator Stop)

This bit runs or stops the IWDT-dedicated on-chip oscillator.

After the setting of the ILCSTP bit has been changed so that the IWDT-dedicated on-chip oscillator operates, supply of the clock is started the MCU internally after a fixed time corresponding to the IWDT-dedicated clock oscillation stabilization time (t_{ILOCO}) has elapsed.

If the IWDT-dedicated clock is to be used, only start using the oscillator after this wait time has elapsed.

Ensure that oscillation by the IWDT-dedicated on-chip oscillator is stable before executing a WAIT instruction to place the chip on software standby mode.

9.2.11 High-Speed On-Chip Oscillator Control Register (HOCOOCR)

Address(es): 0008 0036h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	HCSTP
0	0	0	0	0	0	0	0/1 ^{*1}

Bit	Symbol	Bit Name	Description	R/W
b0	HCSTP	HOCO Stop	0: HOCO is operating. 1: HOCO is stopped.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. The HCSTP bit value after a reset is 0 when the HOCO oscillation enable bit in option function select register 1 (OFS1.HOCOEN) is 0. The HCSTP bit value after a reset is 1 when the OFS1.HOCOEN bit is 1.

HCSTP Bit (HOCO Stop)

This bit runs or stops the HOCO.

When changing the HCSTP bit from 1 to 0 (i.e. changing the HOCO clock from stopped to operating), confirm that the OSCOVFSR.HCOVF bit is 1 before switching the system clock to the HOCO clock.

That is, a fixed time for stabilization of oscillation is required after the setting for HOCO operation. A fixed time is also required for oscillation to stop after the setting to stop the oscillator. Accordingly, take note of the following limitations when starting and stopping the oscillator.

- After stopping the HOCO, confirm that the OSCOVFSR.HCOVF bit is 0 before restarting the HOCO.
- Confirm that the HOCO is operating and that the OSCOVFSR.HCOVF bit is 1 before stopping the HOCO.
- Regardless of whether or not it is selected as the system clock, confirm that the OSCOVFSR.HCOVF bit is 1 before executing a WAIT instruction to place the MCU in software standby mode.
- After stopping the HOCO, confirm that the OSCOVFSR.HCOVF bit is 0 and execute a WAIT instruction before entering software standby mode.

While the HOCO is selected by the SCKCR3.CKSEL[2:0] bits, do not set the HCSTP bit to 1 (HOCO is stopped).

While low-speed operating mode is selected by the SOPCCR.SOPCM bit, do not set the HCSTP bit to 0 (HOCO is operating).

9.2.12 High-Speed On-Chip Oscillator Control Register 2 (HOCOCR2)

Address(es): 0008 0037h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	HCFRQ[1:0]	
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HCFRQ[1:0]	HOCO Frequency Setting	b1 b0 0 0: 32 MHz 1 1: 54 MHz Settings other than above are prohibited.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

High-speed on-chip control register 2 is used to set operation of the high-speed on-chip oscillator.
When the HOCOCR.HCSTP bit is 0 (HOCO is operating), do not write to the HOCOCR2 register.

HCFRQ[1:0] Bits (HOCO Frequency Setting)

These bits set the frequency of the HOCO.

9.2.13 Oscillation Stabilization Flag Register (OSCOVFSR)

Address(es): 0008 003Ch

b7	b6	b5	b4	b3	b2	b1	b0
—	—	UPLOV F	—	HCOVF	PLOVF	—	MOOV F
Value after reset:	0	0	0	0	0/1*1	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MOOVF	Main Clock Oscillation Stabilization Flag	0: Main clock is stopped 1: Oscillation is stable and the clock can be used as the system clock*2	R
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	PLOVF	PLL Clock Oscillation Stabilization Flag	0: PLL is stopped or not stabilized 1: Oscillation is stable and the clock can be used as the system clock	R
b3	HCOVF	HOCO Clock Oscillation Stabilization Flag	0: HOCO is stopped or not stabilized 1: Oscillation is stable and the clock can be used as the system clock*2	R
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	UPLOVF	USB-Dedicated PLL Clock Oscillation Stabilization Flag	0: USB-dedicated PLL is stopped or not stabilized 1: Oscillation is stable and the clock can be used as the UCLK	R
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCOVF value after a reset is 1 when the HOCO oscillation enable bit in option function selection register 1 (OFS1.HOCOEN) is 0. The HCOVF value after a reset is 0 when the OFS1.HOCOEN bit is 1.

Note 2. When an appropriate value is set in the wait control register for each oscillator. If a set value (wait time) is not adequate, clock supply starts before oscillation becomes stable.

The OSCOVFSR register monitors whether oscillation of each oscillator has become stable.

If a wait control register is provided for each oscillator, specify a wait time that is longer than or equal to the stabilization time of the corresponding oscillation circuit.

MOOVF Flag (Main Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the main clock is stable.

[Setting condition]

- After the MOSCCR.MOSTP bit is set to 0 (main clock oscillator is operating) when the MOSTP bit is 1 (main clock oscillator is stopped), the corresponding time set in the MOSCWTCR register has elapsed and supply of the main clock is started to the MCU internally.

[Clearing condition]

- After the MOSCCR.MOSTP bit is set to 1, the processing to stop the oscillation of the main clock oscillator is completed.

PLOVF Flag (PLL Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the PLL clock is stable.

[Setting condition]

After the PLLCR2.PLEN is set to 0 (PLL is operating) when the PLEN bit is 1 (PLL is stopped), the MOOVF flag becomes 1, the PLL clock oscillation stabilization time (tPLL) has elapsed, and supply of the PLL clock is started to the MCU internally.

[Clearing condition]

After the PLLCR2.PLEN bit is set to 1, the processing to stop the oscillation of the PLL is completed.

HCOVF Flag (HOCO Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the HOCO clock is stable.

[Setting condition]

- After the HOCOCR.HCSTP bit is set to 0 (HOCO is operating) when the HCSTP bit is 1 (HOCO is stopped), supply of the HOCO clock is started to the MCU internally.

[Clearing condition]

- After the HOCOCR.HCSTP bit is set to 1, the processing to stop the oscillation of the HOCO is completed.

UPLOVF Flag (USB-Dedicated PLL Clock Oscillation Stabilization Flag)

This flag indicates whether oscillation of the USB-dedicated PLL clock is stable.

[Setting condition]

- After the UPLLCR2.UPLLEN bit is set to 0 (USB-dedicated PLL is operating) when the UPLLEN bit is 1 (USB-dedicated PLL is stopped), the MOOVF flag becomes 1 and the PLL clock stabilization wait time (tPLL) has elapsed, and then supply of the USB-dedicated PLL clock is started to the MCU internally.

[Clearing condition]

- After the UPLLCR2.UPLLEN bit is set to 1, the processing to stop the oscillation of the USB-dedicated PLL clock is completed.

9.2.14 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): 0008 0040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: The oscillation stop detection interrupt is disabled. Oscillation stop detection is not notified to the POE. 1: The oscillation stop detection interrupt is enabled. Oscillation stop detection is notified to the POE.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Oscillation stop detection function is disabled. 1: Oscillation stop detection function is enabled.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

OSTDIE Bit (Oscillation Stop Detection Interrupt Enable)

If the oscillation stop detection flag in the oscillation stop detection status register (OSTDSR.OSTDF) requires clearing, do this after setting the OSTDIE bit to 0. Wait for at least two cycles of PCLKB before again setting the OSTDIE bit to 1. According to the number of cycles for access to read a given I/O register, wait time longer than two cycles of PCLKB may have to be secured.

OSTDE Bit (Oscillation Stop Detection Function Enable)

This bit enables or disables the oscillation stop detection function.

When the OSTDE bit is 1 (oscillation stop detection function enabled), the LOCO stop bit (LOCOCR.LCSTP) is set to 0 and the LOCO operation is started. The LOCO cannot be stopped while the oscillation stop detection function is enabled; writing 1 (LOCO is stopped) to the LOCOCR.LCSTP bit is invalid.

When the oscillation stop detection flag in the oscillation stop detection status register (OSTDSR.OSTDF) is 1 (main clock oscillation stop has been detected), writing 0 to the OSTDE bit is invalid.

When the OSTDE bit is 1, a transition cannot be made to software standby mode. To make a transition to software standby mode, execute the WAIT instruction with the OSTDE bit being 0.

9.2.15 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): 0008 0041h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	OSTDF
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: The main clock oscillation stop has not been detected. 1: The main clock oscillation stop has been detected.	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0 and cannot be modified.	R

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. This bit can only be set to 0.

OSTDF Flag (Oscillation Stop Detection Flag)

This bit is a flag to indicate the main clock status. When the OSTDF flag is 1, it indicates that the main clock oscillation stop has been detected.

Once the main clock oscillation stop is detected, the OSTDF flag is not set to 0 even though the main clock oscillation is restarted. The OSTDF flag is set to 0 by reading 1 from the bit and then writing 0. At least three ICLK cycles of wait time is necessary between writing 0 to the OSTDF flag and reading the OSTDF flag as 0. If the OSTDF flag is set to 0 while the main clock oscillation is stopped, the OSTDF flag becomes 0 and then returns to 1.

When the main clock oscillator (010b) or PLL (100b) is selected by the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]), the OSTDF flag cannot be modified to 0. The OSTDF flag should be set to 0 after switching the clock source to a source other than the main clock oscillator and the PLL.

[Setting condition]

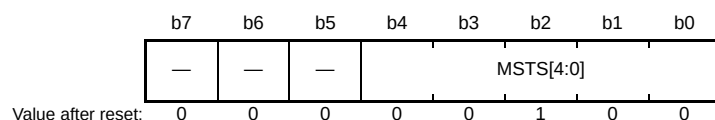
- The main clock oscillation is stopped with the OSTDCR.OSTDE bit being 1 (oscillation stop detection function enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKCR3.CKSEL[2:0] bits are neither 010b nor 100b.

9.2.16 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): 0008 00A2h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	MSTS[4:0]	Main Clock Oscillator Wait Time	b4 b0 0 0 0 0: Wait time = 2 cycles (0.5 μ s) 0 0 0 1: Wait time = 1024 cycles (256 μ s) 0 0 1 0: Wait time = 2048 cycles (512 μ s) 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 1 1 1: Wait time = 65536 cycles (16.384 ms) Settings other than above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 μ s, TYP.)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

MSTS[4:0] Bits (Main Clock Oscillator Wait Time)

Set these bits to select the oscillation stabilization wait time of the main clock oscillator.

Set the main clock oscillation stabilization time to longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is externally input, set these bits to 00000b because the oscillation stabilization time is not required.

The wait time set by the MSTS[4:0] bits is counted using the LOCO clock. The LOCO automatically oscillates when necessary, regardless of the value of the LOCOCR.LCSTP bit.

After the set wait time has elapsed, supply of the main clock is started to the MCU internally and the OSCOVFSR.MOOVF flag becomes 1. If the set wait time is short, supply of the main clock is started before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCOVFSR.MOOVF flag is 0. Do not rewrite this register under any other conditions.

9.2.17 CLKOUT Output Control Register (CKOCR)

Address(es): 0008 003Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CKOSTP	CKODIV[2:0]			CKOSEL[3:0]				—	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	CKOSEL[3:0]	CLKOUT Output Source Select	b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock oscillator 0 0 1 1: Sub-clock oscillator 0 1 0 0: PLL Settings other than above are prohibited.	R/W
b14 to b12	CKODIV[2:0]	CLKOUT Output Division Ratio Select	b14 b2 0 0 0: No division 0 0 1: $\times 1/2$ 0 1 0: $\times 1/4$ 0 1 1: $\times 1/8$ 1 0 0: $\times 1/16$ Settings other than above are prohibited.	R/W
b15	CKOSTP	CLKOUT Output Stop Control	0: CLKOUT pin output enabled*1 1: CLKOUT pin output disabled (always output the low level)	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. It is also necessary to set the pin function control register and port mode register for the corresponding pin.

CKOSEL[3:0] Bits (CLKOUT Output Source Select)

Set these bits to select the LOCO clock, HOCO clock, main clock, sub-clock, or PLL as the source of the clock to be output from the CLKOUT pin.

CKODIV[2:0] Bits (CLKOUT Output Division Ratio Select)

Set these bits to select the division ratio of the clock selected by the CKOSEL[3:0] bits.

Set the CKOSTP bit to 1 when changing the division ratio.

The division ratio of the output clock frequency should be set to no higher than 8 MHz when VCC is 2.7 V or above, and no higher than 4 MHz when VCC is below 2.7 V.

For details on the characteristics of the clock output from the CLKOUT pin, see Table 51.46, Timing of CLKOUT_RF.

CKOSTP Bit (CLKOUT Output Stop Control)

Set this bit to enable or disable output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, a low level is output.

If the CKOSTP bit is rewritten while the clock is still oscillating, a glitch may be generated in the output.

9.2.18 Main Clock Oscillator Forced Oscillation Control Register (MOFCR)

Address(es): 0008 C293h

b7	b6	b5	b4	b3	b2	b1	b0
—	MOSEL	MODRV21	—	—	—	—	—
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	MODRV21	Main Clock Oscillator Drive Capability Switch	VCC ≥ 2.4 V 0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited	R/W
b6	MOSEL	Main Clock Oscillator Switch	0: Resonator 1: External oscillator input	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The EXTAL/XTAL pin is also used as a port. In the initial setting state, the pin is set as a port.

MODRV21 Bit (Main Clock Oscillator Drive Capability Switch)

These bits select the drive capability of the main clock oscillator.

MOSEL Bit (Main Clock Oscillator Switch)

This bit selects the oscillation source of the main clock oscillator.

9.2.19 Memory Wait Cycle Setting Register (MEMWAIT)

Address(es): 0008 0031h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	MEMWAIT
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	MEMWAIT	Memory Wait Cycle Setting*1	0: No wait states 1: Wait states	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. Do not select the MEMWAIT bit = 0 (no wait states) when divided by 1 is selected by the SCKCR.ICK[3:0] bits and a clock of frequency is higher than 32 MHz is selected as the system clock (ICKL) by the SCKCR3.CKSEL[2:0] bits. When a clock of frequency is lower than 32 MHz is selected as the ICLK, it is not necessary to set the MEMWAIT bit to 1 (wait states).

The MEMWAIT register is used to control the wait cycle of the ROM.

MEMWAIT Bit (Memory Wait Cycle Setting)

This bit is used to set the wait cycle of the ROM.

This bit is set to “no wait states” immediately after a reset.

When selecting a clock of frequency higher than 32 MHz as the system clock (ICKL), set the bit to 1 (wait states).

When setting the MEMWAIT bit to 1 (wait states), make sure that high-speed mode is selected. After the value of the MEMWAIT bit is changed to 1, change the system clock to a clock of frequency higher than 32 MHz.

When setting the MEMWAIT bit to 0 (no wait states), make sure that the frequency of the system clock (ICKL) is 32 MHz or lower. When changing the operating power control state, make sure that the value of the MEMWAIT bit is changed to 0.

Table 9.3 lists the restrictions on setting the MEMWAIT bit, and Figure 9.3 and Figure 9.4 show the procedure for changing the MEMWAIT bit.

Table 9.3 Restrictions on Setting the MEMWAIT Bit

MEMWAIT Bit	Operating Power Control State			
	High-Speed Operating Mode		Middle-Speed Operating Mode	Low-Speed Operating Mode
	ICKL ≤ 32 MHz	ICKL > 32 MHz		
0	Can be set	Cannot be set	Can be set	Can be set
1	Can be set	Can be set	Cannot be set	Cannot be set

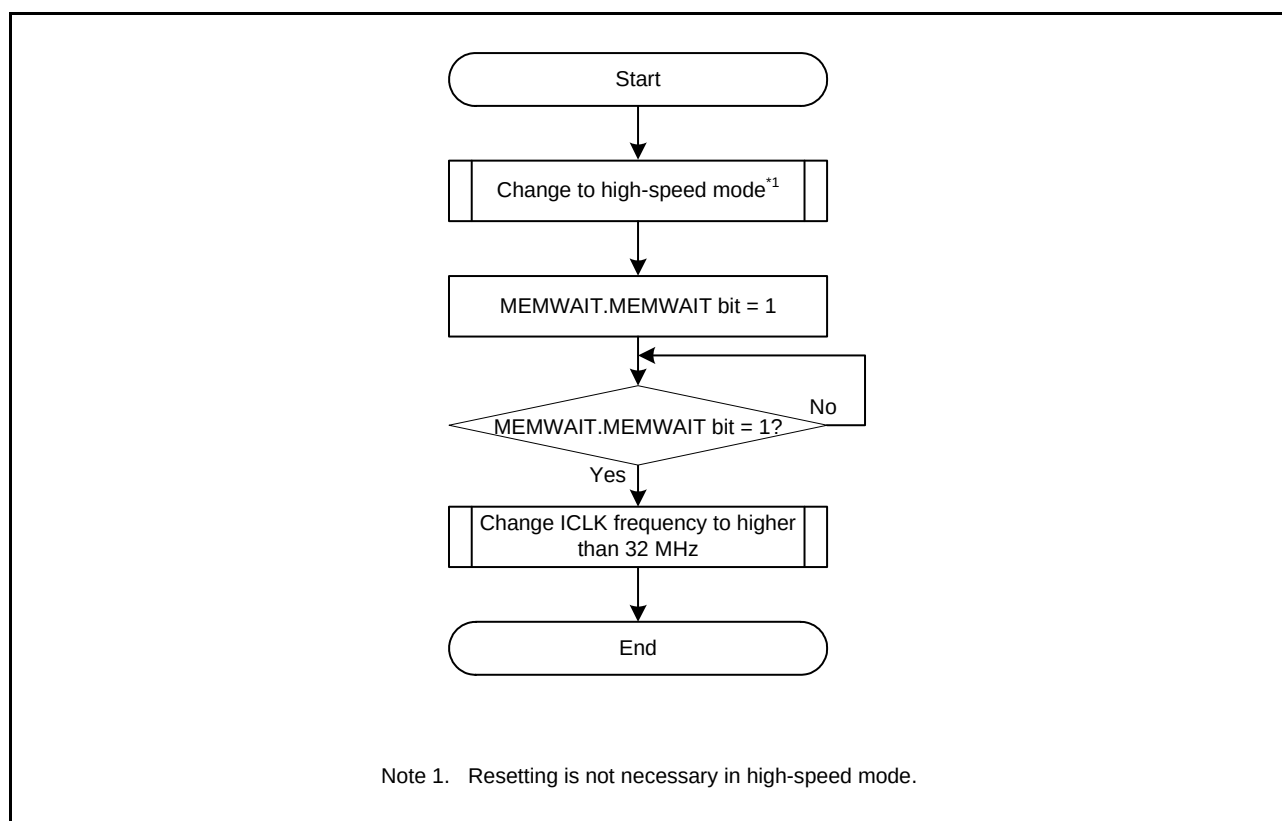


Figure 9.3 Example of MEMWAIT Bit Setting Procedure When Changing ICLK Frequency to Higher than 32 MHz

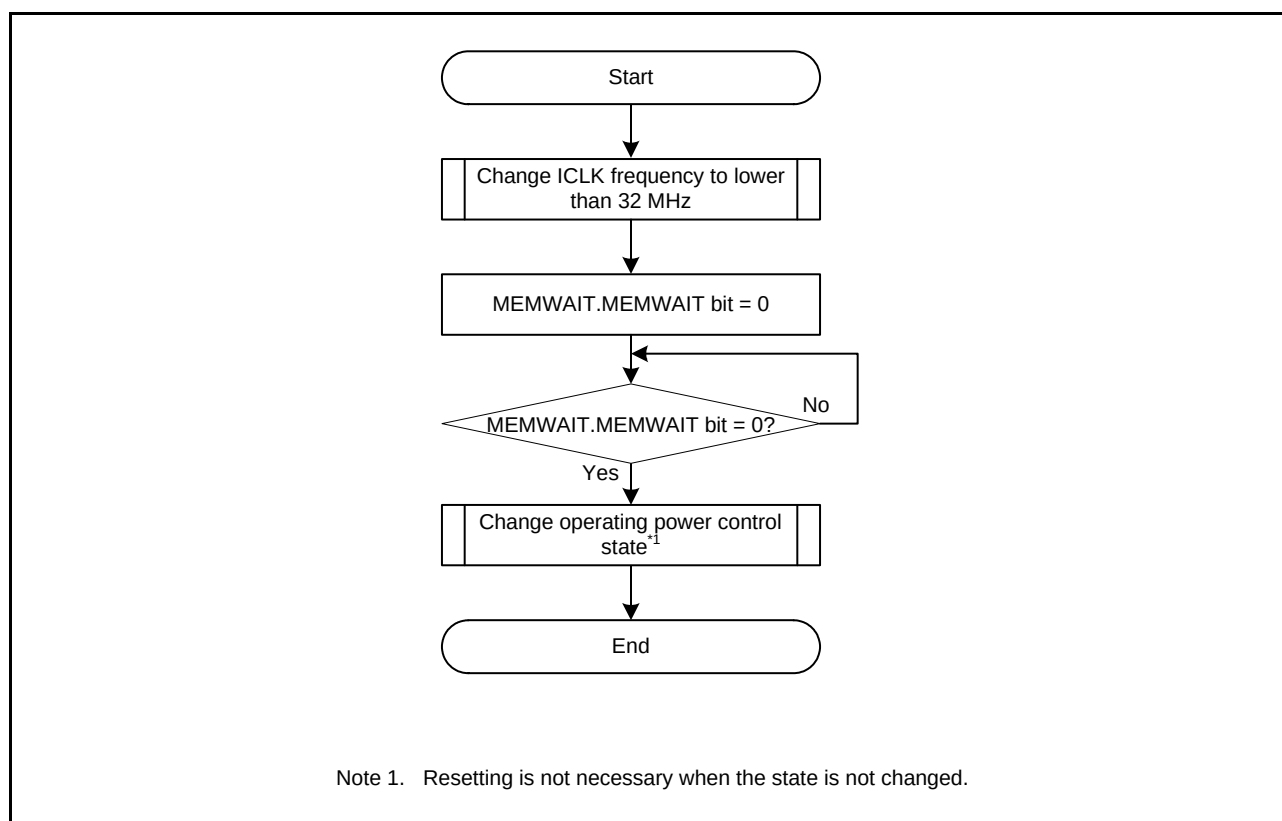
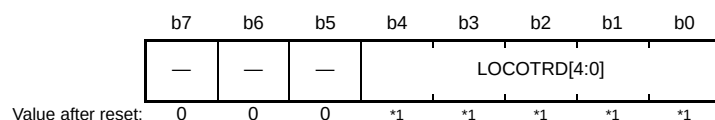


Figure 9.4 Example of MEMWAIT Bit Setting Procedure When Changing ICLK Frequency to Lower than 32 MHz

9.2.20 Low-Speed On-Chip Oscillator Trimming Register (LOCOTRR)

Address(es): 0008 0060h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	LOCOTRD[4:0]	Low-Speed On-Chip Oscillator Frequency Adjustment	b4 b0 1 0 0 0 0: -16 (Frequency: Low) 1 0 0 0 1: -15 : 0 1 1 1 0: 14 0 1 1 1 1: 15 (Frequency: High)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. Chip-specific value

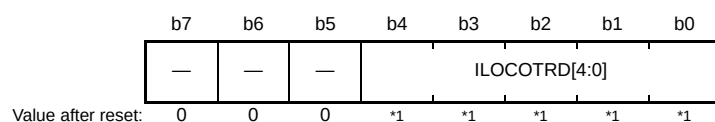
LOCOTRD[4:0] Bits (Low-Speed On-Chip Oscillator Frequency Adjustment)

Set the frequency adjustment value for the low-speed on-chip oscillator.

The setting range is -16 (10h) to 15 (0Fh) by two's complements. The greater the set value is, the higher the frequency is. The frequency is adjusted under certain conditions before shipment, so the value after reset varies with the chip. After a reset, the oscillation frequency returns to the factory default.

9.2.21 IWDTC-Dedicated On-Chip Oscillator Trimming Register (ILOCOTRR)

Address(es): 0008 0064h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	ILOCOTRD[4:0]	IWDTC-Dedicated On-Chip Oscillator Frequency Adjustment	b4 b0 0 0 0 0 0: 0 (Frequency: Low) 0 0 0 0 1: 1 : 1 1 1 1 0: 30 1 1 1 1 1: 31 (Frequency: High)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. Chip-specific value

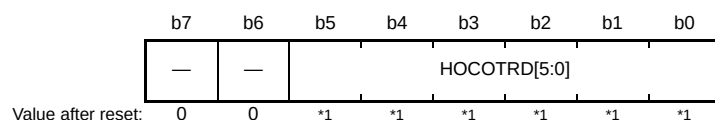
ILOCOTRD[4:0] Bits (IWDTC-Dedicated On-Chip Oscillator Frequency Adjustment)

Set the frequency adjustment value for the IWDTC-dedicated on-chip oscillator.

The setting range is from 0 (00h) to 31 (1Fh) by binary numbers. The greater the set value is, the higher the frequency is. The frequency is adjusted under certain conditions before shipment, so the value after reset varies with the chip. After a reset, the oscillation frequency returns to the factory default.

9.2.22 High-Speed On-Chip Oscillator Trimming Register n (HOCOTRRn) (n = 0, 3)

Address(es): HOCOTRR0 0008 0068h, HOCOTRR3 0008 006Bh



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	HOCOTRD[5:0]	High-Speed On-Chip Oscillator Frequency Adjustment	b5 b0 0 0 0 0 0: 0 (Frequency: Low) 0 0 0 0 1: 1 : 1 1 1 1 0: 62 1 1 1 1 1: 63 (Frequency: High)	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC0 bit to 1 (write enabled) before rewriting this register.

Note 1. Chip-specific value

HOCOTRR0 corresponds to 32 MHz, and HOCOTRR3 corresponds to 54 MHz.

HOCOTRD[5:0] Bits (High-Speed On-Chip Oscillator Frequency Adjustment)

Set the frequency adjustment value for the high-speed on-chip oscillator.

The setting range is from 0 (00h) to 63 (3Fh) by binary numbers. The greater the set value is, the higher the frequency is.

The frequency is adjusted under certain conditions before shipment, so the value after reset varies with the chip. After a reset, the oscillation frequency returns to the factory default.

9.3 Main Clock Oscillator

There are two ways of supplying the clock signal from the main clock oscillator: connecting an oscillator or the input of an external clock signal.

9.3.1 Connecting a Crystal

Figure 9.5 shows an example of connecting a crystal.

A damping resistor (R_d) should be added, if necessary. Since the resistor values vary depending on the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If use of an external feedback resistor (R_f) is directed by the resonator manufacturer, insert an R_f between EXTAL and XTAL by following the instruction.

When connecting a resonator to supply the clock, the frequency of the resonator should be in the frequency range of the resonator for the main clock oscillator described in Table 9.1.

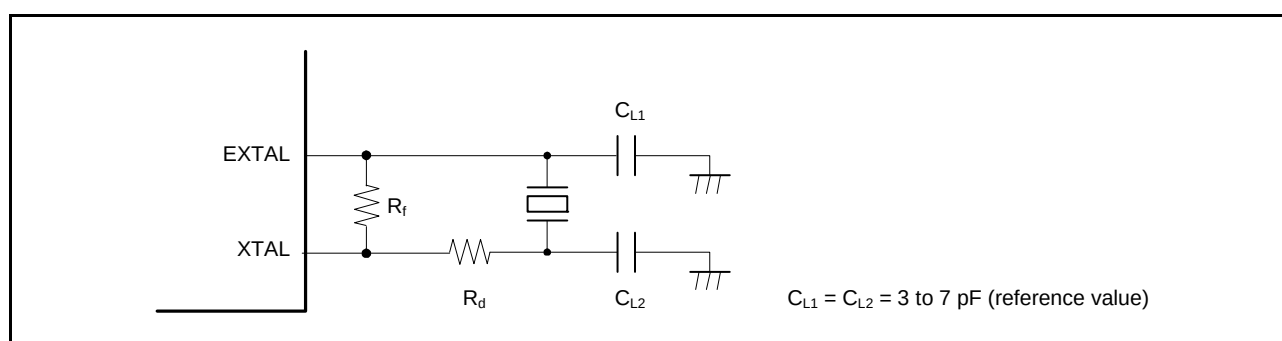


Figure 9.5 Example of Crystal Connection

Table 9.4 Damping Resistance (Reference Values)

Frequency (MHz)	2	8	16	20
R_d (Ω)	0	0	0	0

Figure 9.6 shows an equivalent circuit of the crystal. Use a crystal that has the characteristics shown in Table 9.5 as a reference.

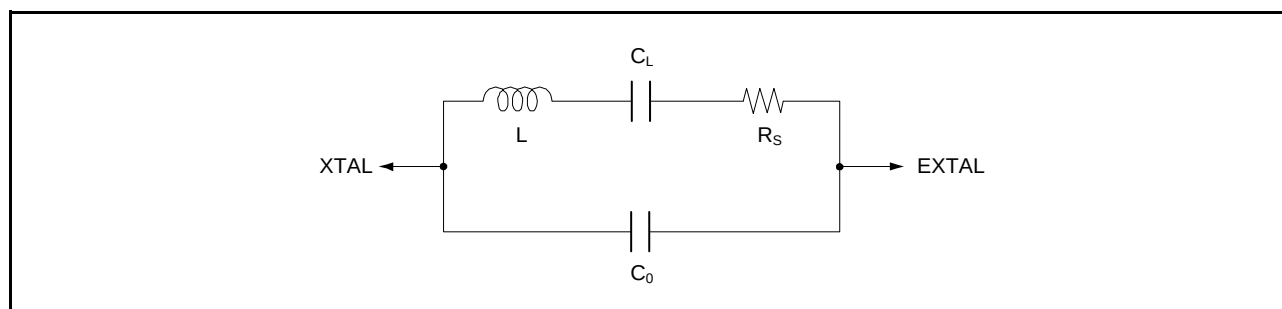


Figure 9.6 Equivalent Circuit of Crystal

Table 9.5 Crystal Characteristics (Reference Values)

Frequency (MHz)	8	12	16
R_S max (Ω)	200	120	56
C_0 max (pF)	1.3	1.3	1.4

9.3.2 External Clock Input

Figure 9.7 shows connection of an external clock. If operation is to be driven by an external clock, set the MOFCR.MOSEL bit to 1 and leave the XTAL pin open-circuit.

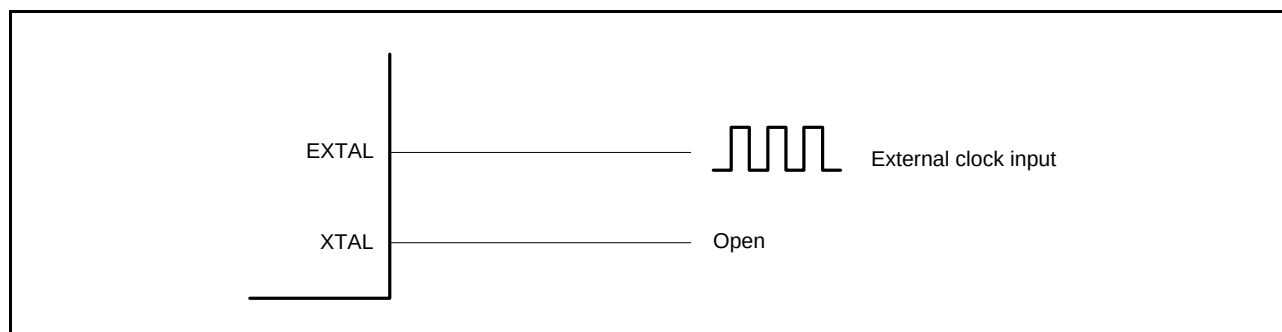


Figure 9.7 Connection Example of External Clock

9.3.3 Handling of Pins When the Main Clock is Not Used

For details on pin handling when the main clock is not used, refer to section 21.5, Handling of Unused Pins.

9.3.4 Notes on the External Clock Input

The frequency of the external clock input can only be changed while the main clock oscillator is stopped. Do not change the frequency of the external clock input while the setting of the main clock oscillator stop bit (MOSCCR.MOSTP) is 0 (main clock oscillator is operating).

9.4 Sub-Clock Oscillator

The only way of supplying the clock signal from the sub-clock oscillator is connecting a crystal.

9.4.1 Connecting 32.768-kHz Crystal

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal, as shown in Figure 9.8.

A damping resistor R_d should be added, if necessary. Since the resistor values vary depending on the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If use of an external feedback resistor (R_f) is directed by the resonator manufacturer, insert an R_f between XCIN and XCOU by following the instruction. When connecting a resonator to supply the clock, the frequency of the resonator should be in the frequency range of the resonator for the sub-clock oscillator described in Table 9.1.

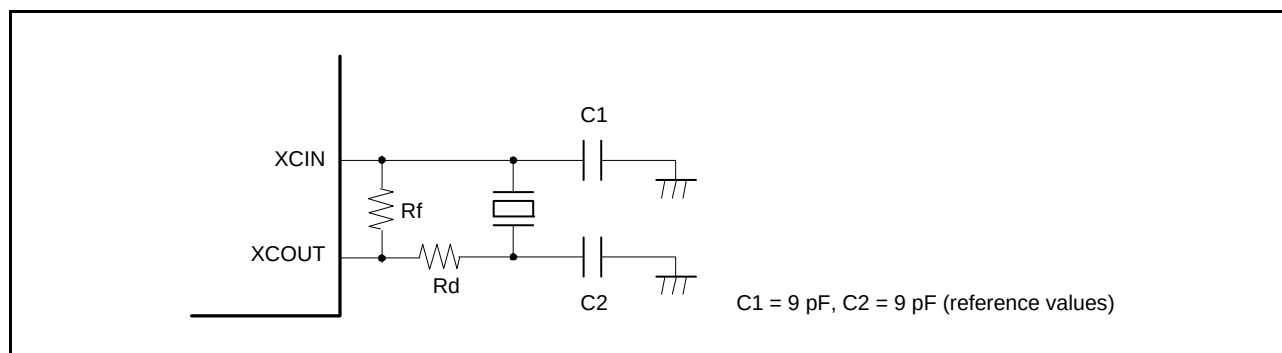


Figure 9.8 Connection Example of 32.768-kHz Crystal

Figure 9.9 shows an equivalent circuit for the 32.768-kHz crystal. Use a crystal that has the characteristics listed in Table 9.6.

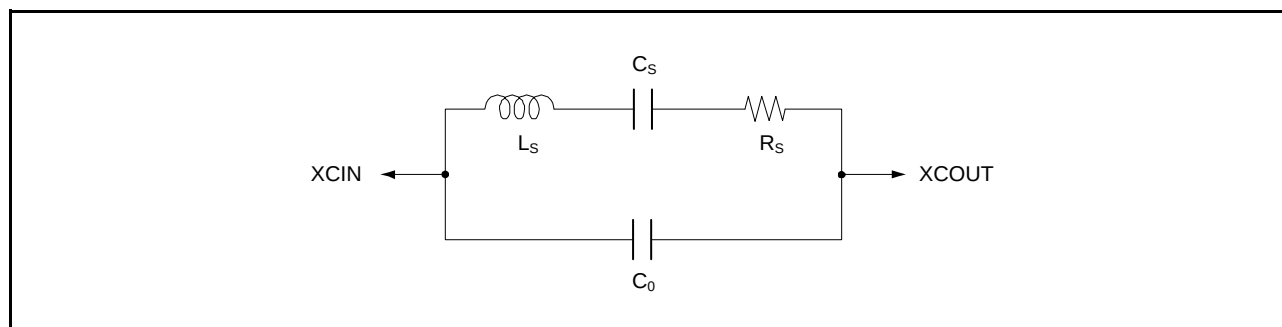


Figure 9.9 Equivalent Circuit for Crystal

Table 9.6 Crystal Characteristics (Reference Values)

Frequency (kHz)	32.768 (Low CL)
R_s max (k Ω)	37
C_0 max (pF)	0.9

9.4.2 Handling of Pins When Sub-Clock is Not Used

If the sub-clock is not in use, connect the XCIN pin to VSS via a resistor (to pull VSS down) and leave the XCOU pin open-circuit as shown in Figure 9.10.

In addition, if an oscillator is not connected, set the sub-clock oscillator stop bit (SOSCCR.SOSTP) to 1 (stopping the oscillator) and the sub-clock oscillator control bit in RTC control register 3 (RCR3.RTCEN) to 0 (stopping the sub-clock oscillator). The value of some RTC registers related to the sub-clock will be undefined after a cold start. Accordingly, be sure to set these bits after a cold start.

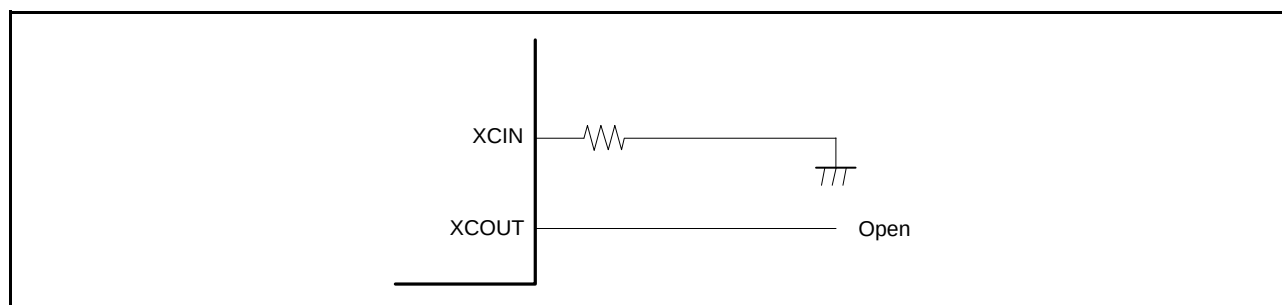


Figure 9.10 Pin Handling when Sub-Clock is Not Used

9.5 Dedicated Clock Oscillator for Bluetooth

In the case of the 85-pin BGA and 56-pin QFN products, operating Bluetooth requires connection to the 32-MHz clock oscillator. The 83-pin LGA product does not require the connection of a resonator because the package includes a 32-MHz crystal resonator. Note that handling of the XTAL1_RF and XTAL2_RF pins of the 83-pin LGA package product differs from that of the other products in that these pins should be externally connected to each other rather than to a resonator.

9.5.1 Connecting the Oscillator

An example of connection of the oscillator is shown in Figure 9.11.

In the case of the 85-pin BGA and 56-pin QFN package products, insert a damping resistor (R_d) as required. Set the resistance to the value recommended by the oscillator manufacturer as the value depends on the oscillator and its driving capability. If the oscillator manufacturer states that the addition of a feedback resistor (R_f) to the oscillator is required, insert R_f between XTAL1_RF and XTAL2_RF according to the instructions.

In the case of an 83-pin LGA package product, XTAL1_RF and XTAL2_RF should be externally connected to each other.

To control the oscillator, use the Bluetooth middleware provided by Renesas. The Bluetooth middleware is also able to control the settings of the on-chip variable capacitors, CL1 and CL2, to adjust the frequency of oscillation. Adjustment of the frequency of the Bluetooth-dedicated clock oscillator is explained in the application note Procedure for Adjusting the Frequency of the Bluetooth-Dedicated Clock Oscillator (R01AN4762). Obtain the latest version of this document from the Renesas website.

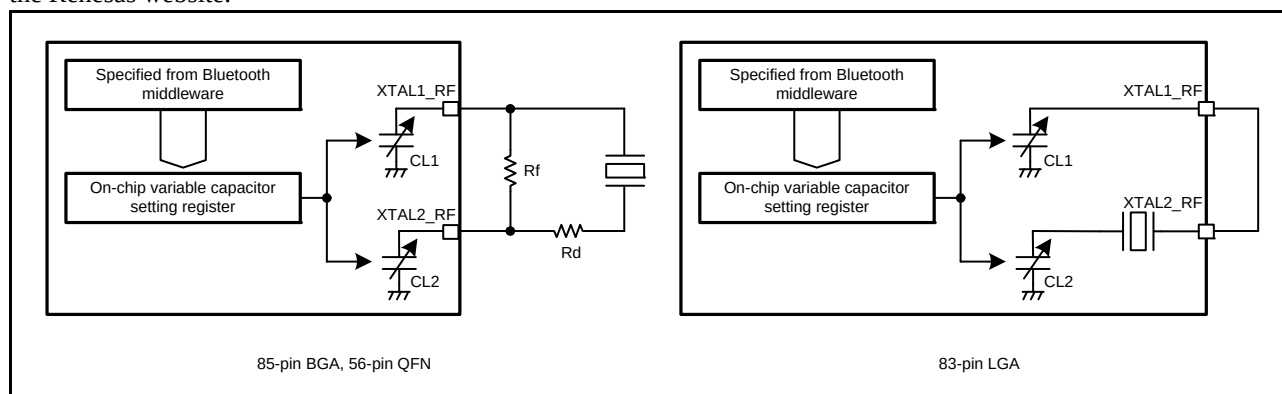


Figure 9.11 Example of the Connection of a 32-MHz Crystal Resonator

9.5.2 Connecting the Bluetooth-Dedicated Clock Output Pin

When the Bluetooth middleware sets up the clock output and the BLE shifts from waiting mode to RF power-down mode, the frequency-divided clock for the Bluetooth-dedicated clock is output. If the BLE subsequently shifts to RF low-power mode, the RF clock output is disabled. The Bluetooth middleware is able to specify the frequency-divisor for the Bluetooth-dedicated clock.

The Bluetooth-dedicated clock output can also be used as the input of the external clock for the main clock oscillator by externally connecting the CLKOUT_RF and EXTAL pins on the board. Figure 9.11 shows an example of a configuration where the Bluetooth-dedicated clock output is used as the input of the external clock for the main clock oscillator.

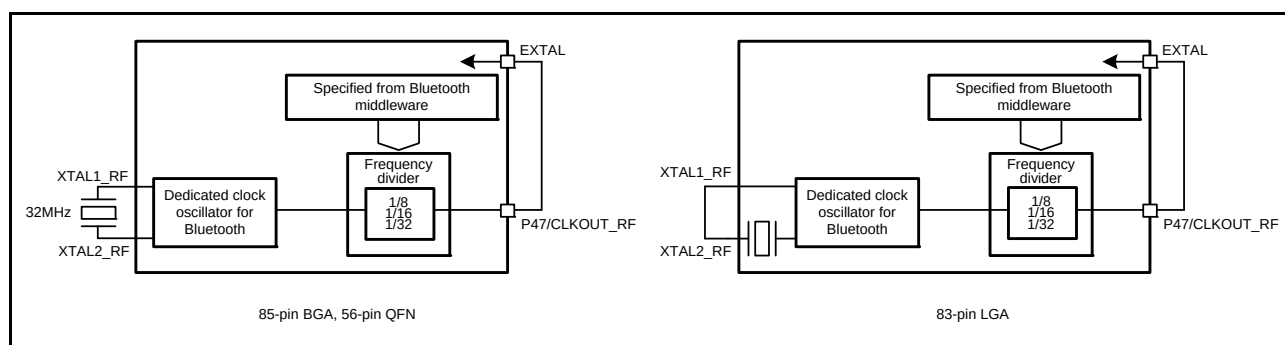


Figure 9.12 Example of Connection of the Bluetooth-dedicated clock output pin

9.6 Oscillation Stop Detection Function

9.6.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function is used to detect the main clock oscillator stop and to supply LOCO clock pulses from the low-speed on-chip oscillator as the system clock source instead of the main clock.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the MTU output can be forcedly driven to the high-impedance on the detection. For details, refer to section 23, Multi-Function Timer Pulse Unit 2 (MTU2a) and section 24, Port Output Enable 2 (POE2a).

In the MCU, the main clock oscillation stop is detected when the input clock remains to be 0 or 1 for a certain period, for example, due to a malfunction of the main clock oscillator (refer to section 51, Electrical Characteristics).

When an oscillation stop is detected, the main clock selected by the clock source select bits (SCKCR3.CKSEL[2:0]) is switched to the LOCO clock by the corresponding selectors in the former stage. Therefore, if an oscillation stop is detected with the main clock selected as the system clock source, the system clock source is switched to the LOCO clock without a change of CKSEL[2:0].

If an oscillation stop is detected while the PLL clock is selected by the clock source select bits (SCKCR3.CKSEL[2:0]) in system clock control register 3, the SCKCR3.CKSEL[2:0] bit value does not change and the PLL clock remains the system clock source. However, the frequency becomes a free-running oscillation frequency.

Also, if an oscillation stop is detected while the USB-dedicated PLL clock is selected by the UPLLCR.UCKPLLSEL bit, the set value of these bits does not change and the USB-dedicated PLL clock remains the UCLK clock source. However, the frequency becomes a free-running oscillation frequency.

Switching between the main clock and LOCO clock is controlled by the oscillation stop detection flag (OSTDSR.OSTDF). The clock source is switched to the LOCO clock when the OSTDF flag is 1, and is switched to the main clock again when the OSTDF flag is set to 0. At this time, if the main clock or PLL clock is selected with the CKSEL[2:0] bits, the OSTDF flag cannot be set to 0. To switch the clock source to the main clock or PLL clock again after the oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock or PLL clock and set the OSTDF flag to 0. After that, check that the OSTDF flag is not 1, and then set the CKSEL[2:0] bits to the main clock or PLL clock after the specified oscillation stabilization time has elapsed.

After a reset is released, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after a specified oscillation stabilization time has elapsed.

The oscillation stop detection function is provided against the main clock stop by an external cause. Therefore, the oscillation stop detection function should be disabled before the main clock oscillator is stopped by the software or a transition is made to software standby mode.

When the system clock with the main clock selected as the system clock source, CAC main clock (CACMCLK), SSI clock (SSISCK), and CAN clock (CANMCLK) are selected, these clocks are switched to the LOCO clock by the oscillation stop detection. The system clock (ICLK) frequency during the LOCO clock operation is specified by the LOCO oscillation frequency and the division ratio set by the system clock (ICLK) select bits (SCKCR.ICK[3:0]).

When the PLL clock is selected as the system clock source and the USB-dedicated PLL clock is selected as the UCLK source, these clocks operate at the PLL free-running frequency by the oscillation stop detection.

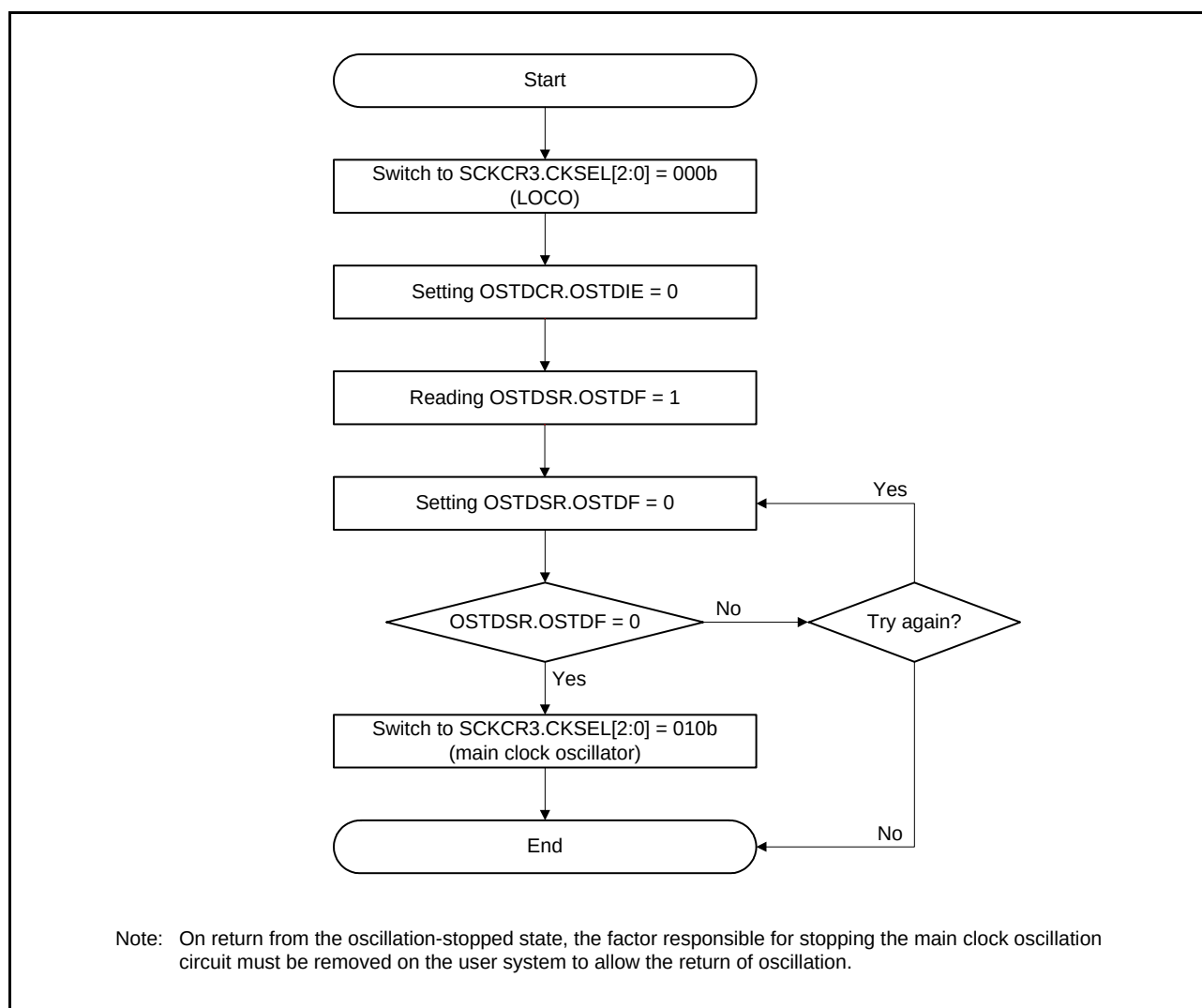


Figure 9.13 Flow of Recovery from Detection of Oscillator Stop

9.6.2 Oscillation Stop Detection Interrupts

The main clock oscillator stop is notified to port output enable 23 (POE) if the oscillation-stop detection flag (OSTDSR.OSTDF) becomes 1 while the oscillation-stop detection interrupt enable bit (OSTDCR.OSTDIE) is 1 (oscillation stop detection interrupt enabled). On accepting the notification of the oscillation stop, the POE sets the OSTST high-impedance flag in input level control/status register 3 (ICSR3.OSTSTF) to 1. After the oscillation stop is detected, wait for at least 10 cycles of PCLK before writing to this ICSR3.OSTSTF flag. When the OSTDSR.OSTDF flag requires clearing, do so setting the oscillation stop detection interrupt enable bit (OSTDCR.OSTDIE) to 0. Wait for at least two cycles of PCLKB clock before again setting the OSTDCR.OSTDIE bit to 1. According to the number of cycles for access to read a given I/O register, wait time longer than two cycles of PCLKB may have to be secured. The oscillation stop detection interrupt is a non-maskable interrupt. Since non-maskable interrupts are disabled in the initial state after a reset release, enable the non-maskable interrupts by the software before using oscillation stop detection interrupts. For details, refer to section 15, Interrupt Controller (ICUb).

When the PLL detects an oscillation stop and is running at its own oscillation frequency, this indicates the occurrence of some system failure. An emergency measure should be taken to handle the failure.

9.7 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

9.8 Internal Clock

Clock sources of internal clock signals are the main clock, sub-clock, HOCO clock, LOCO clock, PLL clock, USB-dedicated PLL clock, and dedicated low-speed clock for the IWDT. The internal clocks listed below are produced from these sources.

- (1) Operating clock of the CPU, DMAC, DTC, ROM, and RAM: System clock (ICLK)
- (2) Operating clock of peripheral modules: Peripheral module clock (PCLKA, PCLKB, and PCLKD)
- (3) Operating clock of the FlashIF: FlashIF clock (FCLK)
- (4) Operating clock of USB modules: USB clock (UCLK)
- (5) Operating clock of CAN modules: CAN clock (CANMCLK)
- (6) Operating clock for the CAC: CAC clock (CACCLK)
- (7) Operating clock for the RTC: RTC-dedicated sub-clock (RTCSCLK)
- (8) Operating clock for the IWDT: IWDT-dedicated low-speed clock (IWDTCCLK)
- (9) Operating clock for the SSI: SSI clock (SSISCK)
- (10) Operating clocks for BLE: The Bluetooth-dedicated clock (BLECLK), and the Bluetooth-dedicated low-speed clock (BLELOCO)
- (11) Operating clock for the low-power timer: LPT clock (LPTCLK)

Frequencies of the internal clocks are set by the combination of the divisors selected by the SCKCR.FCK[3:0], ICK[3:0], PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits, the clock source selected by the SCKCR3.CKSEL[2:0] bits, and the bits that select the frequency of the PLL circuit (PLLCR.STC[5:0] and PLIDIV[1:0] bits, UPLLCR.UPLIDIV[1:0], USTC[5:0] bits, and HOCOCR2.HCFRQ[1:0] bits). If the value of any of these bits is changed, subsequent operation will be at the frequency determined by the new value.

9.8.1 System Clock

The system clock (ICLK) is used as the operating clock of the CPU, DMAC, DTC, ROM, and RAM. The ICLK frequency is specified by the SCKCR.ICK[3:0] bits, and the SCKCR3.CKSEL[2:0] bits, and the PLLCR.STC[5:0] and PLIDIV[1:0] bits.

9.8.2 Peripheral Module Clock

The peripheral module clocks (PCLKA, PCLKB, and PCLKD) are the operating clocks for use by peripheral modules. The PCLKA, PCLKB, and PCLKD frequencies are specified by the SCKCR.PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits, the SCKCR3.CKSEL[2:0] bits, and the PLLCR.STC[5:0] and PLIDIV[1:0] bits. The peripheral module clock used as the operating clock is PCLKD for S12AD, and PCLKA and PCLKB are for other modules.

9.8.3 FlashIF Clock

The FlashIF clock (FCLK) is used as the operating clock of the FlashIF. The FCLK frequency is specified by the SCKCR.FCK[3:0] bits, and the SCKCR3.CKSEL[2:0] bits, and the PLLCR.STC[5:0] and PLIDIV[1:0] bits.

9.8.4 USB Clock

The USB clock (UCLK) is an operating clock for the USB module. The UCLK frequency is specified by the SCKCR3.CKSEL[2:0] bits, and the PLLCR.STC[5:0], PLIDIV[1:0] bits, and the UPLLCR.UPLIDIV[1:0] and USTC[5:0] bits.

A 48-MHz clock must be supplied to the USB module. When the USB module is used, setting must be made so that UCLK is 48 MHz.

9.8.5 CAN Clock

The CAN clock (CANMCLK) is an operating clock for the CAN module. CANMCLK is generated by the main clock oscillator.

9.8.6 CAC Clock

The CAC clock (CACCLK) is an operating clock for the CAC module.

The CACCLK clocks include CACMCLK which is generated by the main clock oscillator, CACSCLK which is generated by the sub-clock oscillator, CACHCLK which is generated by the high-speed on-chip oscillator, CACLCLK which is generated by the low-speed on-chip oscillator, and CACILCLK which is generated by the IWDG-dedicated on-chip oscillator.

9.8.7 RTC-Dedicated Clock

The RTC-dedicated clock (RTCSCLK) is the operating clock for the RTC. RTCSCLK is generated by the sub-clock oscillator.

9.8.8 IWDG-Dedicated Clock

The IWDG-dedicated clock (IWDGCLK) is the operating clock for the IWDG. IWDGCLK is internally generated by the IWDG-dedicated on-chip oscillator.

9.8.9 SSI Clock

The SSI clock (SSISCK) is the operating clock for the SSI. SSISCK is generated by the main clock oscillator.

9.8.10 Clocks for BLE

The Bluetooth-dedicated clock (BLECLK) and the Bluetooth-dedicated low-speed clock (BLELOCO) are the operating clocks for the BLE. To control these clocks, use the Bluetooth middleware provided by Renesas.

9.8.11 Low-Power Timer Clock

The low-power timer clock (LPTCLK) is an operating clock for the low-power timer. The LPTCLK clocks include a clock generated by the sub-clock oscillator and a clock generated by the IWDG-dedicated on-chip oscillator.

9.9 Usage Notes

9.9.1 Notes on Clock Generation Circuit

- (1) The frequencies of the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK) supplied to each module can be selected by the SCKCR register. Each frequency should meet the following:
 Select each frequency that is within the operation guaranteed range of clock cycle time (tcyc) specified in AC characteristics of electrical characteristics.
 The frequencies must not exceed the ranges listed in Table 9.1.
 The peripheral modules operate on the PCLKA, PCLKB and PCLKD. Note therefore that the operating speed of modules such as the timer and SCI varies before and after the frequency is changed.
- (2) The relationship of frequencies of the system clock (ICLK), peripheral module clocks A, B, and D (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK) must be set as follows.
 $ICLK:FCLK = N:1$ or $1:N$ (N is an integer)
 $ICLK:PCLKA, PCLKB, \text{ and } PCLKD = N:1$ or $1:N$ (N is an integer)
- (3) To secure the processing after the clock frequency is changed, modify the pertinent clock control register to change the frequency, and then read the value from the register, and then perform the subsequent processing.

9.9.2 Note on Rewriting the SCKCR3 Register

When the SCKCR3.CKSEL[2:0] bits have been rewritten, the clock output is temporarily stopped to prevent the switch of the clock source from generating a clock pulse of short duration (glitch). The interrupt controller and event link controller may not detect the following signals that were input during this period.

- (1) An external pin interrupt or NMI pin interrupt with a pulse width shorter than 4 cycles of the PCLKB after the switch while the PCLKB frequency is the 1/1 of the clock source (the SCKCR.PCKB[3:0] bits are 0000b).
- (2) An external pin interrupt or NMI pin interrupt with a pulse width shorter than 2.5 cycles of the PCLKB after the switch while the PCLKB frequency is the 1/2 of the clock source (the SCKCR.PCKB[3:0] bits are 0001b).
- (3) An RTC periodic interrupt or RTC periodic event output when the SCKCR3.CKSEL[2:0] bits are changed to "011b" (sub-clock).

When the external pin interrupt or NMI pin interrupt is in use, input the signal with enough pulse width to exceed the time condition described in (1) and (2). When the RTC periodic interrupt or RTC periodic event output is in use, switch the clock source after a periodic interrupt is generated and before the next periodic interrupt is generated.

9.9.3 Notes on Resonator

Since various resonator characteristics relate closely to the user's board design, adequate evaluation is required on the user side before use, referencing the resonator connection example shown in this section. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, the circuit constants should be determined in full consultation with the resonator manufacturer. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

9.9.4 Notes on Board Design

When using a crystal, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 9.14 to prevent electromagnetic induction from interfering with correct oscillation.

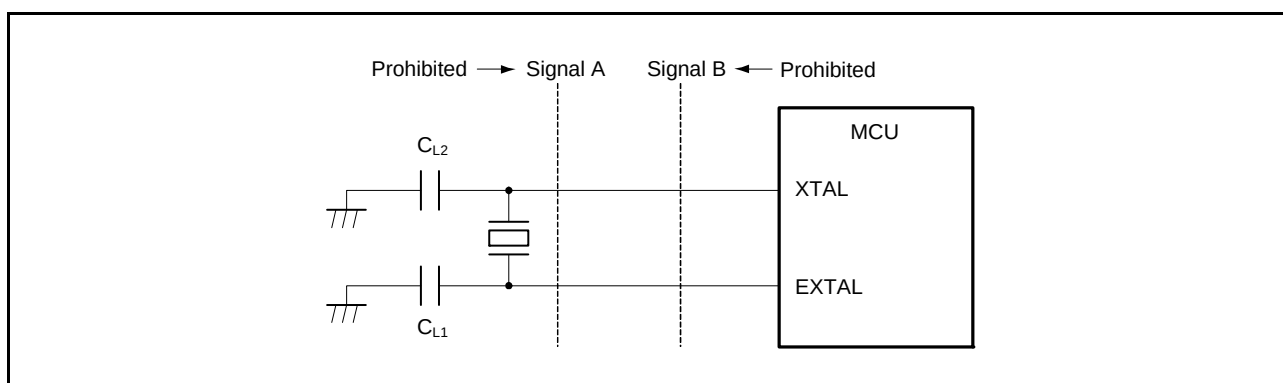


Figure 9.14 Point for Caution on Board Design for the Oscillation Circuit (Applicable to the Main Clock Oscillator as well as the Sub Clock Oscillator and Bluetooth-Dedicated Oscillator)

9.9.5 Notes on Resonator Connection Pins

When the main clock is not used, the EXTAL and XTAL pins can be used as general ports P36 and P37. When using these pins as general ports, be sure to stop the main clock (MOSCCR.MOSTP = 1). However, do not use the EXTAL and XTAL pins as general ports P36 and P37 in a system that uses the main clock.

When the main clock is used, do not set P36 and P37 to output.

9.9.6 Notes on Sub-Clock

The sub-clock can be used as the system clock, as the count source for the realtime clock, or as both. Take note of the following limitations and points for caution regarding the settings, including when the sub-clock is not in use.

- With regard to making the sub-clock oscillator run or stop, setting either the sub-clock oscillator stop bit in the sub-clock oscillator control register (SOSCCR.SOSTP) or the sub-clock oscillator control bit in RTC control register 3 (RCR3.RTCEN) will make the oscillator run.
- To use the sub-clock as the system clock and as the count source of the realtime clock simultaneously, perform initial settings according to the flowchart example shown in Figure 9.15. After that, perform the clock setting procedure shown in section 28.3.2, Clock and Count Mode Setting Procedure.

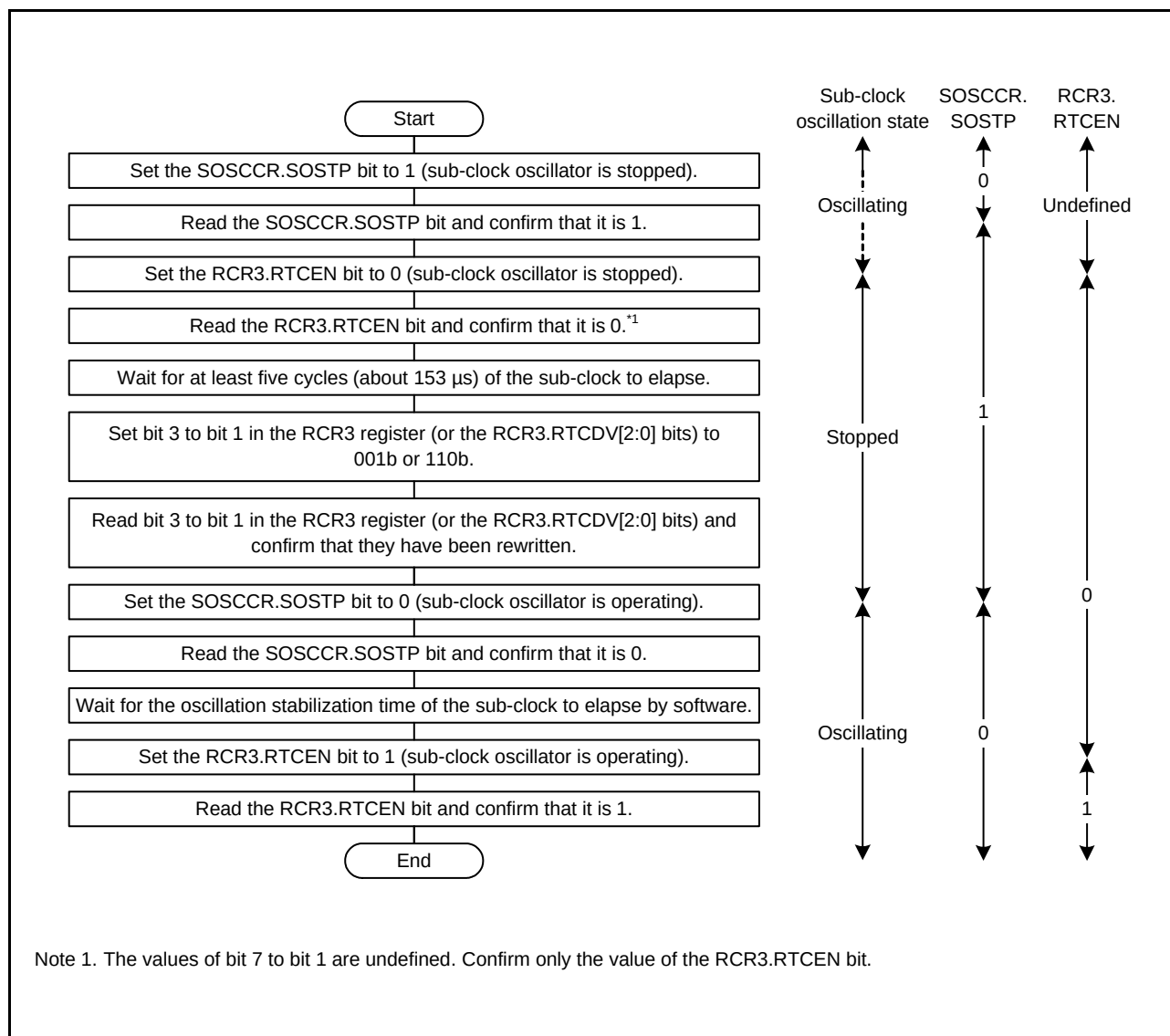


Figure 9.15 Example of Initialization Flowchart When Sub-Clock is Used as Count Source of Realtime Clock

- When using the sub-clock only as the count source of the realtime clock, perform initial settings according to the flowchart example shown in Figure 9.16. After that, perform the clock setting procedure shown in section 28.3.2, Clock and Count Mode Setting Procedure.

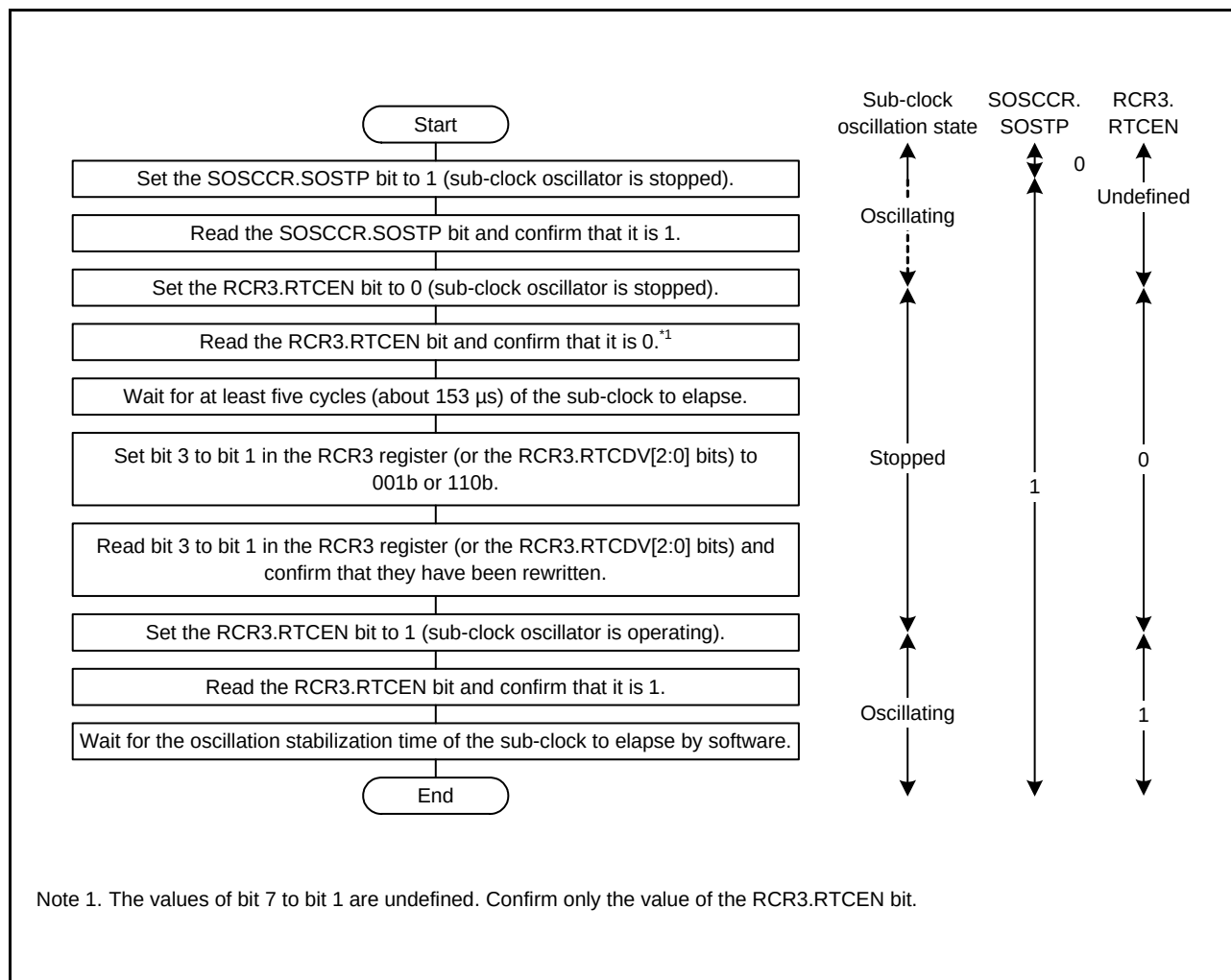


Figure 9.16 Example of Initialization Flowchart When Sub-Clock is Used Only as Count Source of Realtime Clock

- When using the sub-clock only as the system clock, perform initial settings according to the flowchart example shown in Figure 9.17.

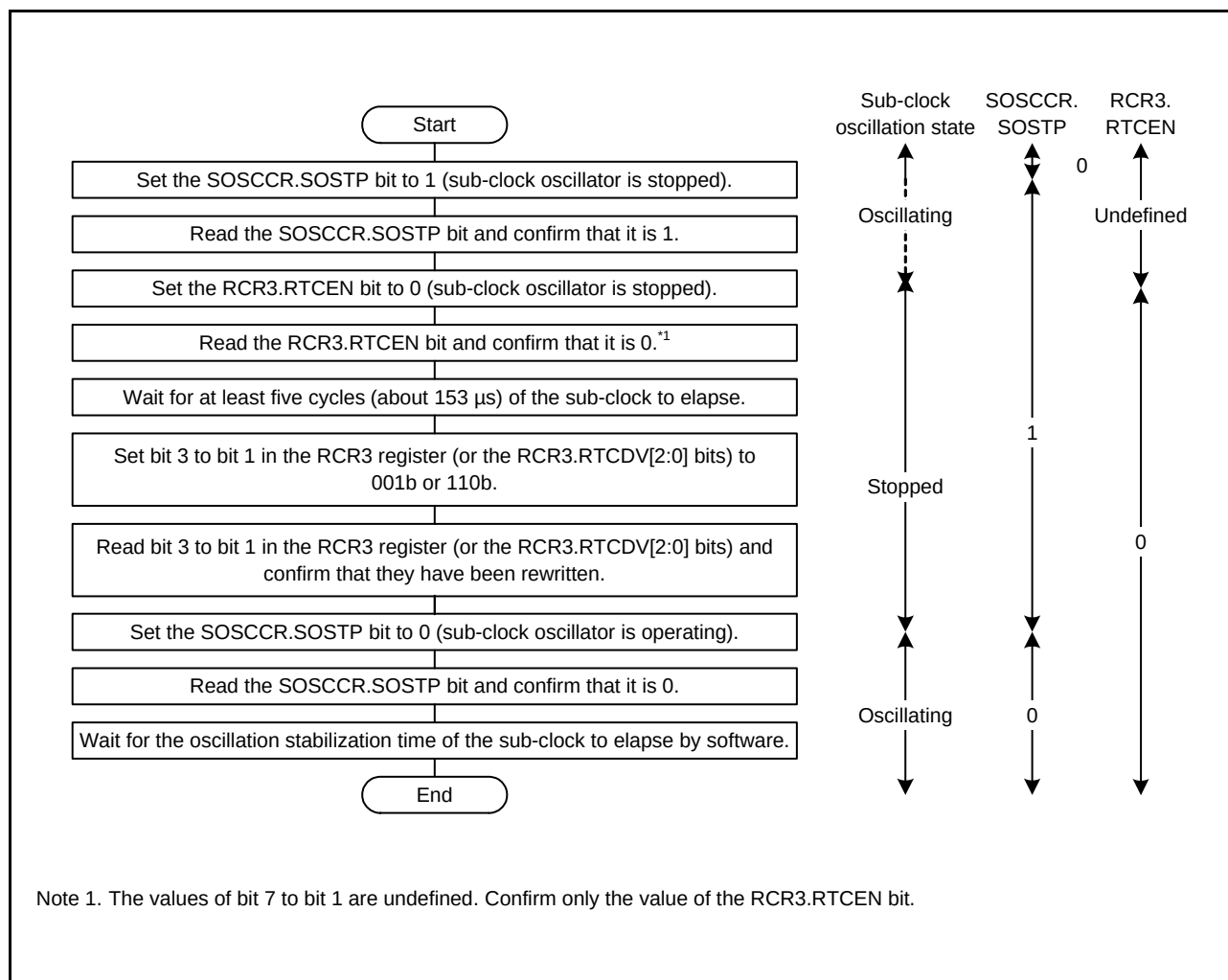


Figure 9.17 Example of Initialization Flowchart When Sub-Clock is Used Only as System Clock

- When not using the sub-clock, perform initial settings according to the flowchart example in Figure 9.18.

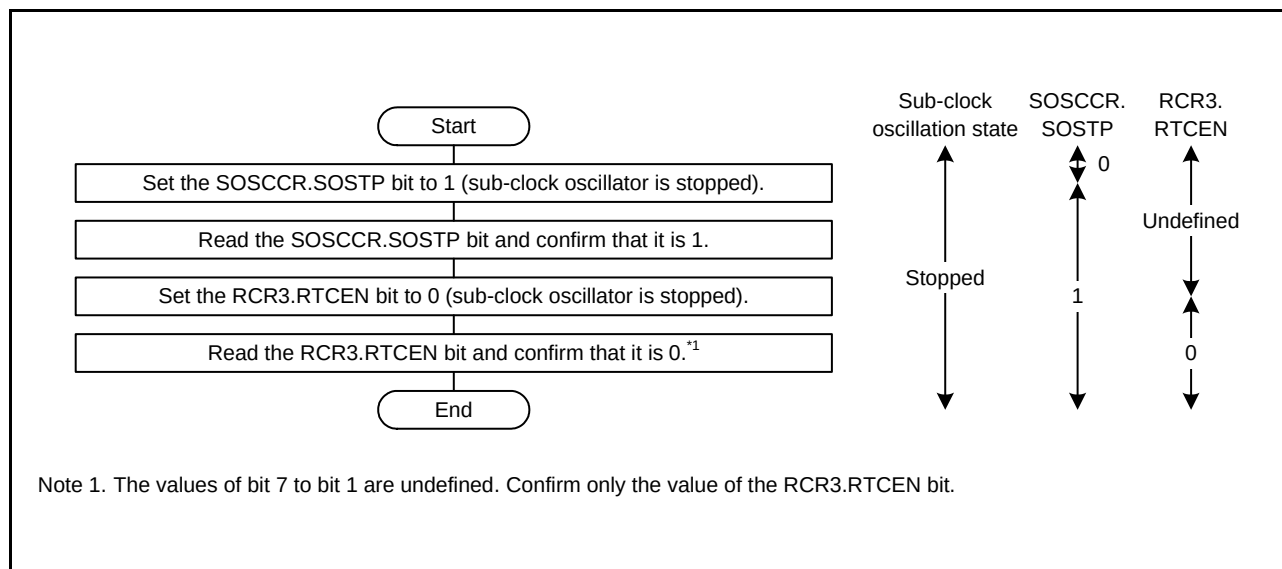


Figure 9.18 Example of Initialization Flowchart When Sub-Clock is Not Used

- Regardless of the RCR3.RTCEN bit setting, wait until the oscillator stabilization wait time elapses before rewriting the SOSCCR.SOSTP bit to 0 (sub-clock oscillator is operating).
- Since the sub-clock control circuit is in an unstable state after a cold start, it must be initialized regardless of whether or not the sub-clock is in use. The sub-clock is initialized by setting the SOSCCR.SOSTP bit to 1 and the RCR3.RTCEN bit to 0 (sub-clock oscillator is stopped). See section 28.2.19, RTC Control Register 3 (RCR3), for instructions to initialize the RCR3.RTCEN bit.
- The RCR3.RTCDV[2:0] bits must also be set when operating the sub-clock oscillator. Set these bits while the sub-clock oscillator is stopped. Do not rewrite these bits while the sub-clock oscillator is operating.
- When successively rewriting the SOSCCR.SOSTP bit followed by the RCR3.RTCEN bit or vice versa, confirm that the first bit rewrite was completed successfully before rewriting the second bit.

10. Clock Frequency Accuracy Measurement Circuit (CAC)

10.1 Overview

The clock frequency accuracy measurement circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is completed or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated.

Table 10.1 lists the specifications of the CAC and Figure 10.1 shows a block diagram of the CAC.

Table 10.1 CAC Specifications

Item	Description
Measurement target clocks	The frequency of the following clocks can be measured. • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input to the CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCCLK) • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Module stop state can be set.

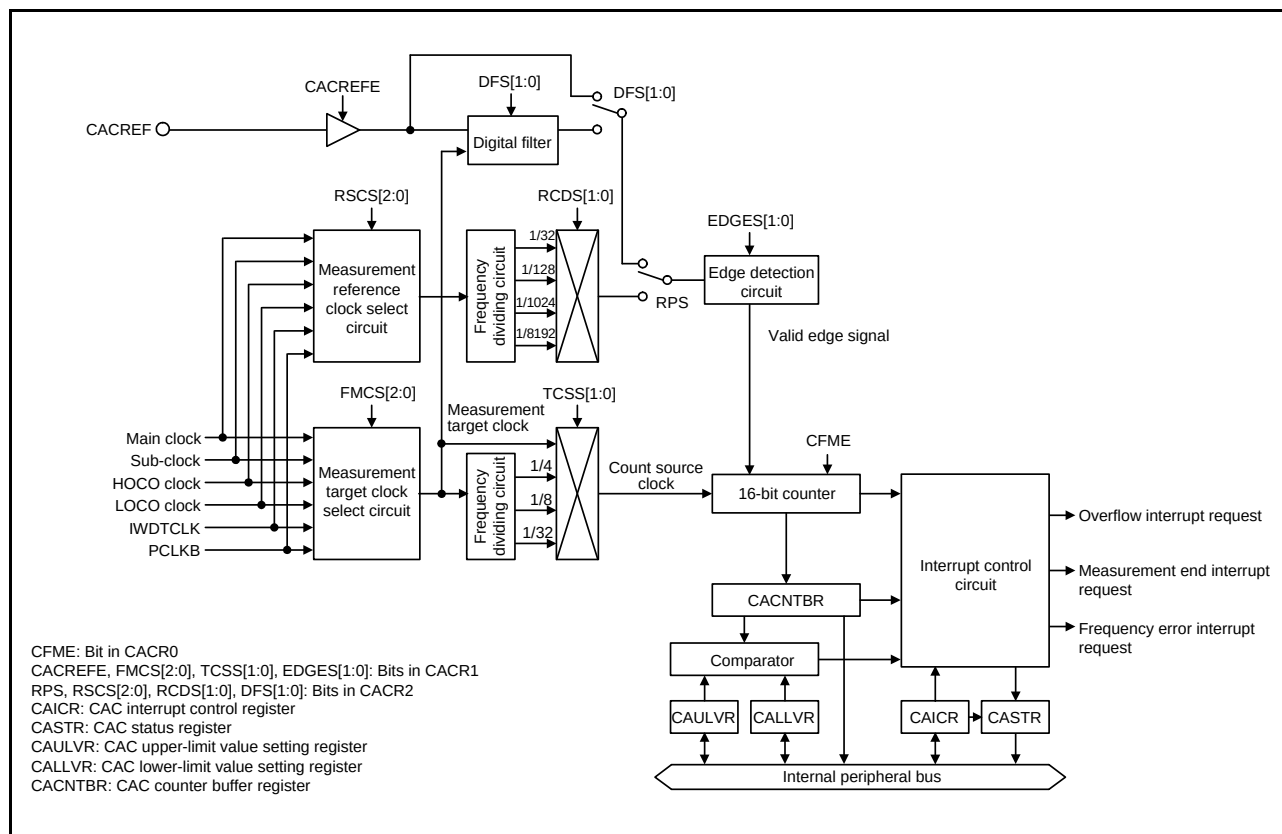


Figure 10.1 CAC Block Diagram

Table 10.2 shows the pin configuration of the CAC.

Table 10.2 Pin Configuration of CAC

Pin Name	I/O	Function
CACREF	Input	Measurement reference clock input pin

10.2 Register Descriptions

10.2.1 CAC Control Register 0 (CACR0)

Address(es): 0008 B000h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	CFME
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Clock frequency measurement is disabled. 1: Clock frequency measurement is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

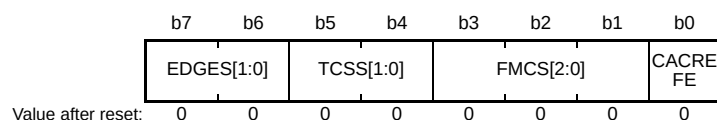
CFME Bit (Clock Frequency Measurement Enable)

This bit specifies whether clock frequency measurement is enabled or disabled.

When rewriting this bit, more time is required than other bits for the new value to be reflected in the register. Further write access to this bit are ignored until the current write access is reflected in the register. Read the bit to confirm that the rewrite has been reflected in the register.

10.2.2 CAC Control Register 1 (CACR1)

Address(es): 0008 B001h



Bit	Symbol	Bit Name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: CACREF pin input is disabled. 1: CACREF pin input is enabled.	R/W
b3 to b1	FMCS[2:0]	Measurement Target Clock Select	b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDt-dedicated clock (IWDtCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than above are prohibited.	R/W
b5, b4	TCSS[1:0]	Timer Count Clock Source Select	b5 b4 0 0: No division 0 1: ×1/4 clock 1 0: ×1/8 clock 1 1: ×1/32 clock	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE Bit (CACREF Pin Input Enable)

This bit specifies whether the CACREF pin input is enabled or disabled.

FMCS[2:0]Bits (Measurement Target Clock Select)

These bits select the measurement target clock whose frequency is to be measured.

TCSS[1:0] Bits (Timer Count Clock Source Select)

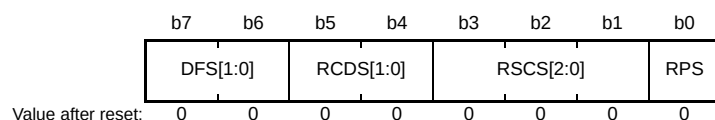
These bits select the count clock source for the clock frequency accuracy measurement circuit.

EDGES[1:0]Bits (Valid Edge Select)

These bits select the valid edge for the reference signal.

10.2.3 CAC Control Register 2 (CACR2)

Address(es): 0008 B002h



Bit	Symbol	Bit Name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internal clock (internally generated signal)	R/W
b3 to b1	RSCS[2:0]	Measurement Reference Clock Select	b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTC dedicated clock (IWDTCCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than above are prohibited.	R/W
b5, b4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ration Select	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock	R/W
b7, b6	DFS[1:0]	Digital Filter Select	b7 b6 0 0: Digital filtering is disabled. 0 1: The sampling clock for the digital filter is the measurement target clock. 1 0: The sampling clock for the digital filter is the measurement target clock divided by 4. 1 1: The sampling clock for the digital filter is the measurement target clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS Bit (Reference Signal Select)

This bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0]Bits (Measurement Reference Clock Select)

These bits select the clock source for generating the measurement reference clock.

RCDS[1:0]Bits (Measurement Reference Clock Frequency Division Ration Select)

These bits select the frequency division ratio of the measurement reference clock.

DFS[1:0]Bits (Digital Filter Select)

The setting of these bits enables or disables the digital filter and selects its sampling clock.

10.2.4 CAC Interrupt Request Enable Register (CAICR)

Address(es): 0008 B003h

b7	b6	b5	b4	b3	b2	b1	b0
—	OVFFC L	MENDF CL	FERRF CL	—	OVFIE	MENDI E	FERRI E
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Request Enable	0: Frequency error interrupt request is disabled. 1: Frequency error interrupt request is enabled.	R/W
b1	MENDIE	Measurement End Interrupt Request Enable	0: Measurement end interrupt request is disabled. 1: Measurement end interrupt request is enabled.	R/W
b2	OVFIE	Overflow Interrupt Request Enable	0: Overflow interrupt request is disabled. 1: Overflow interrupt request is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	When 1 is written to this bit, the CASTR.FERRF flag is cleared. This bit is read as 0.	R/W
b5	MENDFCL	MENDF Clear	When 1 is written to this bit, the CASTR.MENDF flag is cleared. This bit is read as 0.	R/W
b6	OVFFCL	OVFF Clear	When 1 is written to this bit, the CASTR.OVFF flag is cleared. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE Bit (Frequency Error Interrupt Request Enable)

This bit specifies whether the frequency error interrupt request is enabled or disabled.

MENDIE Bit (Measurement End Interrupt Request Enable)

This bit specifies whether the measurement end interrupt request is enabled or disabled.

OVFIE Bit (Overflow Interrupt Request Enable)

This bit specifies whether the overflow interrupt request is enabled or disabled.

FERRFCL Bit (FERRF Clear)

Setting this bit to 1 clears the CASTR.FERRF flag.

MENDFCL Bit (MENDF Clear)

Setting this bit to 1 clears the CASTR.MENDF flag.

OVFFCL Bit (OVFF Clear)

Setting this bit to 1 clears the CASTR.OVFF flag.

10.2.5 CAC Status Register (CASTR)

Address(es): 0008 B004h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	OVFF	MENDF	FERRF
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	FERRF	Frequency Error Flag	0: The clock frequency is within the range corresponding to the settings. 1: The clock frequency has deviated beyond the range corresponding to the settings (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress. 1: Measurement has ended.	R
b2	OVFF	Overflow Flag	0: The counter has not overflowed. 1: The counter has overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FERRF Flag (Frequency Error Flag)

This flag indicates deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside of the setting range.

[Clearing condition]

- 1 is written to the CAICR.FERRFCL bit.

MENDF Flag (Measurement End Flag)

This flag indicates the end of measurement.

[Setting condition]

- Measurement has finished.

[Clearing condition]

- 1 is written to the CAICR.MENDFCL bit.

OVFF Flag (Overflow Flag)

This flag indicates that the counter has overflowed.

[Setting condition]

- The counter has overflowed.

[Clearing condition]

- 1 is written to the CAICR.OVFFCL bit.

10.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address(es): 0008 B006h



CAULVR is a 16-bit readable/writable register that specifies the upper-limit value of the counter used for measuring the frequency. When the frequency rises above the value specified in this register, a frequency error is detected.

Write to this register when the CACR0.CFME bit is 0.

The counter value held in CACNTBR can vary with the difference between the phases of the digital filter and edge-detection circuit on the one hand and the signal on the CACREF pin on the other, so ensure that this setting allows an adequate margin.

10.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address(es): 0008 B008h



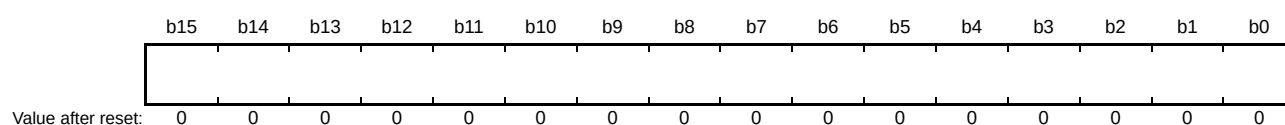
CALLVR is a 16-bit readable/writable register that specifies the lower-limit value of the counter used for measuring the frequency. When the frequency falls below the value specified in this register, a frequency error is detected.

Write to this register when the CACR0.CFME bit is 0.

The counter value held in CACNTBR can vary with the difference between the phases of the digital filter and edge-detection circuit on the one hand and the signal on the CACREF pin on the other, so ensure that this setting allows an adequate margin.

10.2.8 CAC Counter Buffer Register (CACNTBR)

Address(es): 0008 B00Ah



CACNTBR is a 16-bit read-only register that retains the counter value at the time a valid reference signal edge is input.

10.3 Operation

10.3.1 Measuring Clock Frequency

The clock frequency accuracy measurement circuit measures the clock frequency using the CACREF pin input or the internal clock as a reference. Figure 10.2 shows an operating example of the clock frequency accuracy measurement circuit.

The clock frequency accuracy measurement circuit operates as shown below when measuring the clock frequency.

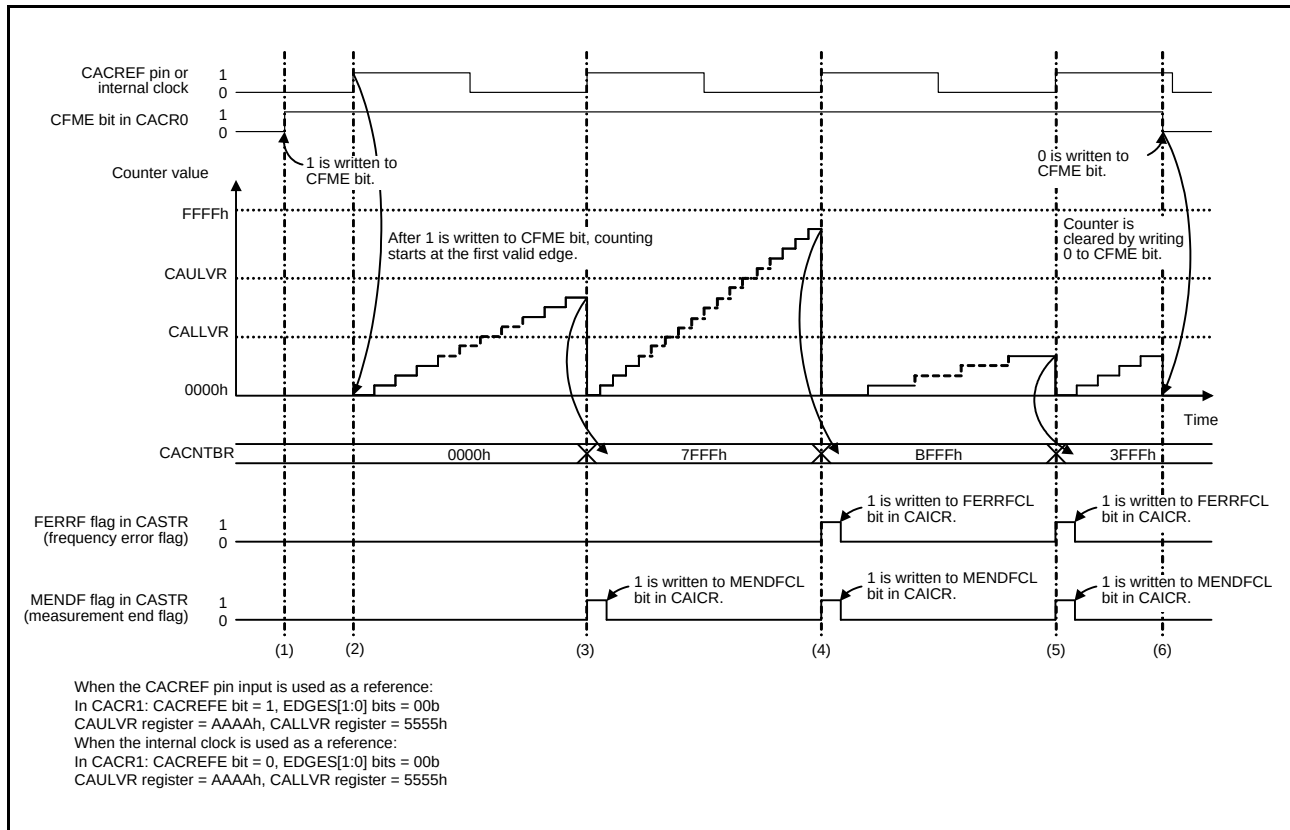


Figure 10.2 Operating Example of Clock Frequency Accuracy Measurement Circuit

- (1) When the CACREF pin input is used as a reference (CACR1.CACREFE bit = 1), clock frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is 0 and the CACR1.CACREFE bit is 1. On the other hand, when the internal clock is used as a reference (CACR1.CACREFE bit = 0), clock frequency measurement is enabled by writing 1 to the CACR0.CFME bit while the CACR2.RPS bit is 1.
- (2) When the CACREF pin input is used as a reference, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits is input from the CACREF pin after 1 is written to the CFME bit. The valid edge is a rising edge (CACR1.EDGES[1:0] = 00b) in Figure 10.2.
When the internal clock is used as a reference, the timer starts up-counting if the valid edge selected by the CACR1.EDGES[1:0] bits is input based on the clock source selected by the CACR2.RSCS[2:0] bits after 1 is written to the CFME bit. The valid edge is a rising edge (CACR1.EDGES[1:0] = 00b) in Figure 10.2.
- (3) When the next valid edge is input, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR. If both $CACNTBR \leq CAULVR$ and $CACNTBR \geq CALLVR$ are satisfied, only the MENDF flag in CASTR is set to 1 because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
- (4) When the next valid edge is input, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of $CACNTBR > CAULVR$, the FERRF flag in CASTR is set to 1 because the

clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.

- (5) When the next valid edge is input, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR. In the case of $CACNTBR < CALLVR$, the FERRF flag in CASTR is set to 1 because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. Also, the MENDF flag in CASTR is set to 1. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
- (6) While the CFME bit in CACR0 is 1, the counter value is transferred in CACNTBR and compared with the values of CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

10.3.2 Digital Filtering of Signals on the CACREF Pin

The CACREF pin has a digital filter. Levels on the target pin for sampling are conveyed to the internal circuitry after matching three consecutive times at the selected sampling interval and the same level continues to be conveyed internally until the level on the pin again matches three consecutive times.

Enabling and disabling of the digital filter and its sampling clock are selectable.

The counter value transferred in CACNTBR may be in error by up to one cycle of the sampling clock due to the difference between the phases of the digital filter and the signal input to the CACREF pin.

When a frequency dividing clock is selected as a count source clock, the counter value error is obtained by the following formula:

Counter value error = (One cycle of the count source clock) / (One cycle of the sampling clock)

10.4 Interrupt Requests

The CAC generates three types of interrupt request: frequency error interrupt, measurement end interrupt, and overflow interrupt. When an interrupt source is generated, the corresponding status flag becomes 1. Table 10.3 lists details on the interrupt requests of the clock frequency accuracy measurement circuit.

Table 10.3 Interrupt Requests of Clock Frequency Accuracy Measurement Circuit

Interrupt Request	Interrupt Enable Bit	Status Flag	Interrupt Source
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	The result of comparing CACNTBR to CAULVR and CALLVR is either $CACNTBR > CAULVR$ or $CACNTBR < CALLVR$.
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	A valid edge is input from the CACREF pin. Note however that a measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit.
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	The counter has overflowed.

10.5 Usage Notes

10.5.1 Module Stop Function Setting

CAC operation can be disabled or enabled using module stop control register C (MSTPCRC). The initial setting is for the CAC to be halted. Register access is enabled by releasing the module stop state. For details, refer to [section 11](#), Low Power Consumption.

11. Low Power Consumption

11.1 Overview

This MCU has several functions for reducing power consumption, by setting clock dividers, stopping modules, changing to low power consumption mode in normal operation, and changing to operating power control mode.

Table 11.1 lists the specifications of low power consumption functions, and Table 11.2 lists the conditions to change to low power consumption modes, states of the CPU and peripheral modules, and the method for exiting each mode.

After a reset, this MCU returns to normal mode, but modules except the DMAC, DTC, and RAM are stopped.

Table 11.1 Specifications of Low Power Consumption Functions

Item	Specification
Clock divider functions	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK). ^{*1}
Module stop function	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode
Operating power control modes	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available - High-speed operating mode - Middle-speed operating mode - Low-speed operating mode

Note 1. For details, refer to section 9, Clock Generation Circuit.

Table 11.2 Operating Conditions of Each Power Consumption Mode

Entering and Exiting Low Power Consumption Modes and Operating States	Sleep Mode	Deep Sleep Mode	Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt	Interrupt* ¹
After exiting from each mode, CPU begins from* ²	Interrupt handling	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible	Stopped
Sub-clock oscillator	Operating possible	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible	Stopped
Low-speed on-chip oscillator	Operating possible	Operating possible	Stopped
IWDT-dedicated on-chip oscillator	Operating possible* ³	Operating possible* ³	Operating possible* ³
PLL	Operating possible	Operating possible	Stopped
USB-dedicated PLL	Operating possible	Operating possible	Stopped
CPU	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
RAM (0000 0000h to 0000 FFFFh)	Operating possible (Retained)	Stopped (Retained)	Stopped (Retained)
DMAC	Operating possible* ⁵	Stopped (Retained)	Stopped (Retained)
DTC	Operating possible* ⁵	Stopped (Retained)	Stopped (Retained)
Flash memory	Operating	Stopped (Retained)	Stopped (Retained)
Watchdog timer (WDT)	Stopped (Retained)	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible* ³	Operating possible* ³	Operating possible* ³
Realtime clock (RTC)	Operating possible	Operating possible	Operating possible
Low power timer (LPT)	Operating possible* ⁸	Operating possible* ⁸	Operating possible* ⁸
Voltage detection circuit (LVD)	Operating possible	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating	Operating
Peripheral modules	Operating possible	Operating possible	Stopped (Retained)* ⁴
I/O ports	Operating	Operating	Retained
RTCCOUT	Operating possible	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible	Operating possible* ⁶
Comparator B	Operating possible	Operating possible	Operating possible* ⁷

"Operating possible" means that operating or stopped can be controlled by the register setting.

"Stopped (Retained)" means that internal register values are retained and internal operations are suspended.

- Note 1. "Interrupts" here indicates an external pin interrupt (the NMI, IRQ0, IRQ1, or IRQ4 to IRQ7) or any of peripheral interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, VBATT pin voltage drop detection, USB and ELC (LPT-dedicated interrupt) interrupts).
- Note 2. This does not include a RES# pin reset, power-on reset, voltage monitoring reset, or independent watchdog-timer reset. One of these reset sources initiate transition to reset state.
- Note 3. Operating or stopping is selected by setting the IWDT sleep mode count stop control bit (IWDTSLCSTP) in option function select register 0 (OFS0) in IWDT auto-start mode. In any mode other than IWDT auto-start mode, operating or stopping is selected by the setting of the sleep mode count stop control bit (SLCSTP) in the IWDT count stop control register (IWDTCSSTPR).
- Note 4. The peripheral logic states are retained.
- Note 5. During sleep mode, do not write to the system control related registers (indicated by 'SYSTEM' in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order)).
- Note 6. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 011b (sub-clock oscillator).
- Note 7. Using the digital filter function is prohibited. Operation for outputting the comparison result to the CMPOBn pin is possible.
- Note 8. When the low-power timer clock source select bit in the low-power timer control register 1 (LPTCR1.LPCNTCKSEL) is 1 (selecting IWDT-dedicated on-chip oscillator), operating or stopping can be selected as described in Note 3. When the value of the bit is 0 (selecting the sub-clock oscillator), only operating is possible.

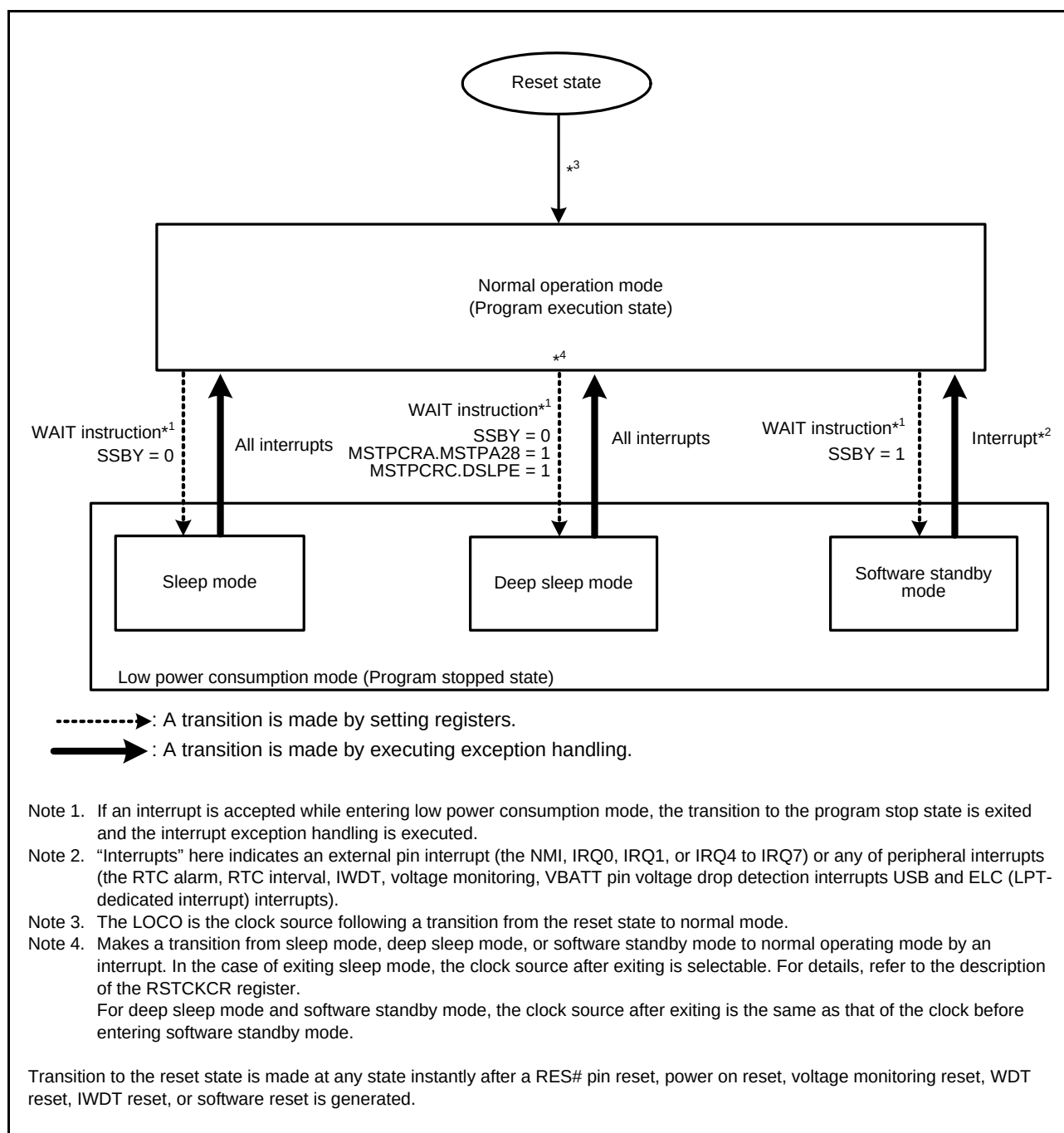


Figure 11.1 Mode Transitions

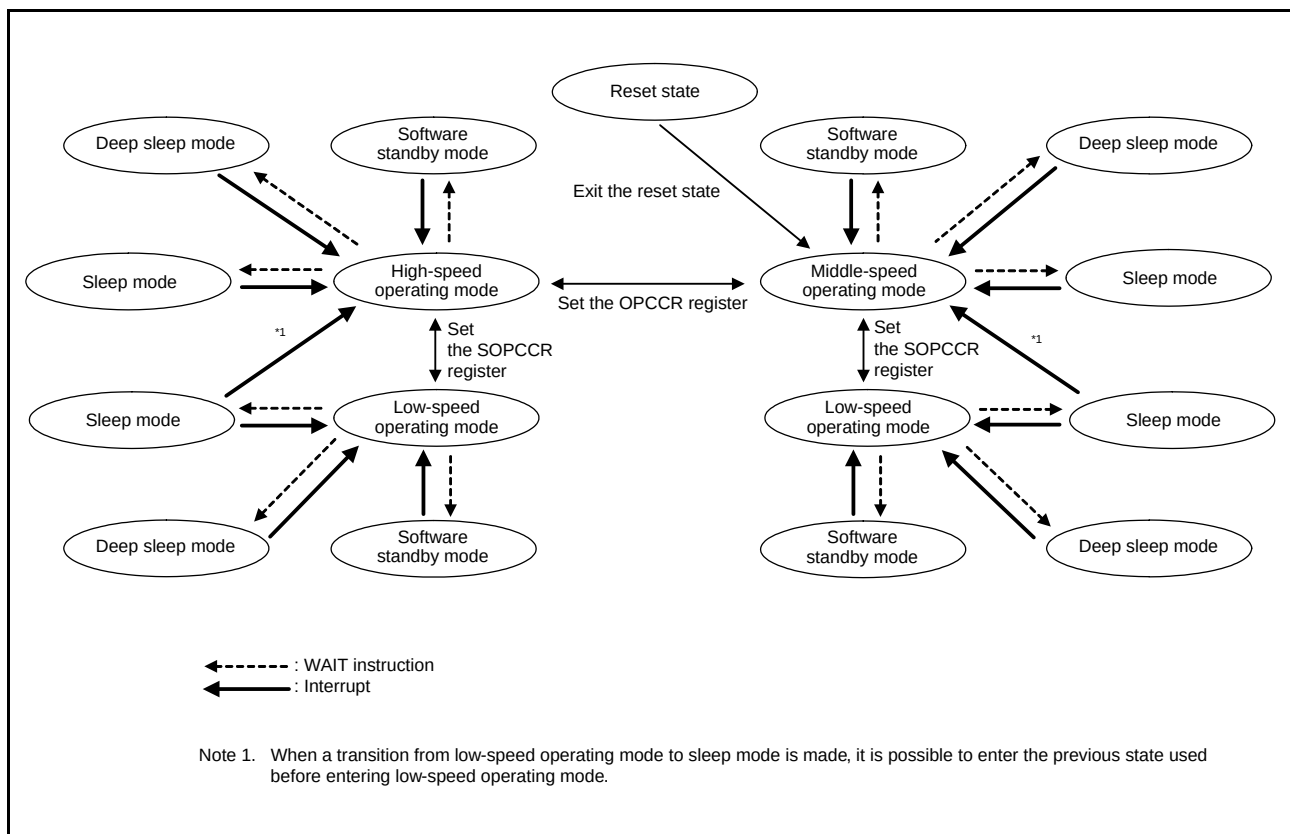


Figure 11.2 Operating Modes

- The sub-clock oscillator does not stop when entering software standby mode.
- It is possible to return from sleep mode to the previous operating state used before entering sleep mode. However, when a transition from low-speed operating mode to sleep mode is made, it is possible to enter the previous state used before entering low-speed operating mode.
- After exiting the reset state, operation starts in middle-speed operating mode.

Table 11.3 Oscillator Usability in Each Mode

	PLL	USB-dedicated PLL	HOCO	LOCO	IWDTCLK	Main Clock Oscillator	Sub-Clock Oscillator
High-speed operating mode	Usable* ¹	Usable* ¹	Usable	Usable	Usable	Usable	Usable
Middle-speed operating mode	Usable* ¹	Usable* ¹	Usable	Usable	Usable	Usable	Usable
Low-speed operating mode	Not usable	Not usable	Not usable	Not usable	Usable	Not usable	Usable

Note 1. The PLL and USB-dedicated PLL are usable when the power supply voltage is 2.4 V or above.

11.2 Register Descriptions

11.2.1 Standby Control Register (SBYCR)

Address(es): 0008 000Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	SSBY	Software Standby	0: Set entry to sleep mode or deep sleep mode after the WAIT instruction is executed 1: Set entry to software standby mode after the WAIT instruction is executed	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

SSBY Bit (Software Standby)

The SSBY bit specifies the transition destination after the WAIT instruction is executed.

When the SSBY bit is set to 1, the MCU enters software standby mode after execution of the WAIT instruction. When the MCU returns to normal mode after an interrupt has triggered and exits from software standby mode, the SSBY bit remains 1. The SSBY bit can be cleared by writing 0 to the SSBY bit.

When the oscillation stop detection function enable bit (OSTDCR.OSTDE) in the oscillation stop detection control register is 1, the set value of the SSBY bit is invalid. Even if the SSBY bit is 1, the MCU will enter sleep mode or deep sleep mode after execution of the WAIT instruction.

11.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): 0008 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	MSTPA 28	—	—	—	—	—	—	—	—	MSTPA 19	—	MSTPA 17	—
Value after reset:	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPA 15	MSTPA 14	MSTPA 13	—	—	—	MSTPA 9	—	—	—	MSTPA 5	MSTPA 4	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b4	MSTPA4	8-bit Timer 3 and 2 (Unit 1) Module Stop	Target module: TMR3, TMR2 0: This module clock is enabled 1: This module clock is disabled	R/W
b5	MSTPA5	8-bit Timer 1 and 0 (Unit 0) Module Stop	Target module: TMR1, TMR0 0: This module clock is enabled 1: This module clock is disabled	R/W
b8 to b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b9	MSTPA9	Multifunction Timer Pulse Unit 2 Module Stop	Target module: MTU (MTU0 to MTU4) 0: This module clock is enabled 1: This module clock is disabled	R/W
b12 to b10	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b13	MSTPA13	16-Bit Timer Pulse Unit Module Stop	Target module: TPU (TPU0 to TPU5) 0: The module stop state is canceled 1: Transition to the module stop state is made	R/W
b14	MSTPA14	Compare Match Timer 1 (Unit 1) Module Stop	Target module: CMT unit 1 (CMT2, CMT3) 0: This module clock is enabled 1: This module clock is disabled	R/W
b15	MSTPA15	Compare Match Timer (Unit 0) Module Stop	Target module: CMT unit 0 (CMT0, CMT1) 0: This module clock is enabled 1: This module clock is disabled	R/W
b16	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b17	MSTPA17	12-Bit A/D Converter Module Stop	Target module: S12AD 0: This module clock is enabled 1: This module clock is disabled	R/W
b18	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b19	MSTPA19	12-Bit D/A Converter Module Stop	Target module: DA 0: This module clock is enabled 1: This module clock is disabled	R/W
b27 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b28	MSTPA28	DMA Controller / Data Transfer Controller Module Stop	Target module: DMAC/DTC 0: This module clock is enabled 1: This module clock is disabled	R/W
b31 to b29	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

11.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): 0008 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	MSTPB30	—	—	—	MSTPB26	MSTPB25	—	MSTPB23	—	MSTPB21	—	MSTPB19	—	MSTPB17	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MSTPB10	MSTPB9	—	—	MSTPB6	—	MSTPB4	—	—	—	MSTPB0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPB0*1	RSCAN0 Module Stop	Target module: RSCAN0 0: This module clock is enabled 1: This module clock is disabled	R/W
b3 to b1	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b4	MSTPB4	Serial Communication Interface SC1h Module Stop	Target module: SC1h (SC112) 0: This module clock is enabled 1: This module clock is disabled	R/W
b5	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b6	MSTPB6	DOC Module Stop	Target module: DOC 0: This module clock is enabled 1: This module clock is disabled	R/W
b8, b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b9	MSTPB9	ELC Module Stop	Target module: ELC 0: This module clock is enabled 1: This module clock is disabled	R/W
b10	MSTPB10	Comparator B Module Stop	Target module: Comparator B 0: This module clock is enabled 1: This module clock is disabled	R/W
b16 to b11	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b17	MSTPB17	Serial Peripheral Interface 0 Module Stop	Target module: RSPi0 0: This module clock is enabled 1: This module clock is disabled	R/W
b18	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b19	MSTPB19*2	USB0 Module Stop	Target module: USB0 0: This module clock is enabled 1: This module clock is disabled	R/W
b20	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b21	MSTPB21	I ² C Bus Interface 0 Module Stop	Target module: RIIC0 0: This module clock is enabled 1: This module clock is disabled	R/W
b22	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b23	MSTPB23	CRC Calculator Module Stop	Target module: CRC 0: This module clock is enabled 1: This module clock is disabled	R/W
b24	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b25	MSTPB25	Bluetooth Low Energy Module Stop	Target module: BLE 0: This module clock is enabled 1: This module clock is disabled	R/W
b26	MSTPB26	Serial Communication Interface 5 Module Stop	Target module: SCi5 0: This module clock is enabled 1: This module clock is disabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b29 to b27	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: This module clock is enabled 1: This module clock is disabled	R/W
b31	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. This bit should be rewritten while the oscillation of the clock to be controlled by this bit is stable. When entering software standby mode after rewriting this bit, wait for two cycles of the CANMCLK after rewriting, and execute a WAIT instruction.

Note 2. This bit should be rewritten while the oscillation of the clock to be controlled by this bit is stable. The clock should be set for oscillation when this bit is 0 (this module clock is enabled). When entering software standby mode after rewriting this bit, wait for two cycles of the UCLK after rewriting, and execute a WAIT instruction. When stopping the clock after rewriting this bit to 1 (this module clock is disabled), wait for two cycles of the UCLK after rewriting, and stop the clock.

11.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): 0008 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DSLPE	—	—	—	MSTPC 27	—	—	—	—	—	—	MSTPC 20	MSTPC 19	—	—	—
Value after reset:	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTPC 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPC0	RAM Module Stop*1	Target module: RAM (0000 0000h to 0000 FFFFh) 0: RAM operating 1: RAM stopped	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b19	MSTPC19	Clock Frequency Accuracy Measurement Circuit Module Stop*2	Target module: CAC 0: This module clock is enabled 1: This module clock is disabled	R/W
b20	MSTPC20	IrDA Module Stop	Target module: IRDA 0: This module clock is enabled 1: This module clock is disabled	R/W
b26 to b21	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b27	MSTPC27	Serial Communication Interface 8 Module Stop	Target module: SCI8 0: This module clock is enabled 1: This module clock is disabled	R/W
b30 to b28	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	DSLPE	Deep Sleep Mode Enable	0: Deep sleep mode is disabled 1: Deep sleep mode is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. The MSTPC0 bit should not be set to 1 during access to the RAM. The RAM should not be accessed while the MSTPC0 bit is 1.

Note 2. The MSTPC19 bit should be rewritten while the oscillation of the clock to be controlled by this bit is stable. For entering software standby mode after rewriting this bit, wait for two cycles of the slowest clock among the clocks output by the oscillators actually oscillating and execute the WAIT instruction.

DSLPE Bit (Deep Sleep Mode Enable)

The DSLPE bit enables or disables a transition to deep sleep mode.

When the CPU executes the WAIT instruction with the DSLPE bit set to 1 and the SBYCR.SSBY and MSTPCRA.MSTPA28 bits meet specified conditions, the MCU enters deep sleep mode. For details, refer to section 11.6.2, Deep Sleep Mode.

11.2.5 Module Stop Control Register D (MSTPCRD)

Address(es): 0008 001Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPD 31	—	—	—	—	—	—	—	—	—	—	—	MSTPD 19	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPD 15	—	—	—	—	MSTPD 10	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b10	MSTPD10	Touch Sensor Control Unit Module Stop	Target module: CTSU 0: This module clock is enabled 1: This module clock is disabled	R/W
b14 to b11	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b15	MSTPD15*1	Serial Sound Interface Module Stop	Target module: SSI 0: This module clock is enabled 1: This module clock is disabled	R/W
b18 to b16	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b19	MSTPD19	SD Host Interface (SDHI) Module Stop	Target module: SDHI 0: This module clock is enabled 1: This module clock is disabled	R/W
b30 to b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	MSTPD31	Trusted Secure IP Function Module Stop*2, *3	Target module: Trusted Secure IP 0: This module clock is enabled 1: This module clock is disabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. When the main clock oscillator is used by the serial sound interface

This bit should be rewritten when the oscillation of the main clock oscillator is stable. When entering software standby mode after rewriting this bit, wait for two cycles of the main clock after rewriting, and execute a WAIT instruction. When stopping the main clock oscillator after rewriting this bit, wait for two cycles of the main clock after rewriting, and stop the main clock oscillator.

Note 2. This bit is reserved in chip version A. Set this bit once to 0 at the beginning of the program to initialize unused circuits.

Note 3. Set this bit once to 0 at the beginning of the program to initialize unused circuits even if the Trusted Secure IP function is not used in chip version B.

11.2.6 Operating Power Control Register (OPCCR)

Address(es): 0008 00A0h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	OPCM TSF	—	OPCM[2:0]		
0	0	0	0	0	0	1	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	OPCM[2:0]	Operating Power Control Mode Select	b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than above are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	OPCMTSF	Operating Power Control Mode Transition Status Flag	0: Transition completed 1: During transition	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

The OPCCR register is used to reduce power consumption in normal operating mode, sleep mode, and deep sleep mode. Power consumption can be reduced according to the operating frequency and operating voltage to be used by the OPCCR setting.

The OPCCR register cannot be rewritten under the following conditions:

- When the OPCCR.OPCMTSF flag is 1 (during transition)
- Time period from WAIT instruction execution for a sleep mode transition, until exit from sleep mode to normal operation
- Time period from WAIT instruction execution for a deep sleep mode transition, until exit from deep sleep mode to normal operation
- When the SOPCCR.SOPCM bit is 1 (low-speed operating mode)

The OPCCR register cannot be rewritten while the flash memory is being programmed or erased (P/E).

For the procedures of changing operating power control modes, refer to Function in section 11.5, Function for Lower Operating Power Consumption.

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order)).

OPCM[2:0] Bits (Operating Power Control Mode Select)

The OPCM[2:0] bits select operating power control mode in normal operating mode, sleep mode, and deep sleep mode. Table 11.4 shows the relationship between operating power control modes, the OPCM[2:0] and SOPCM bit settings, and the operating frequency and voltage ranges.

OPCMTSF Flag (Operating Power Control Mode Transition Status Flag)

This flag indicates the switching control state during and after operating power mode transition.

This flag becomes 1 when the value of the OPCM[2:0] bits is rewritten, and 0 when mode transition is completed. Read this flag and confirm that it is 0 before proceeding to the next processing. Only rewrite the OPCM[2:0] bits when this flag is 0.

11.2.7 Sub Operating Power Control Register (SOPCCR)

Address(es): 0008 00AAh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	SOPC MTSF	—	—	—	SOPC M
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	SOPCM	Sub Operating Power Control Mode Select	0: High-speed operating mode or middle-speed operating mode*1 1: Low-speed operating mode	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SOPCMTSF	Sub Operating Power Control Mode Transition Status Flag	0: Transition completed 1: During transition	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. Depends on the setting of OPCCR.OPCM[2:0].

The SOPCCR register is used to reduce power consumption in normal operating mode, sleep mode, and deep sleep mode by controlling a transition to low-speed operating mode.

Setting this register initiates entry to/exit from low-speed operating mode.

Low-speed operating mode is used for the sub-clock oscillator only.

The OPCCR register cannot be rewritten when the SOPCM bit is 1 (low-speed operating mode).

The SOPCCR register cannot be rewritten under the following conditions:

- When the SOPCCR.SOPCMTSF flag is 1 (during transition)
- Time period from WAIT instruction execution for a sleep mode transition, until exit from sleep mode to normal operation
- Time period from WAIT instruction execution for a deep sleep mode transition, until exit from deep sleep mode to normal operation

This register cannot be rewritten while the flash memory is being programmed or erased (P/E).

For the procedures for changing operating power control modes, refer to Function in section 11.5, Function for Lower Operating Power Consumption.

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 5.1, List of I/O Registers (Address Order)).

SOPCM Bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects operating power control in normal operating mode and sleep mode.

Setting this bit to 1 allows a transition to low-speed operating mode. Setting this bit to 0 allows a return to the operating mode (operating mode set by OPCCR.OPCM[2:0]) before the transition to low-speed operating mode.

Table 11.4 shows the relationship between operating power control modes, the OPCM[2:0] and SOPCM bit settings, and the operating frequency and voltage ranges.

SOPCMTSF Flag (Sub Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the sub operating power control mode is switched. This flag becomes 1 when the value of the SOPCM bit is rewritten, and 0 when mode transition is completed. Read this flag and confirm that it is 0 before proceeding to the next processing. Only rewrite the SOPCM bit when this flag is 0.

Table 11.4 Operating Frequency and Voltage Ranges in Operating Power Control Modes

Operating Power Control Mode	OPCM[2:0] Bits	SOPCM Bit	Operating Voltage Range	Operating Frequency Range						MEMWAIT Bit
				Flash Memory Read Frequency					Flash Memory Programming / Erasure Frequency	
				ICLK	FCLK	PCLKD	PCLKB	PCLKA	FCLK	
High-speed operating mode	000b	0	2.7 to 3.6 V	32 to 54 MHz	Up to 32 MHz	Up to 54 MHz	Up to 32 MHz	Up to 54 MHz	1 to 32 MHz	1*1
				Up to 32 MHz						0/1*1
			2.4 to 2.7 V	Up to 16 MHz	Up to 16 MHz	Up to 32 MHz	Up to 16 MHz	Up to 16 MHz	—	0*2
			1.8 to 2.4 V	Up to 8 MHz	Up to 8 MHz	Up to 8 MHz	Up to 8 MHz	Up to 8 MHz	—	0*2
Middle-speed operating mode	010b	0	2.4 to 3.6 V	Up to 12 MHz	Up to 12 MHz	Up to 12 MHz	Up to 12 MHz	Up to 12 MHz	1 to 12 MHz	0
			1.8 to 2.4 V	Up to 8 MHz	Up to 8 MHz	Up to 8 MHz	Up to 8 MHz	Up to 8 MHz	1 to 8 MHz	0
Low-speed operating mode	000b	1	1.8 to 3.6 V	Up to 32.768 kHz	Up to 32.768 kHz	Up to 32.768 kHz	Up to 32.768 kHz	Up to 32.768 kHz	—	0
	010b	1	1.8 to 3.6 V							

Note: When using the FCLK at lower than 4 MHz during programming or erasing the flash memory, the frequency can be set to 1, 2, or 3 MHz.

Note 1. Change the value according to the procedure for setting the MEMWAIT bit.

Note 2. It is not necessary to set the MEMWAIT bit to 1.

Each operating power control mode is described below.

- High-Speed Operating Mode

The maximum operating frequency during FLASH read is 54 MHz for ICLK, PCLKA, and PCLKD; 32 MHz for PCLKB, and FCLK. The operating voltage range is 1.8 to 3.6 V during FLASH read. However, the maximum operating frequency during FLASH read is 16 MHz for ICLK, FCLK, PCLKA, and PCLKB, and 32 MHz for PCLKD when the operating voltage is 2.4 V or larger and smaller than 2.7 V. The maximum operating frequency during FLASH read is 8 MHz for all the clocks when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

During FLASH programming/erasure, the operating frequency range is 1 to 32 MHz and the operating voltage range is 2.7 to 3.6 V.

The following restriction applies when high-speed operating mode is selected.

- The PLL and USB-dedicated PLL can be used when the operating voltage is 2.4 V or above.

However, the USB cannot be used when the operating voltage is below 3.0 V.

Figure 11.3 shows the operating voltages and frequencies in high-speed operating mode.

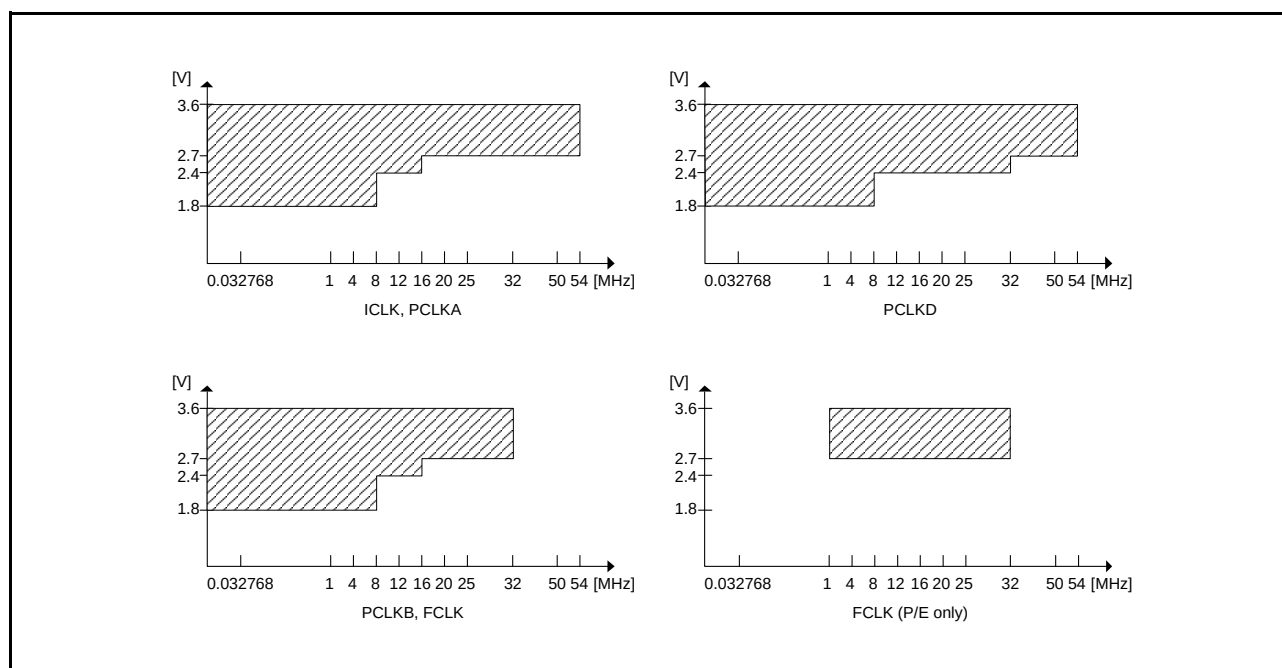


Figure 11.3 Operating Voltages and Frequencies in High-Speed Operating Mode

Note: When using the FCLK at lower than 4 MHz during programming or erasing the flash memory, the frequency can be set to 1, 2, or 3 MHz.

- Middle-Speed Operating Mode

As compared to high-speed operating mode, this mode reduces power consumption for low-speed operation.

The maximum operating frequency during FLASH read is 12 MHz for ICLK, FCLK, PCLKA, PCLKB, and PCLKD.

The operating voltage range is 1.8 to 3.6 V during FLASH read. The maximum operating frequency during FLASH read is 8 MHz for all the clocks when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

During FLASH programming/erasure, the operating frequency range is 1 to 12 MHz and the operating voltage range is 1.8 to 3.6 V. The maximum operating frequency during FLASH programming/erasure is 8 MHz when the operating voltage is 1.8 V or larger and smaller than 2.4 V.

The power consumption of this mode is lower than that of high speed mode under the same conditions.

After a reset is canceled, operation is started from this mode.

The following restriction applies when middle-speed operating mode is selected:

- The PLL and USB-dedicated PLL can be used when the operating voltage is 2.4 V or above.

However, the USB cannot be used when the operating voltage is below 3.0 V.

Figure 11.4 shows the operating voltages and frequencies in middle-speed operating mode.

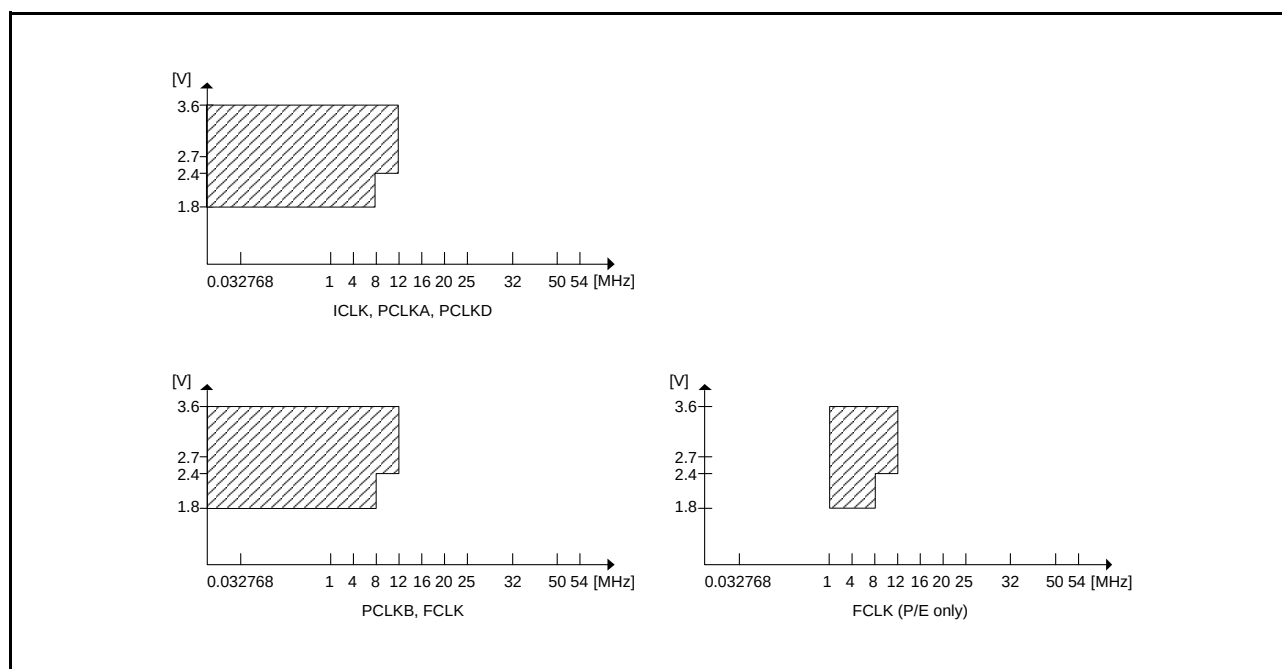


Figure 11.4 Operating Voltages and Frequencies in Middle-Speed Operating Mode

Note: When using the FCLK at lower than 4 MHz during programming or erasing the flash memory, the frequency can be set to 1, 2, or 3 MHz.

- Low-Speed Operating Mode

A transition to low-speed operating mode is set by writing 1 to the SOPCM bit in the SOPCCR register. The setting of the OPCM[2:0] bits cannot be modified during low-speed operating mode. This mode is used only for the sub oscillator of 32.768 kHz.

During reading the flash memory (FLASH), the maximum operating frequency of ICLK, FCLK, PCLKA, PCLKB, and PCLKD is 32.768 kHz. The operating voltage is in the range of 1.8 to 3.6 V.

The following restrictions apply when low-speed operating mode is selected:

- P/E operations for flash memory are prohibited.
- The PLL/USB-dedicated PLL, main clock oscillator, LOCO, and HOCO cannot be used.

Note: The SOPCM bit cannot be set to 1 when the PLLCR2.PLEN bit is 0 (PLL is operating).
 The SOPCM bit cannot be set to 1 when the UPLLCR2.UPLEN bit is 0 (USB-dedicated PLL is operating).
 The SOPCM bit cannot be set to 1 when the HOCOCR.HCSTP bit is 0 (HOCO is operating).
 The SOPCM bit cannot be set to 1 when the MOSCCR.MOSTP bit is 0 (main clock oscillator is operating).
 The SOPCM bit cannot be set to 1 when the LOCOCR.LCSTP bit is 0 (LOCO is operating).

Figure 11.5 shows the operating voltages and frequencies in low-speed operating mode.

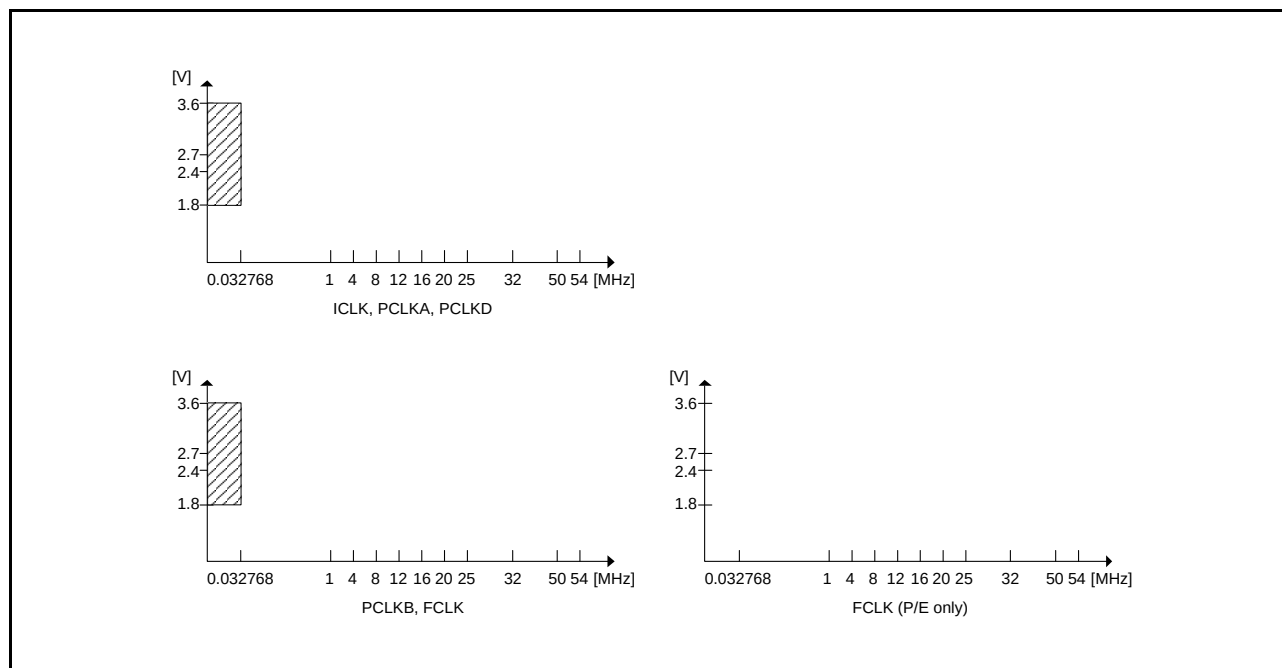
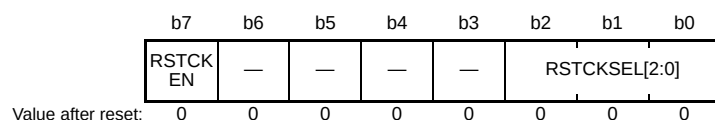


Figure 11.5 Operating Voltages and Frequencies in Low-Speed Operating Mode

11.2.8 Sleep Mode Return Clock Source Switching Register (RSTCKCR)

Address(es): 0008 00A1h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	RSTCKSEL[2:0]	Sleep Mode Return Clock Source Select	b2 b0 0 0 0: LOCO is selected 0 0 1: HOCO is selected*1 0 1 0: Main clock oscillator is selected Settings other than above are prohibited when the RSTCKEN bit is 1.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RSTCKEN	Sleep Mode Return Clock Source Switching Enable	0: Clock source switching at exit from sleep mode is disabled 1: Clock source switching at exit from sleep mode is enabled	R/W

Note: Set the PRCR.PRC1 bit to 1 (write enabled) before rewriting this register.

Note 1. HOCO can only be selected when entering high-speed operating mode.

RSTCKCR is used to control clock source switching at exit from sleep mode.

When exit from sleep mode is initiated by setting RSTCKCR, the main clock oscillator stop bit in the main clock oscillator control register (MOSCCR.MOSTP), the HOCO stop bit in the high-speed on-chip oscillator control register (HOCOCCR.HCSTP), and the LOCO stop bit in the low-speed on-chip oscillator control register (LOCOCR.LCSTP) are automatically modified to the operating state corresponding to the clock source to be used after transition. The value of the RSTCKSEL[2:0] bits is automatically reloaded to the clock source select bits in system clock control register 3 (SCKCR3.CKSEL[2:0]).

RSTCKSEL[2:0] Bits (Sleep Mode Return Clock Source Select)

The RSTCKSEL[2:0] bits select the clock source to be used at exit from sleep mode.

The clock source selected by the RSTCKSEL[2:0] bits is enabled only when the RSTCKEN bit is 1.

As shown in Figure 11.2, Operating Modes, when returning from sleep mode to high-speed operating mode, the LOCO, HOCO, or main clock oscillator can be selected. When returning from sleep mode to middle-speed operating mode, the LOCO or main clock oscillator can be selected. However, in this case, the frequency of each clock (ICLK, FCLK, PCLKA, PCLKB, and PCLKD) must be lower than 12 MHz when the power supply voltage is 2.4 V or above, and lower than 8 MHz when the voltage is below 2.4 V.

Table 11.5 When Exiting Sleep Mode to High-Speed Operating Mode and Middle-Speed Operating Mode

Operating Mode during Sleep	Clock Source during Sleep	RSTCKSEL	Operating Mode after Exiting	Clock Source after Exiting
High-speed operating mode or low-speed operating mode after exit from high-speed operating mode	Sub-clock oscillator	000b (LOCO)	High-speed operating mode	LOCO
		001b (HOCO)		HOCO
		010b (main clock oscillator)		Main clock oscillator
Middle-speed operating mode or low-speed operating mode after exit from middle-speed operating mode	Sub-clock oscillator	000b (LOCO)	Middle-speed operating mode	LOCO
		010b (main clock oscillator)		Main clock oscillator*1

Note 1. The frequency of each clock (ICLK, FCLK, PCLKA, PCLKB, and PCLKD) must be lower than 12 MHz when the power supply voltage is 2.4 V or above, and lower than 8 MHz when the voltage is below 2.4 V.

RSTCKEN Bit (Sleep Mode Return Clock Source Switching Enable)

The RSTCKEN bit enables or disables clock source switching when sleep mode is exited.

The clock source can be switched when exiting sleep mode only while the sub-clock oscillator is selected as the clock for entering sleep mode. Do not enable this bit when entering sleep mode while the HOCO, LOCO, main clock oscillator, or PLL is selected as the clock source.

When returning from sleep mode while this bit is enabled, the SOPCM bit in the SOPCCR register is automatically rewritten to 0 (middle-speed operating mode or high-speed operating mode).

The value of the frequency division setting (in the SCKCR register) is retained.

To exit sleep mode to middle-speed operating mode when the main clock oscillator is selected, the frequency of each clock must be lower than 12 MHz when the power supply voltage is 2.4 V or above, and lower than 8 MHz when the voltage is below 2.4 V.

11.3 Reducing Power Consumption by Switching Clock Signals

The clock frequency can change by setting the SCKCR.FCK[3:0], ICK[3:0], PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits. The CPU, DMAC, DTC, ROM, and RAM clocks can be set by the ICK[3:0] bits. The peripheral module clocks can be set by the PCKA[3:0], PCKB[3:0], and PCKD[3:0] bits.

The flash memory clock can be set by the FCK[3:0] bits.

For details, refer to section 9, Clock Generation Circuit.

11.4 Module Stop Function

The module stop function can be set for each on-chip peripheral module.

When the MSTPmi bit (m = A to D; i = 0 to 31) in MSTPCRA to MSTPCRD is set to 1, the specified module stops operating and enters the module stop state, but the CPU continues to operate independently. When the corresponding MSTPmi bit is set to 0, the module exits the module state and restarts operating at the end of the bus cycle. The internal states of modules are retained in the module stop state.

After a reset is canceled, all modules other than the DMAC, DTC, and on-chip RAM are in the module stop state.

Basically the registers in the module stop state cannot be read or written. However, note that data may be written to these registers if write access is made immediately after the setting of the module stop state. To avoid this, always write to the module stop registers after confirming that the last register setting is done.

11.5 Function for Lower Operating Power Consumption

By selecting an appropriate operating power control mode according to the operating frequency and operating voltage, power consumption can be reduced in normal mode, sleep mode, and deep sleep mode.

11.5.1 Setting Operating Power Control Mode

Examples of the procedures for switching operating power control modes are shown below:

(1) Switching from Normal Power Consumption Mode to Low Power Consumption Mode

- Example 1: From high-speed operating mode to middle-speed operating mode

(High-speed operation in high-speed operating mode)



Set the frequency of each clock to lower than the maximum operating frequency for middle-speed operating mode



Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)



Set the OPCCR.OPCM[2:0] bits to 010b (middle-speed operating mode)



Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)



(Middle-speed operation in middle-speed operating mode)

- Example 2: From high-speed/middle-speed operating mode to low-speed operating mode

(High-speed operation in high-speed operating mode/middle-speed operation in middle-speed operating mode)



Set the frequency of each clock to lower than the maximum operating frequency for low-speed operating mode



Confirm that all clock sources but the sub-clock oscillator are stopped



Confirm that the SOPCCR.SOPCMTSF flag is 0 (transition completed)



Set the SOPCCR.SOPCM bit to 1 (low-speed operating mode)



Confirm that the SOPCCR.SOPCMTSF flag is 0 (transition completed)



Low-speed operation in low-speed operating mode

(2) Switching from Low Power Consumption Mode to Normal Power Consumption Mode

- Example 1: From low-speed operating mode to high-speed/middle-speed operating mode

Low-speed operation in low-speed operating mode



Confirm that the SOPCCR.SOPCMTSF flag is 0 (transition completed)



Set the SOPCCR.SOPCM bit to 0 (high-speed operating mode or middle-speed operating mode)



Confirm that the SOPCCR.SOPCMTSF flag is 0 (transition completed)



Set the frequency of each clock to lower than the maximum operating frequency for high-speed/middle-speed operating mode



(High-speed operation in high-speed operating mode/middle-speed operation in middle-speed operating mode)

- Example 2: From middle-speed operating mode to high-speed operating mode

Middle-speed operation in middle-speed operating mode



Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)



Set the OPCCR.OPCM[2:0] bit to 0 (high-speed operating mode)



Confirm that the OPCCR.OPCMTSF flag is 0 (transition completed)



Set the frequency of each clock to lower than the maximum operating frequency for high-speed operating mode



High-speed operation in high-speed operating mode

11.6 Low Power Consumption Modes

11.6.1 Sleep Mode

11.6.1.1 Entry to Sleep Mode

When the WAIT instruction is executed while the SBYCR.SSBY bit is 0, the CPU enters sleep mode. In sleep mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop.

When the WDT is used, the WDT stops counting when sleep mode is entered.

Counting by the IWDT stops if a transition to sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to sleep mode is made while the IWDT is being used in register start mode and the IWDTCSSTPR.SLCSTP bit is 1.

Furthermore, counting by the IWDT continues if a transition to sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low power consumption modes). In the same way, counting by the IWDT continues if a transition to sleep mode is made while the IWDT is being used in register start mode and the IWDTCSSTPR.SLCSTP bit is 0.

To use sleep mode, make the following settings and then execute a WAIT instruction.

- (1) Set the PSW.I bit*¹ of the CPU to 0.
- (2) Set the interrupt request destination*² to be used for exit from sleep mode.
- (3) Set the priority*³ of the interrupt to be used for exit from sleep mode to a level higher than the setting of the PSW.IPL[3:0] bits*¹ of the CPU.
- (4) Set the IERm.IENj bit*³ to 1 for the interrupt.
- (5) Read the I/O register that is written last and confirm that the written value has been reflected.
- (6) Execute the WAIT instruction (this automatically sets the I bit*¹ in the PSW of the CPU to 1).

Note 1. For details, refer to section 2, CPU.

Note 2. For details, refer to section 15.4.3, Selecting Interrupt Request Destinations.

Note 3. For details, refer to section 15, Interrupt Controller (ICUb).

11.6.1.2 Exit from Sleep Mode

Exit from sleep mode is initiated by any interrupt, a RES# pin reset, a power-on reset, a voltage monitoring reset, or a reset caused by an IWDT underflow.

- Initiated by an interrupt
An interrupt initiates exit from sleep mode and the interrupt exception handling starts. If a maskable interrupt has been masked by the CPU (the priority level*¹ of the interrupt has been set to a value lower than that of the PSW.IPL[3:0] bits*² of the CPU), sleep mode is not exited.
- Initiated by a RES# pin reset
When the RES# pin is driven low, the MCU enters the reset state. When the RES# pin is driven high after the reset signal is input for a predetermined time period, the CPU starts the reset exception handling.
- Initiated by a power-on reset
A power-on reset asserts a reset to the MCU.
When a power-on reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by a voltage monitoring reset
A voltage monitoring reset asserts a reset to the MCU.
When a voltage monitoring reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by an independent watchdog timer reset
An internal reset generated by an IWDT underflow asserts a reset to the MCU. However, when IWDT counting is stopped in sleep mode by setting OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1, the IWDT is stopped in sleep mode and sleep mode is not exited by the independent watchdog timer reset.

Note 1. For details, refer to section 15, Interrupt Controller (ICUb).

Note 2. For details, refer to section 2, CPU.

11.6.1.3 Sleep Mode Return Clock Source Switching Function

To switch the clock source used for exit from sleep mode, set the sleep mode return clock source switching register (RSTCKCR) and the wait control register for each clock. When the return interrupt is generated, after oscillation settling of the oscillator specified as the return clock, the clock source is automatically switched, and then operation exits sleep mode. At this time, the registers related to clock source switching are automatically rewritten.

For details, refer to section 11.2.8, Sleep Mode Return Clock Source Switching Register (RSTCKCR).

For details on settings the oscillation stabilization wait time, refer to section 9.2.16, Main Clock Oscillator Wait Control Register (MOSCWTCR).

11.6.2 Deep Sleep Mode

11.6.2.1 Entry to Deep Sleep Mode

When a WAIT instruction is executed with the MSTPCRC.DSLPE bit set to 1, the MSTPCRA.MSTPA28 bit set to 1, and the SBYCR.SSBY bit cleared to 0, a transition to deep sleep mode is made.

In deep sleep mode, the CPU and the DMAC, DTC, ROM, and RAM clocks stop. Peripheral functions do not stop.

When the WDT is used, the WDT stops counting when deep sleep mode is entered.

Counting by the IWDT stops if a transition to deep sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to deep sleep mode is made while the IWDT is being used in register start mode and the IWDTCSSTPR.SLCSTP bit is 1.

Furthermore, counting by the IWDT continues if a transition to deep sleep mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low power consumption modes). In the same way, counting by the IWDT continues if a transition to deep sleep mode is made while the IWDT is being used in register start mode and the IWDTCSSTPR.SLCSTP bit is 0.

To use deep sleep mode, make the following settings and then execute a WAIT instruction.

- (1) Set the PSW.I bit*¹ of the CPU to 0.
- (2) Set the interrupt request destination*² to be used for exit from deep sleep mode.
- (3) Set the priority*³ of the interrupt to be used for exit from deep sleep mode to a level higher than the setting of the PSW.IPL[3:0] bits*¹ of the CPU.
- (4) Set the IERm.IENj bit*³ to 1 for the interrupt.
- (5) Read the I/O register that is written last and confirm that the written value has been reflected.
- (6) Execute a WAIT instruction (executing a WAIT instruction causes automatic setting of the PSW.I bit*¹ of the CPU to 1).

Note 1. For details, refer to section 2, CPU.

Note 2. For details, refer to section 15.4.3, Selecting Interrupt Request Destinations.

Note 3. For details, refer to section 15, Interrupt Controller (ICUb).

11.6.2.2 Exit from Deep Sleep Mode

Exit from deep sleep mode is initiated by any interrupt, a RES# pin reset, a power-on reset, a voltage monitoring reset, or a reset caused by an IWDT underflow.

- Initiated by an interrupt
An interrupt initiates exit from deep sleep mode and the interrupt exception handling starts. If a maskable interrupt has been masked by the CPU (the priority level*¹ of the interrupt has been set to a value lower than that of the PSW.IPL[3:0] bits*² of the CPU), deep sleep mode is not exited.
- Initiated by the RES# pin reset
When the RES# pin is driven low, the MCU enters the reset state. When the RES# pin is driven high after the reset signal is input for a predetermined time period, the CPU starts the reset exception handling.
- Initiated by a power-on reset
A power-on reset asserts a reset to the MCU.
When a power-on reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by a voltage monitoring reset
A voltage monitoring reset asserts a reset to the MCU.
When a voltage monitoring reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.
- Initiated by the independent watchdog timer
An internal reset generated by an IWDT underflow asserts a reset to the MCU. However, when IWDT counting is stopped in deep sleep mode by setting OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1, the IWDT is stopped in deep sleep mode and deep sleep mode is not exited by the independent watchdog timer reset.

Note 1. For details, refer to section 15, Interrupt Controller (ICUb).

Note 2. For details, refer to section 2, CPU.

11.6.3 Software Standby Mode

11.6.3.1 Entry to Software Standby Mode

When a WAIT instruction is executed with the SBYCR.SSBY bit set to 1, a transition to software standby mode is made. In this mode, the CPU, on-chip peripheral functions, and all the other functions except the sub-clock oscillator stop. However, the contents of the CPU internal registers, RAM data, the states of on-chip peripheral functions, the I/O ports, and the sub-clock oscillator are retained. Software standby mode allows significant reduction in power consumption because the oscillator stops in this mode.

Set the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0 before executing the WAIT instruction.

When the WDT is used, the WDT stops counting when software standby mode is entered.

Counting by the IWDT stops if a transition to software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 1. In the same way, counting by the IWDT stops if a transition to software standby mode is made while the IWDT is being used in register start mode and the IWDTCSLTPR.SLCSTP bit is 1.

Furthermore, counting by the IWDT continues if a transition to software standby mode is made while the IWDT is being used in auto-start mode and the OFS0.IWDTSLCSTP bit is 0 (counting by the IWDT continues through transitions to low power consumption modes). In the same way, counting by the IWDT continues if a transition to software standby mode is made while the IWDT is being used in register start mode and the IWDTCSLTPR.SLCSTP bit is 0.

To use software standby mode, make the following settings and then execute a WAIT instruction.

- (1) Set the PSW.I bit*¹ of the CPU to 0.
- (2) Set the interrupt request destination*² to be used for recovery from software standby mode to the CPU.
- (3) Set the priority*³ of the interrupt to be used for recovery from software standby mode to a level higher than the setting of the PSW.IPL[3:0] bits*¹ of the CPU.
- (4) Set the IERm.IENj bit*³ to 1 for the interrupt.
- (5) Read the I/O register that is written last and confirm that the written value has been reflected.
- (6) Execute a WAIT instruction (executing a WAIT instruction causes automatic setting of the PSW.I bit*¹ of the CPU to 1).

Note 1. For details, refer to section 2, CPU.

Note 2. For details, refer to section 15.4.3, Selecting Interrupt Request Destinations.

Note 3. For details, refer to section 15, Interrupt Controller (ICUb).

11.6.3.2 Exit from Software Standby Mode

Exit from software standby mode is initiated by an external pin interrupt (the NMI, IRQ0, IRQ1, IRQ4 to IRQ7), peripheral function interrupts (the RTC alarm, RTC interval, IWDT, voltage monitoring, VBATT pin voltage drop detection, USB, and ELC (LPT-dedicated interrupt)), a RES# pin reset, a power-on reset, a voltage monitoring reset, or an independent watchdog timer reset. When any trigger which initiates exit from software standby mode is asserted, the oscillators which were operating before entry to software standby mode restart operation. After the oscillation of all these oscillators has been stabilized, operation returns from software standby mode.

- Initiated by an interrupt

When an interrupt request from among the NMI, IRQ0, IRQ1, IRQ4 to IRQ7, RTC alarm, RTC interval, IWDT, voltage monitoring, VBATT pin voltage drop detection, USB, and ELC (LPT-dedicated interrupt) interrupts is generated, each of the oscillators which was operating before the transition to software standby mode resumes oscillation. After the oscillation stabilization wait time of each oscillator set by the MOSCWTCR.MSTS[4:0] bits has elapsed, the MCU exits software standby mode and interrupt exception processing starts.

- Initiated by a RES# pin reset

Clock oscillation starts when the low level is applied to the RES# pin. Clock supply for the MCU starts at the same time. Keep the level on the RES# pin low over the time required for oscillation of the clocks to become stable. Reset exception processing starts when the high level is applied to the RES# pin.

- Initiated by a power-on reset

A power-on reset asserts a reset to the MCU.

When a power-on reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.

- Initiated by a voltage monitoring reset

A voltage monitoring reset asserts a reset to the MCU.

When a voltage monitoring reset is negated by a rise in the supply voltage, the CPU starts the reset exception handling.

- Initiated by an independent watchdog timer reset

An internal reset generated by an IWDT underflow asserts a reset to the MCU.

Note that the independent watchdog timer is stopped in software standby mode due to the register settings (OFS0.IWDTSTRT = 0 and OFS0.IWDTSLCSTP = 1, or OFS0.IWDTSTRT = 1 and IWDTCSTPR.SLCSTP = 1) in software standby mode. In that case, exit from software standby mode by the independent watchdog timer reset cannot be done.

11.6.3.3 Example of Software Standby Mode Application

Figure 11.6 shows an example of entry to software standby mode by the falling edge of the IRQn pin, and exit from software standby mode by the rising edge of the IRQn pin.

In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 01b (falling edge), and then the IRQCRi.IRQMD[1:0] bits are set to 10b (rising edge). After that, the SBYCR.SSBY bit is set to 1 and the WAIT instruction is executed. Thus entry to software standby mode is completed. After that, exit from software standby mode is initiated by the rising edge of the IRQn pin.

To exit software standby mode, settings of the interrupt controller (ICU) are also necessary. For details, refer to section 15, Interrupt Controller (ICUb).

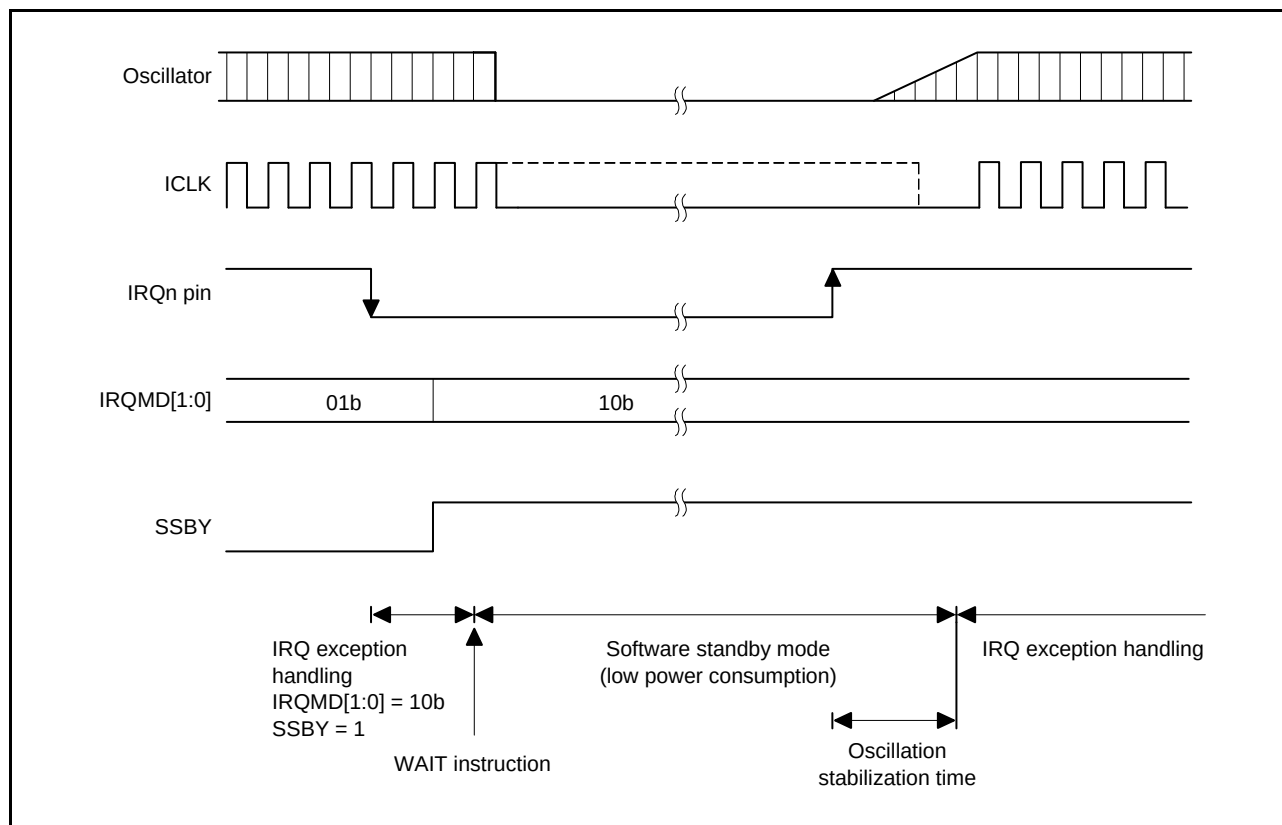


Figure 11.6 Example of Software Standby Mode Application

11.7 Usage Notes

11.7.1 I/O Port States

I/O port states are retained in software standby mode. Therefore, the supply current is not reduced if output signals are high level.

11.7.2 Module Stop State of DMAC and DTC

Before setting the MSTPCRA.MSTPA28 bit to 1, set the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0 to avoid activating the DMAC and DTC.

For details, refer to section 18, DMA Controller (DMACA) and section 19, Data Transfer Controller (DTCa).

11.7.3 On-Chip Peripheral Module Interrupts

Interrupts do not operate in the module stop state. Therefore, if the module stop state is made after an interrupt request is generated, a CPU interrupt source or a DTC startup source cannot be cleared. For this reason, disable interrupts before entering the module stop state.

11.7.4 Write Access to MSTPCRA, MSTPCRB, MSTPCRC, and MSTPCRD

Write accesses to MSTPCRA, MSTPCRB, MSTPCRC, and MSTPCRD should be made only by the CPU.

11.7.5 Timing of WAIT Instructions

The WAIT instruction is executed before completion of the preceding register write. The WAIT instruction being executed before the register setting is modified may cause unintended operation. To avoid this, always execute the WAIT instruction after confirming that the last register setting is done.

11.7.6 Rewrite the Register by DMAC and DTC in Sleep Mode

The WDT stops in sleep mode. Do not set up the DMAC and DTC to rewrite any registers related to the WDT while the chip is in sleep mode.

Depending on the settings of the OFS0.IWDTSLCSTP bit and IWDTCTPR.SLCSTP bit, the IWDT may also stop in sleep mode. To avoid this, do not set up the DMAC and DTC to rewrite any registers related to the IWDT in sleep mode. The RSTCKCR register is a register that switches the clock source at exit from sleep mode. Changing the RSTCKCR register in sleep mode causes unintended operation, so do not write to this register in sleep mode.

12. Battery Backup Function

12.1 Overview

When the voltage at the VCC pin is dropped, power can be supplied to the realtime clock (RTC) and the sub-clock oscillator placed in the battery backup power area from the battery backup power pin (VBATT pin).

When the battery backup function is not used, connect the VBATT pin to the VCC pin and disable the battery backup function (set the VBATTTCR.VBATTDIS bit to 1).

The VBATT pin voltage level and battery backup power voltage drop detection can be confirmed by reading the VBATT status register.

Figure 12.1 shows the configuration of the battery backup function.

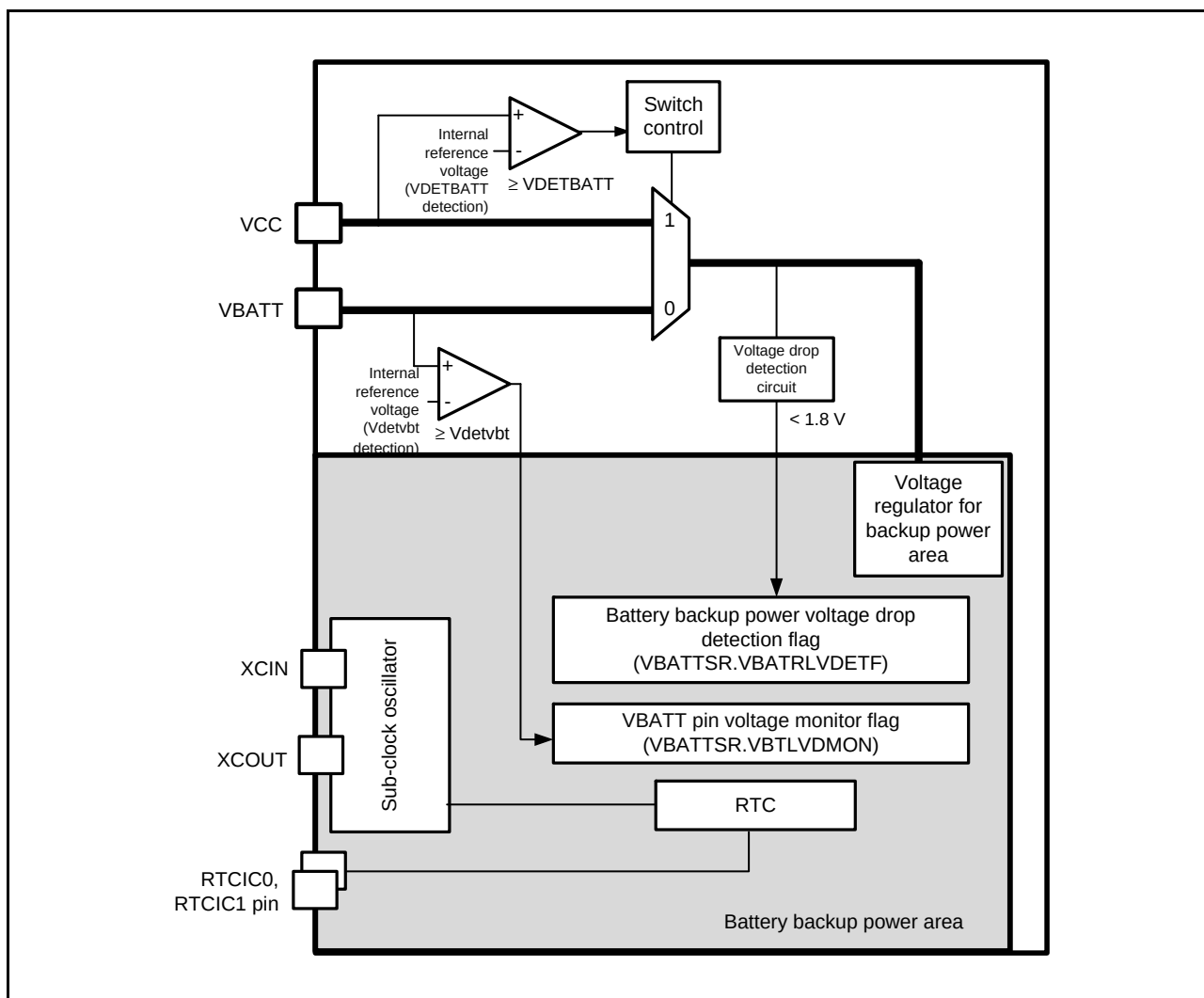


Figure 12.1 Configuration of Battery Backup Function

12.2 Register Descriptions

12.2.1 VBATT Control Register (VBATTCCR)

Address(es): 0008 C29Dh

b7	b6	b5	b4	b3	b2	b1	b0
VBTLVDLVL[1:0]	—	VBTLVDEN	—	—	—	—	VBATTDIS
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	VBATTDIS	Battery Backup Function Disable	0: Battery backup function enabled 1: Battery backup function disabled	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	VBTLVDEN	VBATT Pin Voltage Drop Detection Enable	0: VBATT pin voltage drop detection disabled 1: VBATT pin voltage drop detection enabled	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	VBTLVDLVL[1:0]	VBATT Pin Voltage Drop Detection Level Select	b7 b6 1 0: 2.20 V 1 1: 2.00 V Settings other than above are prohibited.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The VBATTCCR register is used to control operation of the battery backup function.

VBATTDIS Bit (Battery Backup Function Disable)

This bit is used to enable or disable the function for switching the power supply to the backup power area from VCC supply to battery backup power pin (VBATT pin) supply when the voltage at the VCC drops.

When the battery backup function is not used, set the VBATTDIS bit to 1 (battery backup function disabled).

VBTLVDEN Bit (VBATT Pin Voltage Drop Detection Enable)

This bit is used to enable or disable the voltage drop detection function of the VBATT pin.

VBTLVDLVL[1:0] Bits (VBATT Pin Voltage Drop Detection Level Select)

These bits are used to select the detection voltage level (Vdetvbt) when the voltage drop detection function of the VBATT pin is enabled.

VBTLVDLVL bits are enabled when the VBATTCCR.VBATTDIS bit is 0 (battery backup function enabled).

12.2.2 VBATT Status Register (VBATTSR)

Address(es): 0008 C29Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VBTLVDMON	VBATRLVDETF
Value after reset:	0	0	0	0	0	0	1	X

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	VBATRLVDETF	Battery Backup Power Voltage Drop Detection Flag	0: Battery backup power voltage drop (< 1.8 V) not detected 1: Battery backup power voltage drop (< 1.8 V) detected	R/W*1
b1	VBTLVDMON	VBATT Pin Voltage Monitor Flag	0: VBATT pin voltage < Vdetvbt 1: VBATT pin voltage ≥ Vdetvbt or VBATT pin voltage drop detection disabled	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

Note 1. Only 0 can be written after 1 is read.

VBATRLVDETF Flag (Battery Backup Power Voltage Drop Detection Flag)

This flag indicates whether the battery backup power voltage has dropped below 1.8 V.

[Setting condition]

- When the battery backup power voltage drops below 1.8 V.

[Clearing condition]

- When 0 is written to the VBATRLVDETF flag after the VBATTSR register is read while this flag is 1.

By setting the VBATRLVDETF flag to 0 after reading as 1 and enabling the backup function (by setting VBATTCCR.VBATTDIS to 0) after power-on, whether the battery backup power voltage has dropped while the VCC is low can be confirmed when the VCC rises again after the VCC drops and the power supply is switched to VBATT pin supply.

VBTLVDMON Flag (VBATT Pin Voltage Monitor Flag)

This flag indicates whether the VBATT pin voltage is below Vdetvbt.

This flag is enabled when the VBATTCCR.VBATTDIS bit is 0 (battery backup function enabled) and the VBATTCCR.VBTLVDEN bit is 1 (VBATT pin voltage drop detection enabled).

12.2.3 VBATT Pin Voltage Drop Detection Interrupt Control Register (VBTLVDICR)

Address(es): 0008 C29Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	VBTLV DISEL	VBTLV DIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	VBTLVDIE	VBATT Pin Voltage Drop Detection Interrupt Enable	0: VBATT pin voltage drop detection interrupt disabled 1: VBATT pin voltage drop detection interrupt enabled	R/W
b1	VBTLVDISEL	VBATT Pin Voltage Drop Detection Interrupt Enable Type Selects	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

12.3 Operation

12.3.1 Battery Backup Function

When the voltage at the VCC pin is dropped, power can be supplied to the RTC and sub-clock oscillator from the VBATT pin. When the power supply reduction from the VCC pin is detected, connection to power is switched to the power supply from the VBATT pin. The power supply from the VCC pin is resumed when the voltage at the VCC pin exceeds VDET BATT while the RTC is operating on the power supply from the VBATT pin. This power supply change does not affect the RTC operation. When the voltage level at the VBATT pin voltage falls below the operation guaranteed voltage, operation of the RTC cannot be guaranteed.

To use the battery backup function, enable the voltage monitoring 0 reset (set the OFS1.LVDAS bit to 0) and select 2.51 V as the voltage detection 0 level (set OFS1.VDSEL[1:0] to 10b) in advance.

The power is supplied to the following modules from the VBATT pin.

- RTC
- Sub-clock oscillator (including XCIN and XCOU pins)
- RTCIC0 (P30), RTCIC1 (P31)

Figure 12.2 shows the operation for switching to the battery backup function.

Figure 12.3 shows the operation example of the VBATT pin power voltage monitor flag, and Figure 12.4 shows the operation example of the battery backup power voltage drop detection flag.

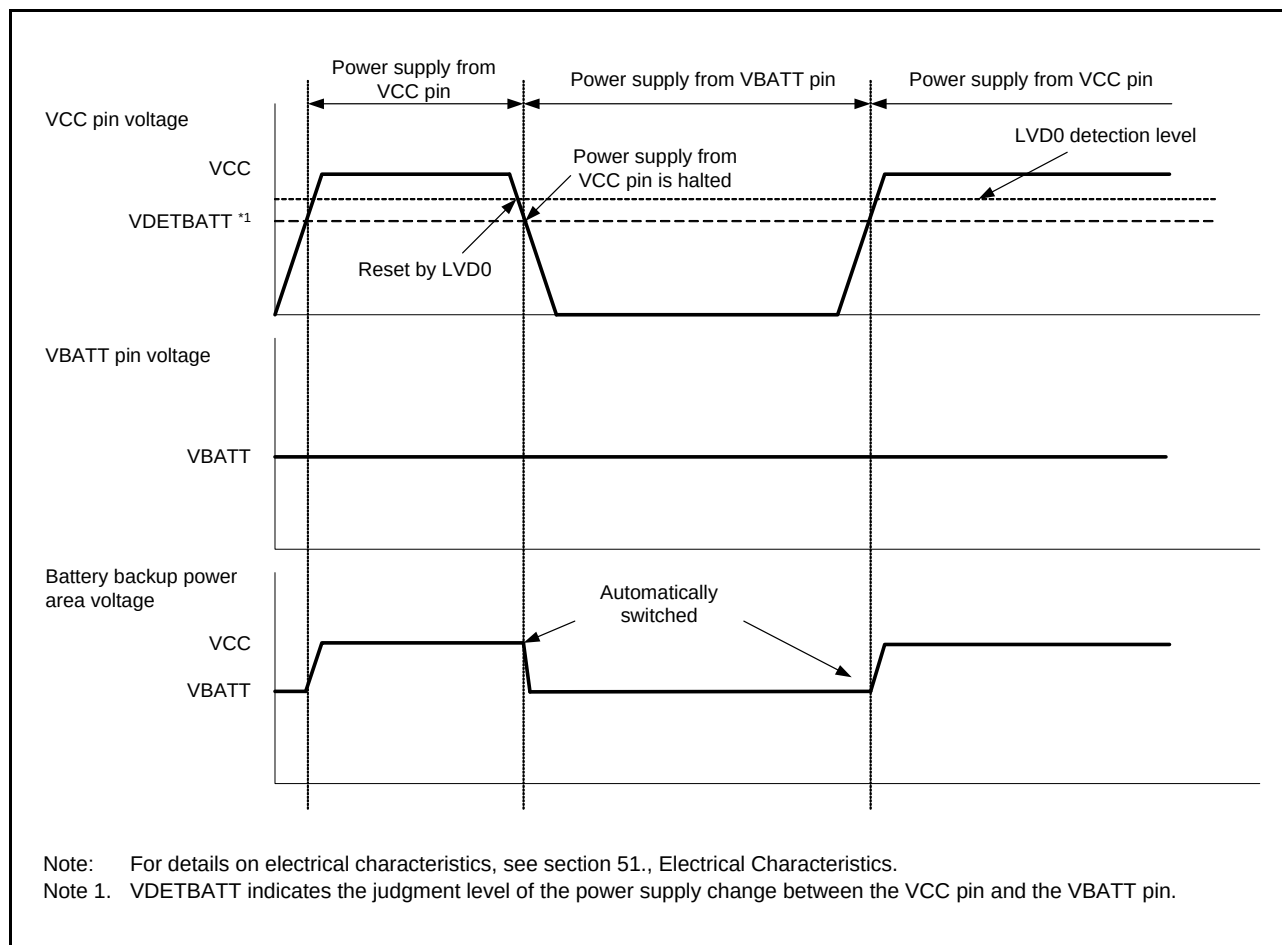


Figure 12.2 Operation for Switching to Battery Backup Function

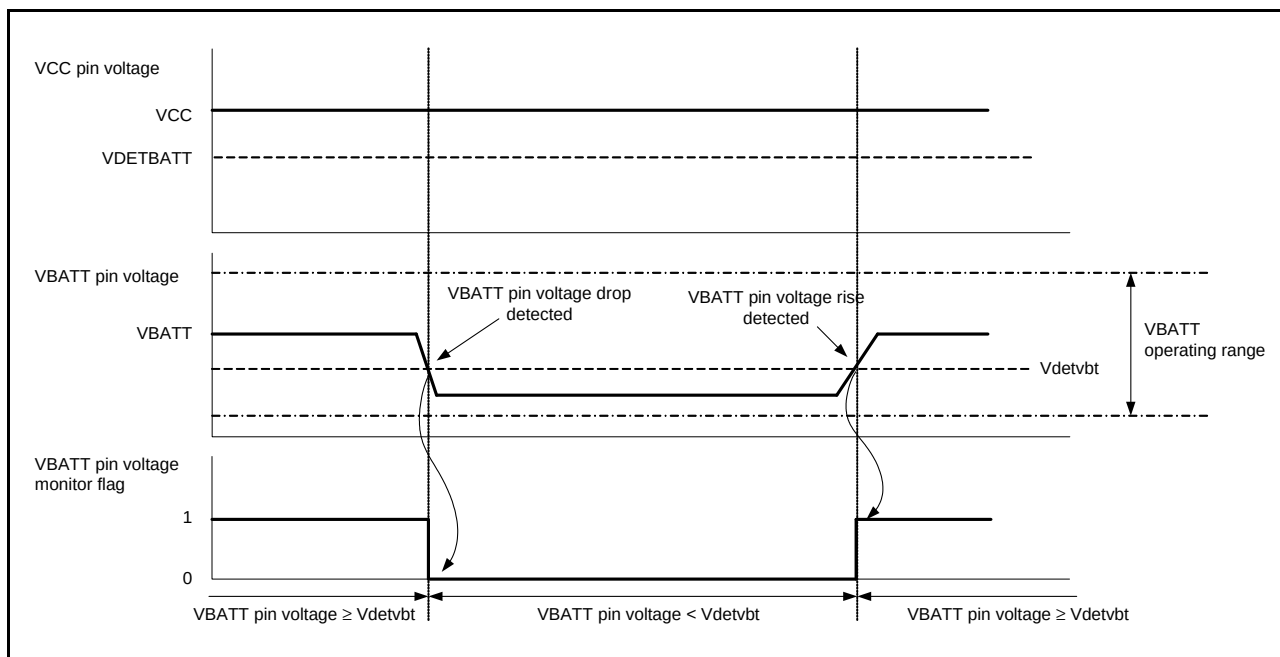


Figure 12.3 Operation Example of the VBATT Pin Power Voltage Monitor Flag

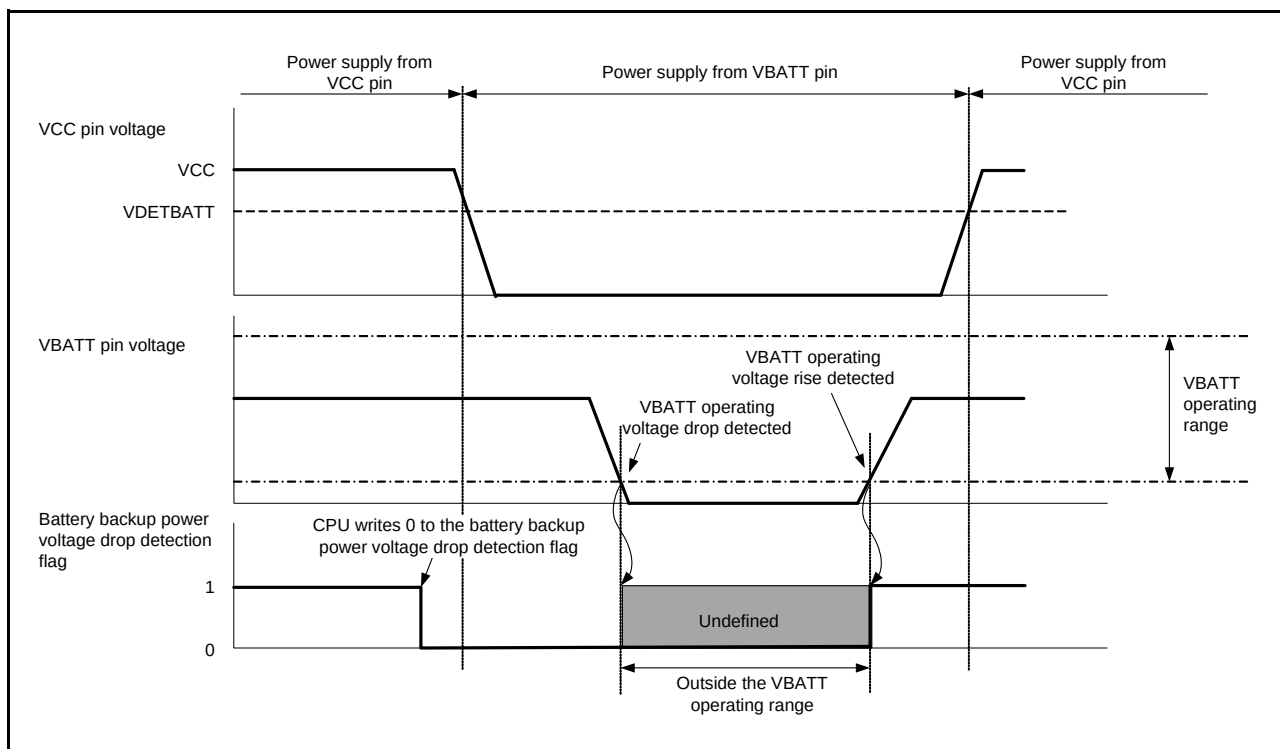


Figure 12.4 Operation Example of the Battery Backup Power Voltage Drop Detection Flag

12.3.2 VBATT Pin Voltage Monitoring Function

When the VCC is supplied, the VBATT pin voltage can be monitored. This function is disabled after a reset.

After the VBATT pin voltage drop detection enable bit (VBATTCR.VBTLVDEN) is set to 1, the VBATT pin voltage level can be monitored by reading the VBATT pin voltage monitor flag (VBATTSR.VBTLVDMON).

12.4 Usage Notes

1. When the VBATT pin is not used, connect the VBATT pin to the VCC pin.
2. When the battery backup function is not used, set the VBATTCR.VBATTDIS bit to 1 (battery backup function disabled).
3. When the voltage level at the VBATT is lower than the guaranteed operation range, operation of the sub-clock and RTC cannot be guaranteed. The RTC must be initialized to restart power supply after the VBATT pin falls below the operation guaranteed voltage.
4. Writing to the RTC registers should be performed while power is being supplied from the VCC pin.
5. When VCC is higher than VDET_{BATT}, the VCC pin and VBATT pin are not connected by means of circuitry. When VCC is lower than VDET_{BATT} and the switch is connected to the VBATT pin, if the voltage at the VBATT pin becomes lower than VCC - 0.6 V, current may flow into the VBATT pin through the parasitic diode between the VCC and VBATT pins.

13. Register Write Protection Function

The register write protection function protects important registers from being overwritten for in case a program runs out of control. The registers to be protected are set with the protect register (PRCR).

Table 13.1 lists the association between the PRCR bits and the registers to be protected.

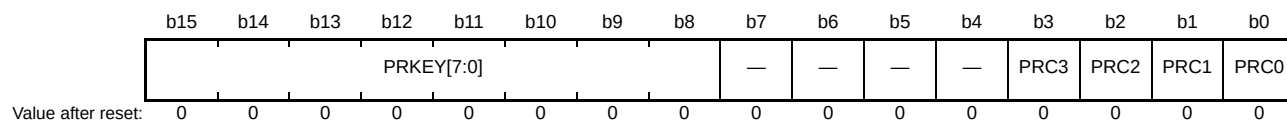
Table 13.1 Association between PRCR Bits and Registers to be Protected

PRCR Bit	Register to be Protected
PRC0	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3
PRC1	- Register related to the operating modes: SYSCR1 - Registers related to low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR - Registers related to the clock generation circuit: MOFCR, MOSCWTCR - Software reset register: SWRR
PRC2	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3	- Registers related to the LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR - Registers related to the battery backup function: VBATTTCR, VBATTSR, VBTLDICR

13.1 Register Descriptions

13.1.1 Protect Register (PRCR)

Address(es): 0008 03FEh



Bit	Symbol	Bit Name	Description	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to operating modes, low power consumption functions, the clock generation circuit, and software reset. 0: Write disabled 1: Write enabled	R/W
b2	PRC2	Protect Bit 2	Enables writing to the registers related to the low power timer. 0: Write disabled 1: Write enabled	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD. 0: Write disabled 1: Write enabled	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control permission and prohibition of writing to the PRCR register. To modify the PRCR register, write A5h to the 8 higher-order bits and the desired value to the 8 lower-order bits as a 16-bit unit.	R/W*1

Note 1. Write data is not retained.

PRCi Bits (Protect Bit i) (i = 0 to 3)

These bits enable or disable writing to the corresponding registers to be protected.

Setting the PRCi bits to 1 and 0 enable and disable writing to the corresponding registers to be protected, respectively.

14. Exception Handling

14.1 Exception Events

During execution of a program by the CPU, the occurrence of a certain event may cause execution of that program to be suspended and execution of another program to be started. Such kinds of events are called exception events.

The RXv2 CPU supports eight types of exceptions. The types of exception events are shown in Figure 14.1.

The occurrence of an exception causes the processor mode to shift to supervisor mode.

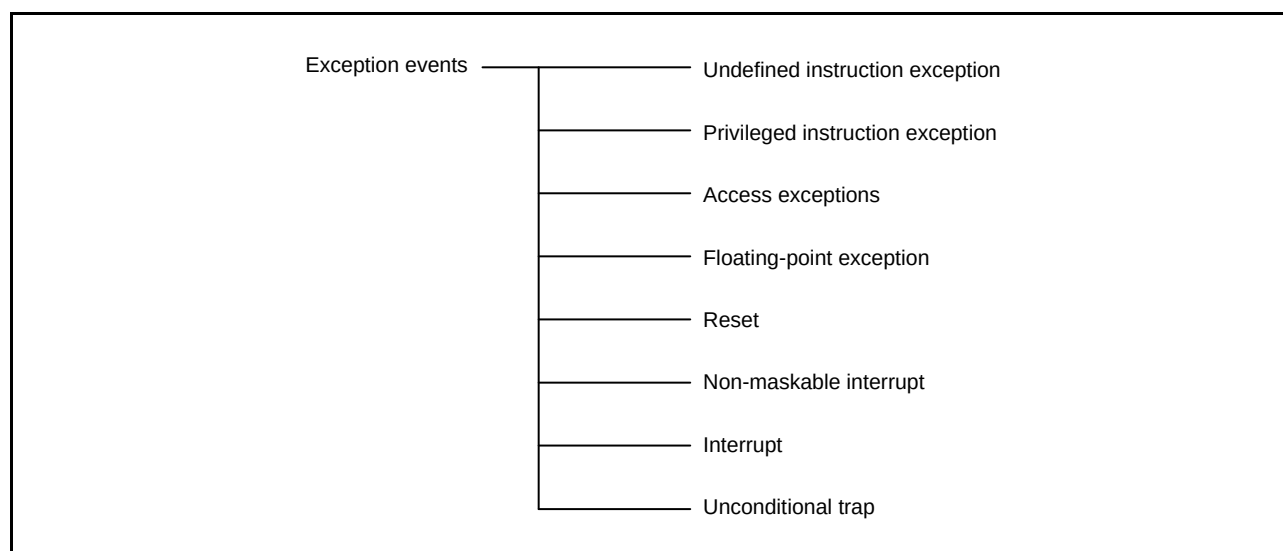


Figure 14.1 Types of Exception Events

14.1.1 Undefined Instruction Exception

An undefined instruction exception occurs when execution of an undefined instruction (an instruction not implemented) is detected.

14.1.2 Privileged Instruction Exception

A privileged instruction exception occurs when execution of a privileged instruction is detected in user mode. Privileged instructions can be executed only in supervisor mode.

14.1.3 Access Exceptions

An access exception occurs when an error is detected in access to memory by the CPU. If the memory-protection unit detects an instruction memory-protection error, an instruction-access exception occurs, and if the unit detects a data memory protection error, an operand-access exception occurs.

14.1.4 Floating-Point Exception

Floating-point exceptions include the five exception events (overflow, underflow, inexact, division-by-zero, and invalid operation) specified in the IEEE754 standard and another floating-point exception that is generated on detection of unimplemented processing. The exception handling of floating-point exceptions is prohibited when the EX, EU, EZ, EO, or EV bit in FPSW is 0.

14.1.5 Reset

A reset is generated by input of a reset signal to the CPU. This has the highest priority of any exception and is always accepted.

14.1.6 Non-Maskable Interrupt

The non-maskable interrupt is generated by input of a non-maskable interrupt signal to the CPU and is only used when a fatal fault is considered to have occurred in the system. Never use the non-maskable interrupt with an attempt to return to the program that was being executed at the time of interrupt generation after the exception handling routine is ended.

14.1.7 Interrupt

Interrupts are generated by the input of interrupt signals to the CPU. A fast interrupt can be selected as the interrupt with the highest priority. In the case of the fast interrupt, hardware pre-processing and hardware post-processing are handled fast. The priority level of the fast interrupt is 15 (the highest). The exception handling of interrupts is masked when the I bit in PSW is 0.

14.1.8 Unconditional Trap

An unconditional trap is generated when the INT or BRK instruction is executed.

14.2 Exception Handling Procedure

In the exception handling, part of the processing is handled automatically by hardware and part of it is handled by a program (exception handling routine) that has been written by the user. Figure 14.2 shows the processing procedure when an exception other than a reset is accepted.

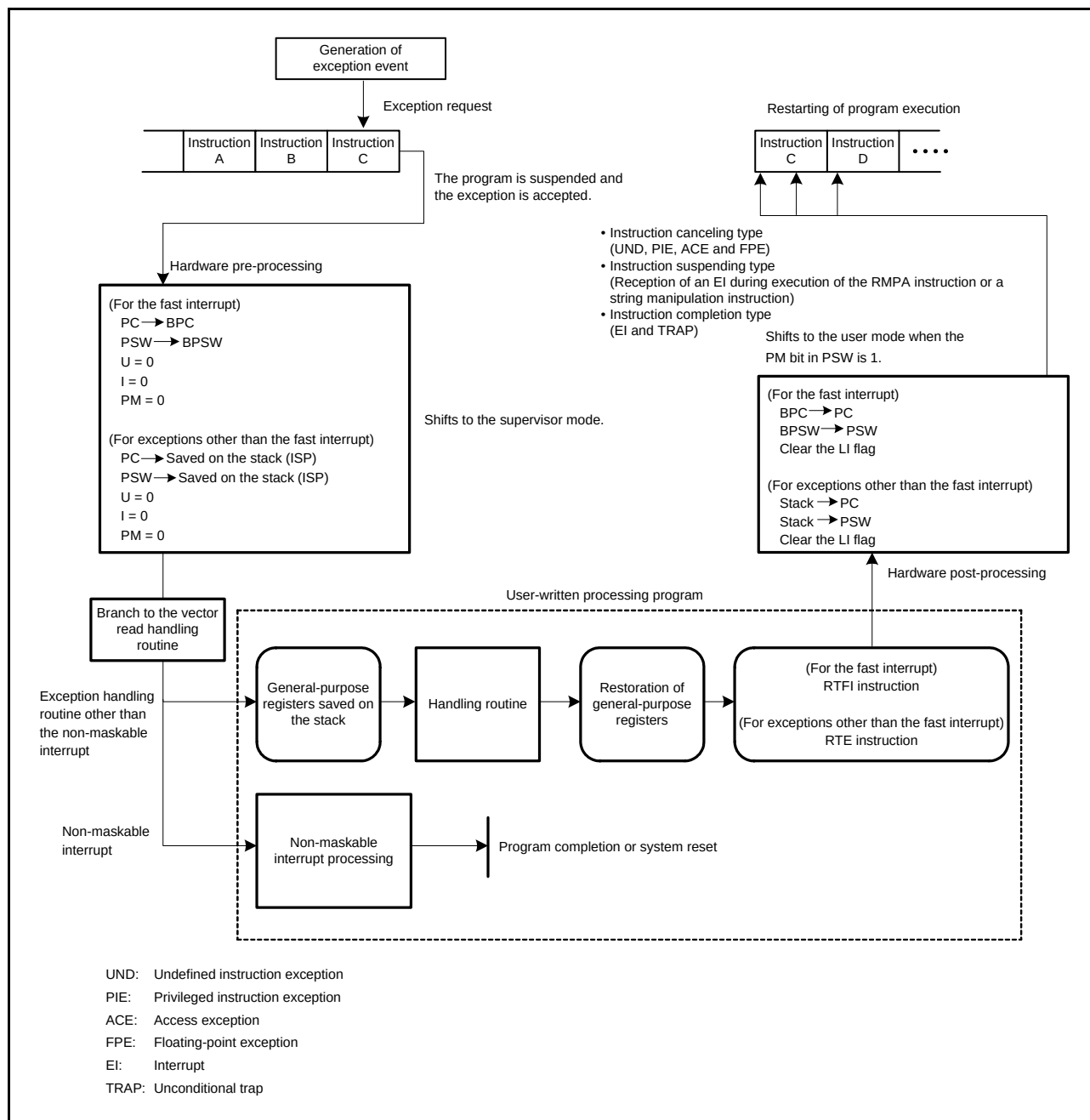


Figure 14.2 Outline of Exception Handling Procedure

When an exception is accepted, hardware processing by the RXv2 CPU is followed by access to the vector to acquire the address of the branch destination. In the vector, a vector address is allocated to each exception, and the branch destination address of the exception handling routine is written to each vector address.

Hardware pre-processing by the RXv2 CPU handles saving of the contents of the program counter (PC) and processor status word (PSW). In the case of a fast interrupt, the contents are saved in the backup PC (BPC) and the backup PSW (BPSW), respectively. In the case of exceptions other than a fast interrupt, the contents are saved in the stack area.

General purpose registers and control registers other than the PC and PSW that are to be used within the exception handling routine must be saved on the stack by a user program at the start of the exception handling routine.

On completion of processing by an exception handling routine, registers saved on the stack are restored and the RTE instruction is executed to restore execution from the exception handling routine to the original program. For return from a fast interrupt, the RTFI instruction is used instead. In the case of a non-maskable interrupt, however, finish the program or reset the system without returning to the original program.

Hardware post-processing by the RXv2 CPU handles restoration of the contents of PC and PSW. In the case of a fast interrupt, the values of BPC and BPSW are restored to PC and PSW, respectively. In the case of exceptions other than a fast interrupt, the values are restored from the stack to PC and PSW.

14.3 Acceptance of Exception Events

When an exception occurs, the CPU suspends the execution of the program and processing branches to the exception handling routine.

14.3.1 Acceptance Timing and Saved PC Value

Table 14.1 lists the timing of acceptance and the program counter (PC) value to be saved for each exception event.

Table 14.1 Acceptance Timing and Saved PC Value

Exception Event		Type of Handling	Acceptance Timing	Value Saved in BPC or on the Stack
Undefined instruction exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Privileged instruction exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Access exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Floating-point exception		Instruction canceling type	During instruction execution	PC value of the instruction that generated the exception
Reset		Instruction abandonment type	Any machine cycle	None
Non-maskable interrupt	During execution of the RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions	Instruction suspending type	During instruction execution	PC value of the instruction being executed
	Other than above	Instruction completion type	At the next break between instructions	PC value of the next instruction
Interrupt	During execution of the RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, and SWHILE instructions	Instruction suspending type	During instruction execution	PC value of the instruction being executed
	Other than above	Instruction completion type	At the next break between instructions	PC value of the next instruction
Unconditional trap		Instruction completion type	At the next break between instructions	PC value of the next instruction

14.3.2 Vector and Site for Saving the Values in the PC and PSW

The vector for each type of exception and the site for saving the values of the program counter (PC) and processor status word (PSW) are listed in Table 14.2. The addresses where the exception vector table and interrupt vector table start must be set. For details, see section 2.6, Vector Table.

Table 14.2 Vector and Site for Saving the Values in the PC and PSW

Exception		Vector	Site for Saving the Values in the PC and PSW
Undefined instruction exception		Exception vector table (EXTB)	Stack
Privileged instruction exception		Exception vector table (EXTB)	Stack
Access exception		Exception vector table (EXTB)	Stack
Floating-point exception		Exception vector table (EXTB)	Stack
Reset		Exception vector table (EXTB)	Nowhere
Non-maskable interrupt		Exception vector table (EXTB)	Stack
Interrupt	Fast interrupt	FINTV	BPC and BPSW
	Other than above	Interrupt vector table (INTB)	Stack
Unconditional trap		Interrupt vector table (INTB)	Stack

14.4 Hardware Processing for Accepting and Returning from Exceptions

This section describes the hardware processing for accepting and returning from exceptions other than a reset.

(1) Hardware Pre-Processing for Accepting an Exception

(a) Saving PSW

- For a fast interrupt
PSW → BPSW
- For exceptions other than a fast interrupt
PSW → Stack

Note: The values in FPSW are not saved by hardware pre-processing. Therefore, if floating-point instructions are to be used within an exception handling routine, the user must save these values on the stack within the exception handling routine.

(b) Updating PM, U, and I Bits in PSW

I: Set to 0

U: Set to 0

PM: Set to 0

(c) Saving PC

- For a fast interrupt
PC → BPC
- For exceptions other than a fast interrupt
PC → Stack

(d) Setting Branch Destination Address of Exception Handling Routine in PC

Processing is shifted to the exception handling routine by acquiring the vector corresponding to the exception and then branching accordingly.

(2) Hardware Post-Processing for Execution of RTE and RTFI Instructions

(a) Restoring PSW

- For a fast interrupt
BPSW → PSW
- For exceptions other than a fast interrupt
Stack → PSW

(b) Restoring PC

- For a fast interrupt
BPC → PC
- For exceptions other than a fast interrupt
Stack → PC

(c) Clearing the LI flag

14.5 Hardware Pre-Processing

The hardware pre-processing from reception of each exception request to execution of the associated exception handling routine are explained below.

14.5.1 Undefined Instruction Exception

1. The value of the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 005Ch.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.2 Privileged Instruction Exception

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 0050h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.3 Access Exceptions

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 0054h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.4 Floating-Point Exception

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) is saved on the stack (ISP).
4. The vector is fetched from the value of EXTB + address 0000 0064h.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.5 Reset

1. The control registers are initialized.
2. The vector is fetched from address FFFF FFFCh.
3. The fetched vector is set to the PC.

14.5.6 Non-Maskable Interrupt

1. The value of the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. If the interrupt was generated during the execution of an RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE instruction, the value of the program counter (PC) for that instruction is saved on the stack (ISP). For other instructions, the PC value of the next instruction is saved.
4. The processor interrupt priority level bits (IPL[3:0]) in PSW are set to Fh.
5. The vector is fetched from the value of EXTB + address 0000 0078h.
6. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.7 Interrupt

1. The value of the processor status word (PSW) is saved on the stack (ISP) or, for the fast interrupt, in the backup PSW (BPSW).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. If the interrupt was generated during the execution of an RMPA, SCMPU, SMOVB, SMOVF, SMOVU, SSTR, SUNTIL, or SWHILE instruction, the value of the program counter (PC) for that instruction is saved. For other instructions, the PC value of the next instruction is saved. Saving of the PC is in the backup PC (BPC) for fast interrupts.
4. The processor interrupt priority level bits (IPL[3:0]) in PSW indicate the interrupt priority level of the interrupt.
5. The vector for an interrupt source other than the fast interrupt is fetched from the interrupt vector table. For the fast interrupt, the address is fetched from the fast interrupt vector register (FINTV).
6. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.5.8 Unconditional Trap

1. The value in the processor status word (PSW) is saved on the stack (ISP).
2. The processor mode select bit (PM), the stack pointer select bit (U), and the interrupt enable bit (I) in PSW are cleared to 0.
3. The value of the program counter (PC) for the next instruction is saved on the stack (ISP).
4. For the INT instruction, the value at the vector corresponding to the INT instruction number is fetched from the interrupt vector table.
For the BRK instruction, the value at the vector from the start address is fetched from the interrupt vector table.
5. The fetched vector is set to the PC and processing branches to the exception handling routine.

14.6 Return from Exception Handling Routine

Executing the instruction listed in Table 14.3 at the end of the corresponding exception handling routine restores the values of the program counter (PC) and processor status word (PSW) that were saved on the stack or in the control registers (BPC and BPSW) immediately before the exception handling sequence.

Table 14.3 Return from Exception Handling Routine

Exception		Instruction for Return
Undefined instruction exception		RTE
Privileged instruction exception		RTE
Access exception		RTE
Floating-point exception		RTE
Reset		Return is impossible
Non-maskable interrupt		Prohibited
Interrupt	Fast interrupt	RTFI
	Other than above	RTE
Unconditional trap		RTE

14.7 Priority of Exception Events

The priority of exception events is listed in Table 14.4. When multiple exceptions are generated at the same time, the exception with the highest priority is accepted first.

Table 14.4 Priority of Exception Events

Priority		Exception Event
↑ High Low	1	Reset
	2	Non-maskable interrupt
	3	Interrupt
	4	Instruction access exception
	5	Undefined instruction exception Privileged instruction exception
	6	Unconditional trap
	7	Operand access exception
	8	Floating-point exception

15. Interrupt Controller (ICUb)

15.1 Overview

The interrupt controller receives interrupt requests from peripheral modules and external pins, and generates an interrupt request to the CPU and a transfer request to the DTC and DMAC.

Table 15.1 lists the specifications of the interrupt controller, and Figure 15.1 shows a block diagram of the interrupt controller.

Table 15.1 Specifications of Interrupt Controller

Item	Description
Interrupts	Peripheral function interrupts - Interrupts from peripheral modules - Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules.
	External pin interrupts - Interrupts from pins IRQ0, IRQ1, and IRQ4 to IRQ7 - Number of sources: 6 - Interrupt detection: Low level/falling edge/rising edge/rising and falling edges One of these detection methods can be set for each source. - Digital filter function: Supported
	Software interrupt - Interrupt generated by writing to a register - One interrupt source
	Event link interrupt The ELSR8I, ELSR18I or ELSR19I interrupt is generated by an ELC event
	Interrupt priority Specified by registers.
	Fast interrupt function Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC/DMAC control Interrupt sources can be used to start the DTC and DMAC.*1
Non-maskable interrupts	NMI pin interrupt - Interrupt from the NMI pin - Interrupt detection: Falling edge/rising edge - Digital filter function: Supported
	Oscillation stop detection interrupt Interrupt on detection of oscillation having stopped
	WDT underflow/refresh error Interrupt on an underflow of the down counter or occurrence of a refresh error
	IWDT underflow/refresh error Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	VBATT voltage monitoring interrupt Voltage monitoring interrupt of the VBATT
Return from power-down modes	- Sleep mode, deep sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. - Software standby mode: Return is initiated by non-maskable interrupts, IRQ0, IRQ1, and IRQ4 to IRQ7 interrupts, or RTC alarm/periodic interrupts.

Note 1. For the DTC and DMAC triggers, refer to Table 15.3, Interrupt Vector Table.

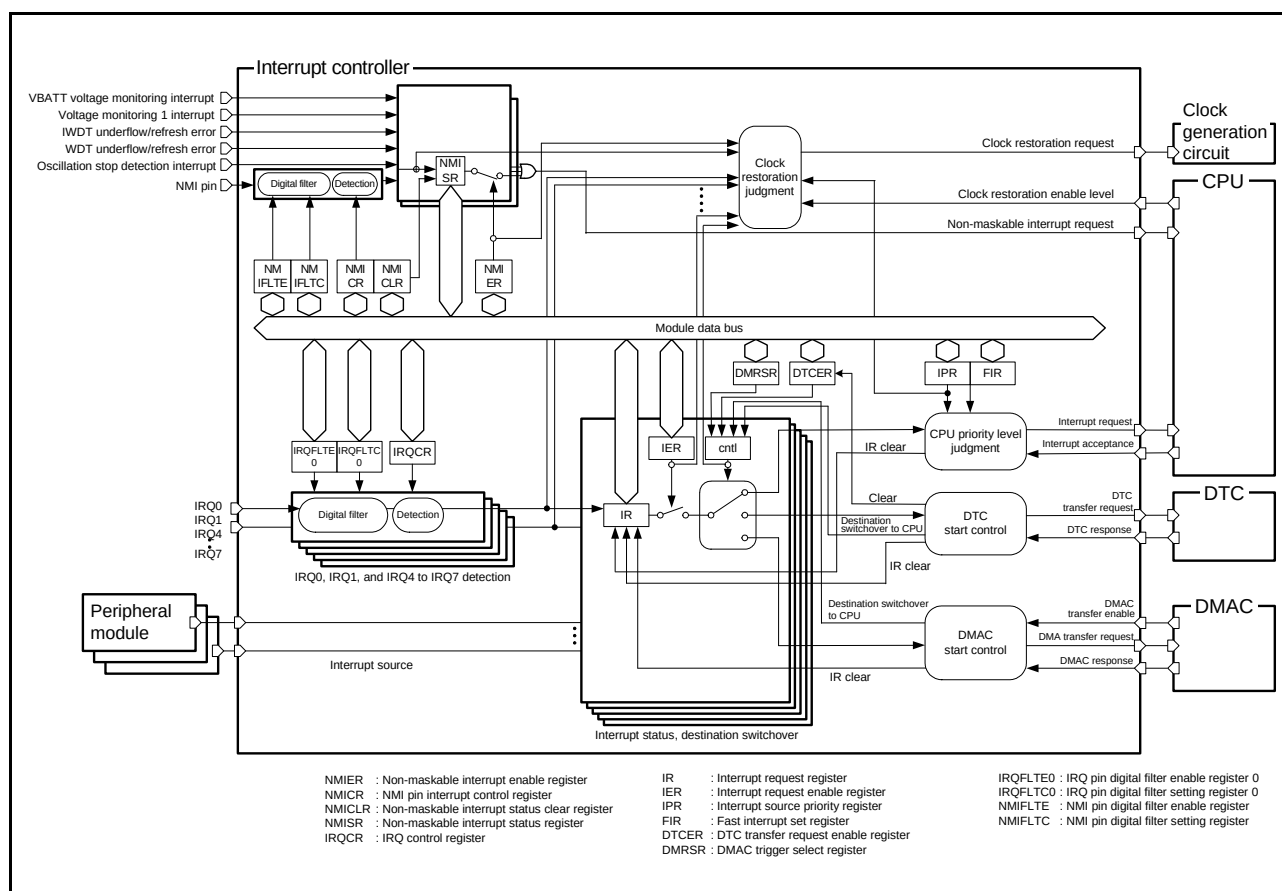


Figure 15.1 Block Diagram of Interrupt Controller

Table 15.2 lists the input/output pins of the interrupt controller.

Table 15.2 Pin Configuration of Interrupt Controller

Pin Name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0, IRQ1, and IRQ4 to IRQ7	Input	External interrupt request pins

15.2 Register Descriptions

15.2.1 Interrupt Request Register n (IRn) (n = interrupt vector number)

Address(es): ICU.IR016 0008 7010h to ICU.IR255 0008 70FFh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	IR
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	IR	Interrupt Status Flag	0: No interrupt request is generated 1: An interrupt request is generated	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. For an edge detection interrupt, only 0 can be written to this bit; do not write 1.
For a level detection interrupt, neither 0 nor 1 can be written.

IRn is provided for each interrupt source, where “n” indicates the interrupt vector number.

For the correspondence between interrupt sources and interrupt vector numbers, see Table 15.3, Interrupt Vector Table.

IR Flag (Interrupt Status Flag)

This flag is the status flag of an individual interrupt request. This flag is set to 1 when the corresponding interrupt request is generated. To detect an interrupt request, the interrupt request output should be enabled by the corresponding peripheral module interrupt enable bit.

There are two interrupt request detection methods: edge detection and level detection. For interrupts from peripheral modules, either edge detection or level detection is determined per interrupt source. For interrupts from IRQi (i = 0, 1, and 4 to 7) pins, edge detection or level detection is selected by setting the corresponding IRQCRi.IRQMD[1:0] bits. For detection of the various interrupt sources, see Table 15.3, Interrupt Vector Table.

(1) Edge detection

[Setting condition]

- The flag is set to 1 in response to the generation of an interrupt request from the corresponding peripheral module or IRQi pin. For interrupt generation by the various peripheral modules, refer to the sections describing the modules.

[Clearing conditions]

- The flag is cleared to 0 when the interrupt request destination accepts the interrupt request.
- The IR flag is cleared to 0 by writing 0 to it. Note, however, that writing 0 to the IR flag is prohibited if the destination of the interrupt request is the DTC or DMAC.

(2) Level detection

[Setting condition]

- The flag remains set to 1 while an interrupt request is being sent from the corresponding peripheral module or IRQi pin. For interrupt generation by the various peripheral modules, refer to the sections describing the modules.

[Clearing condition]

- The flag is cleared to 0 when the source of the interrupt request is cleared (it is not cleared when the interrupt request destination accepts the interrupt request). For clearing interrupts from the various peripheral modules, refer to the sections describing the modules.

When level detection has been selected for an IRQi pin, the interrupt request is withdrawn by driving the IRQi pin high. Do not write 0 or 1 to the IR flag while level detection is selected.

15.2.2 Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh)

Address(es): ICU.IER02 0008 7202h to ICU.IER1F 0008 721Fh

b7	b6	b5	b4	b3	b2	b1	b0
IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	IEN0	Interrupt Request Enable 0	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b1	IEN1	Interrupt Request Enable 1		R/W
b2	IEN2	Interrupt Request Enable 2		R/W
b3	IEN3	Interrupt Request Enable 3		R/W
b4	IEN4	Interrupt Request Enable 4		R/W
b5	IEN5	Interrupt Request Enable 5		R/W
b6	IEN6	Interrupt Request Enable 6		R/W
b7	IEN7	Interrupt Request Enable 7		R/W

Note: Write 0 to the bit that corresponds to the vector number for reservation. These bits are read as 0.

IENj Bit (Interrupt Request Enable j) (j = 0 to 7)

When an IENj bit is 1, the corresponding interrupt request will be output to the destination selected for the request.

When an IENj bit is 0, the corresponding interrupt request will not be output to the destination selected for the request.

The setting of an IENj bit does not affect the IRn.IR flag (n = interrupt vector number). Even if the corresponding IENj bit is 0, the IR flag value changes according to the descriptions in section 15.2.1, Interrupt Request Register n (IRn) (n = interrupt vector number).

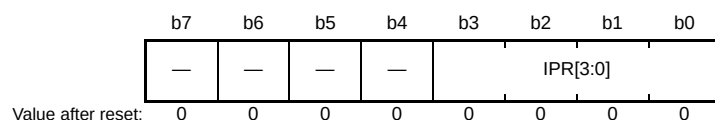
The IERm.IENj bit is set for each request source (vector number).

For the correspondence between interrupt sources and IERm.IENj bits, see Table 15.3, Interrupt Vector Table.

For the procedure for setting IERm.IENj bits during the selection of destinations for interrupt requests, refer to section 15.4.3, Selecting Interrupt Request Destinations.

15.2.3 Interrupt Source Priority Register n (IPRn) (n = interrupt vector number)

Address(es): ICU.IPR000 0008 7300h to ICU.IPR255 0008 73FFh



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IPR[3:0]	Interrupt Priority Level Select	b3 b0 0 0 0 0: Level 0 (interrupt disabled)*1 0 0 0 1: Level 1 0 0 1 0: Level 2 0 0 1 1: Level 3 0 1 0 0: Level 4 0 1 0 1: Level 5 0 1 1 0: Level 6 0 1 1 1: Level 7 1 0 0 0: Level 8 1 0 0 1: Level 9 1 0 1 0: Level 10 1 0 1 1: Level 11 1 1 0 0: Level 12 1 1 0 1: Level 13 1 1 1 0: Level 14 1 1 1 1: Level 15 (highest)	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the interrupt is specified as a fast interrupt, it can be issued even if the priority level is level 0.

For the correspondence between interrupt sources and IPRn registers, see Table 15.3, Interrupt Vector Table.

IPR[3:0] Bits (Interrupt Priority Level Select)

These bits specify the priority level of the corresponding interrupt source.

Priority levels specified by the IPR[3:0] bits are used only to determine the priority of interrupt requests to be transferred to the CPU, and do not affect transfer requests to the DTC or DMAC.

The CPU accepts only interrupt requests higher than the priority level specified by the IPL[3:0] bits in PSW, and handles accepted interrupts.

If two or more interrupt requests are generated at the same time, their priority levels are compared with the value of the IPR[3:0] bits. If interrupt requests of the same priority level are generated at the same time, an interrupt source with a smaller vector number takes precedence.

These bits should be written to while an interrupt request is disabled (IERm.IENj bit = 0 (m = 02h to 1Fh, j = 0 to 7)).

15.2.4 Fast Interrupt Set Register (FIR)

Address(es): ICU.FIR 0008 72F0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIEN	—	—	—	—	—	—	—	FVCT[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	FVCT[7:0]	Fast Interrupt Vector Number	Specify the vector number of an interrupt source to be a fast interrupt.	R/W
b14 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	FIEN	Fast Interrupt Enable	0: Fast interrupt is disabled 1: Fast interrupt is enabled	R/W

The fast interrupt function based on the FIR register setting is applicable only to interrupts to the CPU. It will not affect any transfer request to the DTC or DMAC.

Before writing to this register, be sure to disable interrupt requests (IERm.IENj bit = 0 (m = 02h to 1Fh, j = 0 to 7)).

FVCT[7:0] Bits (Fast Interrupt Vector Number)

The FVCT[7:0] bits specify the vector number of an interrupt source that uses the fast interrupt function.

FIEN Bit (Fast Interrupt Enable)

This bit enables the fast interrupt.

Setting this bit to 1 makes the interrupt request of the vector number specified by the FVCT[7:0] bits a fast interrupt.

When an interrupt request of the vector number specified by the FVCT[7:0] bits is generated and the interrupt request destination is the CPU while the FIEN bit is 1, the interrupt request is output to the CPU as a fast interrupt regardless of the setting of the IPRn register (n = interrupt vector number). When using the fast interrupt for returning from the software standby mode, see section 15.6.2, Return from Software Standby Mode.

If the setting of the IERm.IENj bit has disabled interrupt requests from the interrupt source with the vector number in this register, fast interrupt requests are not output to the CPU.

For settable vector numbers, see Table 15.3, Interrupt Vector Table.

Do not write any reserved vector numbers to the FVCT[7:0] bits.

For details on the fast interrupt, see section 14, Exception Handling, and section 15.4.6, Fast Interrupt.

15.2.5 Software Interrupt Generation Register (SWINTR)

Address(es): ICU.SWINTR 0008 72E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SWINT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWINT	Software Interrupt Generation	This bit is read as 0. Writing 1 issues a software interrupt request. Writing 0 to this bit has no effect.	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written.

SWINT Bit (Software Interrupt Generation)

When 1 is written to the SWINT bit, the interrupt request register 027 (IR027) is set to 1.

If 1 is written to the SWINT bit when the DTC transfer request enable register 027 (DTCER027) is set to 0, an interrupt to the CPU is generated.

If 1 is written to the SWINT bit when the DTC transfer request enable register 027 (DTCER027) is set to 1, a DTC transfer request is issued.

15.2.6 DTC Transfer Request Enable Register n (DTCERn) (n = interrupt vector number)

Address(es): ICU.DTCER027 0008 711Bh to ICU.DTCER255 0008 71FFh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DTCE
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTCE	DTC Transfer Request Enable	0: The corresponding interrupt source is not selected as the DTC trigger. 1: The corresponding interrupt source is selected as the DTC trigger.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

An interrupt source that has been selected as a DMAC trigger should not be specified as a DTC trigger. See Table 15.3, Interrupt Vector Table, for the interrupt sources that are selectable as the DTC trigger.

DTCE Bit (DTC Transfer Request Enable)

When the DTCE bit is set to 1, the corresponding interrupt source is selected as the DTC trigger.

[Setting condition]

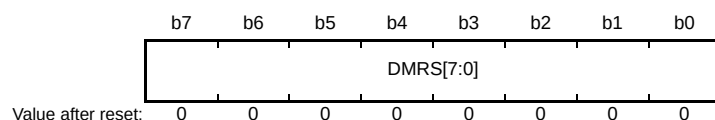
- When 1 is written to the DTCE bit

[Clearing conditions]

- When the specified number of transfers is completed (for the chain transfer, the number of transfers for the last chain transfer is completed)
- When 0 is written to the DTCE bit

15.2.7 DMAC Trigger Select Register m (DMRSRm) (m = DMAC channel number)

Address(es): ICU.DMRSR0 0008 7400h, ICU.DMRSR1 0008 7404h, ICU.DMRSR2 0008 7408h, ICU.DMRSR3 0008 740Ch



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	DMRS[7:0]	DMAC Trigger Select	These bits specify the vector number for the DMA transfer request.	R/W

To specify the same interrupt source for multiple DMRSRm registers is disabled. The interrupt source that has been selected for the DMRSRm trigger should not be specified as the DTC trigger. Otherwise, the correct operation is not guaranteed.

DMRS[7:0] Bits (DMAC Trigger Select)

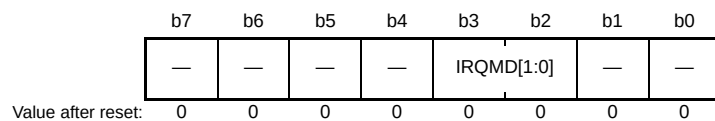
The vector number of the interrupt source used as the DMAC trigger is specified in 8 bits. Do not set the vector numbers that are not assigned for the DMAC trigger.

For the correspondence between interrupt sources and interrupt vector numbers, see Table 15.3, Interrupt Vector Table.

Write to the DMRSRm register while the DMA transfer enable bit of the DMA transfer enable register (DMACm.DMCNT.DTE) is cleared to 0.

15.2.8 IRQ Control Register i (IRQCRi) (i = 0, 1, and 4 to 7)

Address(es): ICU.IRQCR0 0008 7500h, ICU.IRQCR1 0008 7501h, ICU.IRQCR4 0008 7504h to ICU.IRQCR7 0008 7507h



Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3, b2	IRQMD[1:0]	IRQ Detection Sense Select	b3 b2 0 0: Low level 0 1: Falling edge 1 0: Rising edge 1 1: Rising and falling edges	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only change the settings of this register while the corresponding interrupt request enable bit is prohibiting the interrupt request (IENj bit in IERm (m = 02h to 1Fh, j = 0 to 7) is 0). After changing the setting, clear the IR flag in IRn before setting the interrupt enable bit. However, when the change is to the low level, the IR flag does not require clearing.

IRQMD[1:0] Bits (IRQ Detection Sense Select)

These bits select the interrupt detection sensing method of IRQi pin.

For the external pin interrupt detection setting, see section 15.4.8, External Pin Interrupts.

15.2.9 IRQ Pin Digital Filter Enable Register 0 (IRQFLTE0)

Address(es): ICU.IRQFLTE0 0008 7510h

b7	b6	b5	b4	b3	b2	b1	b0
FLTEN 7	FLTEN 6	FLTEN 5	FLTEN 4	—	—	FLTEN 1	FLTEN 0
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FLTEN0	IRQ0 Digital Filter Enable	0: Digital filter is disabled 1: Digital filter is enabled	R/W
b1	FLTEN1	IRQ1 Digital Filter Enable		R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	FLTEN4	IRQ4 Digital Filter Enable	0: Digital filter is disabled 1: Digital filter is enabled	R/W
b5	FLTEN5	IRQ5 Digital Filter Enable		R/W
b6	FLTEN6	IRQ6 Digital Filter Enable		R/W
b7	FLTEN7	IRQ7 Digital Filter Enable		R/W

FLTENi Bit (IRQi Digital Filter Enable) (i = 0, 1, and 4 to 7)

This bit enables the digital filter used for the IRQi pin.

The digital filter is enabled when the FLTENi bit is 1, and disabled when the FLTENi bit is 0.

The IRQi pin level is sampled at the sampling clock cycle specified with the IRQFLTC0.FCLKSELi[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.

For details of the digital filter, see section 15.4.7, Digital Filter.

15.2.10 IRQ Pin Digital Filter Setting Register 0 (IRQFLTC0)

Address(es): ICU.IRQFLTC0 0008 7514h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FCLKSEL7[1:0]		FCLKSEL6[1:0]		FCLKSEL5[1:0]		FCLKSEL4[1:0]		—		—		FCLKSEL1[1:0]		FCLKSEL0[1:0]	
0		0		0		0		0		0		0		0	

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b1, b0	FCLKSEL0[1:0]	IRQ0 Digital Filter Sampling Clock	0 0: PCLK 0 1: PCLK/8	R/W
b3, b2	FCLKSEL1[1:0]	IRQ1 Digital Filter Sampling Clock	1 0: PCLK/32 1 1: PCLK/64	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	FCLKSEL4[1:0]	IRQ4 Digital Filter Sampling Clock	0 0: PCLK 0 1: PCLK/8	R/W
b11, b10	FCLKSEL5[1:0]	IRQ5 Digital Filter Sampling Clock	1 0: PCLK/32 1 1: PCLK/64	R/W
b13, b12	FCLKSEL6[1:0]	IRQ6 Digital Filter Sampling Clock		R/W
b15, b14	FCLKSEL7[1:0]	IRQ7 Digital Filter Sampling Clock		R/W

FCLKSELi[1:0] Bits (IRQi Digital Filter Sampling Clock) (i = 0, 1, and 4 to 7)

These bits select the cycle of the digital filter sampling clock for the IRQi pin.

The sampling clock cycle can be selected from among the PCLK (every cycle), PCLK/8 (once every eight cycles), PCLK/32 (once every 32 cycles), and PCLK/64 (once every 64 cycles).

For details of the digital filter, see section 15.4.7, Digital Filter.

15.2.11 Non-Maskable Interrupt Status Register (NMISR)

Address(es): ICU.NMISR 0008 7580h

b7	b6	b5	b4	b3	b2	b1	b0
—	VBATS T	—	LVD1S T	IWDTST T	WDTST	OSTST	NMIST
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIST	NMI Status Flag	0: NMI pin interrupt is not requested 1: NMI pin interrupt is requested	R
b1	OSTST	Oscillation Stop Detection Interrupt Status Flag	0: Oscillation stop detection interrupt is not requested 1: Oscillation stop detection interrupt is requested	R
b2	WDTST	WDT Underflow/Refresh Error Status Flag	0: WDT underflow/refresh error interrupt is not requested 1: WDT underflow/refresh error interrupt is requested	R
b3	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: IWDT underflow/refresh error interrupt is not requested 1: IWDT underflow/refresh error interrupt is requested	R
b4	LVD1ST	Voltage Monitoring 1 Interrupt Status Flag	0: Voltage monitoring 1 interrupt is not requested 1: Voltage monitoring 1 interrupt is requested	R
b5	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b6	VBATST	VBATT Voltage Monitoring Interrupt Status Flag	0: VBATT voltage monitoring interrupt request is not requested 1: VBATT voltage monitoring interrupt request is requested	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

The NMISR register monitors the status of a non-maskable interrupt source. Writing to the NMISR register is ignored. The setting in the non-maskable interrupt enable register (NMIER) does not affect the status flags in NMISR. Before the end of the non-maskable interrupt handler, read the NMISR register and confirm the generation status of other non-maskable interrupts. Be sure to confirm that all of the bits in the NMISR register are set to 0 before the end of the handler.

NMIST Flag (NMI Status Flag)

This flag indicates the NMI pin interrupt request.

The NMIST flag is read-only, and cleared by the NMICLR.NMICLR bit.

[Setting condition]

- When an edge specified by the NMICR.NMIMD bit is input to the NMI pin

[Clearing condition]

- When 1 is written to the NMICLR.NMICLR bit

OSTST Flag (Oscillation Stop Detection Interrupt Status Flag)

This flag indicates the oscillation stop detection interrupt request.

The OSTST flag is read-only, and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

- When the oscillation stop detection interrupt is generated

[Clearing condition]

- When 1 is written to the NMICLR.OSTCLR bit

WDTST Flag (WDT Underflow/Refresh Error Status Flag)

This flag indicates the WDT underflow/refresh error interrupt request.

The WDTST flag is read-only, and cleared by the NMICLR.WDTCLR bit.

[Setting condition]

- When the WDT underflow/refresh error interrupt is generated

[Clearing condition]

- When 1 is written to the NMICLR.WDTCLR bit

IWDTST Flag (IWDT Underflow/Refresh Error Status Flag)

This flag indicates the IWDT underflow/refresh error interrupt request.

The IWDTST flag is read-only, and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

- When the IWDT underflow/refresh error interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.IWDTCLR bit

LVD1ST Flag (Voltage Monitoring 1 Interrupt Status Flag)

This flag indicates the request for voltage monitoring 1 interrupt.

The LVD1ST flag is read-only, and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

- When the voltage monitoring 1 interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.LVD1CLR bit

VBATST Flag (VBATT Voltage Monitoring Interrupt Status Flag)

This flag indicates the request for the VBATT voltage monitoring interrupt.

[Setting condition]

- When the VBATT voltage monitoring interrupt is generated while this interrupt is enabled at its source.

[Clearing condition]

- When 1 is written to the NMICLR.VBATCLR bit.

15.2.12 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): ICU.NMIER 0008 7581h

b7	b6	b5	b4	b3	b2	b1	b0
—	VBATE N	—	LVD1E N	IWDTE N	WDTE N	OSTEN	NMIEN
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIEN	NMI Pin Interrupt Enable	0: NMI pin interrupt is disabled 1: NMI pin interrupt is enabled	R/(W) *1
b1	OSTEN	Oscillation Stop Detection Interrupt Enable	0: Oscillation stop detection interrupt is disabled 1: Oscillation stop detection interrupt is enabled	R/(W) *1
b2	WDTEN	WDT Underflow/Refresh Error Enable	0: WDT underflow/refresh error interrupt is disabled 1: WDT underflow/refresh error interrupt is enabled	R/(W) *1
b3	IWDTEN	IWDT Underflow/Refresh Error Enable	0: IWDT underflow/refresh error interrupt is disabled 1: IWDT underflow/refresh error interrupt is enabled	R/(W) *1
b4	LVD1EN	Voltage Monitoring 1 Interrupt Enable	0: Voltage monitoring 1 interrupt is disabled 1: Voltage monitoring 1 interrupt is enabled	R/(W) *1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	VBATEN	VBATT Voltage Monitoring Interrupt Enable	0: VBATT voltage monitoring interrupt is disabled 1: VBATT voltage monitoring interrupt is enabled	R/W *1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

NMIEN Bit (NMI Pin Interrupt Enable)

This bit enables the NMI pin interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

OSTEN Bit (Oscillation Stop Detection Interrupt Enable)

This bit enables the oscillation stop detection interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

WDTEN Bit (WDT Underflow/Refresh Error Enable)

This bit enables the WDT underflow/refresh error interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

IWDTEN Bit (IWDT Underflow/Refresh Error Enable)

This bit enables the IWDT underflow/refresh error interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

LVD1EN Bit (Voltage Monitoring 1 Interrupt Enable)

This bit enables the voltage monitoring 1 interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

VBATEN Bit (VBATT Voltage Monitoring Interrupt Enable)

This bit enables the VBATT voltage monitoring interrupt.

A 1 can be written to this bit only once, and subsequent write accesses are no longer enabled.

Writing 0 to this bit is disabled.

15.2.13 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): ICU.NMICLR 0008 7582h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	VBATCLR	—	LVD1CLR	IWDTCCLR	WDTCLR	OSTCLR	NMICLR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMICLR	NMI Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.NMIST flag. Writing 0 to this bit has no effect.	R/(W) *1
b1	OSTCLR	OST Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.OSTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b2	WDTCLR	WDT Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.WDTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b3	IWDTCCLR	IWDT Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.IWDTST flag. Writing 0 to this bit has no effect.	R/(W) *1
b4	LVD1CLR	LVD1 Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.LVD1ST flag. Writing 0 to this bit has no effect.	R/(W) *1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	VBATCLR	VBAT Clear	This bit is read as 0. Writing 1 to this bit clears the NMISR.VBATST flag. Writing 0 has no effect.	R/(W) *1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written to this bit.

NMICLR Bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

OSTCLR Bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

WDTCLR Bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

IWDTCCLR Bit (IWDT Clear)

Writing 1 to the IWDTCCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

LVD1CLR Bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

VBATCLR Bit (VBAT Clear)

Writing 1 to the VBATCLR bit clears the NMISR.VBATST flag. This bit is read as 0.

15.2.14 NMI Pin Interrupt Control Register (NMICR)

Address(es): ICU.NMICR 0008 7583h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	NMIMD	—	—	—
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Change the setting of the NMICR register before the NMI pin interrupt is enabled (before setting the NMIER.NMIEN bit to 1).

NMIMD Bit (NMI Detection Set)

This bit specifies the detection edge of the NMI pin interrupt.

15.2.15 NMI Pin Digital Filter Enable Register (NMIFLTE)

Address(es): ICU.NMIFLTE 0008 7590h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	NFLTE N
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	NFLTEN	NMI Digital Filter Enable	0: Digital filter is disabled 1: Digital filter is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFLTEN Bit (NMI Digital Filter Enable)

This bit enables the digital filter used for the NMI pin interrupt.

The digital filter is enabled when the NFLTEN bit is 1, and disabled when the NFLTEN bit is 0.

The NMI pin level is sampled at the sampling clock cycle specified with the NMIFLTC.NFCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.

For details of the digital filter, see section 15.4.7, Digital Filter.

15.2.16 NMI Pin Digital Filter Setting Register (NMIFLTC)

Address(es): ICU.NMIFLTC 0008 7594h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	NFCLKSEL[1:0]	
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock	b1 b0 0 0: PCLK 0 1: PCLK/8 1 0: PCLK/32 1 1: PCLK/64	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFCLKSEL[1:0] Bits (NMI Digital Filter Sampling Clock)

These bits select the cycle of the digital filter sampling clock for the NMI pin interrupt.

The sampling clock cycle can be selected from among the PCLK (every cycle), PCLK/8 (once every eight cycles), PCLK/32 (once every 32 cycles), and PCLK/64 (once every 64 cycles).

For details of the digital filter, see section 15.4.7, Digital Filter.

15.3 Vector Table

There are two types of interrupts detected by the interrupt controller: maskable interrupts and non-maskable interrupts. When the CPU accepts an interrupt or non-maskable interrupt, it acquires a 4-byte vector address from the vector table.

15.3.1 Interrupt Vector Table

The interrupt vector table is placed in the 1024-byte range (4 bytes × 256 sources) beginning at the address specified in the interrupt table register (INTB) of the CPU. Write a value to the INTB register before enabling interrupts. The value written to the INTB register should be a multiple of 4.

Executing an INT instruction or BRK instruction leads to the generation of an unconditional trap. The same range of memory as shown in Table 15.3, Interrupt Vector Table, is used for the vectors for unconditional traps. The vector for BRK instructions is vector 0 while the vector numbers for INT instructions are specifiable as numbers in the range from 0 to 255.

Table 15.3 lists details of the interrupt vectors. Details of the headings in Table 15.3 are listed below.

Item	Description
Source of interrupt request generation	Name of the source for generation of the interrupt request
Name	Name of the interrupt
Vector no.	Vector number for the interrupt
Vector address offset	Value of the offset from the base address for the vector table
Form of interrupt detection	"Edge" or "level" as the method for detection of the interrupt
CPU interrupt	"✓" in this column indicates usability as a CPU interrupt.
Start the DTC	"✓" in this column indicates usability as a request for DTC transfer.
Start the DMAC	"✓" in this column indicates usability as a request for DMA transfer.
sstb return	"✓" in this column indicates usability as a request for return from software-standby mode.
IER	Name of the IER register and bit corresponding to the vector number
IPR	Name of the IPR register corresponding to the interrupt source
DTCER	Name of the DTCER register corresponding to the DTC trigger

Table 15.3 Interrupt Vector Table (1/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	DMAC	sstb Return	IER	IPR	DTCER
—	For an unconditional trap	0	0000h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	1	0004h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	2	0008h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	3	000Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	4	0010h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	5	0014h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	6	0018h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	7	001Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	8	0020h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	9	0024h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	10	0028h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	11	002Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	12	0030h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	13	0034h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	14	0038h	—	N/A	N/A	N/A	N/A	—	—	—
—	For an unconditional trap	15	003Ch	—	N/A	N/A	N/A	N/A	—	—	—
BSC	BUSERR	16	0040h	Level	✓	N/A	N/A	N/A	IER02.IEN0	IPR000	—
—	Reserved	17	0044h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	18	0048h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	19	004Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	20	0050h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	21	0054h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	22	0058h	—	N/A	N/A	N/A	N/A	—	—	—
FCU	FRDYI	23	005Ch	Edge	✓	N/A	N/A	N/A	IER02.IEN7	IPR002	—
—	Reserved	24	0060h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	25	0064h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	26	0068h	—	N/A	N/A	N/A	N/A	—	—	—
ICU	SWINT	27	006Ch	Edge	✓	✓	N/A	N/A	IER03.IEN3	IPR003	DTCER027
CMT0	CMI0	28	0070h	Edge	✓	✓	✓	N/A	IER03.IEN4	IPR004	DTCER028
CMT1	CMI1	29	0074h	Edge	✓	✓	✓	N/A	IER03.IEN5	IPR005	DTCER029
CMT2	CMI2	30	0078h	Edge	✓	✓	✓	N/A	IER03.IEN6	IPR006	DTCER030
CMT3	CMI3	31	007Ch	Edge	✓	✓	✓	N/A	IER03.IEN7	IPR007	DTCER031
CAC	FERRF	32	0080h	Level	✓	N/A	N/A	N/A	IER04.IEN0	IPR032	—
	MENDF	33	0084h	Level	✓	N/A	N/A	N/A	IER04.IEN1	IPR033	—
	OVFF	34	0088h	Level	✓	N/A	N/A	N/A	IER04.IEN2	IPR034	—
—	Reserved	35	008Ch	—	N/A	N/A	N/A	N/A	—	—	—
USB0	D0FIFO0	36	0090h	Edge	✓	✓	✓	N/A	IER04.IEN4	IPR036	DTCER036
	D1FIFO0	37	0094h	Edge	✓	✓	✓	N/A	IER04.IEN5	IPR037	DTCER037
	USBIO	38	0098h	Edge	✓	N/A	N/A	N/A	IER04.IEN6	IPR038	—
—	Reserved	39	009Ch	—	N/A	N/A	N/A	N/A	—	—	—
SDHI	SBFAI	40	00A0h	Edge	✓	✓	✓	N/A	IER05.IEN0	IPR040	DTCER040
	CDETI	41	00A4h	Level	✓	N/A	N/A	N/A	IER05.IEN1	IPR041	—
	CACI	42	00A8h	Level	✓	N/A	N/A	N/A	IER05.IEN2	IPR042	—
	SDACI	43	00ACh	Level	✓	N/A	N/A	N/A	IER05.IEN3	IPR043	—

Table 15.3 Interrupt Vector Table (2/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	DMAC	sstb Return	IER	IPR	DTCER
RSPi0	SPEi0	44	00B0h	Level	✓	N/A	N/A	N/A	IER05.IEN4	IPR044	—
	SPRi0	45	00B4h	Edge	✓	✓	✓	N/A	IER05.IEN5		DTCER045
	SPTi0	46	00B8h	Edge	✓	✓	✓	N/A	IER05.IEN6		DTCER046
	SPi0	47	00BCh	Level	✓	N/A	N/A	N/A	IER05.IEN7		—
—	Reserved	48	00C0h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	49	00C4h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	50	00C8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	51	00CCh	—	N/A	N/A	N/A	N/A	—	—	—
RSCAN	COMFRXINT	52	00D0h	Edge	✓	✓	✓	N/A	IER06.IEN4	IPR052	DTCER052
	RXFINT	53	00D4h	Level	✓	N/A	N/A	N/A	IER06.IEN5	IPR053	—
	TXINT	54	00D8h	Level	✓	N/A	N/A	N/A	IER06.IEN6	IPR054	—
	CHERRINT	55	00DCh	Level	✓	N/A	N/A	N/A	IER06.IEN7	IPR055	—
	GLERRINT	56	00E0h	Level	✓	N/A	N/A	N/A	IER07.IEN0	IPR056	—
DOC	DOPCF	57	00E4h	Level	✓	N/A	N/A	N/A	IER07.IEN1	IPR057	—
—	Reserved	58	00E8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	59	00ECh	—	N/A	N/A	N/A	N/A	—	—	—
CTSU	CTSUWR	60	00F0h	Edge	✓	✓	✓	N/A	IER07.IEN4	IPR060	DTCER060
	CTSURD	61	00F4h	Edge	✓	✓	✓	N/A	IER07.IEN5		DTCER061
	CTSUFN	62	00F8h	Edge	✓	N/A	N/A	N/A	IER07.IEN6		—
RTC	CUP	63	00FCh	Edge	✓	N/A	N/A	N/A	IER07.IEN7	IPR063	—
ICU	IRQ0	64	0100h	Edge/Level	✓	✓	✓	✓	IER08.IEN0	IPR064	DTCER064
	IRQ1	65	0104h	Edge/Level	✓	✓	✓	✓	IER08.IEN1	IPR065	DTCER065
—	Reserved	66	0108h	—	N/A	N/A	N/A	N/A	—	—	—
BLE	BLEIRQ	67	010Ch	Edge	✓	N/A	✓	N/A	IER08.IEN3	IPR067	—
ICU	IRQ4	68	0110h	Edge/Level	✓	✓	N/A	✓	IER08.IEN4	IPR068	DTCER068
	IRQ5	69	0114h	Edge/Level	✓	✓	N/A	✓	IER08.IEN5	IPR069	DTCER069
	IRQ6	70	0118h	Edge/Level	✓	✓	N/A	✓	IER08.IEN6	IPR070	DTCER070
	IRQ7	71	011Ch	Edge/Level	✓	✓	N/A	✓	IER08.IEN7	IPR071	DTCER071
—	Reserved	72	0120h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	73	0124h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	74	0128h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	75	012Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	76	0130h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	77	0134h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	78	0138h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	79	013Ch	—	N/A	N/A	N/A	N/A	—	—	—
ELC	ELSR8I	80	0140h	Edge	✓	N/A	N/A	✓	IER0A.IEN0	IPR080	—
—	Reserved	81	0144h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	82	0148h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	83	014Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	84	0150h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	85	0154h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	86	0158h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	87	015Ch	—	N/A	N/A	N/A	N/A	—	—	—
LVD	LVD1	88	0160h	Edge	✓	N/A	N/A	✓	IER0B.IEN0	IPR088	—
—	Reserved	89	0164h	—	N/A	N/A	N/A	N/A	—	—	—
USB0	USB0	90	0168h	Level	✓	N/A	N/A	✓	IER0B.IEN2	IPR090	—

Table 15.3 Interrupt Vector Table (3/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	DMAC	sstb Return	IER	IPR	DTCER
VBATT	VBTLVDI	91	016Ch	Edge	✓	N/A	N/A	✓	IER0B.IEN3	IPR091	—
RTC	ALM	92	0170h	Edge	✓	N/A	N/A	✓	IER0B.IEN4	IPR092	—
	PRD	93	0174h	Edge	✓	N/A	N/A	✓	IER0B.IEN5	IPR093	—
—	Reserved	94	0178h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	95	017Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	96	0180h	—	N/A	N/A	N/A	N/A	—	—	—
	Reserved	97	0184h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	98	0188h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	99	018Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	100	0190h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	101	0194h	—	N/A	N/A	N/A	N/A	—	—	—
S12AD	S12ADI0	102	0198h	Edge	✓	✓	✓	N/A	IER0C.IEN6	IPR102	DTCER102
	GBADI	103	019Ch	Edge	✓	✓	✓	N/A	IER0C.IEN7	IPR103	DTCER103
CMPB1	CMPB2	104	01A0h	Edge	✓	✓	✓	N/A	IER0D.IEN0	IPR104	DTCER104
	CMPB3	105	01A4h	Edge	✓	✓	✓	N/A	IER0D.IEN1	IPR105	DTCER105
ELC	ELSR18I	106	01A8h	Edge	✓	✓	✓	N/A	IER0D.IEN2	IPR106	DTCER106
	ELSR19I	107	01ACh	Edge	✓	✓	✓	N/A	IER0D.IEN3	IPR107	DTCER107
SSI0	SSIF0	108	01B0h	Level	✓	N/A	N/A	N/A	IER0D.IEN4	IPR108	—
	SSIRX10	109	01B4h	Edge	✓	✓	✓	N/A	IER0D.IEN5		DTCER109
	SSITX10	110	01B8h	Edge	✓	✓	✓	N/A	IER0D.IEN6		DTCER110
TSIP	RD	111	01BCh	Edge	✓	✓	✓	N/A	IER0D.IEN7	IPR111	DTCER111
	WR	112	01C0h	Edge	✓	✓	✓	N/A	IER0E.IEN0		DTCER112
	ERR	113	01C4h	Edge	✓	N/A	N/A	N/A	IER0E.IEN1	IPR113	—
MTU0	TGIA0	114	01C8h	Edge	✓	✓	✓	N/A	IER0E.IEN2	IPR114	DTCER114
	TGIB0	115	01CCh	Edge	✓	✓	N/A	N/A	IER0E.IEN3		DTCER115
	TGIC0	116	01D0h	Edge	✓	✓	N/A	N/A	IER0E.IEN4		DTCER116
	TGID0	117	01D4h	Edge	✓	✓	N/A	N/A	IER0E.IEN5		DTCER117
	TCIV0	118	01D8h	Edge	✓	N/A	N/A	N/A	IER0E.IEN6	IPR118	—
	TGIE0	119	01DCh	Edge	✓	N/A	N/A	N/A	IER0E.IEN7		—
	TGIF0	120	01E0h	Edge	✓	N/A	N/A	N/A	IER0F.IEN0		—
MTU1	TGIA1	121	01E4h	Edge	✓	✓	✓	N/A	IER0F.IEN1	IPR121	DTCER121
	TGIB1	122	01E8h	Edge	✓	✓	N/A	N/A	IER0F.IEN2		DTCER122
	TCIV1	123	01ECh	Edge	✓	N/A	N/A	N/A	IER0F.IEN3	IPR123	—
	TCIU1	124	01F0h	Edge	✓	N/A	N/A	N/A	IER0F.IEN4		—
MTU2	TGIA2	125	01F4h	Edge	✓	✓	✓	N/A	IER0F.IEN5	IPR125	DTCER125
	TGIB2	126	01F8h	Edge	✓	✓	N/A	N/A	IER0F.IEN6		DTCER126
	TCIV2	127	01FCh	Edge	✓	N/A	N/A	N/A	IER0F.IEN7	IPR127	—
	TCIU2	128	0200h	Edge	✓	N/A	N/A	N/A	IER10.IEN0		—
MTU3	TGIA3	129	0204h	Edge	✓	✓	✓	N/A	IER10.IEN1	IPR129	DTCER129
	TGIB3	130	0208h	Edge	✓	✓	N/A	N/A	IER10.IEN2		DTCER130
	TGIC3	131	020Ch	Edge	✓	✓	N/A	N/A	IER10.IEN3		DTCER131
	TGID3	132	0210h	Edge	✓	✓	N/A	N/A	IER10.IEN4		DTCER132
	TCIV3	133	0214h	Edge	✓	N/A	N/A	N/A	IER10.IEN5	IPR133	—

Table 15.3 Interrupt Vector Table (4/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	DMAC	sstb Return	IER	IPR	DTCER
MTU4	TGIA4	134	0218h	Edge	✓	✓	✓	N/A	IER10.IEN6	IPR134	DTCER134
	TGIB4	135	021Ch	Edge	✓	✓	N/A	N/A	IER10.IEN7		DTCER135
	TGIC4	136	0220h	Edge	✓	✓	N/A	N/A	IER11.IEN0		DTCER136
	TGID4	137	0224h	Edge	✓	✓	N/A	N/A	IER11.IEN1		DTCER137
	TCIV4	138	0228h	Edge	✓	✓	N/A	N/A	IER11.IEN2	IPR138	DTCER138
—	Reserved	139	022Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	140	0230h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	141	0234h	—	N/A	N/A	N/A	N/A	—	—	—
TPU0	TGI0A	142	0238h	Edge	✓	✓	✓	N/A	IER11.IEN6	IPR142	DTCER142
	TGI0B	143	023Ch	Edge	✓	✓	N/A	N/A	IER11.IEN7		DTCER143
	TGI0C	144	0240h	Edge	✓	✓	N/A	N/A	IER12.IEN0		DTCER144
	TGI0D	145	0244h	Edge	✓	✓	N/A	N/A	IER12.IEN1		DTCER145
	TCI0V	146	0248h	Edge	✓	N/A	N/A	N/A	IER12.IEN2	IPR146	—
TPU1	TGI1A	147	024Ch	Edge	✓	✓	✓	N/A	IER12.IEN3	IPR147	DTCER147
	TGI1B	148	0250h	Edge	✓	✓	N/A	N/A	IER12.IEN4		DTCER148
	TCI1V	149	0254h	Edge	✓	N/A	N/A	N/A	IER12.IEN5	IPR149	—
	TCI1U	150	0258h	Edge	✓	N/A	N/A	N/A	IER12.IEN6		—
TPU2	TGI2A	151	025Ch	Edge	✓	✓	✓	N/A	IER12.IEN7	IPR151	DTCER151
	TGI2B	152	0260h	Edge	✓	✓	N/A	N/A	IER13.IEN0		DTCER152
	TCI2V	153	0264h	Edge	✓	N/A	N/A	N/A	IER13.IEN1	IPR153	—
	TCI2U	154	0268h	Edge	✓	N/A	N/A	N/A	IER13.IEN2		—
TPU3	TGI3A	155	026Ch	Edge	✓	✓	✓	N/A	IER13.IEN3	IPR155	DTCER155
	TGI3B	156	0270h	Edge	✓	✓	N/A	N/A	IER13.IEN4		DTCER156
	TGI3C	157	0274h	Edge	✓	✓	N/A	N/A	IER13.IEN5		DTCER157
	TGI3D	158	0278h	Edge	✓	✓	N/A	N/A	IER13.IEN6		DTCER158
	TCI3V	159	027Ch	Edge	✓	N/A	N/A	N/A	IER13.IEN7	IPR159	—
TPU4	TGI4A	160	0280h	Edge	✓	✓	✓	N/A	IER14.IEN0	IPR160	DTCER160
	TGI4B	161	0284h	Edge	✓	✓	N/A	N/A	IER14.IEN1		DTCER161
	TCI4V	162	0288h	Edge	✓	N/A	N/A	N/A	IER14.IEN2	IPR162	—
	TCI4U	163	028Ch	Edge	✓	N/A	N/A	N/A	IER14.IEN3		—
TPU5	TGI5A	164	0290h	Edge	✓	✓	✓	N/A	IER14.IEN4	IPR164	DTCER164
	TGI5B	165	0294h	Edge	✓	✓	N/A	N/A	IER14.IEN5		DTCER165
	TCI5V	166	0298h	Edge	✓	N/A	N/A	N/A	IER14.IEN6	IPR166	—
	TCI5U	167	029Ch	Edge	✓	N/A	N/A	N/A	IER14.IEN7		—
—	Reserved	168	02A0h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	169	02A4h	—	N/A	N/A	N/A	N/A	—	—	—
POE	OEI1	170	02A8h	Level	✓	N/A	N/A	N/A	IER15.IEN2	IPR170	—
	OEI2	171	02ACh	Level	✓	N/A	N/A	N/A	IER15.IEN3	IPR171	—
—	Reserved	172	02B0h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	173	02B4h	—	N/A	N/A	N/A	N/A	—	—	—
TMR0	CMIA0	174	02B8h	Edge	✓	✓	N/A	N/A	IER15.IEN6	IPR174	DTCER174
	CMIB0	175	02BCh	Edge	✓	✓	N/A	N/A	IER15.IEN7		DTCER175
	OVI0	176	02C0h	Edge	✓	N/A	N/A	N/A	IER16.IEN0		—
TMR1	CMIA1	177	02C4h	Edge	✓	✓	N/A	N/A	IER16.IEN1	IPR177	DTCER177
	CMIB1	178	02C8h	Edge	✓	✓	N/A	N/A	IER16.IEN2		DTCER178
	OVI1	179	02CCh	Edge	✓	N/A	N/A	N/A	IER16.IEN3		—

Table 15.3 Interrupt Vector Table (5/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	DMAC	sstb Return	IER	IPR	DTCER
TMR2	CMIA2	180	02D0h	Edge	✓	✓	N/A	N/A	IER16.IEN4	IPR180	DTCER180
	CMIB2	181	02D4h	Edge	✓	✓	N/A	N/A	IER16.IEN5		DTCER181
	OVI2	182	02D8h	Edge	✓	N/A	N/A	N/A	IER16.IEN6		—
TMR3	CMIA3	183	02DCh	Edge	✓	✓	N/A	N/A	IER16.IEN7	IPR183	DTCER183
	CMIB3	184	02E0h	Edge	✓	✓	N/A	N/A	IER17.IEN0		DTCER184
	OVI3	185	02E4h	Edge	✓	N/A	N/A	N/A	IER17.IEN1		—
—	Reserved	186	02E8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	187	02ECh	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	188	02F0h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	189	02F4h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	190	02F8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	191	02FCh	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	192	0300h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	193	0304h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	194	0308h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	195	030Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	196	0310h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	197	0314h	—	N/A	N/A	N/A	N/A	—	—	—
DMAC	DMAC0I	198	0318h	Edge	✓	✓	N/A	N/A	IER18.IEN6	IPR198	DTCER198
	DMAC1I	199	031Ch	Edge	✓	✓	N/A	N/A	IER18.IEN7	IPR199	DTCER199
	DMAC2I	200	0320h	Edge	✓	✓	N/A	N/A	IER19.IEN0	IPR200	DTCER200
	DMAC3I	201	0324h	Edge	✓	✓	N/A	N/A	IER19.IEN1	IPR201	DTCER201
—	Reserved	202	0328h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	203	032Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	204	0330h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	205	0334h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	206	0338h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	207	033Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	208	0340h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	209	0344h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	210	0348h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	211	034Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	212	0350h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	213	0354h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	214	0358h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	215	035Ch	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	216	0360h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	217	0364h	—	N/A	N/A	N/A	N/A	—	—	—
SCI1	ERI1	218	0368h	Level	✓	N/A	N/A	N/A	IER1B.IEN2	IPR218	—
	RX1I	219	036Ch	Edge	✓	✓	✓	N/A	IER1B.IEN3		DTCER219
	TX1I	220	0370h	Edge	✓	✓	✓	N/A	IER1B.IEN4		DTCER220
	TEI1	221	0374h	Level	✓	N/A	N/A	N/A	IER1B.IEN5		—
SCI5	ERI5	222	0378h	Level	✓	N/A	N/A	N/A	IER1B.IEN6	IPR222	—
	RX15	223	037Ch	Edge	✓	✓	✓	N/A	IER1B.IEN7		DTCER223
	TX15	224	0380h	Edge	✓	✓	✓	N/A	IER1C.IEN0		DTCER224
	TEI5	225	0384h	Level	✓	N/A	N/A	N/A	IER1C.IEN1		—

Table 15.3 Interrupt Vector Table (6/6)

Source of Interrupt Request Generation	Name	Vector No.*1	Vector Address Offset	Form of Interrupt Detection	CPU	DTC	DMAC	sstb Return	IER	IPR	DTCER
BLE	ERI	226	0388h	Level	✓	N/A	N/A	N/A	IER1C.IEN2	IPR226	—
	RXI	227	038Ch	Edge	✓	✓	✓	N/A	IER1C.IEN3		DTCER227
	TXI	228	0390h	Edge	✓	✓	✓	N/A	IER1C.IEN4		DTCER228
	TEI	229	0394h	Level	✓	N/A	N/A	N/A	IER1C.IEN5		—
SCI8	ERI8	230	0398h	Level	✓	N/A	N/A	N/A	IER1C.IEN6	IPR230	—
	RXI8	231	039Ch	Edge	✓	✓	✓	N/A	IER1C.IEN7		DTCER231
	TXI8	232	03A0h	Edge	✓	✓	✓	N/A	IER1D.IEN0		DTCER232
	TEI8	233	03A4h	Level	✓	N/A	N/A	N/A	IER1D.IEN1		—
—	Reserved	234	03A8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	235	03ACh	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	236	03B0h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	237	03B4h	—	N/A	N/A	N/A	N/A	—	—	—
SCI12	ERI12	238	03B8h	Level	✓	N/A	N/A	N/A	IER1D.IEN6	IPR238	—
	RXI12	239	03BCh	Edge	✓	✓	✓	N/A	IER1D.IEN7		DTCER239
	TXI12	240	03C0h	Edge	✓	✓	✓	N/A	IER1E.IEN0		DTCER240
	TEI12	241	03C4h	Level	✓	N/A	N/A	N/A	IER1E.IEN1		—
	SCIX0	242	03C8h	Level	✓	N/A	N/A	N/A	IER1E.IEN2	IPR242	—
	SCIX1	243	03CCh	Level	✓	N/A	N/A	N/A	IER1E.IEN3	IPR243	—
	SCIX2	244	03D0h	Level	✓	N/A	N/A	N/A	IER1E.IEN4	IPR244	—
	SCIX3	245	03D4h	Level	✓	N/A	N/A	N/A	IER1E.IEN5	IPR245	—
RIIC0	EEI0	246	03D8h	Level	✓	N/A	N/A	N/A	IER1E.IEN6	IPR246	—
	RXI0	247	03DCh	Edge	✓	✓	✓	N/A	IER1E.IEN7	IPR247	DTCER247
	TXI0	248	03E0h	Edge	✓	✓	✓	N/A	IER1F.IEN0	IPR248	DTCER248
	TEI0	249	03E4h	Level	✓	N/A	N/A	N/A	IER1F.IEN1	IPR249	—
—	Reserved	250	03E8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	251	03ECh	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	252	03F0h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	253	03F4h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	254	03F8h	—	N/A	N/A	N/A	N/A	—	—	—
—	Reserved	255	03FCh	—	N/A	N/A	N/A	N/A	—	—	—

Note 1. An interrupt source with a smaller vector number takes precedence.

15.3.2 Fast Interrupt Vector Table

The address of the entry in the interrupt vector table that corresponds to the vector number of the fast interrupt is placed in the fast interrupt vector register (FINTV) of the CPU.

15.3.3 Non-maskable Interrupt Vector Area

Non-maskable interrupts use the vector area in the exception vector table.

The exception vector table is allocated to the 128-byte area (4 bytes × 32 sources) beginning with the address set in the EXTB register in the CPU. Set a multiple of 4 in the EXTB register.

15.4 Interrupt Operation

The interrupt controller performs the following processing.

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations (CPU interrupt, DTC trigger, or DMAC trigger)
- Determining priority

15.4.1 Detecting Interrupts

Interrupt requests are detected in either of two ways: the detection of edges of the interrupt signal or the detection of a level of the interrupt signal.

Edge detection or level detection is selected for the IRQ_i pins (i = 0, 1, and 4 to 7) as external interrupt requests by the setting of the IRQMD[1:0] bits in IRQCR_i.

For interrupts from peripheral modules, either edge detection or level detection is determined per interrupt source.

For the correspondence between interrupt sources and methods of detection, see Table 15.3, Interrupt Vector Table.

15.4.1.1 Operation of Status Flags for Edge-Detected Interrupts

Figure 15.2 shows the operation of the IR flag in IR_n (n = interrupt vector number) in the case of edge detection of an interrupt from a peripheral module or on an external pin.

The IR flag in IR_n is set to 1 immediately after the transition of the interrupt signal due to generation of the interrupt. If the CPU is the request destination for the interrupt, the IR flag is automatically cleared to 0 on acceptance of the interrupt. If the DMAC or DTC is the request destination for the interrupt, the IR_n.IR flag operation differs according to the DMAC/DTC transfer settings and transfer count. For details, see Table 15.4, Operation When Starting the DMAC/DTC.

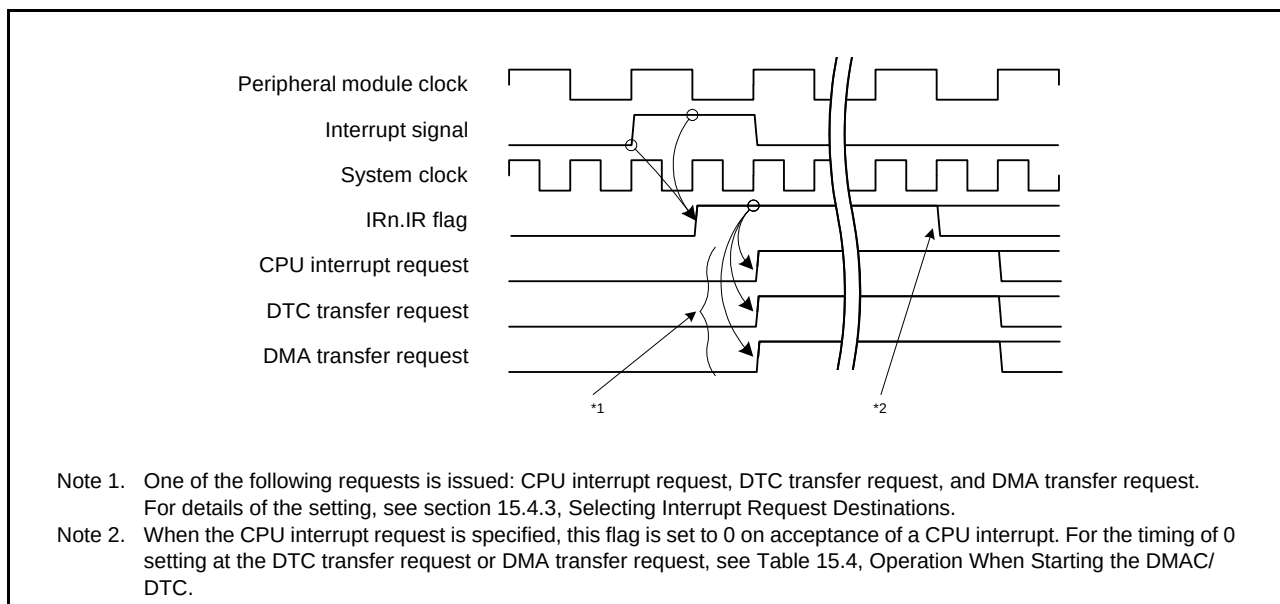


Figure 15.2 IR_n.IR Flag Operation for Edge Detection Interrupts

Figure 15.3 to Figure 15.6 show the interrupt signals of the interrupt controller. Note that the timings of the interrupts with interrupt vector numbers 64 to 95 are different from those of other interrupts. For the IRQ pin interrupts with interrupt vector numbers 64 to 79, “internal delay + 2 PCLK cycles” of delay is added after the IRQ pin input. For the interrupts with interrupt vector numbers 80 to 95, “2 PCLK cycles” of delay is added.

If an interrupt signal is generated every clock cycle, the subsequent interrupts cannot be detected; secure two or more clock cycles of the system clock or peripheral module clock, whichever is slower, between issuance of continuous interrupt requests.

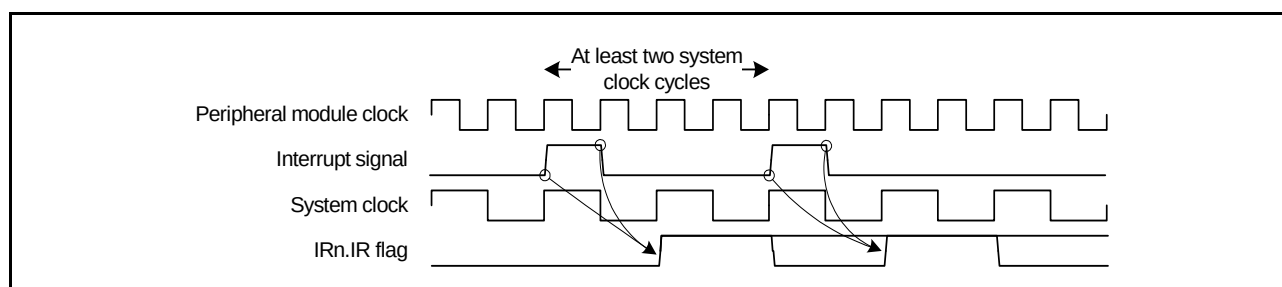


Figure 15.3 Interval Required between Issuance of Continuous Interrupt Requests (when the Frequency of System Clock is Slower than that of the Peripheral Module Clock)

While the IRn.IR flag is 1 after an interrupt request is generated, the interrupt request that is generated again will be ignored.*1

Figure 15.4 shows the timing for IRn.IR flag re-setting.

Note 1. When the transmission or reception interrupt of the SCI, RSPI, RIIC, USB, SSI, SDHI, or RSCAN is generated with the IRn.IR flag being 1, the interrupt request is retained. After the IRn.IR flag is cleared to 0, the IRn.IR flag is set to 1 again by the retained request. For details, see descriptions of the interrupts in section 33, Serial Communications Interface (SCIg, SCIH), section 35, I²C-bus Interface (RIICa), and section 38, Serial Peripheral Interface (RSPIa).

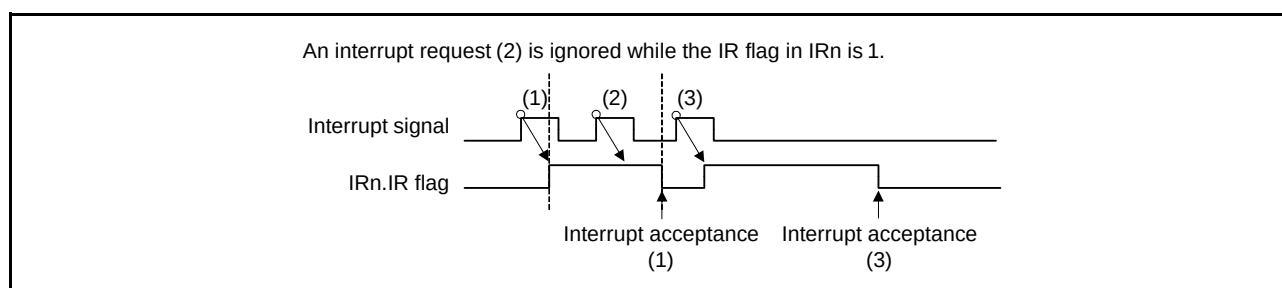


Figure 15.4 Timing for IRn.IR Flag Re-Setting

If an interrupt is disabled after the IRn.IR flag is set to 1 (output of the interrupt request is disabled by the interrupt enable bit of the relevant peripheral module), the IRn.IR flag is not affected but retains its state. Figure 15.5 shows operation when the interrupt is disabled.

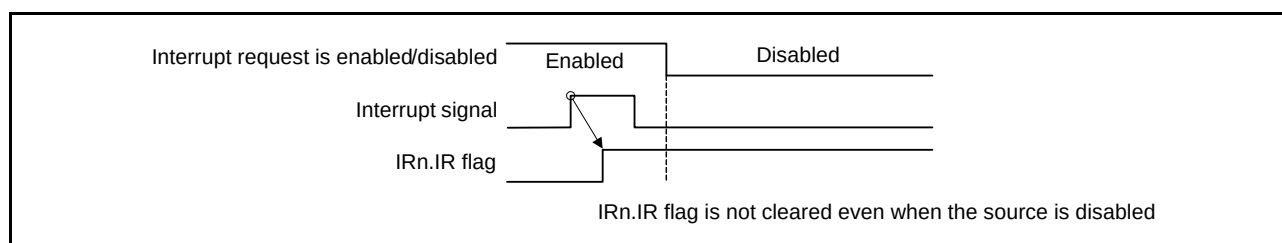


Figure 15.5 Relationship between IRn.IR Flag Operation and Disabling of Interrupt Request

15.4.1.2 Operation of Status Flags for Level-Detected Interrupts

Figure 15.6 shows the operation of the interrupt status flag (IR flag) in IRn (n = interrupt vector number) in the case of level detection of an interrupt from a peripheral module or an external pin.

The IR flag in IRn remains set to 1 as long as the interrupt signal is asserted. To clear the IRn .IR flag to 0, clear the interrupt request in the source generating the interrupt. Confirm that the interrupt request flag in the source generating the interrupt has been cleared to 0 and that the IRn .IR flag has been cleared to 0, and then complete the interrupt handling.

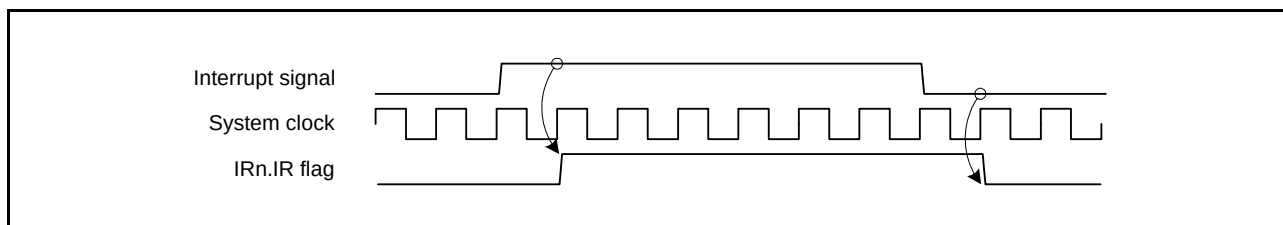


Figure 15.6 IRn .IR Flag Operation for Level Detection Interrupts

Figure 15.7 shows the procedure for handling level detection interrupts.

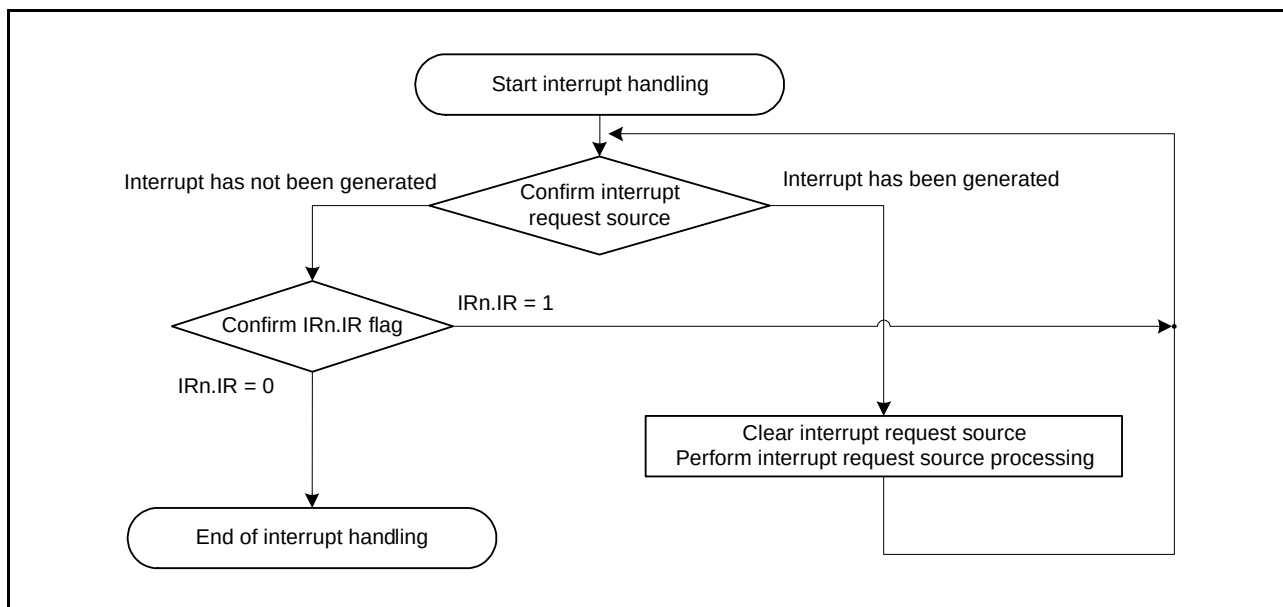


Figure 15.7 Procedure for Handling Level Detection Interrupts

15.4.2 Enabling and Disabling Interrupt Sources

Enabling requests from a given interrupt source requires the following settings.

1. In the case of interrupt requests from peripheral modules, setting the interrupt enable bit for the peripheral module to permit the output of interrupt requests from the source
2. Enabling of the interrupt by the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7)

When an interrupt request that is enabled at the corresponding source is generated, the corresponding IRn.IR flag (n = interrupt vector number) is set to 1.

Setting the IERm.IENj bit to enable an interrupt request allows the interrupt request for which the corresponding IRn.IR is 1 to be output to the interrupt request destination. Setting the IERm.IENj bit to disable an interrupt request suspends the output of the interrupt request for which the corresponding IRn.IR is 1.

The IRn.IR flag is not affected by the IERm.IENj bit.

Use the following procedure to disable interrupt requests.

1. Set the IERm.IENj bit to disable interrupt requests.
2. Set the peripheral module interrupt output enable bit to disable the output. Read the last written register and confirm that writing is completed.
3. Check the IRn.IR flag, and clear the IRn.IR flag if necessary.*1

Note 1. To disable the transmission or reception interrupt of the SCI, RSPI, or RIIC from the enabled state, clear the IRn.IR flag to 0 using the above procedure. For details, see descriptions of the interrupts in section 33, Serial Communications Interface (SCIg, SCIH), section 35, I²C-bus Interface (RIICa), and section 38, Serial Peripheral Interface (RSPIa).

15.4.3 Selecting Interrupt Request Destinations

Possible settings for the request destination of each interrupt are fixed. That is, settings for request destination other than those indicated in Table 15.3, Interrupt Vector Table, are not possible. Do not make an interrupt request destination setting that is not indicated by a “✓” in Table 15.3.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin (i = 0, 1, and 4 to 7), be sure to set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.

The following describes how to specify the destinations of interrupt requests.

(1) DMAC Trigger

Make the following settings for each source while the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) is 0.

1. Specify the vector number of the desired interrupt in the DMAC trigger select register (DMRSRm) for the required channel of the DMAC.*1
2. Set the trigger for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
3. Set the DMAC transfer request enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.

After making the above settings, set the IERm.IENj bit to 1.

In addition, set the DMAC operation enable bit (DMAST.DMST) to 1. The order of making settings for each interrupt and enabling the DMAC operation enable bit does not matter.

For the DMAC setting procedure, refer to section 18.3.7, Activating the DMAC in section 18, DMA Controller (DMACA).

(2) DTC Trigger

Make the following settings for each source while the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) is 0.

1. Set the DTC transfer request enable bit in the DTC transfer request enable register (DTCERn.DTCE (n = interrupt vector number)) for the pertinent source to 1.*1

After making the above settings, set the IERm.IENj bit to 1.

In addition, set the DTC module start bit (DTCST.DTCST) to 1. The order of making settings for each interrupt and enabling the DTC module start bit does not matter.

For the DTC setting procedure, refer to section 19.5, DTC Setting Procedure, in section 19, Data Transfer Controller (DTCa).

Note 1. Do not set a DTC transfer request enable bit (DTCERn.DTCE) and a DMAC trigger select register (DMRSRm) to select the same source. Do not select the same source in more than one DMRSRm register.

(3) CPU Interrupt Request

If the interrupt request destination is neither the DMAC nor the DTC, the interrupt request is sent to the CPU. Set the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) to 1 while neither the DMAC trigger settings nor the DTC trigger settings described above are in place.

Table 15.4 shows operation when the DMAC or DTC is the request destination.

Table 15.4 Operation When Starting the DMAC/DTC

Interrupt Request Destination	DISEL *1	Remaining Number of Transfer Operations	Operation per Request	IR*2	Interrupt Request Destination after Transfer
DMAC	1	≠ 0	DMA transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DMAC
		= 0	DMA transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The DMACm.DMCNT.DTE bit is cleared and the CPU becomes the destination.
	0	≠ 0	DMA transfer	Cleared at the start of DMAC transfer	DMAC
		= 0	DMA transfer*3	Cleared at the start of DMAC transfer*3	The DMACm.DMCNT.DTE bit is cleared and the CPU becomes the destination.
DTC*4	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The DTCERn.DTCE bit is cleared and the CPU becomes the destination.
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after reading DTC transfer information	DTC
		= 0	DTC transfer → CPU interrupt*3	Cleared on interrupt acceptance by the CPU*3	The DTCERn.DTCE bit is cleared and the CPU becomes the destination.

Note 1. DISEL for the DMAC is set by the DMACm.DMCSL.DISEL bit; DISEL for the DTC is set by the DTC.MRB.DISEL bit.

Note 2. When the IRn.IR flag is 1, an interrupt request (DTC or DMA transfer request) that is generated again will be ignored.

Note 3. When the DISEL bit is 0, operation with the remaining number of transfer operations being 0 differs according to whether the source is for the DTC or DMAC.

Note 4. For chain transfer, DTC transfer continues until the last chain transfer ends. Whether a CPU interrupt is generated at the end of chain transfer, the IRn.IR flag clear timing, and the interrupt request destination after transfer are determined by the state of DISEL and the remaining transfer count at the end of chain transfer. For the chain transfer, see Table 19.3, Chain Transfer Conditions in section 19, Data Transfer Controller (DTCa).

The request destination for an interrupt should be changed while the IERm.IENj bit is 0.

When a source is to be changed to an interrupt request or the DMAC trigger source is to be changed while a transfer is not complete (i.e. while the DMACm.DMCNT.DTE bit has not been cleared) after the settings described under (1) DMAC Trigger have been made, follow the procedure below.

1. For both the source to be withdrawn and the source that will have a new trigger, clear the IENj bits in IERm to 0.
2. Check the state of transfer by the DMAC. If transfer is in progress, wait for its completion.
3. Make the settings described under (1) DMAC Trigger.

When a source is to be changed to an interrupt request or the DTC transfer information is to be changed while a transfer is not complete (i.e. while the DTCERn.DTCE bit (n = interrupt vector number) has not been cleared) after the settings described under (2) DTC Trigger have been made, follow the procedure below.

1. For both the source to be withdrawn and the source that will have a new trigger, clear the IENj bits in IERm to 0.
2. Check the state of transfer by the DTC. If transfer is in progress, wait for its completion.
3. Make the settings described under (2) DTC Trigger.

15.4.4 Determining Priority

Interrupt priority is determined for each interrupt request destination.

The priority for each interrupt request destination is determined as follows.

(1) Determining Priority when the CPU is the Request Destination of the Interrupt

A source selected for the fast interrupt has the highest priority. After that, an interrupt source with a larger value of the interrupt priority level select bits (IPR[3:0]) in IPR_n takes priority. If interrupts with the same priority level are generated by multiple sources, the source with the smallest vector number takes precedence.

(2) Determining Priority when the DTC is the Request Destination of the Interrupt

The IPR[3:0] bits in IPR_n (n = interrupt vector number) have no effect. An interrupt source with a smaller vector number takes precedence.

(3) Determining Priority when the DMAC is the Request Destination of the Interrupt

The IPR[3:0] bits in IPR_n have no effect. Regarding the order of priority of DMAC channels, see section 18, DMA Controller (DMACA).

15.4.5 Multiple Interrupts

To enable multiple interrupts of the CPU, set the PSW.I bit to 1 (interrupt enabled) in the handling routine of accepted interrupts.

The PSW.IPL[3:0] bits immediately after processing branches to the interrupt handling routine are set to the same value as the interrupt priority level of the accepted interrupt request. If an interrupt request which has an interrupt level higher than that of the PSW.IPL[3:0] bits is generated at this time, this interrupt request (for multiple interrupts) is accepted. If the interrupt priority level of the accepted interrupt request is 15 (fast interrupt or interrupt when IPR[3:0] are set to 1111b), multiple interrupts are not generated.

15.4.6 Fast Interrupt

The fast interrupt is an interrupt for executing a faster interrupt response by the CPU, so only one of the interrupt sources can be assigned.

The interrupt priority level of the fast interrupt is 15 (highest) regardless of the setting of the IPR[3:0] bits in IPR_n (n = interrupt vector number). In addition, the fast interrupt is accepted with precedence over other interrupt sources with level 15. However, when the value of the PSW.IPL[3:0] bits are 1111b (priority level 15), even the fast interrupt cannot be accepted.

To assign an interrupt source to the fast interrupt, specify the vector number of the source in the FIR.FVCT[7:0] bits, and set the FIR.FIEN bit to 1 (fast interrupt is enabled).

For details on the fast interrupt, see section 2, CPU and section 14, Exception Handling.

15.4.7 Digital Filter

The digital filter function is provided for the external interrupt request IRQi pins (i = 0, 1, and 4 to 7) and NMI pin interrupt.

The digital filter samples input signals at the filter sampling clock (PCLK) and removes the pulses of which length is less than three sampling cycles.

To use the digital filter for the IRQi pin, set the sampling clock cycle (PCLK, PCLK/8, PCLK/32, or PCLK/64) with the IRQFLTC0.FCLKSELi[1:0] bits and set the IRQFLTE0.FLTENi bit to 1 (digital filter enabled).

To use the digital filter for the NMI pin, set the sampling clock cycle (PCLK, PCLK/8, PCLK/32, or PCLK/64) with the NMIFLTC.NFCLKSEL[1:0] bits and set the NMIFLTE.NFLTEN bit to 1 (digital filter enabled).

Figure 15.8 shows an example of digital filter operation.

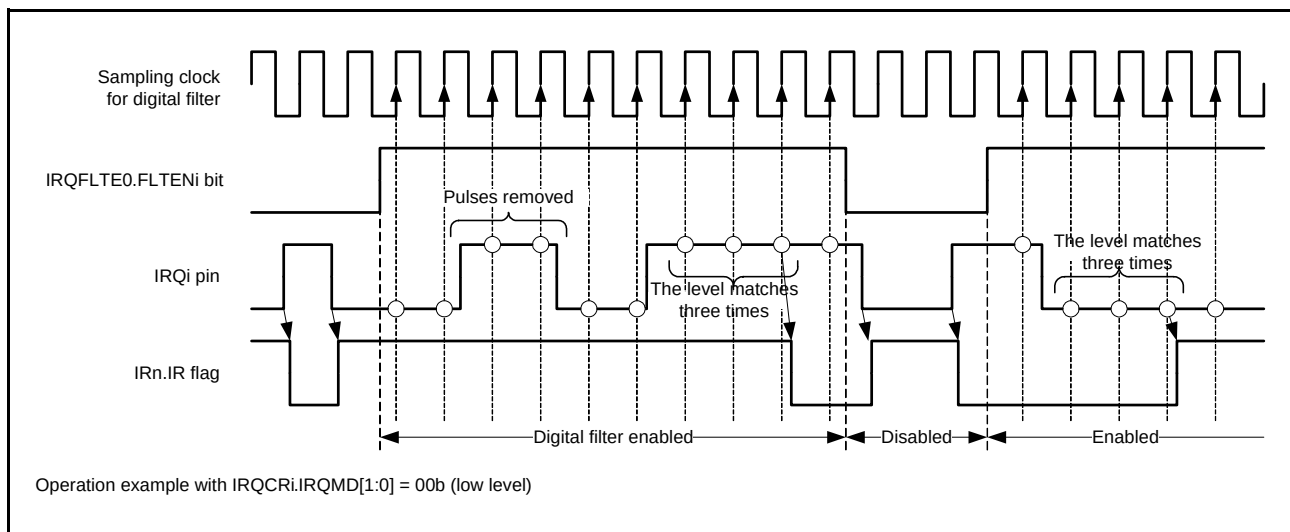


Figure 15.8 Digital Filter Operation Example

Before software standby mode is entered, set the IRQFLTE0.FLTENi and NMIFLTE.NFLTEN bits to 0 (digital filter disabled). To use the digital filter again after return from software standby mode, set the IRQFLTE0.FLTENi or NMIFLTE.NFLTEN bit to 1 (digital filter enabled).

15.4.8 External Pin Interrupts

The procedure for using the signal on an external pin as an interrupt is as follows.

1. Clear the IERm.IENj bit (m = 02h to 1Fh, j = 0 to 7) to 0 (interrupt request disabled).
2. Clear the IRQFLTE0.FLTENi bit (i = 0, 1, and 4 to 7) to 0 (digital filter disabled).^{*1}
3. Set the digital filter sampling clock with the IRQFLTC0.FCLKSELi[1:0] bits.^{*1}
4. Make or confirm the I/O port settings.
5. Set the method of detection for the interrupt in the IRQCRi.IRQMD[1:0] bits.
6. Clear the corresponding IRn.IR flag (n = interrupt vector number) to 0 (if edge detection is in use).
7. Set the IRQFLTE0.FLTENi bit to 1 (digital filter enabled).^{*1}
8. If the interrupt is to be used for DMAC trigger, set the DMRSRm.DMRS[7:0] bits. If the interrupt is to be used for DTC trigger, set the DTCERn.DTCE bit. The interrupt will be a CPU interrupt if neither of these settings is made.
9. Set the IERm.IENj bit to 1 (interrupt request enabled).

Note 1. To use the digital filter function, settings must be made beforehand.

15.5 Non-maskable Interrupt Operation

There are six types of non-maskable interrupt: the NMI pin interrupt, oscillation stop detection interrupt, WDT underflow/refresh error, IWDT underflow/refresh error, voltage monitoring 1 interrupt, and VBATT voltage monitoring interrupt. Non-maskable interrupts are only usable as interrupts for the CPU; that is, they are not capable of DTC or DMAC trigger. Non-maskable interrupts take precedence over all interrupts, including the fast interrupt. Non-maskable interrupt requests are accepted regardless of the states of the I (interrupt enable) bit and IPL[3:0] (processor interrupt priority level) bits in the PSW of the CPU. The current states of the non-maskable interrupts can be checked in the non-maskable interrupt status register (NMISR).

Confirm that all bits in the NMISR have returned to 0 from within the handler for the non-maskable interrupt, before ending the handler.

Non-maskable interrupts are disabled by default. If a system is to use non-maskable interrupts, the following procedure must be followed at the beginning of program processing.

Non-maskable interrupt usage procedure:

1. Set the stack pointer (SP).
2. To use the NMI pin, clear the NMIFLTE.NFLTEN bit to 0 (digital filter disabled).^{*1}
3. To use the NMI pin, set the digital filter sampling clock with the NMIFLTC.NFCLKSEL[1:0] bits.^{*1}
4. To use the NMI pin, set the NMI pin detection sense with the NMICR.NMIMD bit.
5. To use the NMI pin, write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
6. To use the NMI pin, set the NMIFLTE.NFLTEN bit to 1 (digital filter enabled).^{*1}
7. Enable the non-maskable interrupt by writing 1 to the corresponding bit in the non-maskable interrupt enable register (NMIER).

Note 1. To use the digital filter function, settings must be made beforehand.

After 1 is written to the NMIER register, subsequent write access to the NMIE bit in NMIER is ignored. The NMI interrupt cannot be disabled. It can be disabled only by a reset.

For the flow of non-maskable interrupt processing, see section 14, Exception Handling.

Writing 1 to the NMICLR.NMICLR bit clears the NMI status flag (NMISR.NMIST) to 0.

Writing 1 to the NMICLR.OSTCLR bit clears the oscillation stop detection interrupt status flag (NMISR.OSTST) to 0.

Writing 1 to the NMICLR.WDTCLR bit clears the WDT underflow/refresh error status flag (NMISR.WDTST) to 0.

Writing 1 to the NMICLR.IWDTCLR bit clears the IWDT underflow/refresh error status flag (NMISR.IWDTST) to 0.

Writing 1 to the NMICLR.LVD1CLR bit clears the voltage monitoring 1 interrupt status flag (NMISR.LVD1ST) to 0.

Writing 1 to the NMICLR.VBATCLR bit clears the VBATT voltage monitoring interrupt status flag (NMISR.VBATST) to 0.

15.6 Return from Power-Down States

The interrupt sources that can be used to return operation from sleep mode, deep sleep mode, or software standby mode are listed in Table 15.3, Interrupt Vector Table.

For details, refer to section 11, Low Power Consumption. The following describes how to use an interrupt to return operation from each low power consumption mode.

15.6.1 Return from Sleep Mode or Deep Sleep Mode

If the interrupt controller is to return operation from sleep mode in response to an interrupt or non-maskable interrupt, make the following settings for the interrupt.

- Interrupts
 1. Select the CPU as the interrupt request destination.
 2. Use the IEN_j bit in IER_m (m = 02h to 1Fh, j = 0 to 7) to enable the given interrupt request.
 3. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.
- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

15.6.2 Return from Software Standby Mode

The interrupt controller can return operation from a non-maskable interrupt or an interrupt that enables the return from the software standby mode.

The conditions for the return are listed below.

- Interrupts
 1. Select the interrupt source that enables the return from the software standby mode.
 2. Select the CPU as the interrupt request destination.
 3. Use the IEN_j bit in IER_m (m = 02h to 1Fh, j = 0 to 7) to enable the given interrupt request.
 4. Set a priority level higher than that set by the IPL[3:0] bits in the PSW of CPU.
(For the interrupt source specified as a fast interrupt, as well as setting the fast interrupt set register (FIR), the interrupt priority level (IPR_n (n = interrupt vector number)) should be set above the level set by IPL in the PSW of the CPU.)

Interrupt requests through the IRQ pins that do not satisfy the above conditions are not detected while the clock is stopped in software standby mode.

- Non-maskable interrupts

Use the NMIER register to enable the given interrupt request.

- Procedure to make a transition to/from software standby mode
 1. Before software standby mode is entered, disable the digital filter for the interrupt source as a return target (IRQFLTE0.FLTEN_i = 0, NMIFLTE.NFLTEN = 0).
 2. To use the digital filter again after return from software standby mode, enable the digital filter (IRQFLTE0.FLTEN_i = 1, NMIFLTE.NFLTEN = 1).

15.7 Usage Note

15.7.1 Note on WAIT Instruction Used with Non-Maskable Interrupt

Before executing the WAIT instruction, check to see that all the status flags in NMISR are 0.

16. Buses

16.1 Overview

Table 16.1 lists the bus specifications, Figure 16.1 shows the bus configuration, and Table 16.2 lists the addresses assigned for each bus.

Table 16.1 Bus Specifications

Bus Type		Description
CPU bus	Instruction bus	- Connected to the CPU (for instructions) - Connected to on-chip memory (RAM, ROM) - Operates in synchronization with the system clock (ICLK)
	Operand bus	- Connected to the CPU (for operands) - Connected to on-chip memory (RAM, ROM) - Operates in synchronization with the system clock (ICLK)
Memory bus	Memory bus 1	Connected to RAM
	Memory bus 2	Connected to ROM
Internal main bus	Internal main bus 1	- Connected to the CPU - Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	- Connected to the DMAC and DTC - Connected to on-chip memory (RAM, ROM) - Operates in synchronization with the system clock (ICLK)
Internal peripheral bus	Internal peripheral bus 1	- Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) - Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	- Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) - Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	- Connected to peripheral modules (USB0, RSCAN, and CTSU) - Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	- Connected to peripheral modules (MTU2) - Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	- Connected to the flash control module and E2 DataFlash - Operates in synchronization with the FlashIF clock (FCLK)

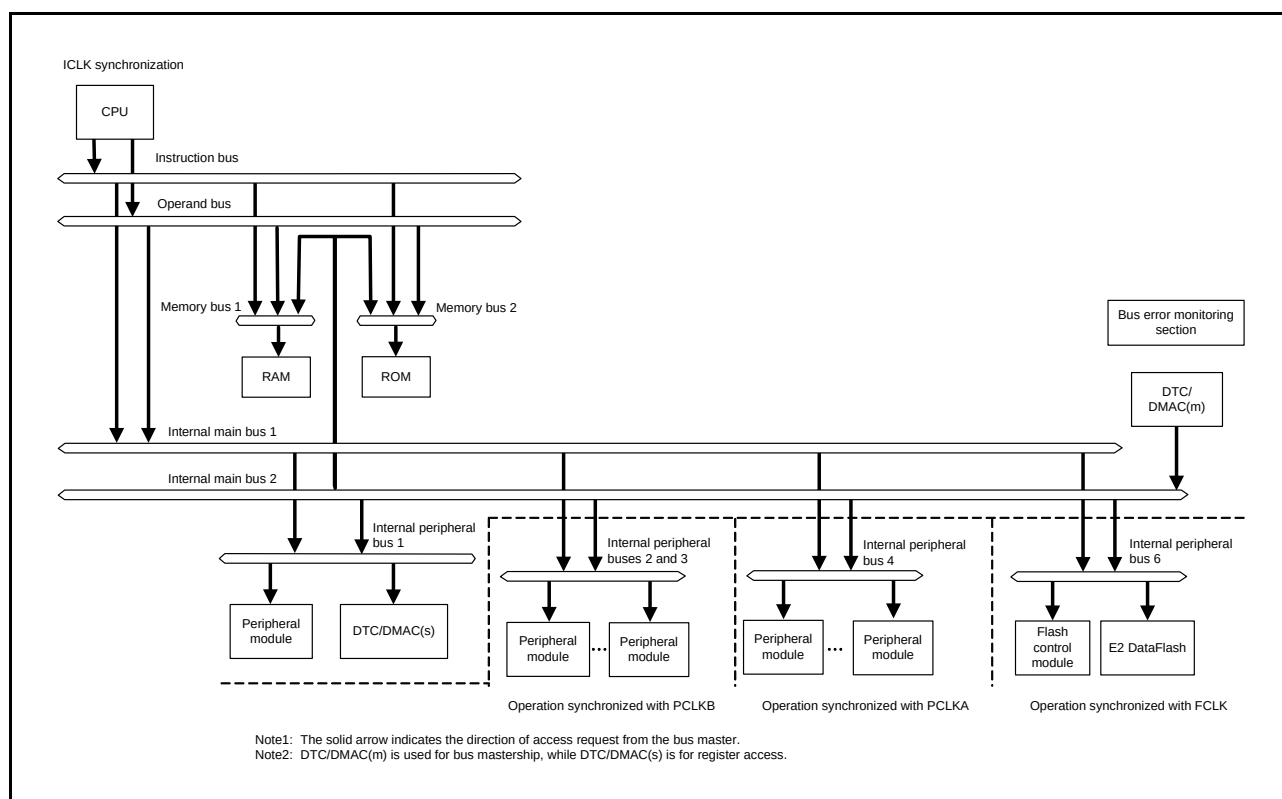


Figure 16.1 Bus Configuration

Table 16.2 Addresses Assigned for Each Bus

Address	Bus	Area
0000 0000h to 0000 FFFFh	Memory bus 1	RAM
0001 0000h to 0007 FFFFh		Reserved area
0008 0000h to 0008 7FFFh	Internal peripheral bus 1	Peripheral I/O registers
0008 8000h to 0009 FFFFh	Internal peripheral bus 2	
000A 0000h to 000B FFFFh	Internal peripheral bus 3	
000C 0000h to 000D FFFFh	Internal peripheral bus 4	
000E 0000h to 000F FFFFh	Reserved area	Reserved area
0010 0000h to 007F FFFFh	Internal peripheral bus 6	Flash control module and E2 DataFlash
0080 0000h to 00FF FFFFh		Reserved area
0100 0000h to 04FF FFFFh	Reserved area	
0500 0000h to 07FF FFFFh		
0800 0000h to 0FFF FFFFh		
1000 0000h to 7FFF FFFFh		
8000 0000h to FFFF FFFFh	Memory bus 2	ROM (for reading only)
FF00 0000h to FFFF FFFFh		

16.2 Description of Buses

16.2.1 CPU Buses

The CPU buses consist of the instruction and operand buses, which are connected to internal main bus 1. As the names suggest, the instruction bus is used to fetch instructions for the CPU, while the operand bus is used for operand access. The instruction bus is 64 bits while the operand bus is 32 bits.

Connection of the instruction and operand buses to RAM and ROM provides the CPU with direct access to these areas, i.e. access is not via internal main bus 1. However, only reading is possible in direct access to ROM by the CPU; programming and erasure are handled via an internal peripheral bus.

Bus requests for instruction fetching and operand access are arbitrated through internal main bus 1. The order of priority is operand access then instruction fetching.

If instruction fetching and operand access are requested for different buses (memory bus 1, memory bus 2, and internal main bus 1), the bus-access operations can proceed simultaneously. For example, parallel access to ROM and RAM is possible.

16.2.2 Memory Buses

The memory buses consist of memory bus 1 and memory bus 2. RAM is connected to memory bus 1 and ROM is connected to memory bus 2. The memory buses are 64 bits. Requests for bus mastership from the CPU buses (instruction fetching and operand) and internal main bus 2 are arbitrated through memory buses 1 and 2.

The priority order of the buses can be set using the memory bus 1 (RAM) priority control bits (BPRA[1:0]) and memory bus 2 (ROM) priority control bits (BPRO[1:0]) in the bus priority control register (BUSPRI) for the corresponding memory buses. When the priority order is fixed, internal main bus 2 has priority over the CPU bus (operand over instruction fetching). When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

16.2.3 Internal Main Buses

The internal main buses consist of a bus for use by the CPU (internal main bus 1) and a bus for use by the other bus-master modules, i.e. the DTC and DMAC (internal main bus 2).

Bus requests for instruction fetching and operand access are arbitrated through internal main bus 1. The order of priority is operand access then instruction fetching.

Requests for bus mastership from the DTC and DMAC are arbitrated by internal main bus 2. The priority order is the DMAC and then DTC as listed in Table 16.3.

Between the DTC and DMAC, only the one that accepted the activation request issues the bus mastership request. The priority order of activation requests between the DTC and DMAC is DMAC0, DMAC1, DMAC2, DMAC3, and then DTC, regardless of the BUSPRI setting.

If the CPU and another bus master are requesting access to different buses (on-chip memory, internal peripheral buses 1 to 4, and 6), the respective bus-access operations can proceed simultaneously.

However, when the CPU executes the XCHG instruction, requests for bus access from masters other than the CPU are not accepted until data transfer for the XCHG instruction is completed regardless of the bus priority control register (BUSPRI) setting. Furthermore, requests for bus access from masters other than the DTC are not accepted during reading and writing-back of transfer control information for the DTC.

Table 16.3 Order of Priority for Bus Masters

Priority	Internal main buses	Bus Master
High	2	DMAC
		DTC
Low	1	CPU

Note: The above applies when the priority order of the buses is fixed.
 The priority order of internal main bus 1 and another bus (internal main bus 2) can be toggled by the bus priority control register (BUSPRI) (round-robin method).

16.2.4 Internal Peripheral Buses

Connection of peripheral modules to the internal peripheral buses is as described in Table 16.4.

Table 16.4 Connection of Peripheral Modules to the Internal Peripheral Buses

Type of Bus	Peripheral Modules
Internal peripheral bus 1	DTC, DMAC, interrupt controller, and bus error monitoring section
Internal peripheral bus 2	Peripheral modules other than those connected to internal peripheral buses 1, 3, and 4
Internal peripheral bus 3	USB0, RSCAN, and CTSU
Internal peripheral bus 4	MTU2
Internal peripheral bus 6	Flash control module and E2 DataFlash

Requests for bus mastership from the CPU (internal main bus 1) and other bus masters (internal main bus 2) are arbitrated through internal peripheral buses 1 to 4, and 6.

The priority order of two internal main buses can be set using the bus priority control register (BUSPRI). The priority order can be set with the internal peripheral bus 1 priority control bits (BUSPRI.BPIB[1:0]), internal peripheral bus 2 and 3 priority control bits (BUSPRI.BPGB[1:0]), internal peripheral bus 4 priority control bits (BUSPRI.BPHB[1:0]), and internal peripheral bus 6 priority control bits (BUSPRI.BPFB[1:0]) for the corresponding internal peripheral buses.

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1. When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted (round-robin method).

The order of accepting requests may change depending on the BUSPRI setting (Refer to Figure 16.2).

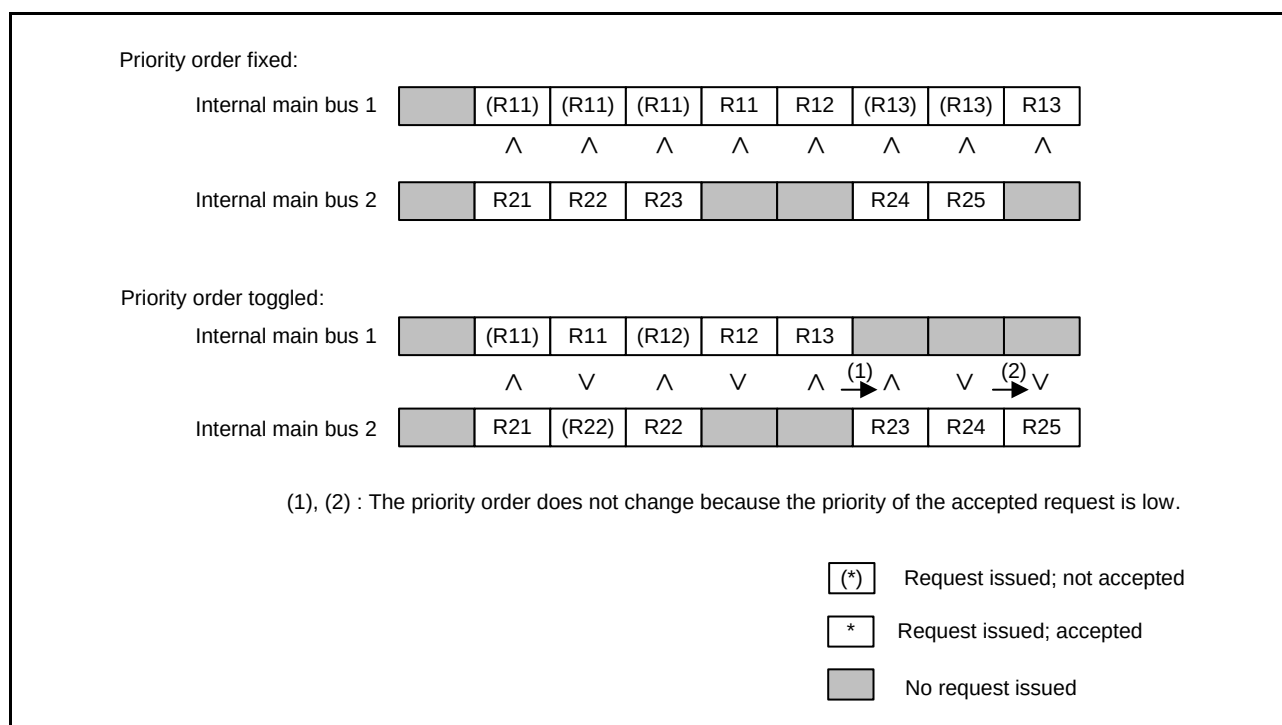


Figure 16.2 Priority Order between Internal Peripheral Bus Accesses

16.2.5 Write Buffer Function (Internal Peripheral Bus)

The internal peripheral bus has the write buffer function, which allows the next round of bus access to start, before the current write access is completed, in write access. However, if the following round of bus access is from the same bus master but to the different internal peripheral bus, it is suspended until the bus operations already in progress are completed. When read access to the internal memory is scheduled after the write access to the internal peripheral bus from the CPU, the following round of bus access can be started before the current bus operation is completed and thus the order of accesses may be changed (Refer to Figure 16.3).

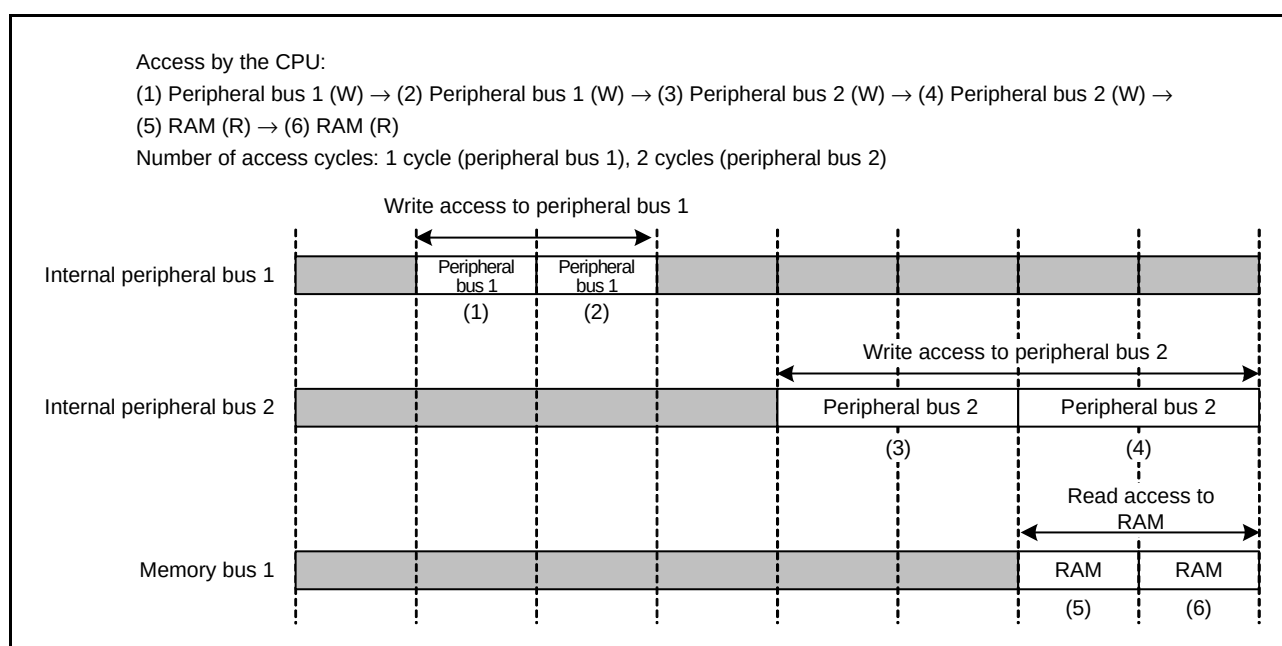


Figure 16.3 Write Buffer Function

16.2.6 Parallel Operation

Parallel operation is possible when different bus-master modules are requesting access to different slave modules. For example, if the CPU is fetching an instruction from ROM and an operand from RAM, the DMAC is able to handle transfer between a peripheral bus and the peripheral bus at the same time.

An example of parallel operations is shown in Figure 16.4. In this example, the CPU is able to employ the instruction and operand buses for simultaneous access to ROM and RAM, respectively. Furthermore, the DMAC simultaneously employs internal main bus 2 for access to a peripheral bus during access to RAM and ROM by the CPU.

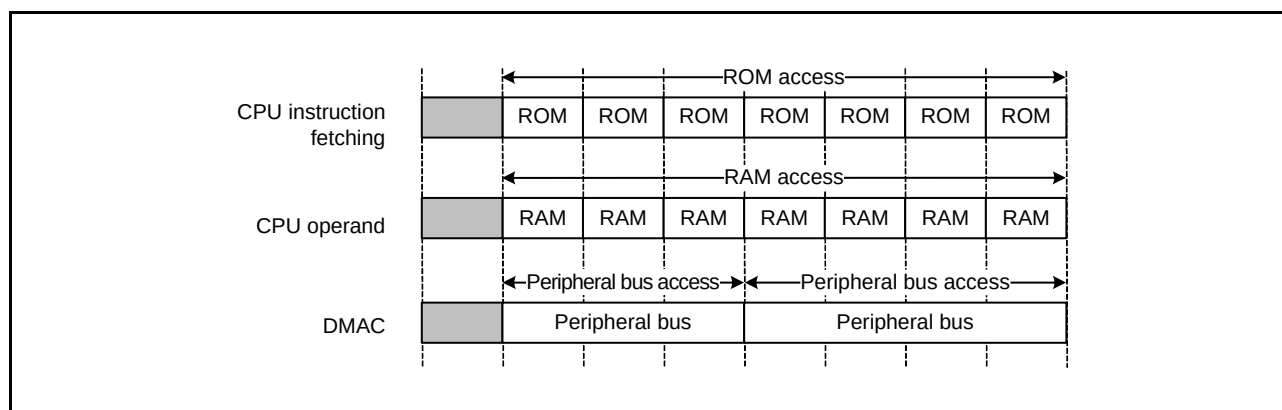


Figure 16.4 Example of Parallel Operations

16.3 Register Descriptions

16.3.1 Bus Error Status Clear Register (BERCLR)

Address(es): 0008 1300h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	STSCLR
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	STSCLR	Status Clear	0: Invalid 1: Bus error status register cleared	(W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only writing 1 is effective; i.e. writing 0 has no effect.

STSCLR Bit (Status Clear)

Writing 1 to this bit clears the bus error status registers 1 and 2 (BERSR1 and BERSR2).

Writing 0 has no effect. It is read as 0.

16.3.2 Bus Error Monitoring Enable Register (BEREN)

Address(es): 0008 1304h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	TOEN	IGAEN
0	0	0	0	0	0	0	0

Value after reset:

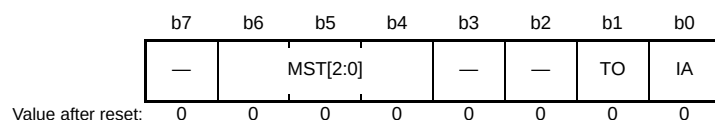
Bit	Symbol	Bit Name	Description	R/W
b0	IGAEN	Illegal Address Access Detection Enable	0: Illegal address access detection is disabled. 1: Illegal address access detection is enabled.	R/W
b1	TOEN	Timeout Detection Enable*1, *2	0: Bus timeout detection is disabled. 1: Bus timeout detection is enabled.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When detection is disabled (the TOEN bit is cleared to 0), bus access can cause the bus to freeze.

Note 2. Do not clear the TOEN bit to 0 (bus timeout detection disabled) while timeout errors are being detected.

16.3.3 Bus Error Status Register 1 (BERSR1)

Address(es): 0008 1308h



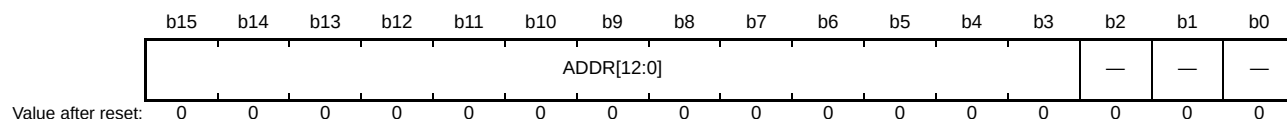
Bit	Symbol	Bit Name	Description	R/W
b0	IA	Illegal Address Access	0: Illegal address access not made 1: Illegal address access made	R
b1	TO	Timeout	0: Timeout not generated 1: Timeout generated	R
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b6 to b4	MST[2:0]	Bus Master Code	b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

MST[2:0] Bits (Bus Master Code)

These bits indicate the bus master that accessed a bus when a bus error occurred.

16.3.4 Bus Error Status Register 2 (BERSR2)

Address(es): 0008 130Ah



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15 to b3	ADDR[12:0]	Bus Error Occurrence Address	The upper 13 bits of an address that was accessed when a bus error occurred (in units of 512 Kbytes).	R

16.3.5 Bus Priority Control Register (BUSPRI)

Address(es): 0008 1310h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	BPFB[1:0]	BPHB[1:0]	BPGB[1:0]	BPIB[1:0]	BPRO[1:0]	BPRO[1:0]	BPRO[1:0]	BPRO[1:0]	BPRO[1:0]	BPRO[1:0]	BPRO[1:0]	BPRO[1:0]
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BPRA[1:0]	Memory Bus 1 (RAM) Priority Control	b1 b0 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(W) *1
b3, b2	BPRO[1:0]	Memory Bus 2 (ROM) Priority Control	b3 b2 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(W) *1
b5, b4	BPIB[1:0]	Internal Peripheral Bus 1 Priority Control	b5 b4 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(W) *1
b7, b6	BPGB[1:0]	Internal Peripheral Bus 2 and 3 Priority Control	b7 b6 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(W) *1
b9, b8	BPHB[1:0]	Internal Peripheral Bus 4 Priority Control	b9 b8 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(W) *1
b11, b10	BPFB[1:0]	Internal Peripheral Bus 6 Priority Control	b11 b10 0 0: The order of priority is fixed. 0 1: The order of priority is toggled. 1 0: Setting prohibited 1 1: Setting prohibited	R(W) *1
b15, b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits can be written to only once while the DTC and DMAC are stopped. When they are written to more than one time, the operation is not guaranteed.

BPRA[1:0] Bits (Memory Bus 1 (RAM) Priority Control)

These bits specify the priority order for memory bus 1 (RAM).

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPRO[1:0] Bits (Memory Bus 2 (ROM) Priority Control)

These bits specify the priority order for memory bus 2 (ROM).

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPIB[1:0] Bits (Internal Peripheral Bus 1 Priority Control)

These bits specify the priority order for internal peripheral bus 1.

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPGB[1:0] Bits (Internal Peripheral Bus 2 and 3 Priority Control)

These bits specify the priority order for internal peripheral buses 2 and 3.

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPHB[1:0] Bits (Internal Peripheral Bus 4 Priority Control)

These bits specify the priority order for internal peripheral bus 4.

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

BPFB[1:0] Bits (Internal Peripheral Bus 6 Priority Control)

These bits specify the priority order for internal peripheral bus 6.

When the priority order is fixed, internal main bus 2 has priority over internal main bus 1.

When the priority order is toggled, a bus has a lower priority when the request of that bus is accepted.

16.4 Bus Error Monitoring Section

The bus error monitoring section monitors the individual areas for bus errors, and when a bus error occurs, the error is indicated to the bus master.

16.4.1 Types of Bus Error

There are two types of bus error: illegal address access and timeout.

Illegal address access is the detection of illegal access to an area, and time-out is the detection of a bus-access operation not being completed within 768 cycles.

16.4.1.1 Illegal Address Access

When the illegal address access detection enable bit (IGAEN) in the bus error monitoring enable register (BEREN) is set to 1, access to the illegal address ranges will lead to illegal address access errors.

The address ranges where access will lead to illegal address access errors are indicated in Table 16.5.

16.4.1.2 Timeout

When the timeout detection enable bit (TOEN) in the bus error monitoring enable register (BEREN) is set to 1, bus access that is not completed within 768 cycles leads to a timeout error.

- Internal peripheral buses (2 and 3): Bus access is not completed within 768 peripheral module clock (PCLKB) cycles from the start of the access. In this MCU, a timeout error does not occur.
Once a timeout error occurs, accesses from the bus master are rejected for 256 PCLKB cycles.
- Internal peripheral buses (4): Bus access is not completed within 768 peripheral module clock (PCLKA) cycles from the start of the access.
Once a timeout error occurs, accesses from the bus master are rejected for 256 PCLKA cycles.
- Internal peripheral bus (6): Bus access is not completed within 768 FlashIF clock (FCLK) cycles from the start of the access.
Once a timeout error occurs, accesses from the bus master are rejected for 256 FCLK cycles. In this MCU, a timeout error does not occur.

16.4.2 Operations When a Bus Error Occurs

When a bus error occurs, the error is indicated to the CPU. Operation is not guaranteed when a bus error occurs.

- Bus error indication to the CPU

An interrupt is generated. The IERn register in the ICU can specify whether to generate an interrupt in the case of a bus error.

16.4.3 Conditions Leading to Bus Errors

Table 16.5 lists the types of bus errors for each area in the respective address space.

If an illegal address access error or timeout is detected when no bus error has occurred (bus error status register n (BERSRn; n = 1 or 2) is cleared), the detected error is reflected on the BERSRn. Once a bus error occurs, no subsequent bus errors are reflected on the register unless the register is cleared.

If bus errors are simultaneously caused by two or more bus masters, error information of only one bus master is reflected. Once a bus error occurs, the status is retained until BERSRn is cleared.

Table 16.5 Types of Bus Errors

Address	Type of Area	Type of Error	
		Illegal Address Access	Timeout
0000 0000h to 0007 FFFFh	Memory bus 1	—	—
0008 0000h to 0008 7FFFh	Internal peripheral bus 1	—	—
0008 8000h to 0009 FFFFh	Internal peripheral bus 2	Δ	—
000A 0000h to 000B FFFFh	Internal peripheral bus 3	Δ	—
000C 0000h to 000D FFFFh	Internal peripheral bus 4	Δ	✓
000E 0000h to 000F FFFFh	Reserved area	—	—
0010 0000h to 0011 FFFFh	Internal peripheral bus 6	—	—
0012 0000h to 007F FFFFh		Δ	—
0080 0000h to 00FF FFFFh		—	—
0100 0000h to 07FF FFFFh	Reserved area	—	—
0800 0000h to 0FFF FFFFh		—	—
1000 0000h to 7FFF FFFFh		✓	—
8000 0000h to FFFF FFFFh	Memory bus 2	—	—
FF00 0000h to FF7F FFFFh		—	—
FF80 0000h to FFFF FFFFh		—	—

—: A bus error does not result.

Δ: A bus error may or may not result.

✓: A bus error results.

Note: The capacity of the RAM, E2 DataFlash, and ROM differs depending on the product. For details, see section 49, RAM, section 50, Flash Memory (FLASH).

16.5 Interrupt

16.5.1 Interrupt Source

An illegal address access error or detection of a timeout leads to a bus error signal for the interrupt controller.

Table 16.6 Interrupt Source

Name	Interrupt Source	DTC Activation	DMAC Activation
BUSERR	Illegal address access error or timeout	Not possible	Not possible

17. Memory-Protection Unit (MPU)

17.1 Overview

The RXv2 CPU incorporates a memory-protection unit that checks the addresses of CPU access to the overall address space (0000 0000h to FFFF FFFFh).

Access-control information can be set for up to eight regions, and permission for access to each region is in accord with this information. The default response to the detection of access to a region where permission has not been set is the generation of a memory-protection error.

The supported access-control information for the individual regions consists of permission to read, permission to write, and permission to execute. This access-control information is effective when the processor mode of the CPU is user mode. Memory protection is not applied when the CPU is in supervisor mode.

Table 17.1 lists the specifications of the memory-protection unit, and Figure 17.1 shows a block diagram of the memory-protection unit.

Table 17.1 Specifications of Memory Protection

Specifications	Description
Region to be covered by memory protection and processor mode	0000 0000h to FFFF FFFFh (in user mode) No memory protection in supervisor mode
Number of regions	8
Page size (smallest unit of protection)	16 bytes
Specifying addresses of individual regions	Setting the page numbers where regions start and end
Setting to make memory protection effective or ineffective in individual regions	A V (valid) bit in each region-n end page number register (REPAGEn) makes the settings effective or ineffective for the corresponding region (n = 0 to 7).
Access-control information settings for individual regions	Instruction execution: Permission to execute Operand access: Permission to read, permission to write
Start of memory-protection operations	After the memory-protection unit has been enabled, access monitoring starting up with the transition to user mode.
Memory-protection error processing	Generation of access exceptions
Addresses where memory-protection errors are generated	Address in instruction execution: The PC value is preserved on the stack. Address in operand access: The address is stored in the data memory-protection error address register (MPDEA).
Determining the reasons for memory-protection errors	The memory-protection error status register (MPESTS) holds indicators of the reason.
Background region setting	Access-control information can be set for the background region (the whole address space).
Processing where regions overlap	The access-control information for access to an overlap between regions is the logical OR of the attributes for the given regions, and permission is given priority.

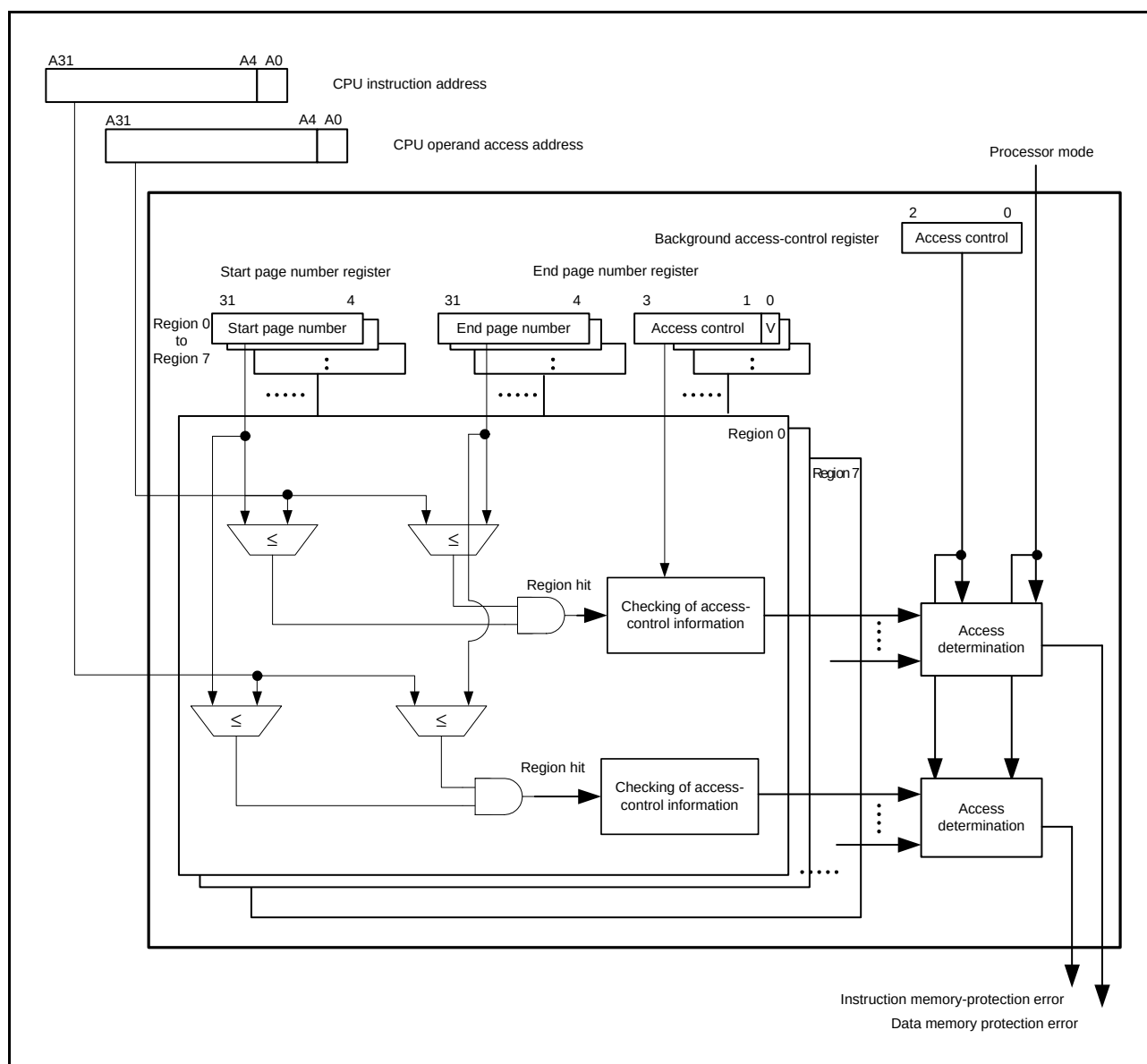


Figure 17.1 Block Diagram of the Memory-Protection Unit

17.1.1 Types of Access Control

There are three types of access control information: permission for instruction execution, permission to read operands, and permission to write operands. Violations of these types of access control are only detected when programs are running in user mode. Violations are not detected when programs are running in supervisor mode.

17.1.2 Regions for Access Control

Up to eight regions for access control are definable. Settings of the range of memory for each access-control region are made in the corresponding region-n start page number register (RSPAGEn) and region-n end page number register (REPAGEn), where n = 0 to 7.

The minimum unit for control of access is the “page”, by which the address space is divided into 16-byte units. The 28 higher-order bits ([31:4]) of the address [31:0] bits correspond to the page number.

The REPAGEn register specifies the access-control information for each area and whether the area is enabled or not.

17.1.3 Background Region

“Background region” refers to the whole address space (0000 0000h to FFFF FFFFh). Access-control information for the background region is set in the background-region access-control register (MPBAC). In contrast to the access-control information for the eight individual regions, protection information for the background region is effective as long as memory protection is enabled (the MPEN bit in the MPEN register is 1).

17.1.4 Overlap between Regions

In cases of overlap between multiple regions, the access-control information becomes the logical OR of the access-control bits for the overlapping regions (including the background region), with permission given priority.

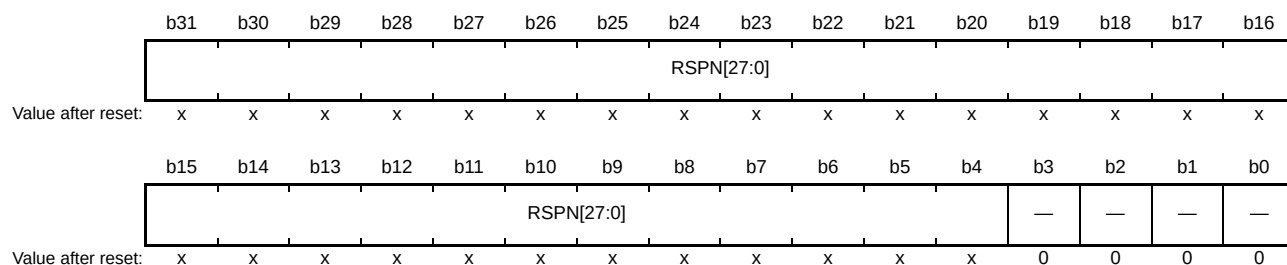
17.1.5 Instructions and Data that Span Regions

Operations in response to the detection of memory-protection errors when instructions or data span regions for which different access-control settings have been made are undefined. Ensure that instructions and data do not span regions for which different access-control settings have been made.

17.2 Register Descriptions

17.2.1 Region-n Start Page Number Register (RSPAGEn) (n = 0 to 7)

Address(es): RSPAGE0 0008 6400h, RSPAGE1 0008 6408h, RSPAGE2 0008 6410h, RSPAGE3 0008 6418h, RSPAGE4 0008 6420h, RSPAGE5 0008 6428h, RSPAGE6 0008 6430h, RSPAGE7 0008 6438h



x: Undefined

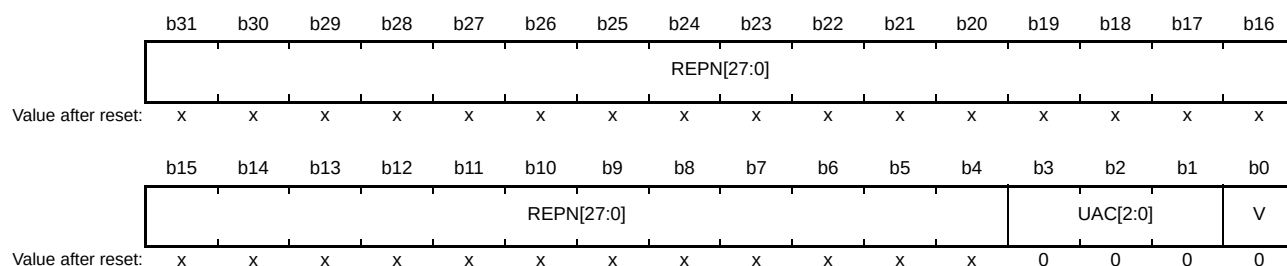
Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b31 to b4	RSPN[27:0]	Region-Start Page Number	Page number where the region starts, for use in region determination	R/W

RSPN[27:0] Bits (Region-Start Page Number)

These bits specify the page number where the region starts.

17.2.2 Region-n End Page Number Register (REPAGEn) (n = 0 to 7)

Address(es): REPAGE0 0008 6404h, REPAGE1 0008 640Ch, REPAGE2 0008 6414h, REPAGE3 0008 641Ch,
REPAGE4 0008 6424h, REPAGE5 0008 642Ch, REPAGE6 0008 6434h, REPAGE7 0008 643Ch



x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	V	Valid Bit	0: Region setting invalid 1: Region setting valid	R/W
b3 to b1	UAC[2:0]	Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R/W
b31 to b4	REPN[27:0]	Region-End Page Number	Page number where the region ends, for use in region determination	R/W

V Bit (Valid Bit)

This bit enables or disables the settings for the corresponding region.

This bit is cleared to 0 when the region invalidation operation register (MPOPI) invalidates all access-controlled areas.

UAC[2:0] Bits (Access Control Bits in User Mode)

These bits specify the access control in user mode.

REPN[27:0] Bits (Region-End Page Number)

These bits specify the page number where the region ends.

Specify a value that is greater than or equal to the page number where the corresponding region starts. The page specified by the region-end page number is part of the target region for memory protection.

17.2.3 Memory-Protection Enable Register (MPEN)

Address(es): 0008 6500h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MPEN	Memory-Protection Enable	1: The memory protection is enabled. 0: The memory protection is disabled.	R/W
b31 to b1	—	Reserved	The read value is 0. The write value should always be 0	R/W

MPEN Bit (Memory-Protection Enable)

This bit enables or disables the memory protection.

After 1 has been written to this bit, address checking for memory protection by the CPU starts on the execution of a branch instruction (RTE or RTFI) that shifts operation to the user mode.

17.2.4 Background Access Control Register (MPBAC)

Address(es): 0008 6504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UBAC[2:0]			—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b3 to b1	UBAC[2:0]	Background Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R/W
b31 to b4	—	Reserved	The read value is 0. The write value should always be 0.	R/W

UBAC[2:0] Bits (Background Access Control Bits in User Mode)

These bits specify the background access control in user mode.

17.2.5 Memory-Protection Error Status-Clearing Register (MPECLR)

Address(es): 0008 6508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CLR	Error Status-Clearing	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: The DMPER and IMPER bits in MPESTS are cleared to 0.	R/W
b31 to b1	—	Reserved	The read value is 0. The write value should always be 0.	R/W

CLR Bit (Error Status-Clearing)

This bit clears the data read/write bit (DRW), the data memory-protection error generation bit (DMPER), and the instruction memory-protection error generation bit (IMPER) in the memory-protection error status register (MPESTS) to 0.

17.2.6 Memory-Protection Error Status Register (MPESTS)

Address(es): 0008 650Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DRW	DMPER	IMPER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IMPER	Instruction Memory-Protection Error Generation	0: No instruction memory-protection error was generated. 1: Instruction memory-protection error was generated.	R
b1	DMPER	Data Memory-Protection Error Generation	0: No data memory-protection error was generated. 1: Data memory-protection error was generated.	R
b2	DRW	Data Read/Write	0: Data were read. 1: Data were written.	R
b31 to b3	—	Reserved	The read value is 0. The write value should always be 0.	R/W

IMPER Bit (Instruction Memory-Protection Error Generation)

This bit indicates the state of memory-protection error generation by instruction execution.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

DMPER Bit (Data Memory-Protection Error Generation)

This bit indicates the state of memory-protection error generation by operand access.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

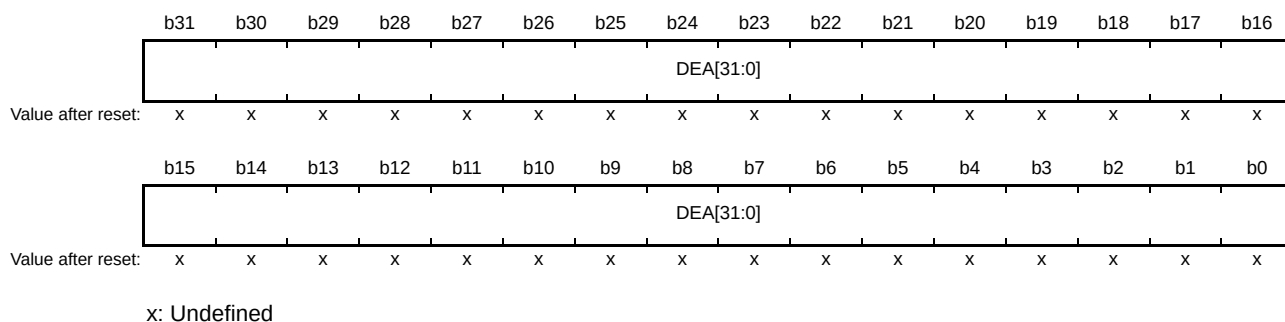
DRW Bit (Data Read/Write)

For a memory-protection error produced by operand access, this bit indicates the read/write attribute of the access operation. This bit is only valid when the DMPER bit is 1.

Setting the error status-clearing bit (CLR) in the memory-protection error status-clearing register (MPECLR) to 1 clears this bit to 0.

17.2.7 Data Memory-Protection Error Address Register (MPDEA)

Address(es): 0008 6514h



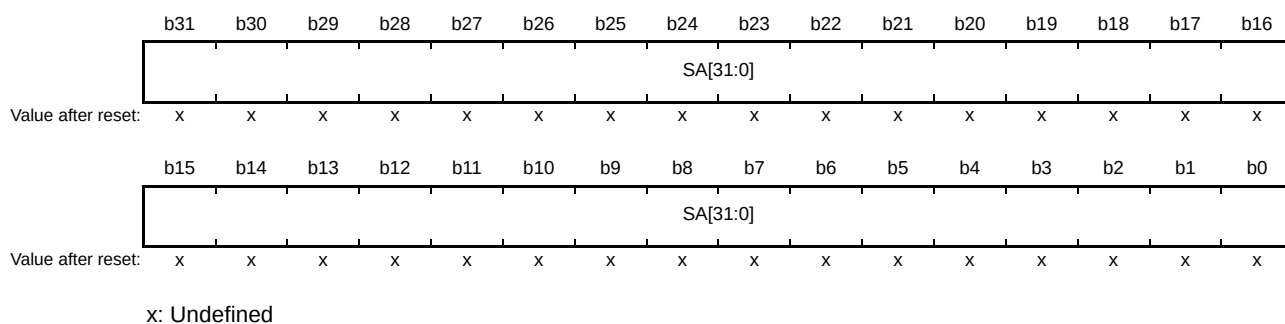
Bit	Symbol	Bit Name	Description	R/W
b31 to b0	DEA[31:0]	Data Memory-Protection Error Address	Data memory-protection error address	R

DEA[31:0] Bits (Data Memory-Protection Error Address)

These bits retain the address for which operand access generated a memory-protection error.

17.2.8 Region Search Address Register (MPSA)

Address(es): 0008 6520h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SA[31:0]	Region Search Address	Address for region searching	R/W

SA[31:0] Bits (Region Search Address)

These bits specify the address for use in comparison with region-start addresses in the region-n start page number registers (RSPAGEn) and region-end addresses in the region-n end page number registers (REPAGEn).

17.2.9 Region Search Operation Register (MPOPS)

Address(es): 0008 6524h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	S
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	S	Region Search Operation Activation	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: A region-search operation proceeds.	R/W
b15 to b1	—	Reserved	The read value is 0. The write value should always be 0.	R/W

S Bit (Region Search Operation Activation)

Setting this bit to 1 makes the memory-protection unit perform a region-search operation. The address specified in the region search address register (MPSA) is compared with the address information for individual regions to search for a hitting region.

The result of searching is stored in the data-hit region bits (HITD[7:0]) of the data-hit region register (MHITD).

Moreover, the logical OR of the respective access control bits for hitting regions is stored in the data-hit region access control bits (UHACD[2:0]) in user mode.

17.2.10 Region Invalidation Operation Register (MPOPI)

Address(es): 0008 6526h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	INV	Region Invalidate Start	[Reading] 0: Fixed value for reading [Writing] 0: Nothing is done. 1: All access-controlled areas are invalidated.	R/W
b15 to b1	—	Reserved	The read value is 0. The write value should always be 0.	R/W

INV Bit (Region Invalidate Start)

Setting this bit to 1 clears the valid (V) bits in all of the region-n end page number registers (REPAGEn) to 0. After a V bit is cleared to 0, all settings other than background access-control settings are invalid.

17.2.11 Instruction-Hit Region Register (MHITI)

Address(es): 0008 6528h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	HITI[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UHACI[2:0]			—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b3 to b1	UHACI[2:0]	Instruction-Hit Region Access Control Bits in User Mode	b3 0: Reading prohibited 1: Read permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution is permitted.	R
b15 to b4	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b23 to b16	HITI[7:0]	Instruction-Hit Region	When the instruction memory-protection error generation bit (MPESTS.IMPER) = 1, [b23:b16] = 0000 0000b indicates that attempted access to the background region led to an instruction memory-protection error. Other than above b23 0: Instruction memory-protection error was not generated in region 7. 1: Instruction memory-protection error was generated in region 7. b22 0: Instruction memory-protection error was not generated in region 6. 1: Instruction memory-protection error was generated in region 6. b21 0: Instruction memory-protection error was not generated in region 5. 1: Instruction memory-protection error was generated in region 5. b20 0: Instruction memory-protection error was not generated in region 4. 1: Instruction memory-protection error was generated in region 4. b19 0: Instruction memory-protection error was not generated in region 3. 1: Instruction memory-protection error was generated in region 3. b18 0: Instruction memory-protection error was not generated in region 2. 1: Instruction memory-protection error was generated in region 2. b17 0: Instruction memory-protection error was not generated in region 1. 1: Instruction memory-protection error was generated in region 1. b16 0: Instruction memory-protection error was not generated in region 0. 1: Instruction memory-protection error was generated in region 0.	R
b31 to b24	—	Reserved	The read value is 0. The write value should always be 0.	R/W

UHACI[2:0] Bits (Instruction-Hit Region Access Control Bits in User Mode)

These bits hold the user-mode access control bits (REPAGEn.UAC[2:0]) for the region where the instruction memory-protection error was generated.

If the error was generated in an overlap between regions, the value stored here is the logical OR of the user-mode access control bits for the corresponding regions (including the background region).

HITI[7:0] Bits (Instruction-Hit Region)

These bits indicate the region where an instruction memory-protection error was generated. These bits are set to 0000 0000b in response to the generation of an instruction memory-protection error in the background region.

17.2.12 Data-Hit Region Register (MHITD)

Address(es): 0008 652Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	HITD[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UHACD[2:0]			—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b3 to b1	UHACD[2:0]	Data-Hit Region Access Control Bits in User Mode	b3 0: Reading prohibited 1: Reading permitted b2 0: Writing prohibited 1: Writing permitted b1 0: Execution prohibited 1: Execution permitted	R
b15 to b4	—	Reserved	The read value is 0. The write value should always be 0.	R/W
b23 to b16	HITD[7:0]	Data-Hit Region	When the data memory-protection error generation bit (MPESTS.DMPER) = 1, [b23:b16] = 0000 0000b indicates that attempted access to the background region led to a data memory-protection error. Other than above b23 0: Neither a data memory-protection error nor a search hit was generated in region 7. 1: A data memory-protection error or search hit was generated in region 7. b22 0: Neither a data memory-protection error nor a search hit was generated in region 6. 1: A data memory-protection error or search hit was generated in region 6. b21 0: Neither a data memory-protection error nor a search hit was generated in region 5. 1: A data memory-protection error or search hit was generated in region 5. b20 0: Neither a data memory-protection error nor a search hit was generated in region 4. 1: A data memory-protection error or search hit was generated in region 4. b19 0: Neither a data memory-protection error nor a search hit was generated in region 3. 1: A data memory-protection error or search hit was generated in region 3. b18 0: Neither a data memory-protection error nor a search hit was generated in region 2. 1: A data memory-protection error or search hit was generated in region 2. b17 0: Neither a data memory-protection error nor a search hit was generated in region 1. 1: A data memory-protection error or search hit was generated in region 1. b16 0: Neither a data memory-protection error nor a search hit was generated in region 0. 1: A data memory-protection error or search hit was generated in region 0.	R
b31 to b24	—	Reserved	The read value is 0. The write value should always be 0.	R/W

UHACD[2:0] Bits (Data-Hit Region Access Control Bits in User Mode)

These bits hold the user-mode access control bits (REPAGEn.UAC[2:0]) that have been set for the region where a data memory-protection error was generated or the region that produced a hit in region searching.

When an error is generated in an overlap between regions or a hit was generated in region searching, the value stored here is the logical OR of the user-mode access control bits for the corresponding regions (including the background region).

HITD[7:0] Bits (Data-Hit Region)

These bits indicate the region where a data memory-protection error was generated or the region that produced a hit in a region search. These bits are set to 0000 0000b for a data memory-protection error generated in the background region.

Note: When access to a register of memory protection unit in user mode generates a data memory-protection error, the value in this register is cleared to 0000 0000h.

17.3 Functions

17.3.1 Memory Protection

Memory protection means monitoring, in accord with the access-control information that has been set for the individual access-control regions and the background region, whether or not access by programs running in user mode violates the access-control settings. The memory-protection unit notifies the CPU of access-control violations (or memory-protection errors) when they are detected, causing the CPU to start access-exception processing.

Memory protection is enabled by setting the memory-protection enable (MPEN) bit in the memory-protection enable (MPEN) register to 1.

An instruction memory-protection error is generated on detection of an instruction-execution violation and a data memory-protection error is generated on detection of an operand-access reading or writing violation. Operand access that leads to a data memory-protection error is not actually executed.

17.3.2 Region Search

Region search means enquiry as to which of the eight specified access regions was “hit” and how the access-control information (permission to execute, to read, and to write) is set.

When the region search operation (S) bit in the region-search operation (MPOP) register is set to 1, the address specified in the region search address (MPSA) register is compared with the addresses for the individual regions. After a region search is executed, the data-hit region register (MHITD) indicates the logical OR of the access-control information for the region which was “hit” and for the other regions.

17.3.3 Protection of Registers Related to the Memory-Protection Unit

Registers related to the memory-protection unit are not accessible through means of access other than operand access by the CPU (i.e. by instruction fetching or DMA). Attempted access to registers related to the memory-protection unit in user mode through operand access by the CPU leads to a data memory-protection error regardless of whether or not memory protection is in effect at the given location.

17.3.4 Flow for Determination of Access by the Memory-Protection Function

Figure 17.2 shows the flow of determination in the case of data access and Figure 17.3 shows the flow of determination in the case of instruction access.

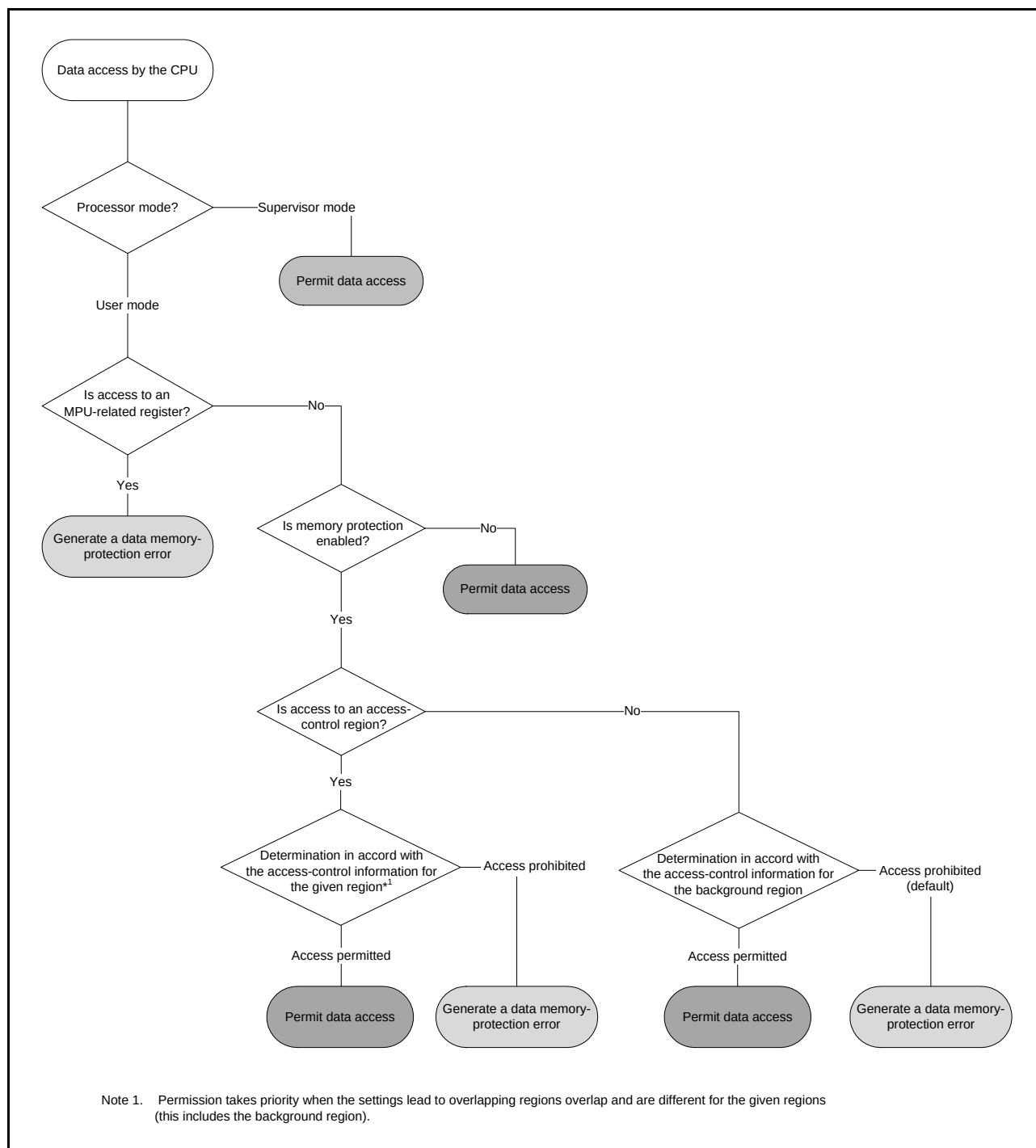


Figure 17.2 Flow of Determination for Data Access

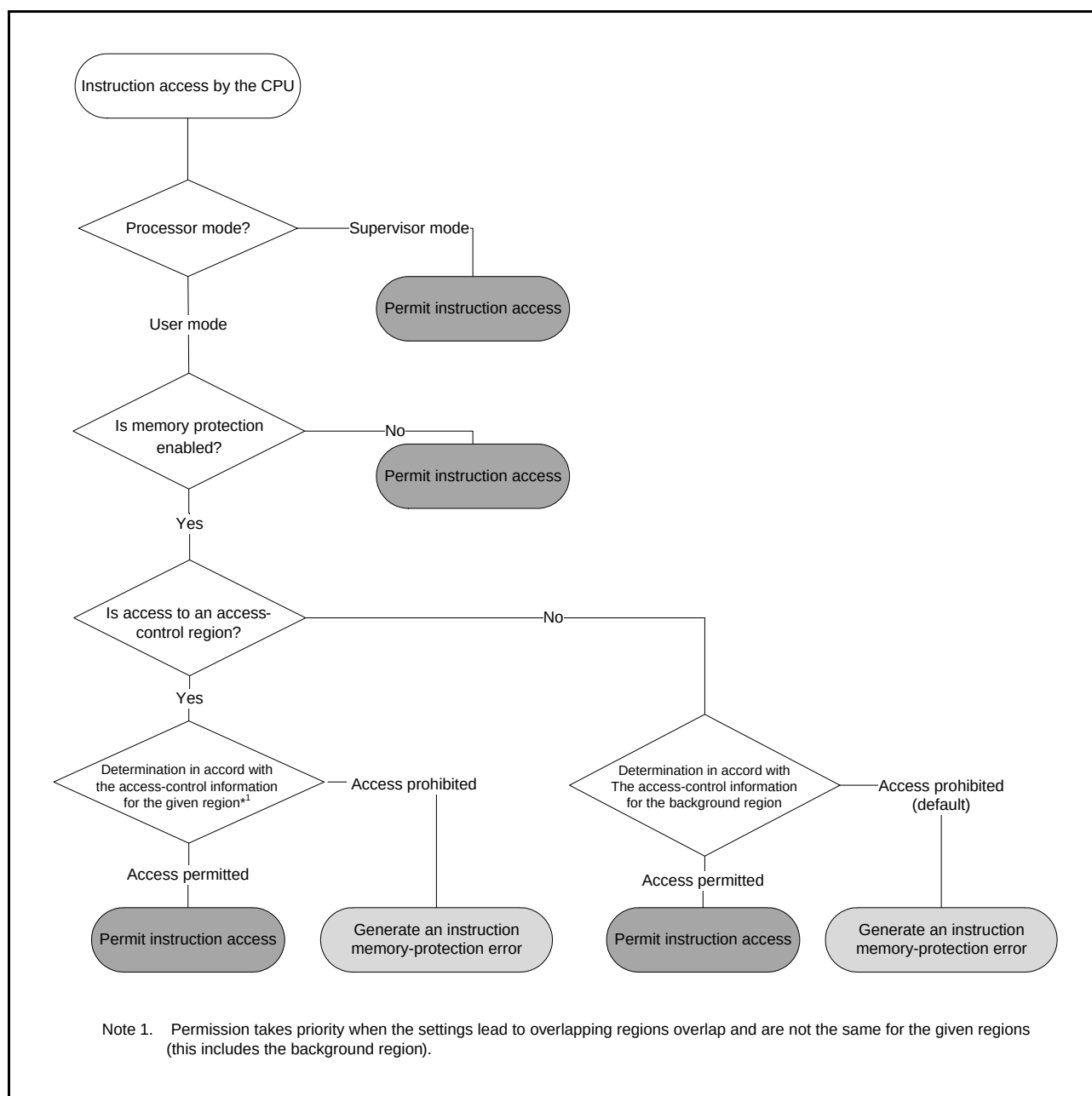


Figure 17.3 Flow of Determination for Instruction Access

17.4 Procedures for Using Memory Protection

17.4.1 Setting Access-Control Information

Access-control information for the various regions is set in supervisor mode.

Settings for up to eight access-control regions are made in the region-n start page number registers (RSPAGEn) and region-n end page number registers (REPAGEn), where n = 0 to 7.

Settings for the background access-control region are made in the background access-control register (MPBAC).

17.4.2 Enabling Memory Protection

Setting the memory-protection enable (MPEN) bit in the memory-protection enable (MPEN) register to 1 while operation is in supervisor mode enables memory protection.

17.4.3 Transition to User Mode

After updating the registers related to the memory-protection unit, read any of these registers and check that the settings have been made before the transition to user mode.

Either of the methods below can be used for the transition from supervisor mode to user mode.

- Set the processor mode setting (PM) bit in the copy of the processor status word (PSW) saved in the stack area to 1 (the setting for user mode) and then execute an RTE instruction.
- Set the PM bit in the backup processor status word (BPSW) to 1 and then execute an RTFI instruction.

Note: Using an MVTC or POPC instruction to write to the PSW.PM bit is invalid. Use an RTE or RTFI instruction to update the value of the PSW.PM bit.

The memory-protection unit starts checking instruction-execution access and operand access by the CPU on the transition to user mode.

17.4.4 Processing in Response to Memory-Protection Errors

The CPU starts access-exception processing on detection of a violation of protection set up by the access-control information (i.e. a memory-protection error). For details on CPU operations in access-exception processing, refer to section 14, Exception Handling.

To determine whether an instruction memory-protection error or data memory-protection error has been generated, check the values of the instruction memory-protection error generation (IMPER) and data memory-protection error generation (DMPER) bits in the memory-protection error status register (MPESTS) from within the exception-processing routine. After confirming the type of error, clear the memory-protection error status register (MPESTS) by writing 1 to the status clearing (MPE) bit in the memory-protection error status clearing register (MPECLR).

(1) When a data memory-protection error is generated

Access-exception processing by the CPU saves the address of the instruction that led to the memory-protection error on the stack. Furthermore, the address of the operand for which access led to a memory-protection error is stored in the data memory-protection error address register (MPDEA) and the region information for the region where the memory-protection error was generated is stored in the data-hit region register (MHITD).

- Violations of access control in access to valid regions 0 to 7

The data-hit region bits (MHITD.HITD[7:0]) with the same region number as the region where the error occurred is set to 1. In user mode, the logical “or” of the region access-control information for the location where the error occurred is set in the data-hit region access-control bits (MHITD.UHACD[2:0]).

- Violations of access control for the background region, besides access to outside valid regions 0 to 7

The data-hit region bits (MHITD.HITD[7:0]) are set to 0000 0000b. In user mode, the access-control information for the background region is set in the data-hit region access-control bits (MHITD.UHACD[2:0]).

Referring to this information can pinpoint the sources of errors.

(2) When an instruction memory-protection error is generated

Access-exception processing by the CPU saves the address of the instruction that led to the memory-protection error on the stack. Furthermore, the region information for the region where the memory-protection error was generated is stored in the instruction-hit region register (MHITI).

- Violations of access control in access to valid regions 0 to 7

The instruction-hit region bit (MHITI.HITI[7:0]) with the same region number as the region where the error occurred is set to 1. In user mode, the logical “or” of the region access-control information for the location where the error occurred is set in the instruction-hit region access-control bits (MHITI.UHACI[2:0]).

- Violations of access control for the background region, besides access to outside valid regions 0 to 7

The instruction-hit region bits (MHITI.HITI[7:0]) are set to 0000 0000b. In user mode, the access-control information for the background region is set in the instruction-hit region access-control bits (MHITI.UHACI[2:0]).

Referring to this information can pinpoint the sources of errors.

18. DMA Controller (DMACA)

This MCU incorporates a 4-channel direct memory access controller (DMAC).

The DMAC module performs data transfers without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

18.1 Overview

Table 18.1 lists the specifications of the DMAC, and Figure 18.1 shows a block diagram of the DMAC.

Table 18.1 Specifications of DMAC

Item		Description
Number of channels		4 (DMACm (m = 0 to 3))
Transfer space		512 Mbytes (0000 0000h to 0FFF FFFFh and F000 0000h to FFFF FFFFh excluding reserved areas)
Maximum transfer volume		1M data (Maximum number of transfers in block transfer mode: 1,024 data × 1,024 blocks)
DMA request source		- Activation source selectable for each channel - Software trigger - Interrupt requests from peripheral modules or trigger input to external interrupt input pins*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0: Highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	- One data transfer by one DMA transfer request - Free running mode (setting in which total number of data transfers is not specified) settable
	Repeat transfer mode	- One data transfer by one DMA transfer request - Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. - Maximum settable repeat size: 1,024
	Block transfer mode	- One block data transfer by one DMA transfer request - Maximum settable block size: 1,024 data
Selective functions	Extended repeat area function	- Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed - Area of 2 bytes to 128 Mbytes separately settable as extended repeat area for transfer source and destination
Interrupt request	Transfer end interrupt	Generated on completion of transferring data volume specified by the transfer counter.
	Transfer escape end interrupt	Generated when the repeat size of data transfer is completed or the extended repeat area overflows.
Power consumption reduction function		Module stop state can be set.
Event link function		Event link request is generated after one data transfer (for block, after one block transfer).

Note 1. For details on DMAC activation sources, see Table 15.3, Interrupt Vector Table in section 15, Interrupt Controller (ICUb).

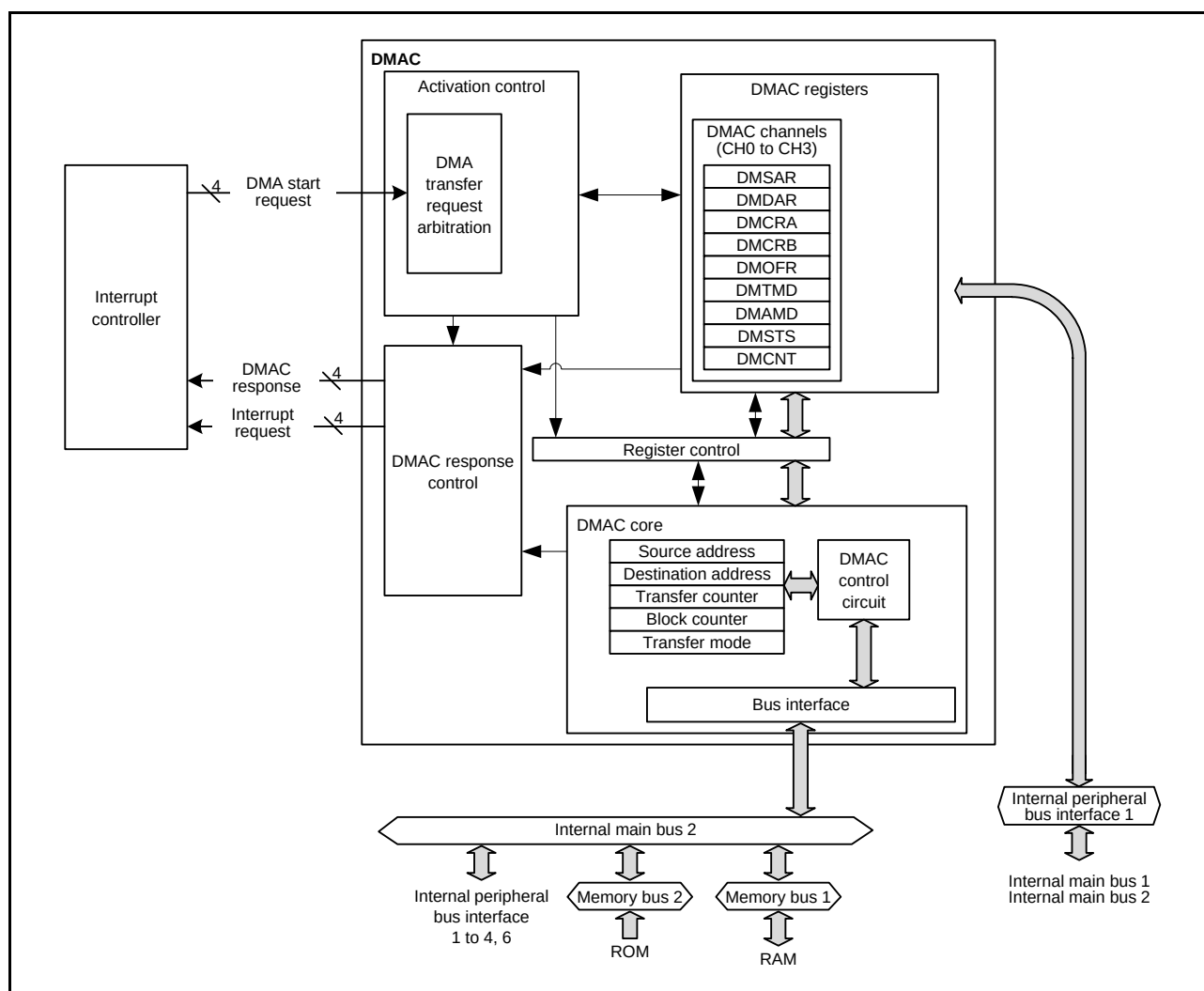
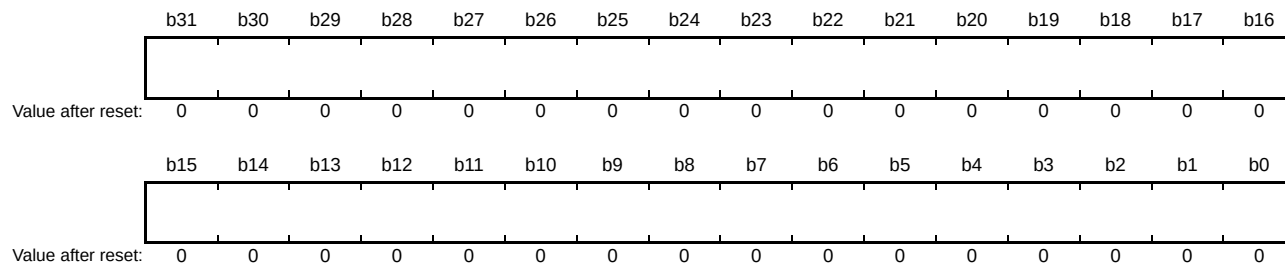


Figure 18.1 Block Diagram of DMAC

18.2 Register Descriptions

18.2.1 DMA Source Address Register (DMSAR)

Address(es): DMAC0.DMSAR 0008 2000h, DMAC1.DMSAR 0008 2040h, DMAC2.DMSAR 0008 2080h, DMAC3.DMSAR 0008 20C0h



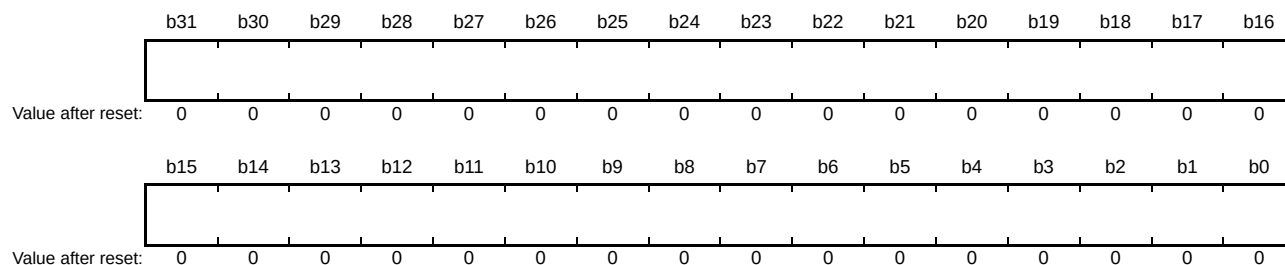
Bit	Description	Setting Range	R/W
b31 to b0	Specifies the transfer source start address.	0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	R/W

Set DMSAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Setting bits 31 to 29 is invalid; a value of bit 28 is extended to bits 31 to 29. Reading DMSAR returns the extended value.

18.2.2 DMA Destination Address Register (DMDAR)

Address(es): DMAC0.DMDAR 0008 2004h, DMAC1.DMDAR 0008 2044h, DMAC2.DMDAR 0008 2084h, DMAC3.DMDAR 0008 20C4h



Bit	Description	Setting Range	R/W
b31 to b0	Specifies the transfer destination start address.	0000 0000h to 0FFF FFFFh (256 Mbytes) F000 0000h to FFFF FFFFh (256 Mbytes)	R/W

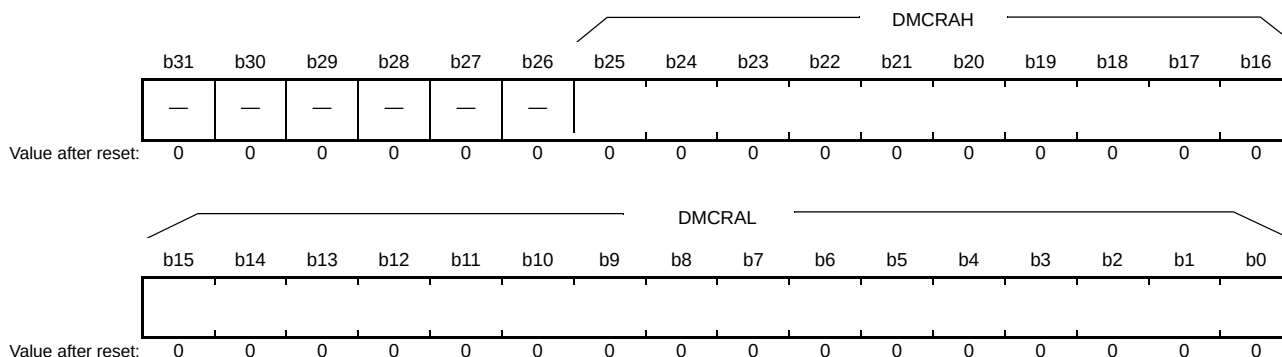
DMDAR specifies the start address of the transfer destination. Set DMDAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Setting bits 31 to 29 is invalid; a value of bit 28 is extended to bits 31 to 29. Reading DMDAR returns the extended value.

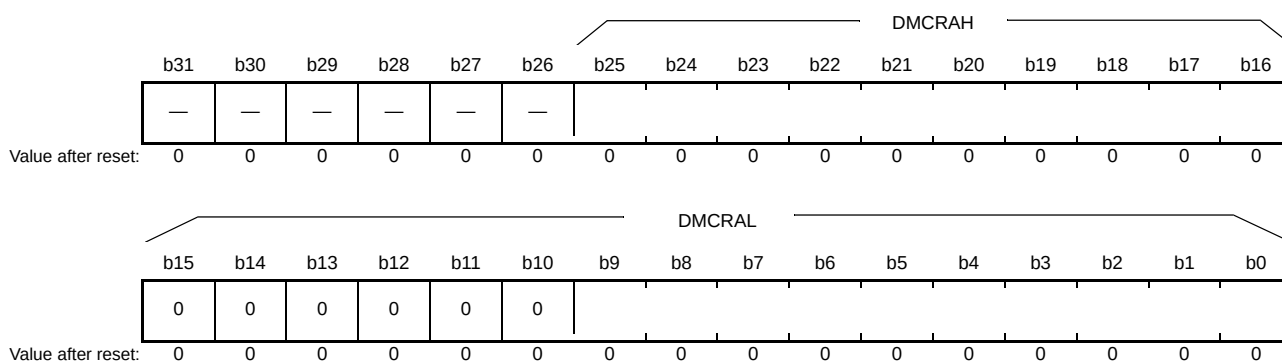
18.2.3 DMA Transfer Count Register (DMCRA)

Address(es): DMAC0.DMCRA 0008 2008h, DMAC1.DMCRA 0008 2048h, DMAC2.DMCRA 0008 2088h, DMAC3.DMCRA 0008 20C8h

- Normal transfer mode



- Repeat transfer mode, block transfer mode



Symbol	Bit Name	Description	R/W
DMCRAL	Lower bits of transfer count	Specifies the number of transfer operations	R/W
DMCRAH	Upper bits of transfer count		R/W

Note: Set the same value for DMCRAH and DMCRAL in repeat transfer mode and block transfer mode.

(1) Normal Transfer Mode (MD[1:0] Bits in DMACm.DMTMD = 00b)

DMCRAL functions as a 16-bit transfer counter.

The number of transfer operations is one when the setting is 0001h, and 65535 when it is FFFFh. The value is decremented by one each time data is transferred.

When the setting is 0000h, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running mode).

DMCRAH is not used in normal transfer mode. Write 0000h to DMCRAH.

(2) Repeat Transfer Mode (MD[1:0] Bits in DMACm.DMTMD = 01b)

DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter.

The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In repeat transfer mode, a value in the range of 000h to 3FFh (1 to 1024) can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which the value in DMCRAH is loaded into DMCRAL.

(3) Block Transfer Mode (MD[1:0] Bits in DMACm.DMTMD = 10b)

DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter.

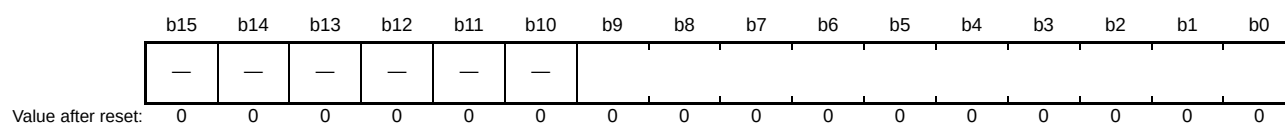
The block size is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h. In block transfer mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits.

The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which the value in DMCRAH is loaded into DMCRAL.

18.2.4 DMA Block Transfer Count Register (DMCRB)

Address(es): DMAC0.DMCRB 0008 200Ch, DMAC1.DMCRB 0008 204Ch, DMAC2.DMCRB 0008 208Ch, DMAC3.DMCRB 0008 20CCh



Bit	Description	Setting Range	R/W
b9 to b0	Specifies the number of block transfer operations or repeat transfer operations.	001h to 3FFh (1 to 1023) 000h (1024)	R/W
b15 to b10	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMCRB specifies the number of block transfer operations and repeat transfer operations in block and repeat transfer mode, respectively.

The number of transfer operations is one when the setting is 001h, 1023 when it is 3FFh, and 1024 when it is 000h.

In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred.

In block transfer mode, the value is decremented by one when the final data of one block size is transferred.

In normal transfer mode, DMCRB is not used. The setting is invalid.

18.2.5 DMA Transfer Mode Register (DMTMD)

Address(es): DMAC0.DMTMD 0008 2010h, DMAC1.DMTMD 0008 2050h, DMAC2.DMTMD 0008 2090h, DMAC3.DMTMD 0008 20D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DCTG[1:0]	DMA Request Source Select	b1 b0 0 0: Software 0 1: Interrupts*1 from peripheral modules or external interrupt input pins 1 0: Setting prohibited 1 1: Setting prohibited	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SZ[1:0]	Transfer Data Size Select	b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	DTS[1:0]	Repeat Area Select	b13 b12 0 0: The destination is specified as the repeat area or block area. 0 1: The source is specified as the repeat area or block area. 1 0: The repeat area or block area is not specified. 1 1: Setting prohibited	R/W
b15, b14	MD[1:0]	Transfer Mode Select	b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Setting prohibited	R/W

Note 1. DMAC activation source is selected using the DMRSRm registers of the ICU. For details on DMAC activation sources, see Table 15.3, Interrupt Vector Table in section 15, Interrupt Controller (ICUb).

DTS[1:0] Bits (Repeat Area Select)

DTS[1:0] select either the source or destination as the repeat area in repeat or block transfer mode. In normal transfer mode, setting these bits is invalid.

18.2.6 DMA Interrupt Setting Register (DMINT)

Address(es): DMAC0.DMINT 0008 2013h, DMAC1.DMINT 0008 2053h, DMAC2.DMINT 0008 2093h, DMAC3.DMINT 0008 20D3h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable	0: Disables an interrupt request for an extended repeat area overflow on the destination address 1: Enables an interrupt request for an extended repeat area overflow on the destination address	R/W
b1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable	0: Disables an interrupt request for an extended repeat area overflow on the source address 1: Enables an interrupt request for an extended repeat area overflow on the source address	R/W
b2	RPTIE	Repeat Size End Interrupt Enable	0: Disables the repeat size end interrupt request. 1: Enables the repeat size end interrupt request.	R/W
b3	ESIE	Transfer Escape End Interrupt Enable	0: Disables the transfer escape end interrupt request. 1: Enables the transfer escape end interrupt request.	R/W
b4	DTIE	Transfer End Interrupt Enable	0: Disables the transfer end interrupt request. 1: Enables the transfer end interrupt request.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DARIE Bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the destination address occurs while this bit is set to 1, the DTE bit in DMCNT is cleared to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that an interrupt by an extended repeat area overflow on the destination address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DTE bit in DMACm.DMCNT of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the destination address, this bit is ignored.

SARIE Bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow on the source address occurs while this bit is set to 1, the DTE bit in DMCNT is cleared to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that an interrupt by an extended repeat area overflow on the source address is requested.

When block transfer mode is used with the extended repeat area function, an interrupt is requested after completion of a 1-block size transfer. When setting 1 in the DTE bit in DMACm.DMCNT of the channel for which a transfer has been stopped, the transfer is resumed from the state when the transfer is stopped.

When the extended repeat area is not specified for the source address, this bit is ignored.

RPTIE Bit (Repeat Size End Interrupt Enable)

When this bit is set to 1 in repeat transfer mode, the DTE bit in DMCNT is cleared to 0 after completion of a 1-repeat size data transfer. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (= repeat area or block area is not specified).

When this bit is set to 1 in block transfer mode, the DTE bit in DMCNT is cleared to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request has been generated. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (= repeat area or block area is not specified).

ESIE Bit (Transfer Escape End Interrupt Enable)

This bit enables or disables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that are generated during DMA transfer.

The transfer escape end interrupt is generated when the ESIF flag in DMSTS is set to 1 with this bit set to 1. The transfer escape end interrupt is cleared by clearing this bit or the ESIF flag in DMSTS to 0.

DTIE Bit (Transfer End Interrupt Enable)

This bit enables or disables the transfer end interrupt request to be generated on completion of a specified number of data transfers.

The transfer end interrupt is generated when the DTIF bit in DMSTS is set to 1 with this bit set to 1. The transfer end interrupt is cleared by clearing this bit or the DTIF bit in DMSTS to 0.

18.2.7 DMA Address Mode Register (DMAMD)

Address(es): DMAC0.DMAMD 0008 2014h, DMAC1.DMAMD 0008 2054h, DMAC2.DMAMD 0008 2094h, DMAC3.DMAMD 0008 20D4h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	DARA[4:0]	Destination Address Extended Repeat Area	Specifies the extended repeat area on the destination address. For details on the settings, see Table 18.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	DM[1:0]	Destination Address Update Mode	b7 b6 0 0: Destination address is fixed. 0 1: Offset addition*1 1 0: Destination address is incremented. 1 1: Destination address is decremented.	R/W
b12 to b8	SARA[4:0]	Source Address Extended Repeat Area	Specifies the extended repeat area on the source address. For details on the settings, see Table 18.2.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15, b14	SM[1:0]	Source Address Update Mode	b15 b14 0 0: Source address is fixed. 0 1: Offset addition*1 1 0: Source address is incremented. 1 1: Source address is decremented.	R/W

Note 1. Offset addition can be specified only for DMAC0.

DARA[4:0] Bits (Destination Address Extended Repeat Area)

These bits specify the extended repeat area on the destination address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 Mbytes.

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer destination, do not specify the extended repeat area on the destination address. When repeat transfer or block transfer is selected, or when DMACm.DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat area or block area), write 00000b in the DARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the DARIE bit in DMINT set to 1. Table 18.2 lists the settings and the corresponding extended repeat areas.

DM[1:0] Bits (Destination Address Update Mode)

These bits select the mode of updating the destination address.

When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is decremented by 1, 2, and 4, respectively.

When offset addition is selected, the offset specified by the DMAC0.DMOFR register is added to the address.

Offset addition can be specified only for DMAC0.

SARA[4:0] Bits (Source Address Extended Repeat Area)

These bits specify the extended repeat area on the source address. The extended repeat area function is realized by updating the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 21 (2 bytes) and 217 (128 Mbytes).

When the lower address overflows the extended repeat area by address increment, the start address of the extended repeat area is set. Similarly, when the lower address underflows the extended repeat area by address decrement, the end address of the extended repeat area is set.

When the repeat area or block area is specified as a transfer source, do not specify the extended repeat area on the source address. When repeat transfer or block transfer is selected, or when DMACm.DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat area or block area), write 00000b in the SARA[4:0] bits.

An interrupt can be requested when an overflow or underflow occurs in the extended repeat area with the SARIE bit in DMINT set to 1. Table 18.2 lists the settings and the corresponding extended repeat areas.

SM[1:0] Bit (Source Address Update Mode)

These bits select the mode of updating the source address.

When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively.

When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively.

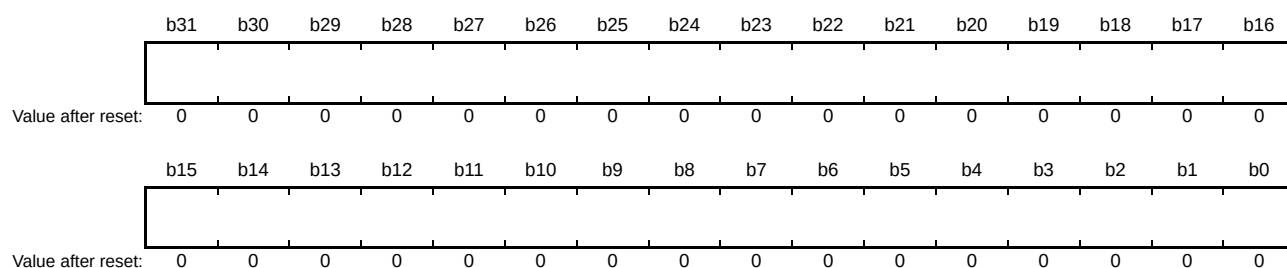
When offset addition is selected, the offset specified by the DMAC0.DMOFR register is added to the address. Offset addition can be specified only for DMAC0.

Table 18.2 SARA[4:0] or DARA[4:0] Settings and Corresponding Repeat Areas

SARA4 to SARA0 or DARA4 to DARA0	Extended Repeat Area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 Kbyte specified as extended repeat area by the lower 10 bits of the address
01011b	2 Kbytes specified as extended repeat area by the lower 11 bits of the address
01100b	4 Kbytes specified as extended repeat area by the lower 12 bits of the address
01101b	8 Kbytes specified as extended repeat area by the lower 13 bits of the address
01110b	16 Kbytes specified as extended repeat area by the lower 14 bits of the address
01111b	32 Kbytes specified as extended repeat area by the lower 15 bits of the address
10000b	64 Kbytes specified as extended repeat area by the lower 16 bits of the address
10001b	128 Kbytes specified as extended repeat area by the lower 17 bits of the address
10010b	256 Kbytes specified as extended repeat area by the lower 18 bits of the address
10011b	512 Kbytes specified as extended repeat area by the lower 19 bits of the address
10100b	1 Mbyte specified as extended repeat area by the lower 20 bits of the address
10101b	2 Mbytes specified as extended repeat area by the lower 21 bits of the address
10110b	4 Mbytes specified as extended repeat area by the lower 22 bits of the address
10111b	8 Mbytes specified as extended repeat area by the lower 23 bits of the address
11000b	16 Mbytes specified as extended repeat area by the lower 24 bits of the address
11001b	32 Mbytes specified as extended repeat area by the lower 25 bits of the address
11010b	64 Mbytes specified as extended repeat area by the lower 26 bits of the address
11011b	128 Mbytes specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited.

18.2.8 DMA Offset Register (DMOFR)

Address(es): DMAC0.DMOFR 0008 2018h



Bit	Description	Setting Range	R/W
b31 to b0	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination.	0000 0000h to 00FF FFFFh (0 bytes to (16 M – 1) bytes) FF00 0000h to FFFF FFFFh (–16 Mbytes to –1 byte)	R/W

Write to this register while the DMAC operation is stopped or DMA transfer is disabled (not during data transfer).
Setting bits 31 to 25 is invalid; a value of bit 24 is extended to bits 31 to 25. Reading DMOFR returns the extended value.

18.2.9 DMA Transfer Enable Register (DMCNT)

Address(es): DMAC0.DMCNT 0008 201Ch, DMAC1.DMCNT 0008 205Ch, DMAC2.DMCNT 0008 209Ch, DMAC3.DMCNT 0008 20DCh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DTE
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	DTE	DMA Transfer Enable	0: Disables DMA transfer. 1: Enables DMA transfer.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTE Bit (DMA Transfer Enable)

When the DMST bit in DMAST is set to 1 (DMAC activation is enabled) and this bit is set to 1 (DMA transfer is enabled), DMA transfer can be started for the corresponding channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit.
- When the specified total volume of data transfer is completed.
- When DMA transfer is stopped by the repeat size end interrupt.
- When DMA transfer is stopped by the extended repeat area overflow interrupt.

18.2.10 DMA Software Start Register (DMREQ)

Address(es): DMAC0.DMREQ 0008 201Dh, DMAC1.DMREQ 0008 205Dh, DMAC2.DMREQ 0008 209Dh, DMAC3.DMREQ 0008 20DDh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	CLRS	—	—	—	SWREQ
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	SWREQ	DMA Software Start	0: DMA transfer is not requested. 1: DMA transfer is requested.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CLRS	DMA Software Start Bit Auto Clear Select	0: SWREQ bit is cleared after DMA transfer is started by software. 1: SWREQ bit is not cleared after DMA transfer is started by software.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SWREQ Bit (DMA Software Start)

When 1 is written to this bit, a DMA transfer request is generated. After DMA transfer is started in response to the request, this bit is cleared to 0 if the CLRS bit is set to 0. This bit is not cleared to 0 while the CLRS bit is set to 1. In this case, a DMA transfer request can be issued again after completion of a transfer.

Note that, however, setting this bit is valid and DMA transfer by software is enabled only when the DCTG[1:0] bits in DMTMD are set to 00b (DMA activation source is software).

Setting this bit is invalid when the DCTG[1:0] bits in DMTMD are set to a value other than 00b.

To start DMA transfer by software with the CLRS bit being 0, ensure that the SWREQ bit is 0, and then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started while the CLRS bit is set to 0 (the SWREQ bit is cleared after DMA transfer is started by software).
- When 0 is written to this bit.

CLRS Bit (DMA Software Start Bit Auto Clear Select)

This bit specifies whether to clear the SWREQ bit to 0 after DMA transfer is started in response to the DMA transfer request generated by setting the SWREQ bit to 1. With this bit set to 0, the SWREQ bit is cleared to 0 after DMA transfer is started. With this bit set to 1, the SWREQ bit is not cleared to 0. In this case, a DMA transfer request can be issued again after completion of a transfer.

18.2.11 DMA Status Register (DMSTS)

Address(es): DMAC0.DMSTS 0008 201Eh, DMAC1.DMSTS 0008 205Eh, DMAC2.DMSTS 0008 209Eh, DMAC3.DMSTS 0008 20DEh

b7	b6	b5	b4	b3	b2	b1	b0
ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ESIF	Transfer Escape End Interrupt Flag	0: A transfer escape end interrupt has not been generated. 1: A transfer escape end interrupt has been generated.	R/W*1
b3 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b4	DTIF	Transfer End Interrupt Flag	0: A transfer end interrupt has not been generated. 1: A transfer end interrupt has been generated.	R/W*1
b6, b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	ACT	DMA Active Flag	0: DMAC operation is suspended. 1: DMAC is operating.	R

Note 1. Only 0 can be written to clear the flag.

ESIF Flag (Transfer Escape End Interrupt Flag)

This flag indicates that the transfer escape end interrupt has been generated.

[Setting conditions]

- When 1-repeat size data transfer is completed in repeat transfer mode with the RPTIE bit in DMINT set to 1.
- When 1-block data transfer is completed in block transfer mode with the RPTIE bit in DMINT set to 1.
- When an extended repeat area overflow on the source address occurs while the SARIE bit in DMINT is set to 1 and the SARA[4:0] bits in DMAMD are set to a value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs while the DARIE bit in DMINT is set to 1 and the DARA[4:0] bits in DMAMD are set to a value other than 00000b (extended repeat area is specified on the transfer destination address)

[Clearing conditions]

- When 0 is written to this bit.
- When 1 is written to the DTE bit in DMCNT.

DTIF Flag (Transfer End Interrupt Flag)

This flag indicates that the transfer end interrupt has been generated.

[Setting conditions]

- When the specified number of unit-transfers are completed in normal transfer mode (the value of DMCRAL becoming 0 on completion of transfer)
- When the specified number of repeat transfer operations are completed in repeat transfer mode (the value of DMCRB becoming 0 on completion of transfer))
- When the specified number of blocks have been transferred in block transfer mode (the value of DMCRB becoming 0 on completion of transfer)

[Clearing conditions]

- When 0 is written to this bit
- When 1 is written to the DTE bit in DMCNT

ACT Flag (DMA Active Flag)

This flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts data transfer operation

[Clearing condition]

- When data transfer in response to one transfer request is completed

18.2.12 DMA Activation Source Flag Control Register (DMCSL)

Address(es): DMAC0.DMCSL 0008 201Fh, DMAC1.DMCSL 0008 205Fh, DMAC2.DMCSL 0008 209Fh, DMAC3.DMCSL 0008 20DFh

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DISEL
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	DISEL	Interrupt Select	0: At the beginning of transfer, clear the interrupt flag of the activation source to 0. 1: At the end of transfer, the interrupt flag of the activation source issues an interrupt to the CPU.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DISEL Bit (Interrupt Select)

This bit selects whether the interrupt flag of the activation source of the DMAC is cleared to 0 or issues an interrupt to the CPU, at the beginning of transfer.

When DMTMD.DCTG[1:0] = 00b (activation by software), the setting of the DISEL bit does not affect the operation.

18.2.13 DMA Module Activation Register (DMAST)

Address(es): 0008 2200h

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DMST
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	DMST	DMAC Operation Enable	0: DMAC activation is disabled. 1: DMAC activation is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMST Bit (DMAC Operation Enable)

When this bit is set to 1, DMAC activation is enabled for all channels.

When 1 is written to the DMACm.DMCNT.DTE bit (DMA transfer is enabled) of multiple channels and then this bit is set to 1 (DMAC activation is enabled), the corresponding multiple channels can be placed in the transfer request acceptable state at the same time.

When the DMST bit is cleared to 0 during DMA transfer, DMA transfer is suspended after completion of the current data transfer corresponding to a single transfer request. DMA transfer is resumed by setting the DMST bit to 1 again.

[Setting condition]

- When 1 is written to this bit

[Clearing condition]

- When 0 is written to this bit

18.3 Operation

18.3.1 Transfer Mode

(1) Normal Transfer Mode

In normal transfer mode, one data is transferred by one transfer request. A maximum of 65535 can be set as the number of transfer operations using the DMCRAL of DMACm. When these bits are set to 0000h, no specific number of transfer operations is set; data transfer is performed with the transfer counter stopped (free running mode). Setting DMCRB of DMACm is invalid in normal transfer mode. Except in free running mode, a transfer end interrupt request can be generated after completion of the specified number of transfer operations.

Table 18.3 summarizes the register update operation in normal transfer mode, and Figure 18.2 shows the operation in normal transfer mode.

Table 18.3 Register Update Operation in Normal Transfer Mode

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request
DMACm.DMSAR	Transfer source address	Increment/decrement/fixed/offset addition*1
DMACm.DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition*1
DMACm.DMCRAL	Transfer count	Decrement by one/not updated (in free running mode)
DMACm.DMCRAH	—	Not updated (Not used in normal transfer mode)
DMACm.DMCRB	—	Not updated (Not used in normal transfer mode)

Note 1. Offset addition can be specified only for DMAC0.

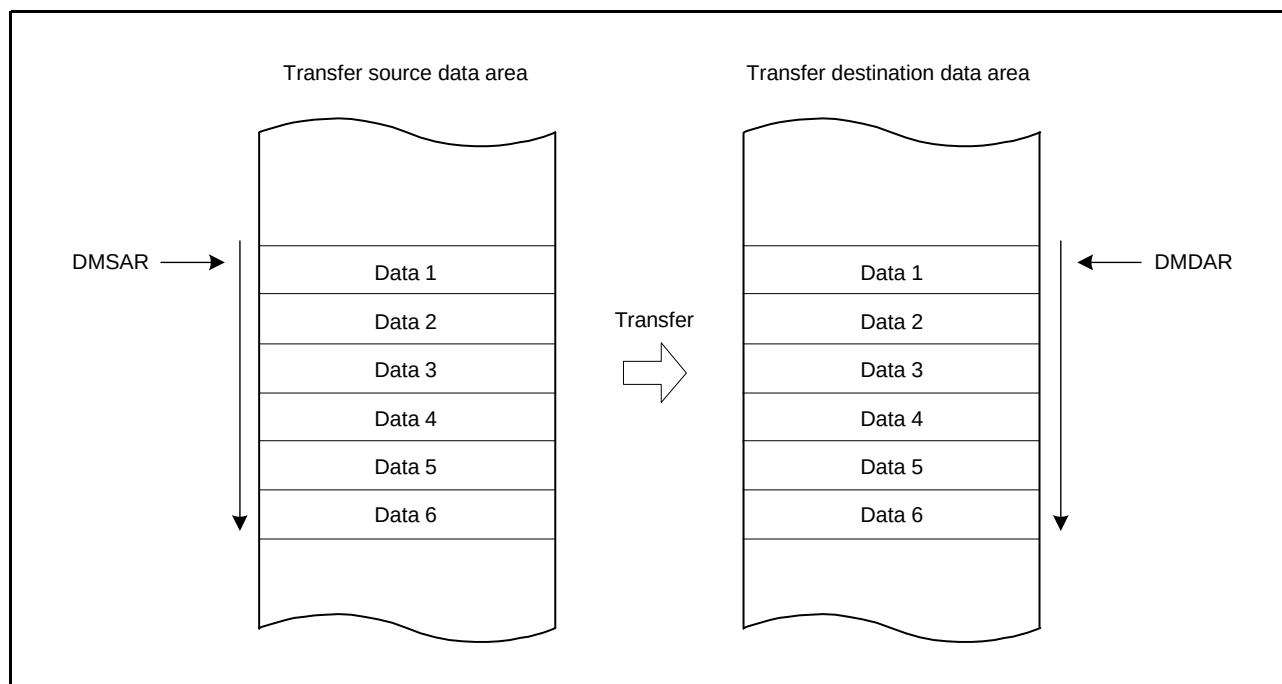


Figure 18.2 Operation in Normal Transfer Mode

(2) Repeat Transfer Mode

In repeat transfer mode, one data is transferred by one transfer request.

A maximum of 1K data can be set as a total repeat transfer size using DMCRA of the DMACm.

A maximum of 1K can be set as the number of repeat transfer operations using DMCRB of the DMACm; therefore, a maximum of 1M data (1K data × 1K count of repeat transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a repeat area. When transfer of the repeat size data is completed, the address of the specified repeat area (DMSAR or DMDAR of the DMACm) returns to the transfer start address. When data of the specified repeat size has all been transferred in repeat transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm in the repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfer operations. Table 18.4 summarizes the register update operation in repeat transfer mode, and Figure 18.3 shows the operation in repeat transfer mode.

Table 18.4 Register Update Operation in Repeat Transfer Mode

Register	Function	Update Operation after Completion of a Transfer by One Transfer Request	
		When DMACm.DMCRAL is not 1	When DMACm.DMCRAL is 1 (Transfer of the Last Data in Repeat Size)
DMACm.DMSAR	Transfer source address	Increment/decrement/fixed/offset addition*1	- DMACm.DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition*1 - DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR - DMACm.DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition*1
DMACm.DMDAR	Transfer destination address	Increment/decrement/fixed/offset addition*1	- DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR - DMACm.DMTMD.DTS[1:0] = 01b Increment/decrement/fixed/offset addition*1 - DMACm.DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition*1
DMACm.DMCRAH	Repeat size	Not updated	Not updated
DMACm.DMCRAL	Transfer count	Decrement by one	DMACm.DMCRAH
DMACm.DMCRB	Count of repeat transfer operations	Not updated	Decrement by one

Note 1. Offset addition can be specified only for DMAC0.

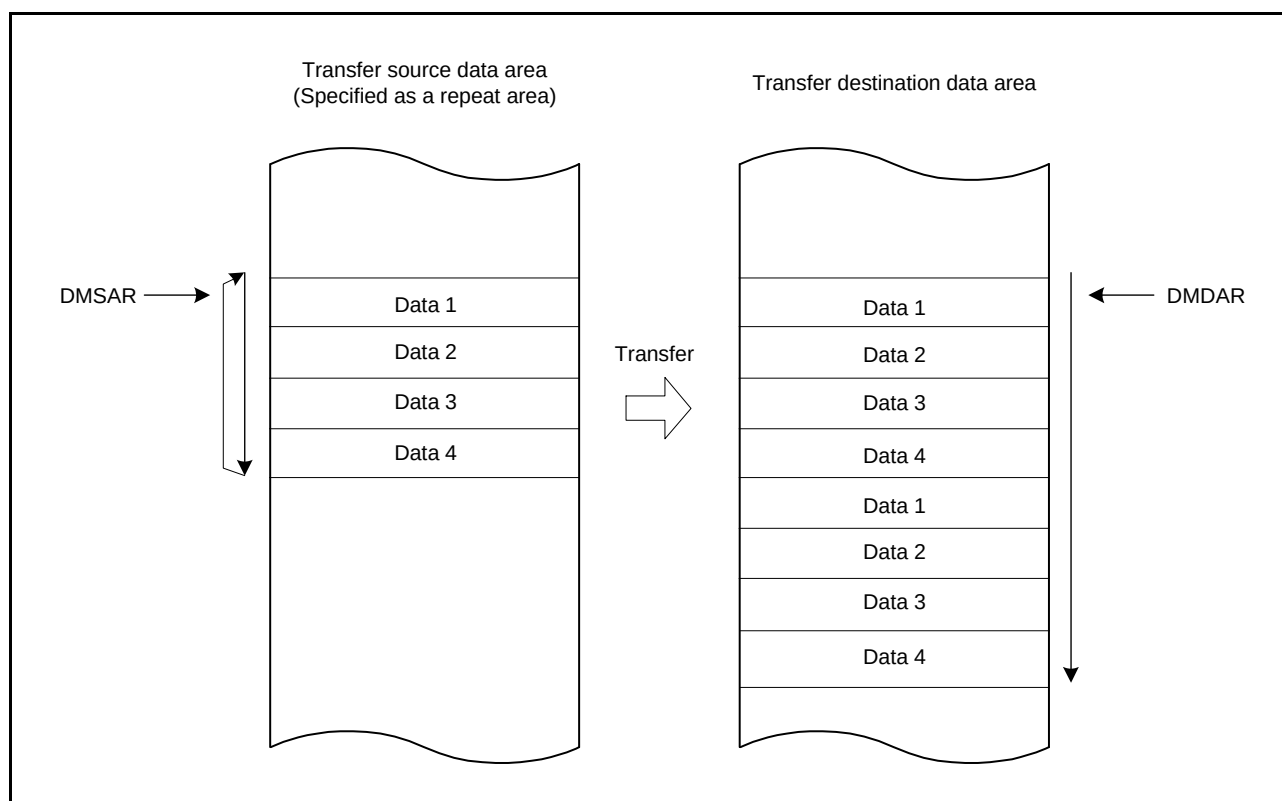


Figure 18.3 Operation in Repeat Transfer Mode

(3) Block Transfer Mode

In block transfer mode, a single block data is transferred by one transfer request.

A maximum of 1K data can be set as a total block transfer size using DMCRA of the DMACm.

A maximum of 1M can be set as the number of block transfer operations using DMCRB of the DMACm; therefore, a maximum of 1M data (1K data × 1K count of block transfer operations) can be set as a total data transfer size.

Either the transfer source or transfer destination can be specified as a block area. When transfer of a single block data is completed, the address of the specified block area (DMSAR or DMDAR of the DMACm) returns to the transfer start address. When a single block data has all been transferred in block transfer mode, DMA transfer can be stopped and the repeat size end interrupt can be requested. DMA transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm in the repeat size end interrupt handling.

Transfer end interrupt request can be generated after completion of the specified number of block transfer operations. Table 18.5 summarizes the register update operation in block transfer mode, and Figure 18.4 shows the operation in block transfer mode.

Table 18.5 Register Update Operation in Block Transfer Mode

Register	Function	Update Operation after Completion of Single-Block Transfer by One Transfer Request
DMACm.DMSAR	Transfer source address	- DMACm.DMTMD.DTS[1:0] = 00b Increment/decrement/fixed/offset addition*1 - DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR - DMACm.DMTMD.DTS[1:0] = 10b Increment/decrement/fixed/offset addition*1
DMACm.DMDAR	Transfer destination address	- DMACm.DMTMD.DTS[1:0] = 00 b Initial value of DMACm.DMDAR - DMACm.DMTMD.DTS[1:0] = 01 b Increment/decrement/fixed/offset addition*1 - DMACm.DMTMD.DTS[1:0] = 10 b Increment/decrement/fixed/offset addition*1
DMACm.DMCRAH	Block size	Not updated
DMACm.DMCRAL	Transfer count	DMACm.DMCRAH
DMACm.DMCRB	Count of block transfer operations	Decrement by one

Note 1. Offset addition can be specified only for DMAC0.

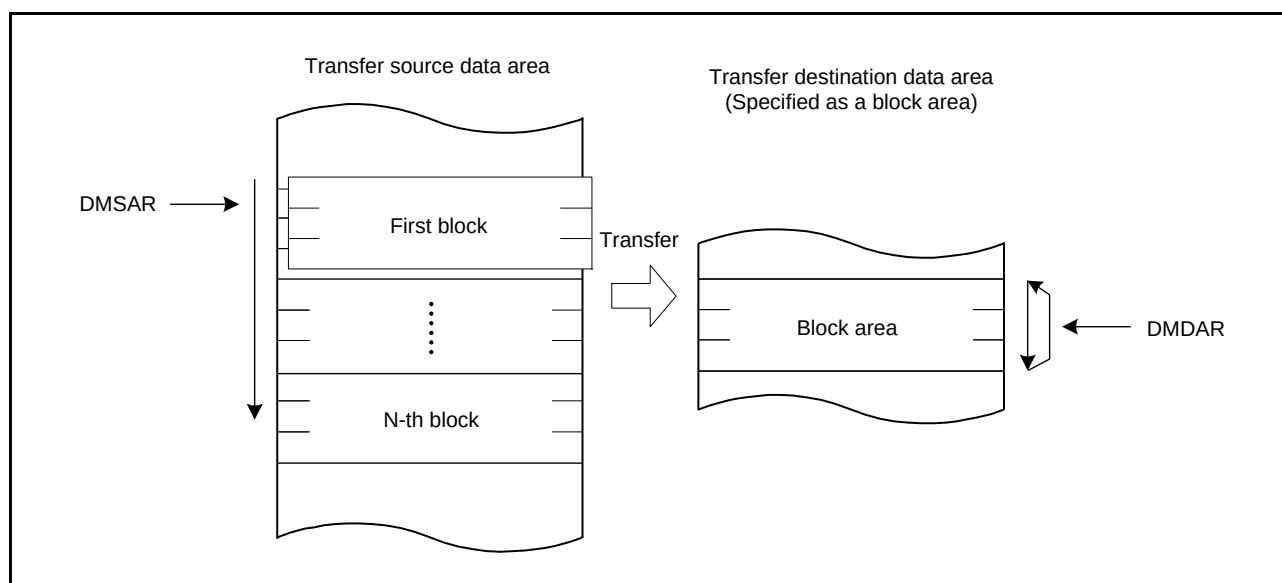


Figure 18.4 Operation in Block Transfer Mode

18.3.2 Extended Repeat Area Function

The DMAC supports a function to specify the extended repeat areas on the transfer source and destination addresses. With the extended repeat areas set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat areas can be specified separately to the transfer source address register (DMSAR) and transfer destination address register (DMDAR) of DMACm.

The extended repeat area on the source address is specified by the SARA[4:0] bits in DMAMD of DMACm. The extended repeat area on the destination address is specified by the DARA[4:0] bits in DMAMD of DMACm. The size can be specified separately for the source and destination sides.

However, the area (of transfer source or transfer destination) which is specified as the repeat area or block area should not be specified as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an interrupt by an extended repeat area overflow can be requested. When an overflow occurs in the extended repeat area on the transfer source while the SARIE bit in DMINT of DMACm is set to 1, the ESIF flag in DMSTS of DMACm is set to 1 and the DTE bit in DMCNT of DMACm is cleared to 0 to stop DMA transfer. At this time, if the ESIE bit in DMINT of DMACm is set to 1, an interrupt by an extended repeat area overflow is requested. When the DARIE bit in DMINT of DMACm is set to 1, the destination address register becomes a target to apply the function. DMA transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm in the interrupt handling.

Figure 18.5 shows an example of the extended repeat area operation.

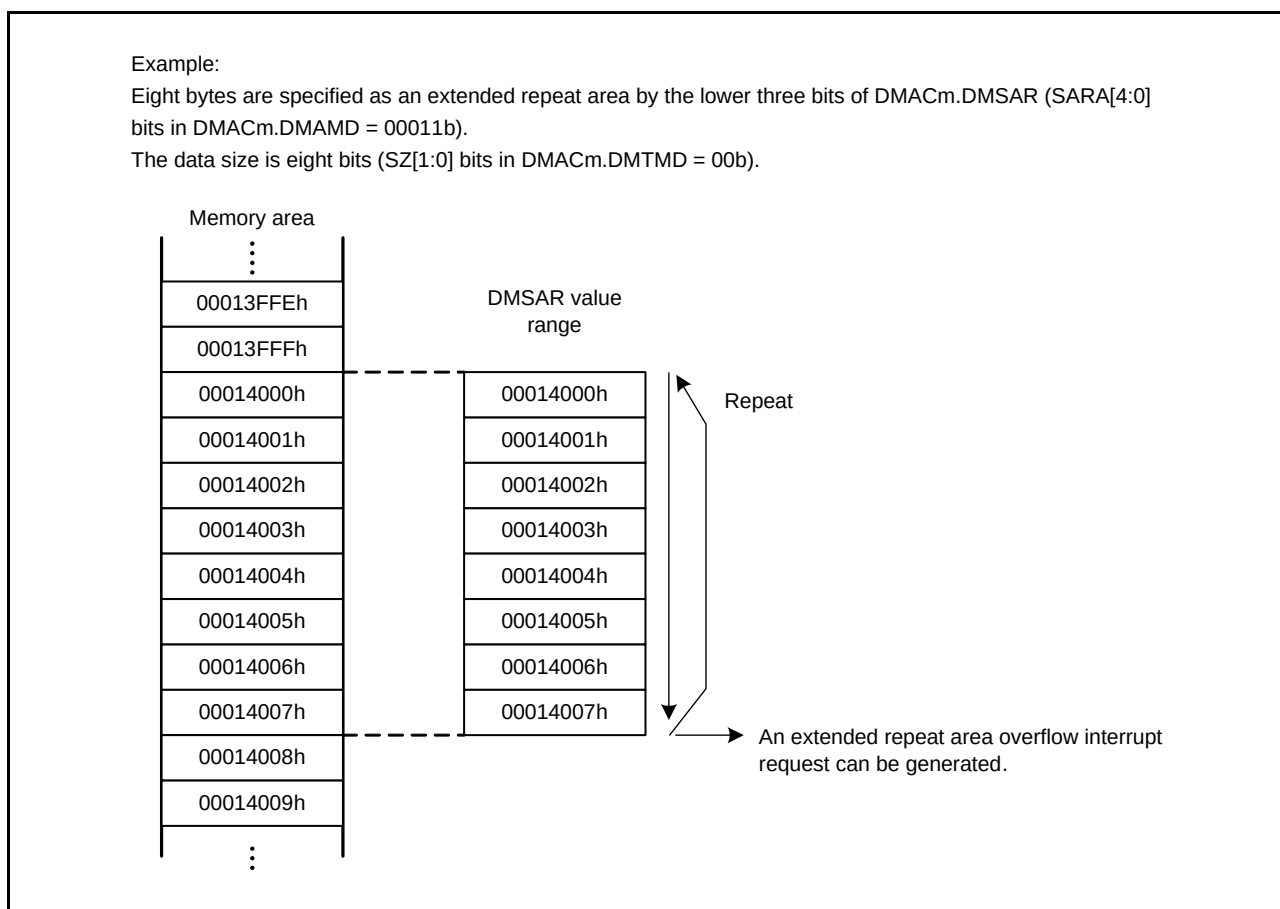


Figure 18.5 Example of Extended Repeat Area Operation

When an interrupt by an extended repeat area overflow is used in block transfer mode, the following should be taken into consideration.

When a transfer is stopped by an interrupt by an extended repeat area overflow, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the interrupt by the overflow is suspended until transfer of the block is completed, and the transfer overruns.

Figure 18.6 shows an example when the extended repeat area function is used in block transfer mode.

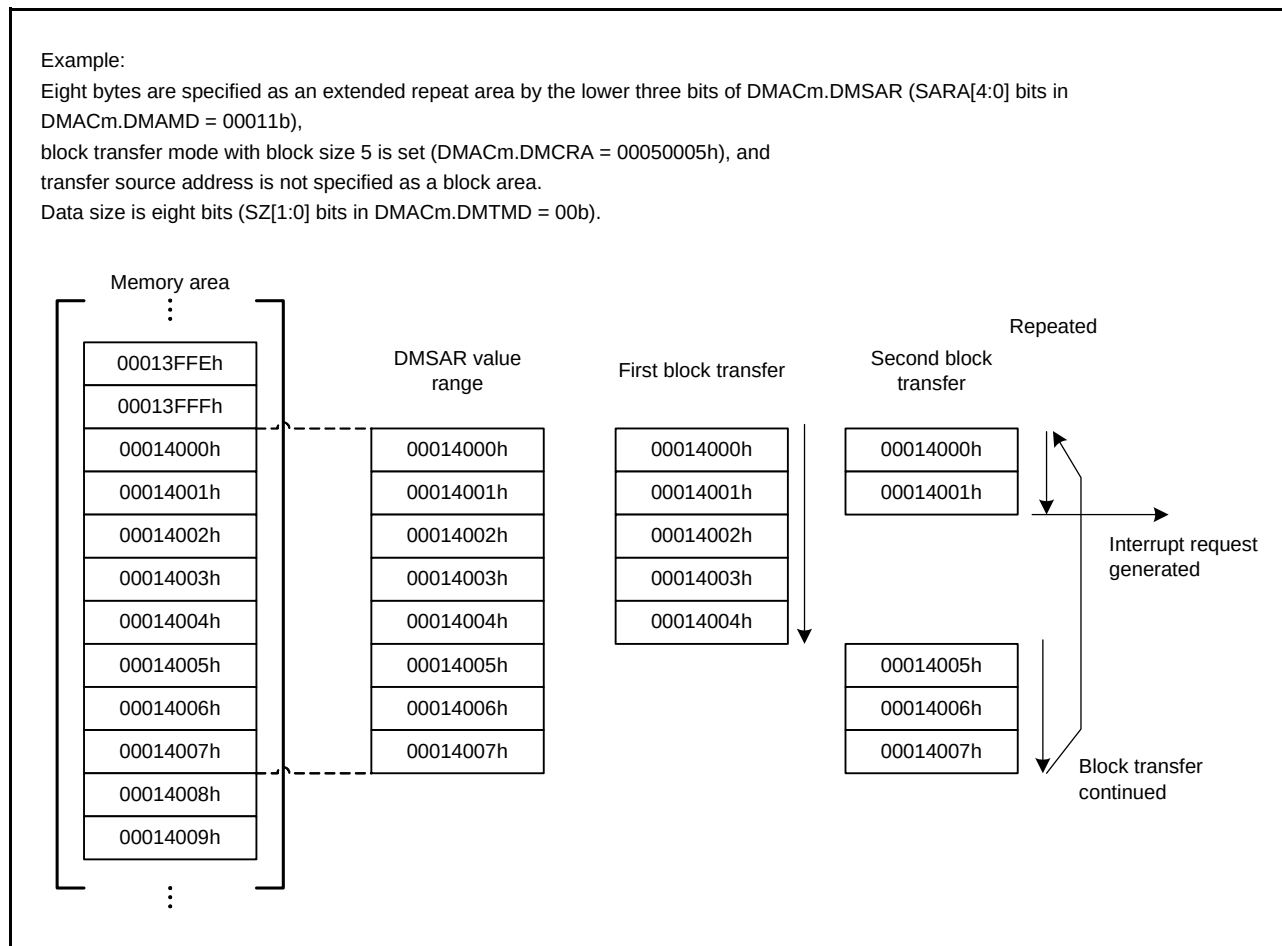


Figure 18.6 Example of Extended Repeat Area Function in Block Transfer Mode

18.3.3 Address Update Function Using Offset

The source and destination addresses can be updated by fixing, increment, decrement, or offset addition. When the offset addition is selected, the offset specified by the DMA offset register (DMOFR of DMAC0) is added to the address every time the DMAC performs one data transfer. This function realizes a data transfer where addresses are allocated to separated areas.

Offset subtraction can also be realized by setting a negative value in DMOFR of DMAC0. In this case, the negative value must be 2's complement.

Address update function using offset can be specified only for the DMAC0 channel.

Table 18.6 shows the address update method in each address update mode.

Table 18.6 Address Update Method in Each Address Update Mode

Address Update Mode	Settings of DMACm.DMAMD.SM[1:0] and DMACm.DMAMD.DM[1:0] for Address Update Modes	Address Update Method (for Different SZ[1:0] Settings in DMTMD of DMACm)		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	-1	-2	-4

Note 1. When setting a negative value in the DMA offset register, the value must be 2's complement. The 2's complement is obtained by the following formula.

2's complement of a negative offset value = $\sim(\text{offset}) + 1$ ($\sim$: bit inversion)

(1) Basic Transfer Using Offset Addition

Figure 18.7 shows an example of address updating using offset addition.

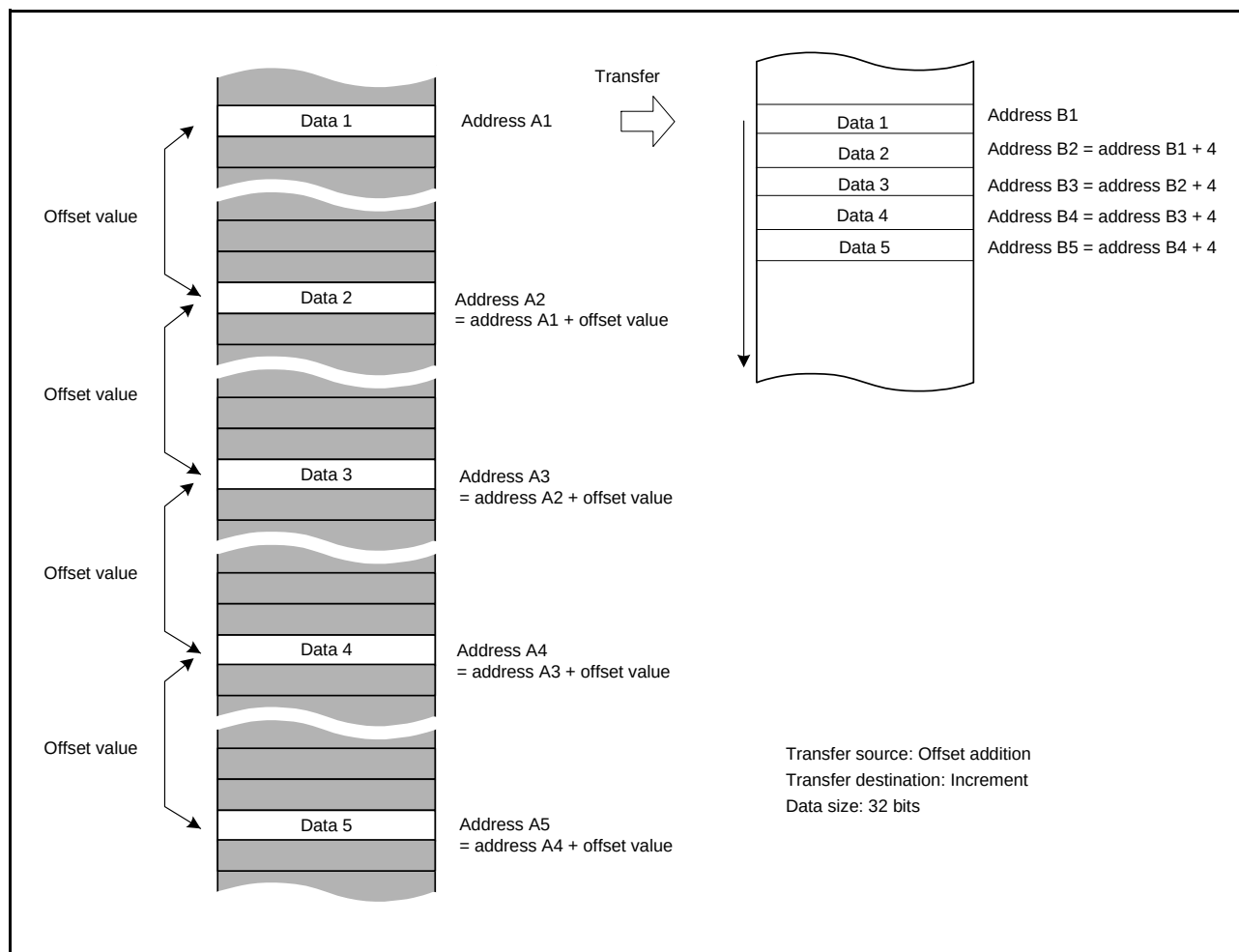


Figure 18.7 Example of Address Updating by Offset Addition

In Figure 18.7, the transfer data is 32 bits long, and offset addition and increment are set as the transfer source address update mode and transfer destination address update mode, respectively. The second and subsequent data is each read from the transfer source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to the continuous locations on the destination.

(2) Example of XY Conversion Using Offset Addition

Figure 18.8 shows the XY conversion using offset addition in repeat transfer mode.

Settings are as follows:

- DMAC0.DMAMD: Transfer source address update mode: Offset addition
- DMAC0.DMAMD: Transfer destination address update mode: Destination address is incremented.
- DMAC0.DMTMD: Transfer data size select: 32 bits
- DMAC0.DMTMD: Transfer mode select: Repeat transfer
- DMAC0.DMTMD: Repeat area select: The source is specified as the repeat area.
- DMAC0.DMOFR: Offset address: 10h
- DMAC0.DMCRA: Repeat size: 4h
- DMAC0.DMINT: The repeat size end interrupt is enabled.

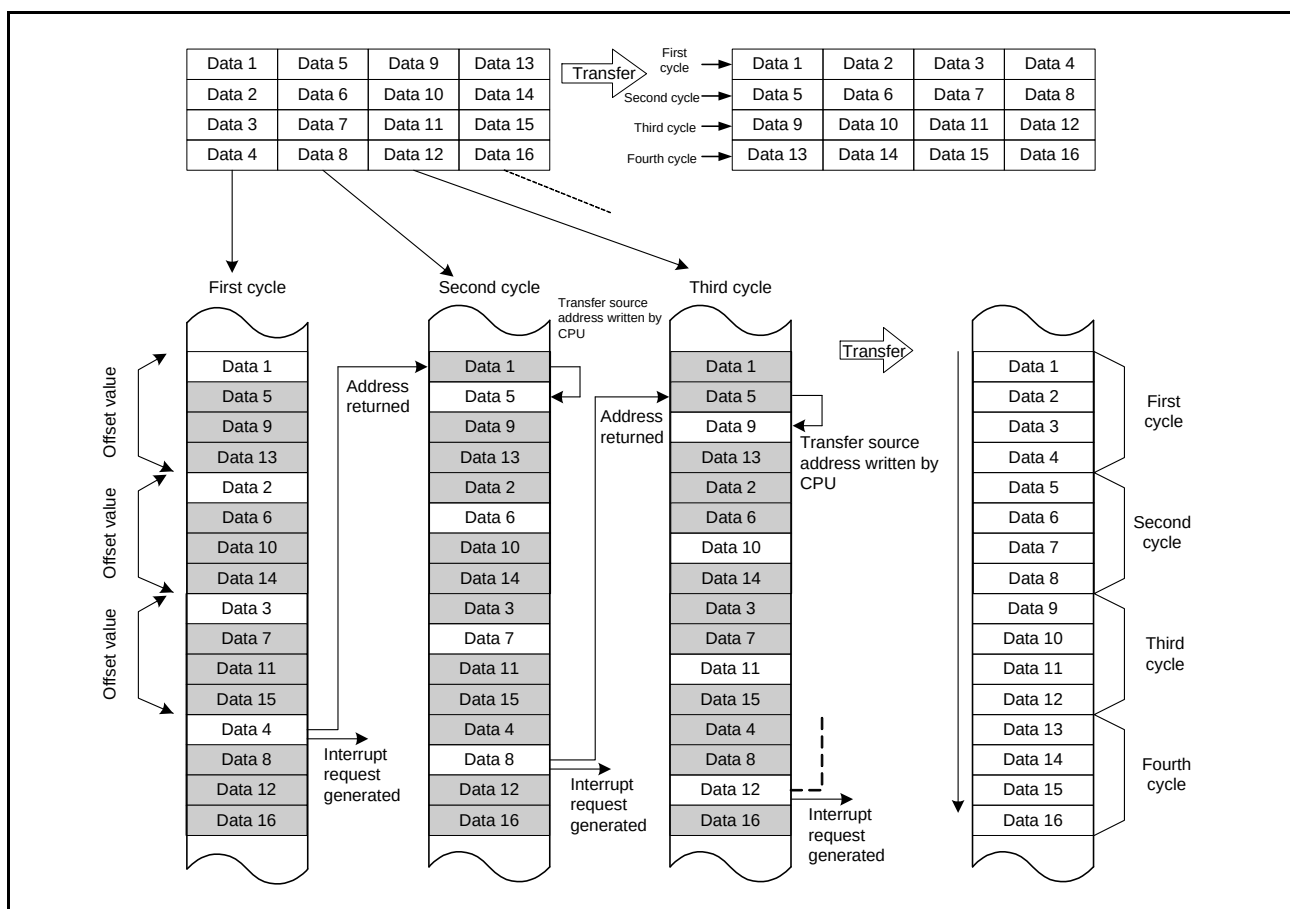


Figure 18.8 XY Conversion Operation Using Offset Addition in Repeat Transfer Mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to the destination continuous addresses. When data 4 is transferred, which means that the repeat size of transfers is completed, the transfer source address returns to the transfer start address (address of data 1 on the transfer source) and a repeat size end interrupt is requested. While this interrupt stops the transfer temporarily, perform the following.

- DMAC0.DMSAR: Rewrite the DMA transfer source address to the address of data 5 (with the above example, the data 1 address + 4).
- DMAC0.DMCNT: Set the DTE bit to 1.

The DMA transfer is resumed from the state when the DMA transfer is stopped. After that, the operations described above are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 18.9 shows a flowchart of the XY conversion.

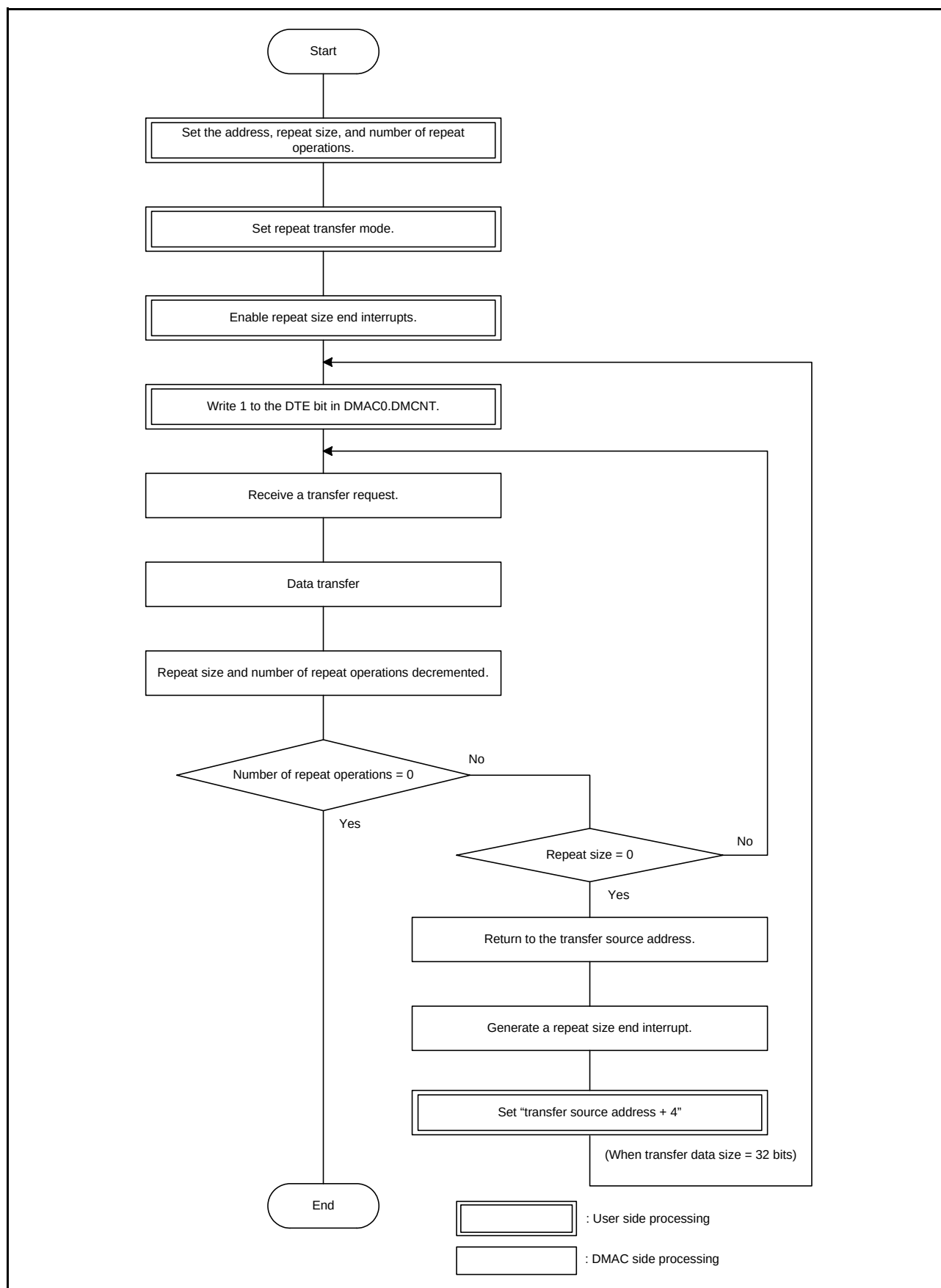


Figure 18.9 XY Conversion Flowchart Using Offset Addition in Repeat Transfer Mode

18.3.4 Activation Sources

Software, the interrupt requests from the peripheral modules, and the external interrupt requests can be specified as the DMAC activation sources. Setting the DCTG[1:0] bits in DMTMD of DMACm selects the activation source.

(1) DMAC Activation by Software

Setting the DCTG[1:0] bits in DMTMD of DMACm to 00b enables the DMAC activation by software.

To start DMA transfer by software, set the DCTG[1:0] bits in DMTMD of DMACm to 00b, and then set the DTE bit in DMCNT of DMACm to 1 (DMA transfer is enabled) and the SWREQ bit in DMREQ of DMACm to 1 (DMA transfer is requested) with the DMST bit in DMAST set to 1 (DMAC activation enabled).

When the DMAC is activated by software while the CLRS bit in DMREQ of DMACm is 0, the SWREQ bit in DMREQ of DMACm is cleared to 0 after data transfer is started in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, the SWREQ bit is not cleared to 0 after data transfer is started. In this case, a DMA transfer request is issued again after completion of a transfer.

(2) DMAC Activation by Interrupt Requests from On-Chip Peripheral Modules or External Interrupt Requests

Interrupt requests from the on-chip peripheral modules and external interrupt requests can be specified as the DMAC activation sources. The activation source can be selected separately for each channel using the DMRSRm registers (m = 0 to 3) of the ICU.

The DMAC is activated when an interrupt request from the on-chip peripheral module or an external interrupt request is generated while the DCTG[1:0] bits in DMTMD of DMACm is set to 01b (interrupts from the peripheral modules and the external interrupt pins are selected), the DTE bit in DMCNT of DMACm is set to 1 (DMA transfer is enabled), and the DMST bit in DMAST is set to 1 (DMAC activation is enabled).

For interrupt requests specified as DMAC activation sources, see Table 15.3, Interrupt Vector Table, in section 15, Interrupt Controller (ICUb).

18.3.5 Operation Timing

Figure 18.10 and Figure 18.11 show DMAC operation timing examples.

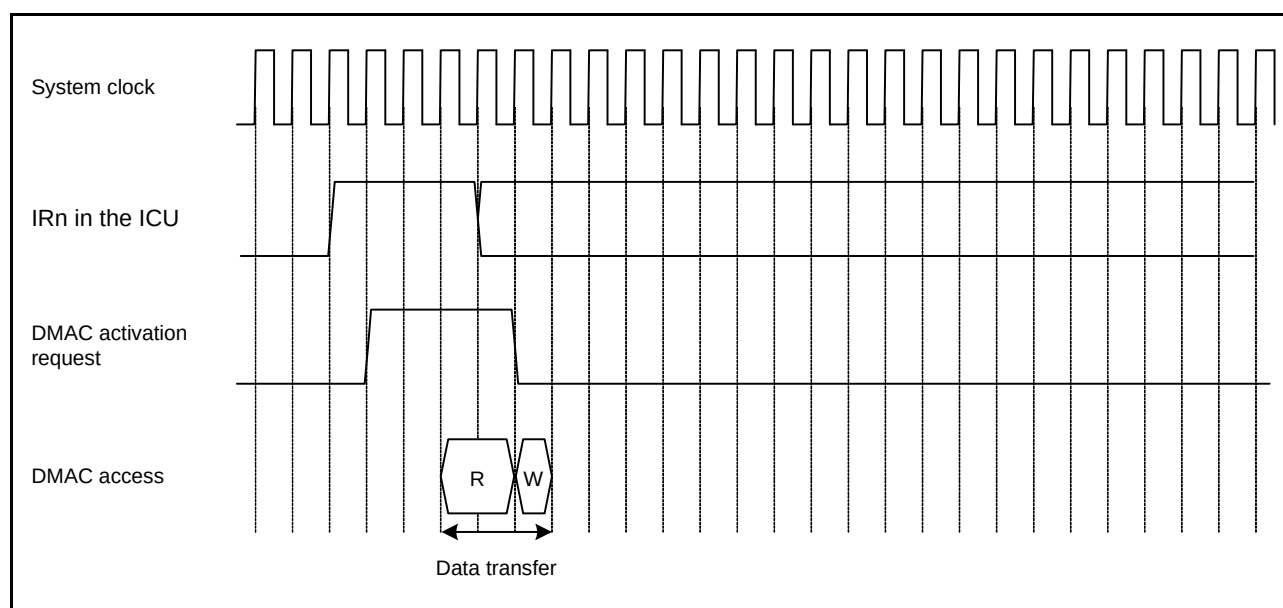


Figure 18.10 DMAC Operation Timing Example (1) (DMA Activation by Interrupt from Peripheral Module/ External Interrupt Input Pin, Normal Transfer Mode, Repeat Transfer Mode)

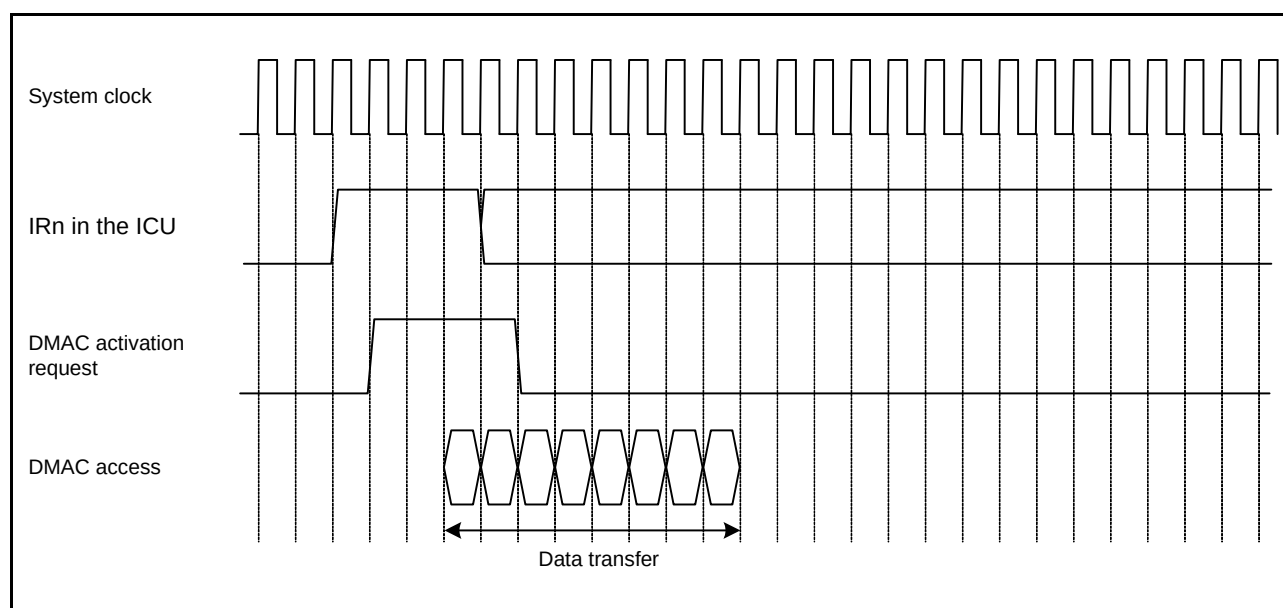


Figure 18.11 DMAC Operation Timing Example (2) (DMA Activation by Interrupt from Peripheral Module/ External Interrupt Input Pin, Block Transfer Mode, Block Size = 4)

18.3.6 DMAC Execution Cycles

Table 18.7 lists execution cycles in one DMAC data transfer operation.

Table 18.7 DMAC Execution Cycles

Transfer Mode	Data Transfer (Read)	Data Transfer (Write)
Normal	Cr+1	Cw
Repeat	Cr+1	Cw
Block*1	$P \times Cr$	$P \times Cw$

Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle is applied.

P: Block size (DMCRAH register setting)

Cr: Data read destination access cycle

Cw: Data write destination access cycle

Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 49, RAM, section 50, Flash Memory (FLASH), and section 5, I/O Registers.

The unit for +1 in “Data Transfer (Read)” column is one system clock cycle (ICLK).

For the operation example, see section 18.3.5, Operation Timing.

18.3.7 Activating the DMAC

Figure 18.12 shows the register setting procedure.

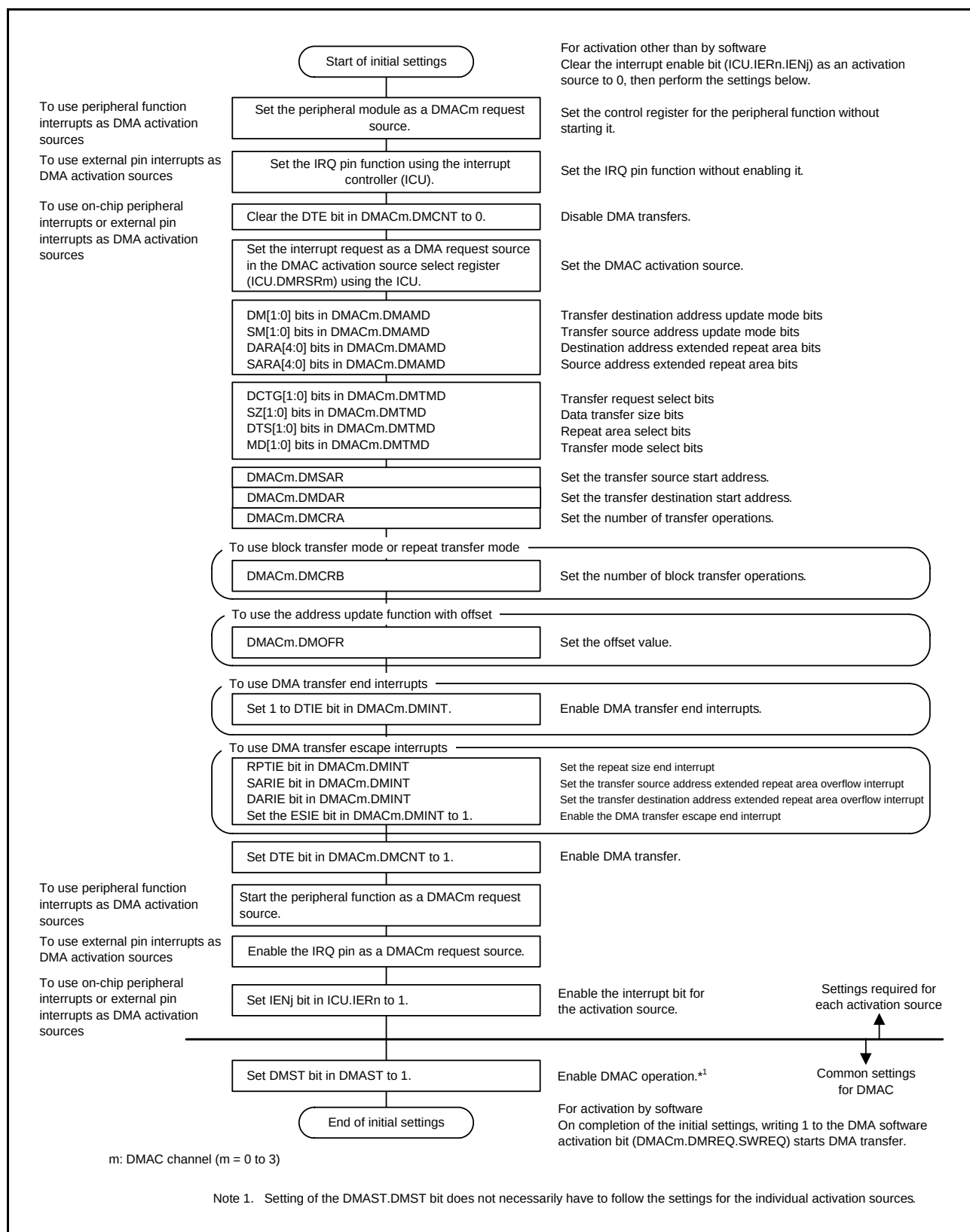


Figure 18.12 Register Setting Procedure

18.3.8 Starting DMA Transfer

Setting the DTE bit in DMCNT of DMACm to 1 (DMA transfer enabled) and setting the DMST bit in DMAST to 1 (DMAC start enabled) enable DMA transfer of channel m (m = 0 to 3).

Another activation request cannot be accepted during the transfer of other DMAC channel or DTC. When the proceeding transfer is completed, channel arbitration is performed where a DMA transfer request of the highest priority channel is accepted and DMA transfer of the channel starts. When DMA transfer starts, the ACT bit in DMSTS of DMACm is set to 1 (the DMAC is in the active state).

18.3.9 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers to be updated are DMSAR, DMDAR, DMCRA, DMCRB, DMCNT, and DMSTS of DMACm.

(1) DMA Source Address Register (DMACm.DMSAR)

When data has been transferred in response to one transfer request, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(2) DMA Destination Address Register (DMACm.DMDAR)

When data has been transferred in response to one transfer request, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(3) DMA Transfer Count Register (DMACm.DMCRA)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(4) DMA Block Transfer Count Register (DMACm.DMCRB)

When data has been transferred in response to one transfer request, the count value is updated. The update operation depends on the transfer mode selected.

For details on register update operation in each transfer mode, refer to Table 18.3 to Table 18.5.

(5) DMA Transfer Enable Bit (DMACm.DMCNT.DTE)

Although the DMACm.DMCNT.DTE bit enables or disables data transfer by the register write access, it is automatically cleared to 0 by the DMAC according to the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is completed
- When DMA transfer is stopped by the repeat size end interrupt
- When DMA transfer is stopped by the extended repeat area overflow interrupt

Writing to the registers for the channels when the corresponding DMACm.DMCNT.DTE bit is set to 1 is prohibited (except for DMACm.DMCNT). In this case, writing must be performed after the bit is cleared to 0.

(6) DMA Active Flag (DMACm.DMSTS.ACT)

The ACT bit in DMSTS of DMACm indicates whether the DMACm is in the idle or active state.

This flag is set to 1 when the DMAC starts data transfer, and is cleared to 0 when data transfer in response to one transfer request is completed.

Even when DMA transfer is stopped by writing 0 to the DTE bit in DMCNT of DMACm during DMA transfer, this flag remains 1 until DMA transfer is completed.

(7) Transfer End Interrupt Flag (DMACm.DMSTS.DTIF)

The DTIF flag in DMSTS of DMACm is set to 1 after DMA transfer of the total transfer size of data is completed.

When both this flag and the DTIE bit in DMINT of DMACm are set to 1, a transfer end interrupt is requested.

This flag is set to 1 when the DMA transfer bus cycle is completed and the ACT flag in DMSTS of DMACm is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DTE bit in DMCNT of DMACm is set to 1 during the interrupt handling.

(8) Transfer Escape End Interrupt Flag (DMACm.DMSTS.ESIF)

The ESIF flag in DMSTS of DMACm is set to 1 when a repeat size end interrupt or extended repeat area overflow interrupt is requested. When this bit and the ESIE bit in DMINT of DMACm are set to 1, a transfer escape end interrupt is requested.

This flag is set to 1 when the bus cycle of the DMA transfer having caused the interrupt request is completed and the ACT flag in DMSTS of DMACm is cleared to 0 indicating the DMA transfer end.

This flag is automatically cleared to 0 when the DTE bit in DMCNT of DMACm is set to 1 during an interrupt handling.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set.

For details, see section 15, Interrupt Controller (ICUb).

18.3.10 Channel Priority

When multiple DMA transfer requests are present, the DMAC determines the priority of channels that have DMA transfer requests.

The channel priority is fixed as channel 0 > channel 1 > channel 2 > channel 3 (channel 0: highest).

When a DMA transfer request is generated during data transfer, channel arbitration is started after the final data has been transferred, and DMA transfer of the higher-priority channel starts.

18.4 Ending DMA Transfer

The operation for ending DMA transfer depends on the transfer end conditions. When DMA transfer ends, the DTE bit in DMCNT and the ACT flag in DMSTS of DMACm are changed from 1 to 0, indicating that DMA transfer has ended.

18.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In Normal Transfer Mode (DMACm.DMTMD.MD[1:0] = 00b)

When the value of DMCRAL of DMACm changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DTE bit in DMCNT of DMACm is cleared to 0 and the DTIF bit in DMSTS of DMACm is set to 1 at the same time. If the DTIE bit in DMINT of DMACm is 1 at this time, a transfer end interrupt request is issued to the CPU or the DTC.

(2) In Repeat Transfer Mode (DMACm.DMTMD.MD[1:0] = 01b)

When the value of DMCRB of DMACm changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DTE bit in DMCNT of DMACm is cleared to 0 and the DTIF bit in DMSTS of DMACm is set to 1 at the same time. If the DTIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC.

(3) In Block Transfer Mode (DMACm.DMTMD.MD[1:0] = 10b)

When the value of DMCRB of DMACm changes from 1 to 0, DMA transfer ends on the corresponding channel, and the DTE bit in DMCNT of DMACm is cleared to 0 and the DTIF bit in DMSTS of DMACm is set to 1 at the same time. If the DTIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt Controller (ICUb).

18.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, a repeat size end interrupt is requested when transfer of a 1-repeat size of data is completed while the RPTIE bit in DMINT of DMACm is set to 1. When the interrupt is requested to complete DMA transfer, the DTE bit in DMCNT of DMACm is cleared to 0 and the ESIF flag in DMSTS of DMACm is set to 1. If the ESIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC. Here, the transfer can be resumed by writing 1 to the DTE bit in DMCNT of DMACm.

A repeat size end interrupt can be requested also in block transfer mode. In block transfer mode, the interrupt is requested in the same way as in repeat transfer mode when transfer of a 1-block size data is completed.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt Controller (ICUb).

18.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the SARIE or DARIE bit in DMINT of DMACm is set to 1, an interrupt by an extended repeat area overflow is requested. When the interrupt is requested, the DMA transfer is terminated, the DTE bit in DMCNT of DMACm is cleared to 0, and the ESIF flag in DMSTS of DMACm is set to 1. If the ESIE bit in DMINT of DMACm is 1 at this time, an interrupt request is issued to the CPU or the DTC.

Even if an interrupt by an extended repeat area overflow is requested during a read cycle, the following write cycle is performed.

In block transfer mode, even if an interrupt by an extended repeat area overflow is requested during a 1-block transfer, the remaining data in the block is transferred; transfer is terminated after a block transfer.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For details, see section 15, Interrupt Controller (ICUb).

18.5 Interrupts

Each DMAC channel can output an interrupt request to the CPU or the DTC after transfer in response to one request is completed. When the transfer destination is the on-chip peripheral bus, an interrupt request is generated upon completion of data write to the write buffer not to the actual transfer destination.

Table 18.8 lists the relation among the interrupt sources, the interrupt status flags, and the interrupt enable bits. Figure 18.13 shows the schematic logic diagram of interrupt outputs. Figure 18.14 shows the DMAC interrupt handling routine to resume or terminate DMA transfer.

Table 18.8 Relation among Interrupt Sources, Interrupt Status Flags, and Interrupt Enable Bits

Interrupt Sources		Interrupt Enable Bits	Interrupt Status Flags	Request Output Enable Bits
Transfer end		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
Escape transfer end	Repeat size end	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	Source address extended repeat area overflow	DMACm.DMINT.SARIE		
	Destination address extended repeat area overflow	DMACm.DMINT.DARIE		

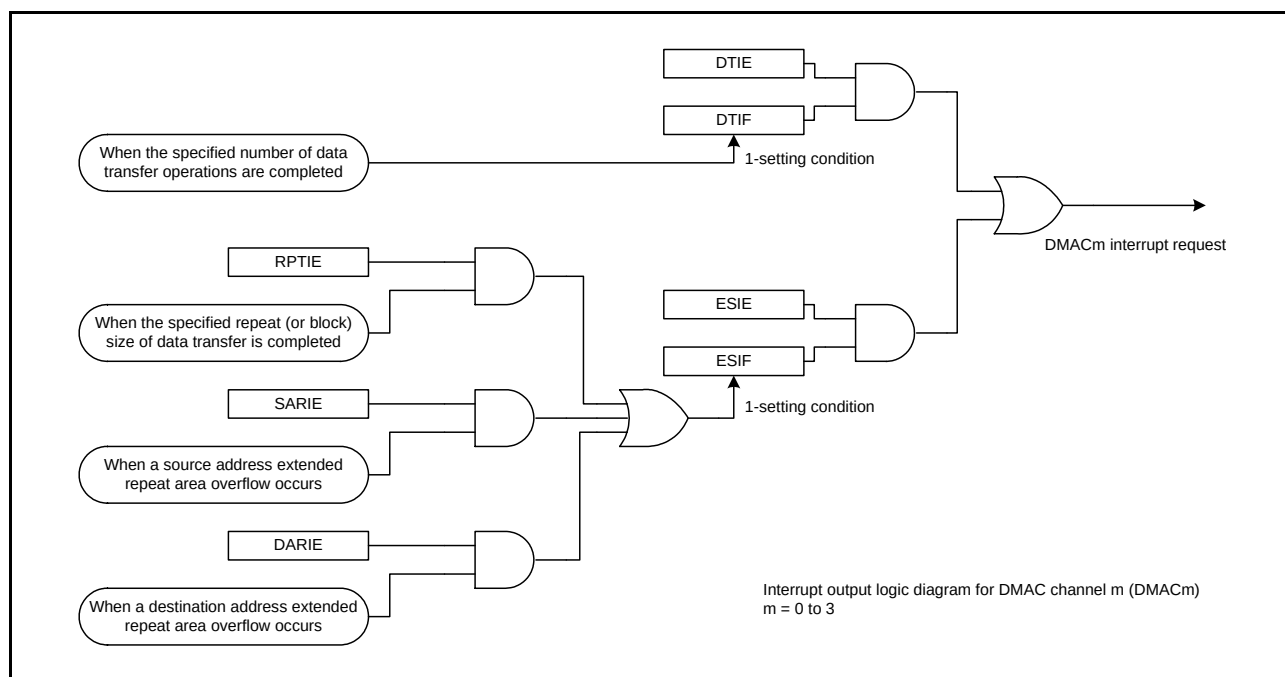


Figure 18.13 Schematic Logic Diagram of Interrupt Outputs

Specifically, the different procedures are used for canceling an interrupt to restart DMA transfer in the following two cases: (1) discontinuing or terminating DMA transfer and (2) continuing DMA transfer.

(1) When Discontinuing or Terminating DMA Transfer

Write 0 to the DTIF bit in DMSTS of DMACm to clear a transfer end interrupt, and to the ESIF bit in DMSTS of DMACm to clear a repeat size interrupt and an extended repeat area overflow interrupt. The DMACm remains in the stop state. When starting another DMA transfer after that, set the appropriate registers, and set the DTE bit in DMCNT of DMACm to 1 (DMA transfer enabled).

(2) When Continuing DMA Transfer

Write 1 to the DTE bit in DMCNT of DMACm. The ESIF bit in DMSTS of DMACm is automatically cleared to 0 (interrupt source cleared), and DMA transfer is resumed.

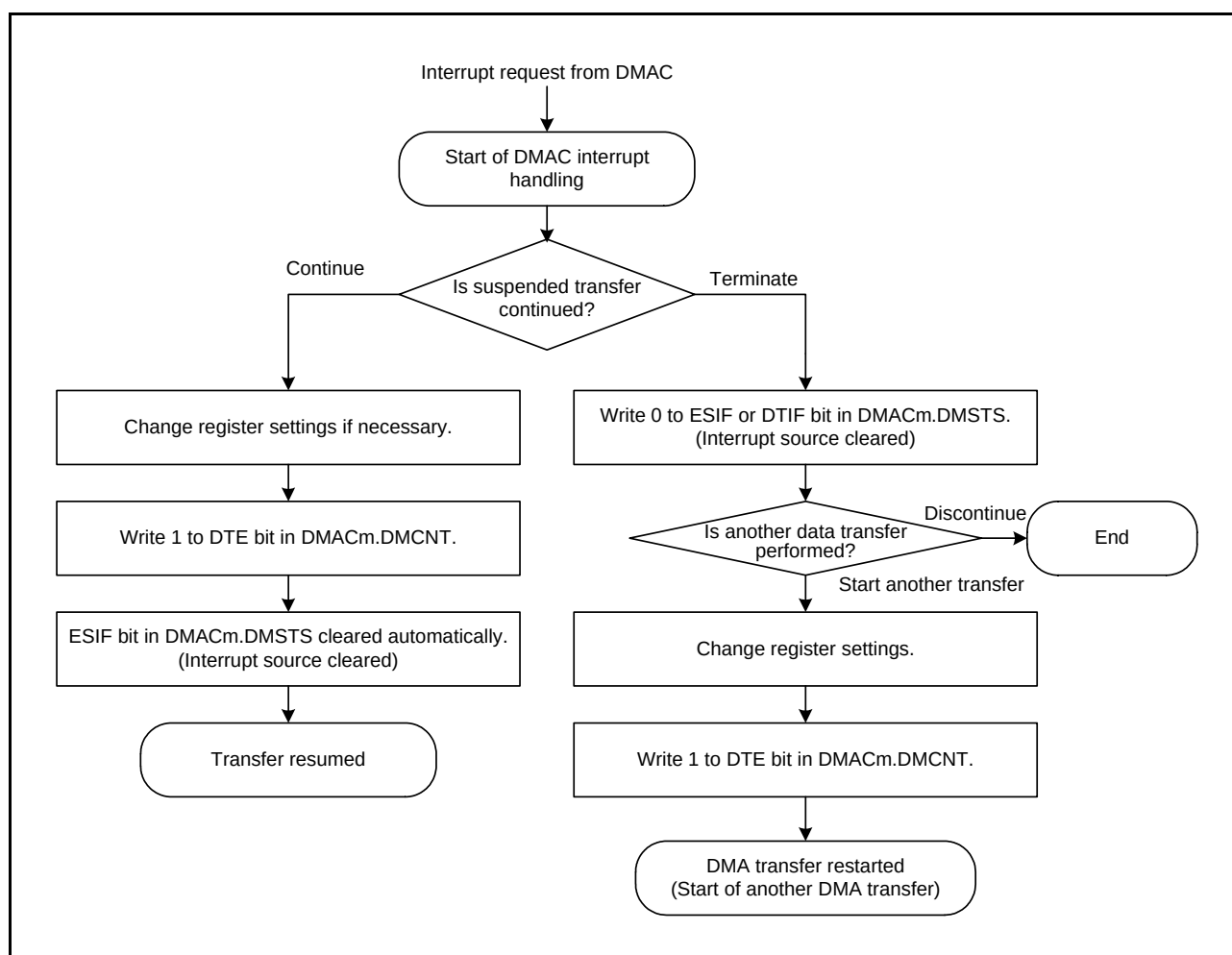


Figure 18.14 DMAC Interrupt Handling Routine to Resume/Terminate DMA Transfer

18.6 Event Link Function

Each DMAC channel outputs an event link request signal each time the channel completes data transfer (or block transfer in block transfer mode). However, when the transfer destination is the internal peripheral bus, an event link request signal is generated when the write to the write buffer is accepted.

18.7 Low Power Consumption Function

Before transition to the module stop state or software standby mode, clear the DMAST.DMST bit to 0 (DMAC activation is disabled), and then perform the following.

(1) Module Stop Function

Writing 1 to the MSTPA28 bit (transition to the module-stop state) in MSTPCRA enables the module-stop function of the DMAC. If DMA transfer is in progress at the time 1 is written to the MSTPA28 bit, the transition to the module-stop state proceeds after DMA transfer has ended. While the MSTPA28 bit is 1, accessing the DMAC registers are prohibited. Writing 0 to the MSTPA28 bit releases the DMAC from the module-stop state.

(2) Software Standby

Make settings in accord with the procedure under section 11.6.3.1, Entry to Software Standby Mode in section 11, Low Power Consumption.

If DMA transfer operations are in progress at the time the WAIT instruction is executed, the transition to software standby follows the completion of DMA transfer.

(3) Note on Low Power Consumption Function

For the WAIT instruction and the register setting procedure, see section 11.7.5, Timing of WAIT Instructions in section 11, Low Power Consumption.

To perform DMA transfer after returning from low power consumption mode, set the DMST bit in DMAST to 1 again. To use a request that is generated in software standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination in accordance with the description in section 15.4.3, Selecting Interrupt Request Destinations in section 15, Interrupt Controller (ICUb), and then execute the WAIT instruction.

18.8 Usage Notes

18.8.1 DMA Transfer to Peripheral Modules

In DMA transfer to a peripheral module, the ACT bit in DMSTS of DMACm may be cleared to 0 (DMAC transfer suspended) during the period from the beginning of the final data write to the end of the peripheral bus access.

18.8.2 Access to the Registers during DMA Transfer

The DMSAR, DMDAR, DMCRA, DMCRB, DMTMD, DMINT, DMAMD, DMOFR, and DMCSL registers of DMACm must not be accessed while the ACT bit in DMSTS of the same channel is set to 1 (DMAC active state) or the DTE bit in DMCNT of the same channel is set to 1 (DMA transfer enabled).

18.8.3 DMA Transfer to Reserved Areas

DMA transfer to the reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on the reserved areas, see section 4, Address Space.

18.8.4 Interrupt Request by the DMA Activation Source Flag Control Register (DMCSL) at the End of each Transfer

While the DMACm.DMCSL.DISEL bit is 1, an interrupt is issued to the CPU at the end of each transfer that has been activated by one DMA request. Unlike the transfer end interrupt that the DMAC outputs or the escape end interrupt, the interrupt of this type is issued to the CPU at the end of DMA transfer without clearing the interrupt flag of the DMAC activation source to 0 by changing the interrupt request destination to the CPU. In this case, since the interrupt flag is not cleared to 0 at the end of DMAC transfer, it should be cleared to 0 by the CPU interrupt routine.

The interrupt flag is cleared when the CPU interrupt is accepted.

For the change of the settings on the interrupt flag or the interrupt request destination, see section 15, Interrupt Controller (ICUb). For the DMACm.DMCSL.DISEL bit setting, see section 18.2.12, DMA Activation Source Flag Control Register (DMCSL).

18.8.5 Setting of DMAC Activation Source Select Register of the Interrupt Controller (ICU.DMRSRm)

The DMAC activation source select register (ICU.DMRSRm) should be set while the DMA transfer enable bit (DMACm.DMCNT.DTE) is cleared to 0 (DMA transfer is disabled). Moreover, the DTC activation enable register (ICU.DTCERm) that corresponds to the same vector number that has been set by the ICU.DMRSRm register should not be set to 1. For details on the ICU.DTCERn and ICU.DMRSRm, see section 15, Interrupt Controller (ICUb).

18.8.6 Suspending or Restarting DMA Activation

To suspend a DMA activation request, write 0 to the interrupt enable bit for the activation source (ICU.IERn.IENj bit). To restart the DMA transfer, write 1 to the ICU.IERn.IENj bit with the setting shown in section 18.3.7, Activating the DMAC.

19. Data Transfer Controller (DTCa)

This MCU incorporates a data transfer controller (DTC).

The DTC is triggered by an interrupt request to perform data transfers.

19.1 Overview

Table 19.1 lists the specifications of the DTC, and Figure 19.1 shows a block diagram of the DTC.

Table 19.1 DTC Specifications

Item	Description
Number of transfer channels	The same number as all interrupt sources that can start the DTC transfer.
Transfer modes	- Normal transfer mode A single transfer request leads to a single data transfer. - Repeat transfer mode A single transfer request leads to a single data transfer. The transfer address is returned to the transfer start address after the number of data transfers corresponding to "repeat size". The maximum number of repeat transfers is 256, and the maximum data transfer size is 256×32 bits, 1024 bytes. - Block transfer mode A single transfer request leads to the transfer of a single block. The maximum block size is 256×32 bits = 1024 bytes.
Chain transfer	- Multiple types of data transfers can sequentially be executed in response to a single request. - Either "performed only when the transfer counter becomes 0" or "every time" can be selected.
Transfer space	- In short-address mode: 16 Mbytes (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) - In full-address mode: 4 Gbytes (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	- Single data: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits) - Single block size: 1 to 256 data
CPU interrupt source	- An interrupt request can be generated to the CPU on a request source for a data transfer. - An interrupt request can be generated to the CPU after a single data transfer. - An interrupt request can be generated to the CPU after data transfer of specified volume.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Low power consumption function	Module stop state can be set.

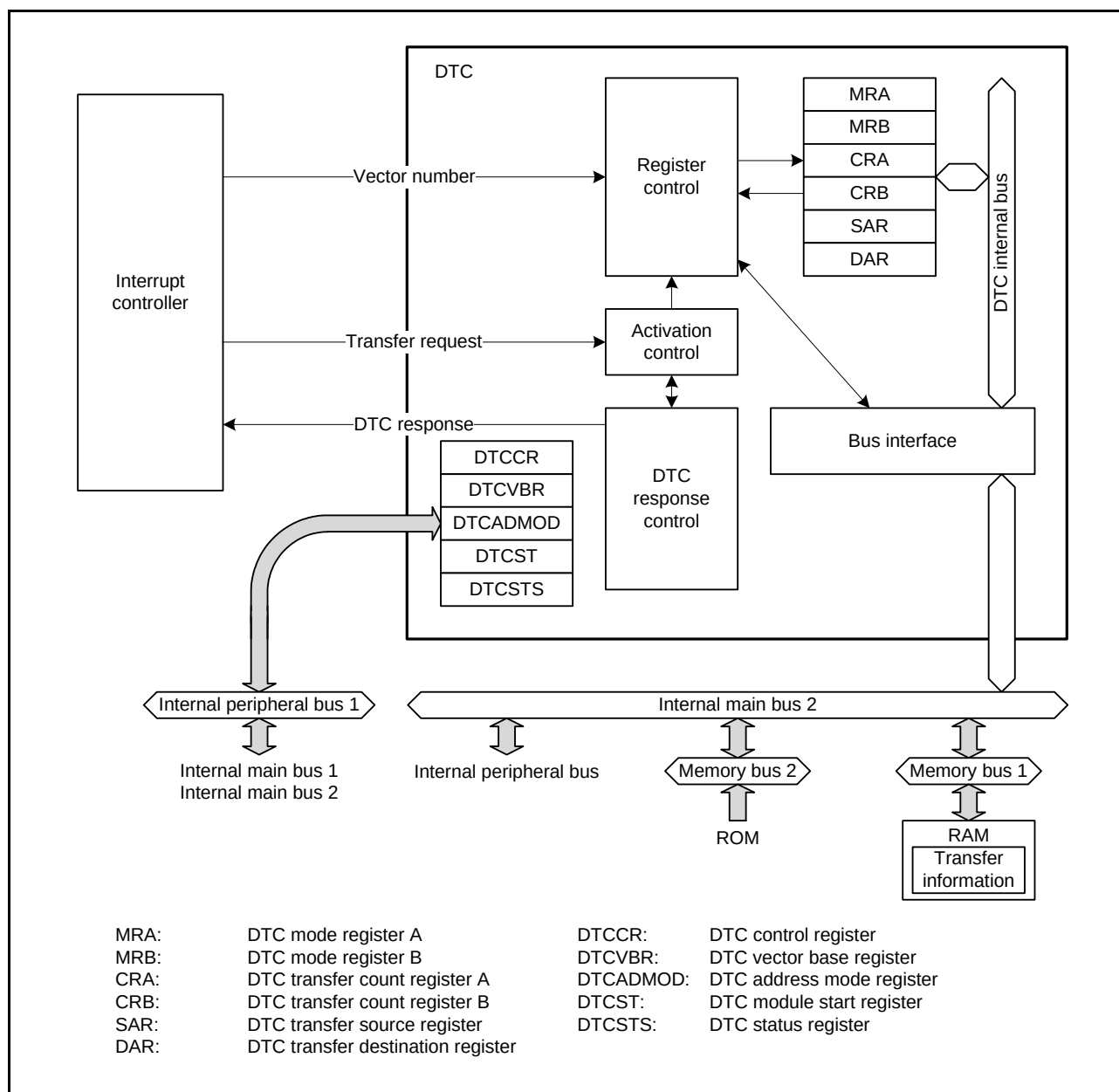


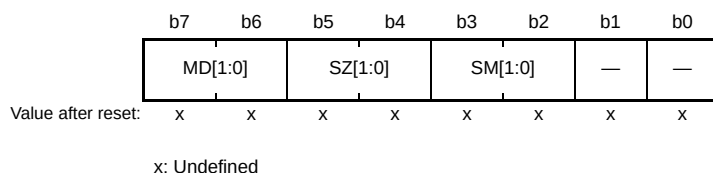
Figure 19.1 DTC Block Diagram

19.2 Register Descriptions

Registers MRA, MRB, SAR, DAR, CRA, and CRB are DTC internal registers, which cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the RAM area as transfer information. When accepting a transfer request, the DTC reads the transfer information from the RAM area and sets it in the internal registers. After the data transfer ends, the values of the updated internal register are written back to the RAM area as transfer information.

19.2.1 DTC Mode Register A (MRA)

Address(es): (inaccessible directly from the CPU)



Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	Set these bits to 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: The address in the SAR register is fixed. (write-back to SAR is skipped.) 0 1: The address in the SAR register is fixed. (write-back to SAR is skipped.) 1 0: The SAR value is incremented after a data transfer. (+1 when the SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b) 1 1: The SAR value is decremented after a data transfer. (−1 when the SZ[1:0] bits are 00b, −2 when 01b, −4 when 10b)	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: Byte (8-bit) transfer 0 1: Word (16-bit) transfer 1 0: Longword (32-bit) transfer 1 1: Setting prohibited	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited	—

MRA register is used to select the DTC operating mode and cannot be accessed directly from the CPU.

19.2.2 DTC Mode Register B (MRB)

Address(es): (inaccessible directly from the CPU)

b7	b6	b5	b4	b3	b2	b1	b0
CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	Set these bits to 0.	—
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 0 1: The address in the DAR register is fixed. (Write-back to DAR is skipped.) 1 0: The DAR value is incremented after data transfer. (+1 when the MRA.SZ[1:0] bits are 00b, +2 when 01b, +4 when 10b) 1 1: The DAR value is decremented after data transfer. (−1 when the MRA.SZ[1:0] bits are 00b, −2 when 01b, −4 when 10b)	—
b4	DTS	DTC Transfer Mode Select	0: Transfer destination side is repeat area or block area. 1: Transfer source side is repeat area or block area.	—
b5	DISEL	DTC Interrupt Select	0: An interrupt request to the CPU is generated on completion of the specified number of data transfers. 1: An interrupt request to the CPU is generated for each data transfer.	—
b6	CHNS	DTC Chain Transfer Select	0: Chain transfer is performed on completion of each transfer. 1: Chain transfer is performed only when the transfer counter is changed from 1 to 0 or 1 to CRAH.	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer is disabled. 1: Chain transfer is enabled.	—

MRB register is used to select the DTC operating mode and cannot be accessed directly from the CPU.

DTS Bit (DTC Transfer Mode Select)

The DTS bit specifies the side (transfer source or destination) to be a repeat area or block area in repeat transfer mode or block transfer mode.

CHNS Bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition.

When the CHNE bit is 0, setting of the CHNS bit is ignored. For details on the conditions to select the chain transfer, refer to Table 19.3, Chain Transfer Conditions.

When the next transfer is chain transfer, completion of the specified number of transfers is not determined, the interrupt status flag for the request source is not cleared, and an interrupt request to the CPU is not generated.

CHNE Bit (DTC Chain Transfer Enable)

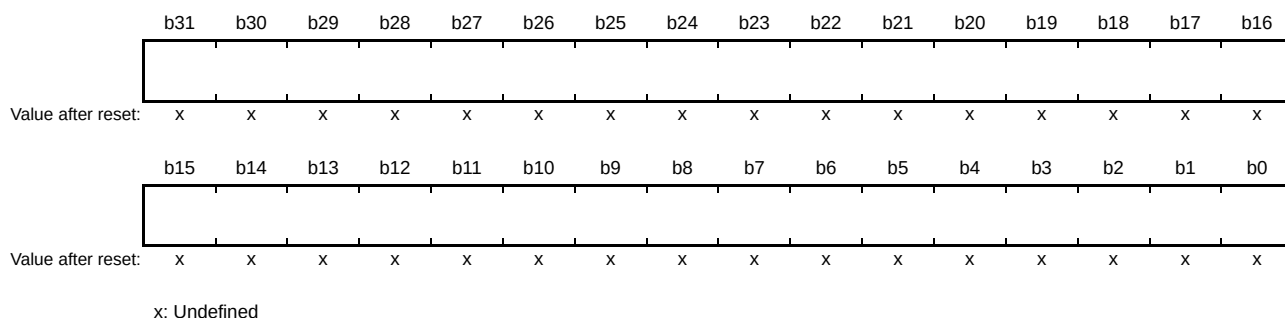
The CHNE bit enables or disables chain transfer.

The chain transfer condition is selected by the CHNS bit.

For details of chain transfer, refer to section 19.4.6, Chain Transfer.

19.2.3 DTC Transfer Source Register (SAR)

Address(es): (inaccessible directly from the CPU)



SAR register is used to set the transfer source start address.

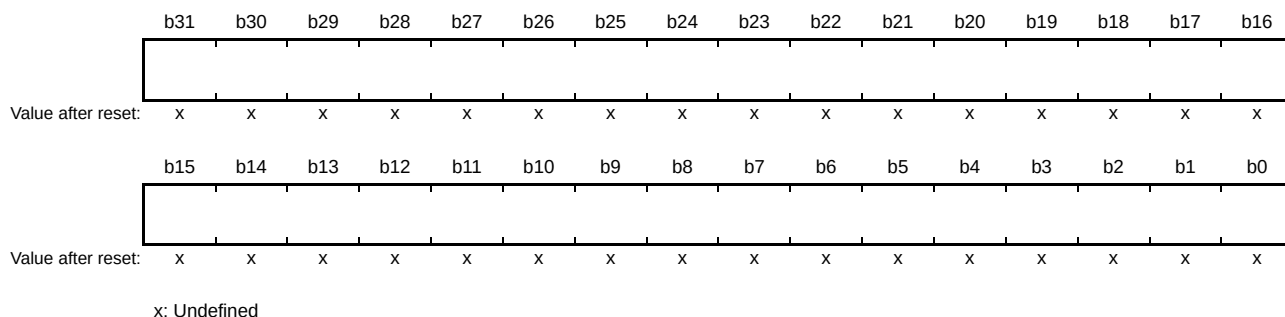
In full-address mode, 32 bits are valid.

In short-address mode, lower 24 bits are valid and upper 8 bits (b31 to b24) are ignored. The address of this register is extended by the value specified by b23.

SAR register cannot be accessed directly from the CPU.

19.2.4 DTC Transfer Destination Register (DAR)

Address(es): (inaccessible directly from the CPU)



DAR register is used to set the transfer destination start address.

In full-address mode, 32 bits are valid.

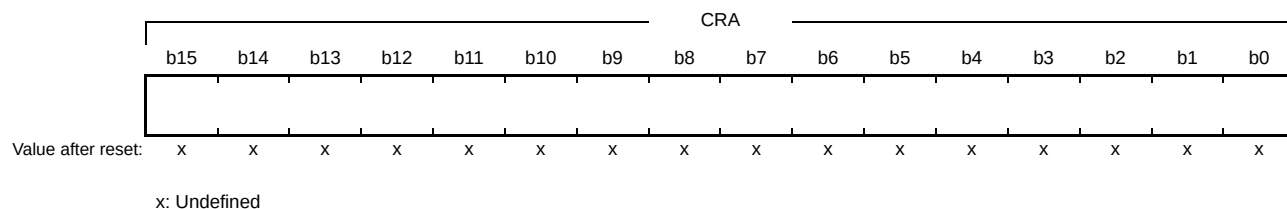
In short-address mode, lower 24 bits are valid and upper 8 bits (b31 to b24) are ignored. The address of this register is extended by the value specified by b23.

DAR register cannot be accessed directly from the CPU.

19.2.5 DTC Transfer Count Register A (CRA)

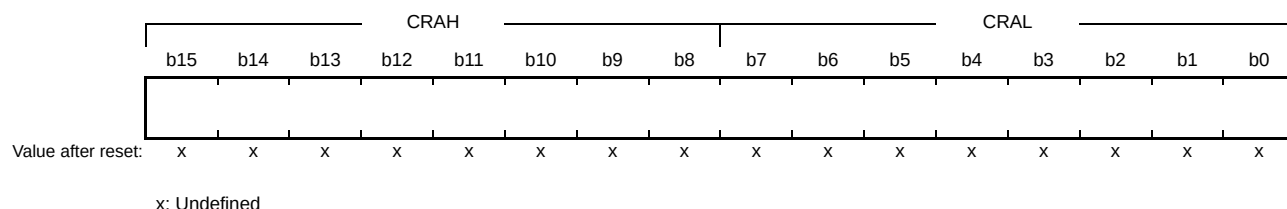
- Normal transfer mode

Address(es): (inaccessible directly from the CPU)



- Repeat transfer mode/block transfer mode

Address(es): (inaccessible directly from the CPU)



Symbol	Register Name	Description	R/W
CRAL	Transfer Counter A Lower Register	Set transfer count. This register functions as a transfer counter during data transfer.	—
CRAH	Transfer Counter A Upper Register	Set transfer count. This register functions as a reload register during data transfer.	—

Note: The function depends on transfer mode.

Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

This register is for counting the number of transfers and cannot be accessed directly from the CPU.

(1) Normal transfer mode (MRA.MD[1:0] bits = 00b)

CRA register functions as a 16-bit transfer counter in normal transfer mode.

The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively.

The CRA value is decremented (–1) at each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] bits = 01b)

The CRAH register retains the transfer count and the CRAL register functions as an 8-bit transfer counter.

The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.

The CRAL value is decremented (–1) at each data transfer. When it reaches 00h, the CRAH value is reloaded to the CRAL register.

(3) Block transfer mode (MRA.MD[1:0] bits = 10b)

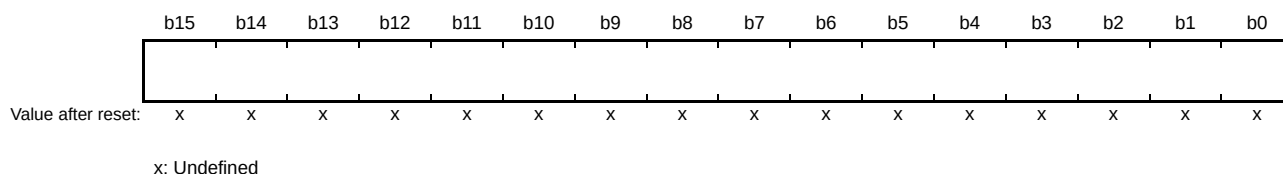
The CRAH register retains the block size and the CRAL register functions as an 8-bit block size counter.

The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively.

The CRAL value is decremented (–1) at each data transfer. When it reaches 00h, the CRAH value is reloaded to the CRAL register.

19.2.6 DTC Transfer Count Register B (CRB)

Address(es): (inaccessible directly from the CPU)



CRB register is used to set the block transfer count for block transfer mode and cannot be accessed directly from the CPU.

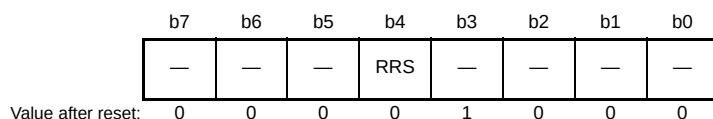
The transfer count is 1, 65535, and 65536 when the set value is 0001h, FFFFh, and 0000h, respectively.

The CRB value is decremented (–1) when the final data of a single block size is transferred.

When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

19.2.7 DTC Control Register (DTCCR)

Address(es): DTC.DTCCR 0008 2400h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Information Read Skip Enable	0: Transfer information read is not skipped. 1: Transfer information read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCCR register is used to control the DTC operation.

RRS Bit (DTC Transfer Information Read Skip Enable)

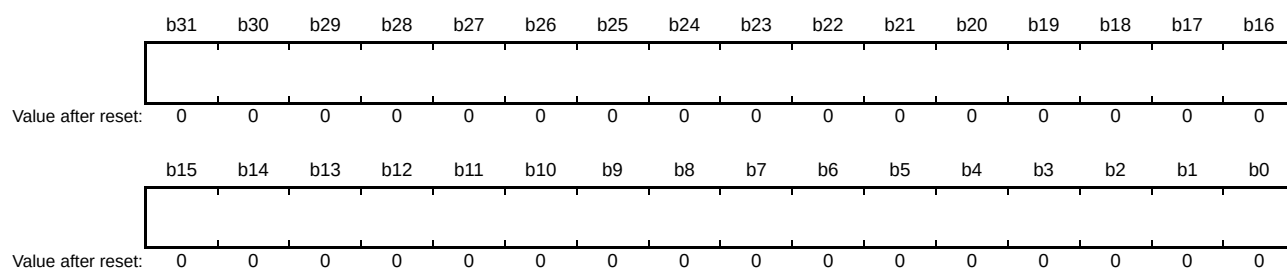
The DTC vector number is compared with the vector number in the previous data transfer.

When these vector numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transferred information. However, when the previous transfer was chain transfer, the transferred information is read regardless of the value of the RRS bit.

Furthermore, when the transfer counter (CRA register) became 0 during the previous normal transfer and when the transfer counter (CRB register) became 0 during the previous block transfer, the transferred information is read regardless of the RRS bit value.

19.2.8 DTC Vector Base Register (DTCVBR)

Address(es): DTC.DTCVBR 0008 2404h

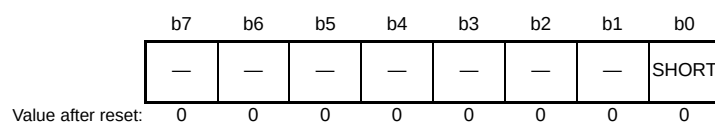


The DTCVBR register is used to set the base address for calculating the address to which the DTC vector is allocated. Values for the upper 4 bits (b31 to b28) cannot be written but reflect the value written to b27. The lower 10 bits are reserved and the values are fixed to 0. Write 0 to the lower 10 bits if necessary.

It can be set in the range of 0000 0000h to 07FF FC00h and F800 0000h to FFFF FC00h in 1-Kbyte units.

19.2.9 DTC Address Mode Register (DTCADMOD)

Address(es): DTC.DTCADMOD 0008 2408h



Bit	Symbol	Bit Name	Description	R/W
b0	SHORT	Short-Address Mode Set	0: Full-address mode 1: Short-address mode	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCADMOD register is used to specify the area accessible by the DTC.

SHORT Bit (Short-Address Mode Set)

This bit is used to select address mode of registers SAR and DAR.

Full-address mode allows the DTC to access to a 4-Gbyte space (0000 0000h to FFFF FFFFh).

Short-address mode allows the DTC to access to a 16-Mbyte space (0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh).

19.2.10 DTC Module Start Register (DTCST)

Address(es): DTC.DTCST 0008 240Ch

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	DTCST
0	0	0	0	0	0	0	0

Value after reset:

Bit	Symbol	Bit Name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module stop 1: DTC module start	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST Bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When this bit is set to 0, transfer requests are no longer accepted.

If this bit is set to 0 during data transfer, the accepted transfer request is active until the processing is completed.

Set the DTCST bit to 0 before making a transition to the module stop state, deep sleep mode, or software standby mode.

Set the DTCST bit to 1 to resume the data transfer after returning from the module stop state, deep sleep mode, or software standby mode.

For details on transitions to the module stop state, deep sleep mode, and software standby mode, refer to section 19.9, Low Power Consumption Function, and section 11, Low Power Consumption.

19.2.11 DTC Status Register (DTCSTS)

Address(es): DTC.DTCSTS 0008 240Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	VECN[7:0]	DTC Active Vector Number Monitoring Flag	These bits indicate the vector number for the request source when data transfer is in progress. The value is only valid if data transfer is in progress (the value of the ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15	ACT	DTC Active Flag	0: Data transfer is not in progress. 1: Data transfer is in progress.	R

VECN[7:0] Flags (DTC Active Vector Number Monitoring Flag)

While data transfer is in progress, these bits indicate the vector number corresponding to the request source for the transfer.

When the DTCSTS register is read, the value of the VECN[7:0] flags is valid if the value of the ACT flag was 1 (data transfer is in progress) and invalid if the value of the ACT flag was 0 (data transfer is not in progress).

For the correspondence between the DTC request sources and the vector addresses, refer to section 15.3.1, Interrupt Vector Table in section 15, Interrupt Controller (ICUb).

ACT Flag (DTC Active Flag)

This flag indicates the state of data transfer operation.

[Setting condition]

- When the data transfer is started by a transfer request.

[Clearing condition]

- When the data transfer is completed in response to a transfer request.

19.3 Request Sources

The DTC data transfer is triggered by an interrupt request. Setting the ICU.DTCERn.DTCE bit (n = interrupt vector number) to 1 selects the corresponding interrupt request as a request source for the DTC.

For the correspondence between the DTC request sources and the vector addresses, refer to section 15.3.1, Interrupt Vector Table in section 15, Interrupt Controller (ICUb). For request by software, refer to section 15.2.5, Software Interrupt Generation Register (SWINTR) in section 15, Interrupt Controller (ICUb).

Once the DTC has accepted a transfer request, it does not accept another transfer request until transfer for that single request is completed, regardless of the priority of the requests.

When multiple transfer requests are generated during data transfer by the DMAC/DTC, the request with the highest priority on completion of the current transfer is accepted. When multiple transfer requests are generated while the DTCST.DTCST bit is 0 (DTC module stop), the request with the highest priority at the moment when the bit is subsequently set to 1 (DTC module start) is accepted.

The DTC performs the following operations at the start of a single data transfer (or the last of the consecutive transfers in the case of a chain transfer).

- On completion of a specified number of data transfer, the ICU.DTCERn.DTCE bit is set to 0 and an interrupt is requested to the CPU.
- If the MRB.DISEL bit is 1, an interrupt is requested to the CPU on completion of data transfer.
- For the other transfers, the interrupt status flag of the request source is set to 0 at the start of data transfer.

19.3.1 Allocating Transfer Information and DTC Vector Table

The DTC reads the start address of the transfer information corresponding to each request source from the vector table and reads the transfer information starting at that address.

The vector table should be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC vector base register (DTCVBR) to set the base address of the DTC vector table.

Transfer information is allocated in the RAM area. The start address of the transfer information n with vector number n should be allocated at $DTCVBR + 4n$.

Transfer information should be aligned on a 4-byte boundary. The size of a transfer information is 12 bytes in short-address mode or 16 bytes in full-address mode. Use the DTCADMOD.SHORT bit to select short-address mode (SHORT bit = 1) or full-address mode (SHORT bit = 0).

Figure 19.2 shows the relationship between the DTC vector table and transfer information.

Figure 19.3 shows the allocation of transfer information in the RAM area. The lower addresses vary according to the endian of the corresponding allocation area. For details, refer to section 19.10.2, Allocating Transfer Information.

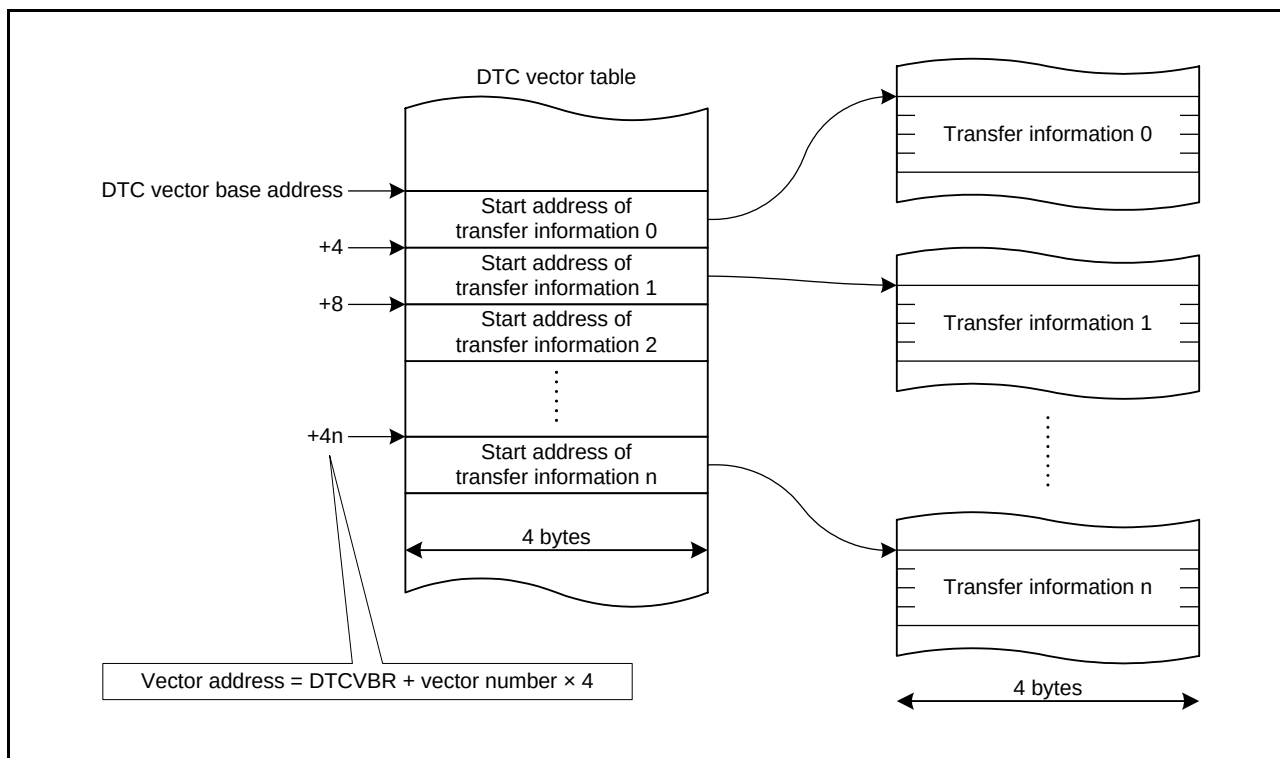


Figure 19.2 DTC Vector Table and Transfer Information

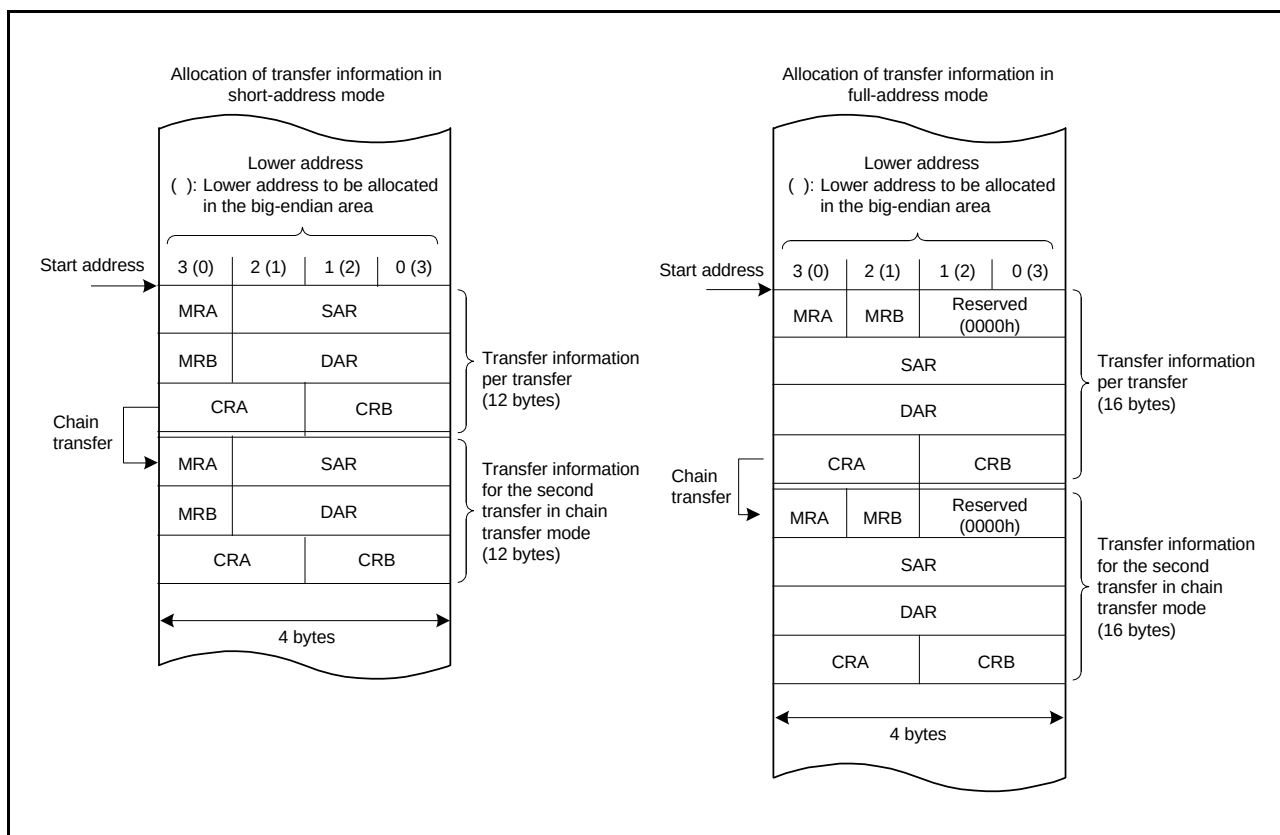


Figure 19.3 Allocation of Transfer Information in the RAM Area

19.4 Operation

The DTC transfers data in accordance with the transfer information. Storage of the transfer information in the RAM area is required before DTC operation.

When the DTC accepts a transfer request, it reads the DTC vector corresponding to the vector number. Next, the DTC reads transfer information from the address pointed by the DTC vector, transfers data, and then writes back the transfer information after the data transfer. Allocating transfer information in the RAM area allows data transfer of arbitrary number of channels.

There are three transfer modes: normal transfer mode, repeat transfer mode, and block transfer mode.

Set a transfer source address in the SAR register and a transfer destination address in the DAR register. The SAR and DAR registers are updated after the transfer according to the respective settings (increment, decrement, or fixed).

Table 19.2 lists transfer modes of the DTC.

Table 19.2 Transfer Modes of the DTC

Transfer Mode	Data Size Transferred on Single Transfer Request	Increment/Decrement of Memory Address	Settable Transfer Count
Normal transfer mode	1 byte/1 word/1 longword	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536
Repeat transfer mode*1	1 byte/1 word/1 longword	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes/1 to 256 words/1 to 256 longwords)	Incremented/decremented by 1, 2, or 4 or address fixed	1 to 65536

Note 1. Set transfer source or transfer destination in the repeat area.

Note 2. Set transfer source or transfer destination in the block area.

Note 3. After data transfer of the specified count, the initial state is restored and the operation is continued (repeated).

Setting the MRB.CHNE bit to 1 allows multiple transfers (chain transfer) on a single transfer request. The setting in combination with the MRB.CHNS bit enables a chain transfer when the specified number of data transfers is completed. Figure 19.4 shows the operation flowchart of the DTC. Table 19.3 lists chain transfer conditions.