

Port1_10M_3555MHz_TM3.1_CHL_CSE0a



Port1_10M_3555MHz_TM3.1_CHL_CSE0b



Port1_10M_3555MHz_TM3.1_CHL_CSE1



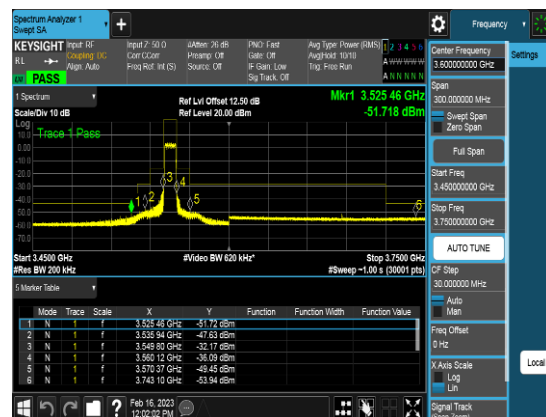
Port1_10M_3555MHz_TM3.1_CHL_CSE2



Port1_10M_3555MHz_TM3.1_CHL_CSE3



Port1_10M_3555MHz_TM3.1_CHL_CSEpart96



Port1_10M_3624.99MHz_TM3.1_CHM_CSE0a



Port1_10M_3624.99MHz_TM3.1_CHM_CSE0b



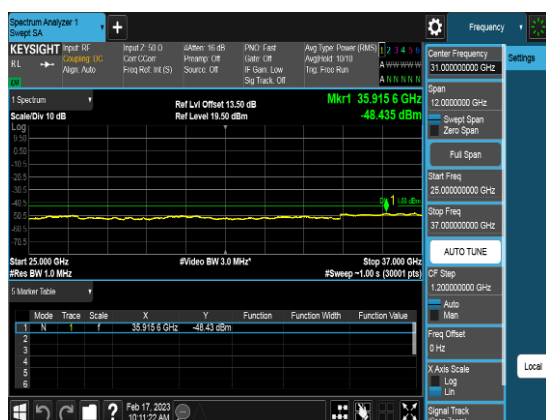
Port1_10M_3624.99MHz_TM3.1_CHM_CSE1



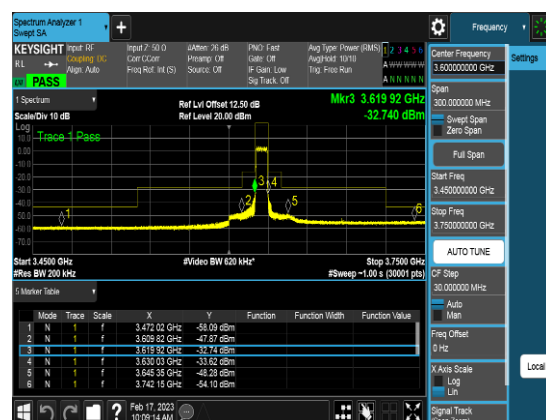
Port1_10M_3624.99MHz_TM3.1_CHM_CSE2



Port1_10M_3624.99MHz_TM3.1_CHM_CSE3



Port1_10M_3624.99MHz_TM3.1_CHM_CSEpart 96



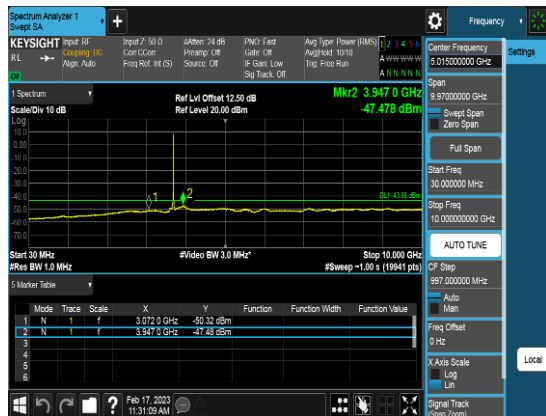
Port1_10M_3694.98MHz_TM3.1_CHH_CSE0a



Port1_10M_3694.98MHz_TM3.1_CHH_CSE0b



Port1_10M_3694.98MHz_TM3.1_CHH_CSE1



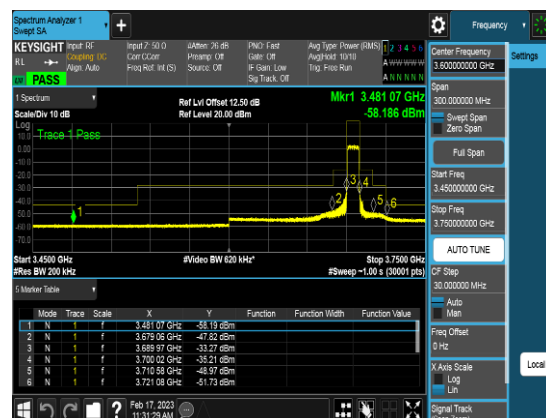
Port1_10M_3694.98MHz_TM3.1_CHH_CSE2



Port1_10M_3694.98MHz_TM3.1_CHH_CSE3



Port1_10M_3694.98MHz_TM3.1_CHH_CSEpart9
6



Port1_20M_3560.01MHz_TM3.1_CHL_CSE0a



Port1_20M_3560.01MHz_TM3.1_CHL_CSE0b



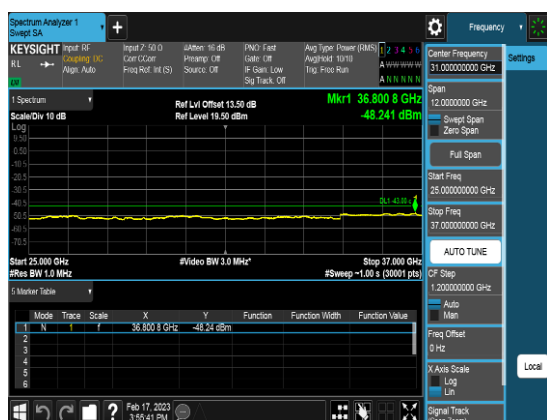
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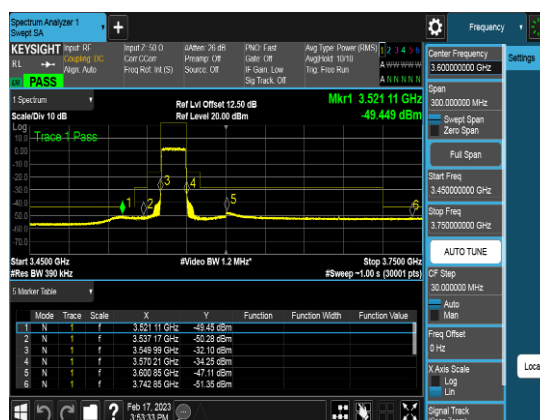
Port1_20M_3560.01MHz_TM3.1_CHL_CSE2



Port1_20M_3560.01MHz_TM3.1_CHL_CSE3



Port1_20M_3560.01MHz_TM3.1_CHL_CSEpart9
6



Port1_20M_3624.99MHz_TM3.1_CHM_CSE0a



Port1_20M_3624.99MHz_TM3.1_CHM_CSE0b



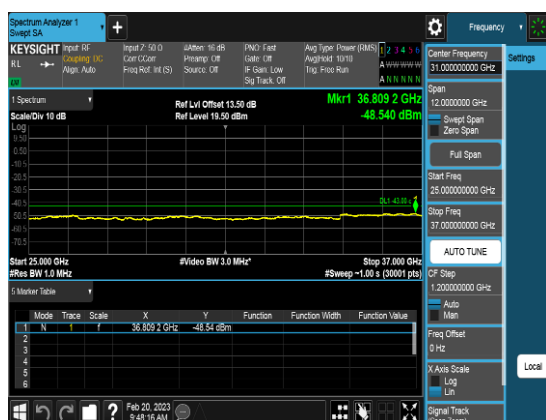
Port1_20M_3624.99MHz_TM3.1_CHM_CSE1



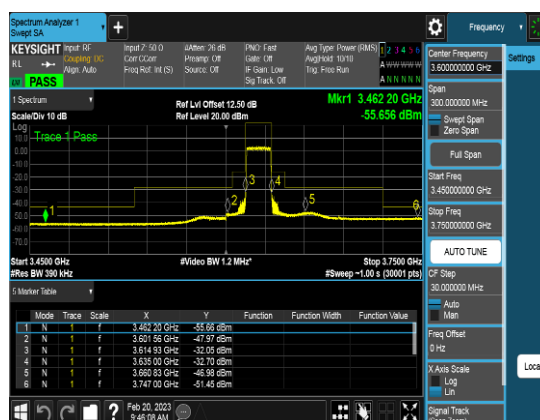
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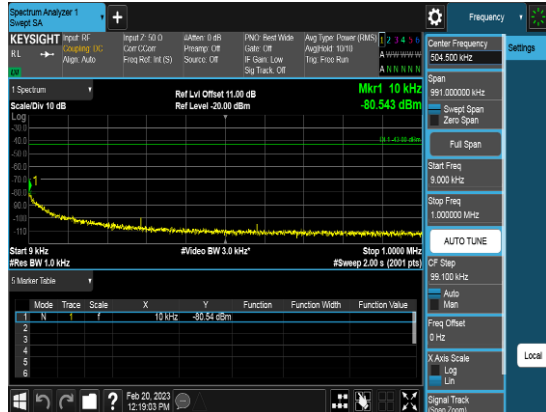
Port1_20M_3624.99MHz_TM3.1_CHM_CSE3



Port1_20M_3624.99MHz_TM3.1_CHM_CSEpart 96



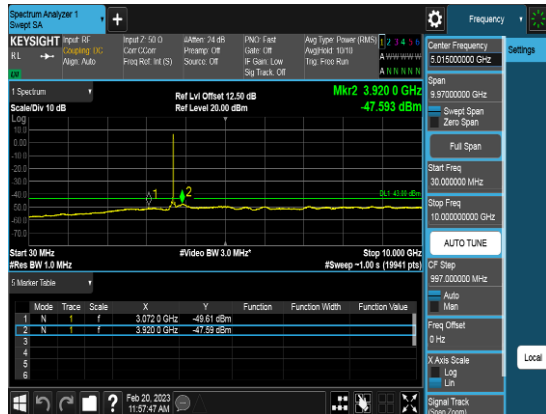
Port1_20M_3690MHz_TM3.1_CHH_CSE0a



Port1_20M_3690MHz_TM3.1_CHH_CSE0b



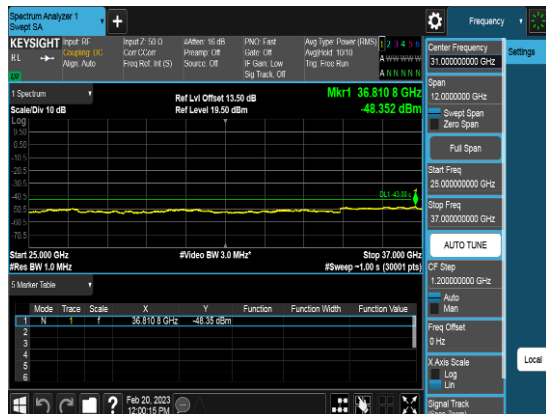
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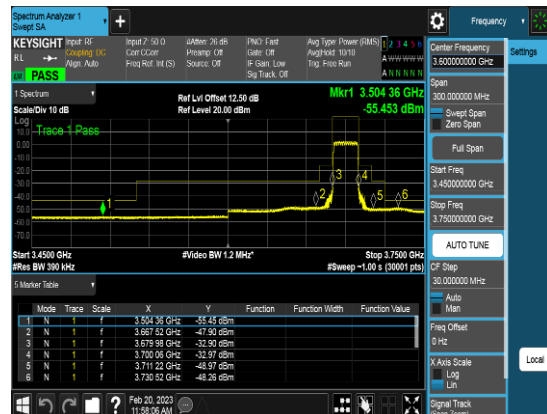
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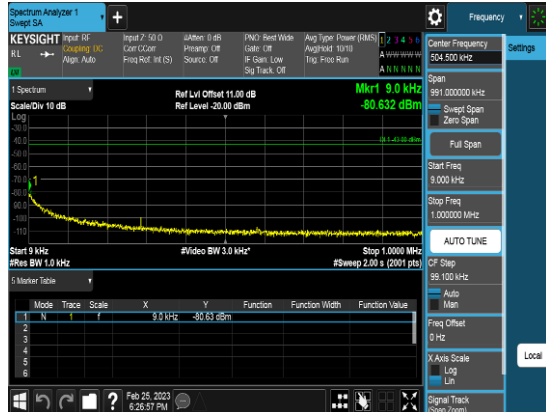
Port1_20M_3690MHz_TM3.1_CHH_CSE3



Port1_20M_3690MHz_TM3.1_CHH_CSEpart96



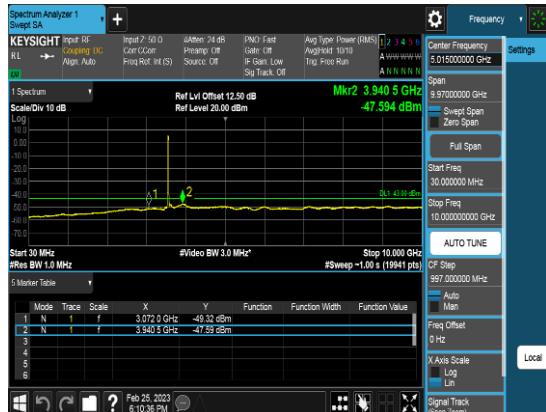
Port1_30M_3565.02MHz_TM3.1_CHL_CSE0a



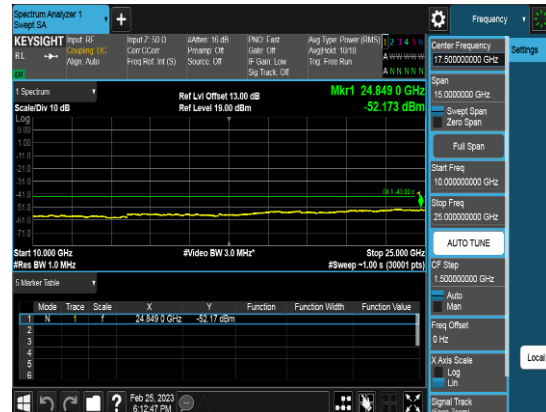
Port1_30M_3565.02MHz_TM3.1_CHL_CSE0b



Port1_30M_3565.02MHz_TM3.1_CHL_CSE1



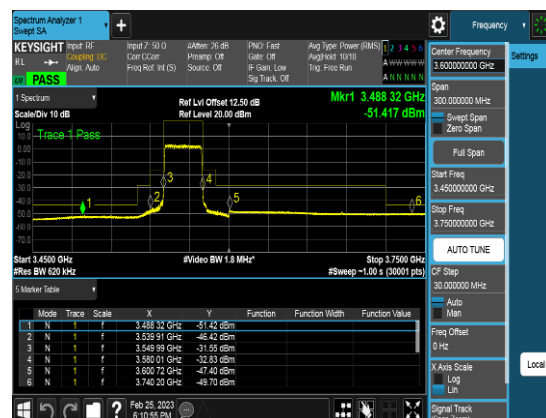
Port1_30M_3565.02MHz_TM3.1_CHL_CSE2



Port1_30M_3565.02MHz_TM3.1_CHL_CSE3



Port1_30M_3565.02MHz_TM3.1_CHL_CSEpart9
6



Port1_30M_3624.99MHz_TM3.1_CHM_CSE0a



Port1_30M_3624.99MHz_TM3.1_CHM_CSE0b



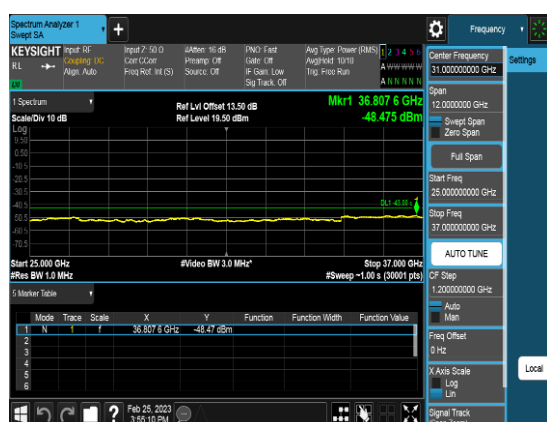
Port1_30M_3624.99MHz_TM3.1_CHM_CSE1



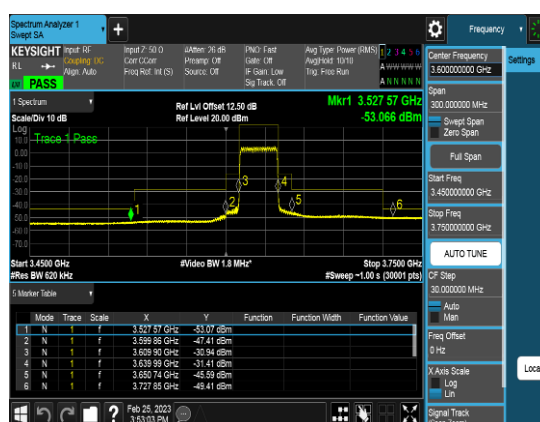
Port1_30M_3624.99MHz_TM3.1_CHM_CSE2



Port1_30M_3624.99MHz_TM3.1_CHM_CSE3



Port1_30M_3624.99MHz_TM3.1_CHM_CSEpart 96



Port1_30M_3684.99MHz_TM3.1_CHH_CSE0a



Port1_30M_3684.99MHz_TM3.1_CHH_CSE0b



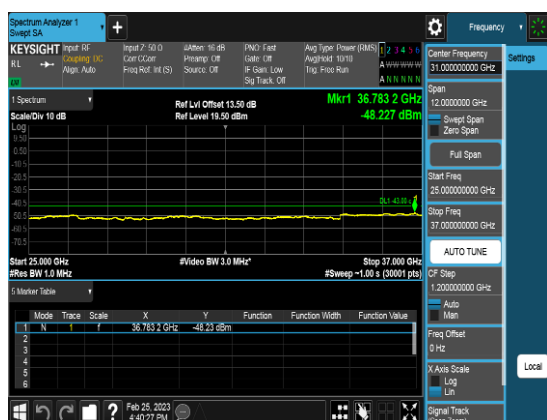
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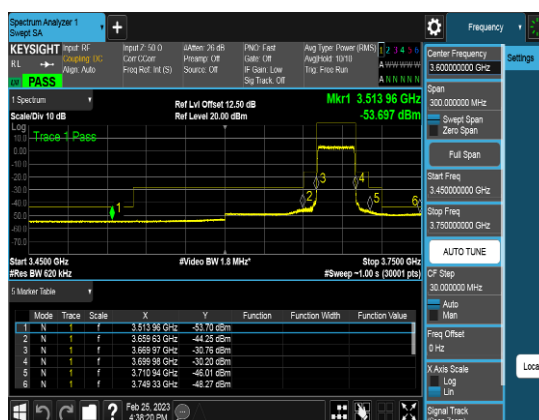
Port1_30M_3684.99MHz_TM3.1_CHH_CSE2



Port1_30M_3684.99MHz_TM3.1_CHH_CSE3



Port1_30M_3684.99MHz_TM3.1_CHH_CSEpart9
6



Port1_40M_3570MHz_TM3.1_CHL_CSE0a



Port1_40M_3570MHz_TM3.1_CHL_CSE0b



Port1_40M_3570MHz_TM3.1_CHL_CSE1



Port1_40M_3570MHz_TM3.1_CHL_CSE2



Port1_40M_3570MHz_TM3.1_CHL_CSE3



Port1_40M_3570MHz_TM3.1_CHL_CSEpart96



Port1_40M_3624.99MHz_TM3.1_CHM_CSE0a



Port1_40M_3624.99MHz_TM3.1_CHM_CSE0b



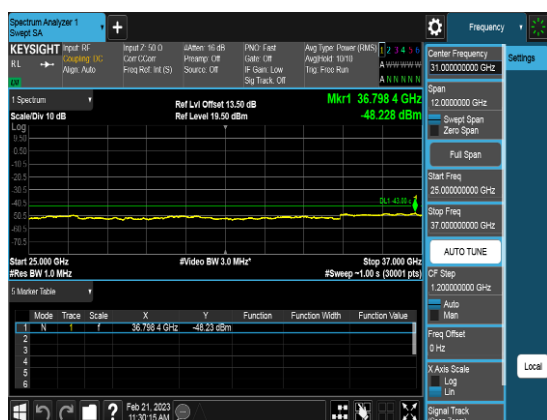
Port1_40M_3624.99MHz_TM3.1_CHM_CSE1



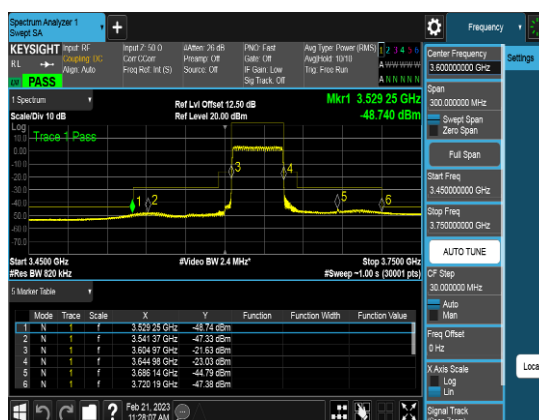
Port1_40M_3624.99MHz_TM3.1_CHM_CSE2



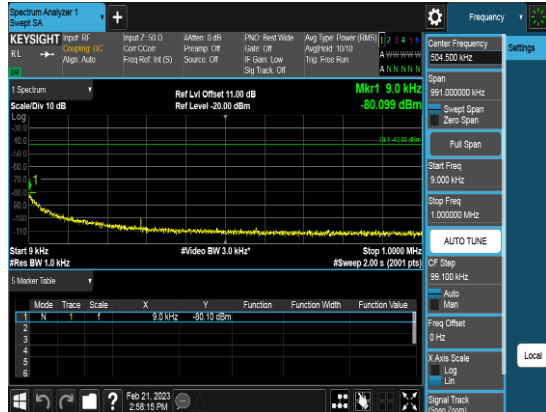
Port1_40M_3624.99MHz_TM3.1_CHM_CSE3



Port1_40M_3624.99MHz_TM3.1_CHM_CSEpart 96



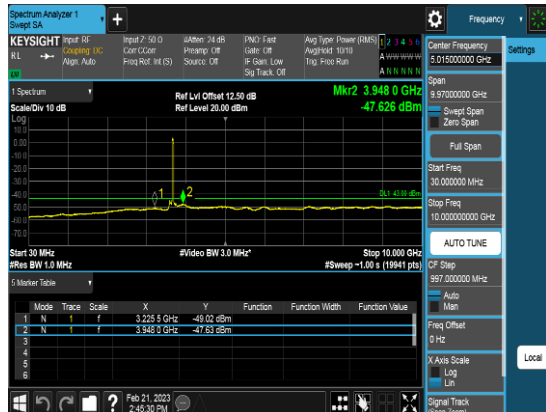
Port1_40M_3679.98MHz_TM3.1_CHH_CSE0a



Port1_40M_3679.98MHz_TM3.1_CHH_CSE0b



Port1_40M_3679.98MHz_TM3.1_CHH_CSE1



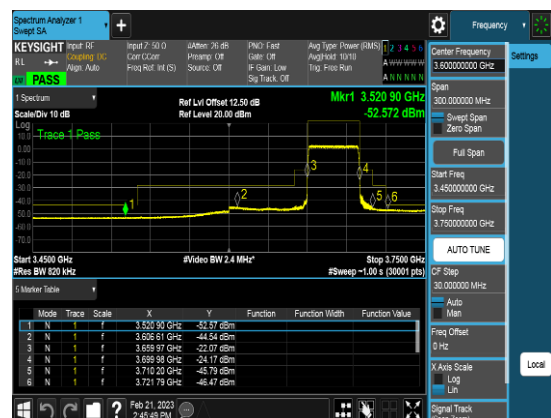
Port1_40M_3679.98MHz_TM3.1_CHH_CSE2



Port1_40M_3679.98MHz_TM3.1_CHH_CSE3



Port1_40M_3679.98MHz_TM3.1_CHH_CSEpart9
6



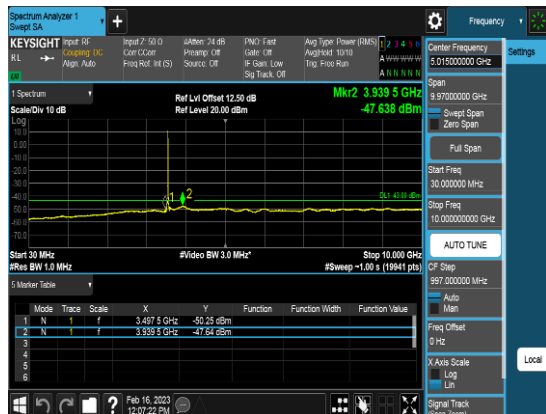
Port2_10M_3555MHz_TM3.1_CHL_CSE0a



Port2_10M_3555MHz_TM3.1_CHL_CSE0b



Port2_10M_3555MHz_TM3.1_CHL_CSE1



Port2_10M_3555MHz_TM3.1_CHL_CSE2



Port2_10M_3555MHz_TM3.1_CHL_CSE3



Port2_10M_3555MHz_TM3.1_CHL_CSEpart96

