

Datasheet of Bluetooth BM79BLETRMC2 Module

ISSC Technologies Corp.

Revision History

Date	Revision Content	Version
2013/06/24	First Version	0.9
2013/10/01	Final version	1.0

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1. Introduction

Part Name: ISSC BM79BLETRMC2 Bluetooth module

Part Number: BM79BLETRMC2-xxxxxx

The ISSC BM79BLETRMC2 Bluetooth module is design for Bluetooth standard BLE electronic accessories via Bluetooth connectivity. It is available in the 2.4GHz ISM band Class 2 Radio, compatible with Bluetooth Core Specification Version 4.0 BLE. ISSC IS1679SM single chip solution combines transceiver and baseband function to decrease the external components. It narrows down the module size and minimizes its cost. The optimized power design minimizes power consumption to extend battery using period.

1.1. Major Components

- ISSC IS1679SM (40 pin QFN, single-chip Bluetooth transceiver and baseband processor)
- Serial EEPROM 8K (1024*8) TSSOP 8P

1.2. Features

- Bluetooth 4.0 BLE compliant
- RSSI
- UART Transparent
- Low power 1.8V RF operation
- RF transmitter output power Class 2
- RF receiver sensitivity: -92dBm@ BLE, in typical.
- Internal ROM and 4Mibts of flash
- I2C compatible interface
- 1 LED driver

1.3. Application

- Health care
- LED Control / Lighting
- RC Toys
- Electrical Scale
- Blood Pressure Monitors
- Industrial Applications (CNC, PLC, RFID)

Product Specification

1.4. Chipset

6x6 mm² 40 pin QFN IS1679SM

1.5. Interfaces

- Multi function GPIO interface
- Bluetooth RF interface
- UART up to 921600 bps
- I2C for external EEPROM and authentication chip

1.6. Hardware Design Considerations

- Power

The module requires 4.2 - 3.3V

- Power ramp-up timing restriction

- 1) BAT_IN : ramp-up (0 to 1.6V) < 200ms
- 2) PMULDO_O : PMU-logic ramp-up (0 to 1.6V) < 60ms
- 3) VCC_RF (1.8V power domain) : RF BPOR ramp-up (0 to 1.6V) < 20ms

- Power on sequence (See Fig 1 for detail)

- 1) BAT_IN: must be first!
- 2) 3.3V power domain: VDD_IO/ VDD_FIO must power-up early than 1.8V power.
- 3) 1.8V power domain: 1V8/ VCC_RF/ VDD_XO/ 1V8_U_P
- 4) RST_N: digital reset released from 0 to 1.6V must be the last one.

- Recommended operating conditions

Rating	Min	Typ	Max
VDD_IO_x,	3.1V		3.63V
SW_BTN	3.2V		4.3V
BAT_IN	3.2V		4.3V

- Clock Sources

A high accuracy crystal with ± 10 ppm tolerance is connected to the BM79BLETRMC2 clock input pins.

- Serial Flash and Firmware Version

Firmware code is stored on chip internal flash.

- Radio Characteristics

Frequency Band: 2402-2480 GHz

Number of Channels:

Low Energy
40 MHz channels (2MHz)

- Current Consumption (It is the average current consumption and measured by FLUKE multi-meter)

Low Energy (BAT_IN = 3.7V & UART RX_IND Function Enable)

Operation Mode	AVG current	Unit	Note
Standby mode (Advertising)	4.89	mA	Adv interval = 20ms
	0.97	mA	Adv interval = 160ms
	0.86	mA	Adv interval = 1000ms
Deep power down mode	0.102	mA	
Connected	2.76	mA	Connection interval = 20ms
	0.84	mA	Connection interval = 500ms
	0.81	mA	Connection interval = 1000ms
Connected with data transmit (20 bytes MCU data/Connection Event)	6.16	mA	Connection interval = 20ms
	1.12	mA	Connection interval = 500ms
	0.94	mA	Connection interval = 1000ms

- Terminal characteristics

Condition :	Min	Typ	Max	Unit
VDD_IO=3.3V				
I/O voltage levels				
V _{IL} input logic levels low	-0.3		0.8	V
V _{IH} input logic levels high	2.0		3.6	V
V _{OL} output logic levels low			0.4	V
V _{OH} output logic levels high	2.4			V
Reset terminal				
V _{TH,res} threshold voltage		1.6		V
Input and tri-state current with				
Pull-up Resistor		65		Kohm
Leakage current	-10		+10	μA
Vdd supply current				
TX mode			70	mA
RX mode			70	mA

- Baud Rate

Desired baud rate	Clock	Actual Baud rate	Error Rate %
921600	48000000	923077	0.16
460800	48000000	461538	0.16
230400	48000000	230769	0.16
115200	16000000	111888	-2.87
57600	16000000	58608	1.75
38400	16000000	38462	0.16
28800	16000000	28623	-0.62
19200	16000000	19231	0.16
14400	16000000	14480	0.55
9600	16000000	9615	0.16
4800	16000000	4808	0.16
2400	16000000	2399	-0.03

- Testing Criterion

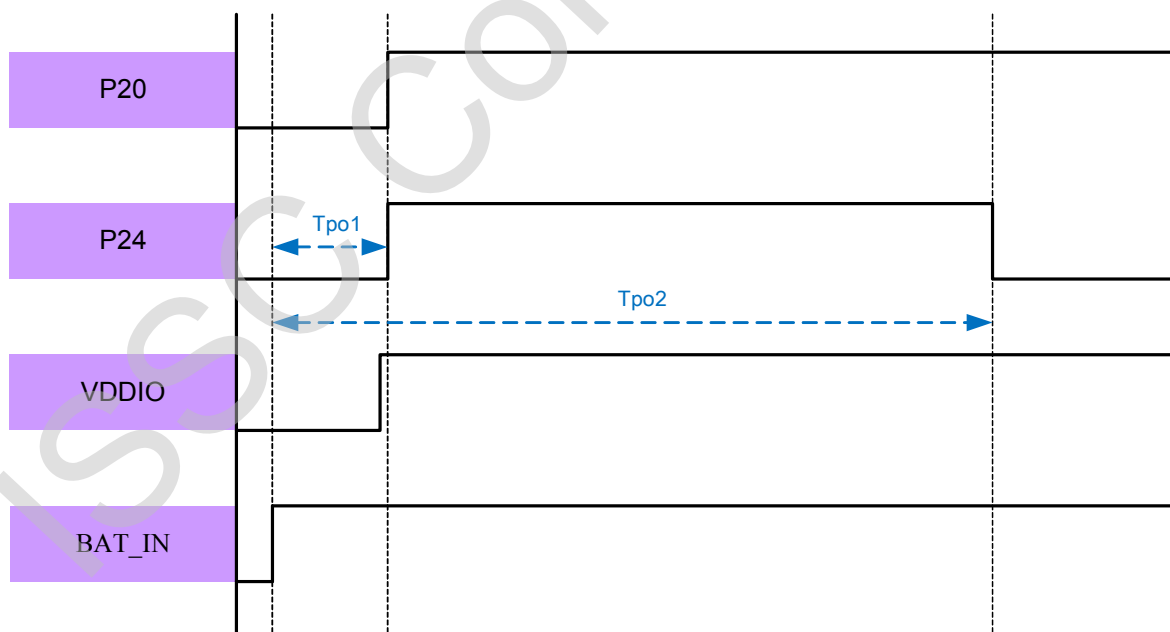
NO.	Testing Item Name	Spec.
1	Device Initialization	
2	System Verify	System Power>1.6V
3	PMU LDO trim	1.8~2.1
4	LDO18 Calibration	1.85~1.97V
5	LDO33 Calibration	3.1~3.4V
6	RF frequency calibration	< 10k Hz
7	RF TX power verify	> -5 dBm
8	8852 output power	-2dBm~+4dBm
9	Initial carrier test	+/- 30KHz
10	Single slot sensitivity	> -70dBm
11	Multi slot sensitivity	> -70dBm
12	Modulation index test	$140\text{KHz} \leq f_{1\text{avg}} \leq 175\text{KHz}$ $f_{2\text{max}} \geq 115\text{KHz}$ $f_2/f_{1\text{avg}} \geq 0.8$

- Timing Sequence

Timing Sequence for Mode selection Pin (P20, P24) under APP mode(For normally use)

Pin No.	I/O	Name	Description
2	I	BAT_IN	4.2V~3.2V power input
5	P	VDD_IO	Main power supply
16	I	P20	System configuration, refer to P2_4, MCU do NOT drive under APP Mode
17	I	P24	Boot mode selection (MCU NOT drive under APP Mode) P2_0/ P2_4: HH → Application LL → Boot mode LH → HCI UART mode for testing and system configuration.

	Min	Typ	Max	Unit
T_{po1}		4		ms
T_{po2}		24		ms



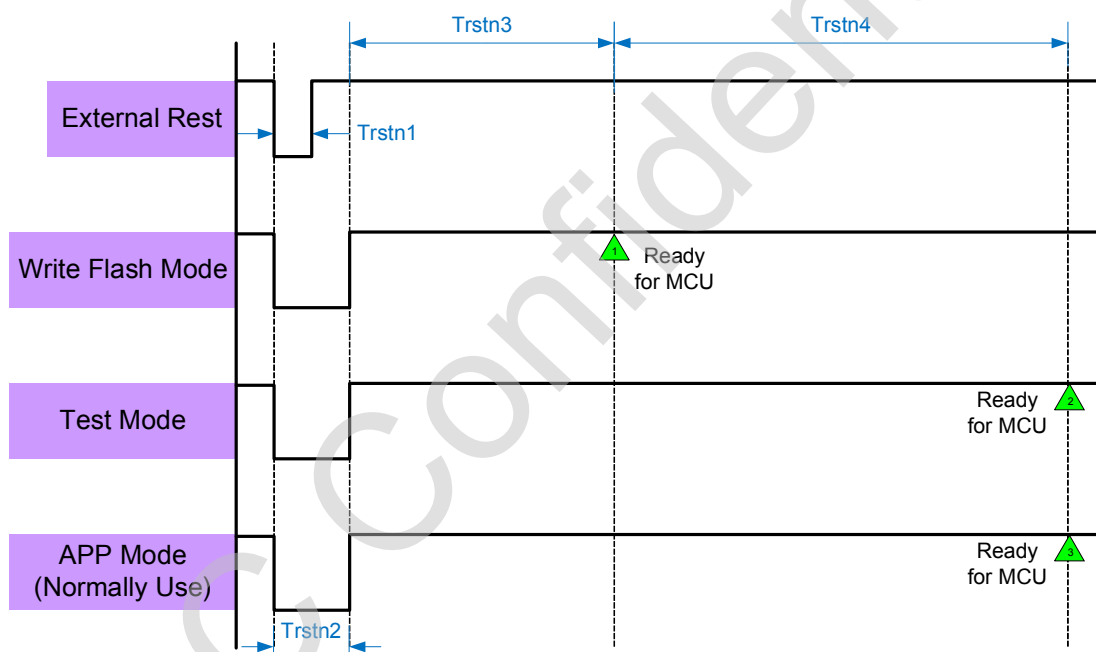
P20, P24 Mode Selection Timing Diagram

Fig. 1: Timing diagram of power ramp and P20/P24 mode selection

Timing Sequence for Rest Pin (RST_N) under three different modes

19	I	RST_N	External reset input (Low Active)
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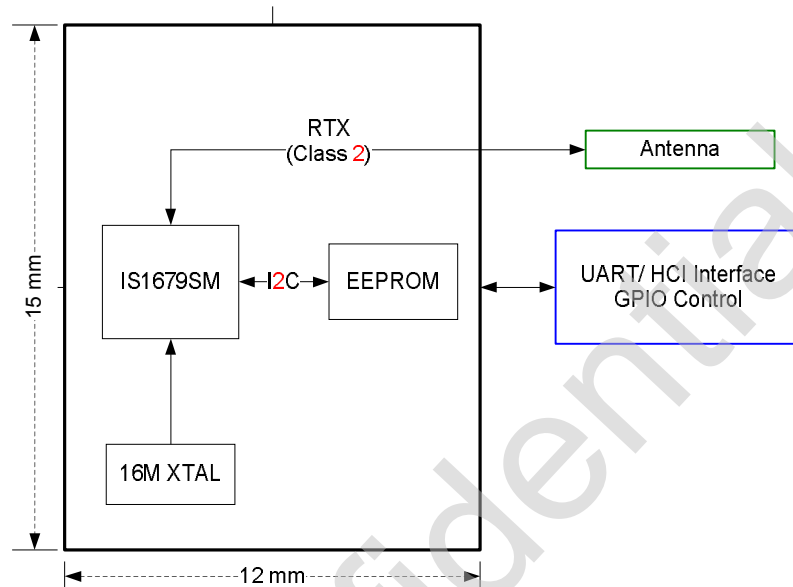
	Min	Typ	Max	Unit
T_{rstn1}	62.5			ns
T_{rstn2}		5		ms
T_{rstn3}		60		ms
T_{rstn4}		400		ms



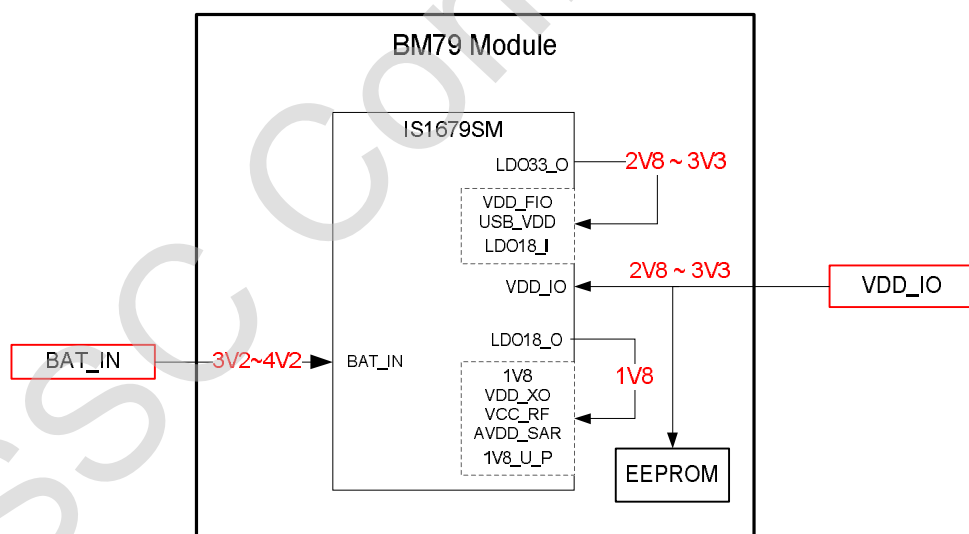
RST_N Timing Diagram

2. Hardware Architecture

Block Diagram



Power Tree



3. Compatibility Requirements

The BM79BLETRMC2 Bluetooth module shall pass the standard test plan, which includes hardware compatibility and reliability, and software compatibility test.

4. Environmental Requirements

4.1. Temperature

Conditions	Operating Temperature	Non-Operating Temperature
Minimum	-10 °C	-40°C
Maximum	+70 °C	+85 °C

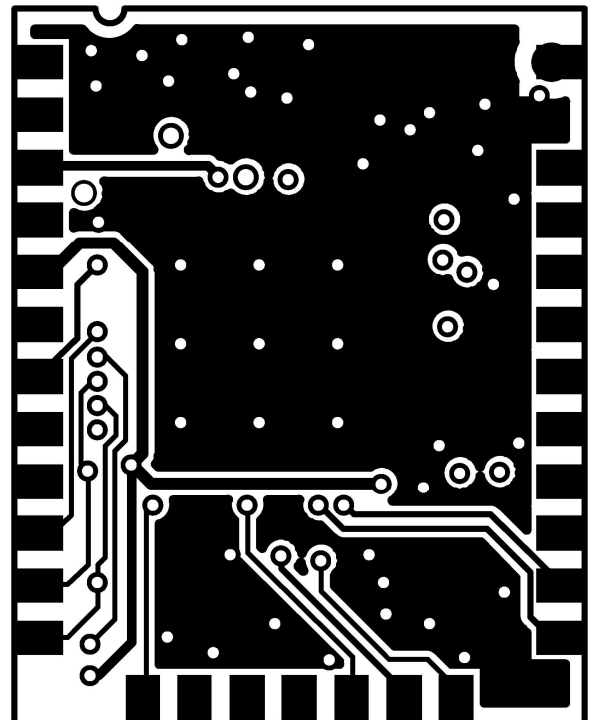
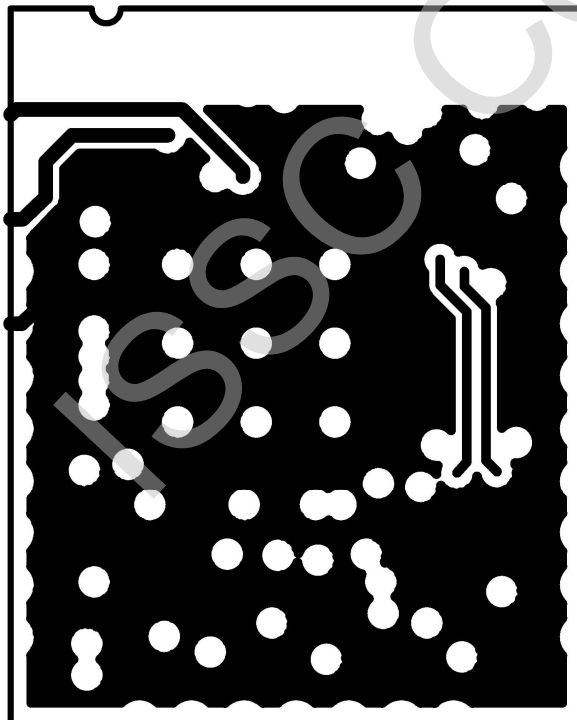
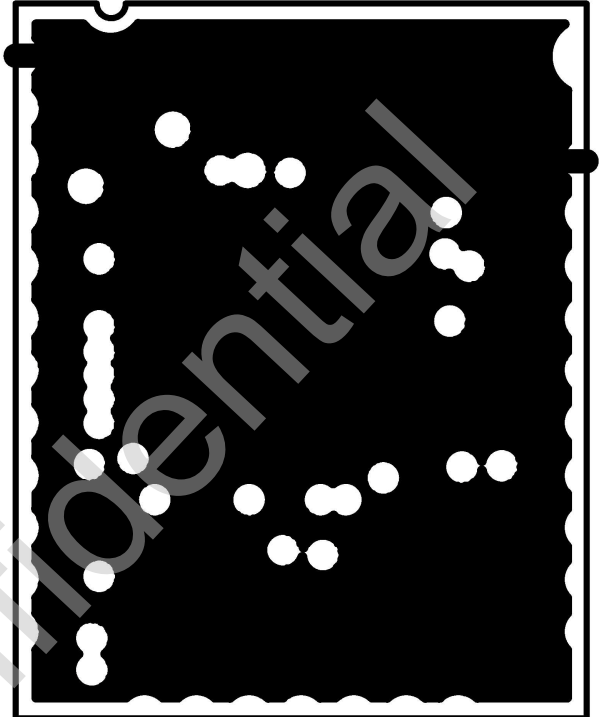
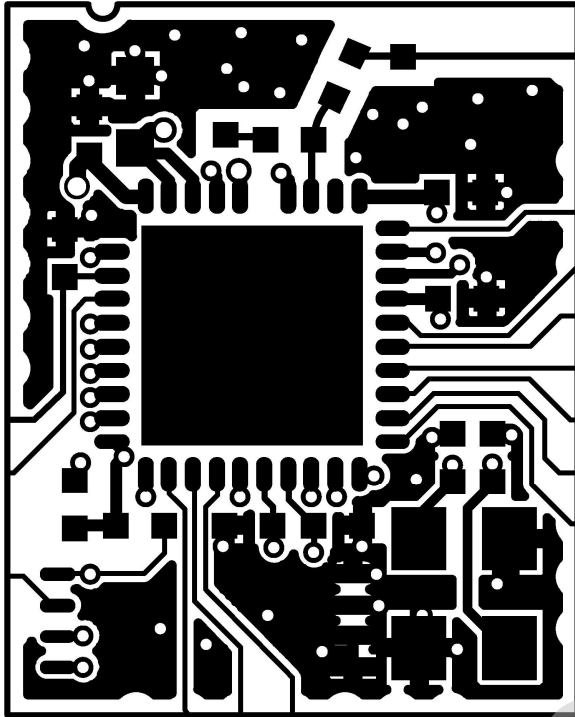
4.2. Humidity

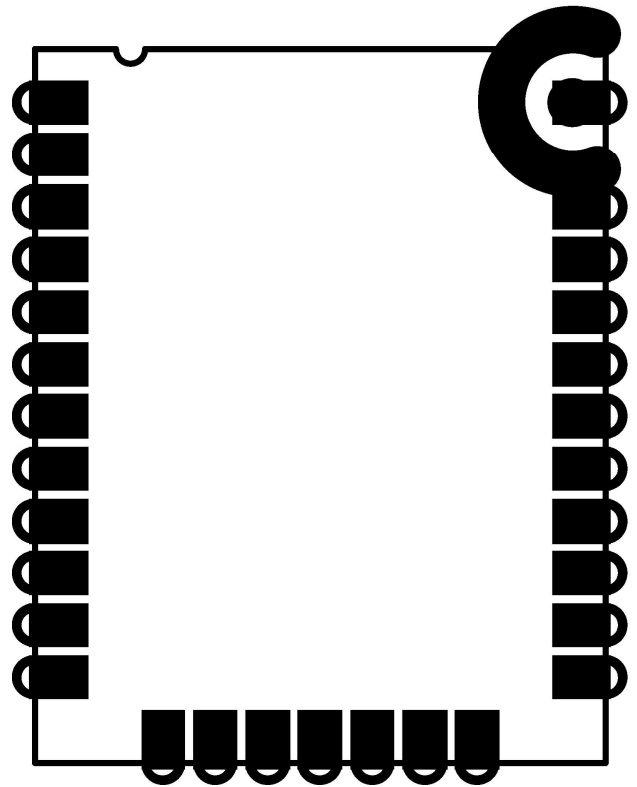
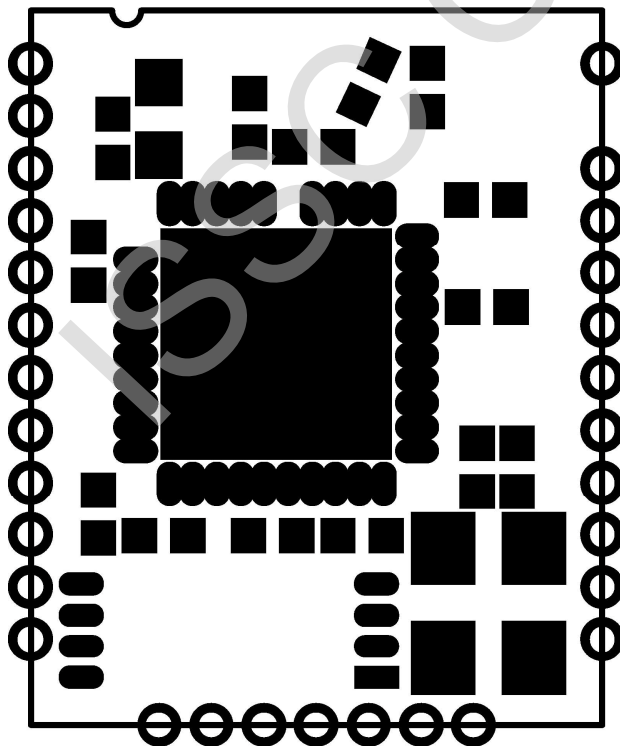
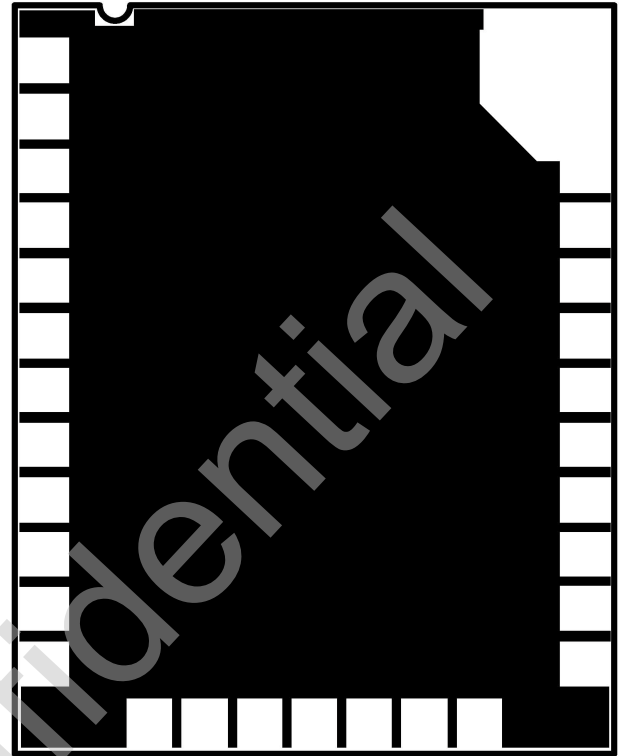
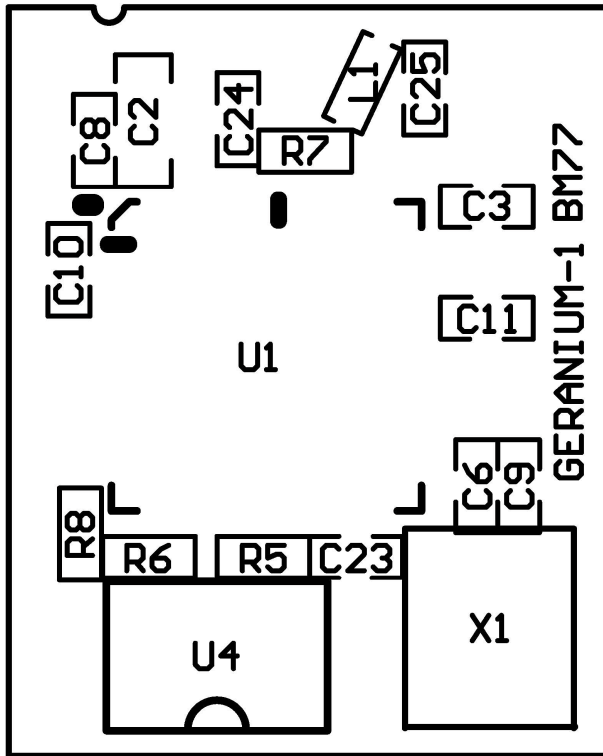
Conditions	Operating Humidity	Non-Operating Humidity
Minimum	10%	5%
Maximum	90%	95%

A rectangle is shown with a horizontal dimension of 15mm and a vertical dimension of 12. The dimensions are indicated by arrows and labels outside the rectangle.

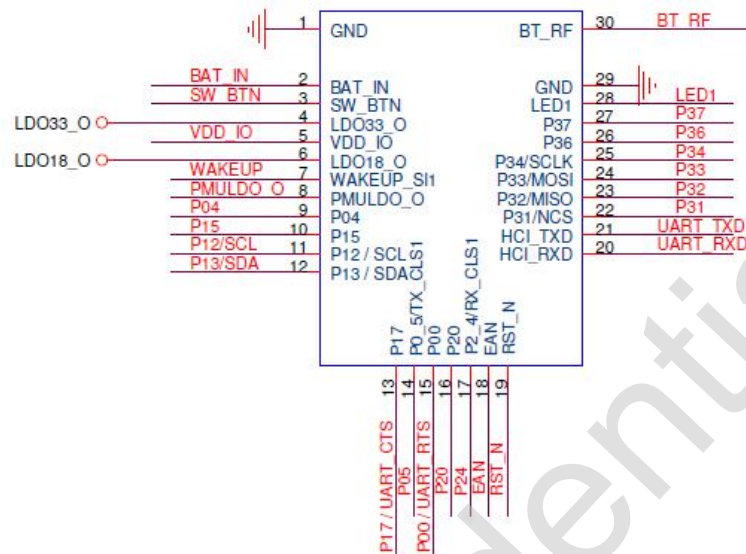
-
- Technical drawing of a microchip package showing dimensions and a warning.
- Dimensions (mm):
- Top width: 12.35
 - Left height: 15.7
 - Bottom width: 12
 - Right height: 15
 - Pin pitch (vertical): 1.27
 - Pin pitch (horizontal): 1.27
 - Pin width: 0.6
 - Pin spacing: 0.7
 - Pin length: 1.8
 - Pin thickness: 0.15
 - Pin diameter: 1.7
 - Pin diameter: 0.6
 - Pin diameter: 9.7
 - Pin diameter: 2.2
 - Pin diameter: 30
 - Pin diameter: 1.8
 - Pin diameter: 1.5
 - Pin diameter: 2.7
- Warning: Keep out Anything
- SIZE: 3.1mm x 3.0mm

Appendix C: Geber





Appendix D: PIN Assignment



P/N	I/O	Name	Description
1	P	GND	Ground
2	P	BAT_IN	4.2~3.3V power input
3	I	SW_BTN	Input for software button. H: Power on L: Power off
4	P	LDO33_O	3V3 LDO output
5	P	VDD_IO	Main power supply
6	P	LDO18_O	LDO18 output
7	I	WAKEUP	Wakeup BM79 from Shutdown state. (Low Active)
8	P	PMULDO_O	Output of PMULDO
9	O	P04	UART_TX_IND: H: BM79 indicate UART data will be transmitted out after a certain timing. (Setting by EEPROM, default 5ms) L: Otherwise. STATUS_IND_2: BM79 State indication , refer to P15

P/N	I/O	Name	Description
10	O	P15	STATUS_IND: Bluetooth link status indication P15/P04: HH → Power default and Shutdown state. P15/P04: HL → Access state. P15/P04: LL → Link State w/o UART_TXD. P15/P04: LH → Link State with UART_TXD.
11	N/A	P12/ SCL	I2C_SCL, for Authentication Coprocessor 2.0B/ C
12	N/A	P13/ SDA	I2C_SDA, for Authentication Coprocessor 2.0B/ C
13	I	P17	- UART_CTS: - Configurable Functional GPIO
14	I/O	P05	Configurable Functional GPIO
15	O	P00	- UART_RTS - Configurable Functional GPIO
16	I	P20	System configuration, refer to P2-4. (No drive under APP Mode)
17	I	P24	Boot mode selection. (No drive under APP Mode) P2-0/ P2-4: HH → Application(For normally use) LL → Boot mode LH → HCI UART mode for testing and system configuration.
18	I	EAN	ROM/Flash selection. (No drive under APP Mode) H: ROM code; L: Flash code
19	I	RST_N	External reset input (Low Active), reset pulse period must > 62.5ns
20	I	HCI_RXD	UART_RXD
21	O	HCI_TXD	UART_TXD
22	I/O	P31	Configurable functional GPIO.
23	I	P32	Configurable functional GPIO.
24	I	P33	Configurable functional GPIO.
25	I	P34	Configurable functional GPIO.
26	O	P36	CP_RST: Reset Authentication Coprocessor 2.0B/C
27	I/O	P37	Configurable functional GPIO
28	O	LED1	LED1 driver
29	P	GND	Ground
30	RI/O	BT_RF	RF port

Appendix E: Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217°C to peak): 1~2°C/sec max.

Preheat : 150~200°C 、 60~180 seconds

Temperature maintained above 217°C : 60~150 seconds

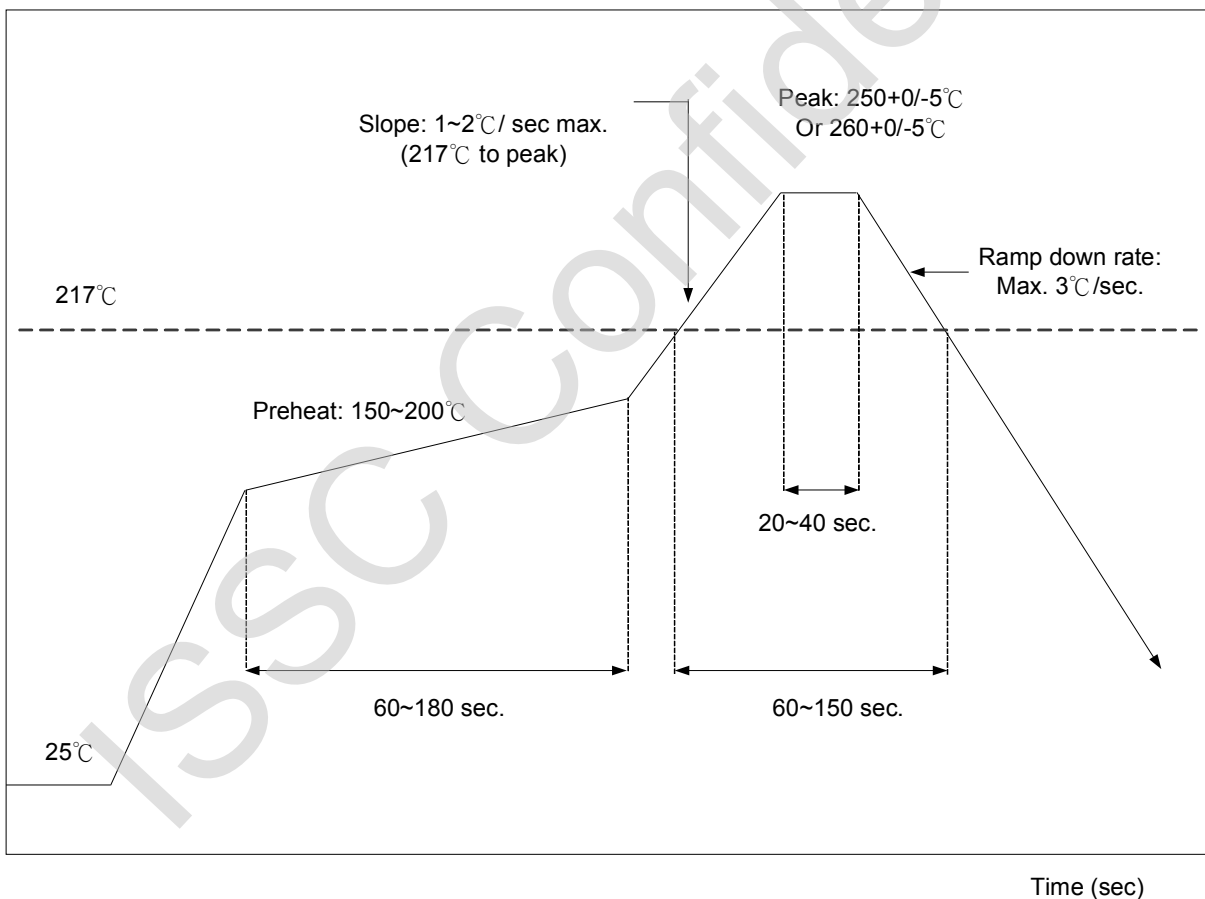
Time within 5°C of actual peak temperature: 20 ~ 40 sec.

Peak temperature : 250+0/-5°C or 260+0/-5°C

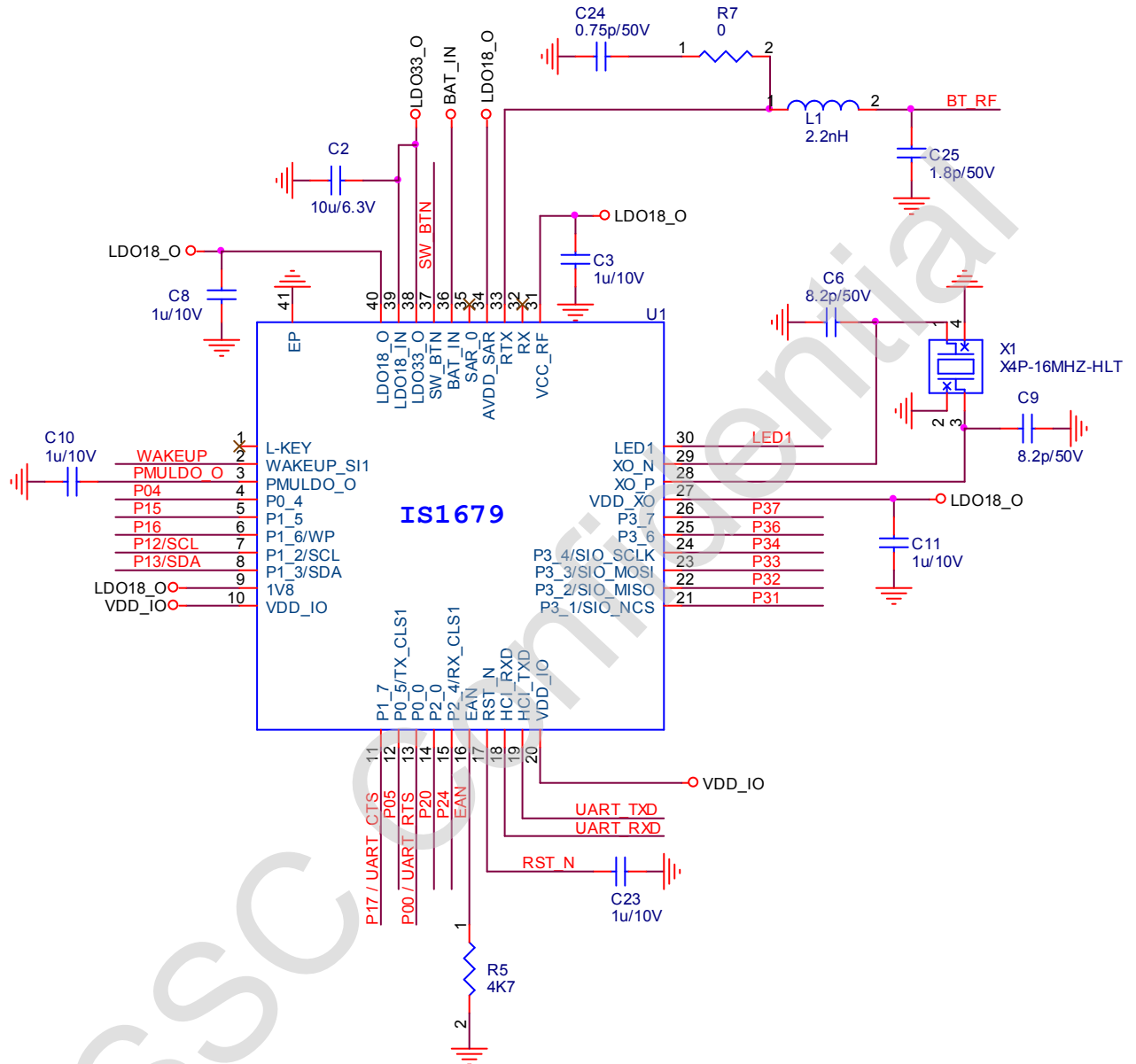
Ramp-down rate : 3°C/sec. max.

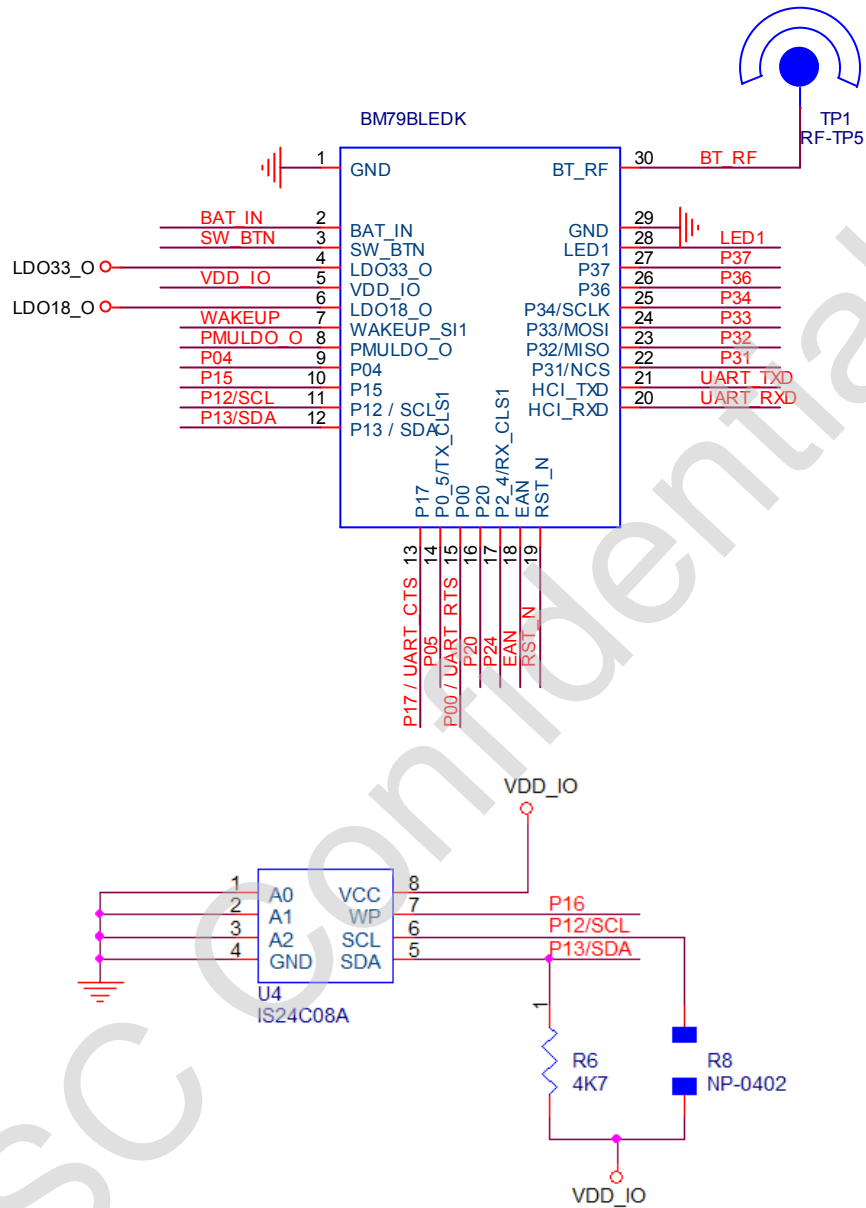
Time 25°C to peak temperature : 8 minutes max.

Cycle interval : 5 minus

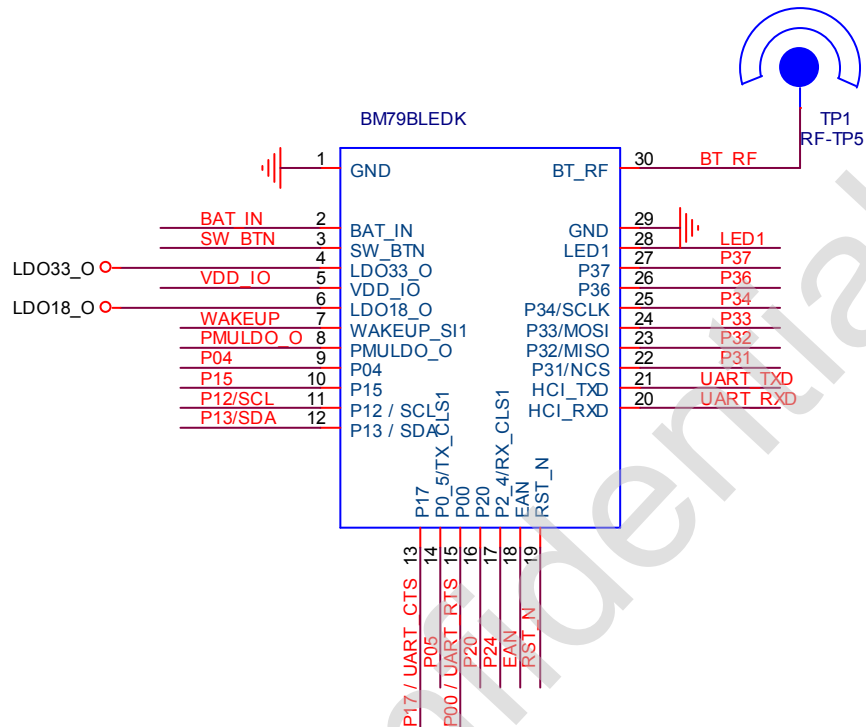


Appendix F: Schematic





Appendix G: Reference Schematic



EAN, P20, P24 are recommended to reserve with test point for future firmware, EEPROM table update after the module are welded on load board.

Appendix H: Label Information

TBA

Appendix I: Packaging Information

TBA

Appendix J: Reversion History

Version	Date	History
0.9	2013/06/24	First Version
1.0	2013/10/01	Final Version