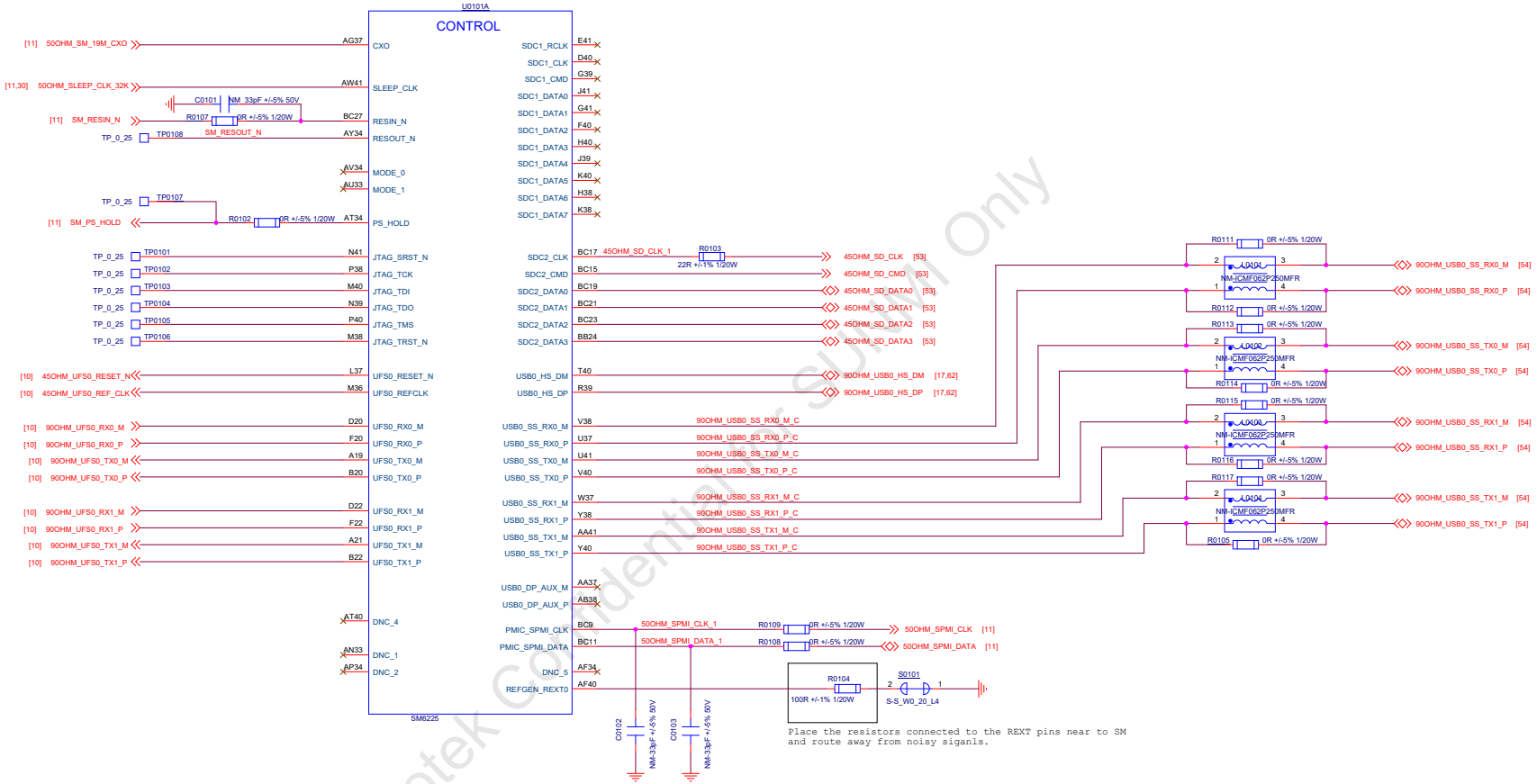
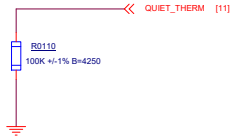


Place the resistors connected to the REXT pins near to SM and route away from noisy siganls.

1) Place near the SM
2) Route the SPMI signals in Daisy Chain/Star routing from SM to the PMICS to avoid stubs.



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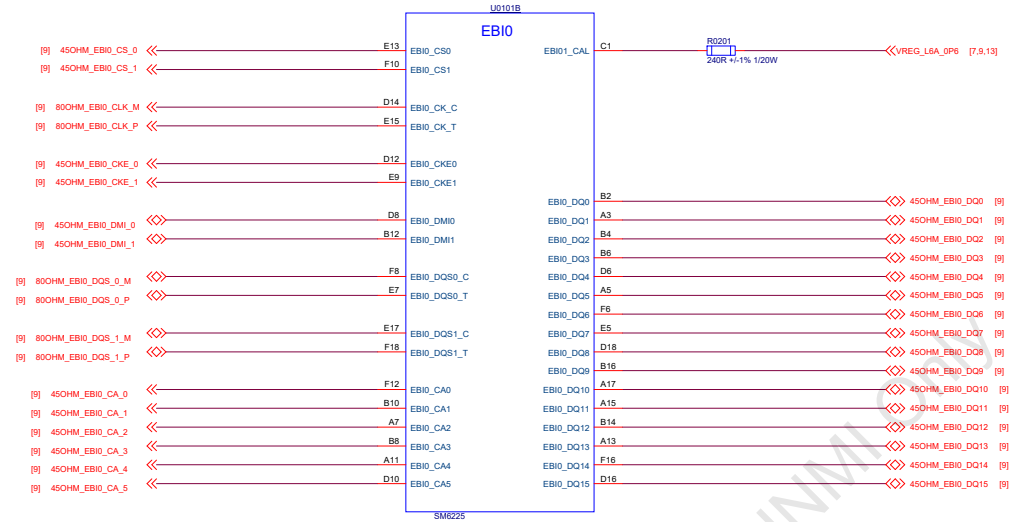
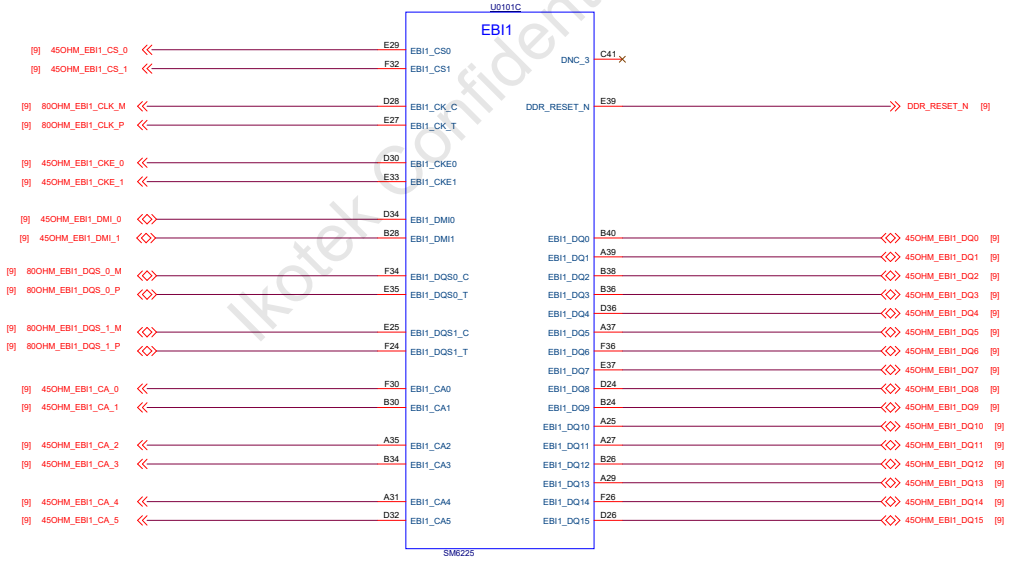
Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Honson
Size	A2		
Date:	Monday, March 20, 2023	Sheet	1 of 64





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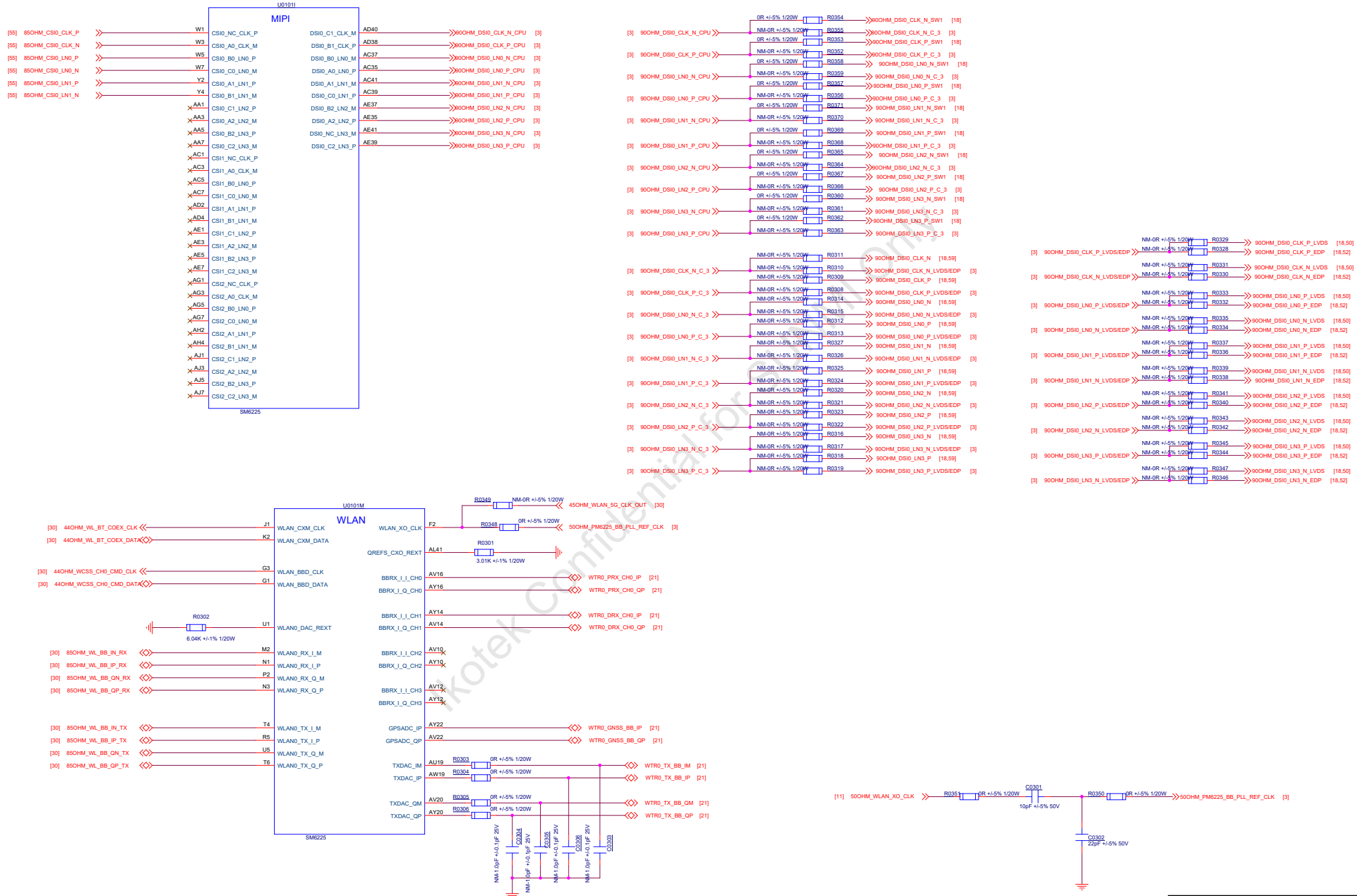
Organization: Quectel ODM Solutions			
Project: T3-EU			Ver: V1.1
Drawn By: Dongy	Checked By: Honson		Size: A2
Date: Monday, March 20, 2023	Sheet 2 of 64		



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Project	T3-EU		Ver V1.1
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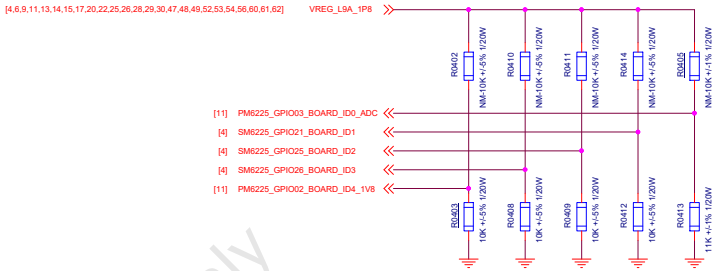
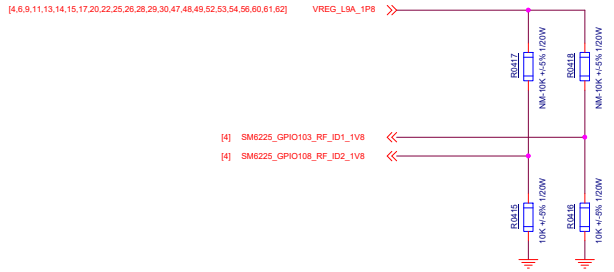
Board ID



GPIO_48	WDOG_DISABLE	BOOT_CONFIG[0]
GPIO_50	FAST_BOOT_SEL_0	BOOT_CONFIG[1]
GPIO_51	FAST_BOOT_SEL_1	BOOT_CONFIG[2]
GPIO_53	FAST_BOOT_SEL_2	BOOT_CONFIG[3]
GPIO_55	FAST_BOOT_SEL_3	BOOT_CONFIG[4]

FAST_BOOT[3:0]	BOOT Sequence
0b0000	eMMC -> SD -> eDL (eDL path - USB only)
0b0001	SD -> eMMC -> eDL (eDL path - USB only)
0b0010	SD -> eDL (eDL path - USB only)
0b0011	USB -> eDL
0b0100	UFS -> SD -> eDL (eDL path - USB only)
0b0101	SD -> UFS -> eDL (eDL path - USB only)
0b0110	UFS -> eDL (eDL path - USB only)
0b0111	eMMC -> SD -> eDL (eDL path - USB only)
0b1000	eMMC -> eDL (eDL path - USB only)



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Project	T3-EU		Ver V1.1
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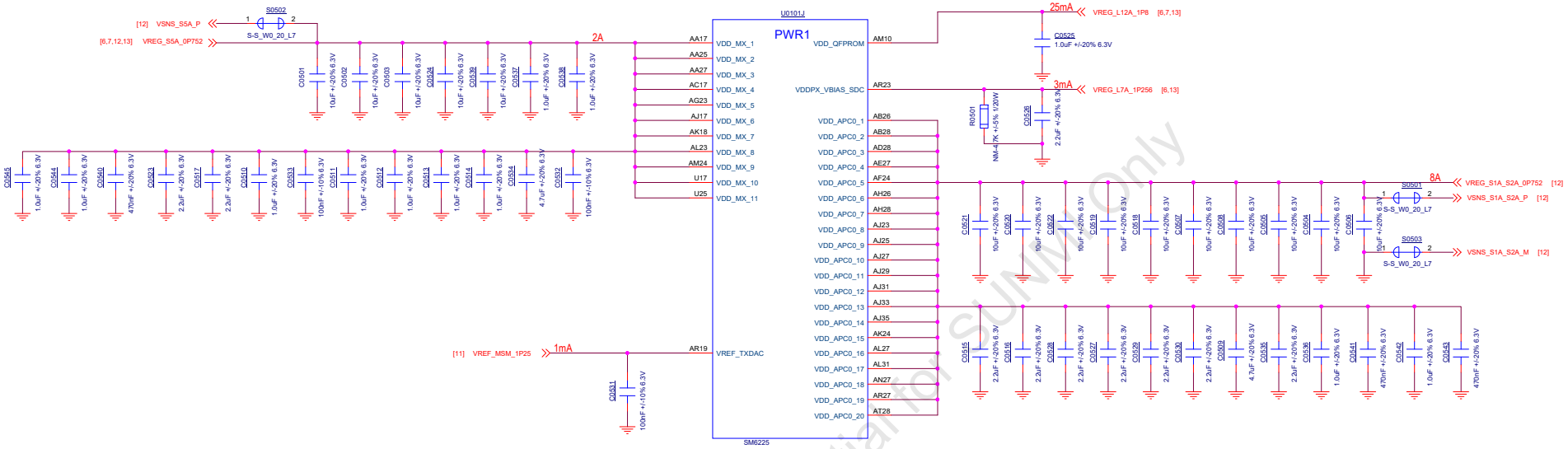

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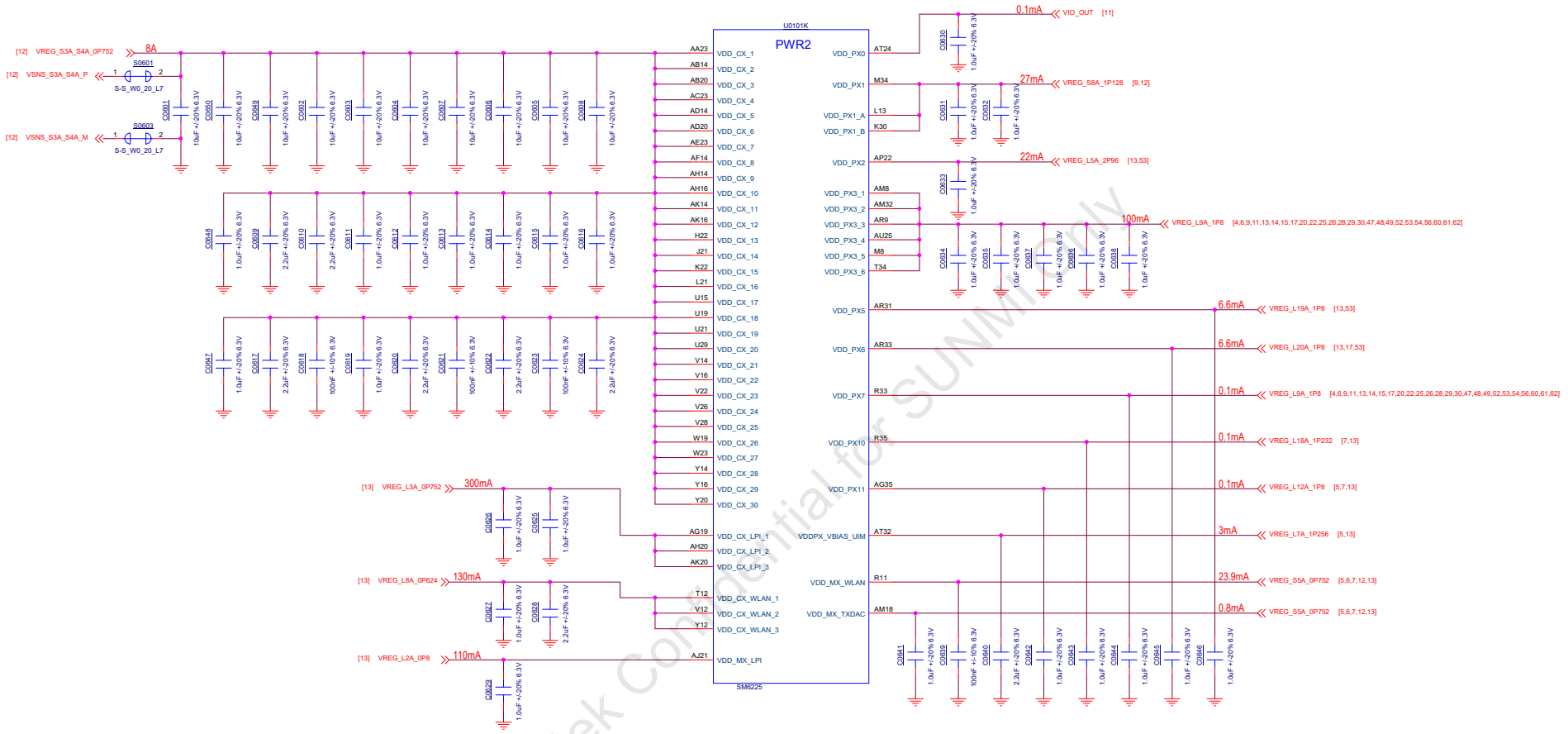
Project	T3-EU		Ver V1.1
Drawn By Dongy		Checked By Honson	Size A2
Date: Monday, March 20, 2023		Sheet 5 of 83	



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Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
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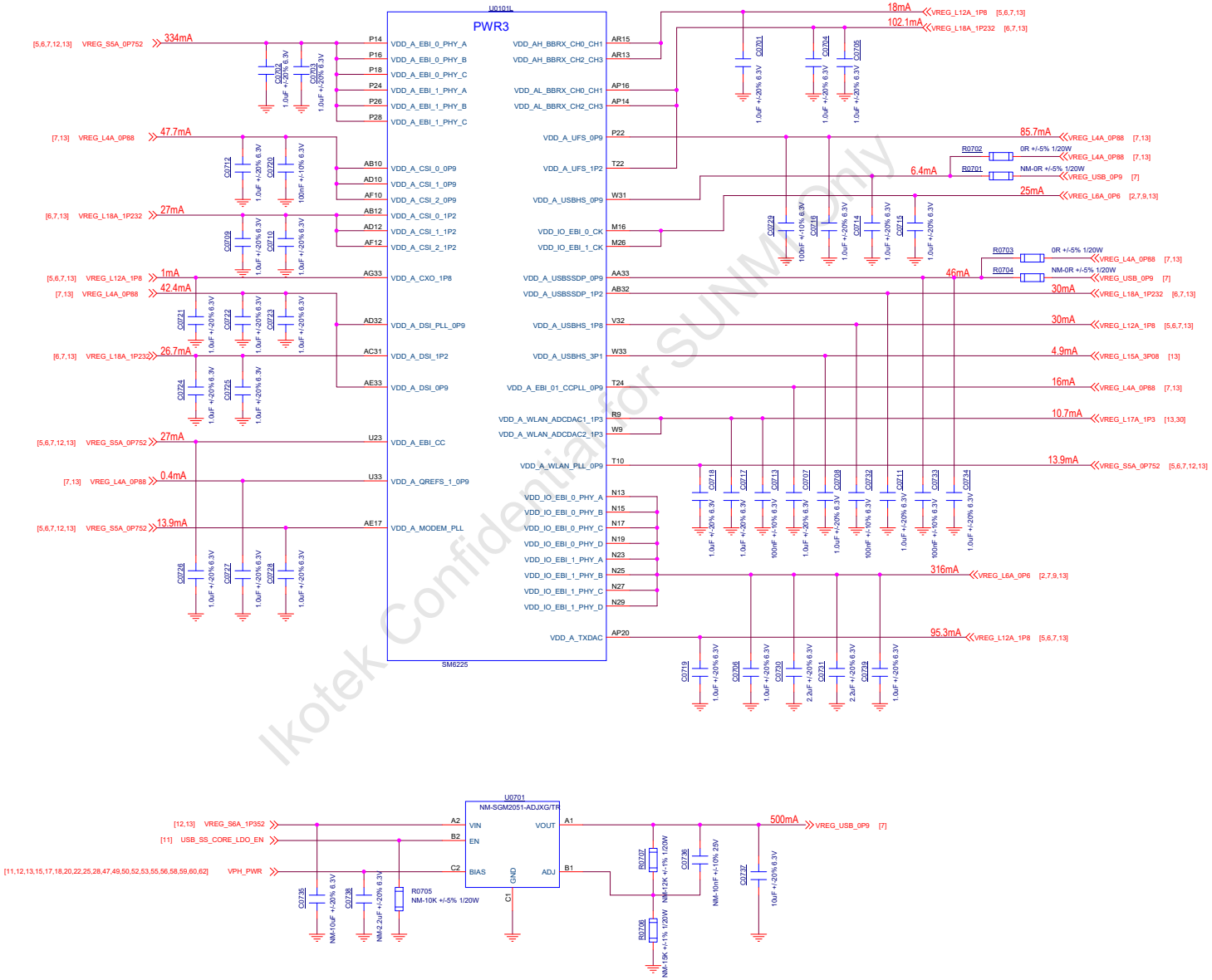

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Drawn By	Dongy	Checked By	Honson
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Project	T3-EU		Ver V1.1
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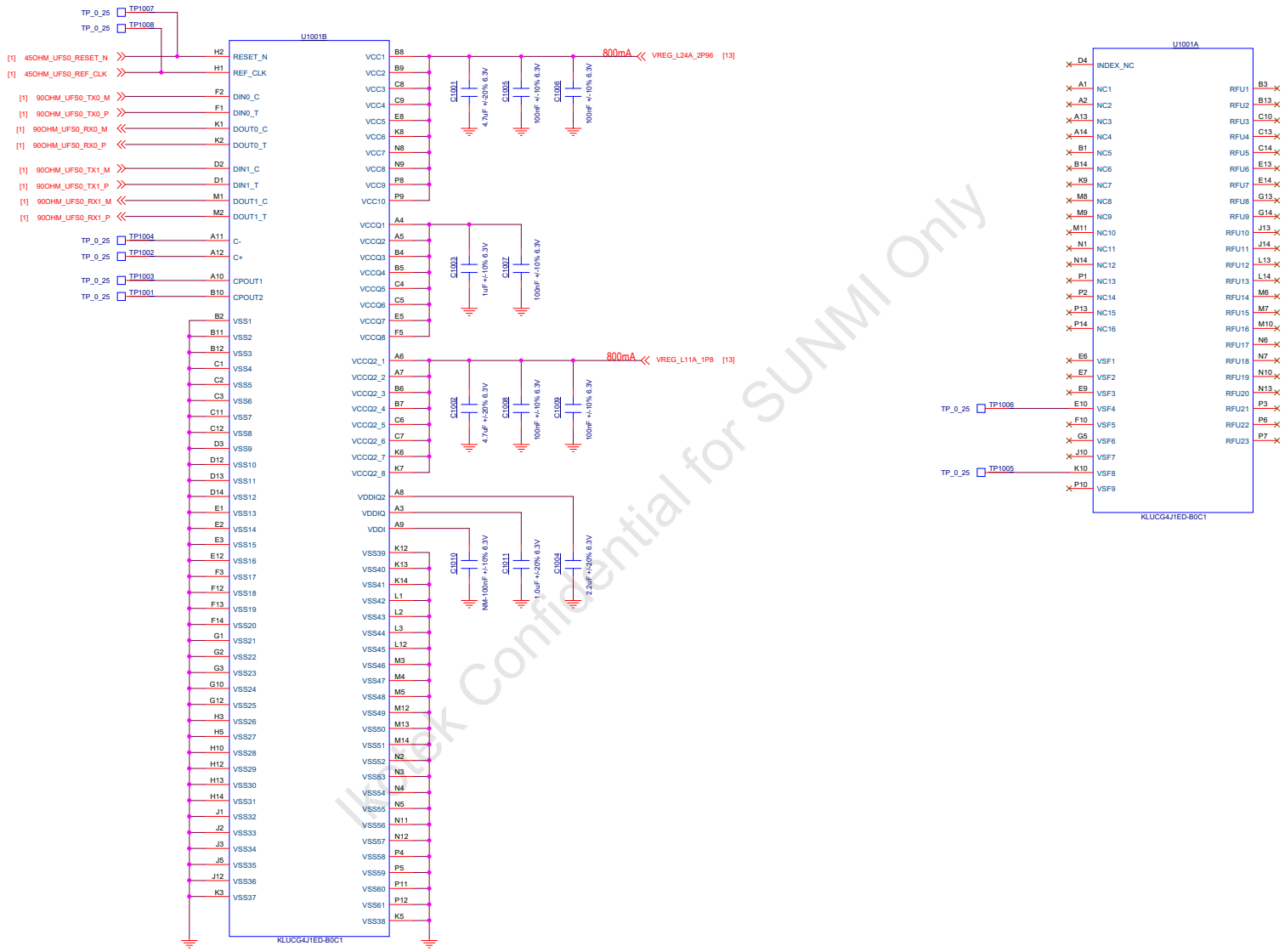

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Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Honson	Size	A2
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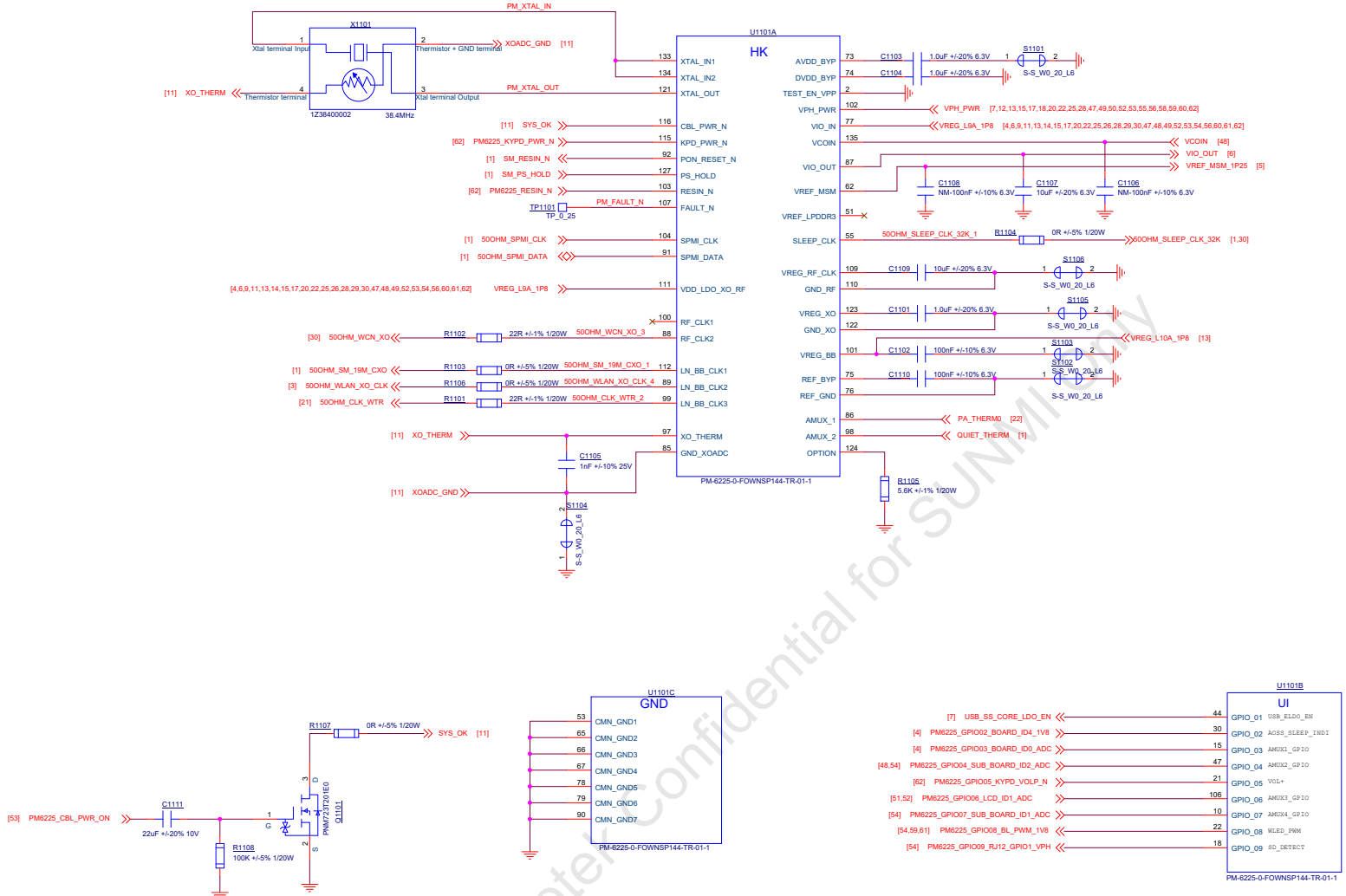

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Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Honson
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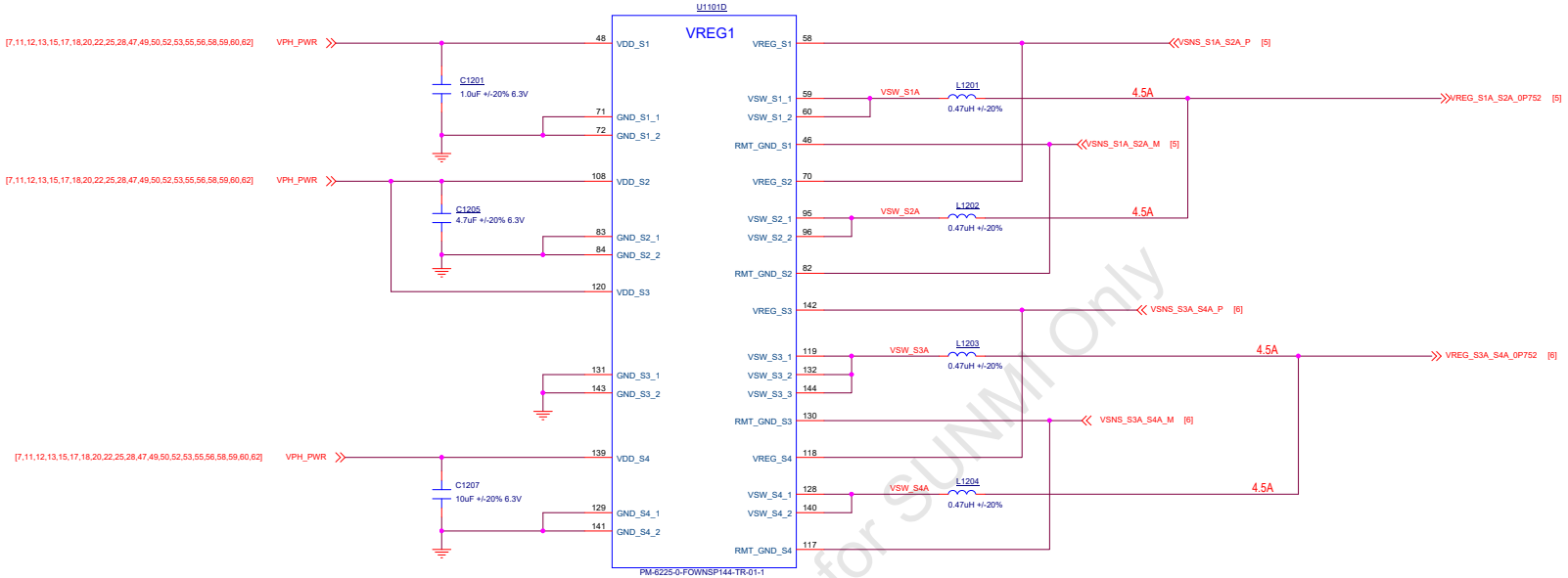

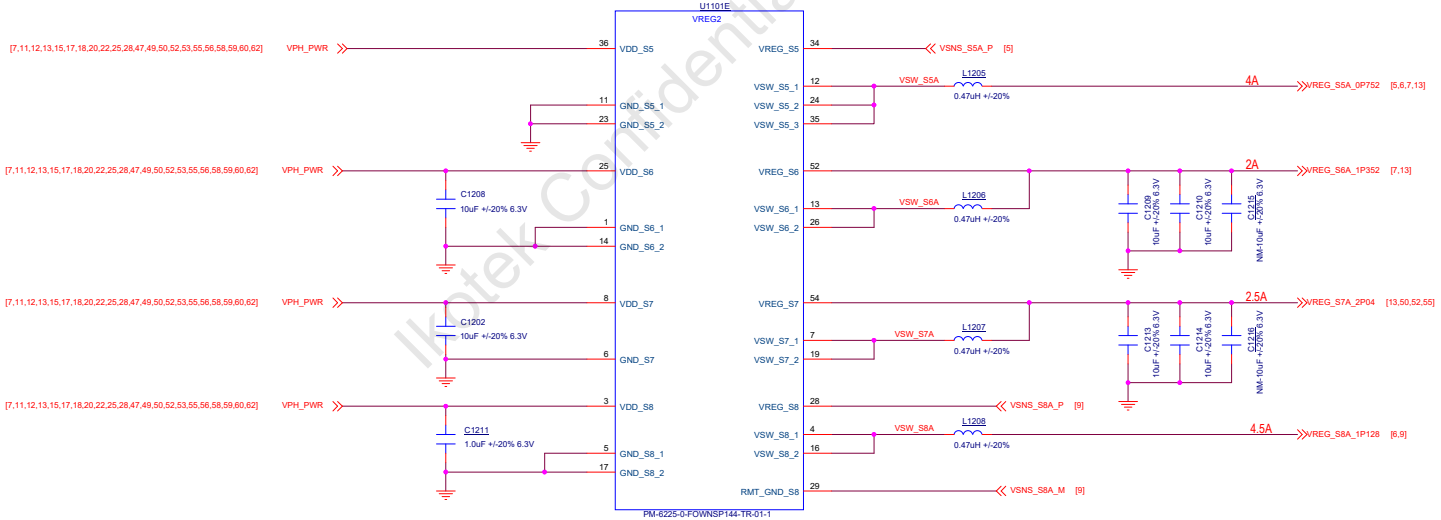

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Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
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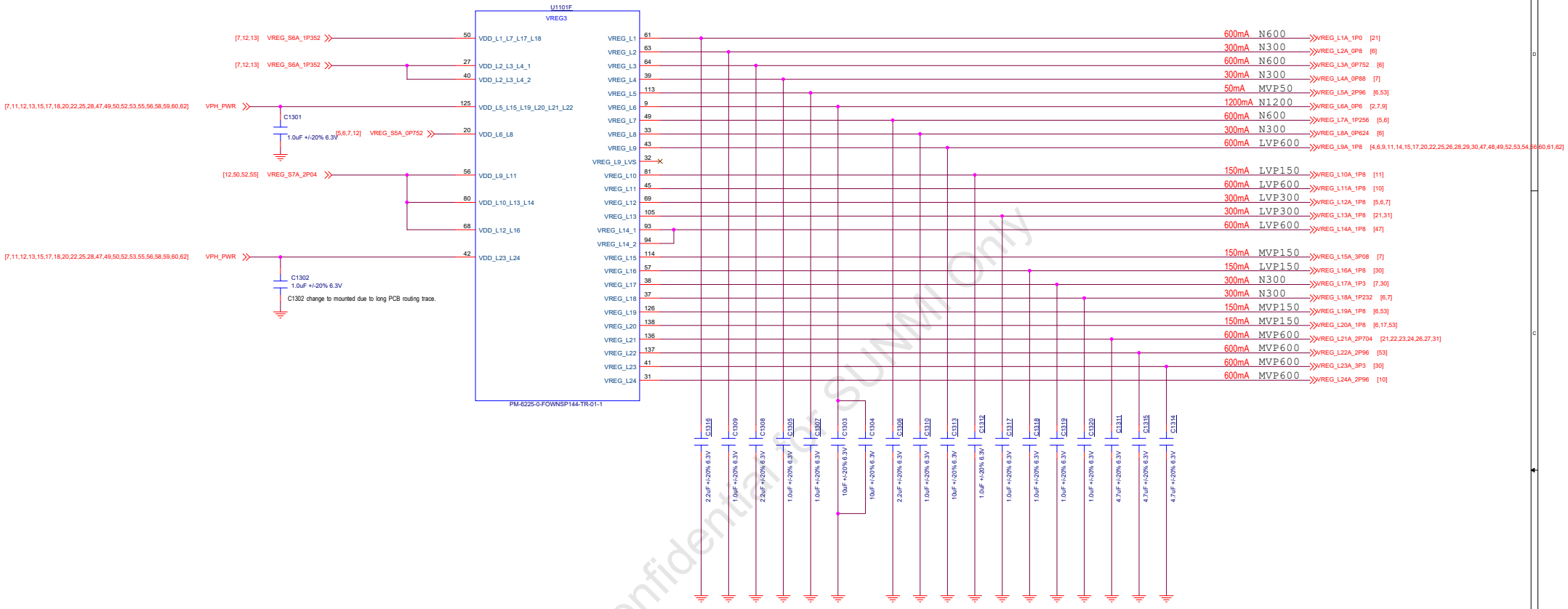

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NOTE: Place these caps close to PMIC.
Prioritize N1200s over N300s for placement.

N1200FT(2 x 10uF)
Min : 20uF , Max : 44uF

N1200 (1x 4.7uF)
Min : 4.7uF , Max : 22uF

N600 (1x 2.2uF)

N300 (1 X 1uF)
Min : 1uF , Max : 10uF

Doesn't have to be close to its pin

Psuedo-Capless

MVP150 - Min : 0.47uF , Max : 5uF
MVP600 - Min : 4.7uF , Max : 23.5uF
LVP600 - Min : 4.7uF , Max

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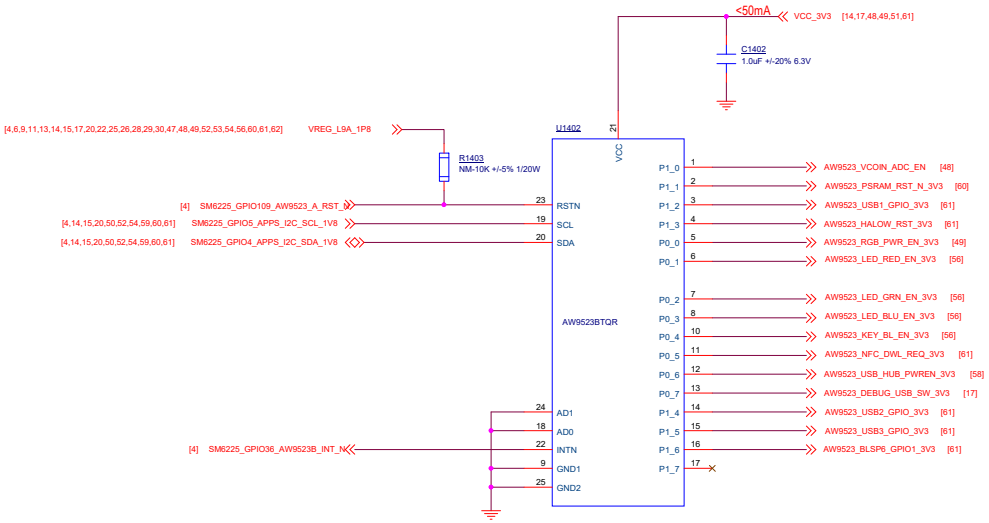
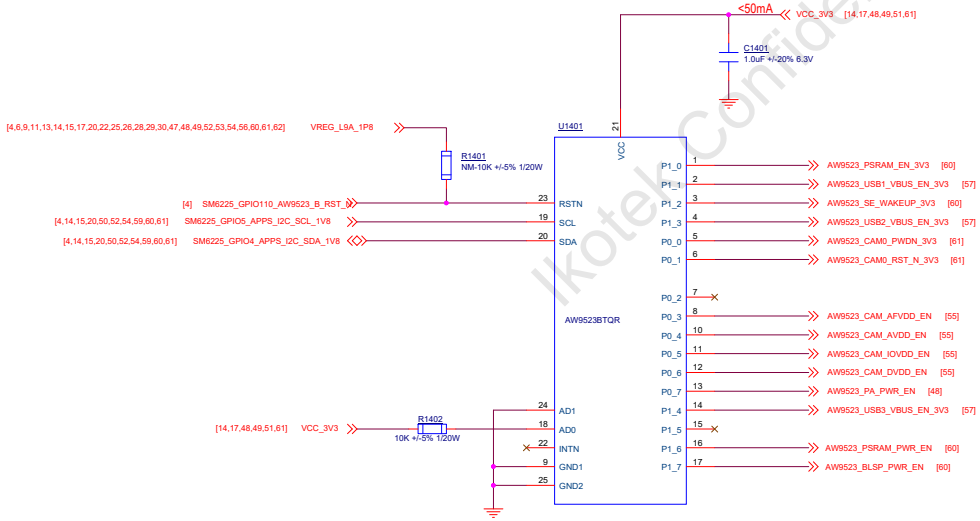


AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z



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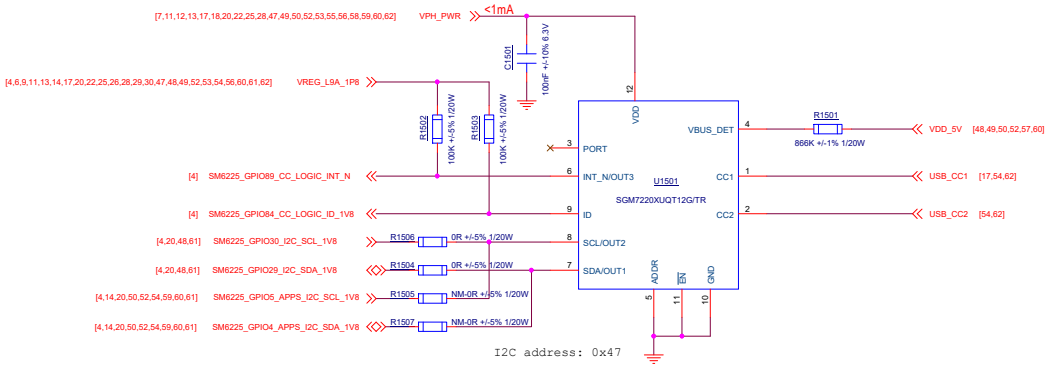

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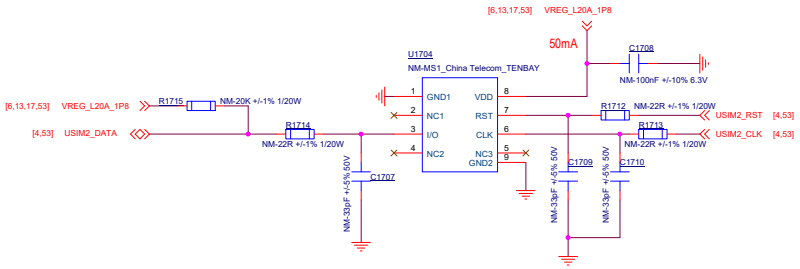
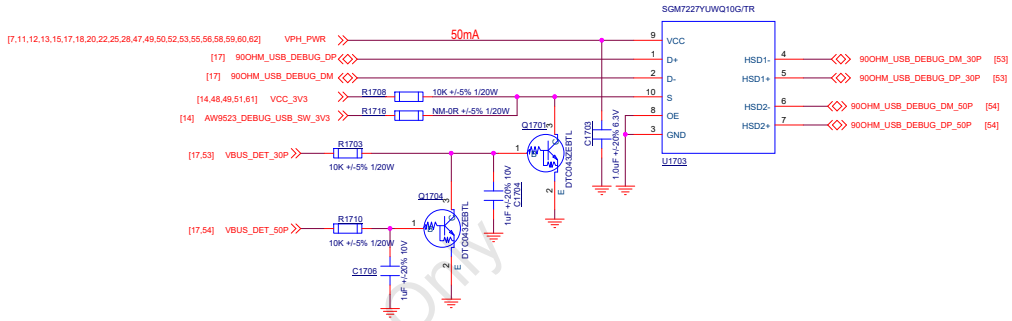
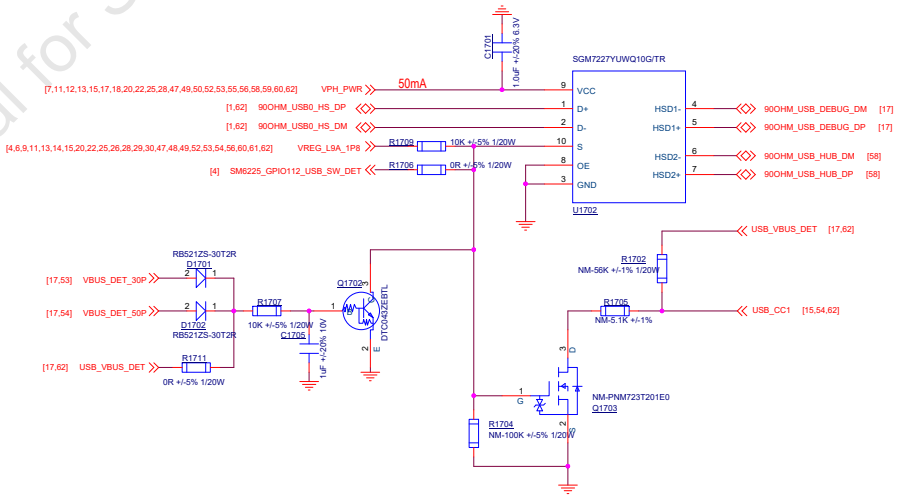
eSIM



USB DEBUG SWITCH





FUNCTION TABLE

$\overline{OE}$	S	HSD1+, HSD1-	HSD2+, HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	×	OFF	OFF

Switches Shown For Logic "0" Input

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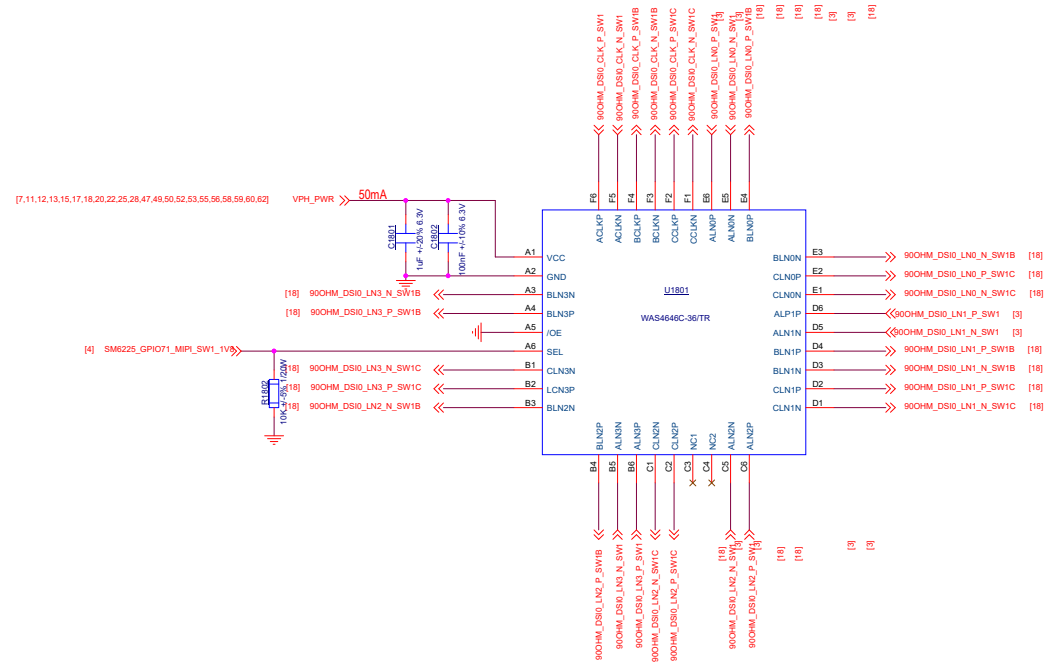

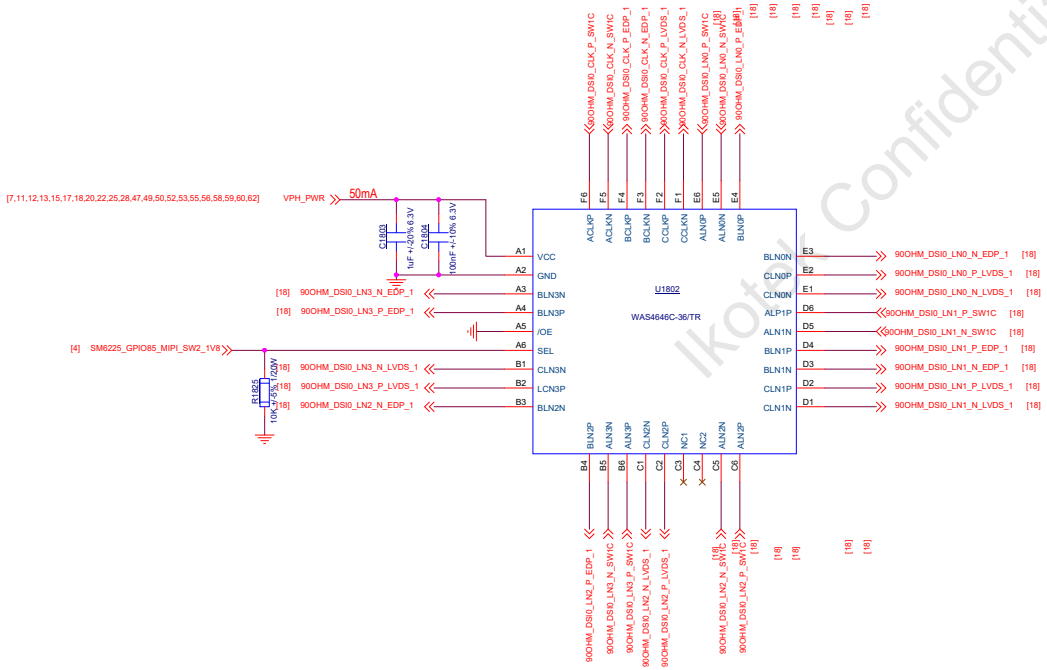

[18] 90OHM_DSI0_CLK_N_SW1B	0R +/-5% 1/20W	R1829	90OHM_DSI0_CLK_N [3,59]
[18] 90OHM_DSI0_CLK_P_SW1B	0R +/-5% 1/20W	R1828	90OHM_DSI0_CLK_P [3,59]
[18] 90OHM_DSI0_LN0_N_SW1B	0R +/-5% 1/20W	R1831	90OHM_DSI0_LN0_N [3,59]
[18] 90OHM_DSI0_LN0_P_SW1B	0R +/-5% 1/20W	R1830	90OHM_DSI0_LN0_P [3,59]
[18] 90OHM_DSI0_LN1_N_SW1B	0R +/-5% 1/20W	R1813	90OHM_DSI0_LN1_N [3,59]
[18] 90OHM_DSI0_LN1_P_SW1B	0R +/-5% 1/20W	R1827	90OHM_DSI0_LN1_P [3,59]
[18] 90OHM_DSI0_LN2_N_SW1B	0R +/-5% 1/20W	R1806	90OHM_DSI0_LN2_N [3,59]
[18] 90OHM_DSI0_LN2_P_SW1B	0R +/-5% 1/20W	R1826	90OHM_DSI0_LN2_P [3,59]
[18] 90OHM_DSI0_LN3_N_SW1B	0R +/-5% 1/20W	R1832	90OHM_DSI0_LN3_N [3,59]
[18] 90OHM_DSI0_LN3_P_SW1B	0R +/-5% 1/20W	R1810	90OHM_DSI0_LN3_P [3,59]
[18] 90OHM_DSI0_CLK_N_EDP_1	0R +/-5% 1/20W	R1818	90OHM_DSI0_CLK_N_EDP [3,52]
[18] 90OHM_DSI0_CLK_P_EDP_1	0R +/-5% 1/20W	R1817	90OHM_DSI0_CLK_P_EDP [3,52]
[18] 90OHM_DSI0_LN0_N_EDP_1	0R +/-5% 1/20W	R1814	90OHM_DSI0_LN0_N_EDP [3,52]
[18] 90OHM_DSI0_LN0_P_EDP_1	0R +/-5% 1/20W	R1804	90OHM_DSI0_LN0_P_EDP [3,52]
[18] 90OHM_DSI0_LN1_N_EDP_1	0R +/-5% 1/20W	R1822	90OHM_DSI0_LN1_N_EDP [3,52]
[18] 90OHM_DSI0_LN1_P_EDP_1	0R +/-5% 1/20W	R1803	90OHM_DSI0_LN1_P_EDP [3,52]
[18] 90OHM_DSI0_LN2_N_EDP_1	0R +/-5% 1/20W	R1821	90OHM_DSI0_LN2_N_EDP [3,52]
[18] 90OHM_DSI0_LN2_P_EDP_1	0R +/-5% 1/20W	R1819	90OHM_DSI0_LN2_P_EDP [3,52]
[18] 90OHM_DSI0_LN3_N_EDP_1	0R +/-5% 1/20W	R1824	90OHM_DSI0_LN3_N_EDP [3,52]
[18] 90OHM_DSI0_LN3_P_EDP_1	0R +/-5% 1/20W	R1807	90OHM_DSI0_LN3_P_EDP [3,52]
[18] 90OHM_DSI0_CLK_N_LVDS_1	0R +/-5% 1/20W	R1809	90OHM_DSI0_CLK_N_LVDS [3,50]
[18] 90OHM_DSI0_CLK_P_LVDS_1	0R +/-5% 1/20W	R1820	90OHM_DSI0_CLK_P_LVDS [3,50]
[18] 90OHM_DSI0_LN0_N_LVDS_1	0R +/-5% 1/20W	R1805	90OHM_DSI0_LN0_N_LVDS [3,50]
[18] 90OHM_DSI0_LN0_P_LVDS_1	0R +/-5% 1/20W	R1823	90OHM_DSI0_LN0_P_LVDS [3,50]
[18] 90OHM_DSI0_LN1_N_LVDS_1	0R +/-5% 1/20W	R1811	90OHM_DSI0_LN1_N_LVDS [3,50]
[18] 90OHM_DSI0_LN1_P_LVDS_1	0R +/-5% 1/20W	R1816	90OHM_DSI0_LN1_P_LVDS [3,50]
[18] 90OHM_DSI0_LN2_N_LVDS_1	0R +/-5% 1/20W	R1812	90OHM_DSI0_LN2_N_LVDS [3,50]
[18] 90OHM_DSI0_LN2_P_LVDS_1	0R +/-5% 1/20W	R1808	90OHM_DSI0_LN2_P_LVDS [3,50]
[18] 90OHM_DSI0_LN3_N_LVDS_1	0R +/-5% 1/20W	R1815	90OHM_DSI0_LN3_N_LVDS [3,50]
[18] 90OHM_DSI0_LN3_P_LVDS_1	0R +/-5% 1/20W	R1801	90OHM_DSI0_LN3_P_LVDS [3,50]

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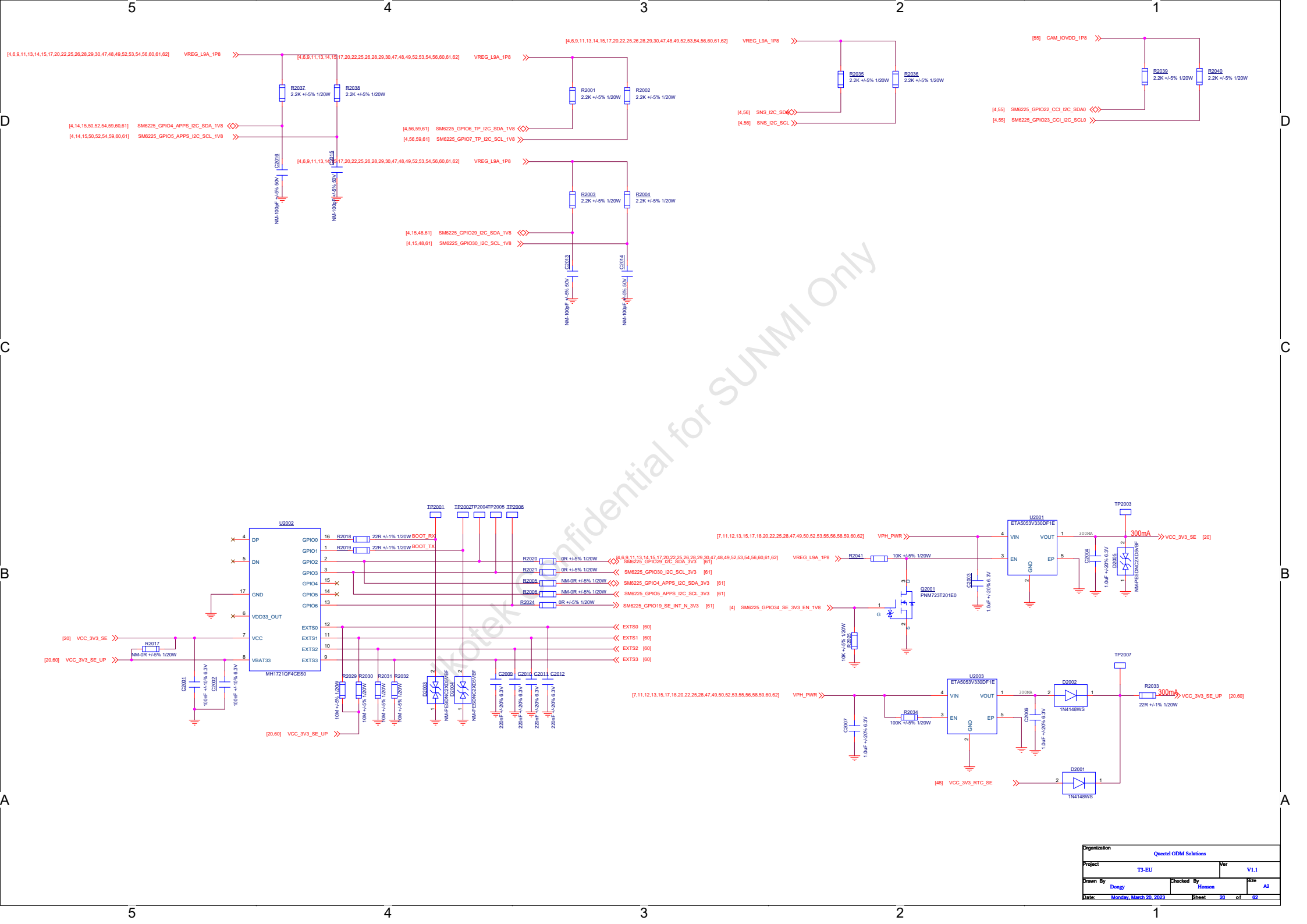

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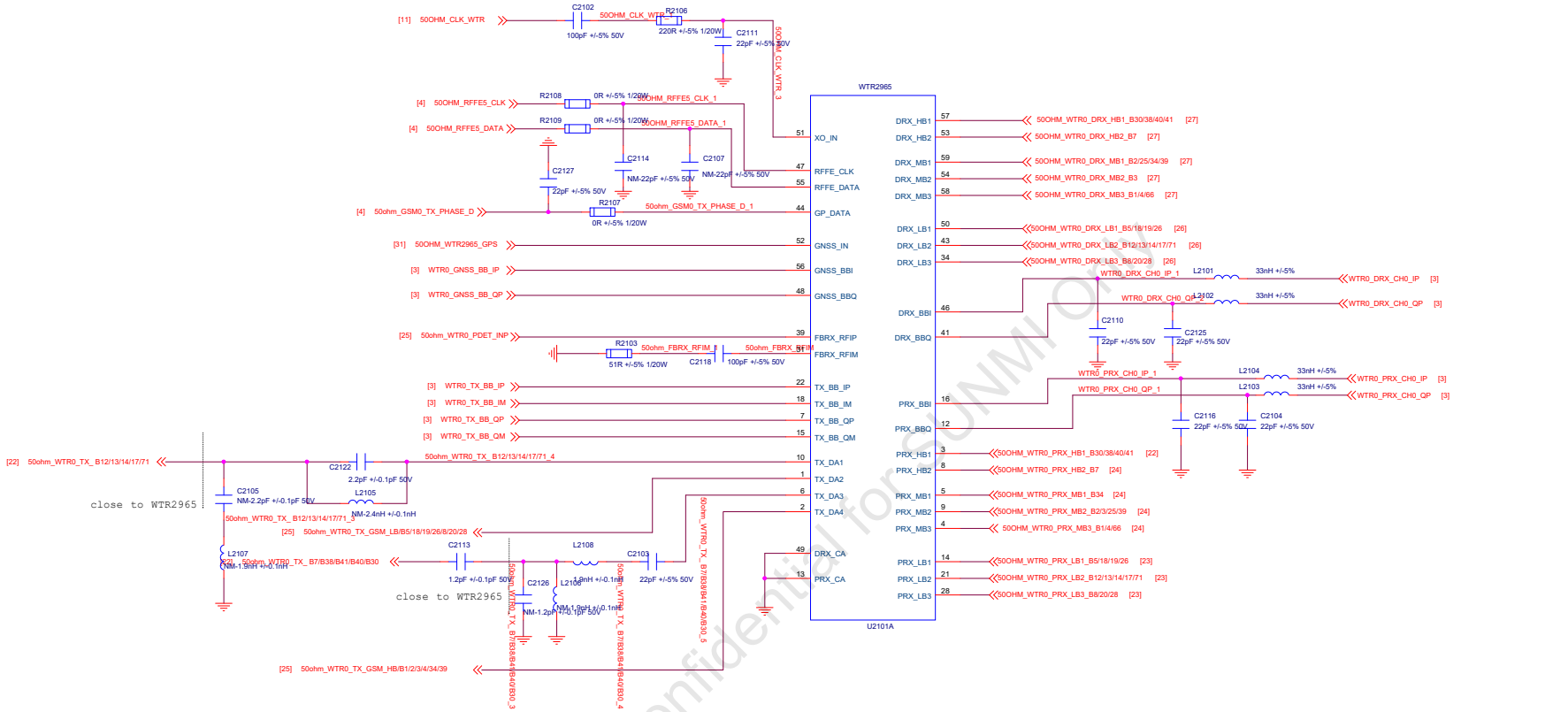

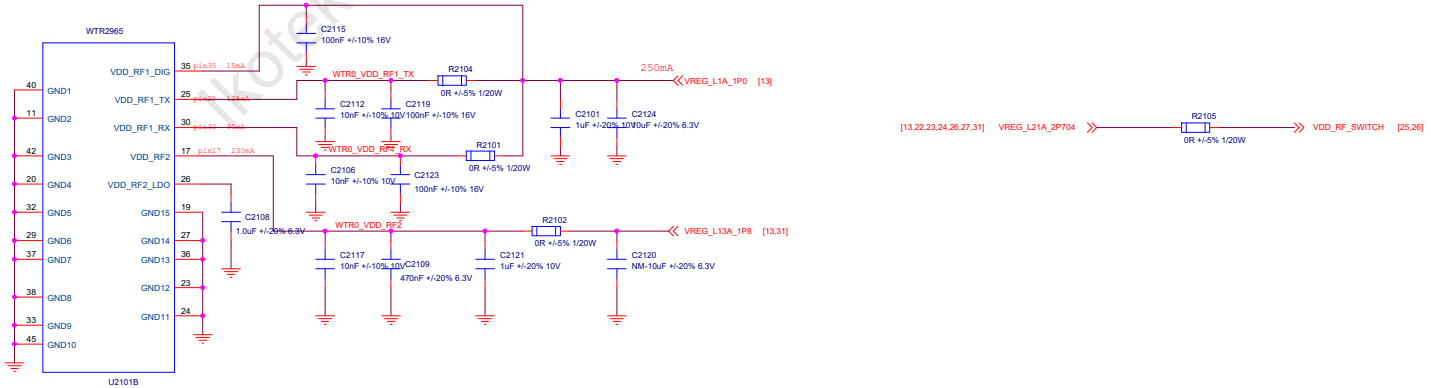

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Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
Size	A2		
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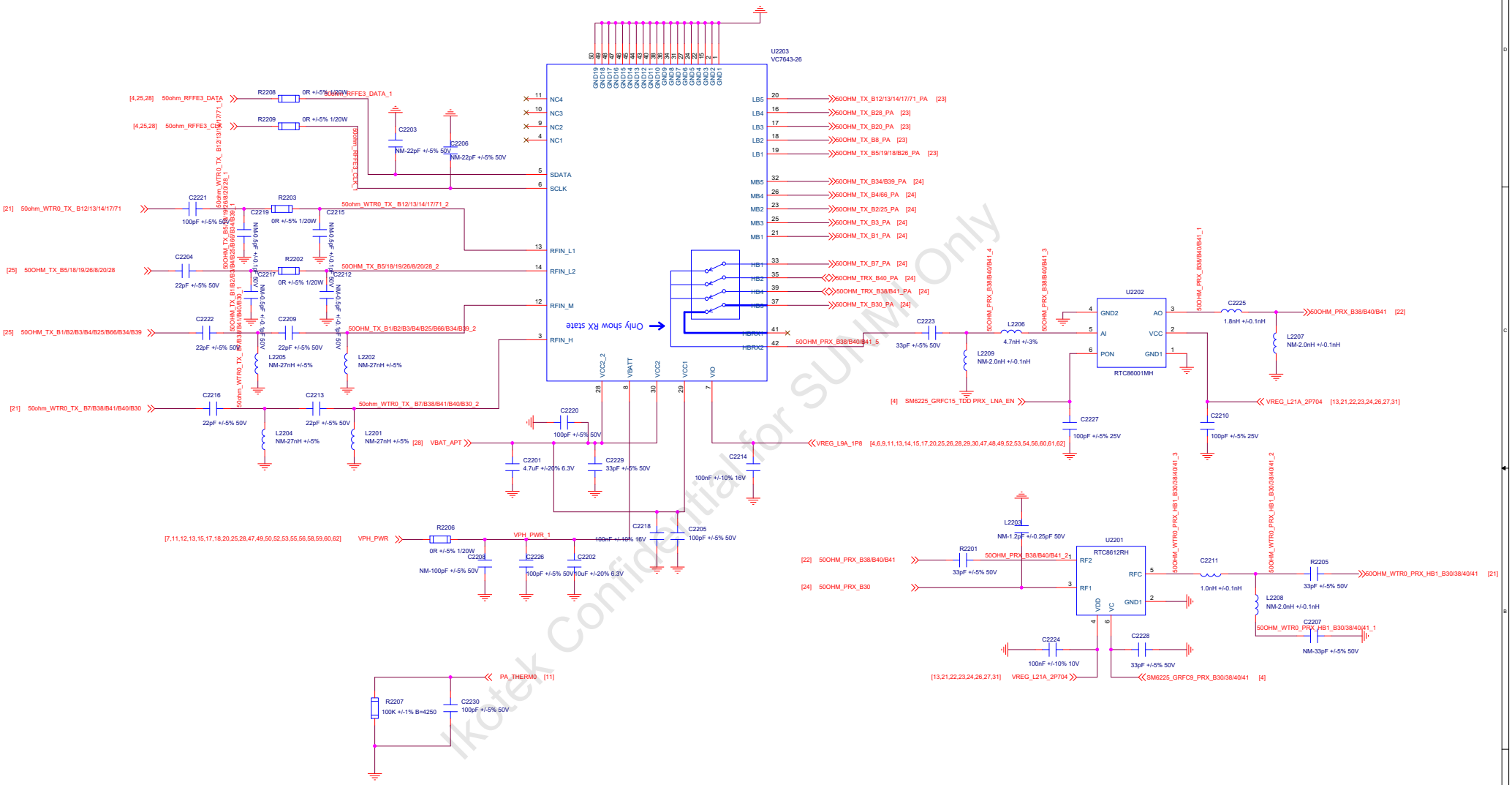

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Organization	Quectel Wireless Solutions		
Project	T3-EU		Ver V1.1
Drawn By Hobart		Checked By Stefan	Size A2
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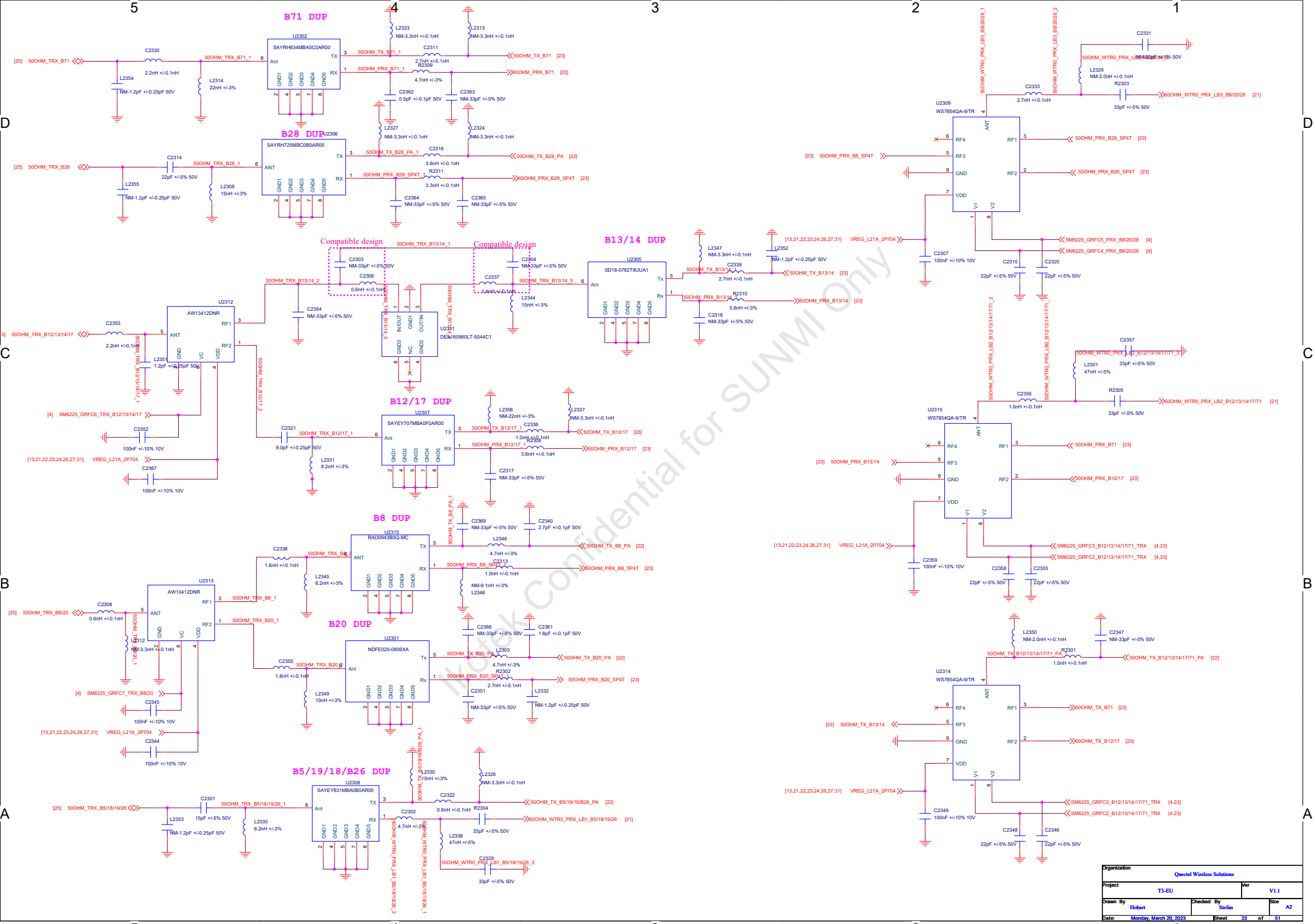

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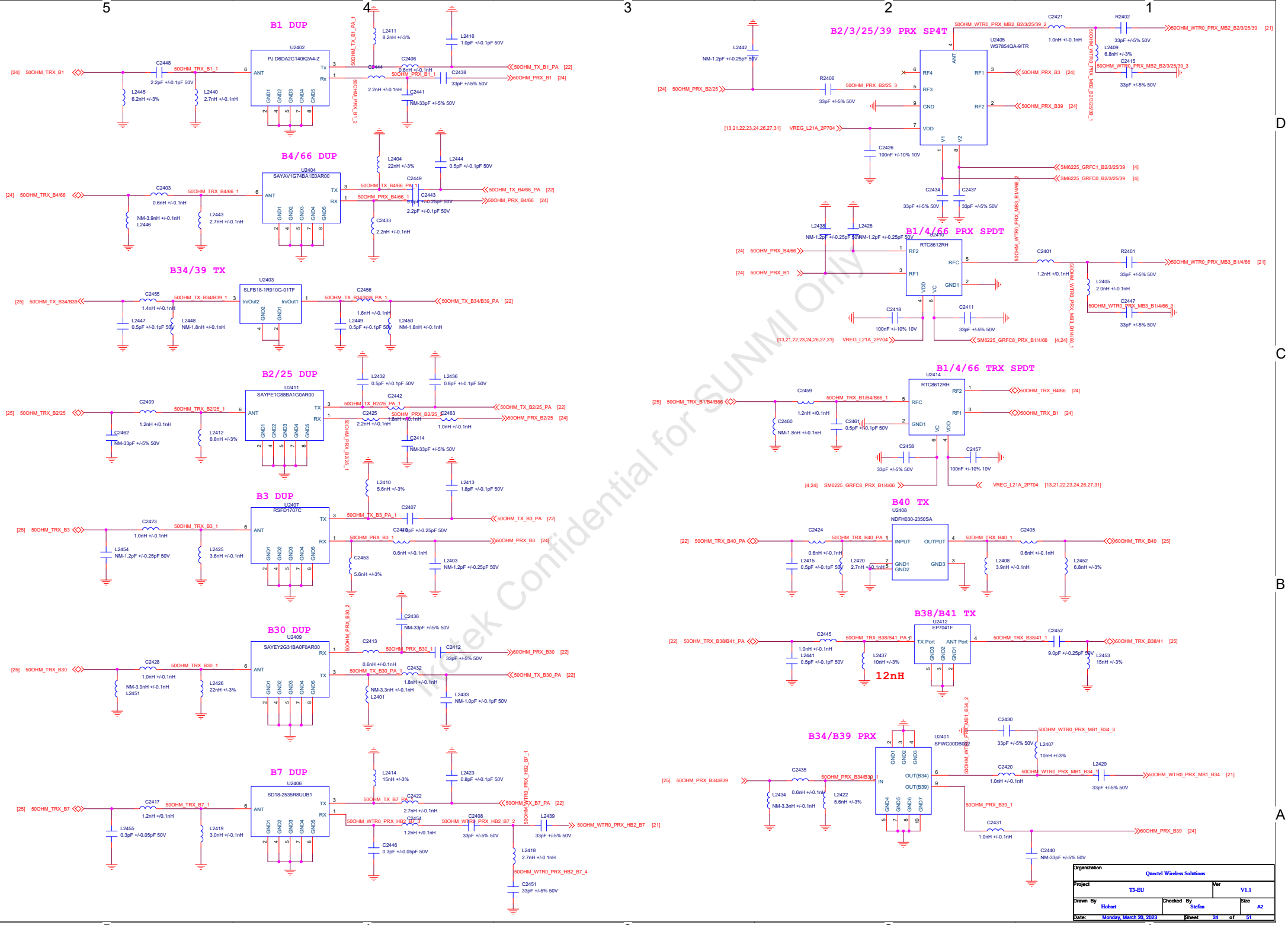

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Organization	Quectel Wireless Solutions
Project	T3-EU
Ver	V1.1
Drawn By	Hobart
Checked By	Stefan
Size	A2
Date:	Monday, March 20, 2023
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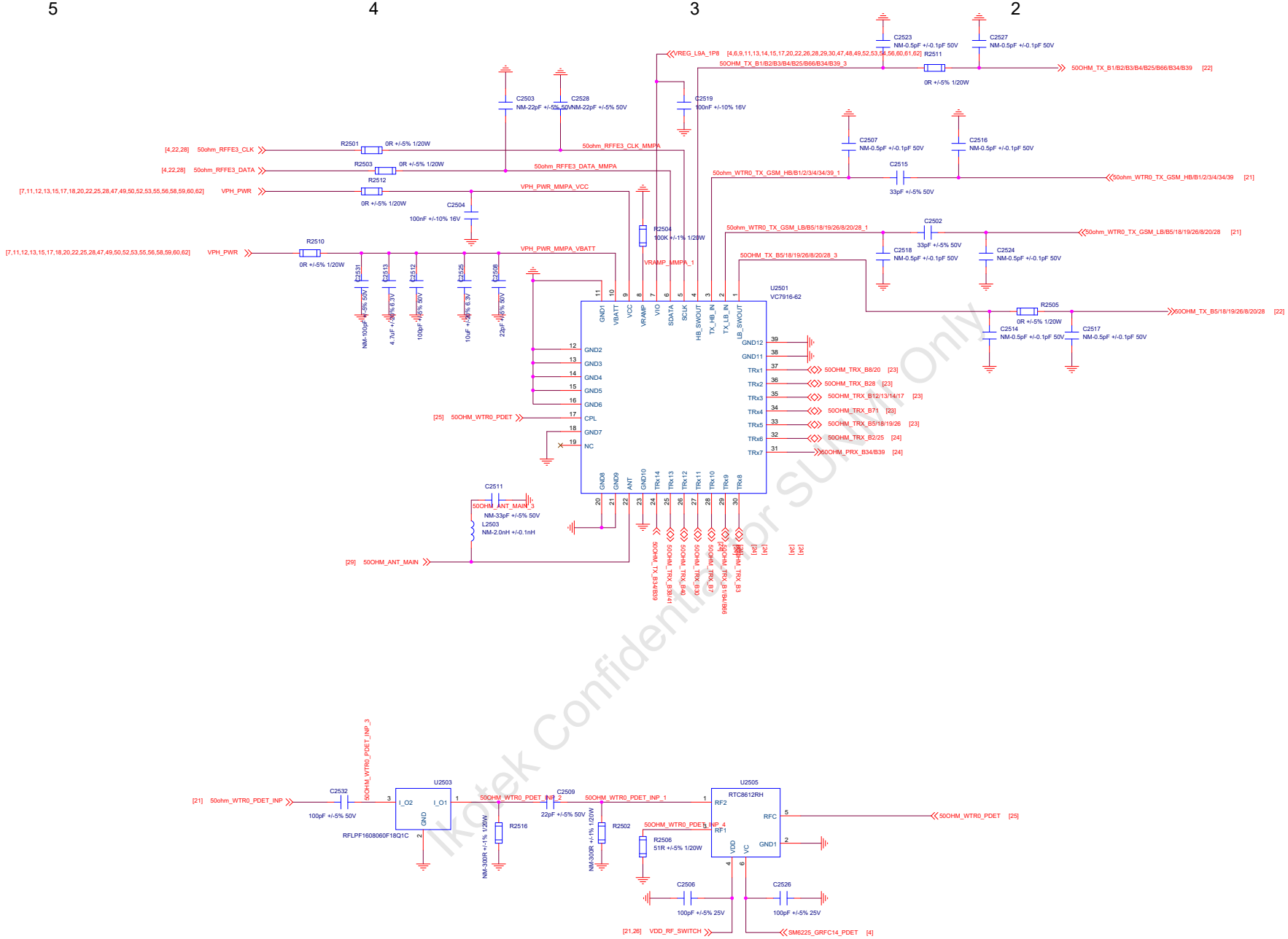

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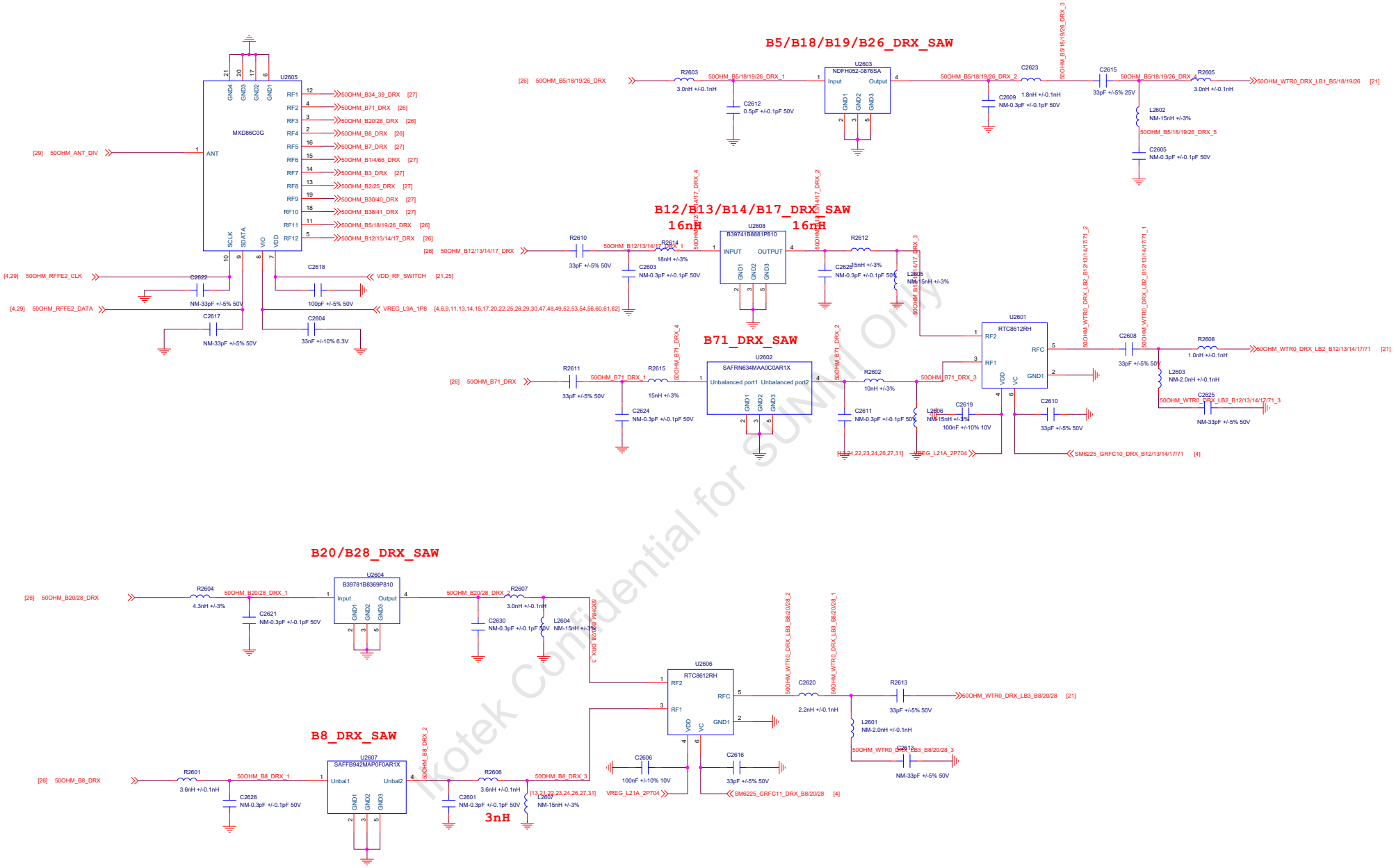
Organization	Quectel Wireless Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
Size	A2		
Date:	Monday, March 20, 2023	Sheet	25 of 51



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Organization	Quectel Wireless Solutions
Project	T3-EU
Ver	V1.1
Drawn By	Hobart
Checked By	Stefan
Size	A2
Date:	Monday, March 20, 2023
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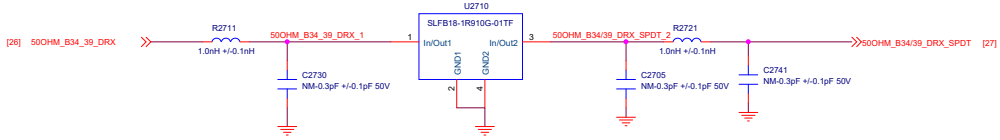
B34_B39_DRX_SAW



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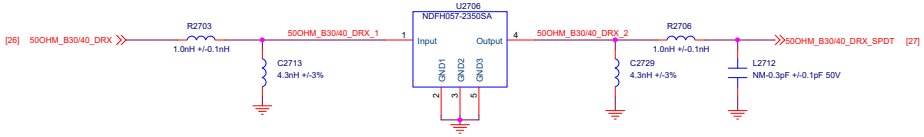

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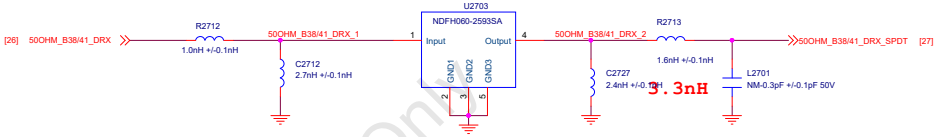

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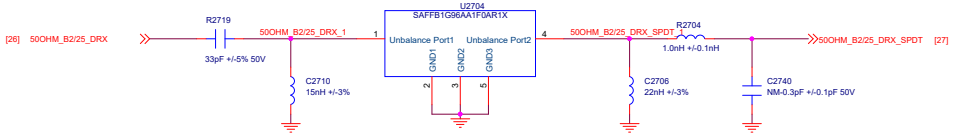

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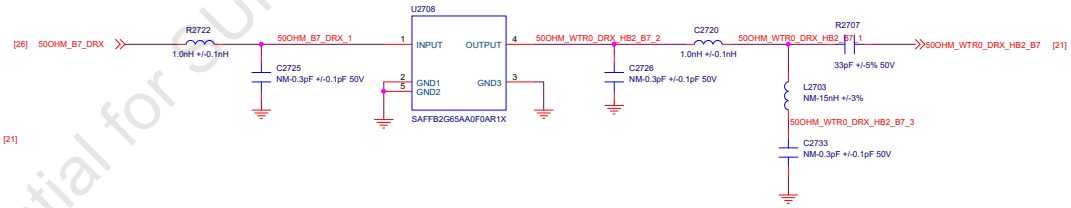

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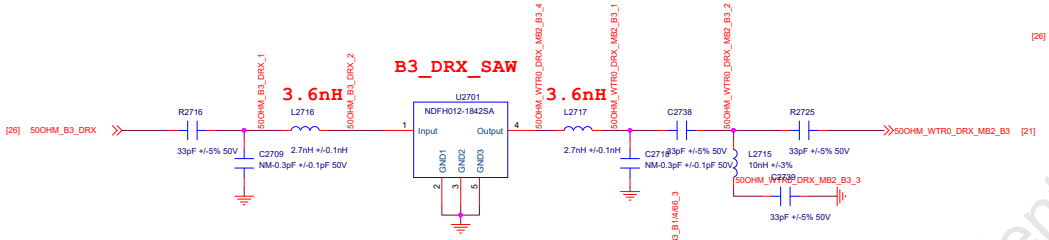
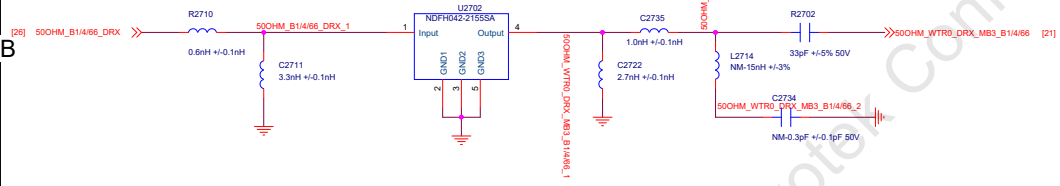
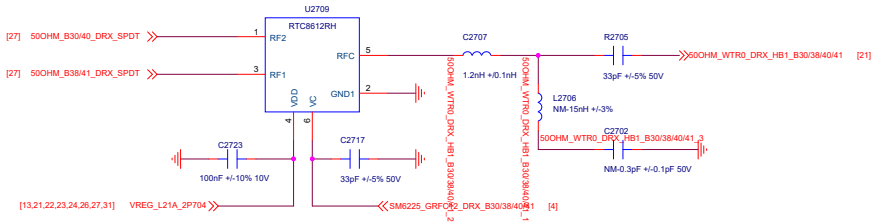


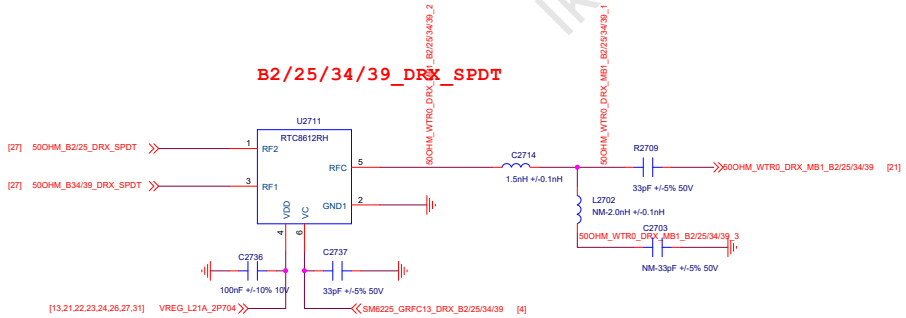
B1/B4/B66_DRX_SAW



B30/38/40/41_DRX_SPDT



B2/25/34/39_DRX_SPDT



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Organization	Quectel Wireless Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
Size	A2		
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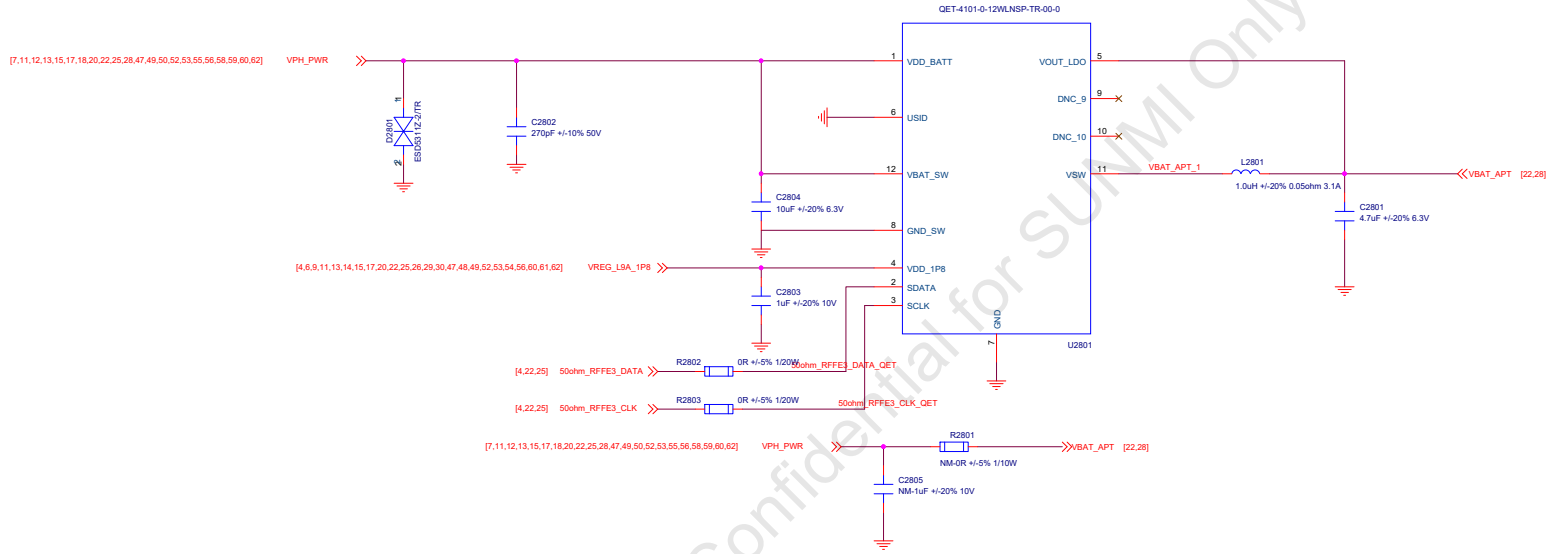

Ikotek Confidential for SUMMI Only

Organization	Quectel Wireless Solutions
Project	T3-EU
Ver	V1.1
Drawn By	Hobart
Checked By	Stefan
Size	A2
Date:	Monday, March 20, 2023
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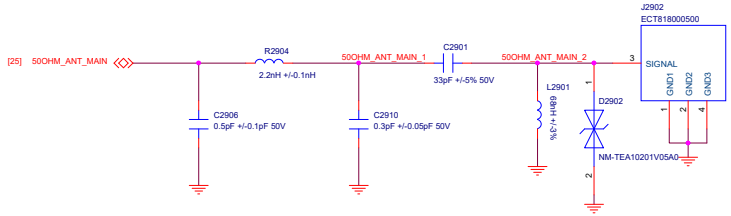
MAIN_ANT



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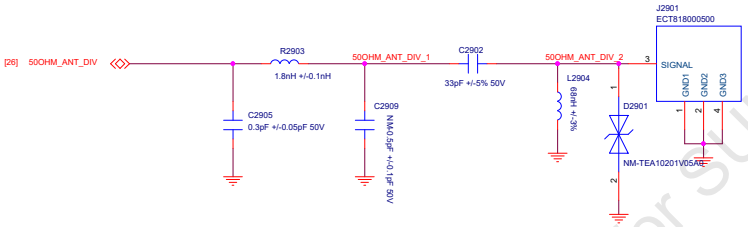
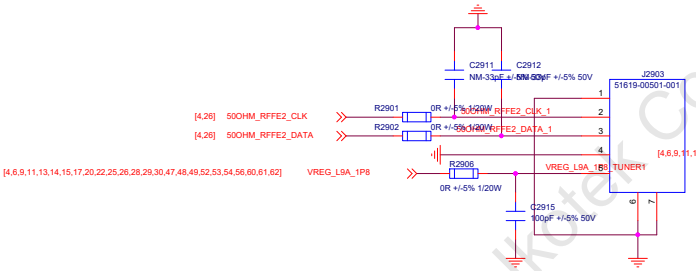
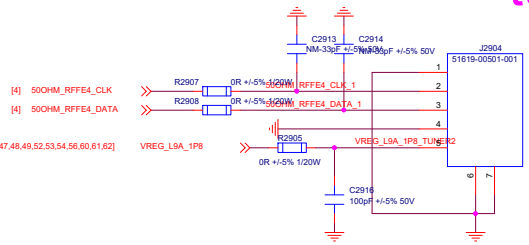


tuner





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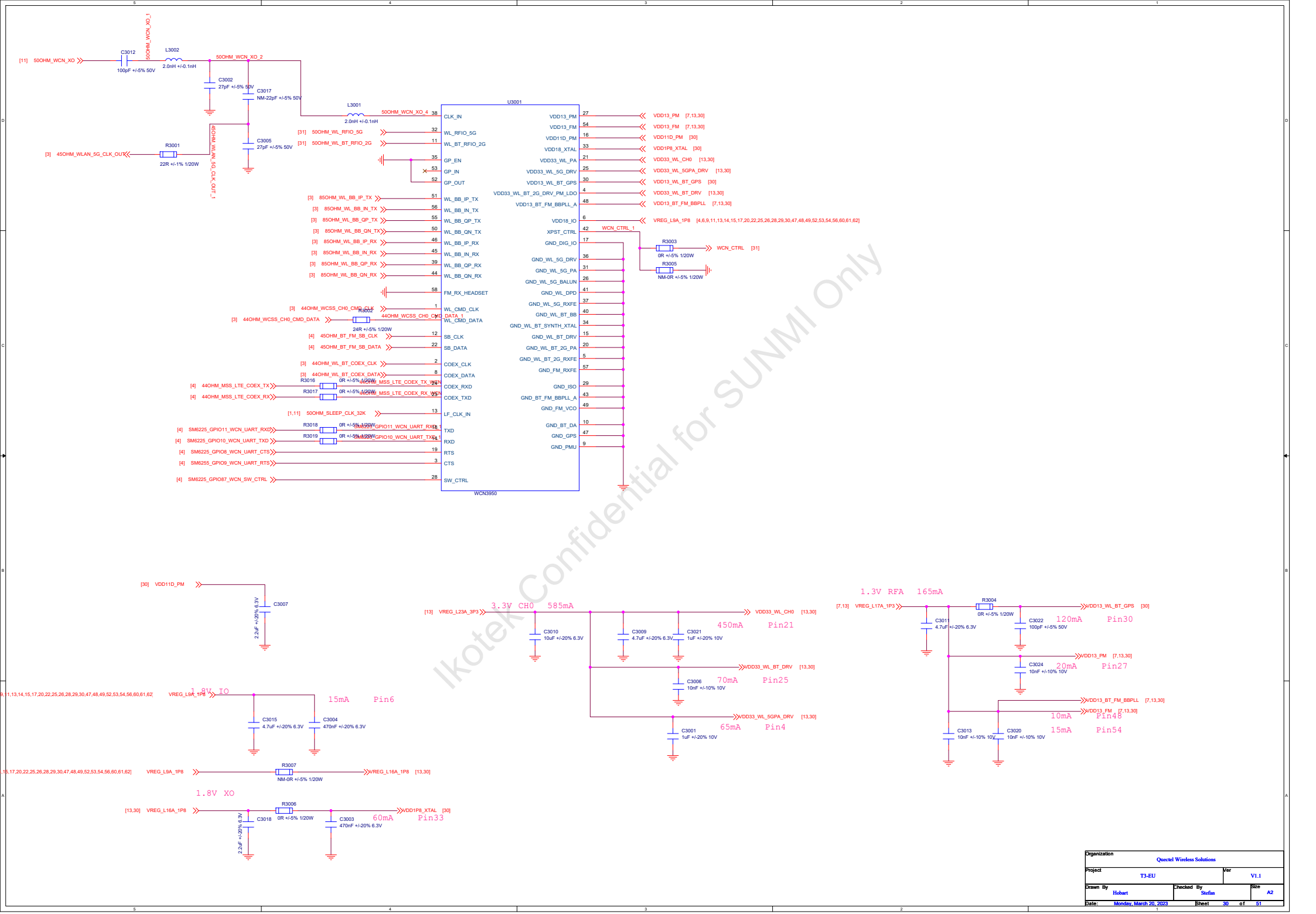
Organization	Quectel Wireless Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
Size	A2		
Date:	Monday, March 20, 2023	Sheet	29 of 51



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Organization	Quectel Wireless Solutions		
Project	T3-EU		Ver V1.1
Drawn By Hobart		Checked By Stefan	Size A2
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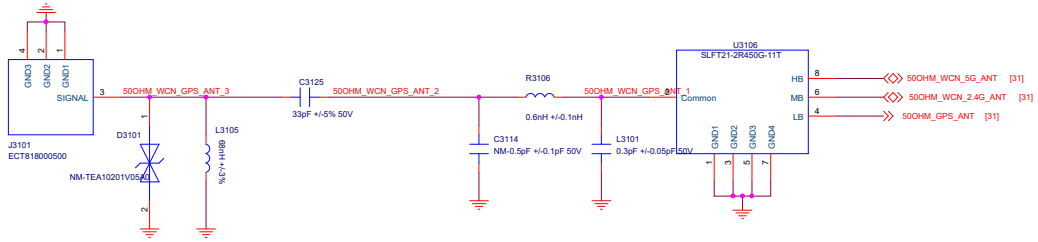
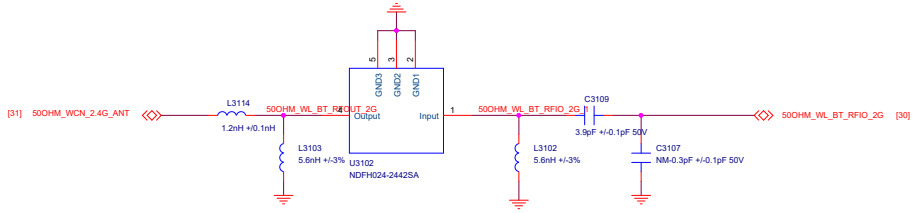
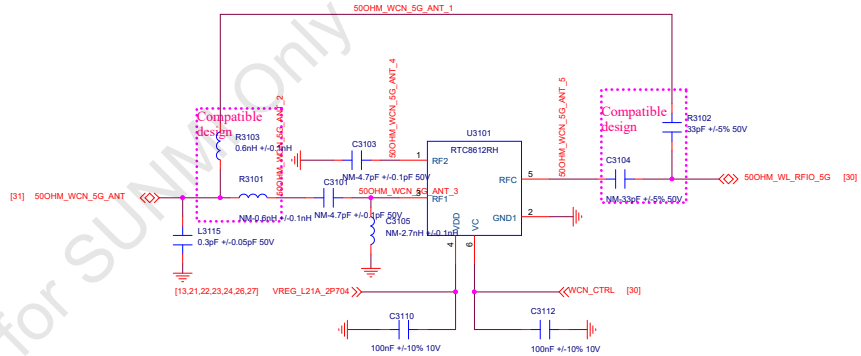
WIFI_BT_GPS_ANT



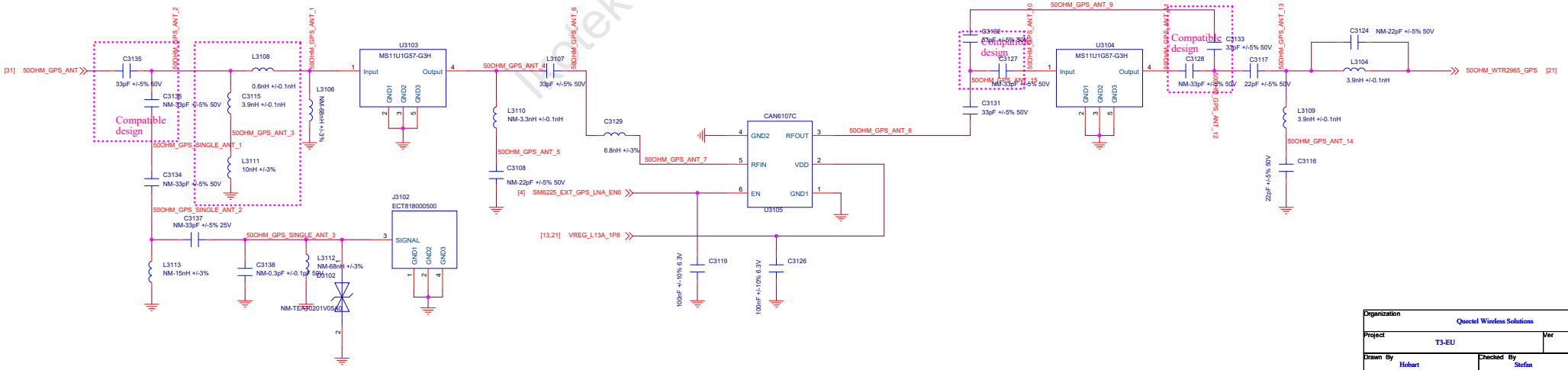
WCN





GPS

Notch filter: If B13 is supported, B13 Notch is required
to suppress 2nd order harmonics of B13 TX.



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Organization	Quectel Wireless Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Hobart	Checked By	Stefan
Size	A2		
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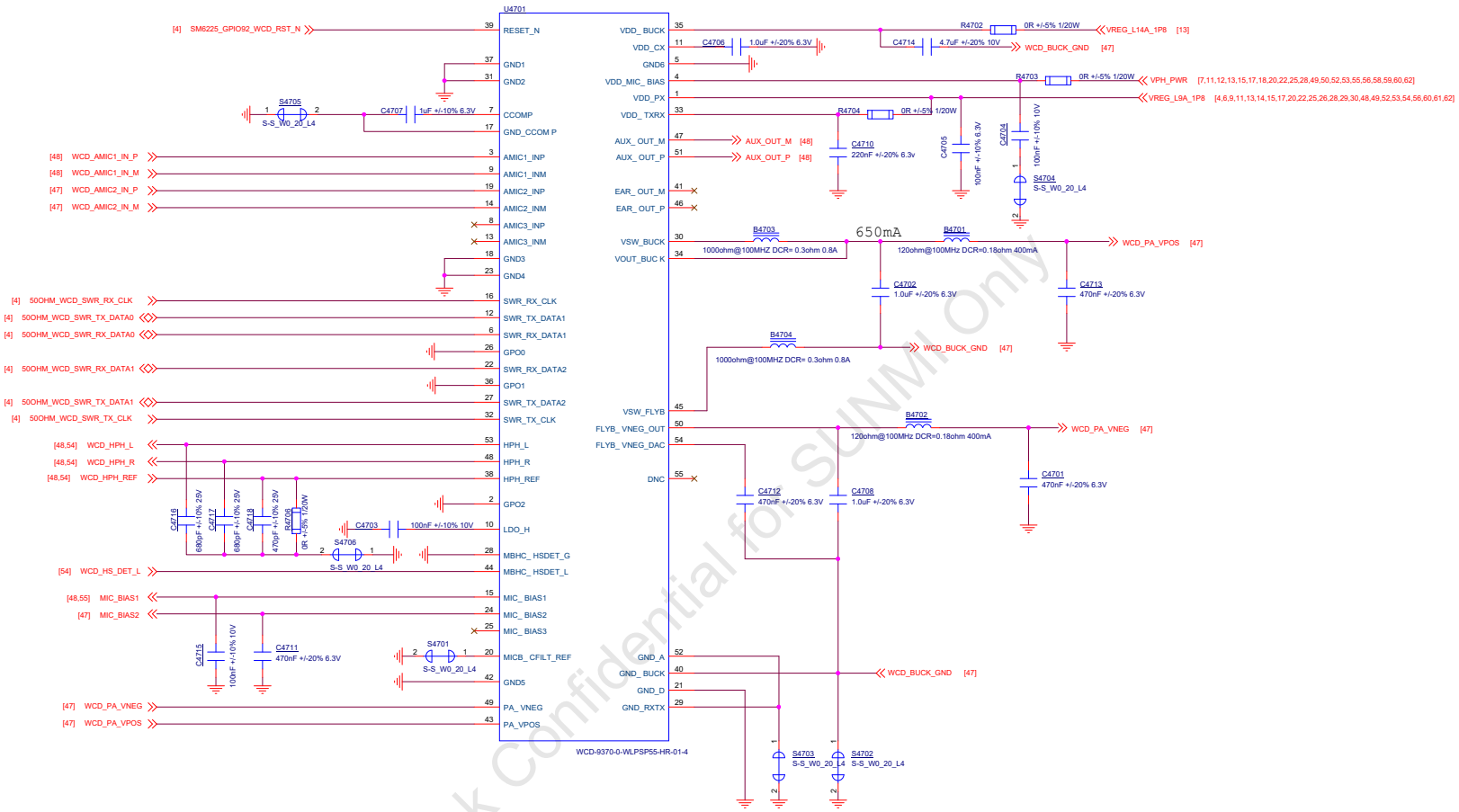
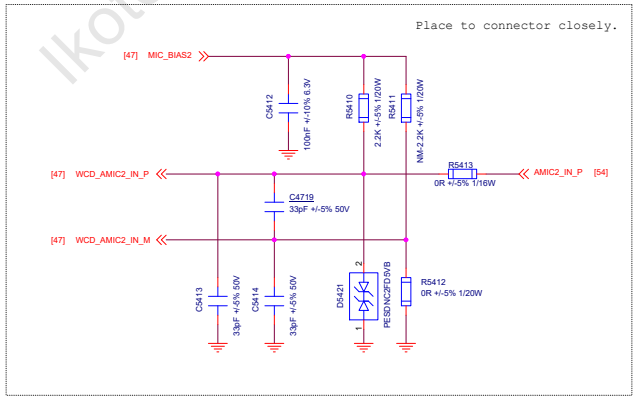
CODEC





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Organization	Quectel ODM Solutions		
Project	T3-EU	Ver	V1.1
Drawn By	Dongy	Checked By	Honson
Size	A2		
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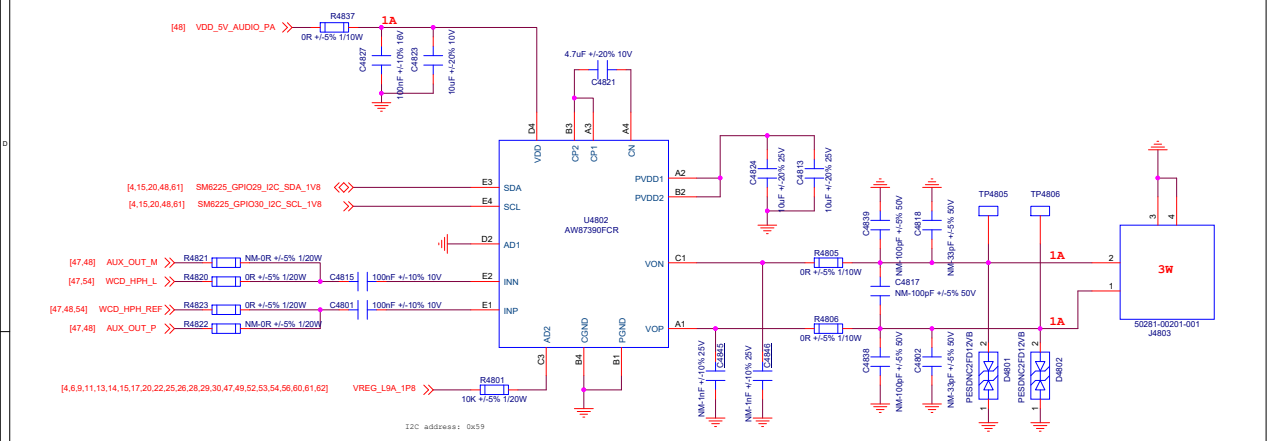
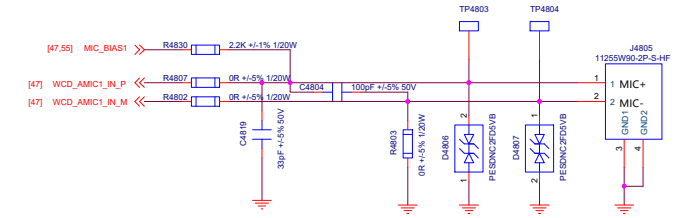
SPK_L



AMIC



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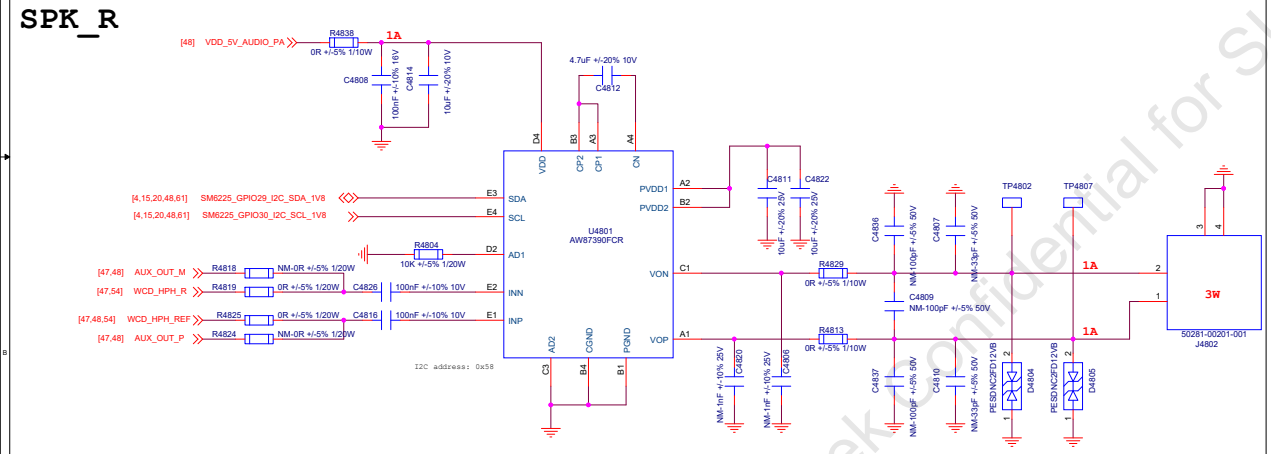
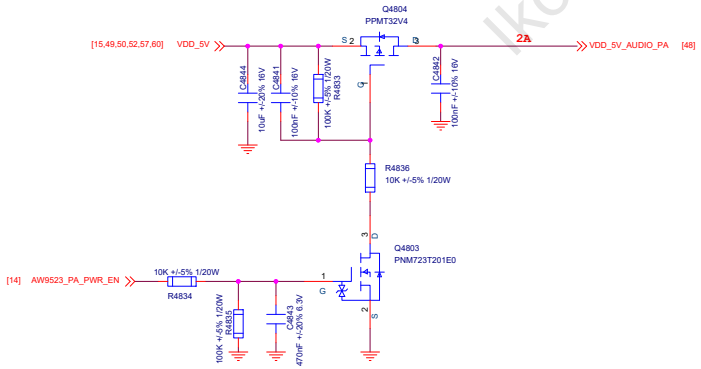
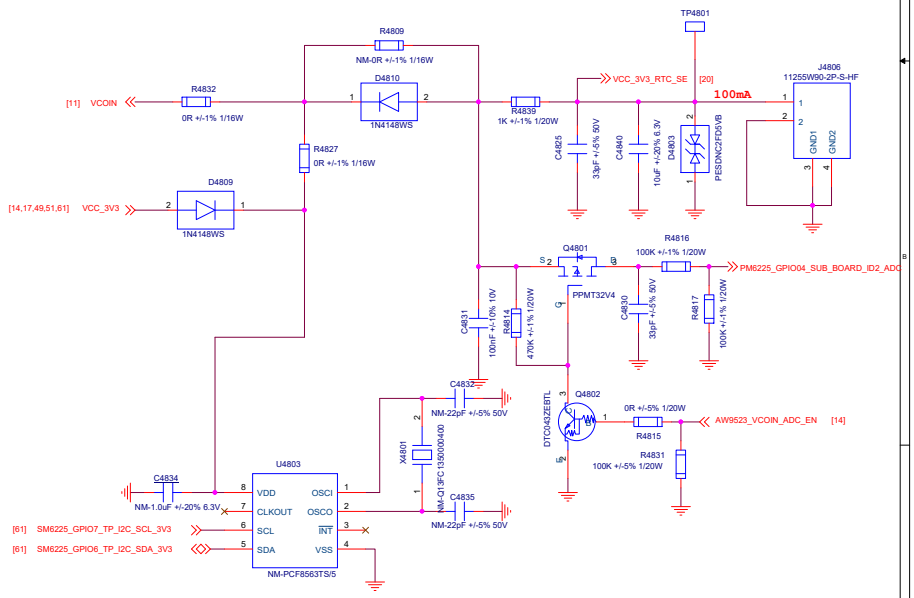




RTC



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Drawn By Dongy	Checked By Honson		Size A2
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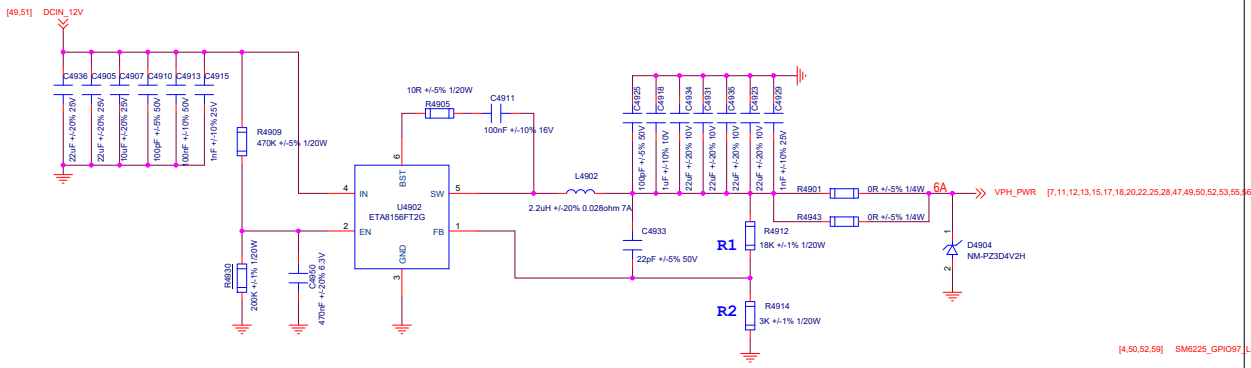
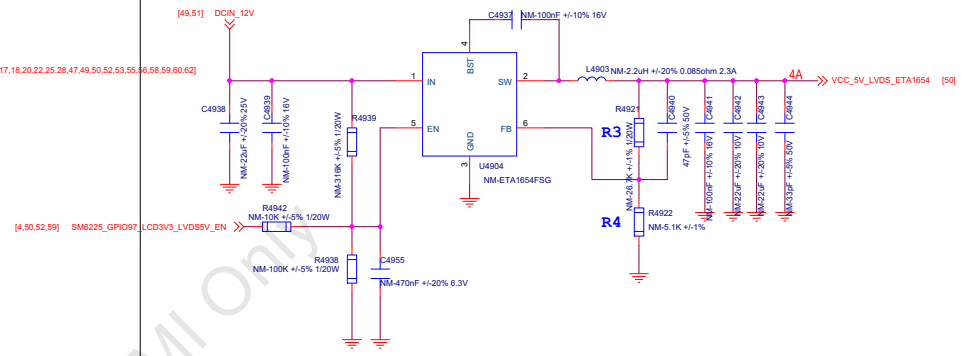
DC12V to 4V



VOUT=0.6*(R1/R2+1)=4.2V

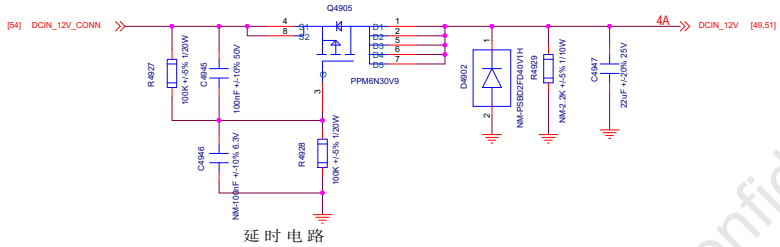
ETA8156FT2G Resistors R2 has to between 1K to 24K

DC12V to 5V

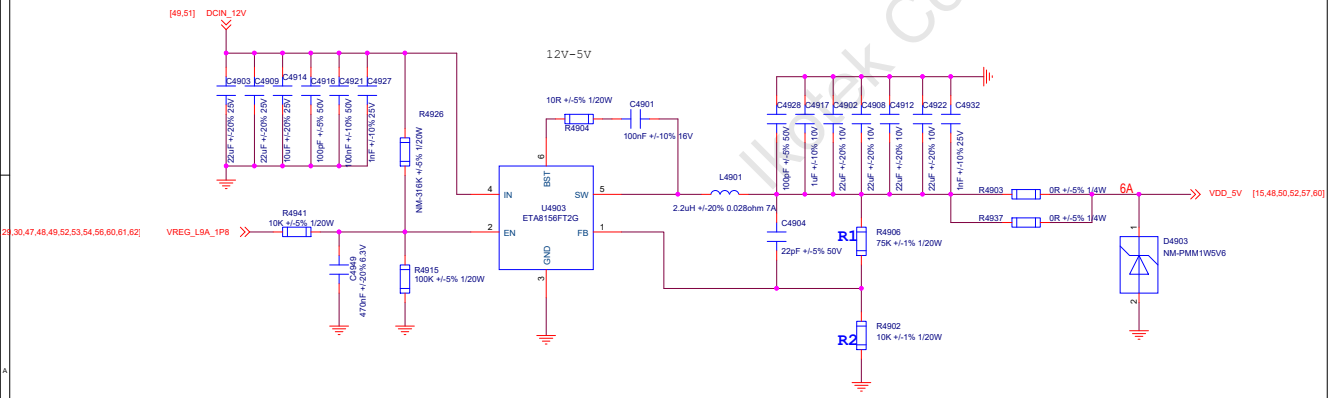


VOUT=0.805*(R3/R4+1)=5.019V

DC12V to 5V



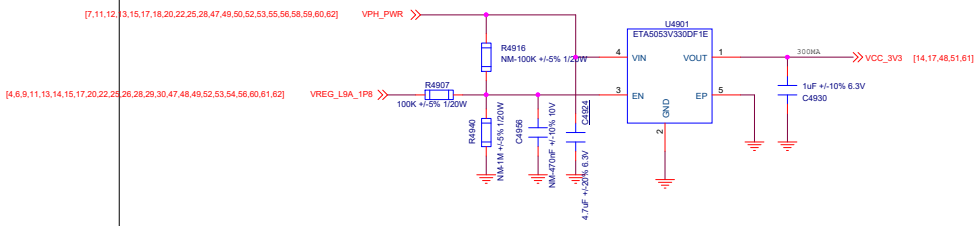
延时电路

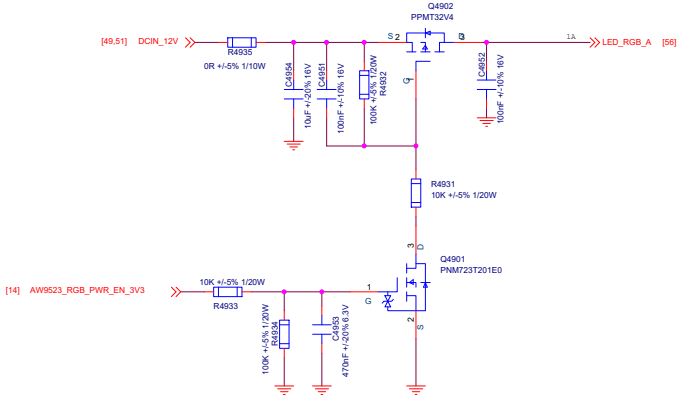


VOUT=0.6*(R1/R2+1)=5.1V

ETA8156FT2G Resistors R2 has to between 1K to 24K

VCC_3V3





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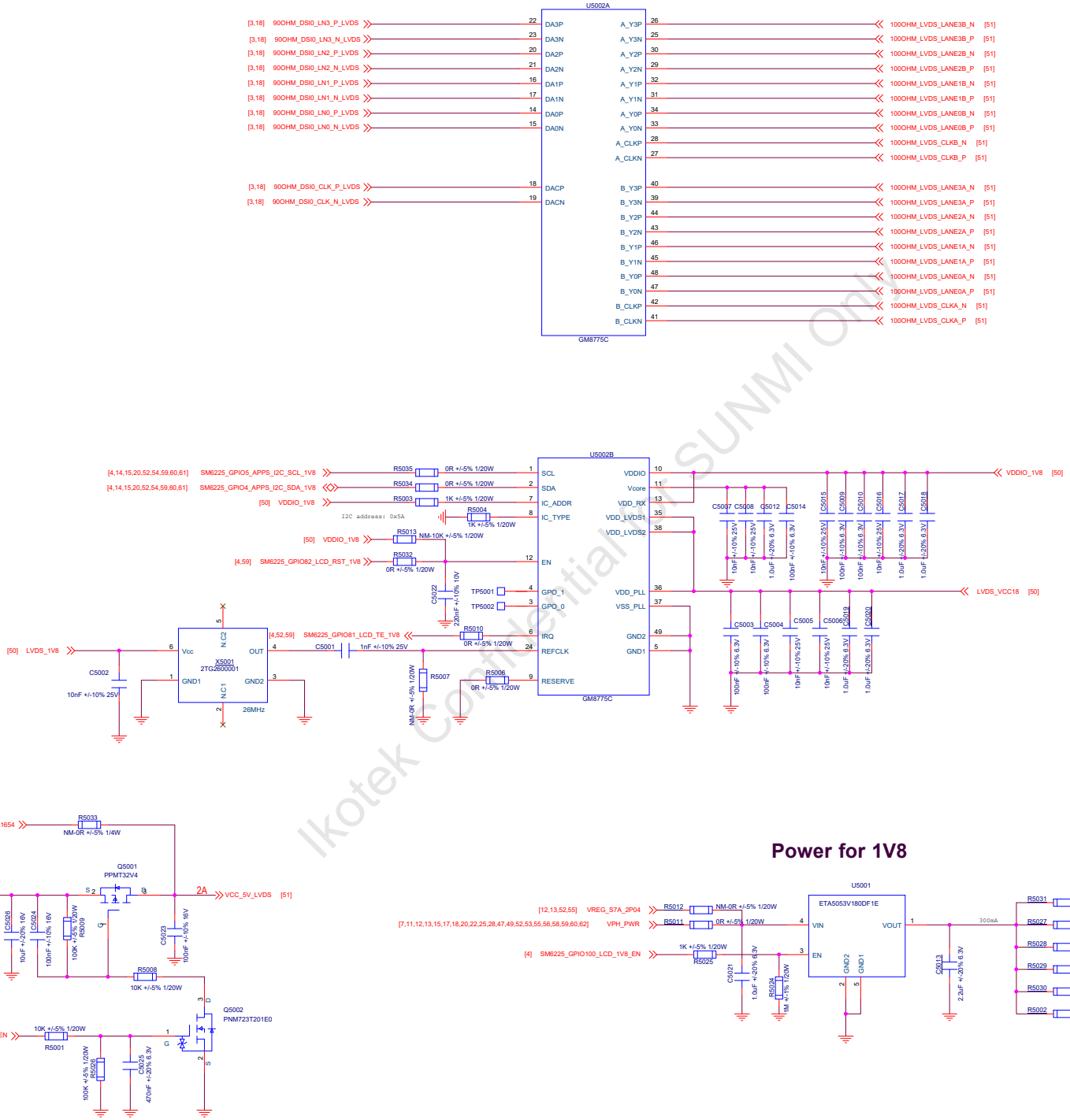
GM8775C



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Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
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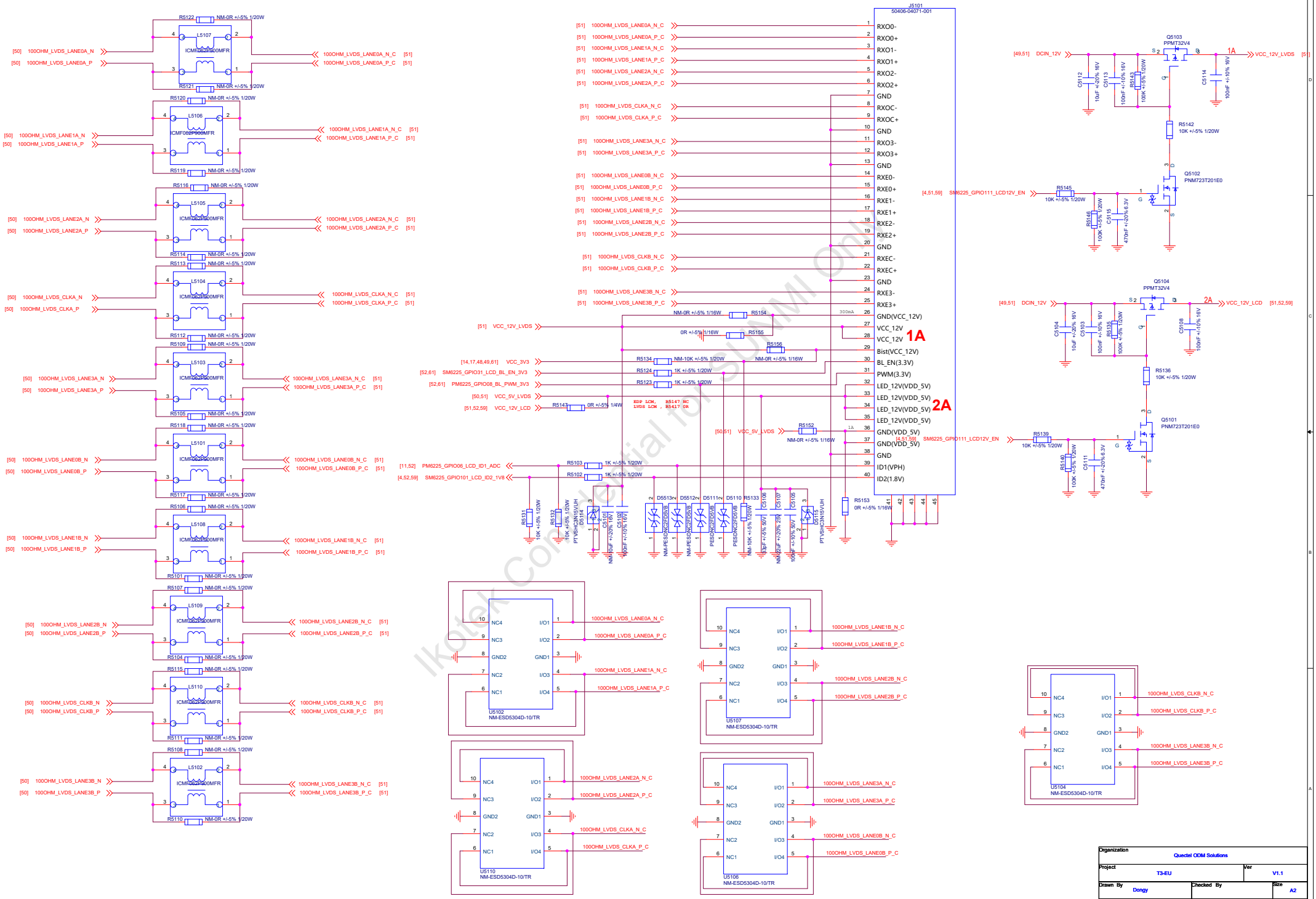
LVDS_CONNECTOR



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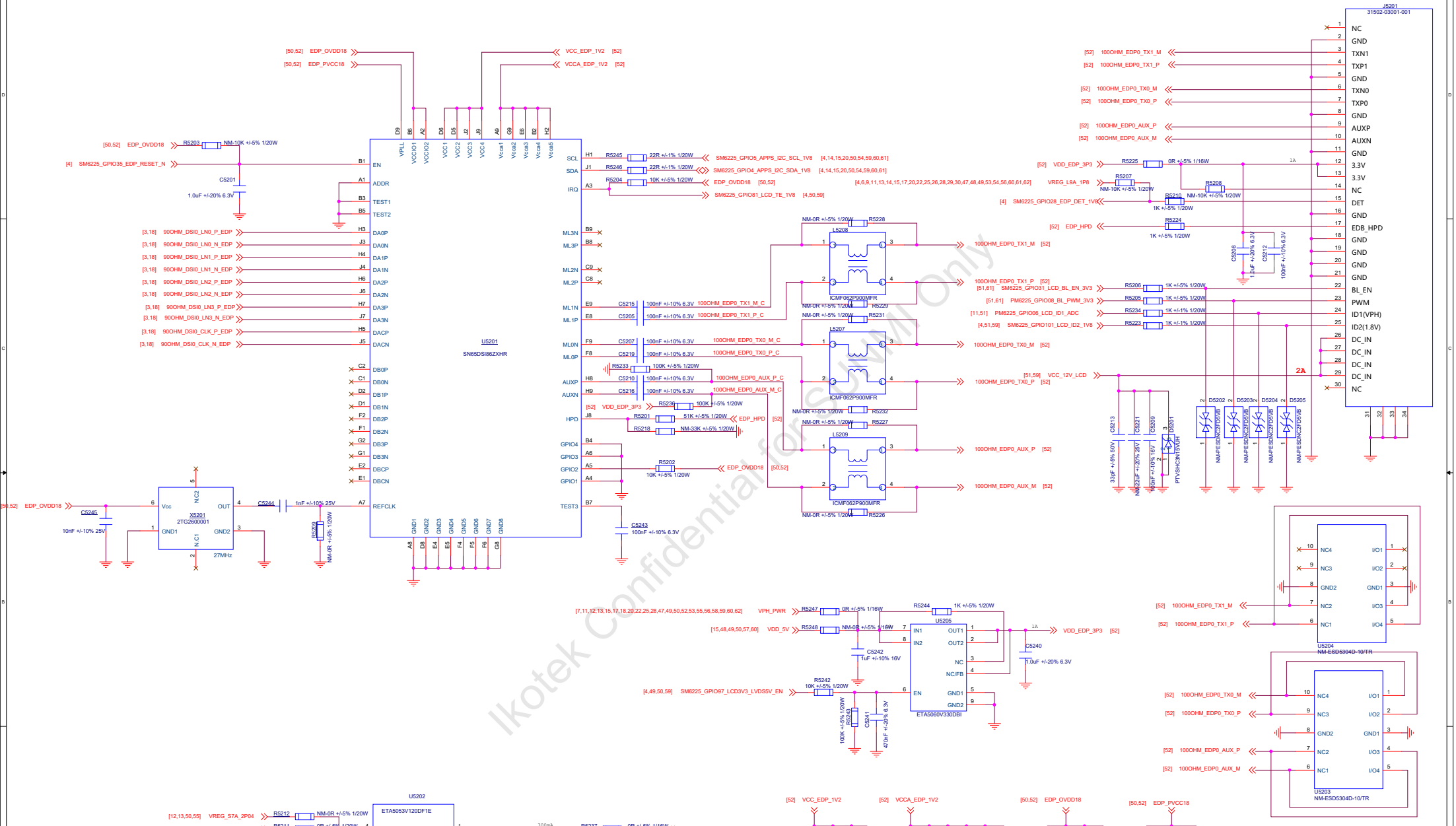
eDP LCM



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Organization	Quectel ODM Solutions
Project	T3-EU
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Checked By	Honson
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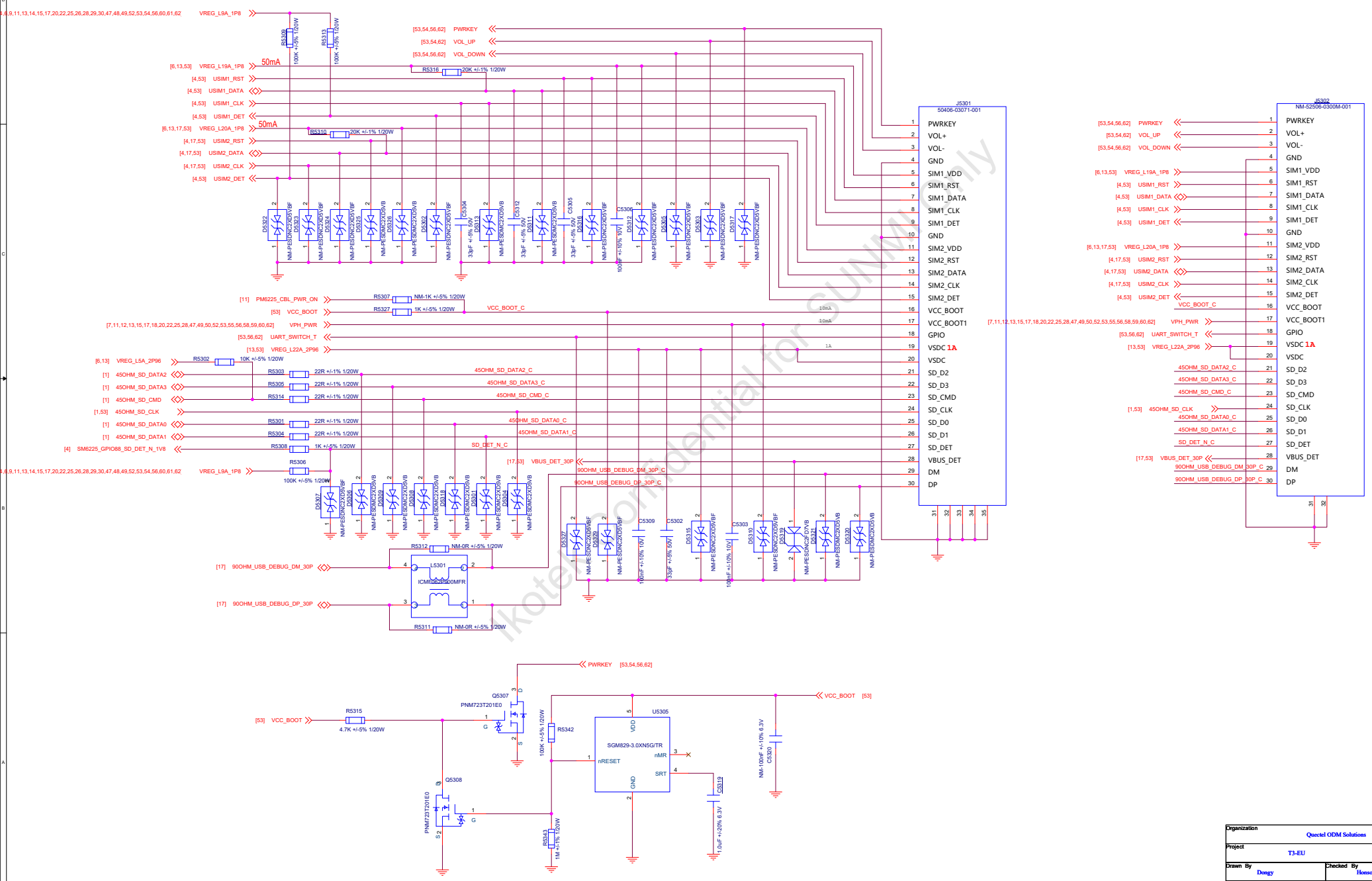
30P CONNECTOR



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Organization	Quectel ODM Solutions
Project	T3-EU
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Checked By	Honson
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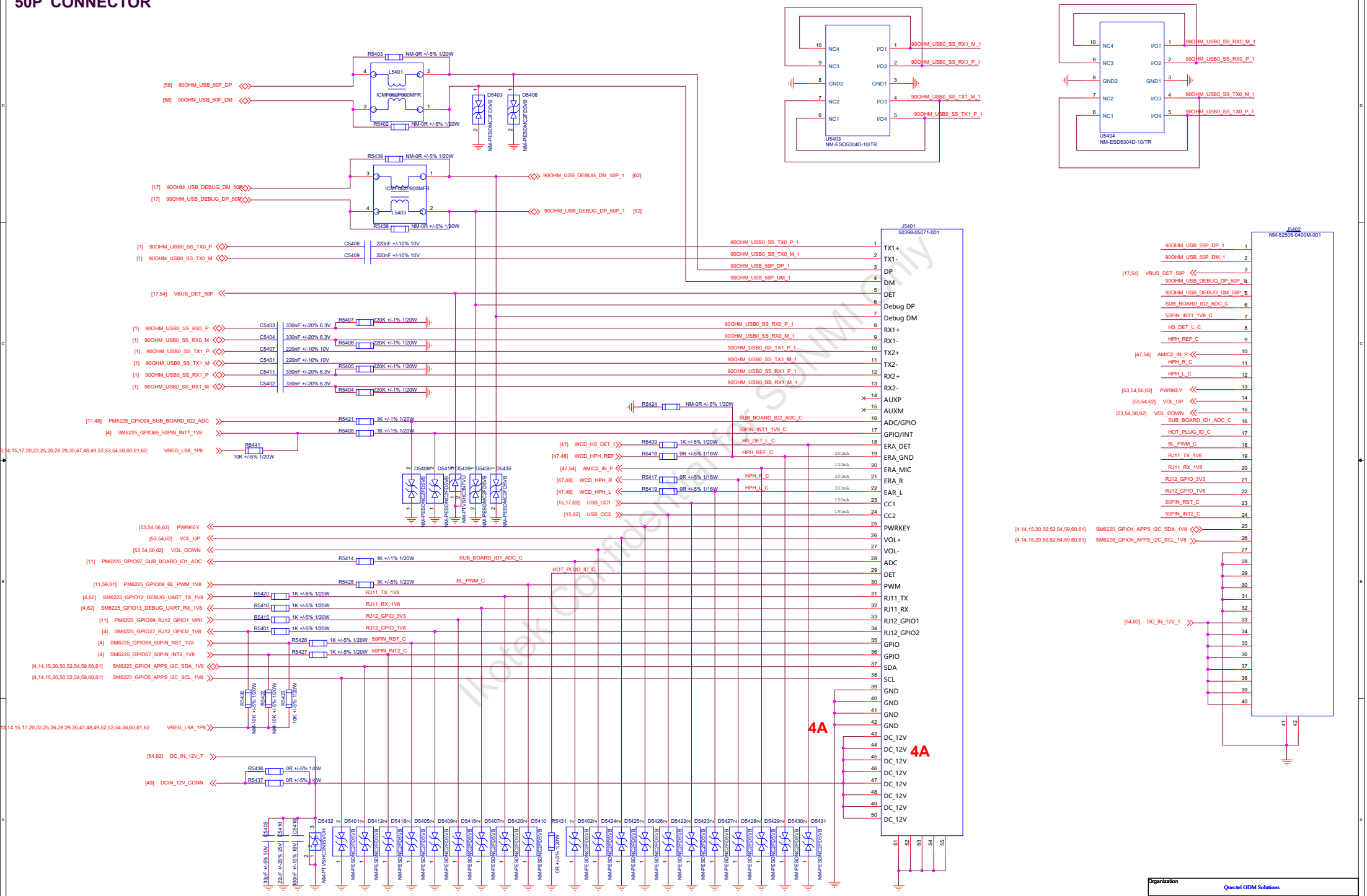
50P CONNECTOR



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Organization	Quectel ODM Solutions
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Checked By	Honson
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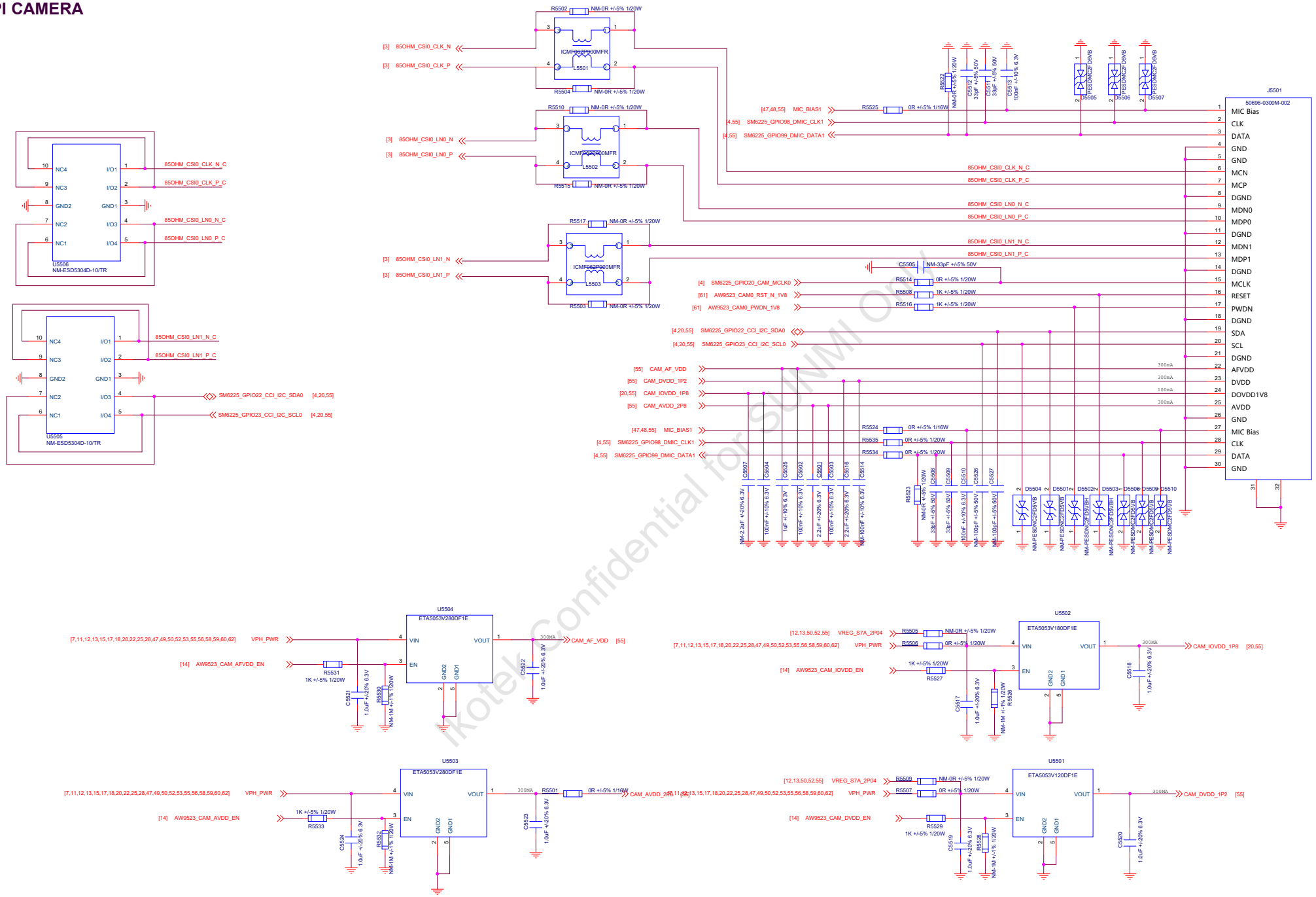
MIPI CAMERA



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Organization	Quectel ODM Solutions
Project	T3-EU
Ver	V1.1
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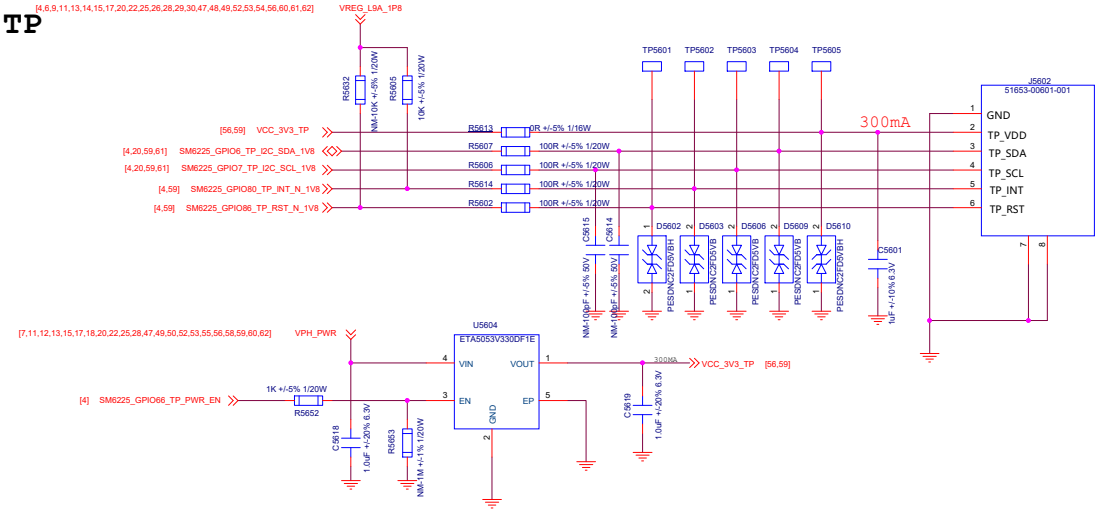
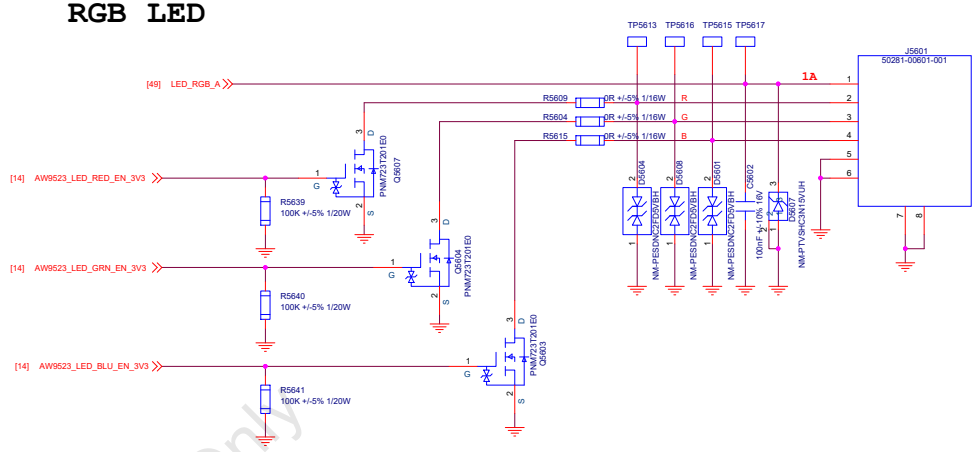
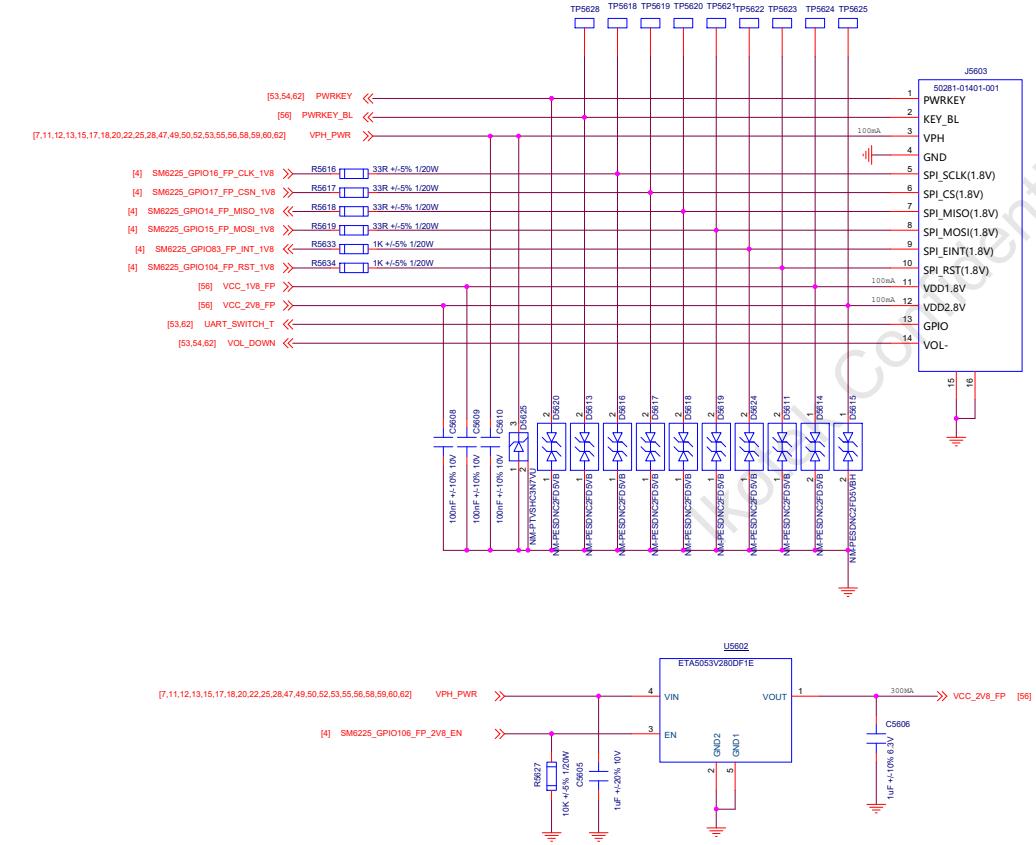
TP



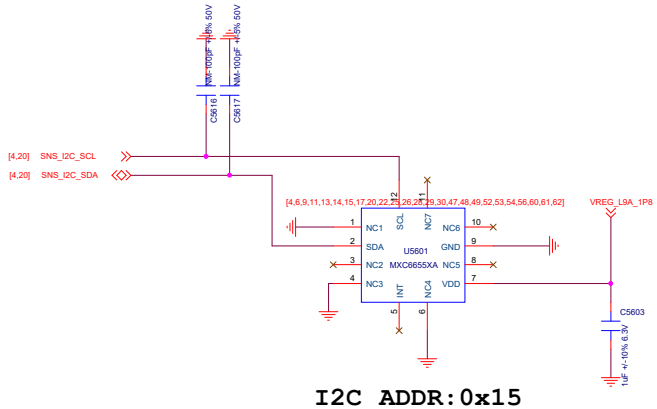
RGB LED



PWRKEY



G-SENSOR



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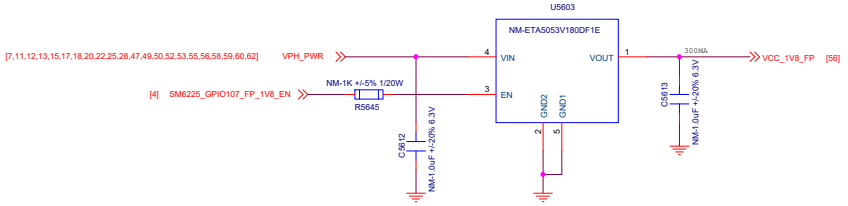

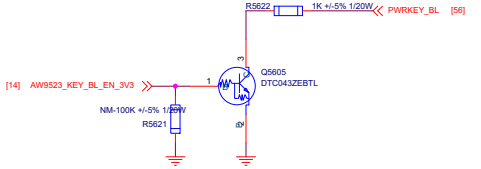

Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
Date: Monday, March 20, 2023	Sheet 56 of 63		

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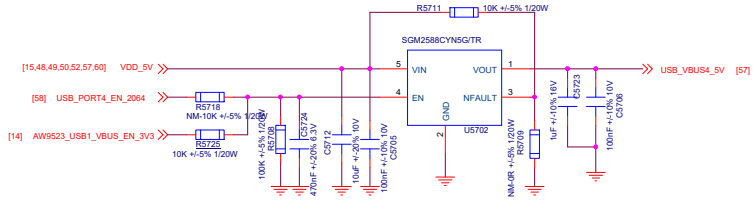
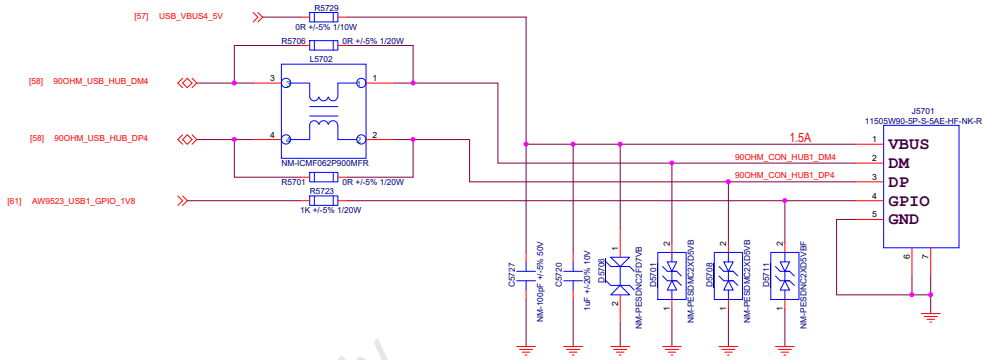
USB CON

USB1_VBUS_OCP





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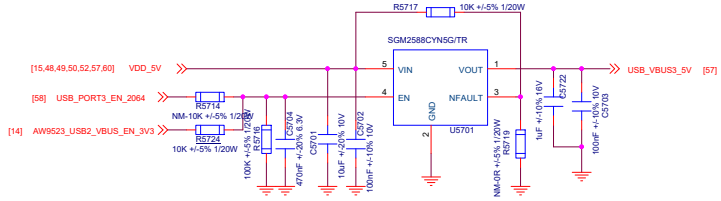

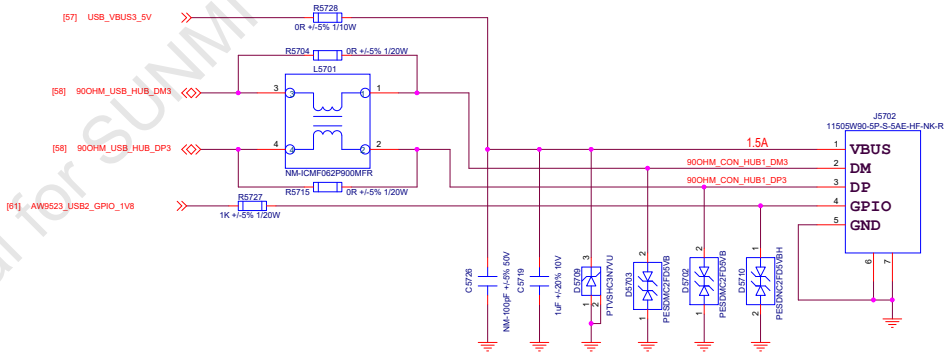

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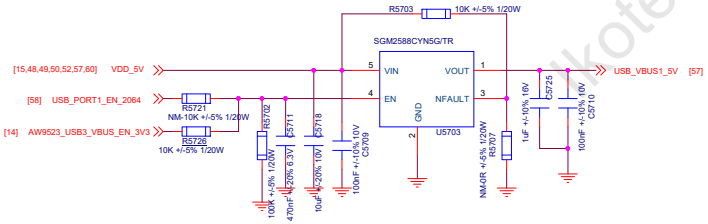

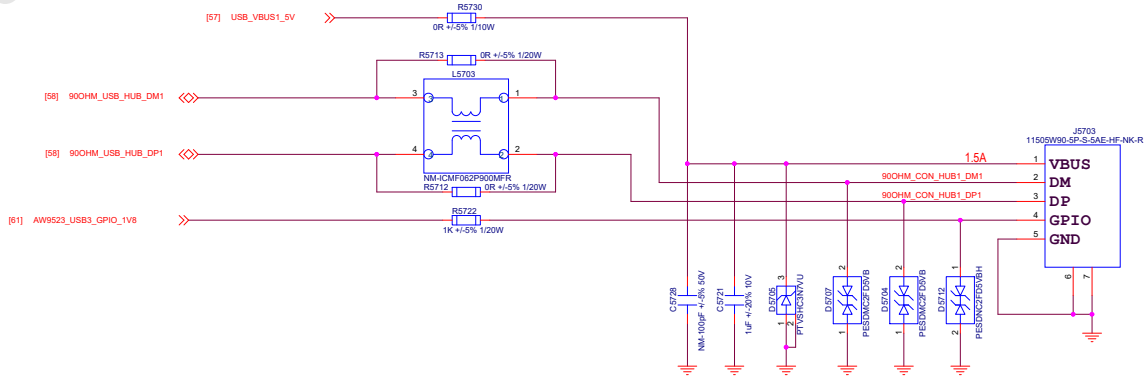

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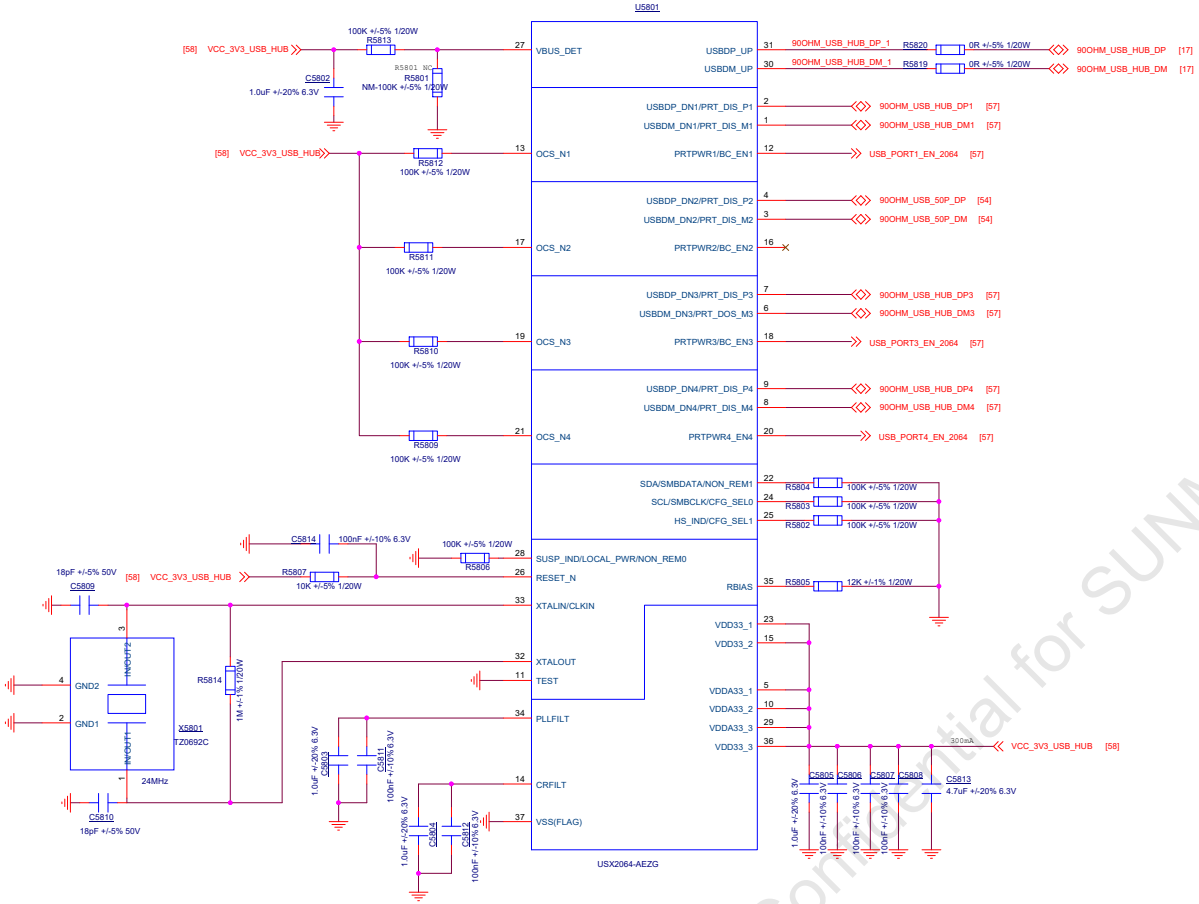
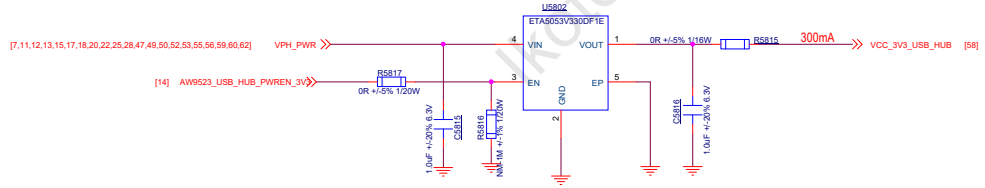
Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
Date: Monday, March 20, 2023	Sheet 57 of 83		





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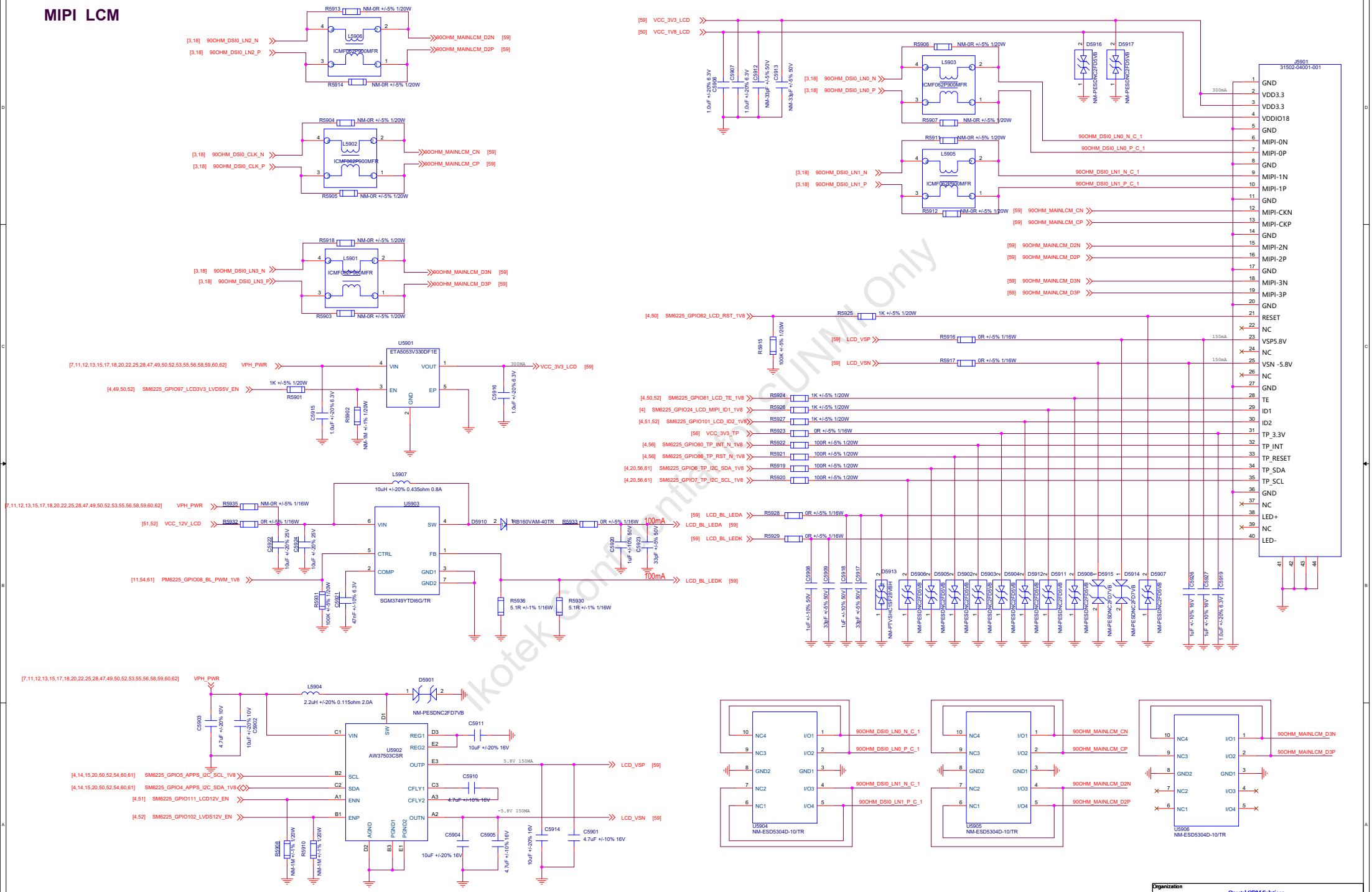
Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
Date: Monday, March 20, 2023	Sheet 58 of 63		

MIPI LCM



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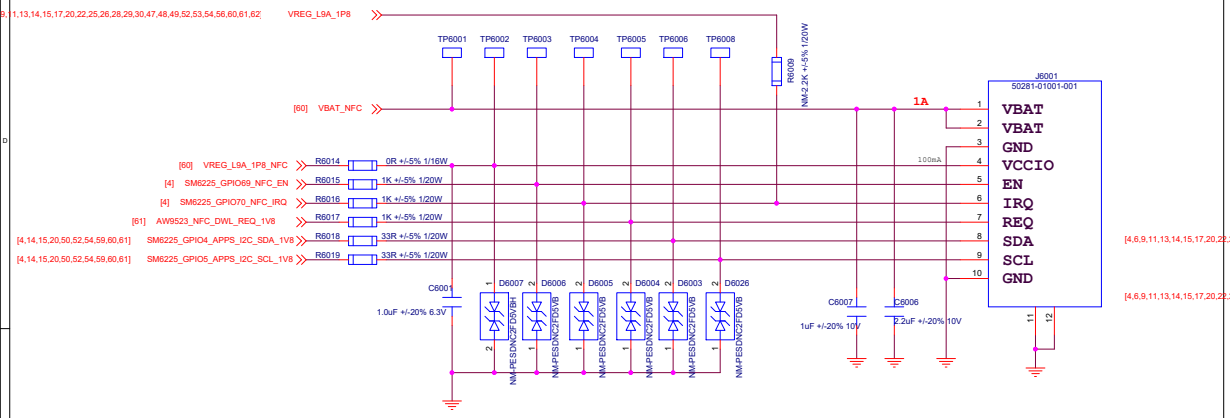
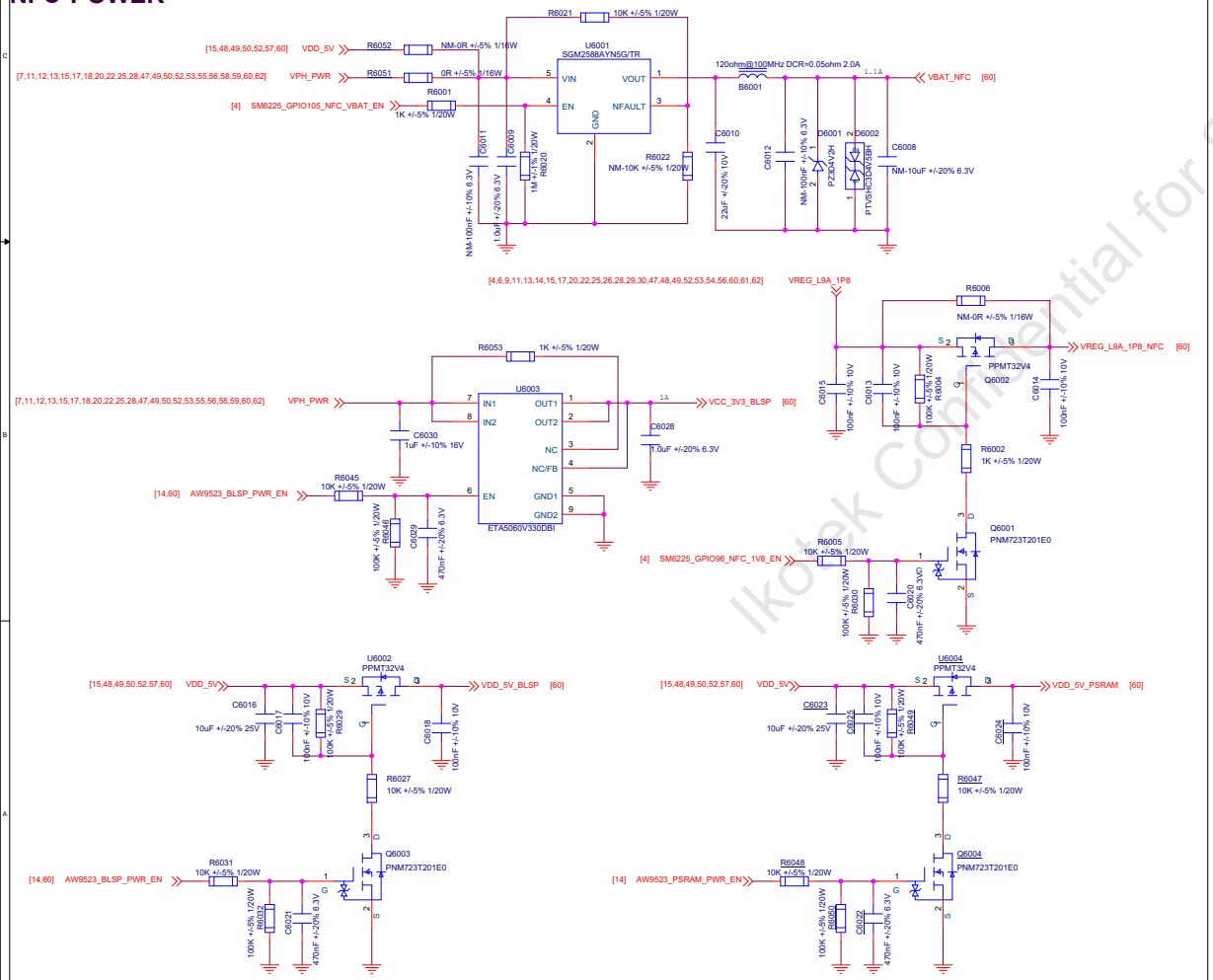
Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
Date: Monday, March 20, 2023	Sheet 59 of 83		

NFC



NFC POWER



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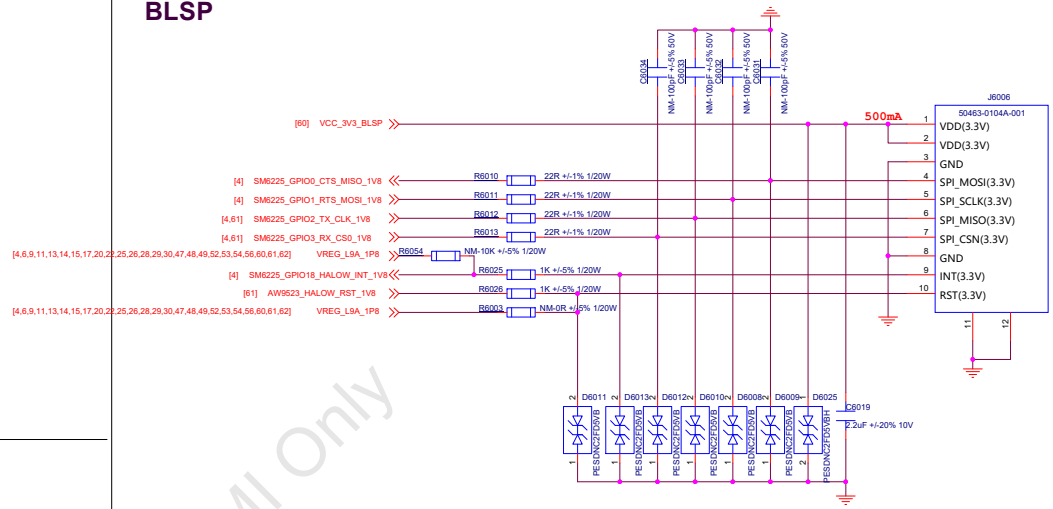

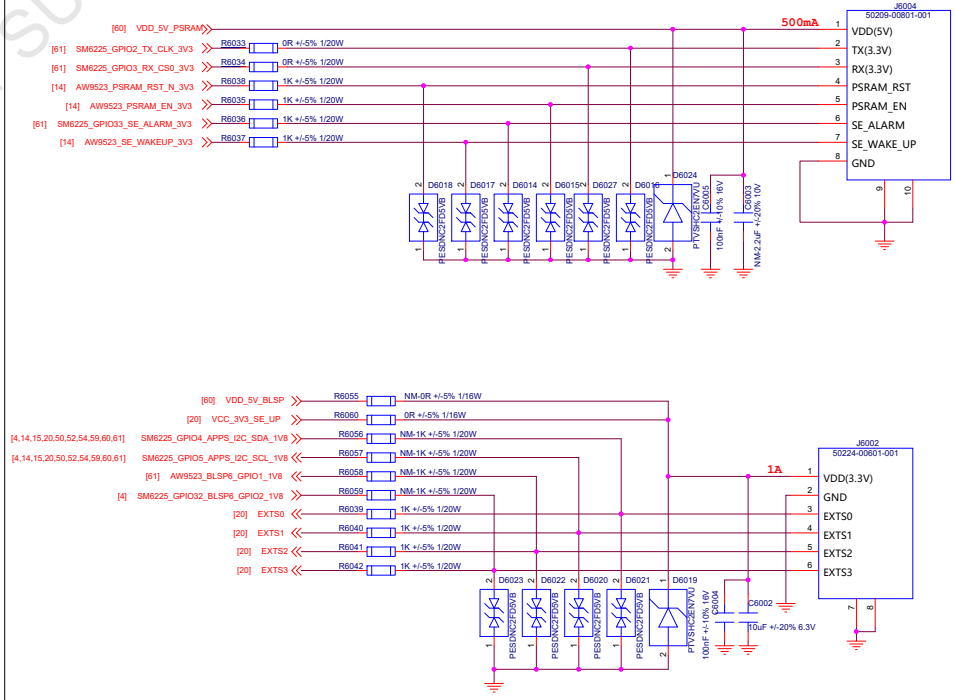

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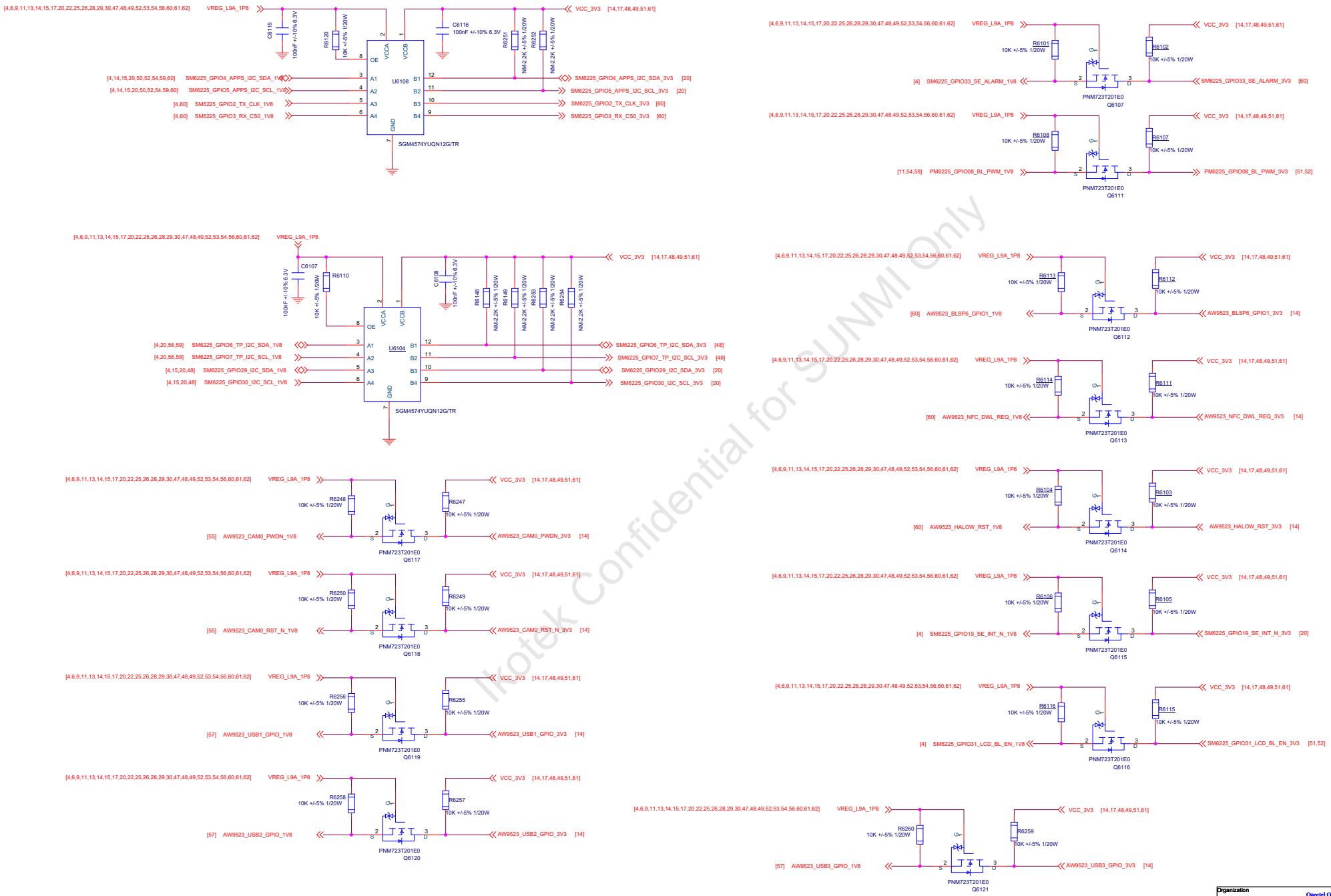
Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy	Checked By Honson		Size A2
Date: Monday, March 20, 2023	Sheet 60 of 63		

QUP[0]



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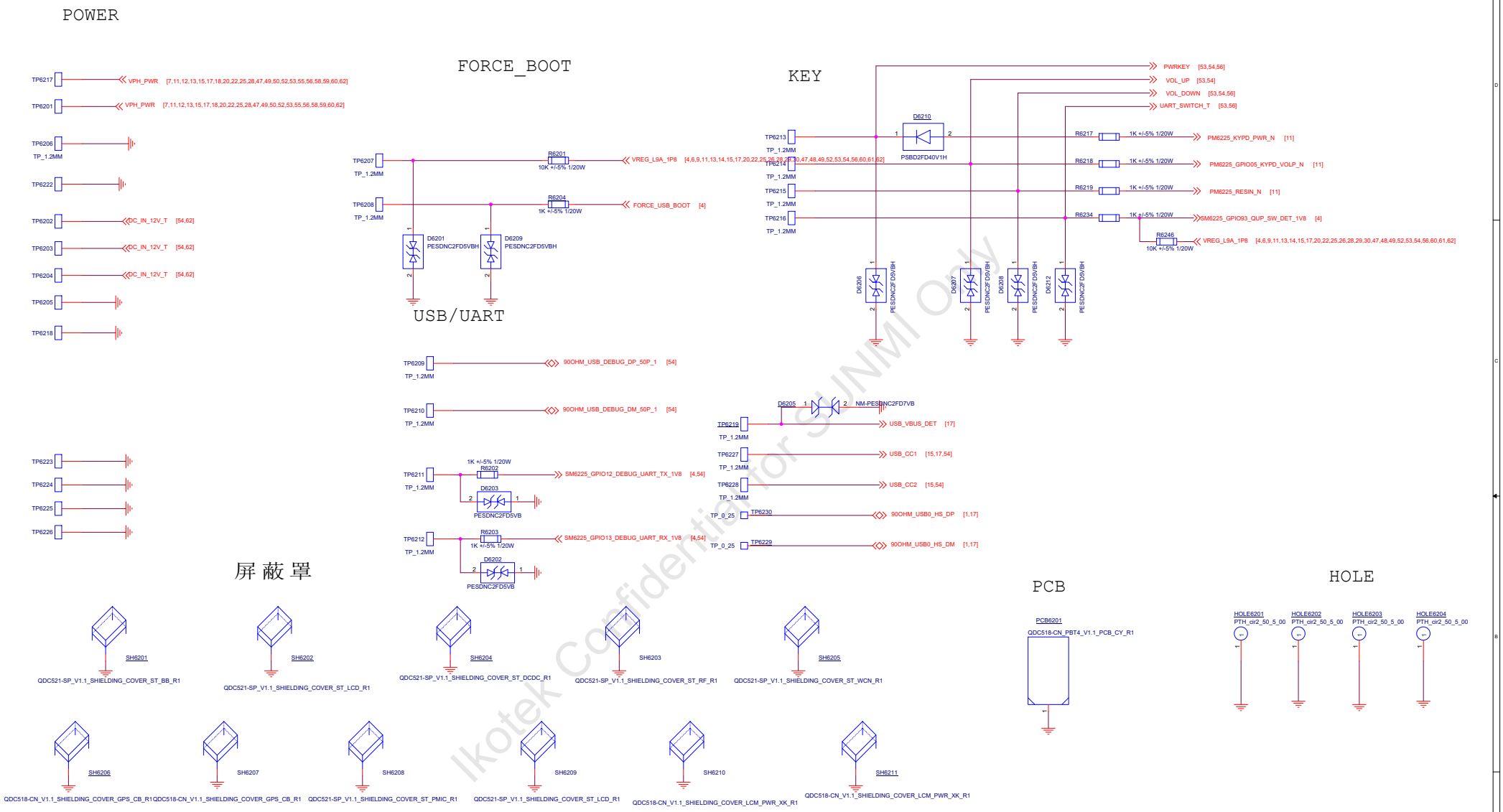
Organization	Quectel ODM Solutions		
Project	T3-EU		Ver V1.1
Drawn By Dongy		Checked By Honson	Size A2
Date: Monday, March 20, 2023		Sheet 61 of 63	



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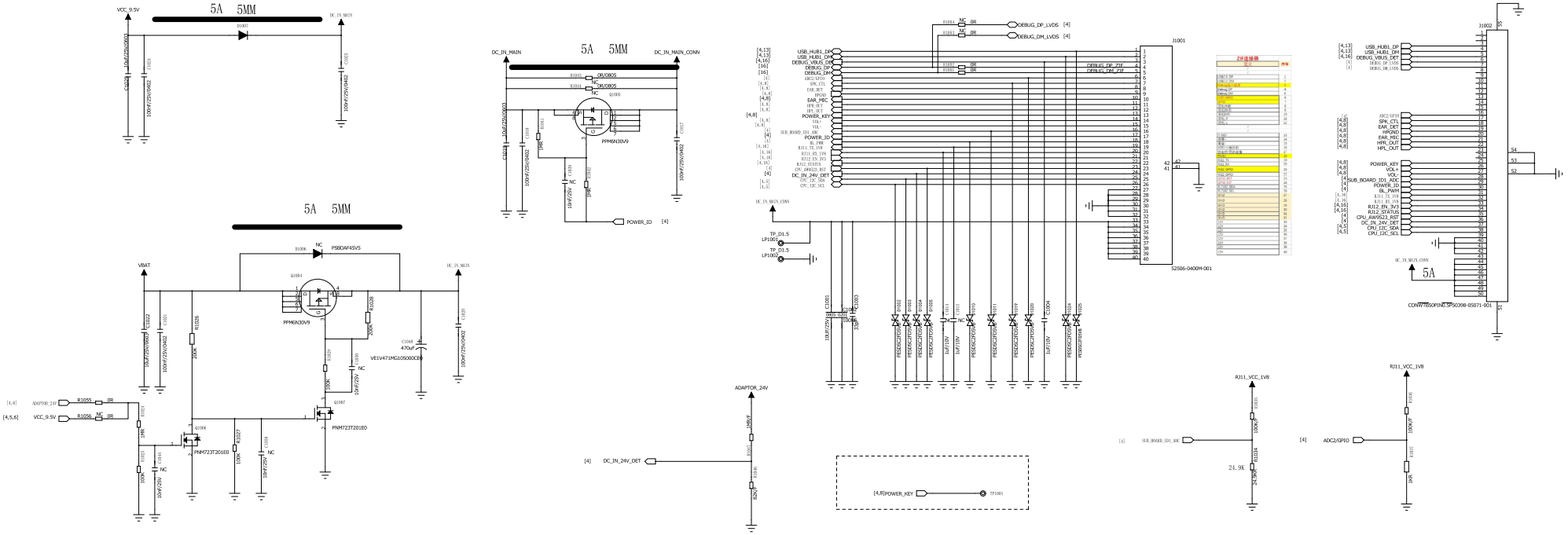
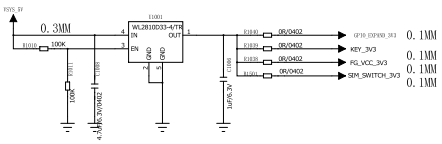
Title	<Title>		
Size A2	Document Number <Doc>		Rev <RevCode>
Date: Monday, March 20, 2023	Sheet 62 of 63		

IO CONNECT

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:





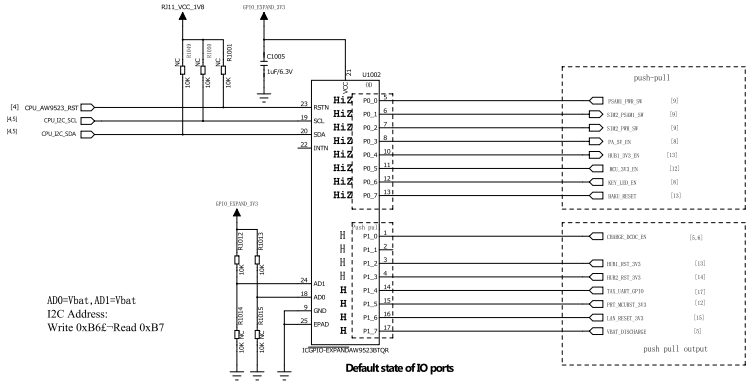


Table 1. Default state of IO ports , AD1/AD0 and P0_x/P1_x

AD1	AD0	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
GND	GND	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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AW9523B datasheet
May 2016 V1.1.1

GND	VBAT	0	0	0	0	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VBAT	GND	1	1	1	1	0	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	0	0	0	0
VBAT	VBAT	1	1	1	1	1	1	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

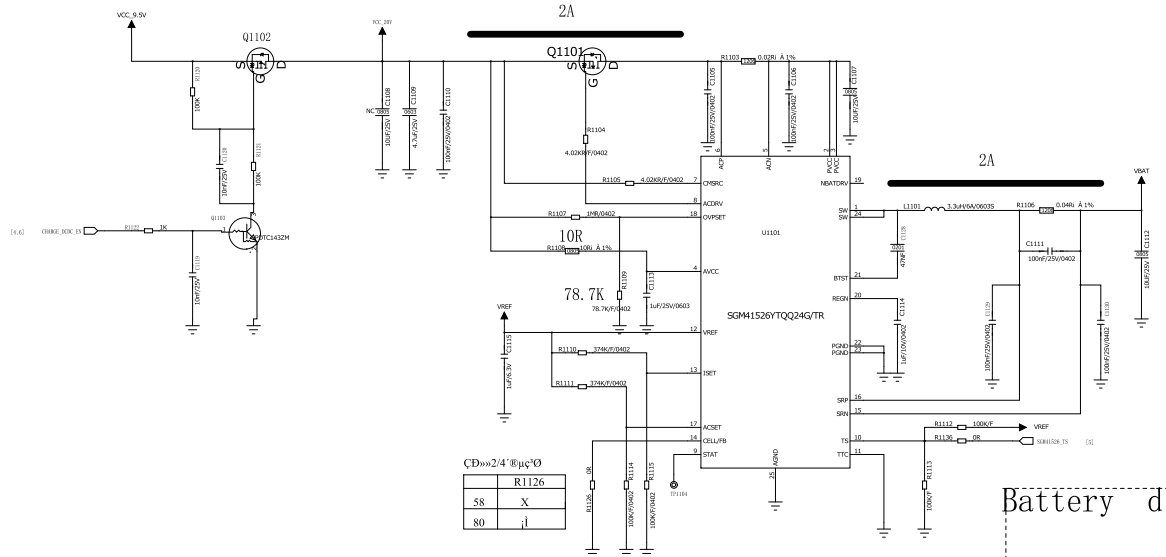
1	0	1	1	0	AD1	AD0	R/$\overline{W}$

AD1/AD0 value match with AW9523B pin AD1/AD0 respectively

COMPANY:	Sunmi		
TITLE:	Luxembourg		
DRAWN: ZMQ	DATED: 23.02.27		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE: <Code>	SIZE: A0	DRAWING NO: 01.BLOCK DIAGRANG	REV: V2.0.C
SCALE: <Scale>		SHEET: 4 OF 18	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

58 Battery CON



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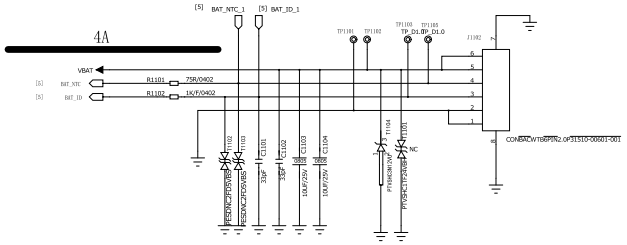
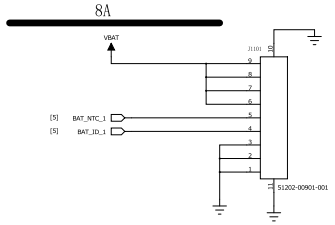
	R1126
58	X
80	¡ì

Table 1. Defining Number of Battery Cells for SGM41526

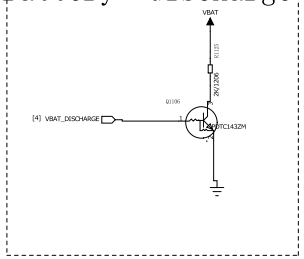
CELL Pin Voltage	Charge Voltage Regulation
Floating	8.4V (2 Cells)
VREF	12.6V (3 Cells)
AGND	16.8V (4 Cells)



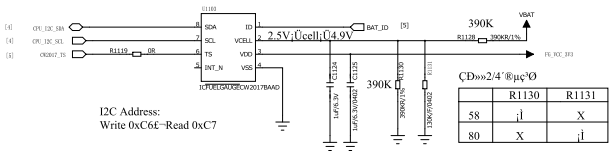
80 Battery CON



Battery discharge



Fuel Gauge



I2C Address:
Write 0xC6E~Read 0xC7

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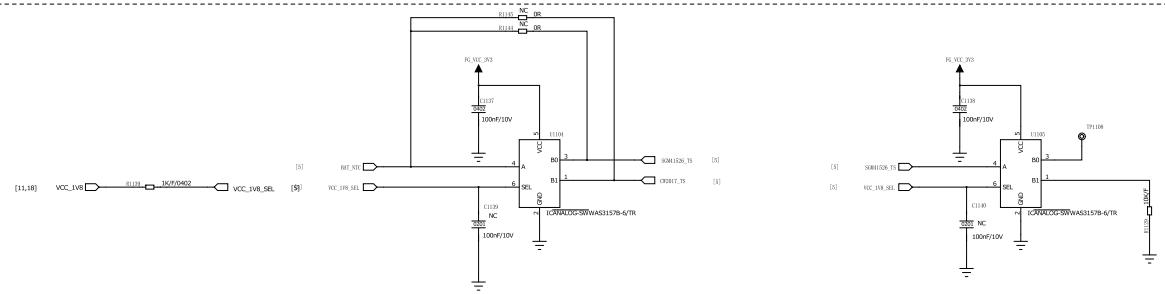
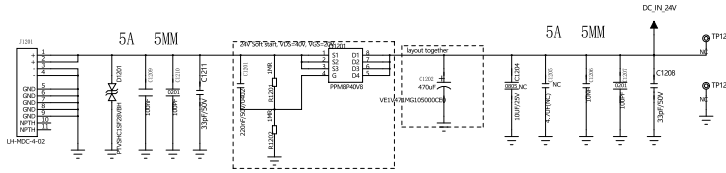
	R1130	R1131
58	¡ì	X
80	X	¡ì



Logic Level (SEL pin, Pin 6)	Function
L	B0 connected to A
H	B1 connected to A

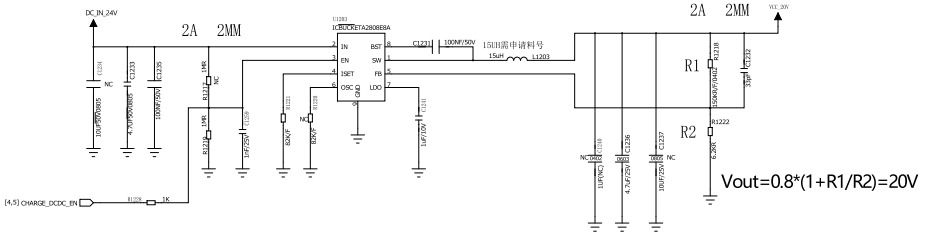
COMPANY: Sunmi			
TITLE: Luxembourg			
DRAWN: ZMQ	DATED: 23.02.27		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
RELEASED: <Released By>	DATED: <Release Date>		
SCALE: <Scale>		SHEET: 5 OF 18	

24V DCIN

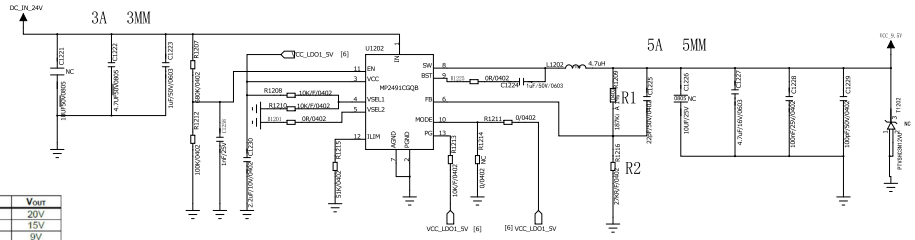


Reference FTP:DC-IN_STD_SCH_V1.1_20221209

DCDC 24V-20V 3A



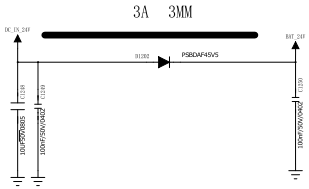
DCDC 24V-9.5V 6A



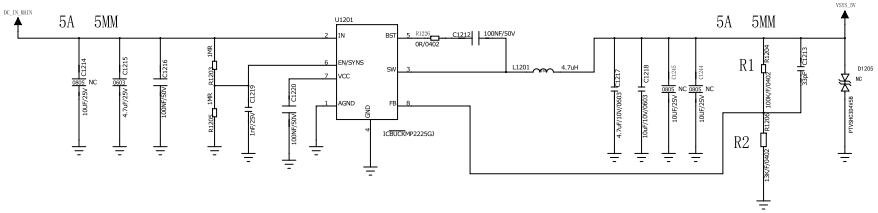
VSEL1	VSEL2	V_{REF}	V_{OUT}
0	0	2V	20V
VCC	0	1.5V	15V
0	VCC	0.9V	9V
1/2*VCC	0	1.2V	12V
VCC	VCC	0.5V	5V

Vout=1.2V*(1+R1/R2)

Reference FTP:Manila_MB_SCH_V1.0.A_20220826-1536



DCDC VBAT/9.5V - 5V 5A



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COMPANY: Sunmi			
TITLE: Luxembourg			
DRAWN: ZMQ	DATED: 23.02.27		
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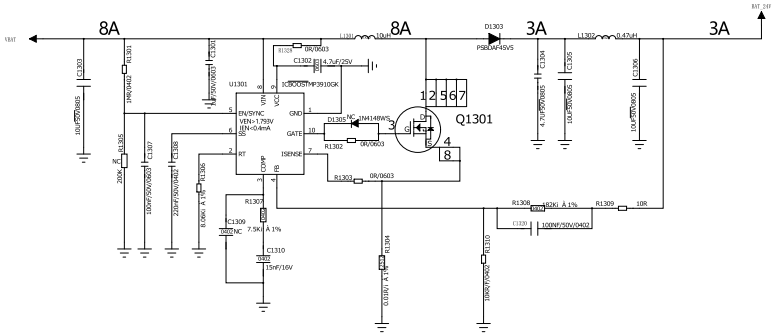
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 6 OF 18

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: Luxembourg	
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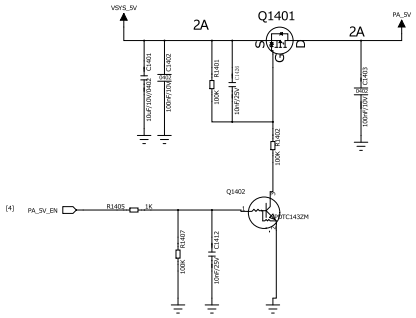
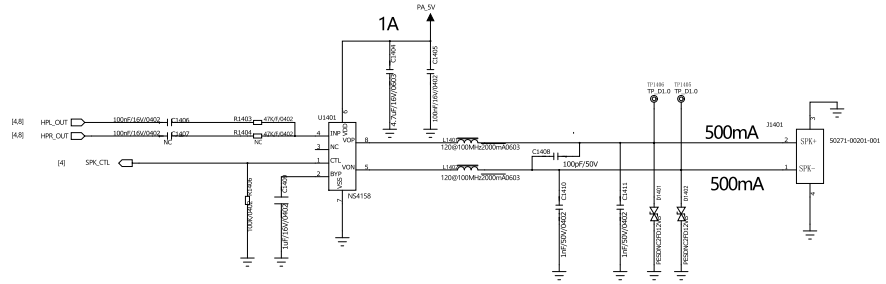
		SCALE: <Scale>	SHEET: 7 OF 18

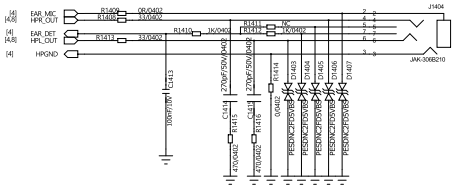
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Audio PA





Audio JACK



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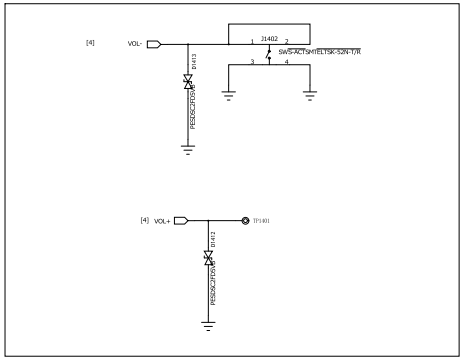

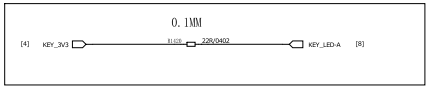

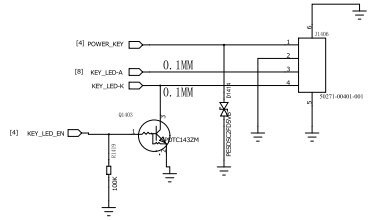

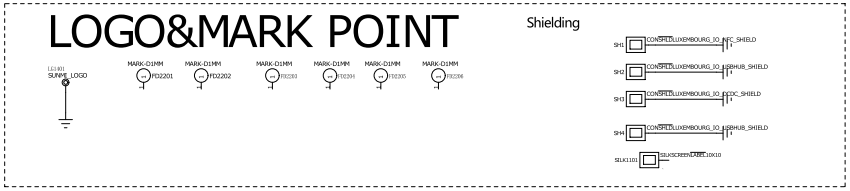

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TITLE: Luxembourg				
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CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0	DRAWING NO: 01.BLOCK DIAGRAM
QUALITY CONTROL: <QC By>	DATED: <QC Date>			REV: V2.0.C
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 8 OF 18

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

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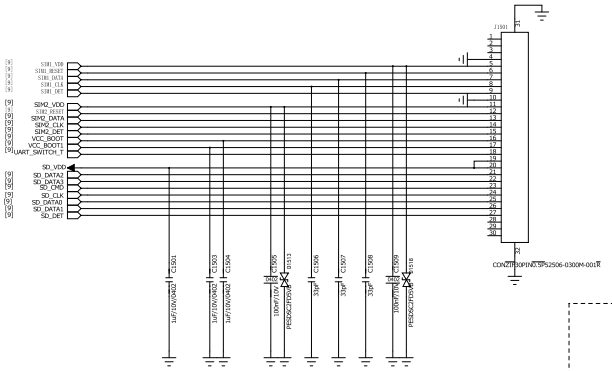
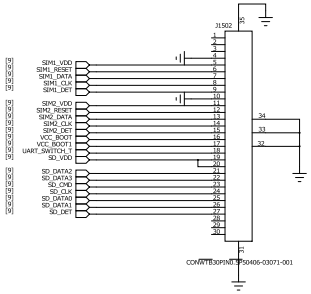
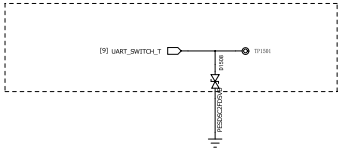


LVDS





序号	定义			序号	定义
1	POWERKEY	1.8V	开机键 and 音量-键进FASTBOOT	1	POWERKEY
2	VOL+	1.8V		2	VOL+
3	VOL-	1.8V		3	VOL-
4	GND			4	GND
5	SIM1_VDD	平台		5	SIM1_VDD
6	SIM1_RESET	1.8V		6	SIM1_RESET
7	SIM1_DATA			7	SIM1_DATA
8	SIM1_CLK			8	SIM1_CLK
9	SIM1_DET	1.8V		9	SIM1_DET
10	GND			10	GND
11	SIM2_VDD	平台		11	SIM2_VDD
12	SIM2_RESET	1.8V		12	SIM2_RESET
13	SIM2_DATA			13	SIM2_DATA
14	SIM2_CLK			14	SIM2_CLK
15	SIM2_DET	1.8V		15	SIM2_DET
16	VCC_BOOT		上电自启 硬件电路控制脚（核心板上设计PWR	16	VCC_BOOT
17	VCC_BOOT1		上电自启 VBAT	17	VCC_BOOT1
18	GPIO——QUP—Switch		用于QUP的debug和UART的切换,主板预留测试	18	GPIO——QUP—Switch
19	SDCARD_VDD	峰值700mA		19	SDCARD_VDD
20	SDCARD_VDD			20	SDCARD_VDD
21	SDCARD_D2			21	SDCARD_D2
22	SDCARD_D3			22	SDCARD_D3
23	SDCARD_CMD			23	SDCARD_CMD
24	SDCARD_CLK			24	SDCARD_CLK
25	SDCARD_D0			25	SDCARD_D0
26	SDCARD_D1			26	SDCARD_D1
27	SDCARD_DET	1.8V		27	SDCARD_DET
28	DEBUG_VBUS1	5V	底座优先级更高	28	DEBUG_VBUS1
29	USB_DEBUG_D-			29	USB_DEBUG_D-
30	USB_DEBUG_D+			30	USB_DEBUG_D+

①主板预留开机电路。
②高通同时兼容CBL开机电路方式

16 17pin连接在一起，则可以通过主板电路实现自动开机

返回

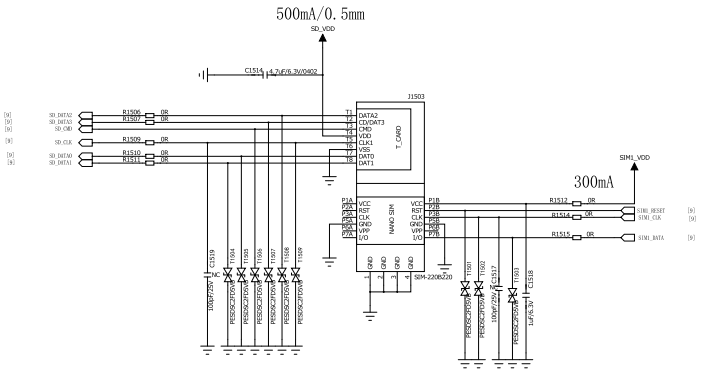
30PIN定义 LVDS连接器

连接器型号：S-50398-050

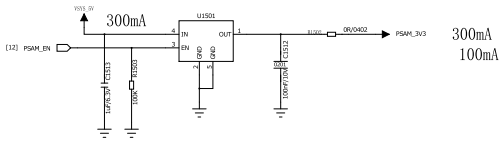
30PIN定义 ZIF连接器

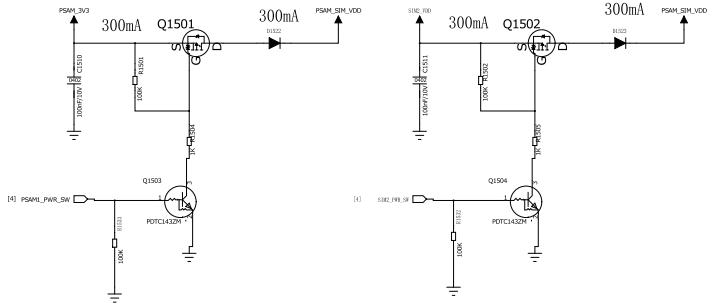
连接器型号： 52506-0300M-001

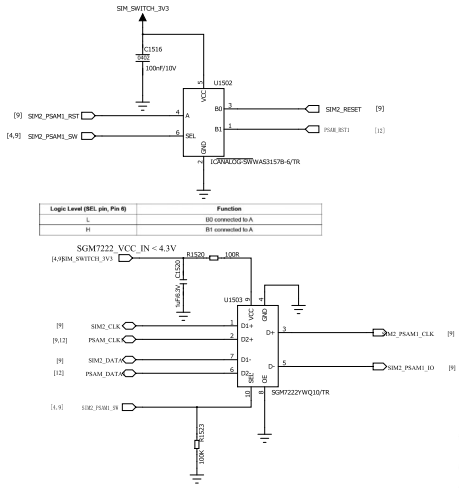
T+SIM1



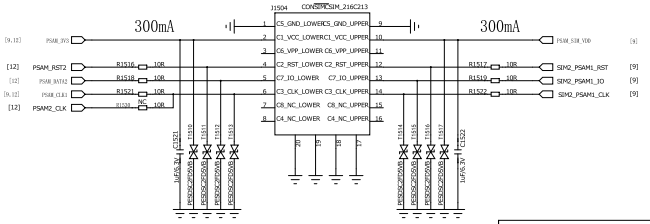
SIM2/PSAM1+PSAM2







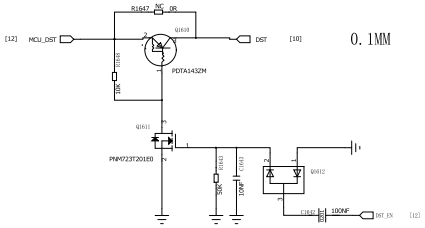
Logic Level (SEL pin, Pin 6)	Function
L	B0 connected to A
H	B1 connected to A



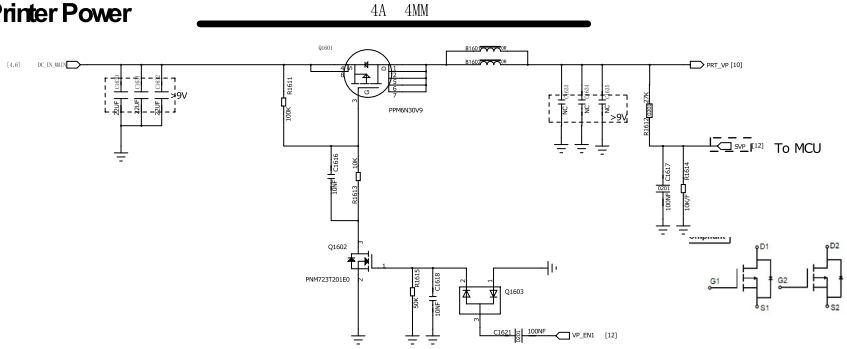
$\overline{OE}$	S	HSD1+ HSD1-	HSD2+ HSD2-
0	0	ON	OFF
0	1	OFF	ON
1	×	OFF	OFF

DRAWN: ZMQ	DATED: 23.02.27	COMPANY: Sunmi	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: Luxembourg	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
SCALE: <Scale>		SHEET: 9 OF 18	

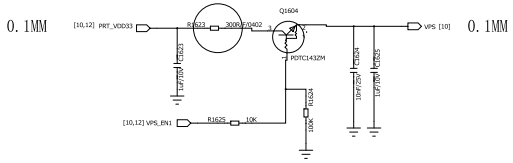
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



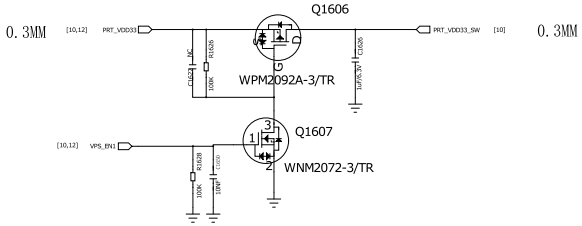
Printer Power



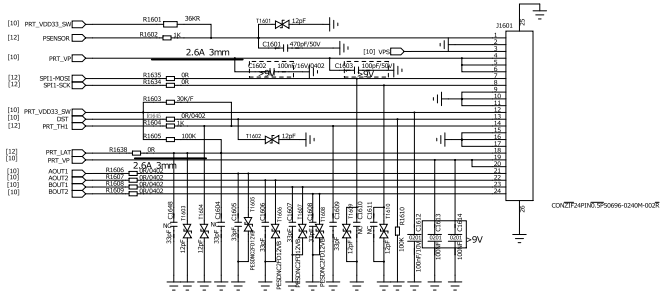
Power for Sensor



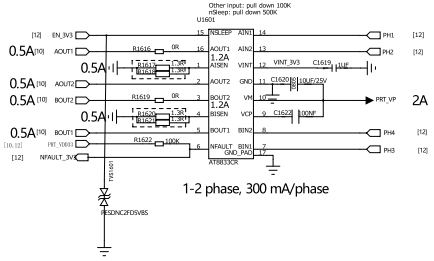
Printer VDD Supply Switch



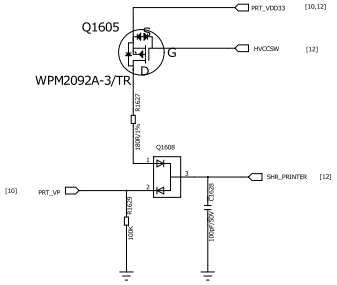
Printer connect



Printer MOTO Driver

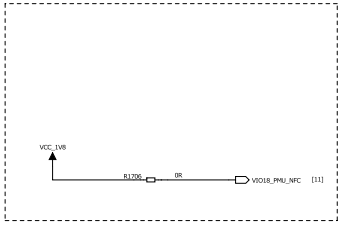


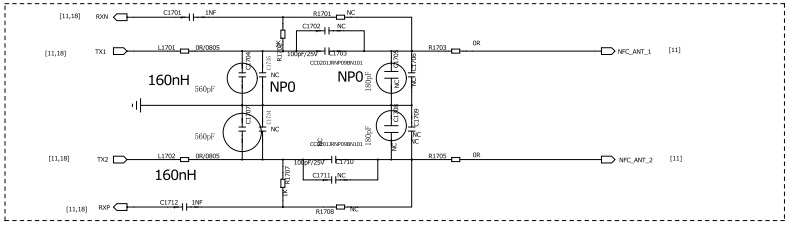
Printer Heating Dot Check

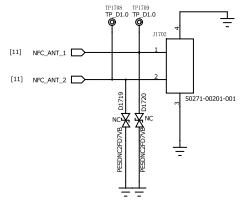


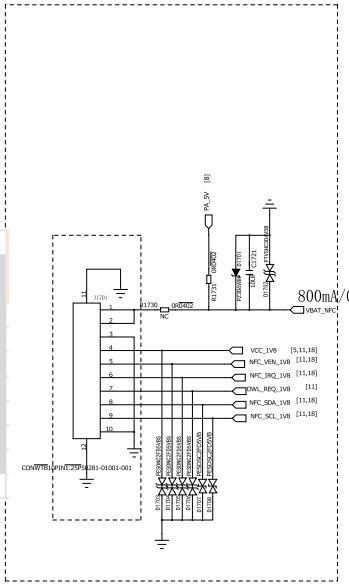
COMPANY: Sunmi			
TITLE: Luxembourg			
DRAWN: ZMQ	DATED: 23.02.27		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 10 18

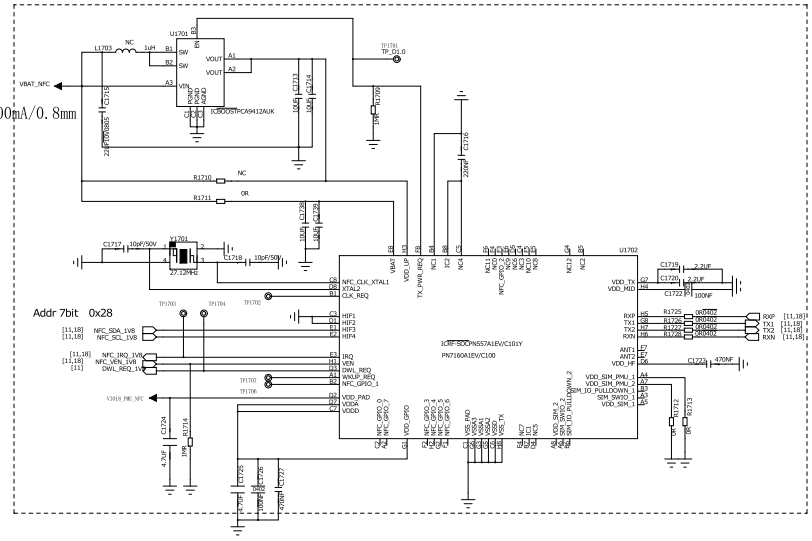
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:











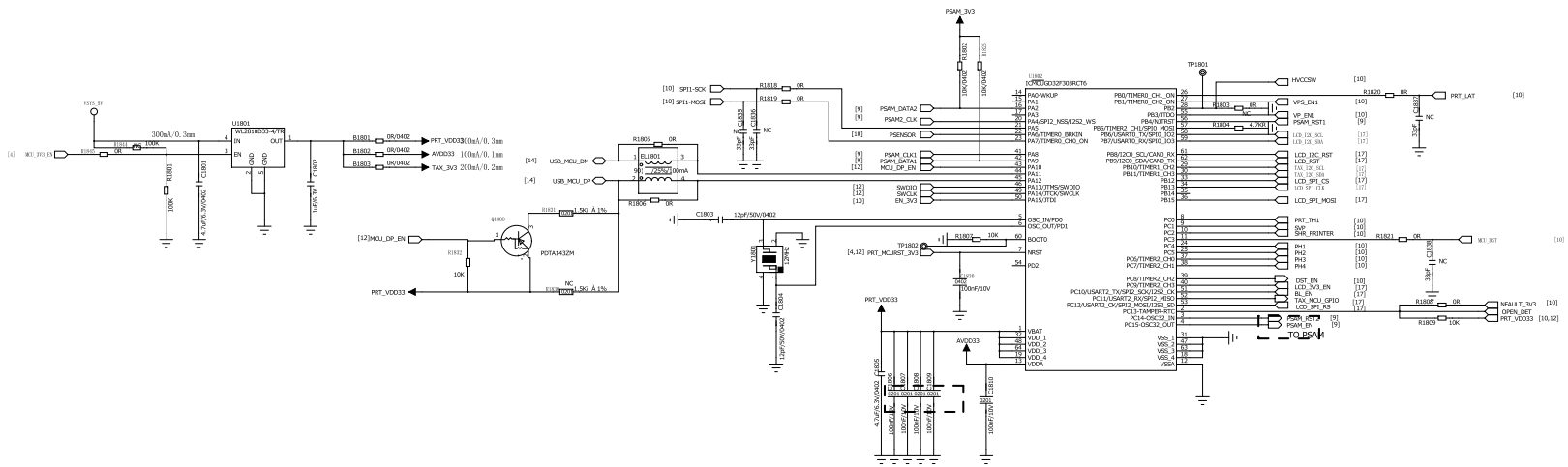
HIF2	HIF1	IIC_WRITE	IIC_READ
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

序号	定义	
1	VBAT(3.6V-4.2V)	开关、延时电路，1A
2	VBAT(3.6V-4.2V)	开关、延时电路，1A
3	GND	
4	1.8V_VCCIO	1.8V
5	NFC_EN	1.8V
6	NFC_IRQ	1.8V
7	DWL_REQ	1.8V
8	IIC_SDA	1.8V
9	IIC_SCL	1.8V
10	GND	

DRAWN: ZMQ	DATED: 23.02.27	COMPANY: Sunmi	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: Luxembourg	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
		SCALE: <Scale>	SHEET: 1 of 18

POWER

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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RELEASED: <Released By>	DATED: <Release Date>

COMPANY:	Sunmi
TITLE:	Luxembourg
CODE: <Code>	SIZE: A0
DRAWING NO:	01.BLOCK DIAGRAM
REV:	V2.0.C
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REVISION RECORD			
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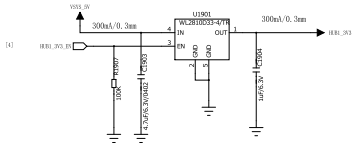
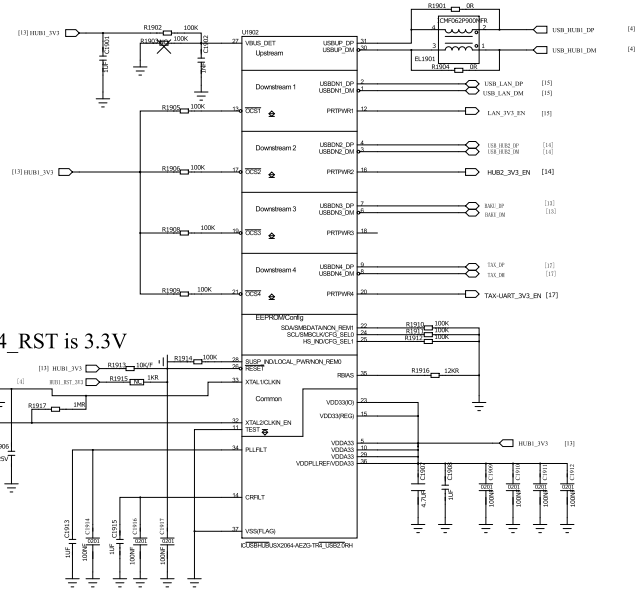
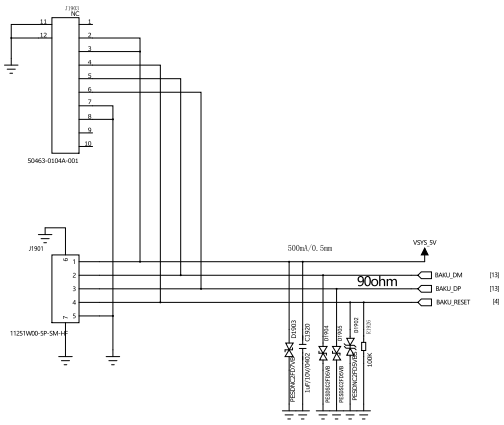
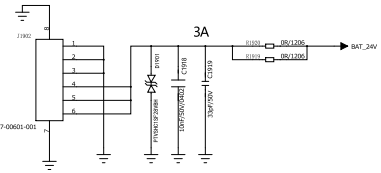




BAKU connect





COMPANY: Sunmi			
TITLE: Luxembourg			
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QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
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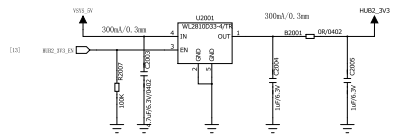
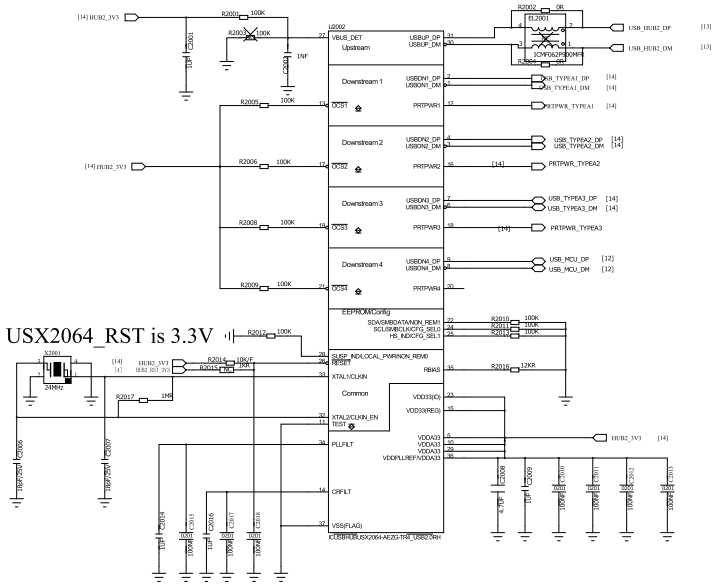
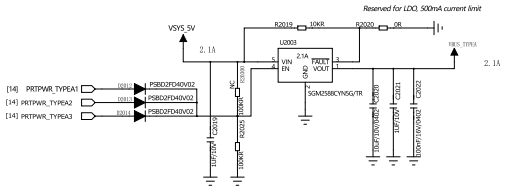
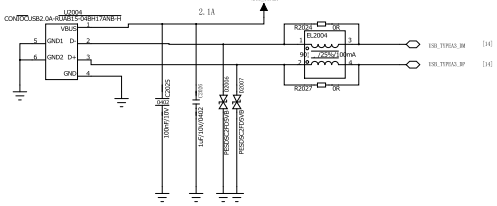
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

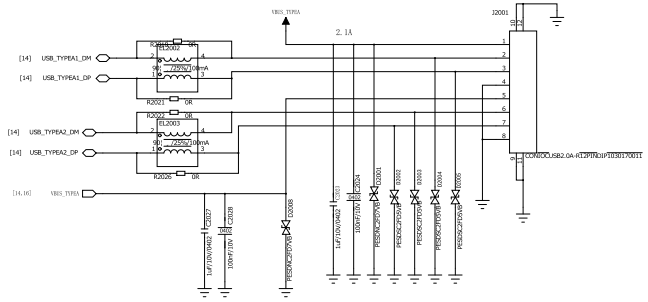




Double-deck TYPE-A



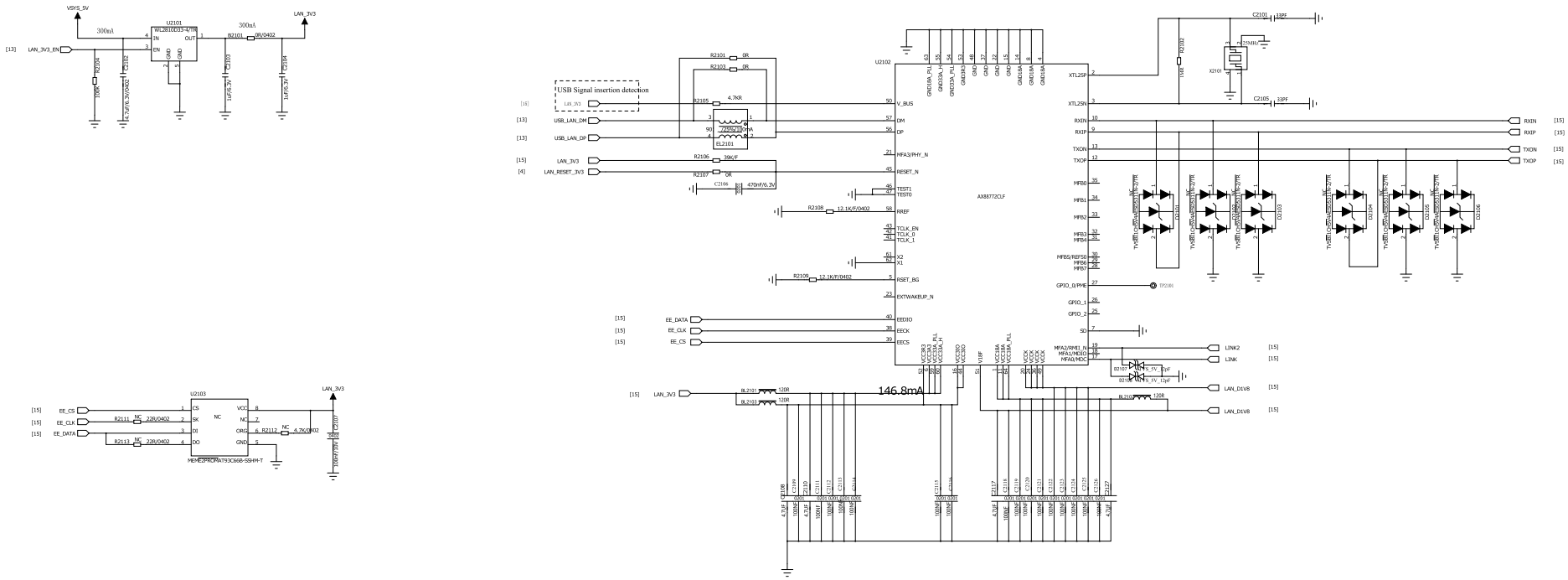




Reference FTP:USB2.0 interface and MOS switch circuit_V1.1
Reference FTP:100M LAN_LAN9513_V1.1
Reserve a GPIO to control reset signal
Add Common-mode TVS

DRAWN: ZMQ	DATED: 23.02.27	COMPANY: Sunmi	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: Luxembourg	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: 01.BLOCK DIAGRAM	REV: V2.0.C
		SCALE: <Scale>	SHEET: 14 of 18

USB-LAN



RJ45

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY:	Sunmi		
TITLE:	Luxembourg		
DRAWN: ZMQ	DATED: 23.02.27		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0
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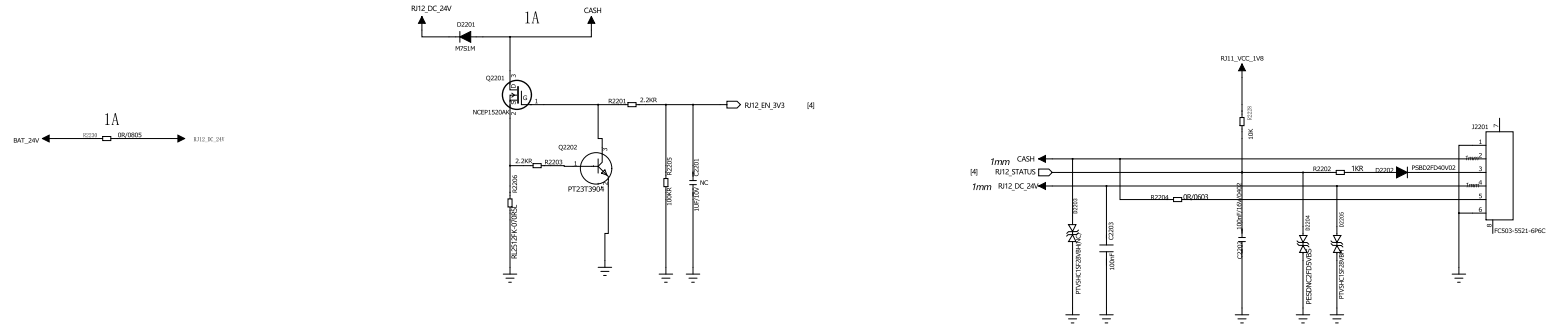
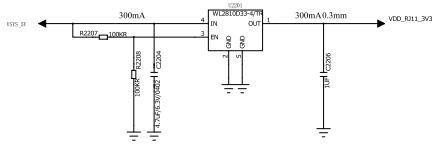
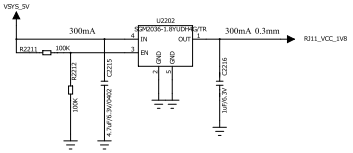
RJ12

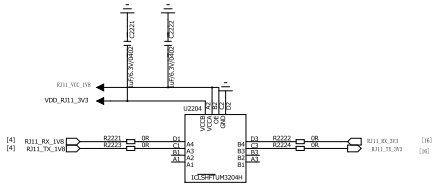


Reference FTP:RJ12_STD_SCH_V1.0_20211231

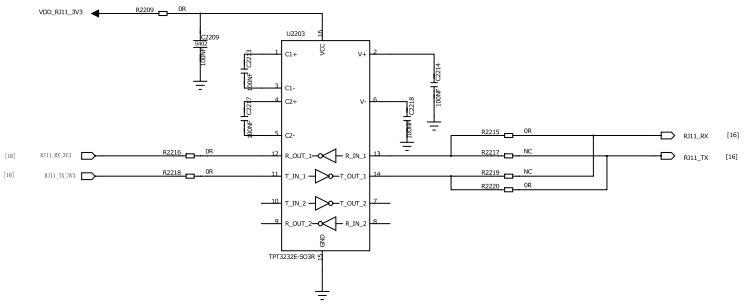
RS232

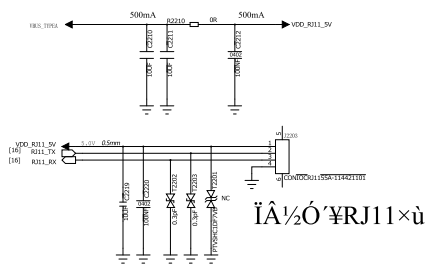






RJ11

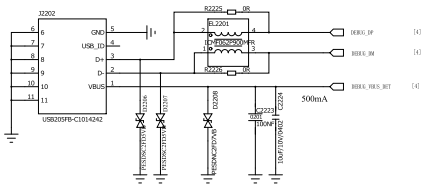




ÏÂ½Ó´¥RJ11×ù

TP_RJ11-UART_AudioJACK

MicroUSB for Debug



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TITLE:	Luxembourg
DRAWN: ZMQ	DATED: 23.02.27
CHECKED: <Checked By>	DATED: <Checked Date>
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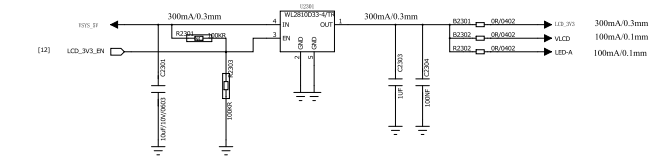
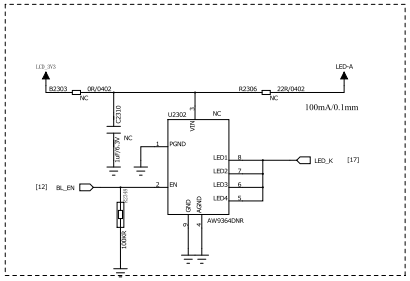
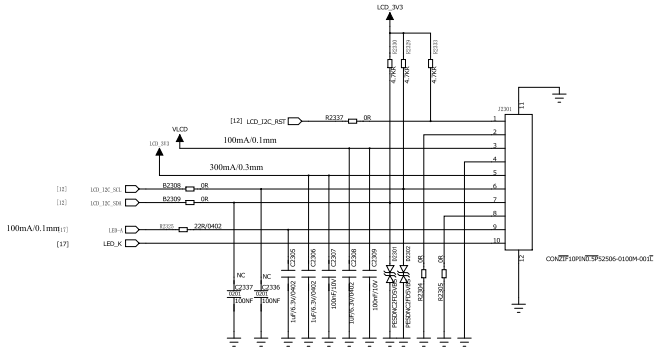
SCALE: <Scale>	SHEET: 16 / 18

SUB LCD

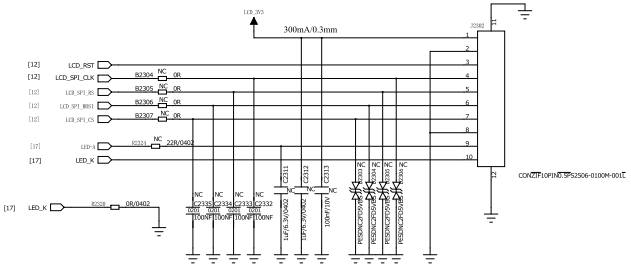




LCD-I2C

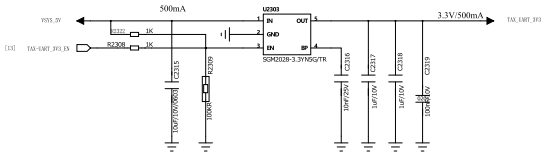


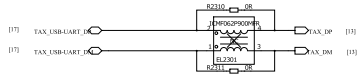
LCD-SPI

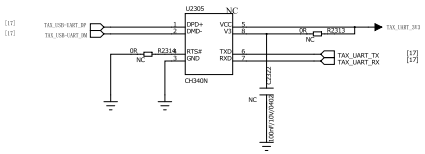


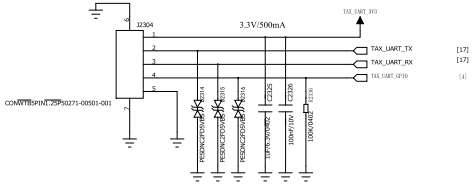
TAX-UART

NC









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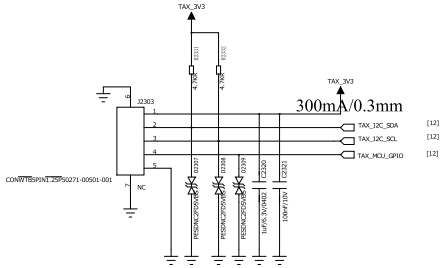

REVISION RECORD			
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COMPANY: Sunmi			
TITLE: Luxembourg			
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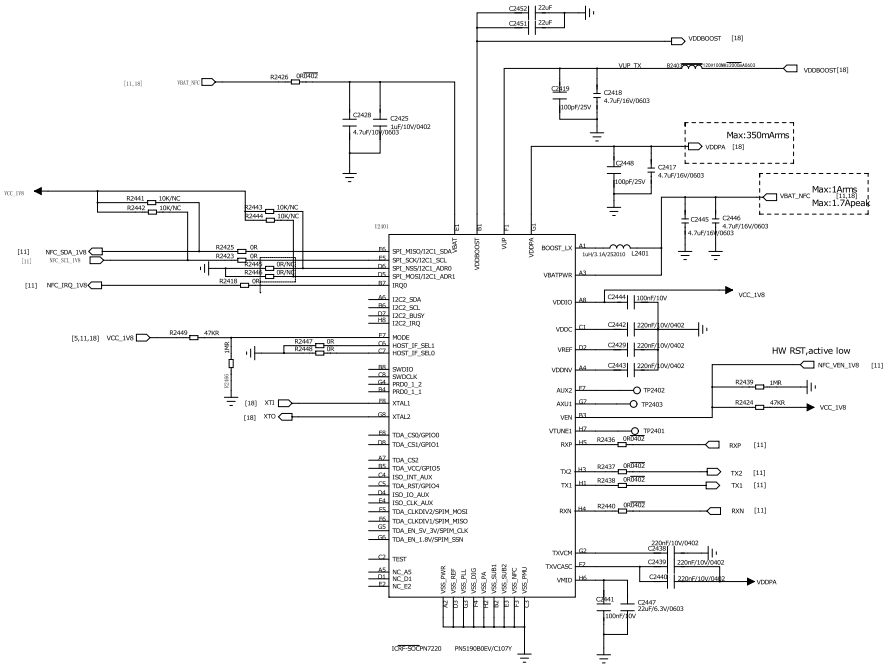
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 17 / 18

REVISION RECORD			
LTR.	ECO NO:	APPROVED:	DATE:



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