

A block diagram of the Wireless-485 design is included in Figure 1. This block diagram is appropriate for both sides of the link. The block diagram indicates the major ICs being used in the design as well as the oscillators being used. For generating RF frequencies, the CC430F5147 contains an internal VCO and PLL that phase locks the generated RF carrier to the 26MHz input reference frequency. This block diagram captures the Wireless-485 design as it is currently being built in production and does not include any population options that are not being utilized.

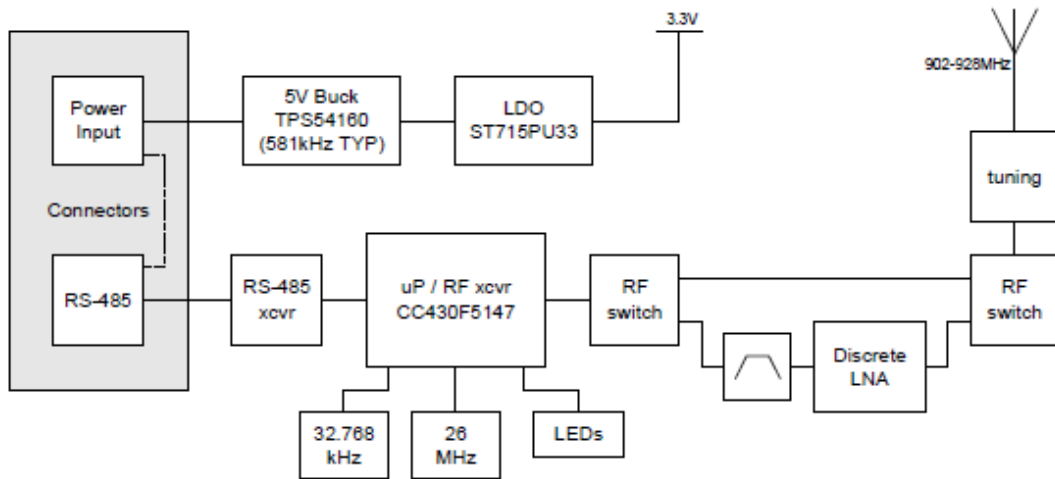


Figure 1 Electronics Block Diagram