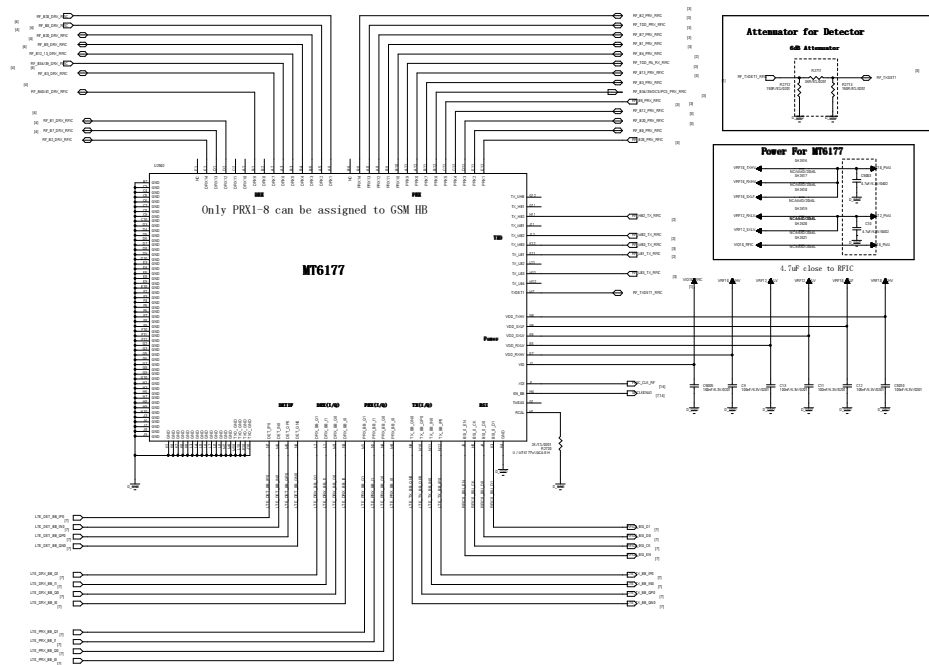
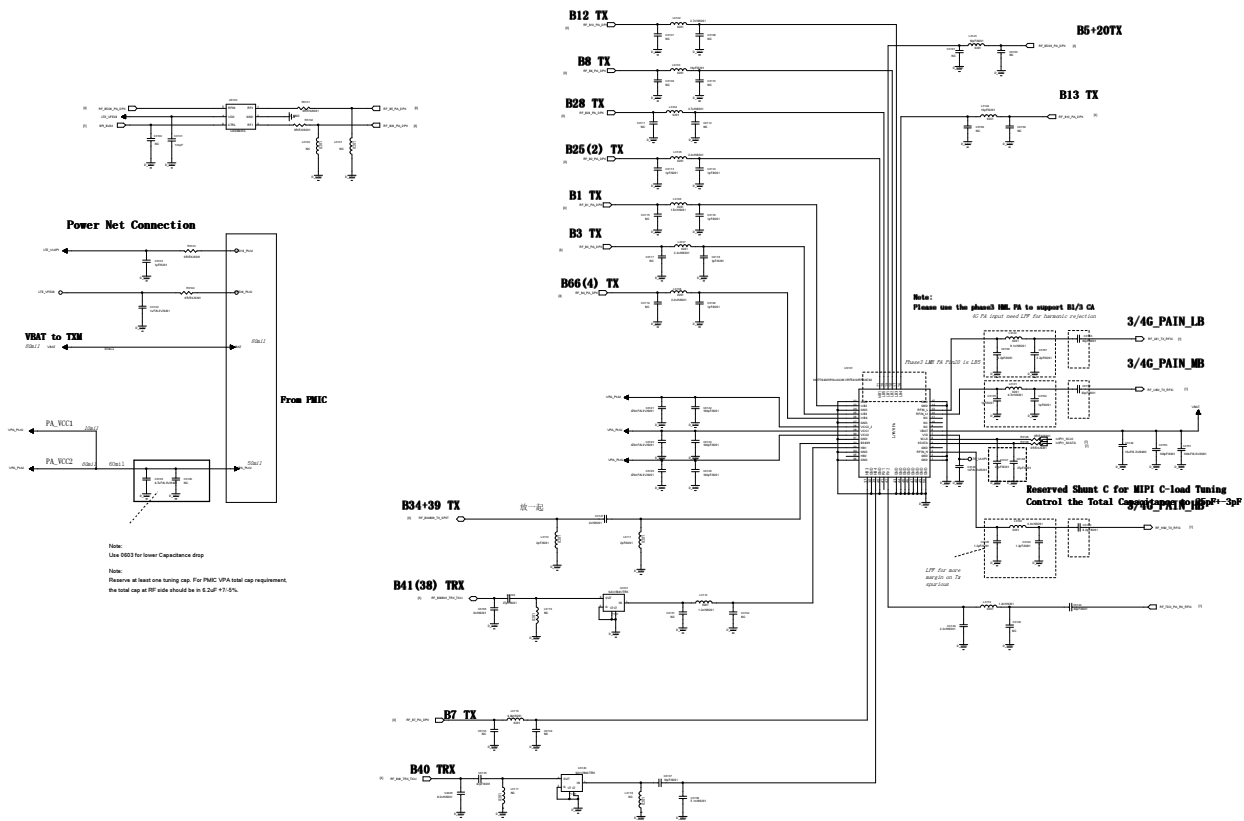
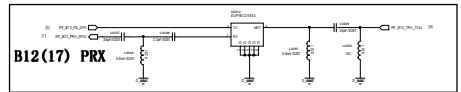
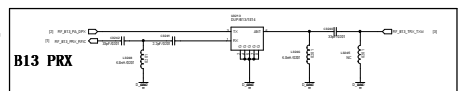
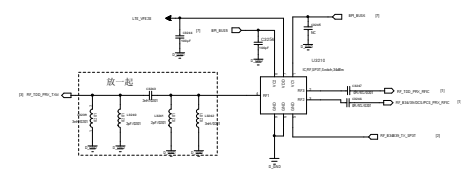
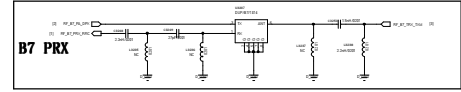
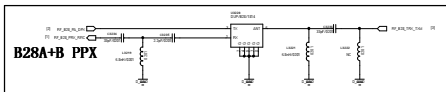
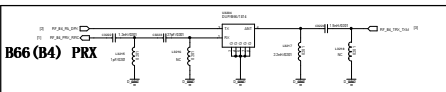
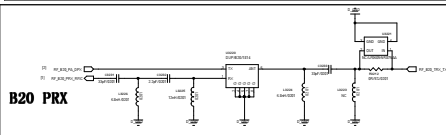
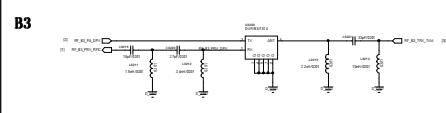
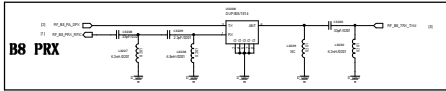
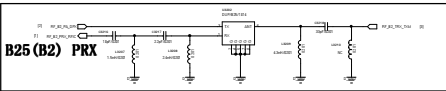
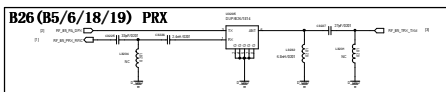
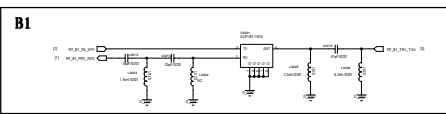
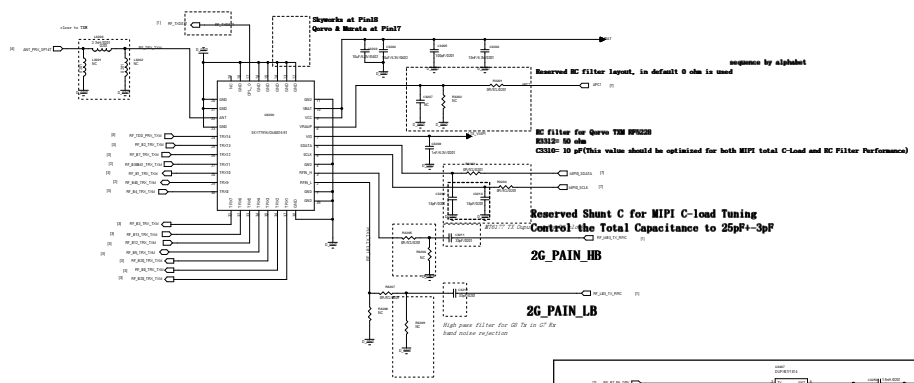
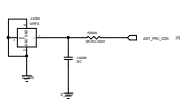
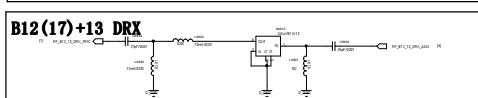
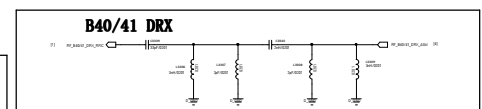
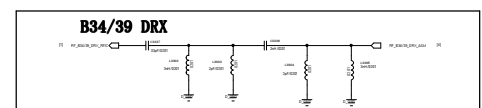
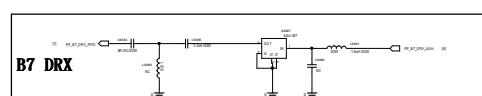
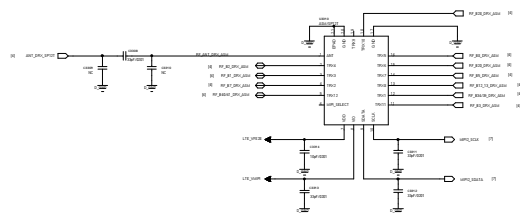


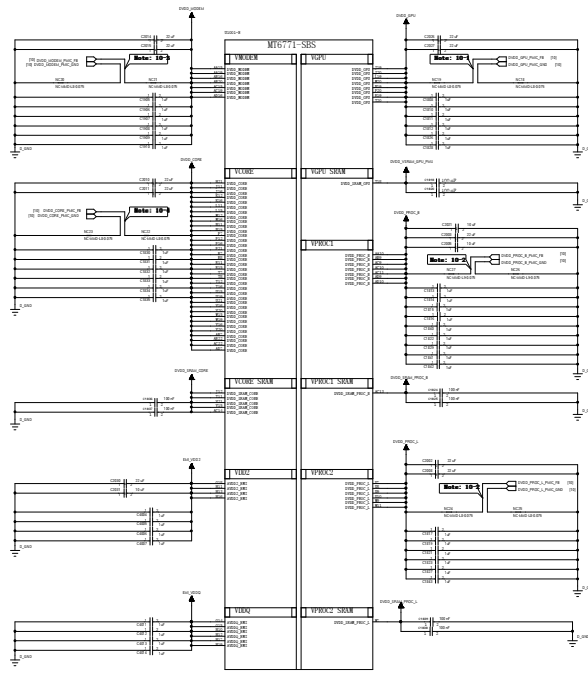




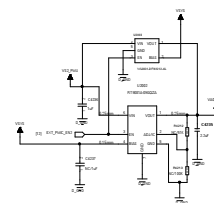
HMLB_Primary-ANT



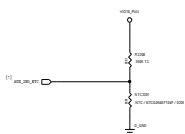




Schematic design notice of "10_M_POWER_POW" page.	
Note 10-1:	Differential pair of DVDD_GPU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-2:	Differential pair of DVDD_PROC remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-3:	Differential pair of DVDD_MODEM remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-4:	Differential pair of DVDD_CORE remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)

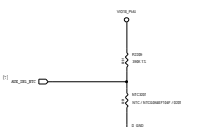


Note 11-4: Connects "AVDD09_UFS" to GND when UFS is not used.



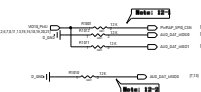
Thermistor to sense AP temperature

1. **RESISTANCE** keep a distance about 4" to 6" away from AP and for them other heat sources 10 cm at least.
2. **The distance** to the shortest distance from package edge to edge.



Thermistor to sense RF PA temperature

1. **RESISTANCE** must closer to 100 Ohm 7 Ohm or the highest 10 Ohm.
2. **The distance** to the shortest distance from package edge to edge.



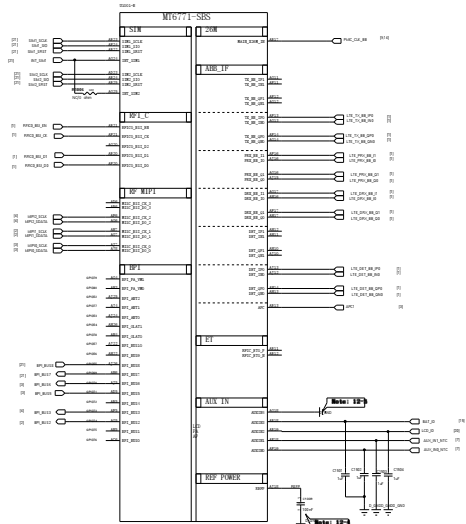
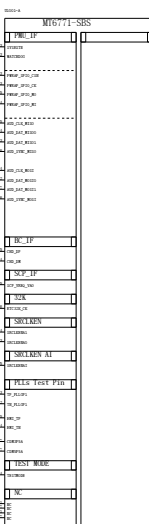
Schematic design notice of "12 BB 1" page.

Note 12-1: "PWRAP, SPB, CSN" and "AUD_DAT_MISO" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP, SPB, CSN	AUD_DAT_MISO	AP_JTAG	ID_JTAG
HI	LO	N/A	N/A
LO	LO	SPL_CS/SPL_CLK/ SPL_MOSI/MIENTS	N/A
LO	LO	SPL_CS/SPL_CLK/ SPL_MOSI/MIENTS	DPL11VCP1_HSINC/DPL1_VSINC/DPL1_DE/ DPL1_OVSD1/MSIS1/DE
LO	HI	MSIO1_CLK/MSIO1_DATA/DAT2	N/A

Note 12-2: "AUD_DAT_MISO" is bootstrap pin to enable serial JTAG output over USB 0 interface or not.
When "AUD_DAT_MISO" is pulled to high in system start up and then USB 0 interface will be switched into serial JTAG mode.
"AUD_DAT_MISO" is bootstrap pin to select system booting up from eMMC or UFS device.

AUD_DAT_MISO1	Boot device
LO	eMMC
HI	UFS

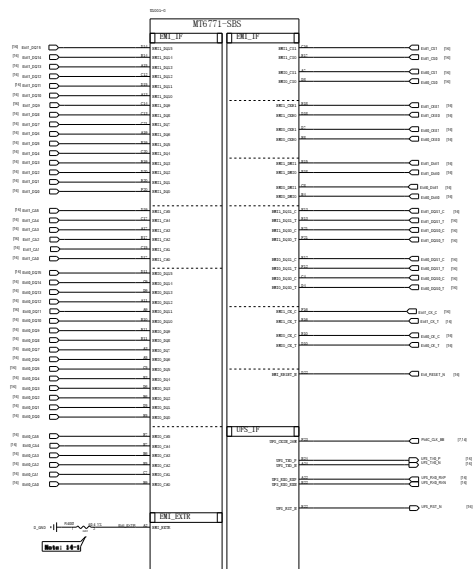


Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-4: The de-coupling cap. for REPP (A118 ball) have to be placed as close to BB as possible.

Note 12-5: AUD_SYNC, MISO and AUD_CLK, MISO are DDR type feature in bootstrap

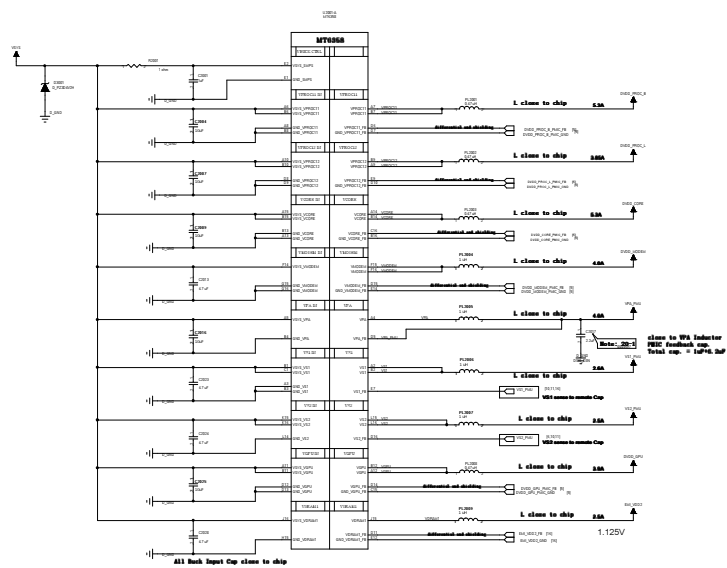
AUD_SYNC, MISO	AUD_CLK, MISO	DDR
LO	LO	UPDDR4EXH x 2 EN
HI	LO	UPDDR3
HI	HI	UPDDR4EXH x 1 EN



Schematic design notice of "14_BR_3" page.

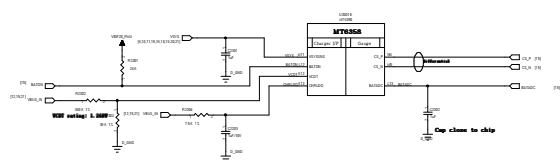
The resistor of DSR, EXTR for DRAM has to be placed near to SB as close as possible

Note 14-1: E46021, please select E3.4 ohm 1% resistor



Schematic design notice of "20_POWER_MT6358-Buck" page.

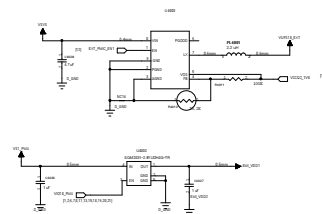
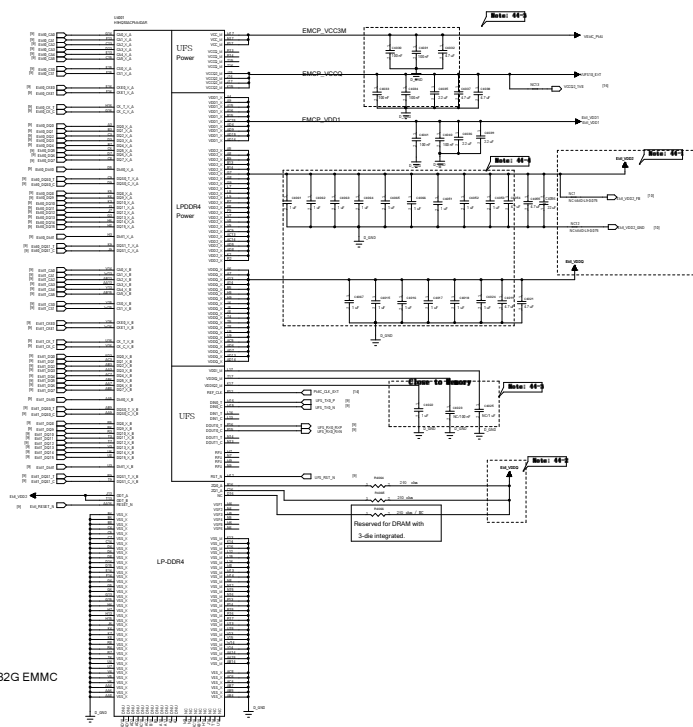
Note 20-1: Please select C2017 with 0402 size



Note 22-1: EXT_PMIC_EN1 : For UFS_1V8, and keep floating if it is not used
EXT_PMIC_EN2 : For VA09 of SSUSB/UFS, and keep floating if it is not used

HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VSD1.DQ01_batt)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.25V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	V\$1
1	0	1.25V	OFF	LP3	VDRAM1
1	1	1.25V	1.8V	LP4X (Ext x 1 EN)	V\$1

3G LPDDR4X+32G EMMC



Schematic design notice of "44 Memory, eMMC LPDDR4X"

Note 44-1: Please refer to power supply related page select VDDIM2 / VDDIM1 output voltage properly for LPDDR4X.

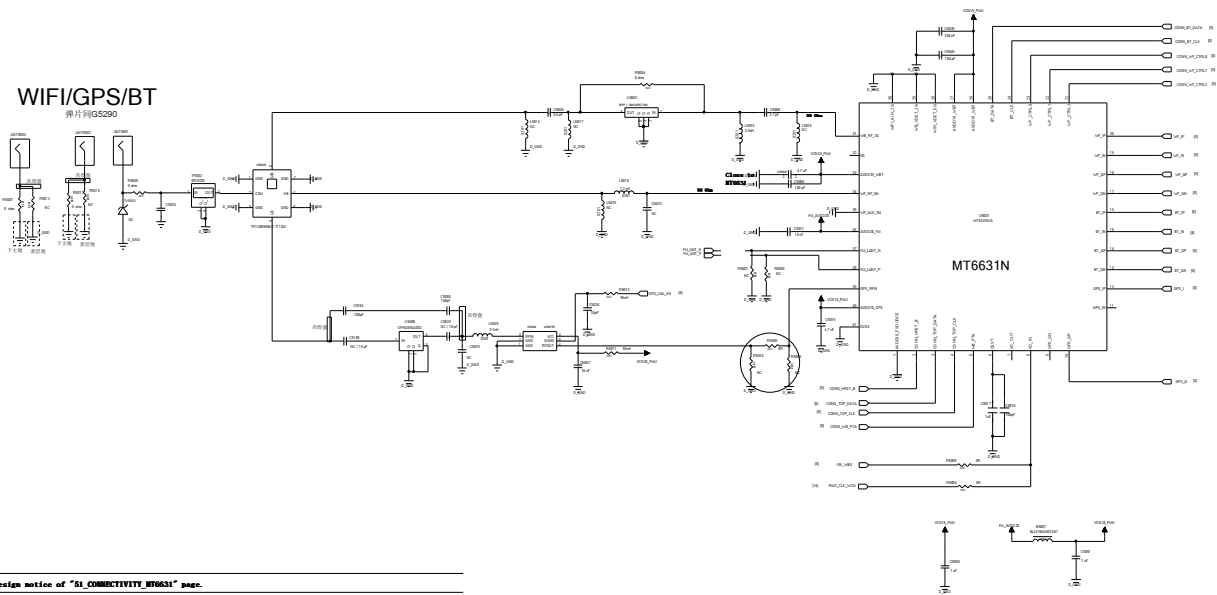
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.

Note 44-3: Please refer to eMCP vendor's datasheet or MIX common design notice to get the recommendation bypass cap. value for VCC/VDDQ/VDDI power domains of eMMC.

Note 44-4: VDDQ VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC (30uF, at PMIC page), please also refer to WMD and layout guide for placement.

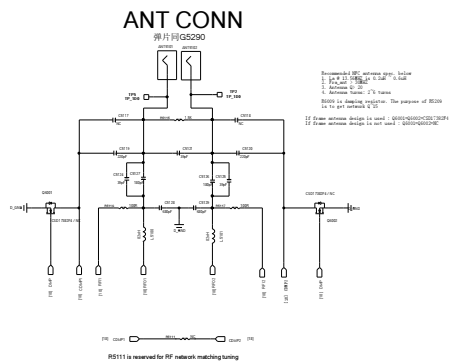
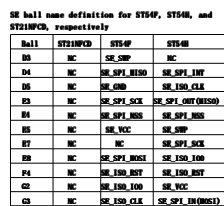
WIFI/GPS/BT

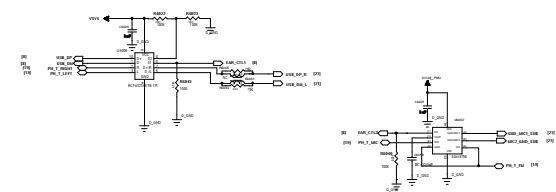
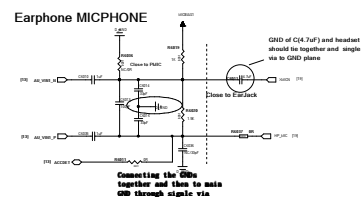
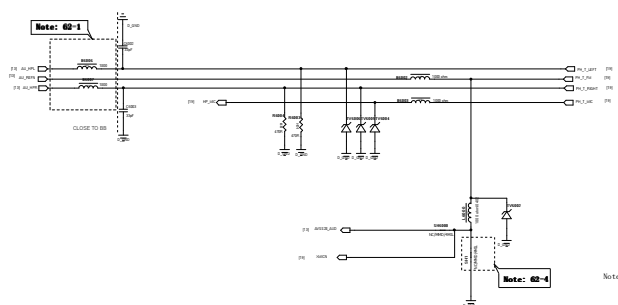
贴片料Q5290



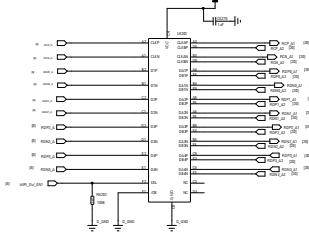
Schematic design notice of "SI_CONNECTIVITY_MT6631N" page.

Note SI-1: Note SI-1: Add 3dB resistor attenuator at external LNA output for more AGC saturation margin. Please let total RF loss < 6dB from external LNA output to GPS chip-input.

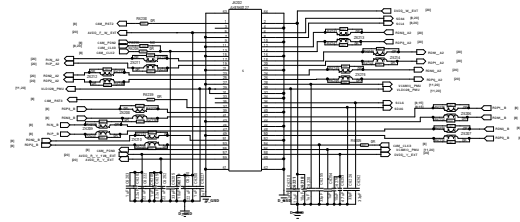




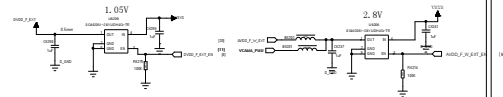
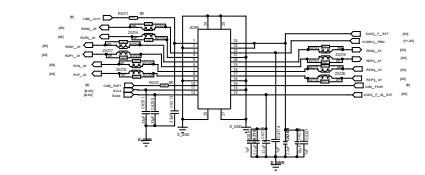
MIPI SWITCH



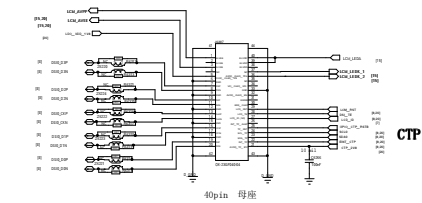
双摄像头封装定义



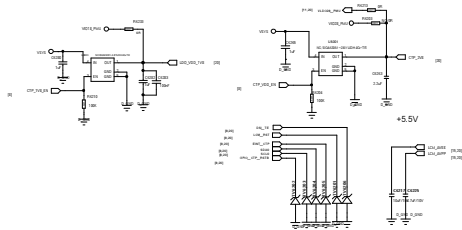
FOT CAM 前摄像头



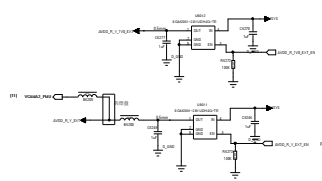
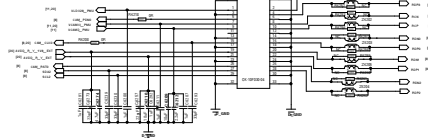
Main LCM



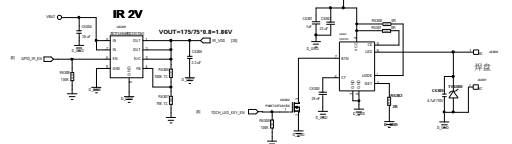
CTP



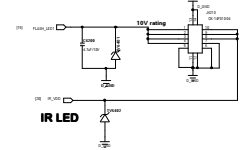
MAIN CAM

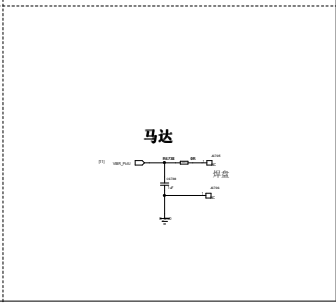
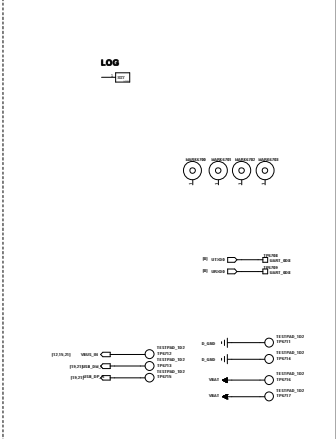
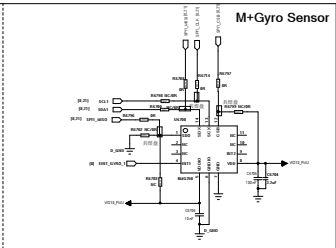
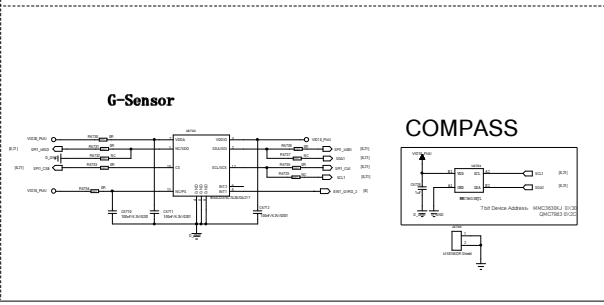
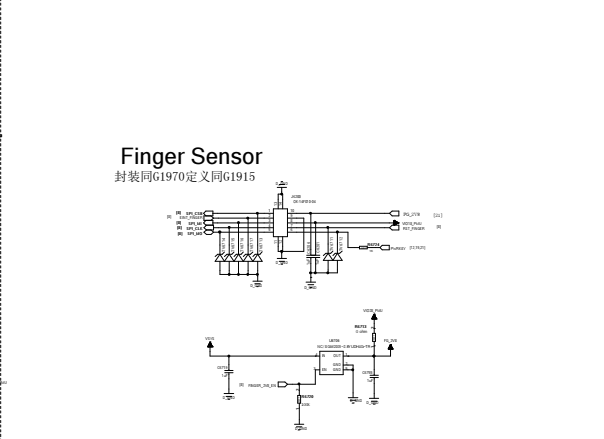
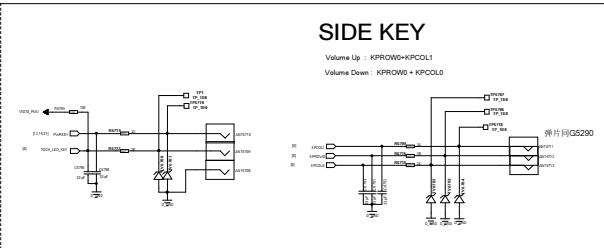
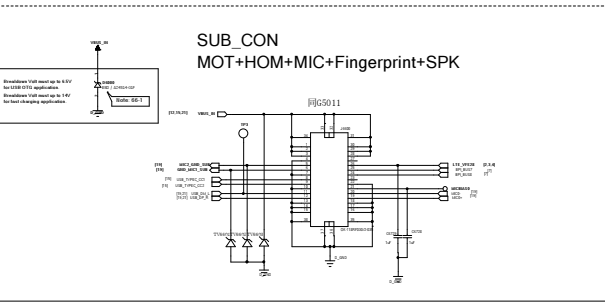
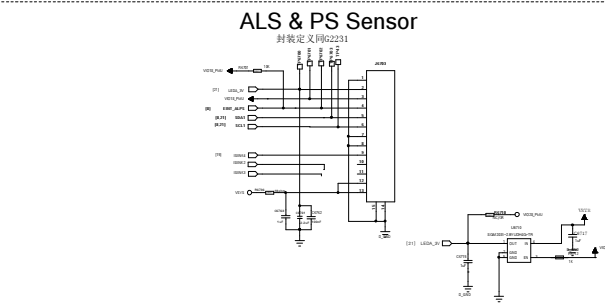
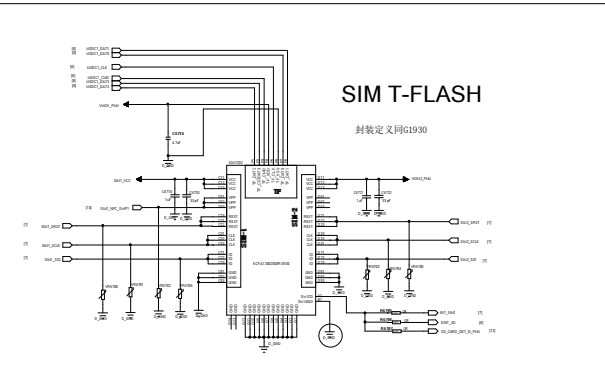


TOCH LED

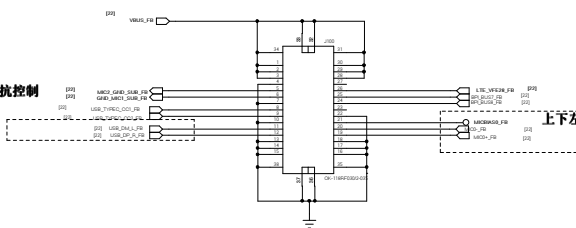


FLASH LED



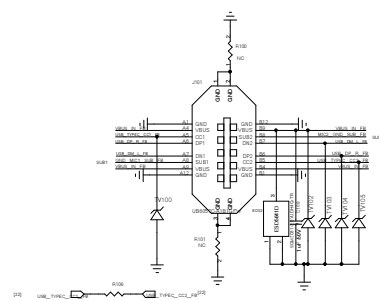


这两根要做阻抗控制

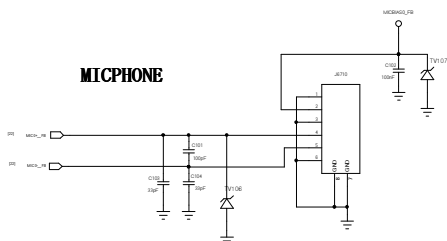


上下左右不包地，避开电源线

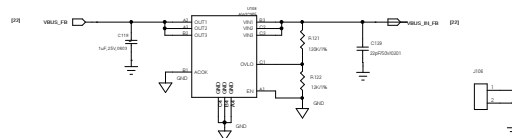
下主地 表层地



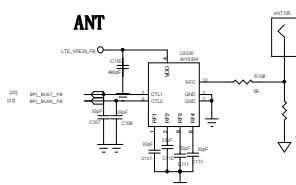
MICPHONE



OVP



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