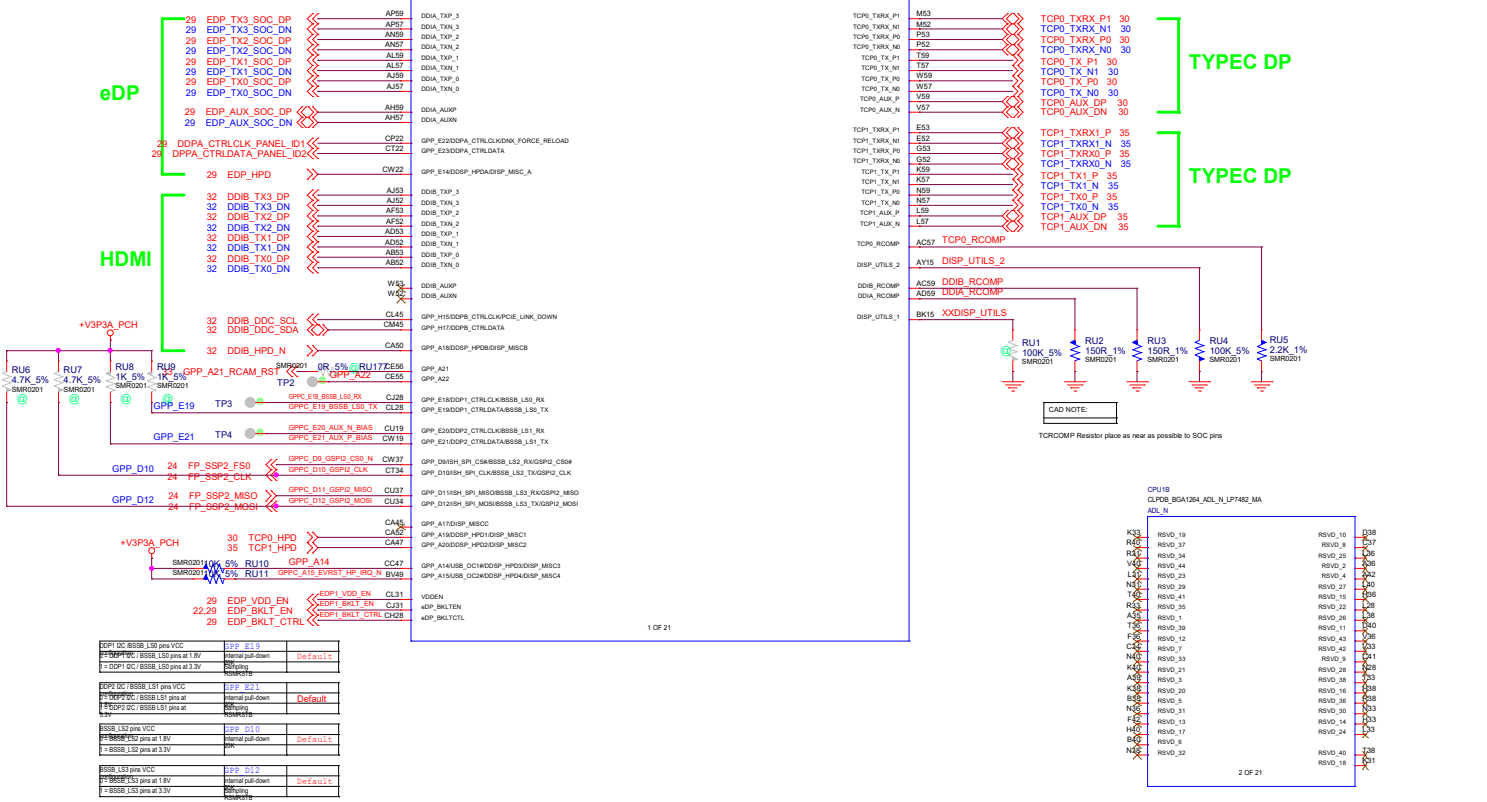
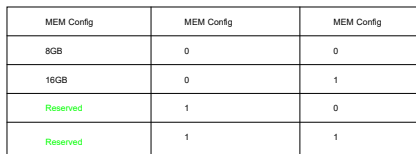


20220901 check ok

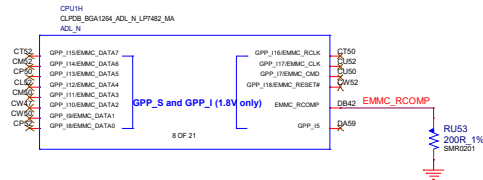
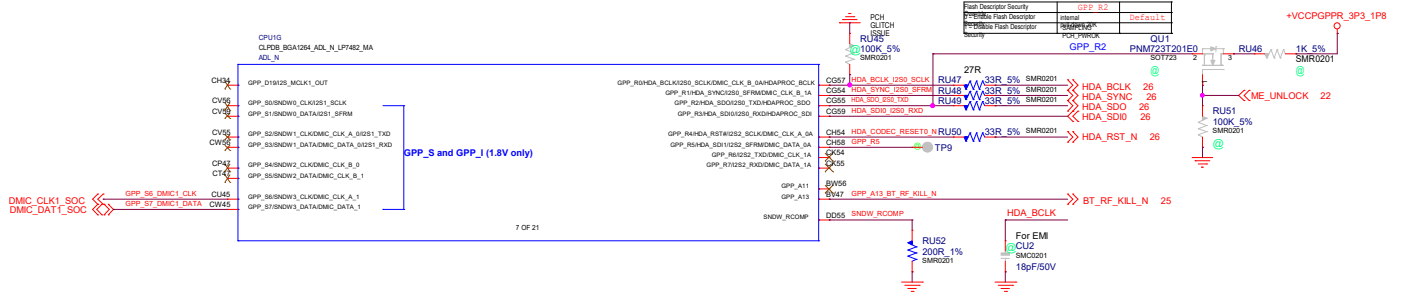
CPU1A
CLPB8_BGA1064_ADL_N_LF7482_MA
ADL_N



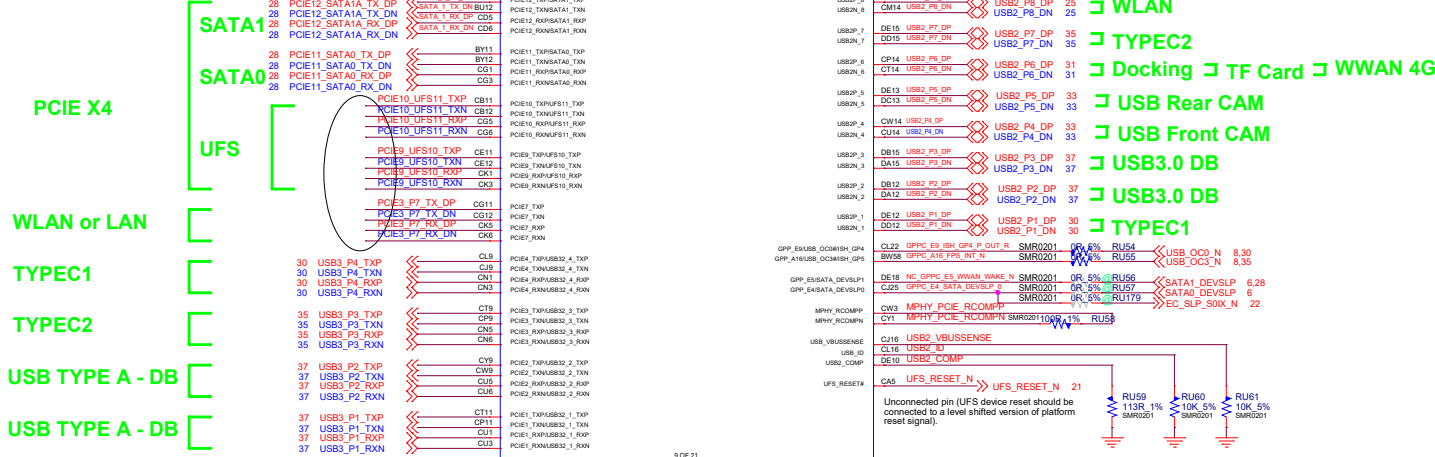
Title		
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TB130CADLN			
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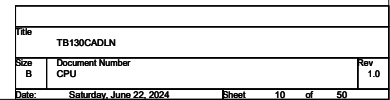


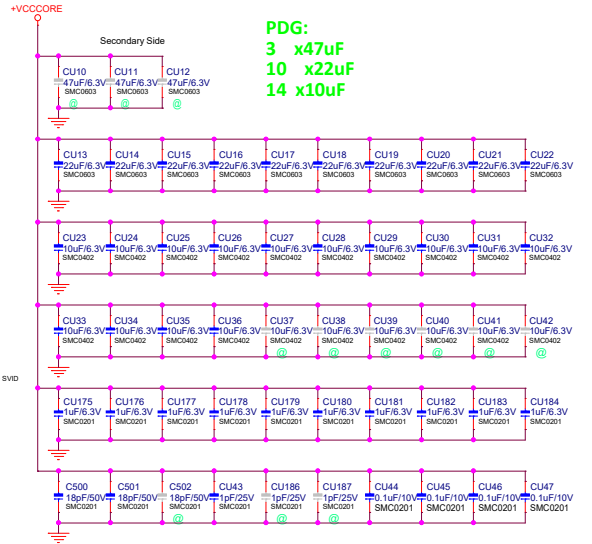
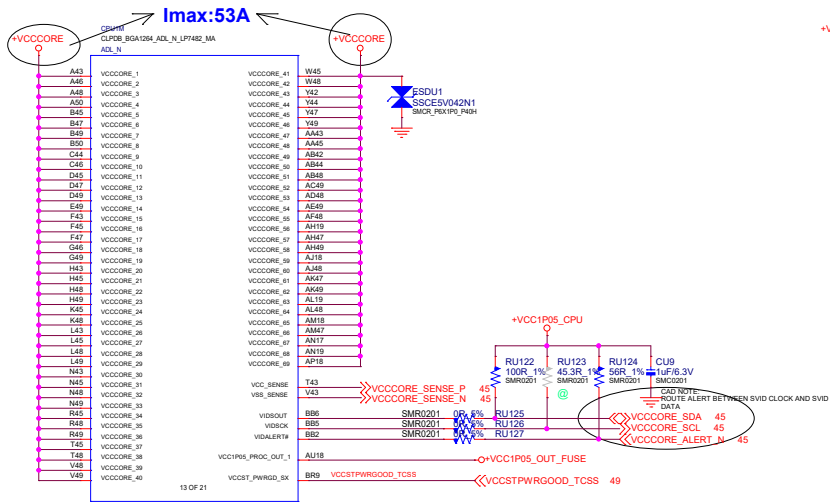
Title		
TB130CADLN		
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Date:	Saturday, June 22, 2024	Sheet 7 of 50



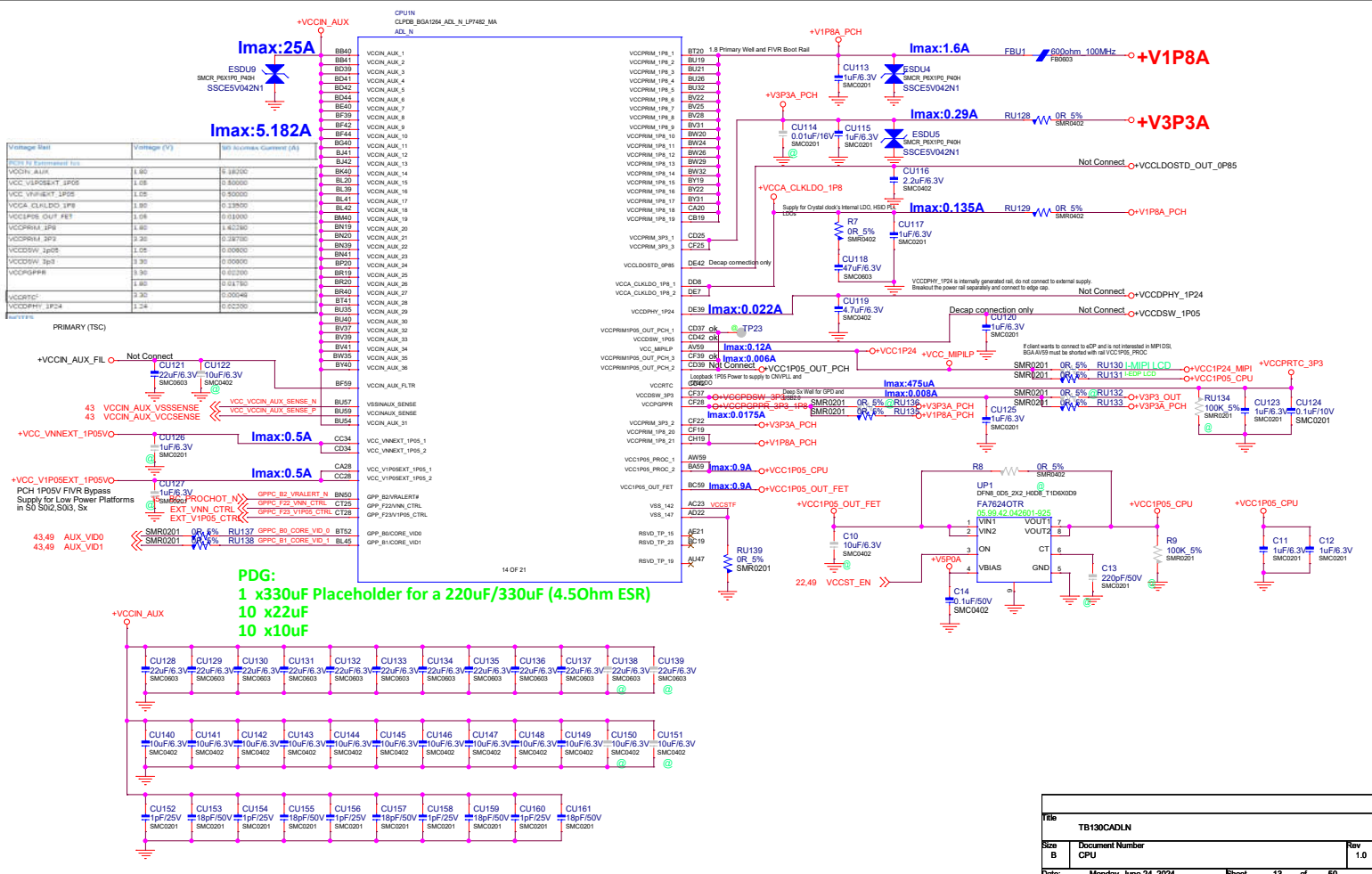
Title		
TB130CADLN		
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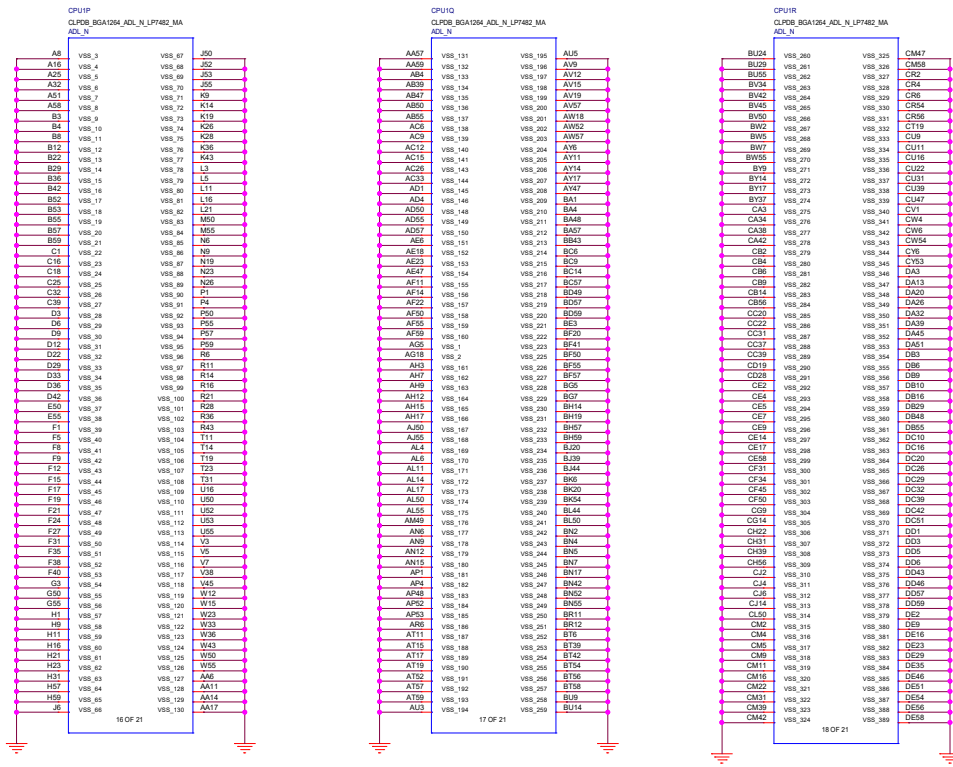


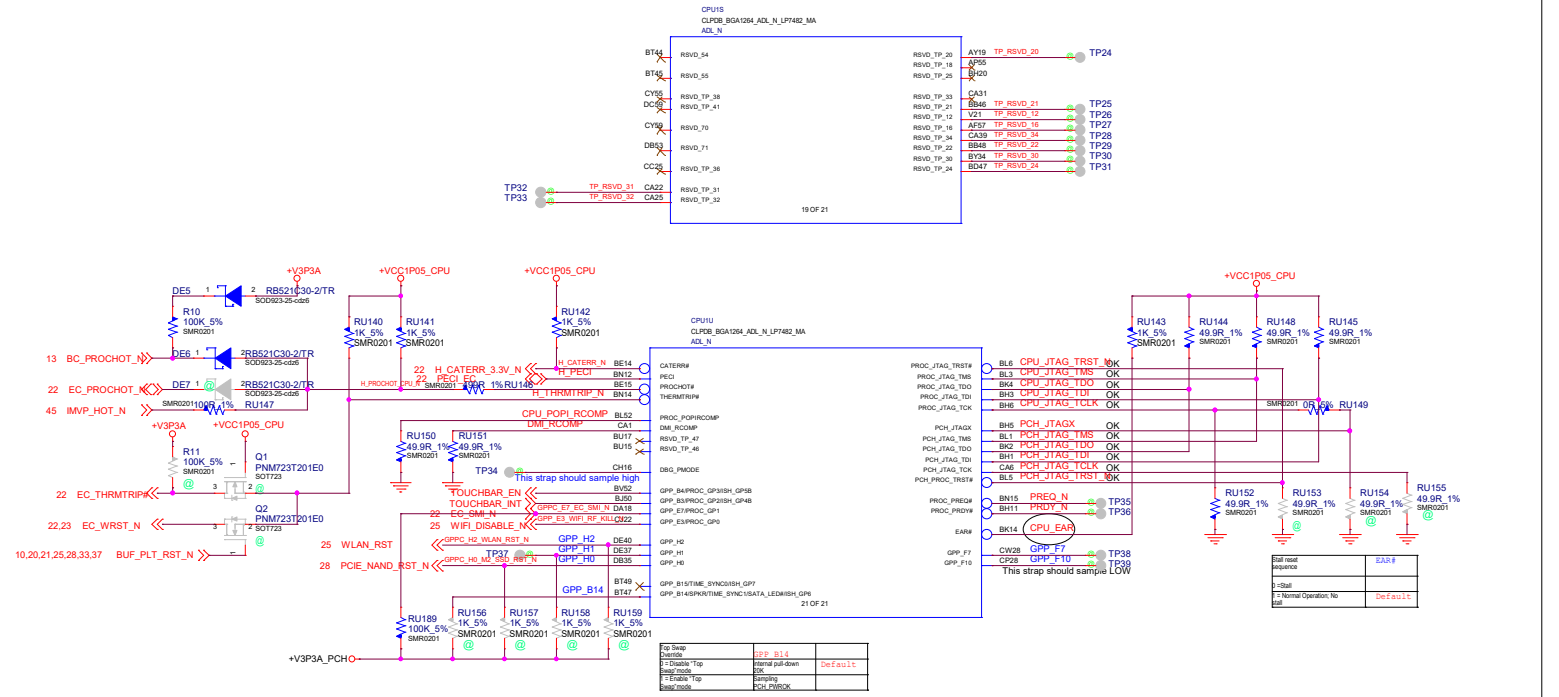


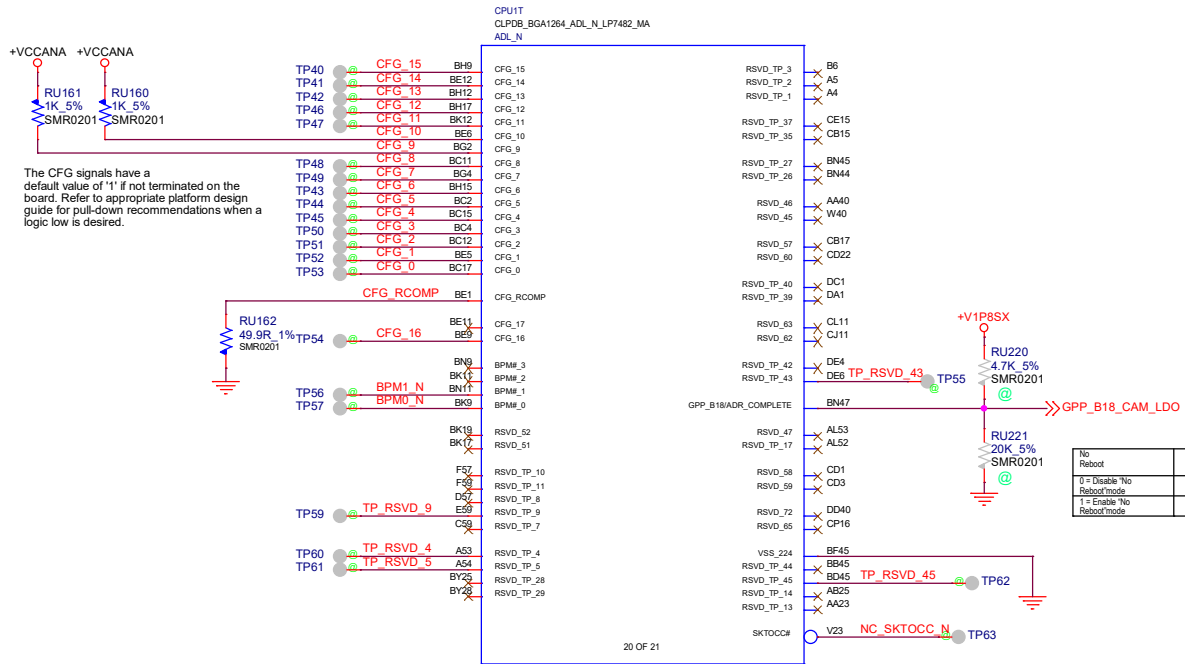


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No Reboot	GPP_B18	
0 = Disable No Reboot mode	internal pull-down 20K	Default
1 = Enable No Reboot mode	Sampling PCH_PWR0K	

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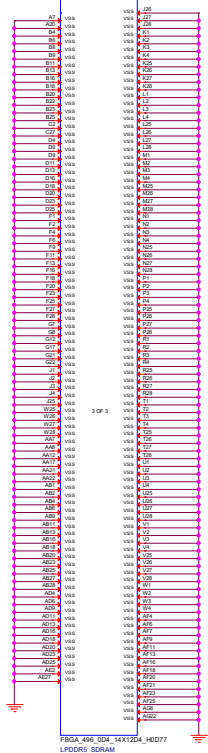
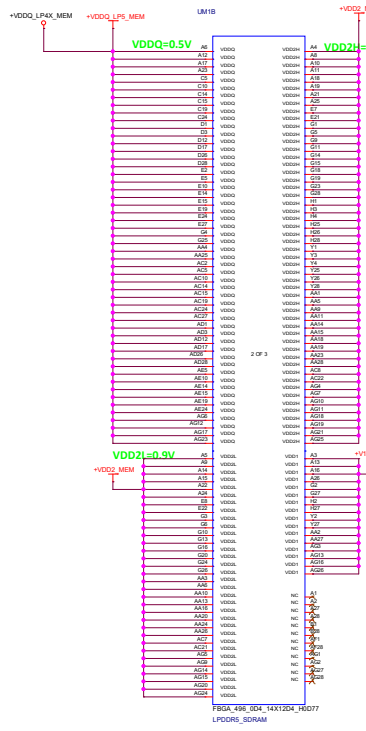
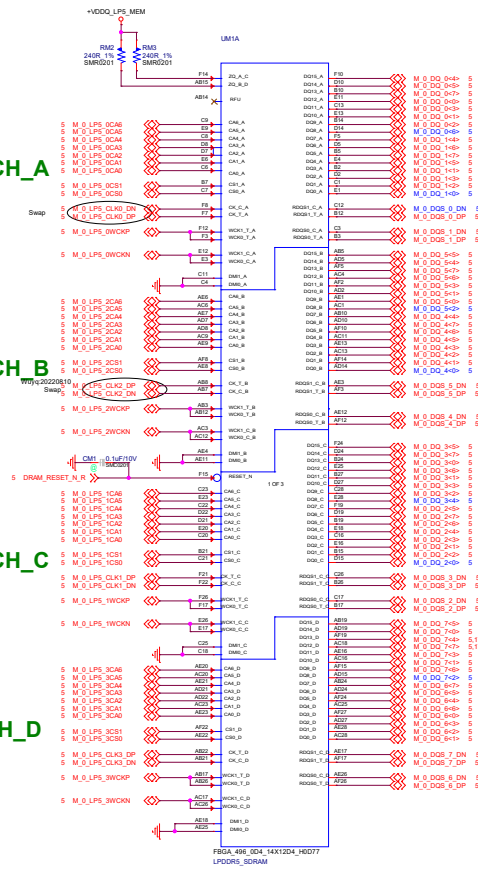
LPDDR5 MEMORY CHANNEL0

LP5_CH_A

LP5_CH_B

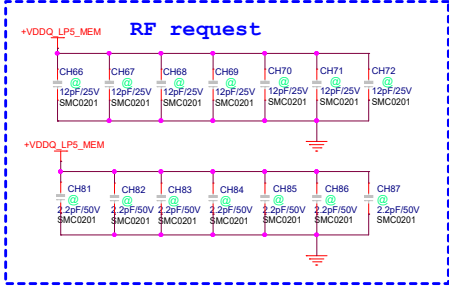
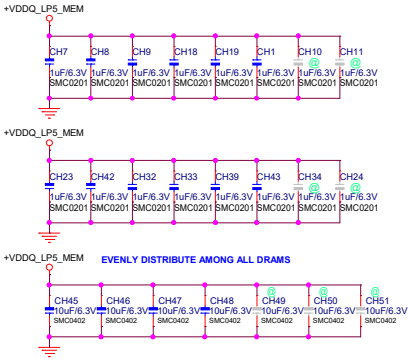
LP5_CH_C

LP5_CH_D



+VDDQ_LP5_MEM DECAPS

Note: 6 CAPS PER DRAM

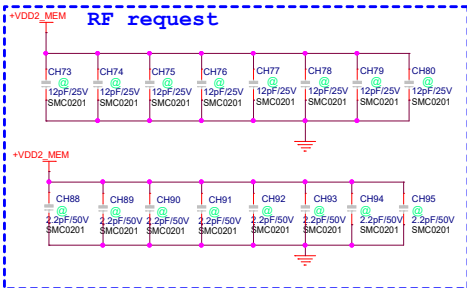
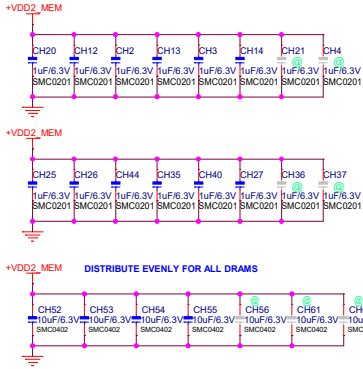


VDDQ EMC CAPS

0402 12PF: TOTAL 4
0402 2.2PF: TOTAL 4

+VDD2_MEM DECAPS

DISTRIBUTE EVENLY, 6 FOR EACH DRAM MODULE

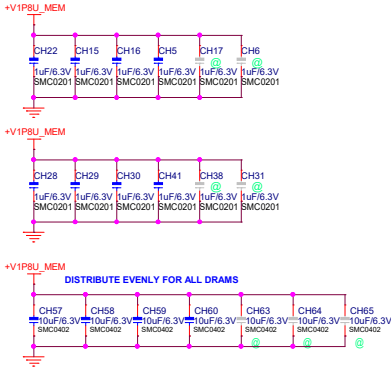


VDD2 EMC CAPS

0402 12PF: TOTAL 6
0402 2.2PF: TOTAL 6

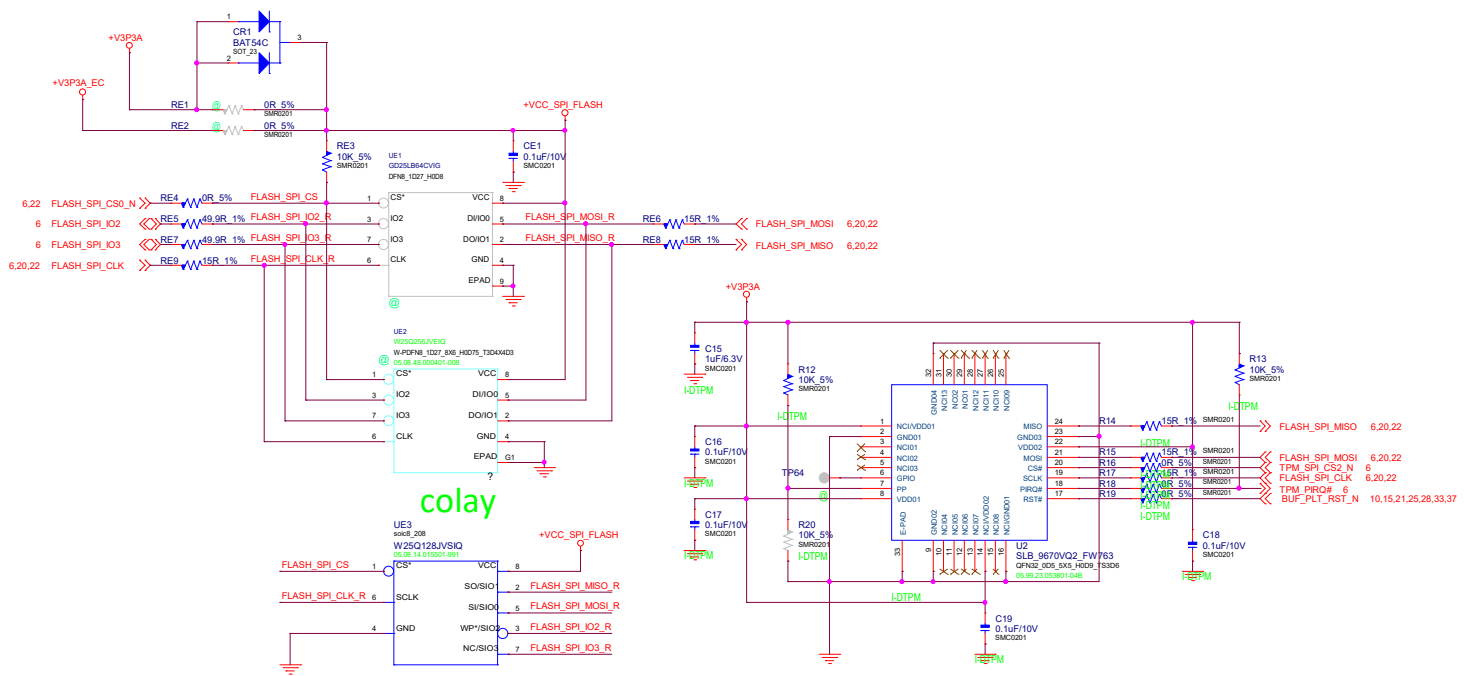
+V1.8U_MEM DECAPS

DISTRIBUTE EVENLY, 4 FOR EACH DRAM MODULE



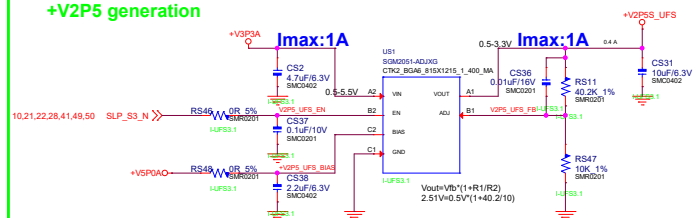
+VDD2_MEM	1UF	8
	10UF	4
+VDDQ_LP5_MEM	1UF	8
	10UF	4
+VPP_MEM	1UF	6
	10UF	4

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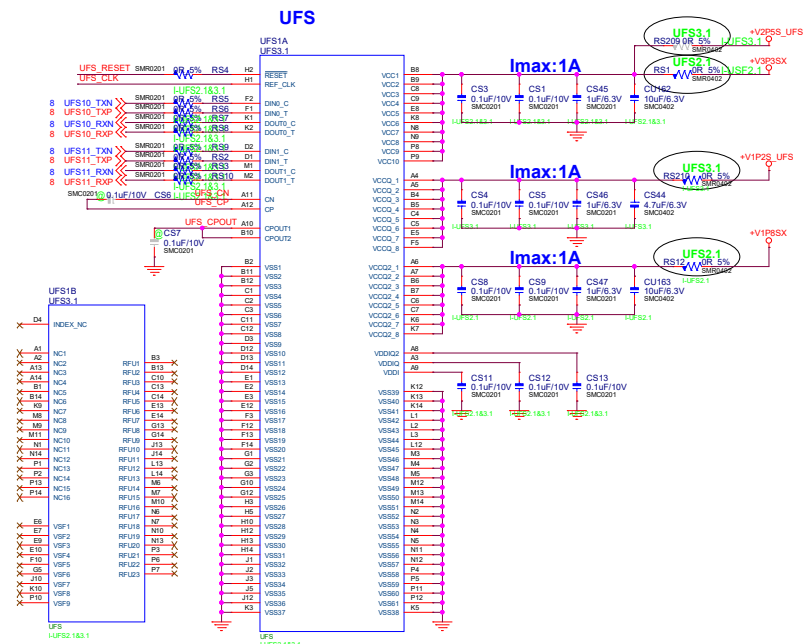
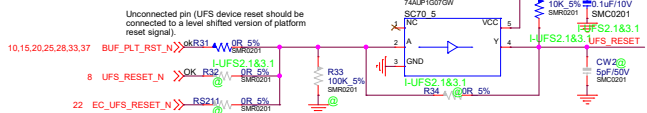
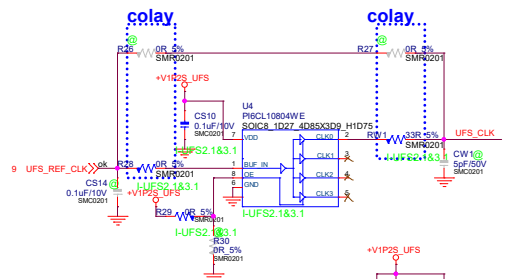
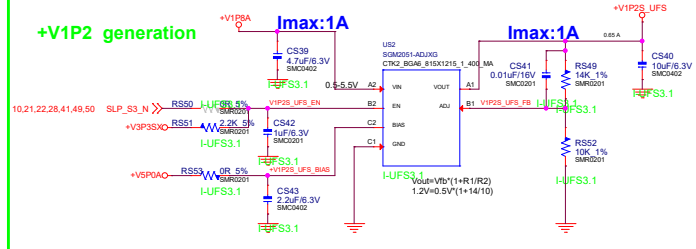


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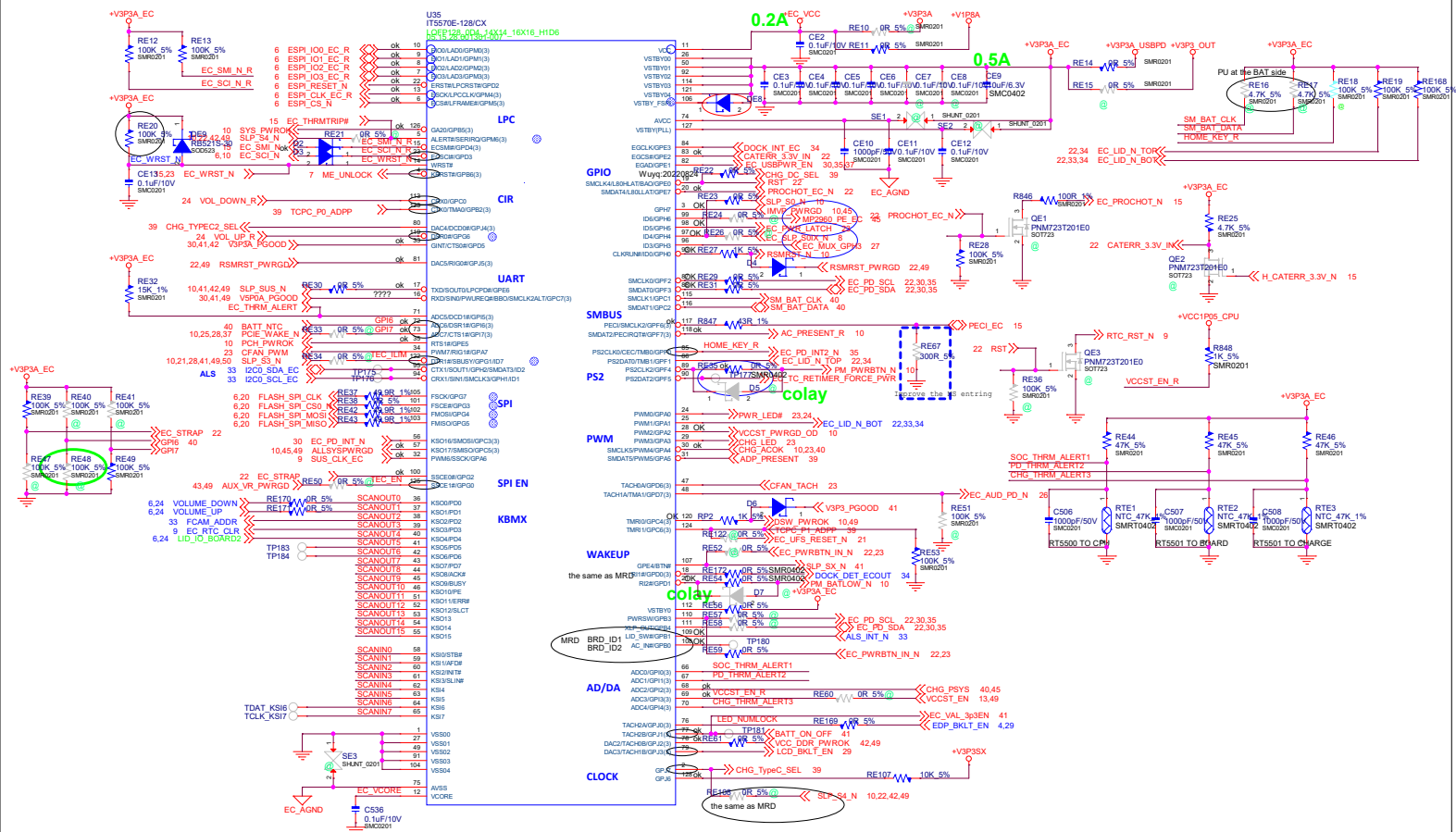
UFS3.1 +V2P5 generation



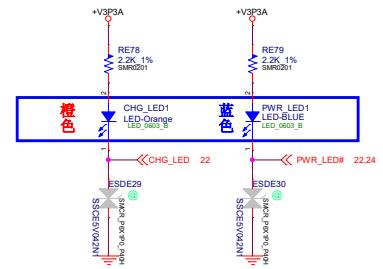
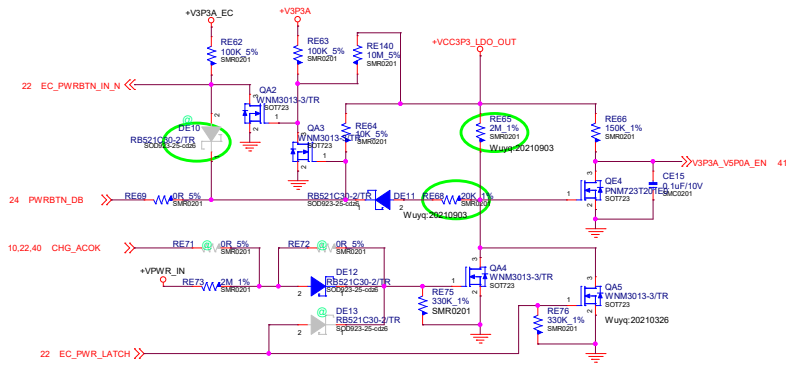
+V1P2 generation



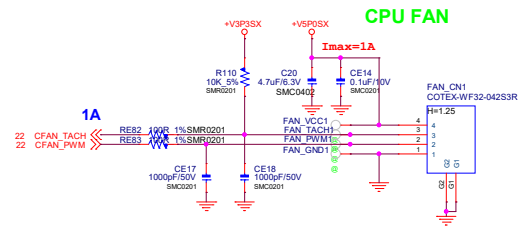
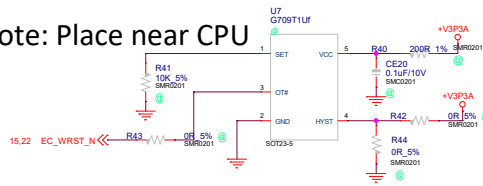
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A3	UFS	1.0
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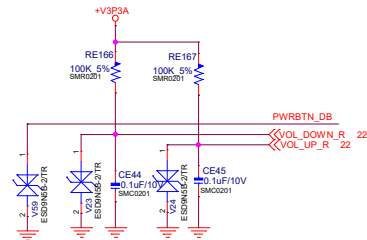
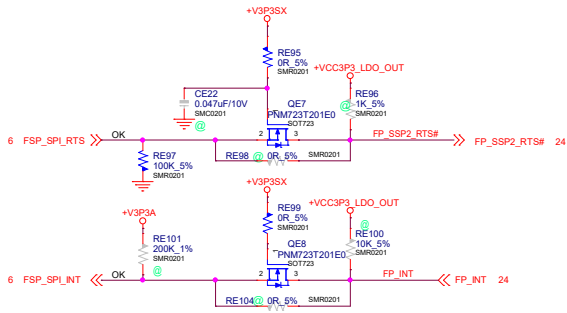
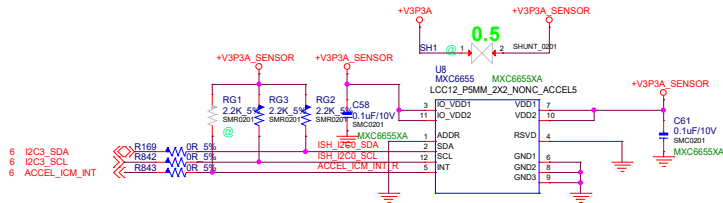
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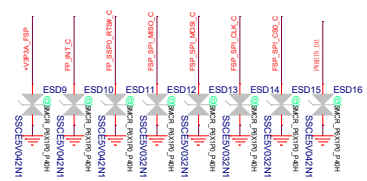
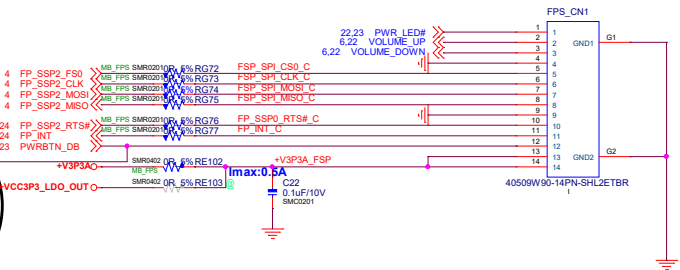
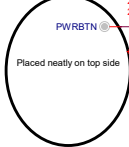
CAD Note: Place near CPU



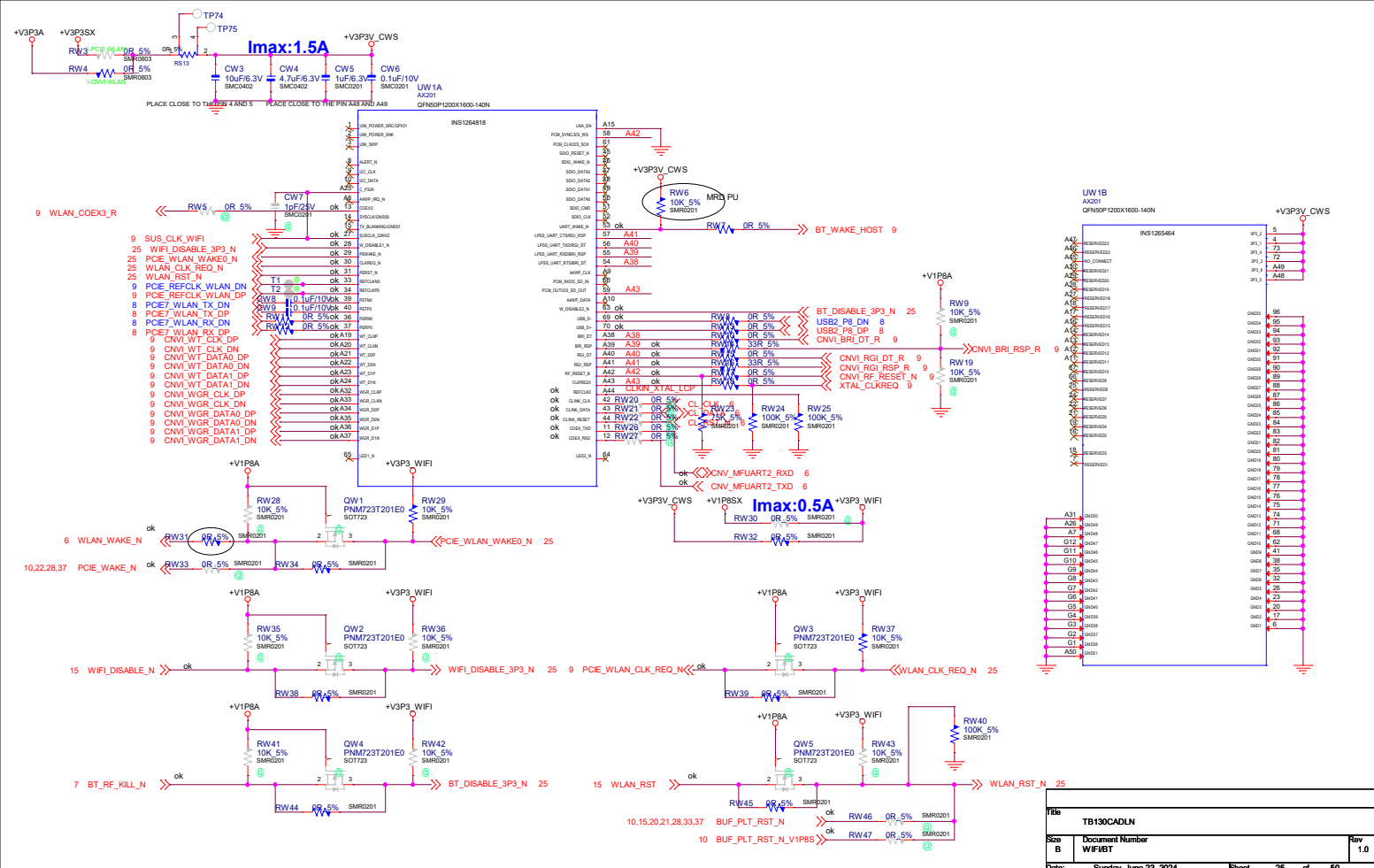
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A3	CPU FAN	1.0
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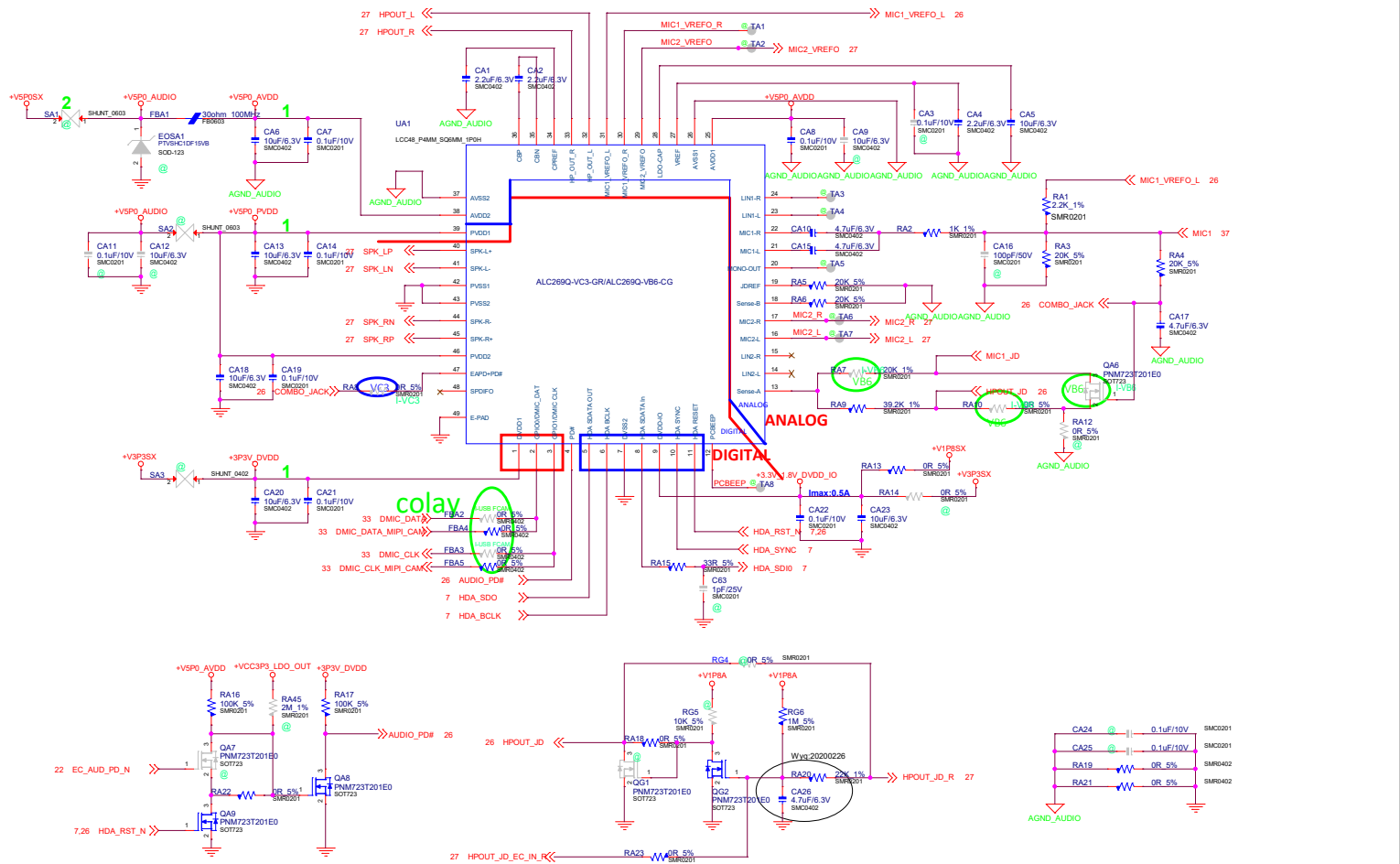


3.3V IO

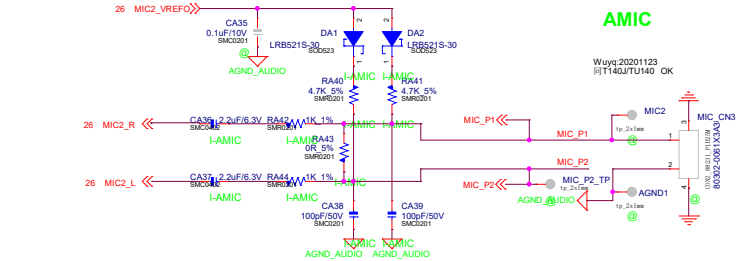
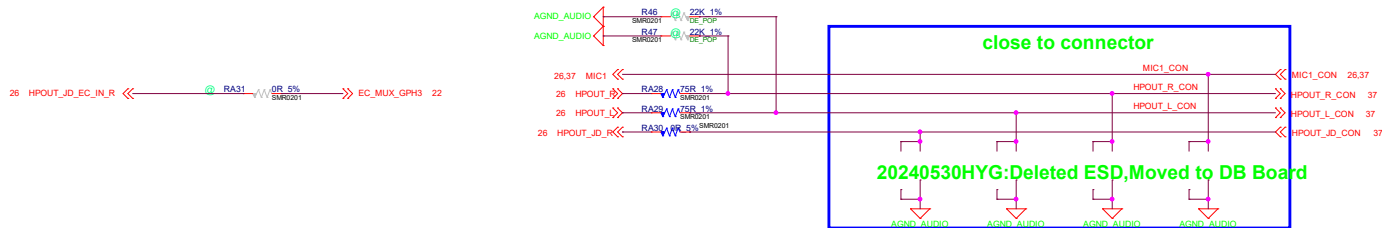
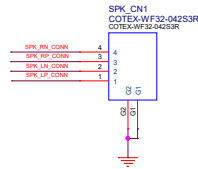
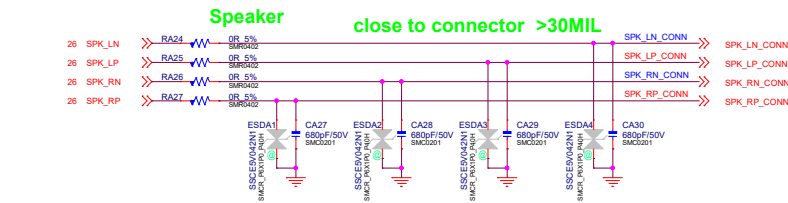


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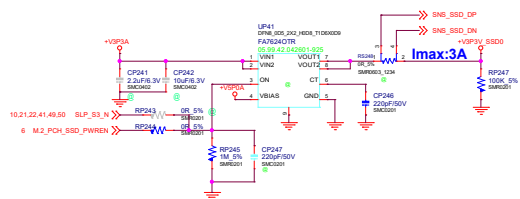




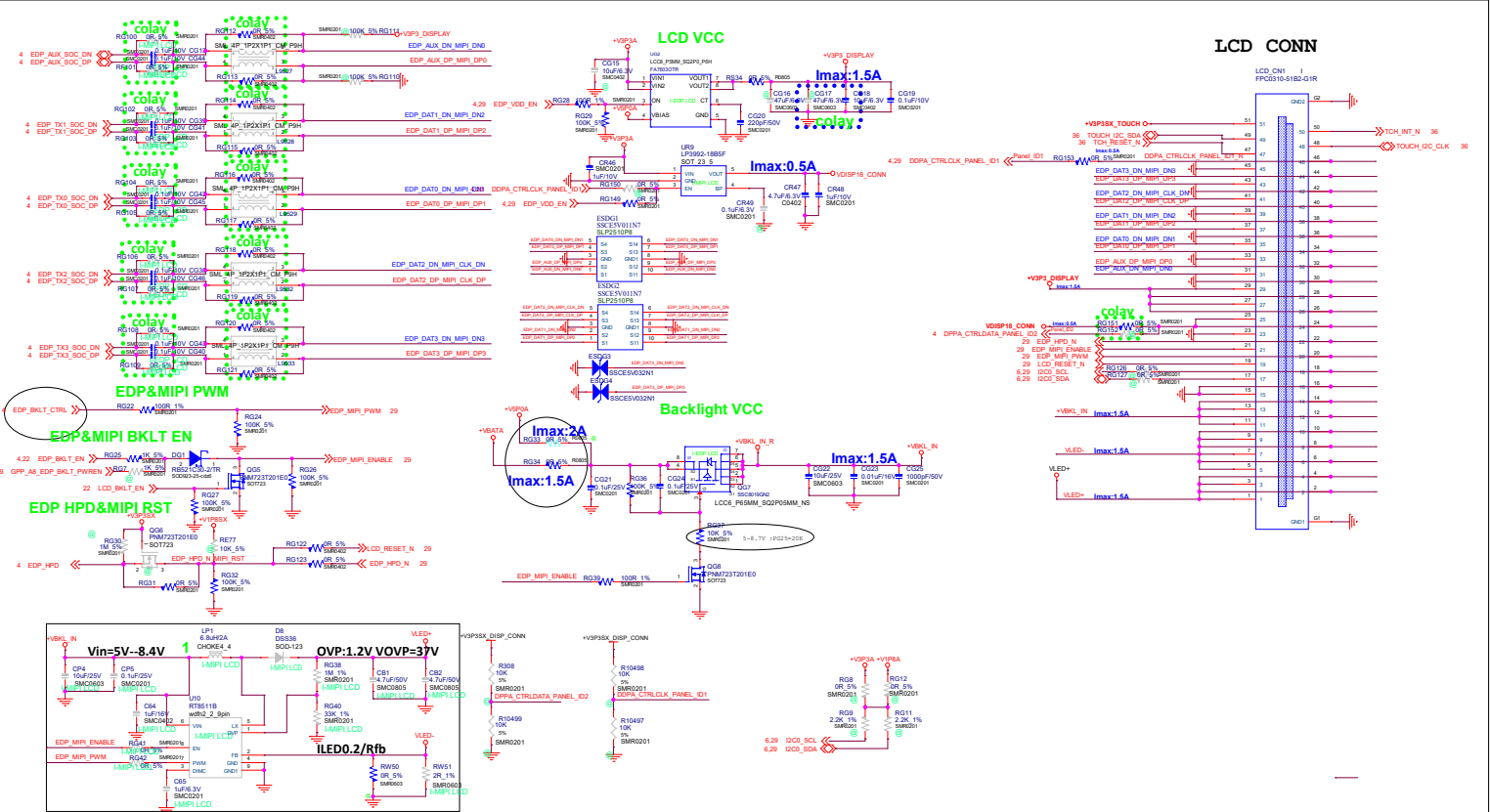
Title		
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Size	Document Number	Rev
A3	AUDIO CODEC	1.0
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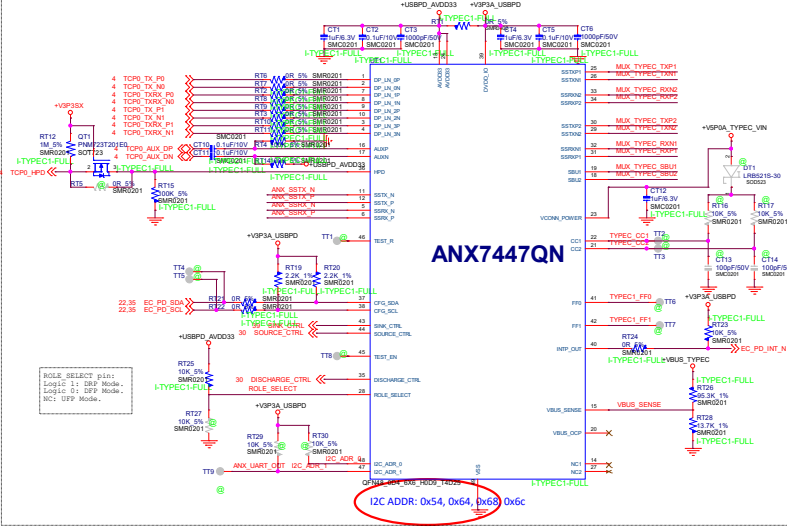


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Size	Document Number				Rev
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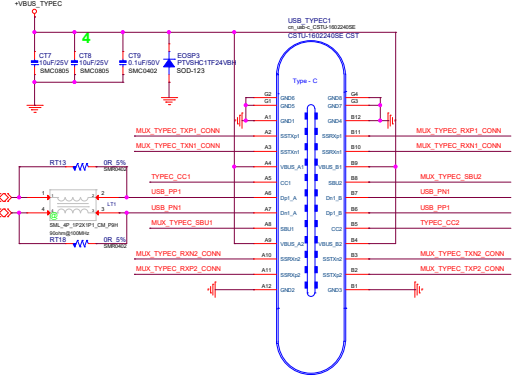


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C	EDP	
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ANX7447



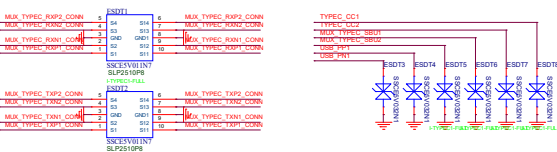
TYPEC CONN



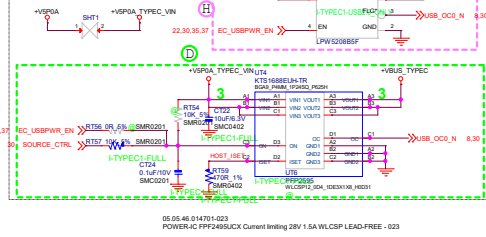
FULL FUNCTION & DATA ONLY OPTION



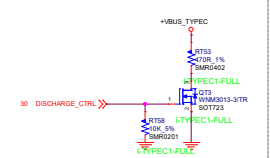
ESD Diodes



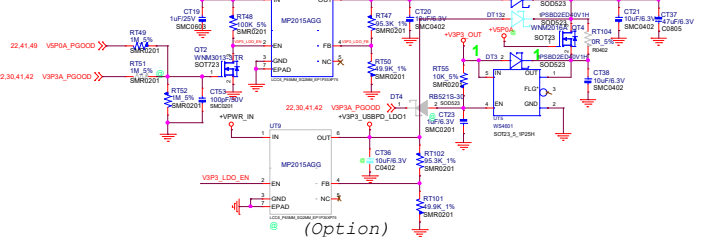
VBUS Control



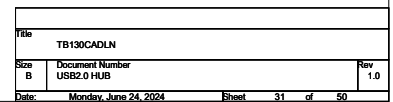
VBUS Discharge

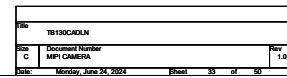


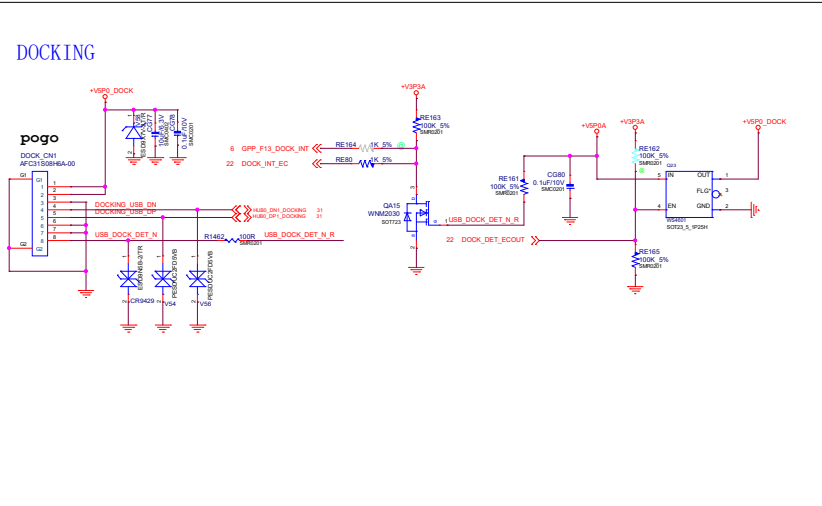
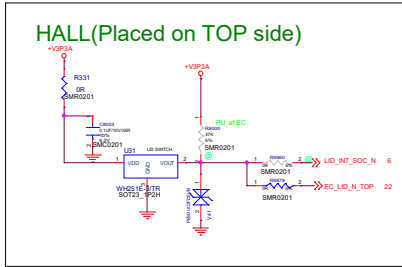
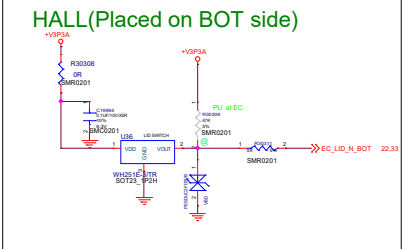
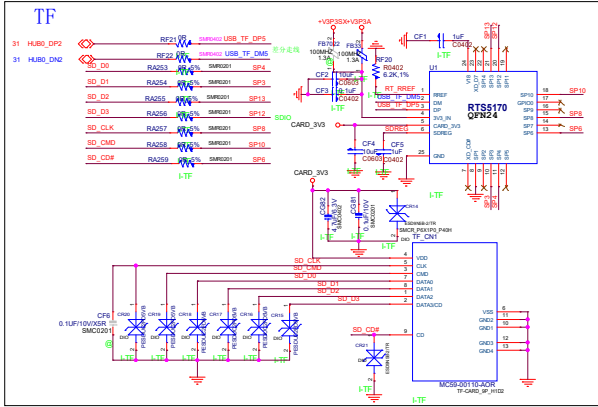
USBPD POWER



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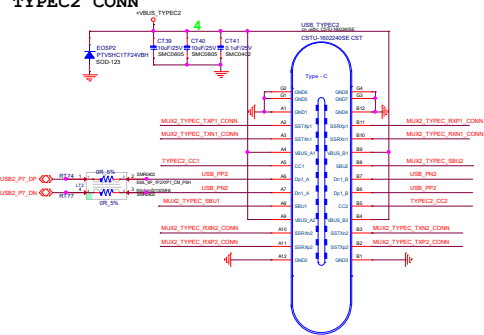






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TYPEC2 CONN



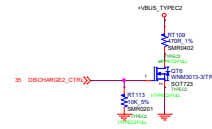
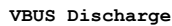
CPU



CAD NOTES:

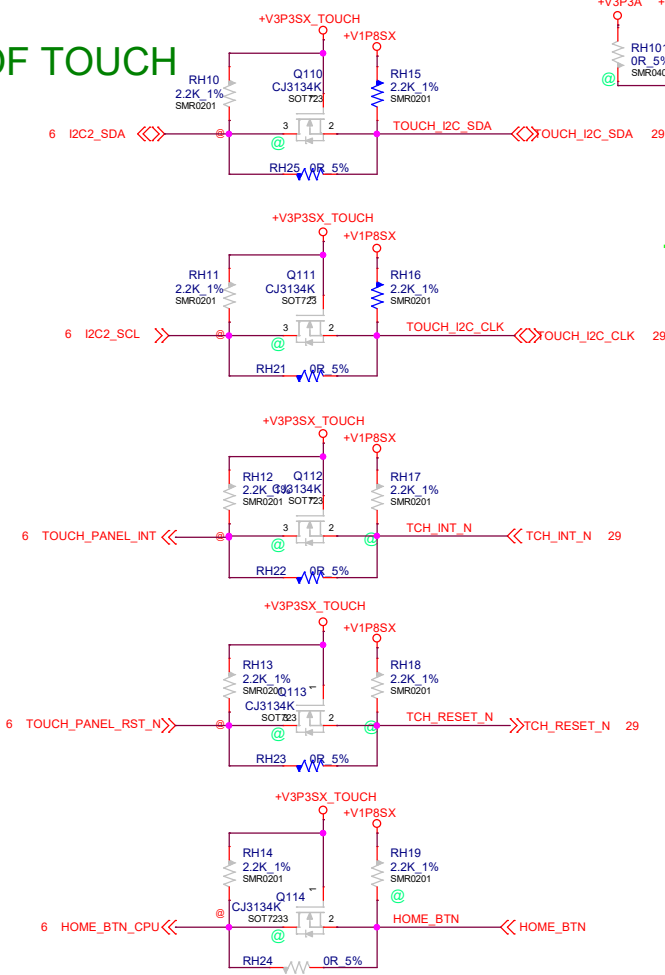
CAD NOTES:

Share PAD or VIA:	Part A & E
	Part B & F
	Part C & C

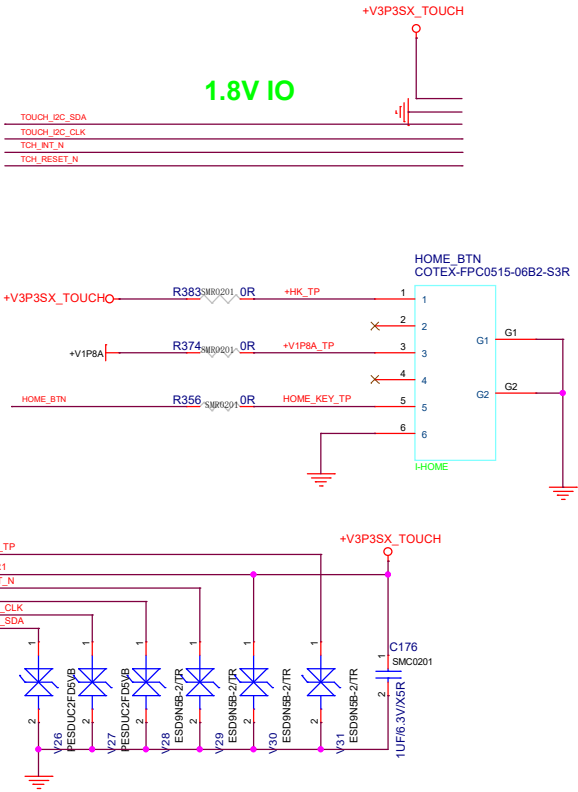


File TB130CADLN			
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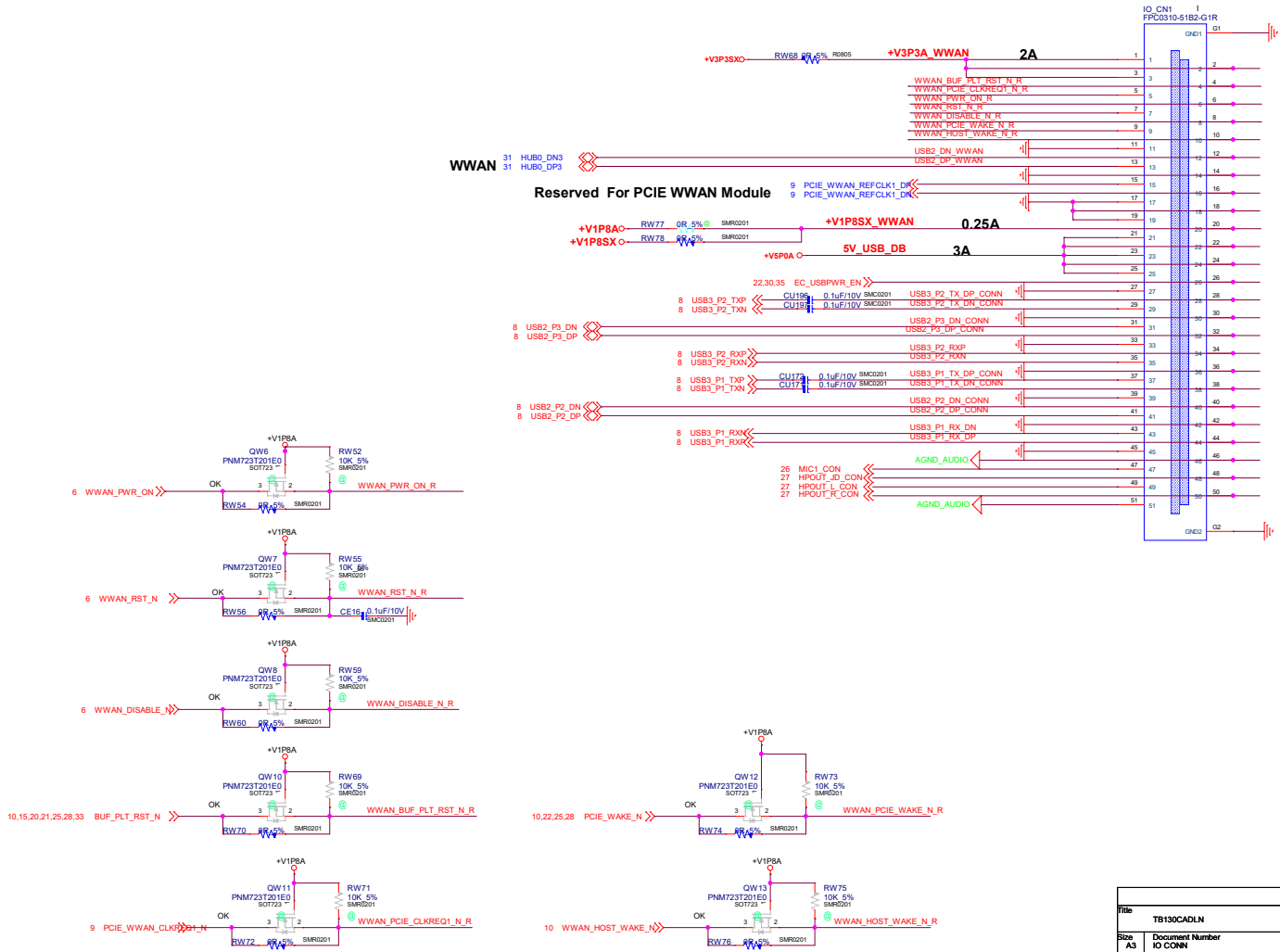
COF TOUCH



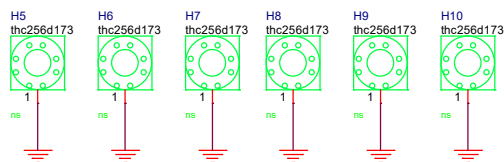
Touch panel



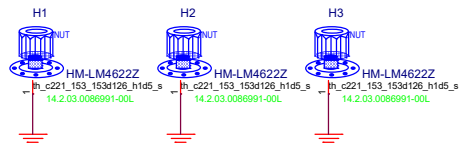
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TB130CADLN New Footprint



Same as NB133ADLL1



Same as Reference Board

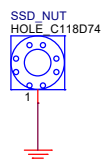
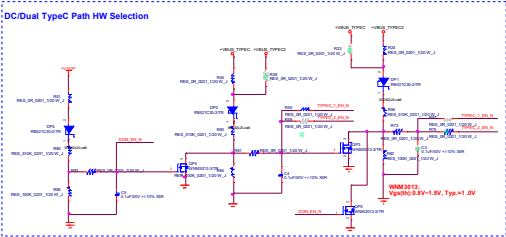
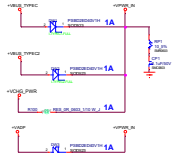
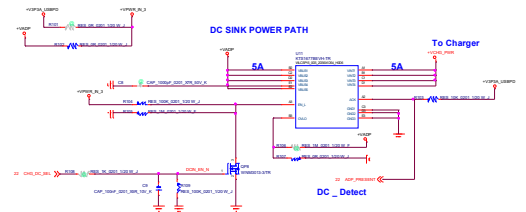
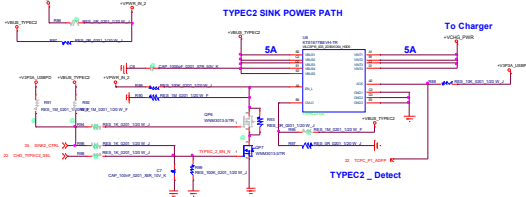
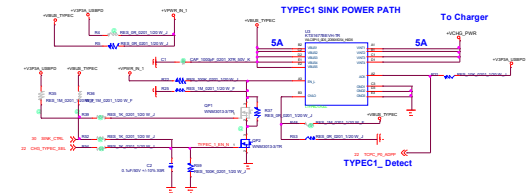


Figure 1 shows six schematic representations of FMKs (FMK1 to FMK6). Each FMK is depicted as a circle with a grey nucleus and a red 'X' on the cell membrane. A green circle with a number (1-6) is next to each. Labels 'fmarkc' and 'MARK' are present for each FMK.

[TOP](#)

BOT

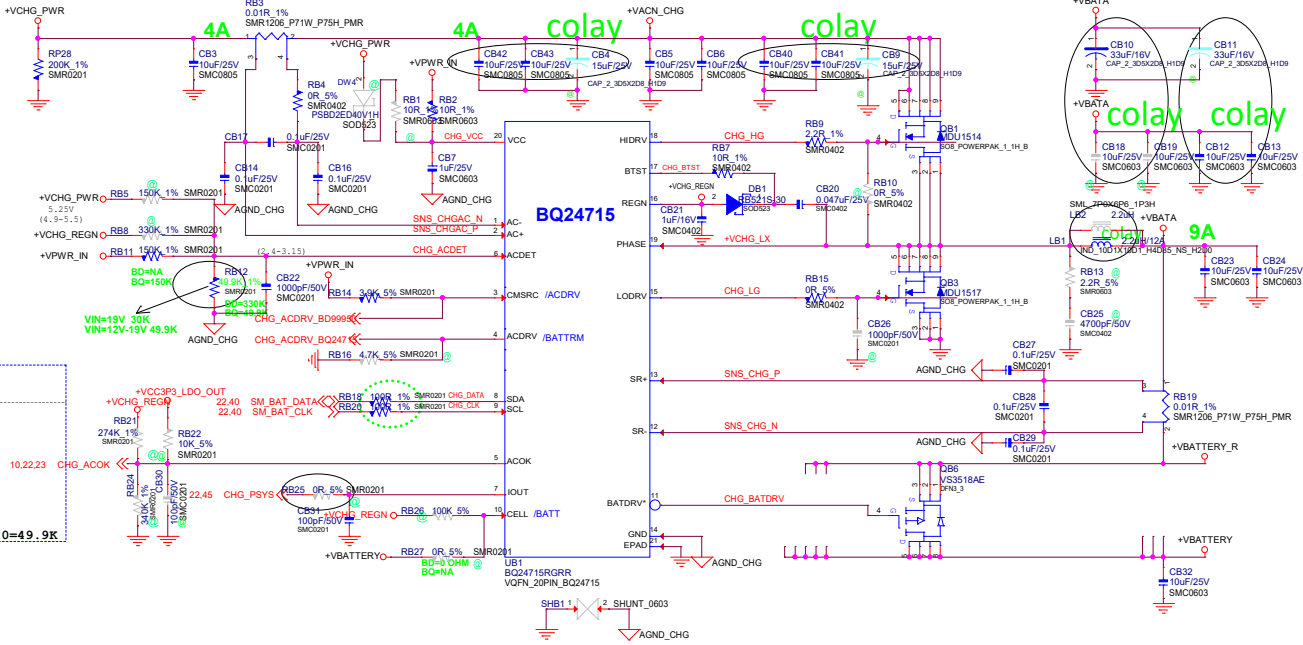
Title TB130CADLN			
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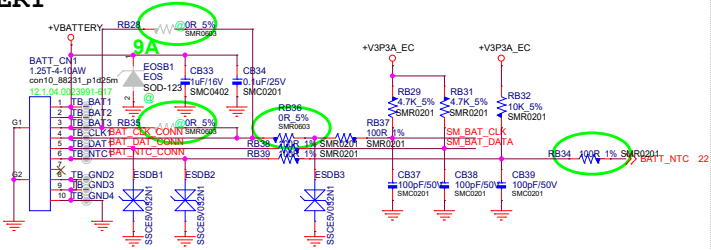
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1	DCIN Only	1	0	0
2	TYPEC1 Only	0	1	0
3	TYPEC2 Only	0	0	1
4	DCIN+TYPEC1	1	0	0
5	DCIN+TYPEC2	1	0	0
6	TYPEC1+TYPEC2	0	1	0
7	DCIN+TYPEC1+TYPEC2	1	0	0

CHARGER

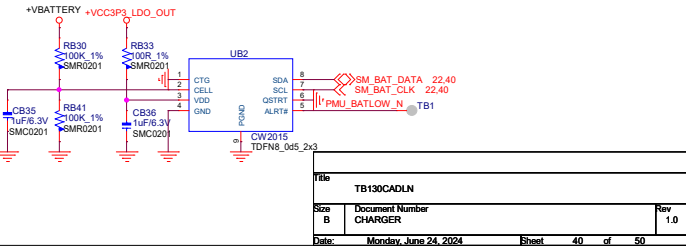
BQ24715
1:RB1=0.01Ω
2:RB23=0Ω
3:CB7=0.1μF/50V
4:RB4=3.9K RB8=NA
5:DB1=RB521S30
6:RB3=10Ω
7:CB9=0.047μF/25V
8:QB2=NA QB3=MDV3605
9:RB16=NA
10:RB6=NA RB9=150K RB10=49.9K



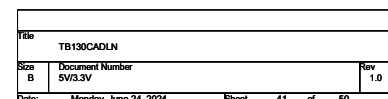
BATTERY



GAS Guage



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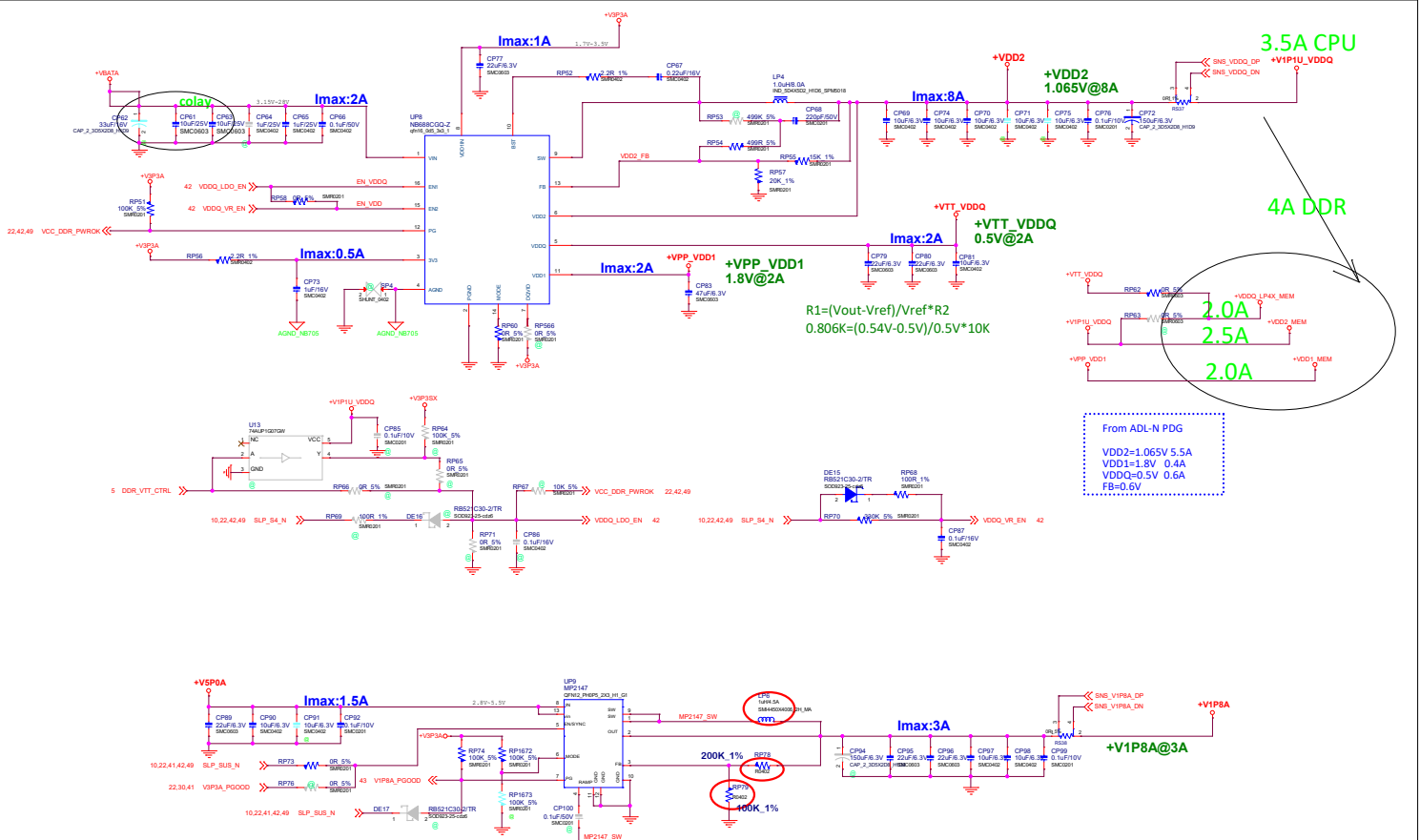
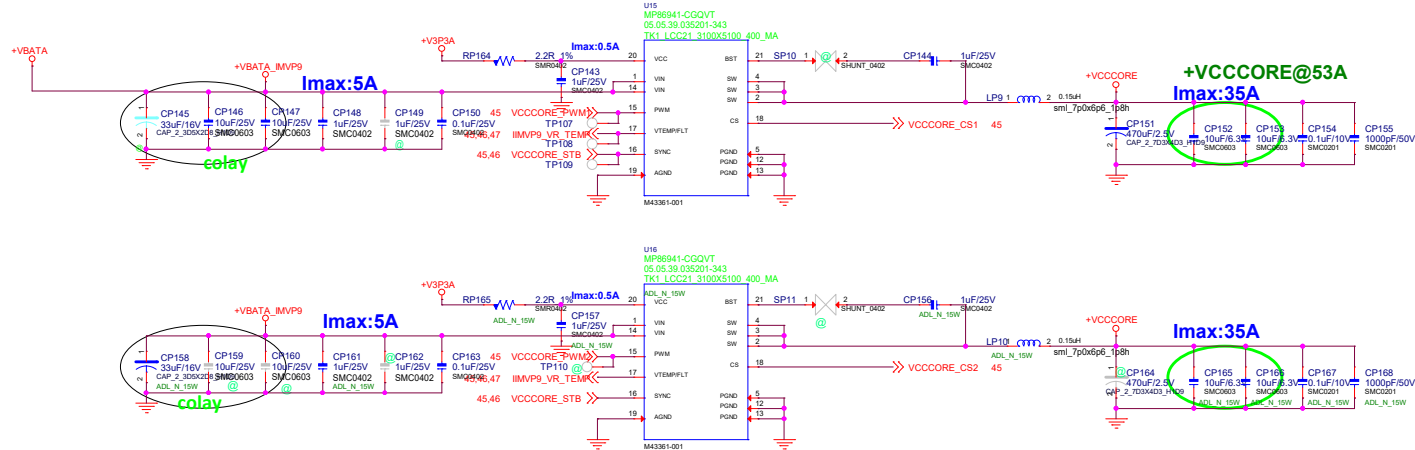


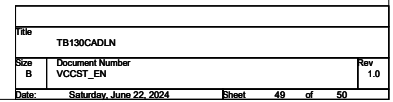
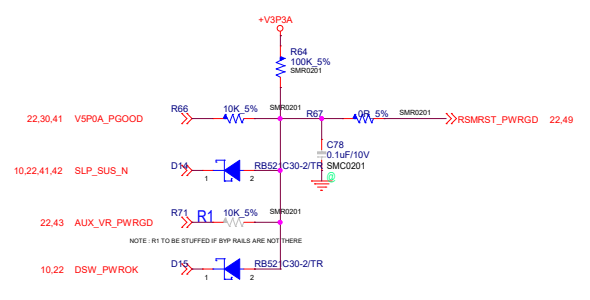
Table 1: Resistor Values for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)



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NOTE:
STUFF R3E10 FOR FIVR
STUFF R3E9 FOR MBVR



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