

MATERIAL SPECIFICATION

Title : IC INTEGRATE_ACCESS POINT_SoC IPQ-5018-0-MRQFN232-TR-01-0 MRQFN-232

1. General description

IPQ5018 is a highly integrated 802.11ax Wi-Fi/Bluetooth 5.1 system-on-chip (SoC) designed and built for high-performance, power efficient, and cost-effective wireless networking applications including home routers, mesh nodes, and gateways.

2. Electrical characteristics

Absolute maximum ratings

Parameter		Min	Max	Unit	Comments
Power supply voltages					
AVDD_PLL_1P05	Core power for PLL	-0.3	1.15	V	
DPAD_VREF_DQ	DDR DQ reference voltage	-0.3	0.891	V	
CMN_LDO_VDD18	1.8V or 1.95V analog power.	-0.3	2.057	V	
CMN_PLL_1P05	1.05V power for CMN_PLL, from 1GPHY LDO in PCB board	-0.3	1.15	V	Connect to VDD_LDO_1P05 on board
VDD1P8_QFPROM_BLOW	Power for programming Q-fuses	-0.3	2.05	V	
VDD_TOP	Core power supply	-0.3	1.42	V	
VDD_LEFT	Core power supply	-0.3	1.42	V	
VDD_RIGHT	Core power supply	-0.3	1.42	V	
VDD_BOTTOM	Core power supply	-0.3	1.42	V	
UPHY_AVDDTX	1.05V power supply for Tx and Rx digital part	-0.3	1.15	V	Connect to CMN_LDO_1P05 on board
UPHY_AVDDPLL	1.05V power supply for PLL and Rx analog part	-0.3	1.15	V	Connect to CMN_LDO_1P05 on board
PCIEX2_AVDDTX	Dual-lane PCIe PHY analog power	-0.3	1.15	V	Connect to CMN_LDO_1P05 on board
PCIEX2_AVDDPLL	Dual-lane PCIe PHY analog power	-0.3	1.15	V	Connect to CMN_LDO_1P05 on board
PCIEX2_AVDDREFCLK	Dual-lane PCIe PHY analog power	-0.3	1.15	V	Connect to CMN_LDO_1P05 on board

CH01_AVDDH_1P8	HV power for channel0 and channel1	-0.3	1.98	V	
CH23_AVDDH_1P8	HV power for channel2 and channel3	-0.3	1.98	V	
CH0_AVDD_1P05	Core power for channel0 and channel1	-0.3	1.15	V	Connect to VDD_LDO_1P05 on board
CH3_AVDD_1P05	Core power for channel2 and channel3	-0.3	1.15	V	Connect to VDD_LDO_1P05 on board

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AVDDH_LDO_1P8	LDO input HV power	-0.3	1.98	V	
VDD1P8_ADCRX0	1.8V supply for WL ADC, DAC, chain 0	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_ADCRX1	1.8V supply for WL ADC, DAC, chain 1	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_BT_TRX	Supply for BT TRX	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_BTPA	Supply for BT PA	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_BTSYN	Supply for BT Synthesizer	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_REFCLK	Supply for BT and WL BBPLL	-0.3	2.057	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_SYN	Supply for WL Synthesizer	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_WL_BB0	Supply for WL baseband, chain 0	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_WL_BB1	Supply for WL baseband, chain 1	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_WL_TPC0	Supply for WL TPC, chain 0	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_WL_TPC1	Supply for WL TPC, chain 1	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_WL_TRX0	Supply for WL TRX, chain 0	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA

VDD1P8_WL_TRX1	Supply for WL TRX, chain 1	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P8_XTAL	Supply for the XO	-0.3	2.05	V	Connect to PMU output VDD1P8_PMU_RFA
VDD1P95_PMU_IN	SWREG supply, input of PMU LDOs	-0.3	2.05	V	

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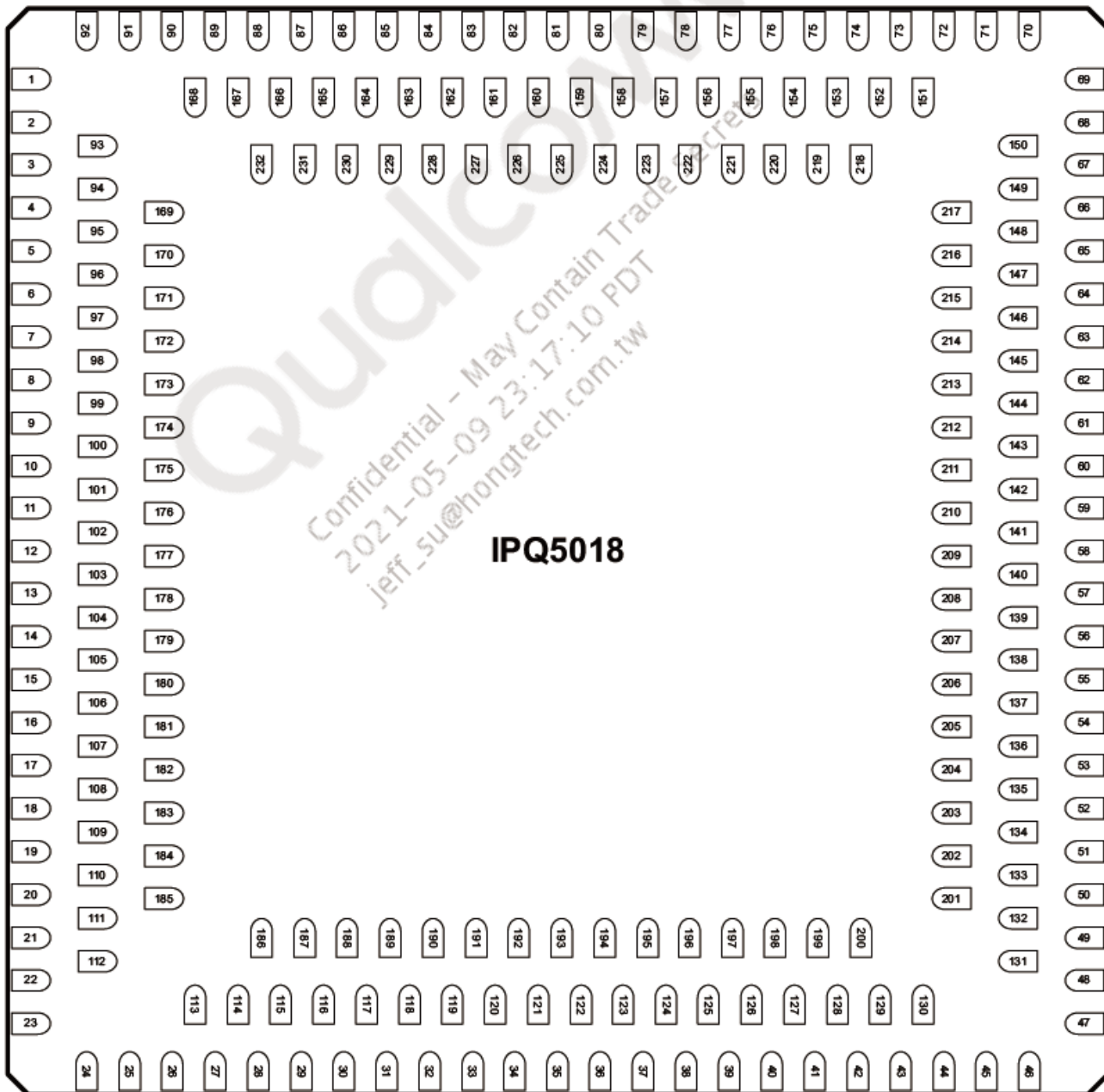
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VDD2P2_RF0	Supply for WL PA, Chain 0	-0.3	2.3	V	
VDD2P2_RF1	Supply for WL PA, Chain 1	-0.3	2.3	V	
VCC_1P8	USB 1.8V	-0.3	2.057	V	
VCC_3P3	USB 3.3V	-0.3	3.63	V	
DVDDQ_DDR_BOTTOM	DDR power supply	-0.3	1.485	V	
DVDDQ_DDR_LEFT	DDR power supply	-0.3	1.485	V	
DVDDVCO	VDD core power supply	-0.3	1.42	V	
AVDDVCO	PLL power supply	-0.3	1.155	V	
AVDD1P35	Power supply for VTT LDO	-0.3	1.485	V	
SGMII_AVDDPLL	1.05V power supply for PLL and Rx analog part	-0.3	1.15	V	Connect to VDD_LDO_1P05 on board
SGMII_AVDDTX	1.05V power supply for Tx and Rx digital part	-0.3	1.15	V	Connect to VDD_LDO_1P05 on board
VDDIO_BOTTOM_1	IO power supply	-0.3	2.09	V	
VDDIO_BOTTOM_2	IO power supply	-0.3	2.09	V	
VDDIO_LEFT	IO power supply	-0.3	2.09	V	
VDDIO_RIGHT	IO power supply	-0.3	2.09	V	
VDDIO_TOP_1	IO power supply	-0.3	2.09	V	
VDDIO_TOP_2	IO power supply	-0.3	2.09	V	
VDDIO_TOP_3	IO power supply	-0.3	2.09	V	
T _s	Storage Temperature ^{1 2}	-55	+150	°C	

3. Pin configuration

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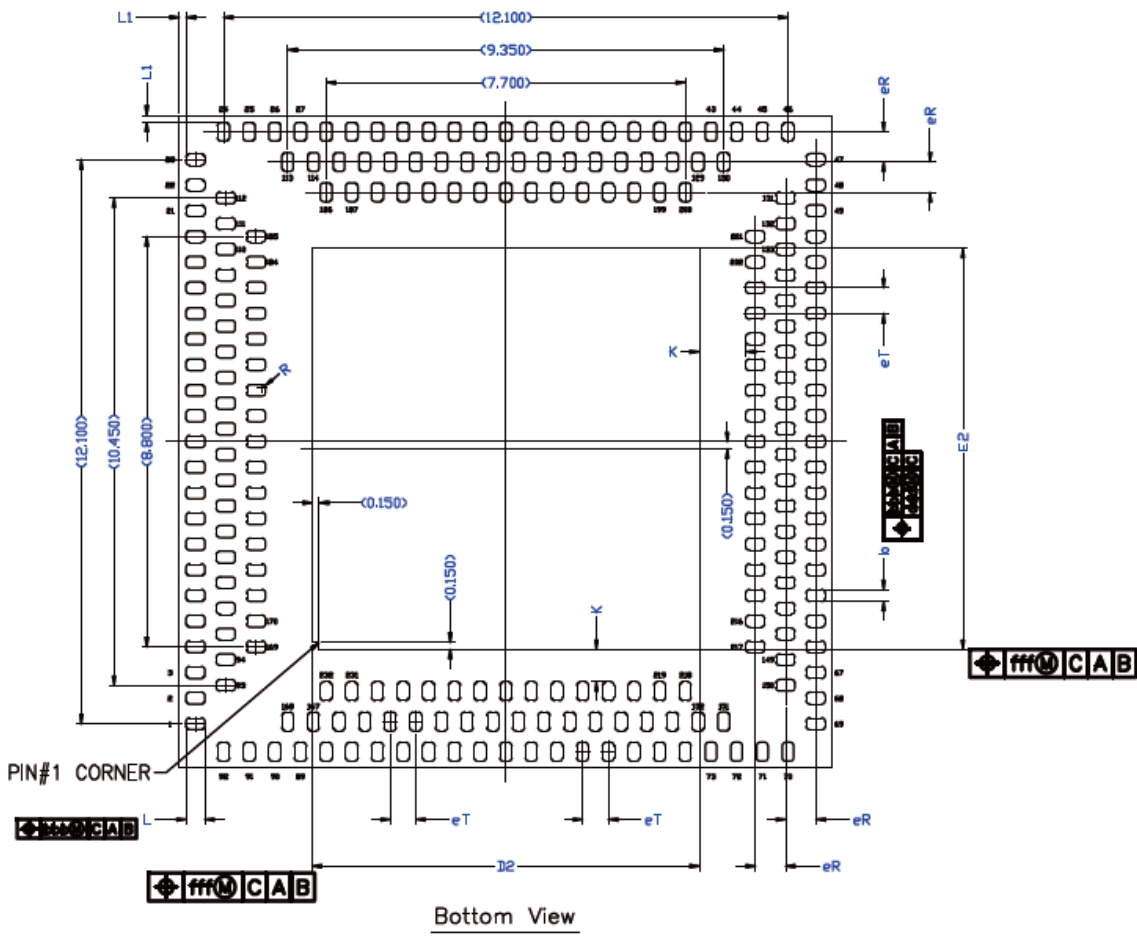
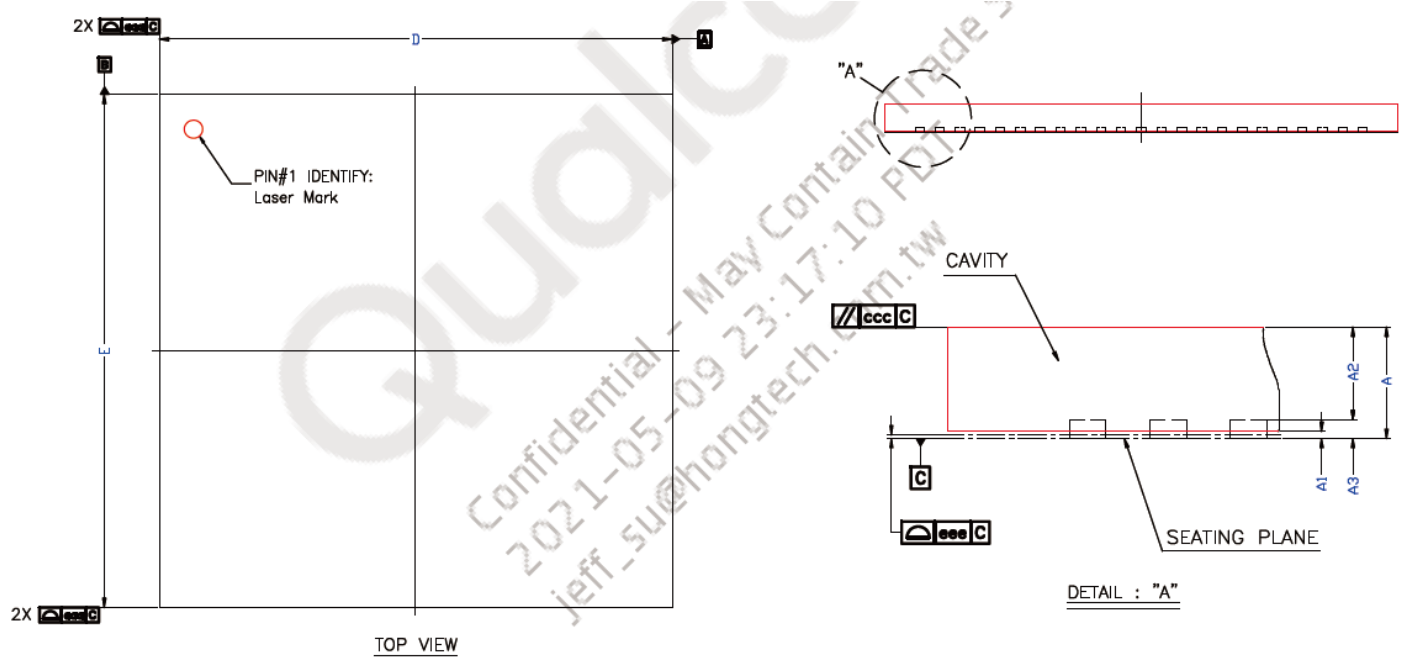
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4. Package information

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Notes:

1. N is the number of terminals.
2. Dimensioning and tolerances confirm to ASME Y14.5M. – 2009.
3. The pin #1 identifier must exist on the top surface of the package by using indentation mark or other feature of package body.
4. Bilateral coplanarity zone applies to the exposed pad as well as the terminals.
5. Applied only to terminals.

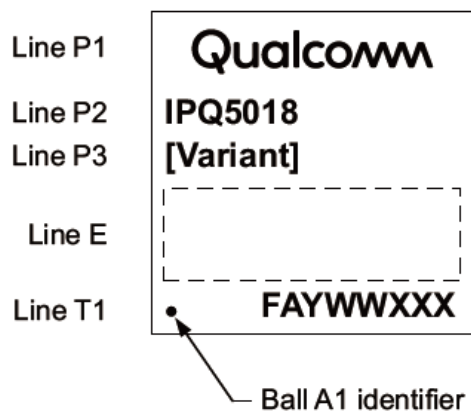
Symbol	Dimension in mm			Dimension in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.85	—	—	0.033
A1	0.02	0.05	0.08	0.001	0.002	0.003
A2	0.60	0.65	0.71	0.024	0.026	0.028
A3	0.12	0.13	0.14	0.005	0.005	0.006
D	13.90	14.00	14.10	0.547	0.551	0.555
E	13.90	14.00	14.10	0.547	0.551	0.555
D2	8.20	8.30	8.40	0.323	0.327	0.331
E2	8.50	8.60	8.70	0.335	0.339	0.343
eT	0.55 BSC			0.022 BSC		
eR	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
b	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.10	0.15	0.20	0.004	0.006	0.008
K	0.20	—	—	0.008	—	—
aaa	0.100			0.004		
bbb	0.100			0.004		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.100			0.004		
fff	0.100			0.004		
Note: Controlling dimension: millimeter						

Layout recommend 同 742A50180200

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Part marking



Line	Marking	Description
Line P1	Qualcomm	Qualcomm name
Line P2	IPQ5018	Qualcomm Technologies, Inc. product name
Line P3	[Variant]	Device variant information ■ See Table 4-3 for assigned values.
Line T1	FAYWWXXX	F = source of supply code ■ F = F (TSMC) A = assembly site code ■ A = E (ASE, Taiwan) ■ A = K (SPIL, Taiwan) Y = single/last digit of year WW = two-digit work week of year specified by Y XXX = traceability number
Pin 1	●	Ball A1 identifier
Line E		Space reserved for optional additional trace information

Table 4-5 Ordering numbers

Ordering number
IPQ-5018-0-MRQFN232-MT-01-0
IPQ-5018-0-MRQFN232-TR-01-0