



A7671

Hardware Design

LTE Module

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1. Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics, and test results of the A7671 module. With the help of this document, customers can quickly understand the A7671 module.

Referring to other software application notes and user guides, customers can use module to design and develop applications easily. SIMCom provides a set of evaluation boards to test easily and develop A7671 module. The evaluation board tools include an EVB board, a USB cable, an antenna and other peripherals.

1.1. Documentation Overview

The documents listed in Table 1 primarily cover the module's technical information. To thoroughly understand the device and its application, it is necessary to study all relevant documents.

Table 1: A7671 Series Documents Overview

No.	Document	Description
1	A7671_Hardware_Design (This document)	Mainly introducing interface functions, recommend circuit, PCB layout guidelines, packaging and other hardware components, as well as the use of AT commands
2	SIMCom_A7671 Series_Reference_Design	Reference circuit applications
3	8BE000-A7678-TE_V4.01_DL&PCB	TE SCH&PCB PDF Document
4	SIMCOM_EVB_DL&PCB	SIMCOM_EVB SCH&PCB PDF Document
5	MOD_A7671X_135	Reference Package (Pads)
6	A76XX Series_AT Command Manual	AT Command Manual
7	Module Secondary SMT Process User Guide	Module Secondary SMT Guidelines
8	SIMCOM EVB Kit User Guide	EVB Kit User Guide Document
9	A76XX_Series_CAT1_Module_Schematic&Layout_checklist	Peripheral circuit schematic and PCB checklist

NOTE

This current revision is an early release to support initial product developers. The content is subject to change without advance notice.

1.2. Product Outline

The module supports LTE-FDD and LTE-TDD. The supported radio frequency bands are described in the following table.

Table 2: Module Frequency Bands

Standard	Frequency	A7671			
		A7671G	A7671S	A7671E	A7671SA
LTE-FDD	LTE-FDD B1	✓	✓	✓	✓
	LTE-FDD B2	✓			✓
	LTE-FDD B3	✓	✓	✓	✓
	LTE-FDD B4	✓			✓
	LTE-FDD B5	✓	✓	✓	✓
	LTE-FDD B7	✓		✓	✓
	LTE-FDD B8	✓	✓	✓	✓
	LTE-FDD B12	✓			
	LTE-FDD B13	✓			
	LTE-FDD B18	✓			
	LTE-FDD B19	✓			
	LTE-FDD B20	✓		✓	
	LTE-FDD B25	✓			
	LTE-FDD B26	✓			
	LTE-FDD B28	✓		✓	✓
	LTE-FDD B66	✓			✓
	LTE-FDD B71	✓			
LTE-TDD	LTE-TDD B34	✓	✓		
	LTE-TDD B38	✓	✓		
	LTE-TDD B39	✓	✓		
	LTE-TDD B40	✓	✓		
	LTE-TDD B41	✓	✓		

Category CAT1

Table 3: Module Feature Difference

Function	MNXV	LNXV
USIM	✓	✓
GNSS	✓	
SMS	✓	✓
Wi-Fi Scan	✓	✓
FOTA	✓	✓

NOTE

The functions supported by the module are subject to the actual hardware model and software version.

With a small physical dimension of 24*24*2.4mm, the module can meet almost any space requirement in customers' applications, such as telematics, surveillance devices, industrial routers remote diagnostics, etc.

The module provides 134 pins, including 80 LCC pins in the outer ring and 54 LGA pins in the inner ring. This document will introduce all the functional pins.

1.3. Hardware Interface Overview

The interfaces are described in detail in the following chapters, including:

- Power supply
- USB 2.0 interface
- Three UART interfaces, one full function serial port, one ordinary serial port and one debug serial port.
- One USIM interface
- One I2C interface
- ADC interface * 2
- SPI interface(Customized software)
- General input and output interfaces (GPIOs)
- LCD interface(Customized software)
- USB boot download and guidance interface
- One analog audio output interface (Customized software)
- Module operation status indication interface
- Network status indication interface
- Power on self-start interface

- Antenna interface
- GNSS antenna interface(Optional)

1.4. Hardware Block Diagram

The block diagram of the A7671 module is shown in the figure below.

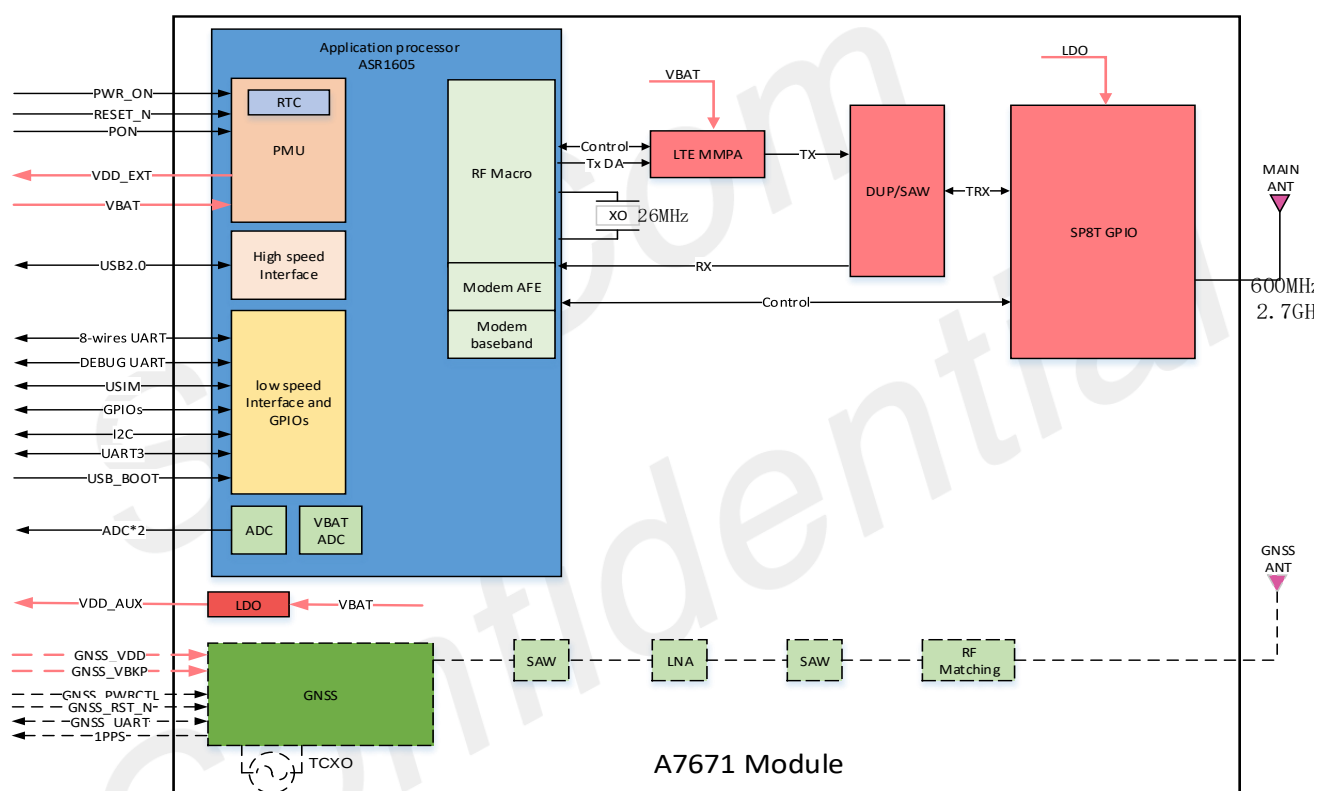


Figure 1: Block Diagram

1.5. Functional Overview

Table 4: General Features

Feature	Implementation
Power supply	VBAT: 3.3V~4.2V, Recommended VBAT: 3.8V
Power saving	Current in Sleep mode@DRX=0.32S typical: 1.5mA

	Current in Sleep mode@DRX=0.64S typical: 1.1mA Current in Sleep mode@DRX=1.28S typical: 1mA Current in Sleep mode@DRX=2.56S typical: 0.9mA Current in PSM mode typical: 6uA Please refer to the table 60
Radio frequency bands	Please refer to the table 2
Transmitting power	LTE power level: 3 (23dBm±2.7dB)
Data Transmission Throughput	FDD-LTE category 1 : 10 Mbps (DL), 5 Mbps (UL) TDD-LTE category 1 : 8 Mbps (DL), 3 Mbps (UL)
Antenna	LTE antenna interface GNSS antenna interface(optional)
SMS	MT, MO, CB, Text, PDU mode Short Message (SMS) storage device: USIM Card, CB does not support saving in SIM Card Support CS and PS domain SMS
USIM interface	Support identity card: 1.8V/ 3V
USIM application toolkit	Support SAT class 3 Support USAT
Phonebook management	Support phonebook types: SM/FD/ON/AP/SDN
RTC	Support RTC for alarm clock, timer, auto power-on by alarm clock or other functions
Audio feature	Support one analog audio output interface
I2C interface	Support I2C interface Comply with I2C bus protocol specification Multi host mode not supported
UART interface	● Full function serial port Baud rate support from 300bps to 3686400bps AT command and data can be sent through serial port Support RTS/CTS hardware flow control ● Debug serial port Support debug function ● UART3 serial port Ordinary two-wire serial port
USB	Compliant with USB 2.0 specification and supports slave mode but not master mode. This interface can be used for AT command sending, data transmission, software debugging and upgrading.
Firmware upgrade	Firmware upgrade via USB/FOTA
Physical characteristics	Size: 24(±0.15)mm*24(±0.15)mm*2.4(±0.2)mm Weight: 2.8±0.1g
Temperature range	Normal operation temperature: -30°C to +75°C Extended operation temperature: -40°C to +85°C* Storage temperature: -40°C to +90°C

NOTE

When the module is within the extended operation temperature range, module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

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2. Package Information

2.1. Pin Assignment Overview

The following figure is a top view of the pin assignment of the module for A7671.

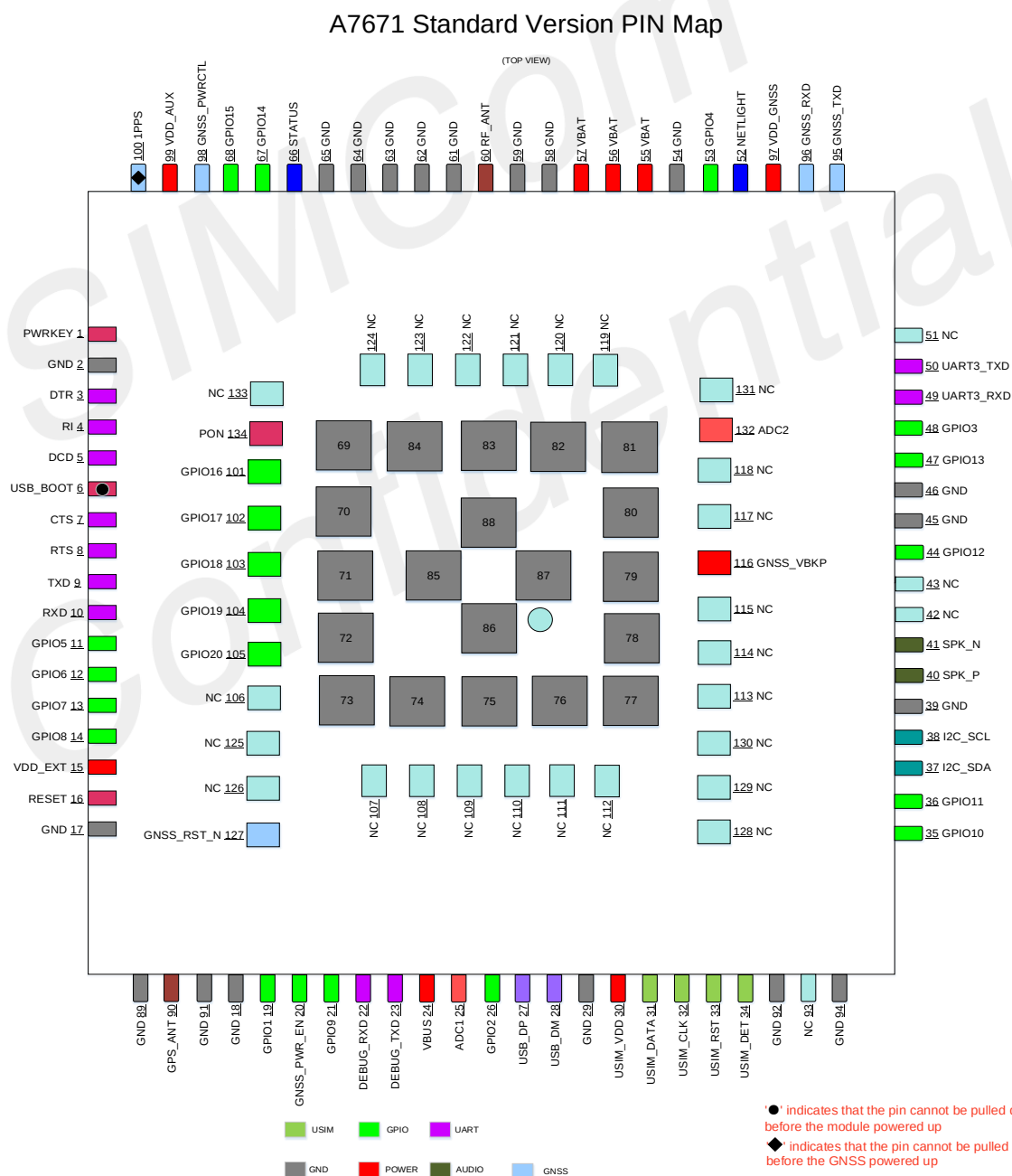


Figure 2: Pin Assignment Overview

Table 5: Pin Description

PIN NO	PIN NAME	PIN NO	PIN NAME
1	PWRKEY	2	GND
3	DTR	4	RI
5	DCD	6	USB_BOOT●
7	CTS	8	RTS
9	TXD	10	RXD
11	GPIO5	12	GPIO6
13	GPIO7	14	GPIO8
15	VDD_EXT	16	RESET
17	GND	18	GND
19	GPIO1	20	GNSS_PWR_EN
21	GPIO9	22	DEBUG_RXD
23	DEBUG_TXD	24	VBUS
25	ADC1	26	GPIO2
27	USB_DP	28	USB_DM
29	GND	30	USIM_VDD
31	USIM_DATA	32	USIM_CLK
33	USIM_RST	34	USIM_DET
35	GPIO10	36	GPIO11
37	I2C_SDA	38	I2C_SCL
39	GND	40	SPK_P
41	SPK_N	42	NC
43	NC	44	GPIO12
45	GND	46	GND
47	GPIO13	48	GPIO3
49	UART3_RXD	50	UART3_TXD
51	NC	52	NETLIGHT
53	GPIO4	54	GND
55	VBAT	56	VBAT
57	VBAT	58	GND
59	GND	60	RF_ANT
61	GND	62	GND
63	GND	64	GND
65	GND	66	STATUS
67	GPIO14	68	GPIO15
69	GND	70	GND
71	GND	72	GND
73	GND	74	GND

75	GND	76	GND
77	GND	78	GND
79	GND	80	GND
81	GND	82	GND
83	GND	84	GND
85	GND	86	GND
87	GND	88	GND
89	GND	90	GNSS_ANT
91	GND	92	GND
93	NC	94	GND
95	GNSS_TXD	96	GNSS_RXD
97	VDD_GNSS	98	GNSS_PWRCTL
99	VDD_AUX	100	1PPS◆
101	GPIO16	102	GPIO17
103	GPIO18	104	GPIO19
105	GPIO20	106	NC
107	NC	108	NC
109	NC	110	NC
111	NC	112	NC
113	NC	114	NC
115	NC	116	GNSS_VBKP
117	NC	118	NC
119	NC	120	NC
121	NC	122	NC
123	NC	124	NC
125	NC	126	NC
127	GNSS_RST_N	128	NC
129	NC	130	NC
131	NC	132	ADC2
133	NC	134	PON

NOTE

1. '●' Indicates that the pin cannot be pulled down before the module powered up. Otherwise, it will affect the normal start-up of the module.
2. '◆' Indicates that the pin cannot be pulled up before the GNSS powered up. Otherwise, it will affect the normal start-up of the GNSS.
3. NC: NOT CONNECT. Do not connect them to GND.
4. The round dot PIN is only for internal use within SIMCom and does not require the design of solder pads. Please refer to section 6.3 and 6.4.

2.2. Pin Description

Table 6: Pin Parameter Abbreviation

Pin type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input
DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down
OD	Open Drain

Table 7: 1.8V IO Parameters Definition

Power Domain	Parameter	Description	Min.	Typ.	Max.
1.8V	V _{IH}	High level input	VCC * 0.65	1.8V	1.98V
	V _{IL}	Low level input	-0.3V	0V	VCC * 0.35
	R _{pu}	Pull up resistor	55K	79 K	121K
	R _{pd}	Pull down resistor	51K	87 K	169K
	I _{IL}	Input leakage current	-	-	10uA
	V _{OH}	Output level range	1.35V	-	-
	V _{OL}	Output low range	-	-	0.45V
	I _{OL}	Maximum current driving capacity at low level output Vpad=0.2V I _{OL} DCS[1:0]=			
		00	7.6mA	12.8mA	18.0mA
		01	15.2mA	25.3mA	35.5mA
		10	22.6mA	37.4mA	52.2mA
		11	29.7mA	49.0mA	67.9mA
	I _{OH}	Maximum current driving capacity at			

	high level output $V_{pad}=VCC-0.2V$ $I_{OH} DCS[1:0]=$			
	00	4.8mA	10.8mA	18.9mA
	01	9.5mA	21.5mA	37.4mA
	10	14.3mA	32.1mA	55.9mA
	11	18.9mA	42.4mA	73.9mA

Table 8: 3.0V IO Parameters Definition

Power Domain	Parameter	Description	Min.	Typ.	Max.
3.0V	V_{IH}	High level input	2V	VCC	$VCC+0.3$
	V_{IL}	Low level input	-0.3V	0V	0.8V
	R_{pu}	Pull up resistor	26K	47K	72K
	R_{pd}	Pull down resistor	27K	54K	267K
	I_{IL}	Input leakage current	-	-	2uA
	V_{OH}	Output level range	2.4V	-	-
	V_{OL}	Output low range	-	-	0.4V
	I_{OL}	Maximum current driving capacity at low level output $V_{pad}=0.4V$ $I_{OL} DS[2:0]=$			
		000	3.1mA	5.5mA	8.6mA
		001	4.7mA	8.2mA	12.7mA
		010	6.2mA	10.8mA	16.9mA
		011	7.7mA	13.4mA	20.8mA
		100	9.3mA	16.1mA	24.9mA
		101	10.8mA	18.7mA	28.8mA
		110	12.3mA	21.2mA	32.6mA
		111	13.8mA	23.7mA	36.3mA
	I_{OH}	Maximum current driving capacity at high level output $V_{pad}=VCC-0.5V$ $I_{OH} DS[2:0]=$			
		000	5.0mA	7.5mA	10.5mA
		001	7.5mA	11.2mA	15.7mA
		010	10.1mA	14.9mA	21.0mA
		011	12.6mA	18.6mA	26.2mA
		100	15.1mA	22.3mA	31.4mA
		101	17.6mA	26.0mA	36.5mA
		110	20.1mA	29.8mA	41.8mA
		111	22.6mA	33.4mA	46.9mA

Table 9: Pin Description

Pin Name	Pin No.	Pin Parameter		Description	Note
		Power Domain	Type		
Power Supply					
VBAT	55,56,57	-	PI	Module input voltage ranges from 3.3V to 4.2V, typical values is 3.8V.	
VDD_EXT	15	-	PO	1.8V power output, output current up to 50 mA.	Default on. If unused, keep it open.
VDD_AUX	99	-	PO	3.0V power output, output current up to 50 mA.	If unused, keep it open.
GND	2,17,18,29,39,45,46,54,58,59,61,62,63,64,65,69,70,71,72,73,74,75,76,77,78,79,80,81,82,83,84,85,86,87,88,89,91,92,94	-	-	Ground	
System Control					
PWRKEY	1	-	DI,PU	Power ON/OFF input, active low.	Default high V _{IH} : 0.7*VBAT V _{IL} : 0.3*VDD_EXT It has been internally pulled up to the VBAT with 50K (Typical).
RESET	16	-	DI,PU	System reset control input, active low.	Default high V _{IH} : 0.7*VBAT V _{IL} : 0.5V It has been internally pulled up to the VBAT with 50K (Typical).
USIM Interface					
USIM_DET	34	1.8V	DI	USIM card insert detect.	It can be set to high/low active with the AT command, refer to Document [18].
USIM_DATA	31	1.8/3.0V	DIO	USIM data signal.	This pin has been

					pull-up with 4.7K Ω resistor to USIM_VDD internally.
USIM_CLK	32	1.8/3.0V	DO	USIM clock signal.	
USIM_RST	33	1.8/3.0V	DO	USIM reset signal.	
USIM_VDD	30	1.8/3.0V	PO	USIM card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.

USB Interface

VBUS	24	-	PI	Valid USB detection input. Active high, $V_{min}=3.0V$, $V_{max}=5.2V$, $V_{norm}=5V$.	
USB_DN	28	-	AIO	Negative electrode of the differential, bi-directional USB signal.	
USB_DP	27	-	AIO	Positive electrode of the differential, bi-directional USB signal.	

Full Function UART Interface

TXD	9	1.8V	DOH	Data output	If unused, keep it open.
RXD	10	1.8V	DI	Data input	
RTS	8	1.8V	DI	RTS input	Connect to the RTS of DTE. If unused, keep it open.
CTS	7	1.8V	DO	CTS output	Connect to the CTS of DTE. If unused, keep it open.
DCD	5	1.8V	DO	Carrier detection	If unused, keep it open.
DTR	3	1.8V	DI	DTE Ready	
RI	4	1.8V	DO	Ringing indicator	

Debug UART

DEBUG_RXD	22	1.8V	DI	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DEBUG_TXD	23	1.8V	DOH		

Serial Port UART3

UART3_TXD	50	1.8V	DO	Data output	Two-wire serial port.
UART3_RXD	49	1.8V	DI	Data input	

I2C Interface

I2C_SDA	37	1.8V	OD	I2C data IO	If unused, keep it open. Need pull up to VDD_EXT.
I2C_SCL	38	1.8V	OD	I2C clock output	

Analog Audio Interface

SPK_P	40	-	AO	Audio receiver output positive	
SPK_N	41	-	AO	Audio receiver output negative	

GPIO

GPIO1	19	1.8V	IO,PD	General purpose I/O	If unused, keep it open.
GPIO2	26	1.8V	IO,PD	General purpose I/O	
GPIO3	48	1.8V	IO,PU	General purpose I/O	
GPIO4*	53	1.8V	IO,PU	General purpose I/O	
GPIO5	11	1.8V	IO,PD	General purpose I/O	
GPIO6	12	1.8V	IO,PD	General purpose I/O	
GPIO7	13	1.8V	IO,PD	General purpose I/O	
GPIO8	14	1.8V	IO,PD	General purpose I/O	
GPIO9	21	1.8V	IO,PD	General purpose I/O	
GPIO10	35	1.8V	IO,PU	General purpose I/O	
GPIO11	36	1.8V	IO,PU	General purpose I/O	
GPIO12	44	1.8V	IO,PD	General purpose I/O	
GPIO13	47	1.8V	IO,PD	General purpose I/O	
GPIO14	67	1.8V	IO,PD	General purpose I/O	
GPIO15	68	1.8V	IO,PD	General purpose I/O	
GPIO16	101	1.8V	IO,PD	General purpose I/O	
GPIO17	102	1.8V	IO,PD	General purpose I/O	
GPIO18	103	1.8V	IO,PU	General purpose I/O	
GPIO19	104	1.8V	IO,PU	General purpose I/O	
GPIO20	105	1.8V	IO,PD	General purpose I/O	

GNSS

GNSS_VBKP	116	-	PI	GNSS VRTC power input, input voltage 1.62V~3.6V, recommend 2.8V power supply.	It is necessary for GNSS function!
VDD_GNSS	97	1.8V	DO	The power input for GNSS.	Module VDD_EXT (PIN 15) can be used for this power supply.
GNSS_PWRC TL	98	1.8V	DI	The enable control PIN of GNSS VIO/Vcore power supply.	Active high.
GNSS_RXD	96	1.8V	DI	GNSS UART RX	Connect to MCU

					UART_TXD; Or use 1K resistor in series in module AUX_UART_TXD (PIN 50).
GNSS_TXD	95	1.8V	DO	GNSS UART TX	Connect to MCU UART_RXD; Or use 1K resistor in series in module AUX_UART_RXD (PIN 49).
GNSS_RST_N	127	1.8V	AI	GNSS RST interface	Internal pull up, active low.
1PPS◆	100	1.8V	DO	1PPS signal output	Seconds pulse signal, do not pull up before GNSS power up. It can be used for accurate timing. Output pulse signal approximately 6 seconds after successful positioning. If unused, keep it open.

ANT Interface

RF_ANT	60	-	AIO	Main antenna	
GNSS_ANT	90	-	AIO	GNSS antenna	

Other Pins

ADC1	25	-	AI	General Purpose ADC	Voltage input range 0-1.2 V.
ADC2	132	-	AI	General Purpose ADC	Voltage input range 0-1.2 V.
NETLIGHT*	52	1.8V	DO	Network registration status indicator (LED).	
STATUS	66	1.8V	DO	Module status indicator (LED).	
USB_BOOT●	6	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	It is recommended to place a test point for easy debugging and upgrade. Do not pull down before normal boot.
GNSS_PWR_EN	20	1.8V	DO	Only can be connect to GNSS_PWRCTRL.	
PON	134	VBAT	AI	Automatic power on control pin.	If unused, keep it open.
NC	51,93,106,107,108,109,110,111,112,113,	-	-	Not connect	

114,115,117,
118,119,120,
121,122,123,
124,125,126,
128,129,130,
131,133

NOTE

1. Please reserve a test point for USB_BOOT, GND, DEBUG_TXD and VDD_EXT. If there is no USB connector, please also reserve a test point for USB_VBUS, USB_DP, and USB_DN for firmware upgrading.
2. '●' Indicates that the pin cannot be pulled down before the module powered on. Otherwise, it will affect the normal start-up of the module.
3. '◆' Indicates that the pin cannot be pulled up before the GNSS powered on. Otherwise, it will affect the normal start-up of the GNSS.
4. 33pF capacitor must be connected in parallel near PIN 52(NETLIGHT) and PIN 53(GPIO4).
5. The UART_CTS pin will be pulled low after power-on if USB is connected. Therefore, it is not recommended to use this pin to control external circuits, in order to avoid unexpected behavior or logic conflicts.

The following figure shows the package outline drawing of A7671.



The side length dimension is excluding the burr area.

3. Interface Application

3.1. Power Supply

The module offers 3 power supply pins (55, 56, 57) as VBAT power input pin. A7671 supplies power to the internal RF and baseband circuits through these 3 pins.

When the module is transmitting at maximum power in LTE mode, the current can reach up to a peak current, please ensure that the external power supply capacity is no less than 1.2A.

Table 10: Power Interface Pins Definition

Pin Name	Pin No.	Type	Description	Note
VBAT	55,56,57	PI	Module power input	The input voltage range is 3.3V~4.2V, and the external power supply needs to provide a current carrying capacity of 1.2A.
GND	2,17,18,29,39,45,46,54,58,59,61~65,69~88,89,91,92,94			

Table 11: VBAT Pins Electronic Characteristic

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Module supply voltage	3.3	3.8	4.2	V
I _{VBAT (peak)}	Module consumption peak current	-	-	1	A
I _{VBAT (average)}	Module average consumption current (idle mode)	-	9	-	mA
I _{VBAT (sleep)}	Current in Sleep mode@DRX=0.32S	-	1.5	-	mA
	Current in Sleep mode@DRX=0.64S	-	1.1	-	mA
	Current in Sleep mode@DRX=1.28S	-	1	-	mA
	Current in Sleep mode@DRX=2.56S	-	0.9	-	mA
I _{VBAT (PSM)}	Current in PSM mode	-	6	-	uA
I _{VBAT (power-off)}	Module average consumption current (off leakage current)	-	5	-	uA

NOTE

Test condition: VBAT power supply 3.8V, the module is tested on EVB board, and the power input has a 200uF tantalum capacitor.

During PCB design, attention should be paid to the trace impedance of the VBAT power supply. When the module operates under high-power conditions with a large load current, voltage drop caused by trace impedance increases accordingly. Theoretical DC impedance can be estimated using a DC impedance simulation tool or the following formula:

$$R_{\text{trace}} = \rho \cdot \frac{L}{A} = \rho \cdot \frac{L}{W \cdot T}$$

R_{trace} : DC resistance of the trace (Ohm)

ρ : Resistivity of copper, approximately $1.68 \times 10^{-8} \Omega \cdot \text{m}$ at room temperature (increases with temperature)

L : Trace length (meters)

A : Cross-sectional area of the trace (square meters)

W : Trace width (meters)

T : Copper thickness (meters)

If there are vias along the PCB trace, their DC resistance must also be considered. When multiple vias are used, calculate the total resistance as parallel resistance. The DC resistance of a single via can be calculated using the following formula:

$$R_{\text{via}} = \rho \cdot \frac{L}{A} = \frac{4\rho L}{\pi (D_{\text{outer}}^2 - D_{\text{inner}}^2)}$$

R_{via} : DC resistance of the via (Ohm)

ρ : Resistivity of copper, approximately $1.68 \times 10^{-8} \Omega \cdot \text{m}$ at room temperature (increases with temperature)

L : Via depth (meters)

A : Cross-sectional area of the via (square meters)

D_{outer} : Outer diameter of the via (meters)

D_{inner} : Inner diameter of the via (meters)

NOTE

The resistivity of copper increases with temperature. Therefore, in high-temperature environments, the impedance of the VBAT power trace will be higher.

3.1.1. Power Supply Design Guide

In the customer's design, special attention must be paid to the design of the power supply. If the voltage drops below 3.3V, the RF performance of the module will be affected, the module will shut down if the voltage is too low. It is recommended to select an LDO or DC-DC chip with an enable pin, and the enable pin is controlled by the MCU.

NOTE

When the power supply can provide a continuous current of 1.2A, the total capacity of the external power supply capacitor is recommended to be no less than 200uF.

It is recommended to place four 10pF/33pF/0.1uF/1uF ceramic capacitors near VBAT to improve RF performance and system stability. At the same time, it is recommended that the VBAT layout routing width from the power supply on the PCB to the module be at least 2mm. The recommended reference design is as follows:

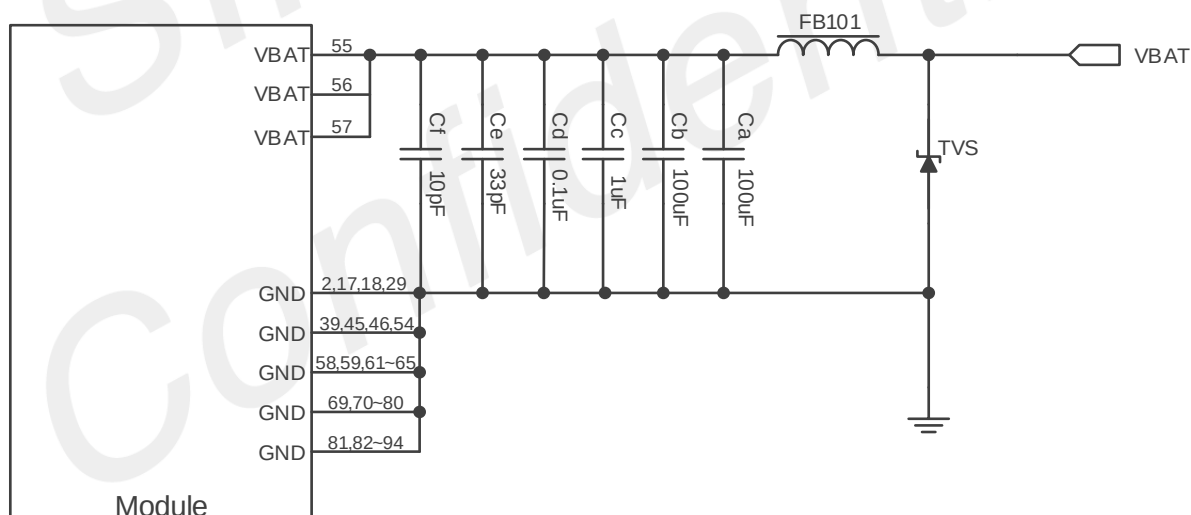


Figure 4: Power Supply Application Circuit

If the VBAT input contains high-frequency interference, it is recommended to add magnetic beads for filtering. The recommended types of magnetic beads are BLM21PG300SN1D and MPZ2012S221A.

In addition, in order to prevent the damage of A7671 caused by surge and overvoltage, it is recommended to parallel one TVS on the VBAT pin of the module.

Table 12: TVS for VBAT Part Number List

Manufacturer	Part Number	V_{RWM}	$V_{C(Max)}$	$P_{PP(Max)}$	$C_{J(Max)}$	Package
WILL	ESD56301D05-2/TR	5V	9.5V	1500W	700pF	DFN1610-2L
WILL	ESD56301D04-2/TR	4.85V	11V	2000W	480pF	DFN1610-2L
WAYON	WS2057KP	5V	12V	2040W	700pF	DFN1610-2L
WAYON	WS4.5DPHXM	4.85V	11V	2255W	700pF	DFN1610-2L

NOTE

When selecting TVS by customer, it is necessary to pay attention to the clamping voltage in the case of surge protection. The clamping voltage should not be higher than 10V when 100V surge input.

3.1.2. Recommended Power Supply Circuit

In order to avoid damaging the module, please do not cut off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

It is suggested that customer's design should have the ability to cut off the power supply for module in abnormal state, and then switch on the power supply to restart the module.

When the input power is greater than 5V, it is recommended to use DCDC chip. When the input is less than 5V, use the LDO power supply. If the OPEN LINUX secondary development function of the module is used, since there is no MCU, a low-cost MCU can be added to play the role of the hardware watchdog that can pull PWRKEY to start up and power off.

It is recommended that a switching mode power supply is used. The following figure shows the DC-DC regulator reference circuit:

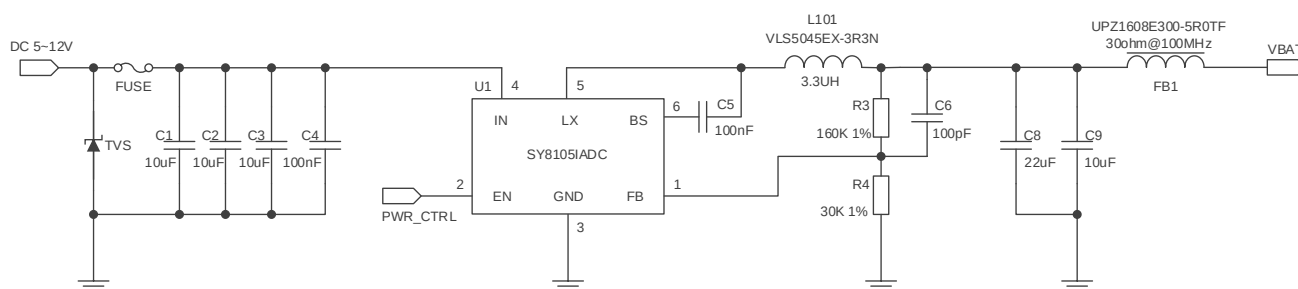


Figure 5: Power Supply Reference Circuit

When the VBAT power is turned off, the voltage should decrease rapidly within 50ms. To avoid voltage

anomalies, when the VBAT is lower than the minimum value, the system must power on the VBAT at a voltage which lower than 100mV for at least 2 second to restart the system.

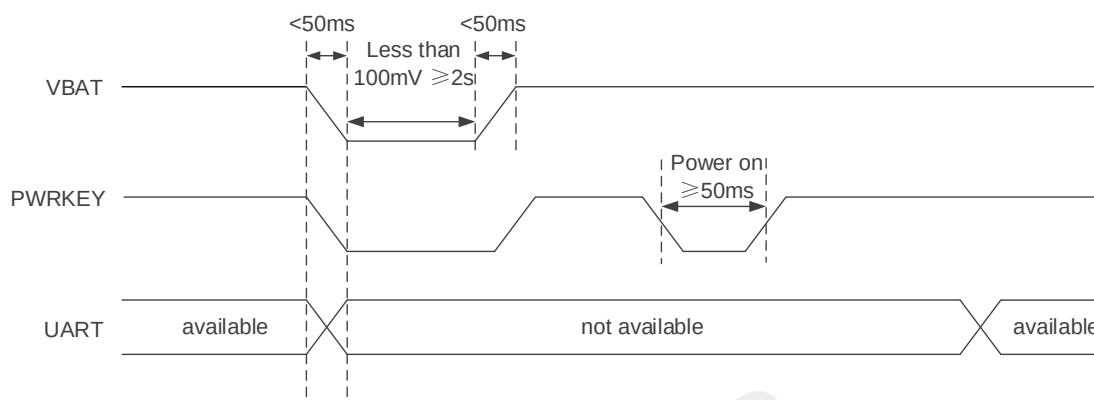


Figure 6: Power-off and Power-on Restart Sequence

3.1.3. Voltage Monitor

AT command 'AT+CBC' can be used to monitor VBAT voltage.

AT command 'AT+CVALARM' can be used to set high/low voltage alarm, when the actual voltage exceeds the preset range, a warning message will be reported through the AT port.

AT command 'AT+CPMVT' can be used to set high/low voltage power off, when the actual voltage exceeds the preset range, the module will shut down automatically.

NOTE

Overvoltage alarm and overvoltage shutdown are off by default. For details of AT commands, please refer to document [1].

3.2. Power On/ Off and Reset

3.2.1. Power On

Table 13: PWRKEY Interface Pin Definition

Pin Name	Pin No.	Type	Description	Note
PWRKEY	1	DI,PU	Power ON/OFF input, active low.	It has been internally pulled up to the VBAT with 50K (Typical).

Customer can power on the module by pulling down the PWRKEY pin. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is as follows:

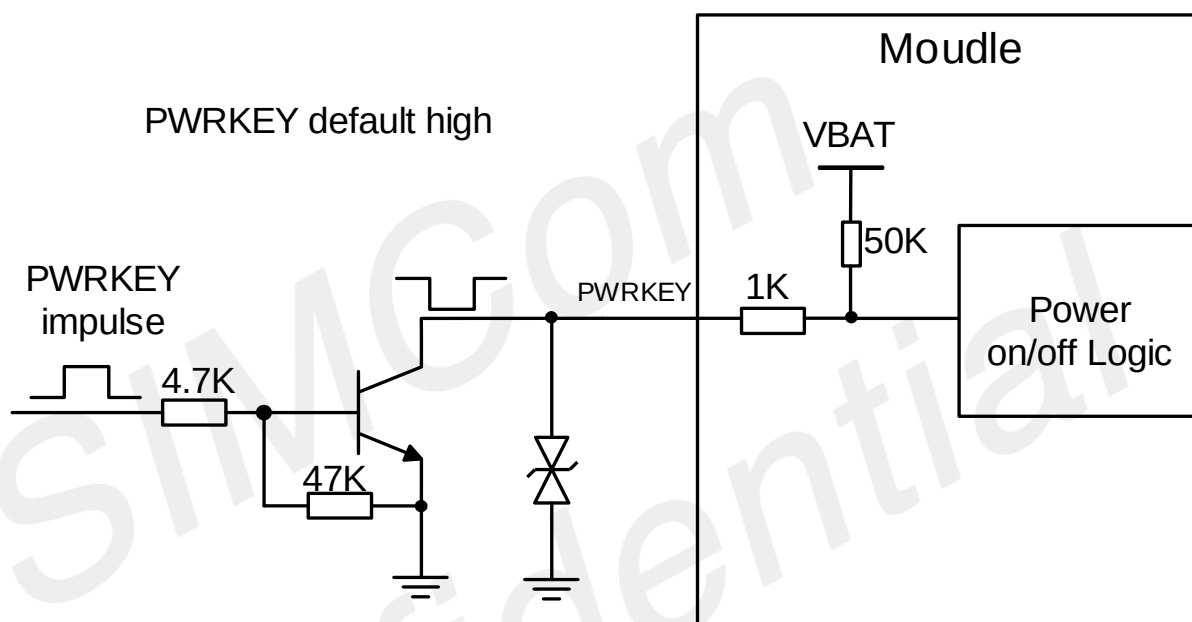


Figure 7: Reference Power on/off Circuit

NOTE

1. It is forbidden to pull down both RESET and PWRKEY to power on the module at the same time.
2. Do not connect a capacitor larger than 10pF on the PWRKEY and RESET. Otherwise, the module will start automatically if the low level is detected during the power-on.

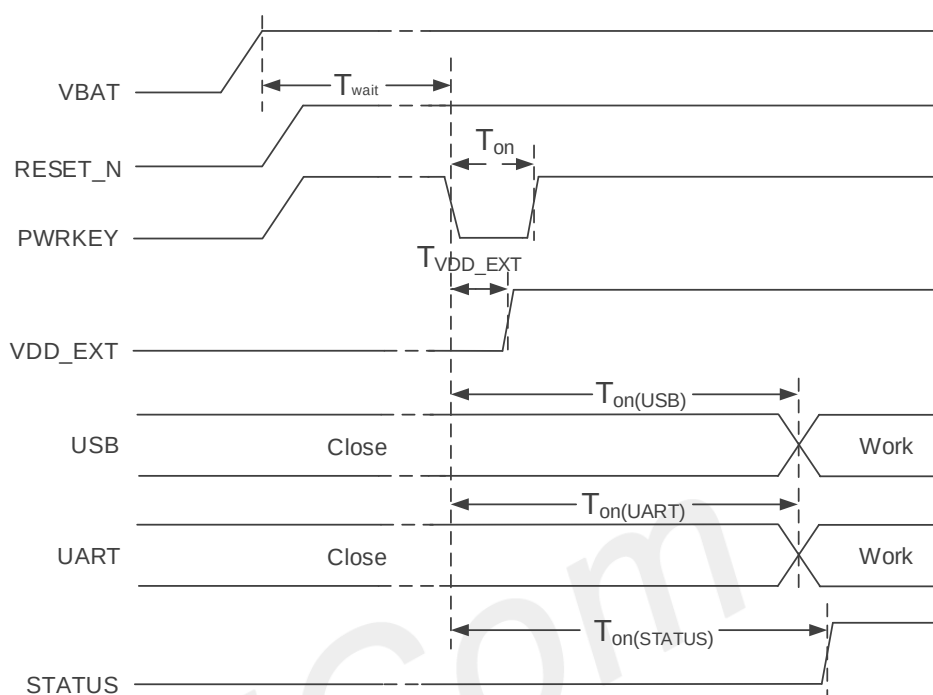


Figure 8: Power on Sequence

Table 14: Power on Timing and Electronic Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{on(wait)}$	The time from VBAT power-on stabilization to PWRKEY pin pull-down validity	40	-	-	ms
T_{on}	The time of active low-level impulse of PWRKEY pin to power on module	10	-	-	ms
$T_{on(vdd_ext)}$	Output time of VDD_EXT	-	9	-	ms
$T_{on(status)}$	The time from power-on issue to STATUS pin output high level (indicating power up ready)	-	-	9	s
$T_{on(uart)}$	The time from power-on issue to UART port ready	-	-	7	s
$T_{on(usb)}$	The time from power-on issue to USB port ready	-	-	7	s
V_{IH}	Input high level voltage on PWRKEY pin	$0.7 \cdot V_{BAT}$	-	V_{BAT}	V
V_{IL}	Input low level voltage on PWRKEY pin	0	0	$0.3 \cdot V_{DD_EXT}$	V

3.2.2. Power Off

The following methods can be used to power off the module.

- Power off by pulling the PWRKEY pin down to a low level for 2.5s.
- Power off Module by AT command 'AT+CPOF'.
- Over-voltage or under-voltage automatic power off, the voltage range can be set by 'AT+CPMVT'.

- Over-temperature or under-temperature automatic power off.

It is strongly recommended that the customer use PWRKEY or 'AT+CPOF' to shut down, and then cut off VBAT (especially when the module does not need to work). In addition, the customer cannot shut down VBAT by disconnecting it, which may cause damage to flash.

NOTE

When the temperature exceeds the range of $-30 \sim +75^{\circ}\text{C}$, A7671 will report warning information through AT port. When the temperature exceeds the range of $-40 \sim +85^{\circ}\text{C}$, A7671 will shut down automatically. For a detailed description of 'AT+CPOF' and 'AT+CPMVT', please refer to document [1].

PWRKEY can be used to power off the module. For power off sequence, please see the following figure:

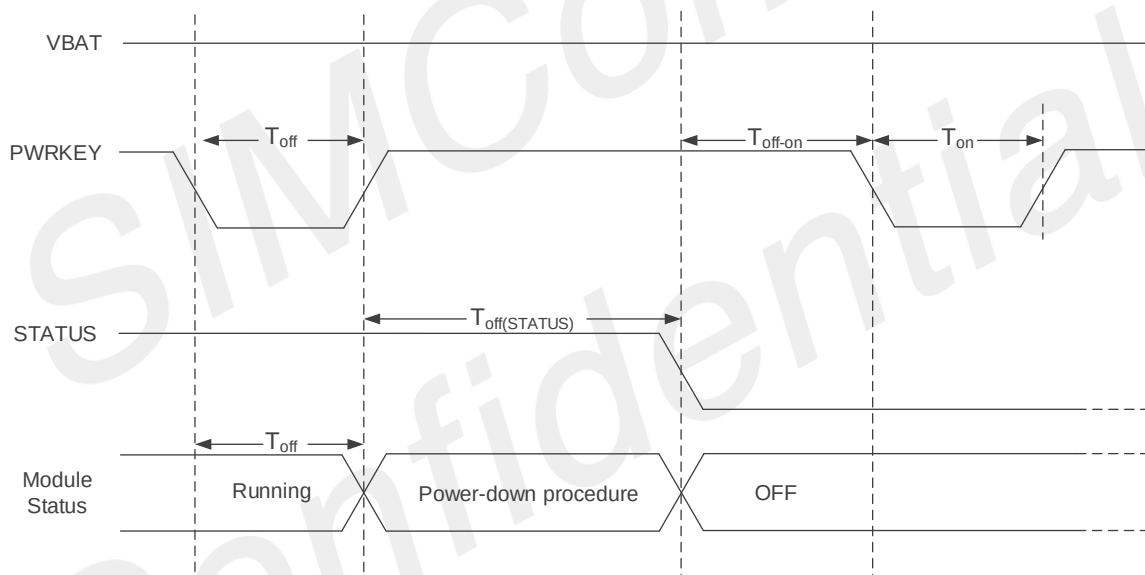


Figure 9: Power off Timing Sequence

Table 15: Power off Sequence Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{off}	Power off low level pulse width	2.5	-	-	s
$T_{\text{off(vdd_ext)}}$	VDD_EXT shutdown time	-	-	4	s
$T_{\text{off(status)}}$	Power off time (according to status interface)	-	-	4	s
$T_{\text{off-on}}$	Power off - power on buffer time	2	-	-	s

NOTE

The status pin can be used to judge whether the module is powered on or not. When the module is powered

on and initialization is completed, the status outputs a high level. Otherwise, the low level will be maintained all the time.

3.2.3. Reset

Table 16: RESET Interface Pin Definition

Pin Name	Pin No.	Type	Description	Note
RESET	16	DI,PU	System reset control input, active low.	It has been internally pulled up to the VBAT with 50K (Typical).

The module can be reset by pulling down the RESET pin to a low level. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is shown as follows:

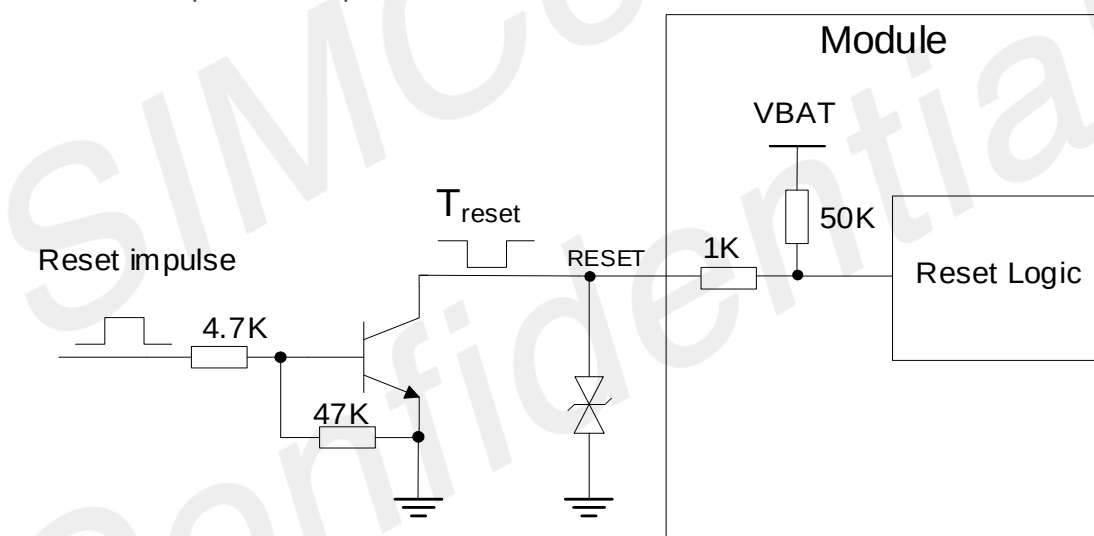


Figure 10: Reference Reset Circuit

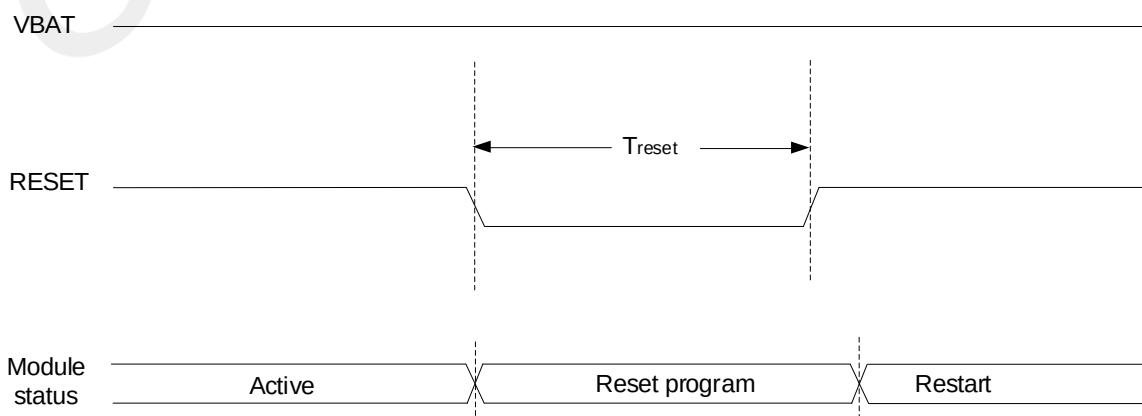


Figure 11: Reset Timing Sequence

Table 17: RESET Pin Electronic Characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RESET}	The active low level time impulse on RESET pin to reset module	2	2.5	-	s
V_{IH}	Input high level voltage	$0.7 \cdot V_{\text{BAT}}$	-	V_{BAT}	V
V_{IL}	Input low level voltage	0	0	0.5	V

NOTE

1. It is recommended to use the RESET pin only in case of emergency, such as the module is not responding. The reset time is recommended to be 2.5s.
2. Do not connect a capacitor larger than 10pF on the PWRKEY and RESET. Otherwise, the module will start automatically if the low level is detected during the power-on.

3.3. UART Interface

The module provides three serial ports, the main communication serial port is MAIN_UART, one ordinary serial port for peripherals communication, and the DEBUG_UART dedicate to print log. The module is a Data Communication Equipment (DCE).

Table 18: UART Information

Interface Type	Support Baud Rate (Bps)	Default Baud Rate (Bps)	Function Description
Full function UART	300 600 1200 2400 4800 9600 19200 38400 57600 115200 230400 460800 921600 1842000 and 3686400	115200	Data transmission and AT command transmission
Debug UART	115200	115200	Module partial log output
Two-wire UART	9600 115200 230400 921600	115200	Used to communicate with peripherals

Table 19: UART Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
Full Function UART Interface					
TXD	9	1.8V	DOH	Data output	If unused, keep it open.
RXD	10	1.8V	DI	Data input	

RTS	8	1.8V	DI	DTE request sent	Connect to the RTS of DTE. If unused, keep it open.
CTS	7	1.8V	DO	DTE clears sending	Connect to the CTS of DTE. If unused, keep it open.
DCD	5	1.8V	DO	Carrier detection	If unused, keep it open.
DTR	3	1.8V	DI	DTE Ready	
RI	4	1.8V	DO	Ringing indicator	
Debug UART					
DEBUG_TXD	23	1.8V	DOH	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DEBUG_RXD	22	1.8V	DI		
Two-Wire UART					
UART3_TXD	50	1.8V	DOH	Data output	Two-wire serial port
UART3_RXD	49	1.8V	DI	Data input	

NOTE

1. The UART3 baud rate is only set to adapt to GNSS baud rate if the module supported; otherwise the UART3 supported baud rate from 9600 to 3686400bps.
2. It is recommended that the baud rate of the serial port without the flow control function not exceed 921600.

3.3.1. UART Design Guide

When customer uses full-function serial port, please refer to the following connection mode:

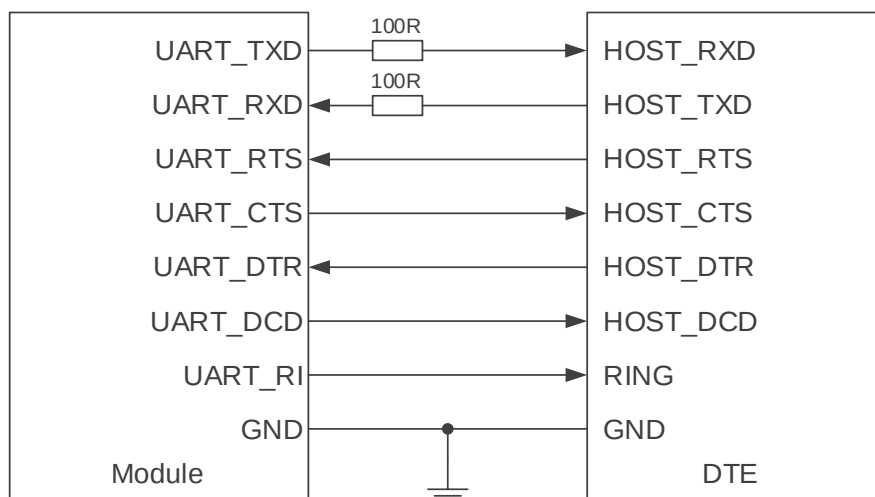


Figure 12: Serial Port Connection Diagram (Full-Function Mode)

When using 2-wire serial port, please refer to the following connection mode:

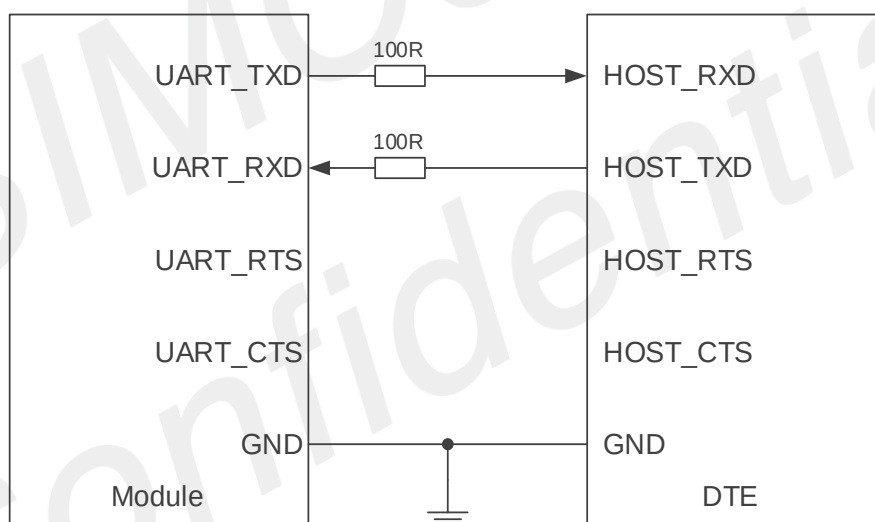


Figure 13: Serial Port Connection Diagram (NULL Mode)

When the module and the main control are connected using a level conversion chip (interface level mismatch), the reference design is shown in the following figure:



The recommended triode model is MMBT3904.



NOTE

1. The parasitic capacitance of the transistor will affect the edge of the high-speed digital signal. It is not recommended to use this circuit when the signal speed is higher than 115200bps.
2. It is recommended that the TXD and RXD are connected with 100R resistors in series on the module end to prevent damage to module pins caused by static electricity or surge.

3.3.2. RI and DTR Behavior

RI usually keeps high level output. When receiving a short message or URC report, RI outputs a low level for 120ms (short message)/60ms (URC), and then returns to a high-level state.

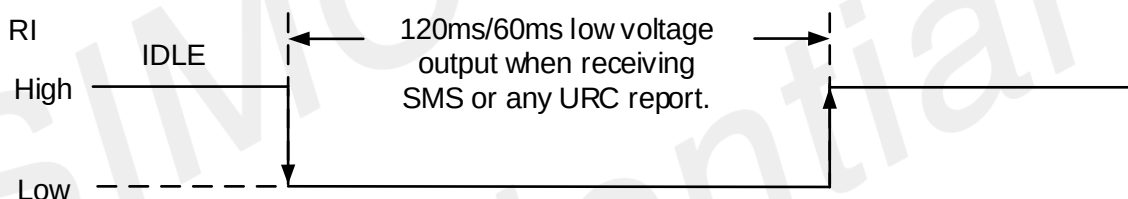


Figure 16: RI Behaviour (SMS and URC Report)

3.3.3. DTR Function Description

The DTR can be used as the sleep-wake pin of the module. After the module enters sleep mode, pull down the DTR to wake up the module. DTR defaults to high level.

When the customers set "AT+CSCLK=1", the module will automatically enter sleep mode. After entering sleep mode, the serial port function cannot communicate normally, and external pulling down the DTR can wake up the module.

After setting the AT command "AT+CSCLK=0", pulling the DTR pin to a high level will not have any effect, and the normal communication of the serial port function will not be affected.

3.4. USB Interface

The module contains a USB interface, which complies with the USB2.0 specification as a peripheral, but does not support USB charging function and USB HOST mode.

USB supports high speed mode (480Mbps) and full speed mode (12Mbps), it is used for AT command communication, data transmission, firmware upgrade and software debugging.

Table 20: USB Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
VBUS	24	-	PI	Valid USB detection input. Active high, $V_{min}=3.0V$, $V_{max}=5.2V$, $V_{norm}=5.0V$	
USB_DP	25	-	AIO	Positive electrode of the differential, bi-directional USB signal.	
USB_DN	26	-	AIO	Negative electrode of the differential, bi-directional USB signal.	

3.4.1. USB Reference Design

USB is the main debugging port and software upgrade interface. It is recommended that customers reserve USB test points for debugging during design. If a main control chip is connected, 0R resistors must be reserved for switching external test points during design. The recommended reference design is as follows:

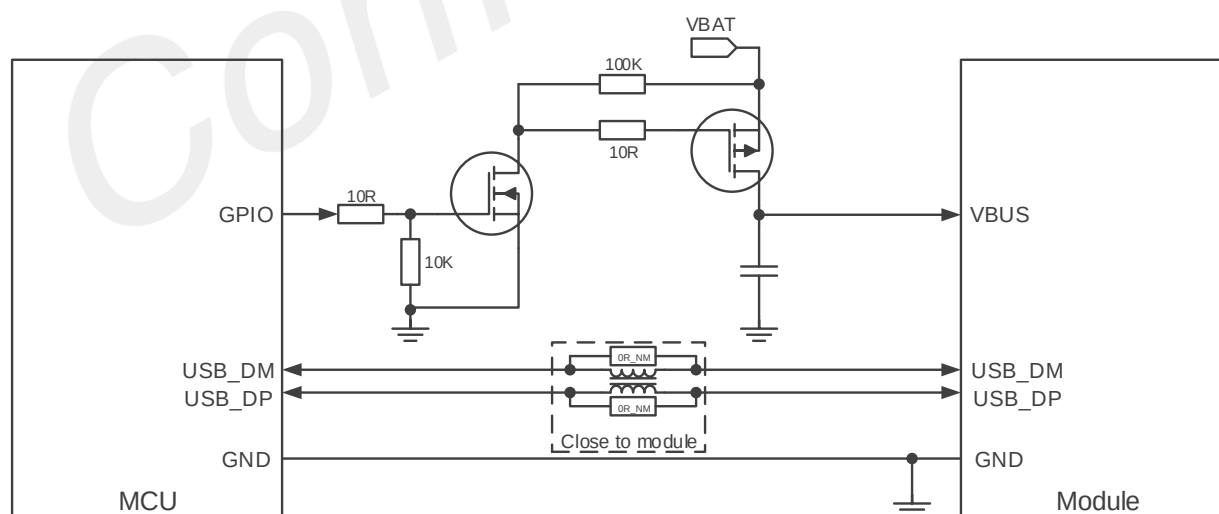


Figure 17: USB to MCU Circuit Diagram

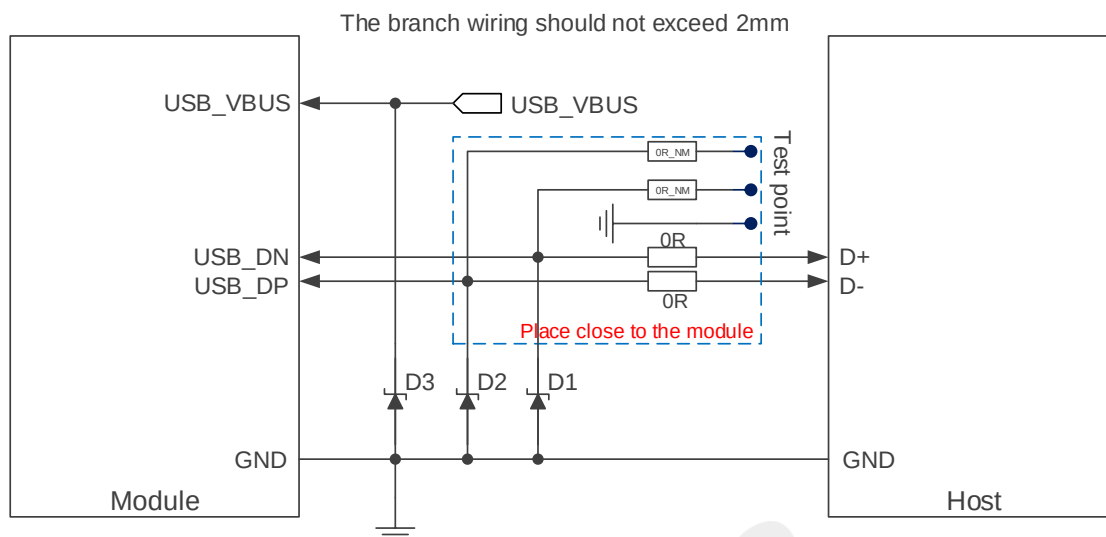


Figure 18: USB Circuit Diagram

Customers should pay attention to the selection of D3 devices when using, it is recommended to choose anti-static and anti-surge two-in-one devices, you can place a TVS tube. The parasitic capacitance of TVS(D1 and D2) on the USB data cable must be less than 1pF. The following table shows the recommended models.

USB_VBUS is the USB detection pin for module, it's active high and the available identification voltage is 3.0V~5.2V, generally recommend to connect to the VBUS signal of external USB connector or of MCU, it also can be connected to other power supplies, such as the VBAT. If the USB_VBUS pin is connected to the power supply, it's recommended to reserve a switch circuit to ensure that the power supply can be turned off then turn it on, that make USB enumerating afresh.

Table 21: TVS for USB_VBUS Part Number List

Manufacturer	Part Number	V_{RWM}	$V_{C(Max)}$	$C_{J(Max)}$	Package
WAYON	WS07DP	7V	20V	1000pF	DFN1610-2L
PRISEMI	PTVSHC2EN7VU	7V	24V	750pF	DFN1610-2L
BILLSEMI	BLE7V065B6U	7V	16V	500pF	DFN1610-2L
LRC	LTVS16H7.0T5G	7V	15V	750pF	DFN1610

Table 22: TVS for USB_DP, USB_DN Part Number List

Manufacturer	Part Number	V_{RWM}	$V_{C(Max)}$	$C_{J(Max)}$	Package
WILL	ESD9X5VU-2/TR	5V	8V	0.9pF	WBFBP-02C
LRC	LESD9L5.0T5G	5V	9.8V	0.9pF	SOD-923
WAYON	WE05DUCF	5V	14V	0.7pF	DFN1006-2L
ON	ESD9L5.0ST5G	5V	9.8V	0.9pF	SOD-923

NOTE

1. The USB data cable must be strictly routed in 90Ω differential. The TVS devices D1 and D2 on the data line must be selected with equivalent capacitance less than 1pF.
2. Route away from other sensitive signals (RF, audio, and XO).
3. The USB 2.0 speed detection is automatically determined through the USB protocol. Customer does not need to additionally pull up the DP. Otherwise, it may affect the USB enumeration of the module.

3.4.2. USB_BOOT Interface

The module provides one forced download boot interface 'USB_BOOT'.

Table 23: USB_BOOT Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
USB_BOOT	6	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	Please reserve 2 test points for debug. Do not pull down USB_BOOT during normal power on!

If the module fails to boot, customers can force upgrade through the USB_BOOT port.

Before the module is powered on, pull down the USB_BOOT pin to GND, then apply VBAT power to the module, and press RESET to enter the download mode. After entering the download mode, release USB_BOOT and remove the pull-down.

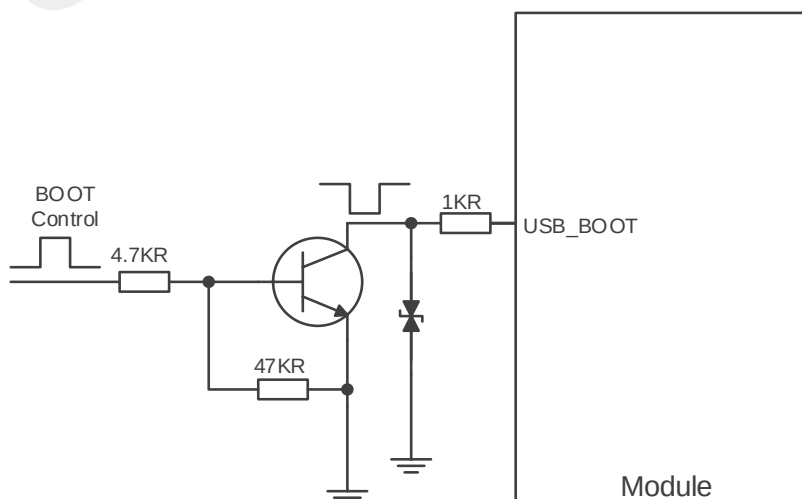
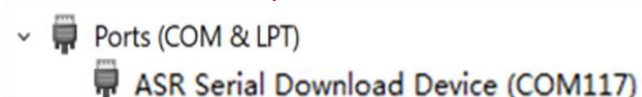


Figure 19: Reference USB_BOOT Circuit

Customers will see the download port in the device manager port of the windows system.

Force-download port:



The port after powering on normally:

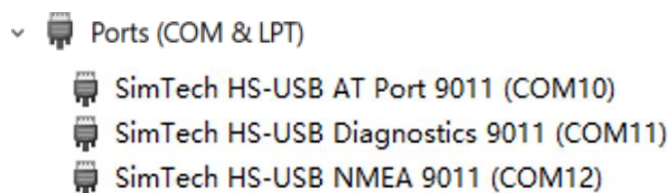


Figure 20: The USB Port

NOTE

1. USB_BOOT only has a forced download boot function before booting up (cannot be pulled down before normal use), and other functions after booting up.
2. When there is an MCU externally, the USB_BOOT signal needs to be connected to the MCU. USB_BOOT is controlled by the MCU to enable firmware upgrades even if the module firmware is damaged.
3. If there is no MCU outside, USB_BOOT test points must be reserved for easy debugging and upgrading.
4. The forced download mode requires firmware to be loaded from the USB interface, so if there is an MCU, the USB port must be connected to the MCU. If there is no MCU, the USB port must be connected to the USB interface or a reserved test point.

3.5. USIM Interface

The module supports both 1.8V and 3.0V USIM cards. The interface power of the USIM card is provided by the voltage regulator inside the module.

Table 24: USIM Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
USIM_DET	34	1.8V	DO	USIM card insert detect.	It can be set to high/low active with the AT command, refer to

					Document [18].
USIM_DATA	31	1.8/3.0V	DIO	USIM data signal.	This pin has been pulled up with 4.7KΩ resistor to USIM_VDD internally.
USIM_CLK	32	1.8/3.0V	DO	USIM clock signal.	
USIM_RST	33	1.8/3.0V	DO	USIM reset signal.	
USIM_VDD	30	1.8/3.0V	PO	USIM card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.

Table 25: USIM Electronic Characteristic in 1.8V Mode ($V_{USIM_VDD}=1.8V$)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{USIM_VDD}	LDO power output voltage	1.62	1.8	1.98	V
V_{IH}	High-level input voltage	$0.7 \cdot V_{USIM_VDD}$	-	$V_{USIM_VDD} + 0.4$	V
V_{IL}	Low-level input voltage	-0.4	0	$0.25 \cdot V_{USIM_VDD}$	V
V_{OH}	High-level output voltage	$V_{USIM_VDD} - 0.4$	-	V_{USIM_VDD}	V
V_{OL}	Low-level output voltage	0	0	0.2	V

Table 26: USIM Electronic Characteristic in 3.0V Mode ($V_{USIM_VDD}=3.0V$)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{USIM_VDD}	LDO power output voltage	2.7	3.0	3.3	V
V_{IH}	High-level input voltage	$0.7 \cdot V_{USIM_VDD}$	-	$V_{USIM_VDD} + 0.4$	V
V_{IL}	Low-level input voltage	-0.4	0	$0.25 \cdot V_{USIM_VDD}$	V
V_{OH}	High-level output voltage	$V_{USIM_VDD} - 0.45$	-	V_{USIM_VDD}	V
V_{OL}	Low-level output voltage	0	0	0.3	V

3.5.1. USIM Hot Swap Function

The USIM card supports the hot swap function. You can use AT+UIMHOTSWAPON=1 to turn on the hot swap detection function.

If the USIM card holder is of the normally open type, the AT command “AT+UIMHOTSWAPLEVEL=0” can be sent to set the detection level to a low level, when USIM_DET is pulled down, the USIM card is considered inserted.

If the USIM card holder is of the normally closed type, the AT command “AT+UIMHOTSWAPLEVEL=1” can be sent to set the detection level to a high level, when USIM_DET is pulled up, it is considered that the USIM card is inserted.

For more detailed information on USIM card AT operation, please refer to the document [1]. If the USIM card hot swap function is not used, the customer can maintain the USIM_DET pin is disconnected.

3.5.2. USIM Application Guide

It is recommended to use ESD protection component. Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

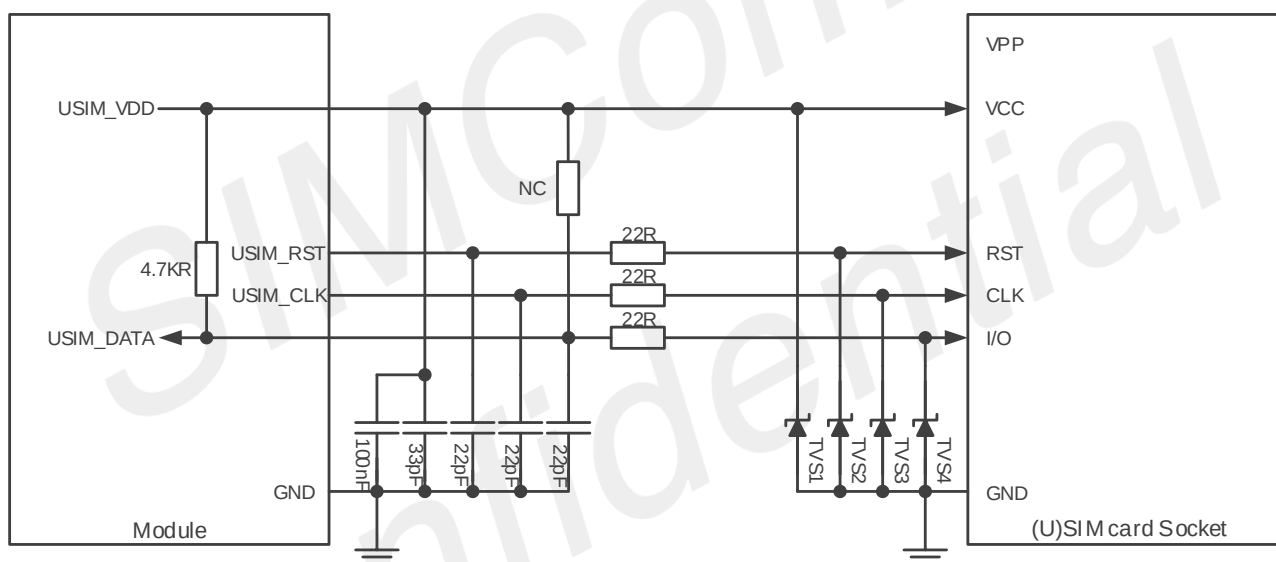


Figure 21: USIM Interface Reference Circuit

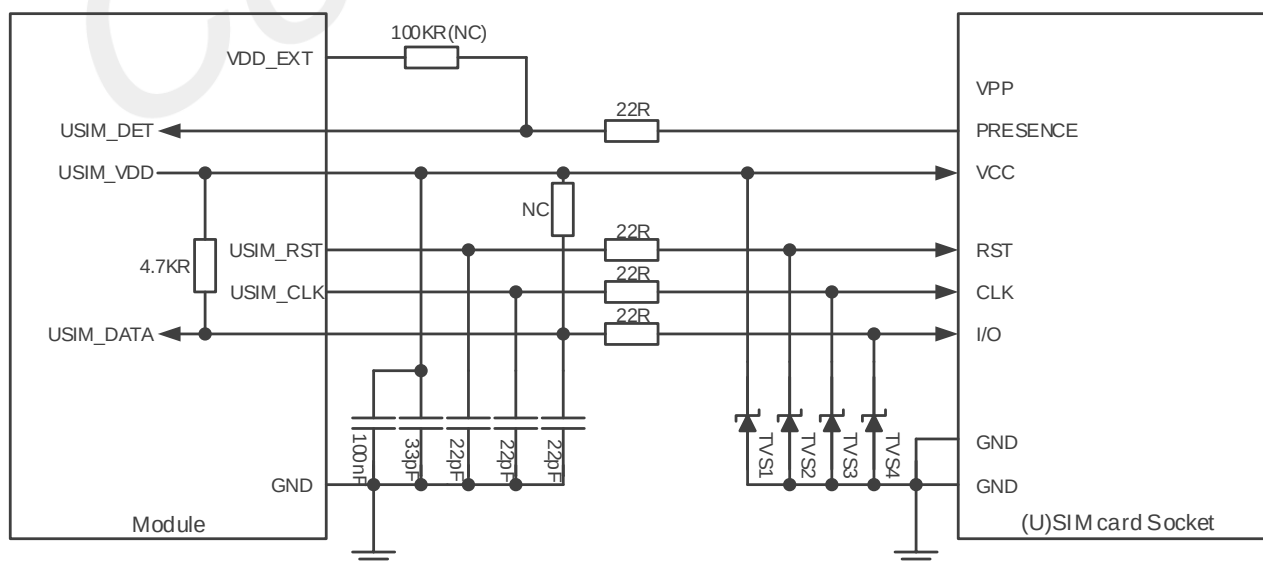


Figure 22: USIM Interface Reference Circuit (8PIN)

NOTE

1. USIM_DATA has been pulled up with a 4.7K Ω resistor to USIM_VDD in module.
2. A 100nF capacitor on USIM_VDD is used to reduce interference.
3. For more details of AT commands about USIM, please refer to document [1].

The circuit of the USIM card is easy to be interfered with, resulting in the failure to recognize or drop the card, etc. so please follow the following principles during the design:

- Be sure to keep the USIM socket away from the main antenna during the PCB layout phase.
- USIM card traces should be away from RF, VBAT and high speed signals, at the same time the USIM card traces should be as short as possible.
- Keep the USIM socket's GND pin directly connected to the main ground.
- To prevent USIM_CLK from other signal interference, it is suggested to make separate package to protect USIM_CLK processing.
- Place TVS near the USIM socket, and the parasitic capacitance of TVS should not be greater than 15pF, such as WS03DTUMS-B.
- Connect 22 Ω resistors in series between USIM socket and module can enhance ESD protection performance.
- The rise/fall time of USIM_CLK should not exceed 40ns.

Table 27: TVS for USIM Socket Part Number List

Manufacturer	Part Number	V _{RWM}	V _{C(Max)}	P _{PP(Max)}	C _{J(Max)}	Package
WAYON	WS03DTUMS-B	3.3V	8V	35W	0.7pF	DFN0603-2L
WILL	ESD9X5VU-2/TR	5V	8V	72W	0.9pF	DFN1006-2L

3.6. SPI Interface (Need to Customize Software)

The module provides a set of 4 wire SPI interface with maximum clock rate of 52MHz. It supports master mode and provides full-duplex format, synchronous and serial communication with peripheral devices.

Table 28: SPI Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
SPI_CLK	11	1.8V	DO	SPI clock	If unused, keep it open.
SPI_CS	12	1.8V	DO	SPI chip select signal	
SPI_MISO	14	1.8V	DI	SPI master input slave output	
SPI_MOSI	13	1.8V	DO	SPI master output slave input	

The recommended reference design is as follows:

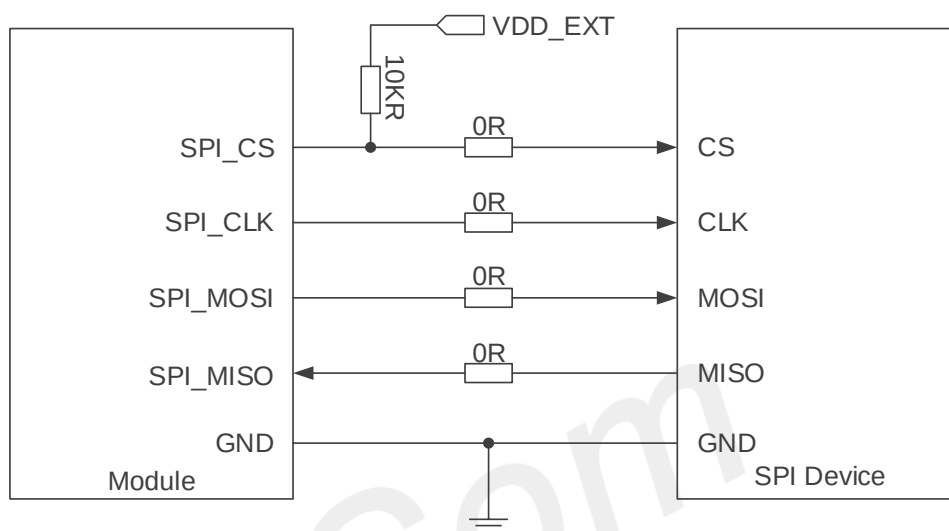


Figure 23: SPI Reference Circuit

3.7. Audio Interface (Need to Customize Software)

The module provides an analog audio output interface, which can be connected to an external speaker for multimedia playback.

Table 29: Analog Audio Output Interface Definition

Pin Name	No.	Power Domain	Type	Description	Note
SPK_P	40	-	AO	Analog audio output channel (+)	Do not connect SPK_P to GND.
SPK_N	41	-	AO	Analog audio output channel (-)	

The recommended reference design is as follows:

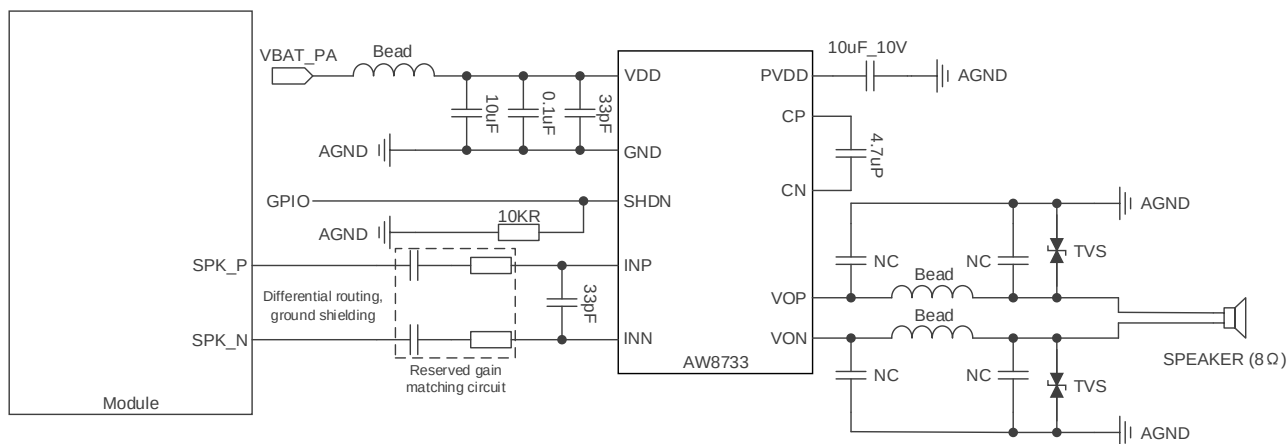


Figure 24: Analog Audio Reference Circuit

NOTE

The A7671X-MNXY/LNXY do not support Audio function.

3.8. I2C Interface

The module provides one I2C interface, which supports standard speed clock frequency 100Kbps and high speed clock frequency 400Kbps. Its operation voltage is 1.8V.

Table 30: I2C Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
I2C_SCL	38	1.8V	OD	I2C clock output	If unused, keep it open. Need to pull up to VDD_EXT.
I2C_SDA	37	1.8V	OD	I2C data I/O	

The recommended reference design is as follows:

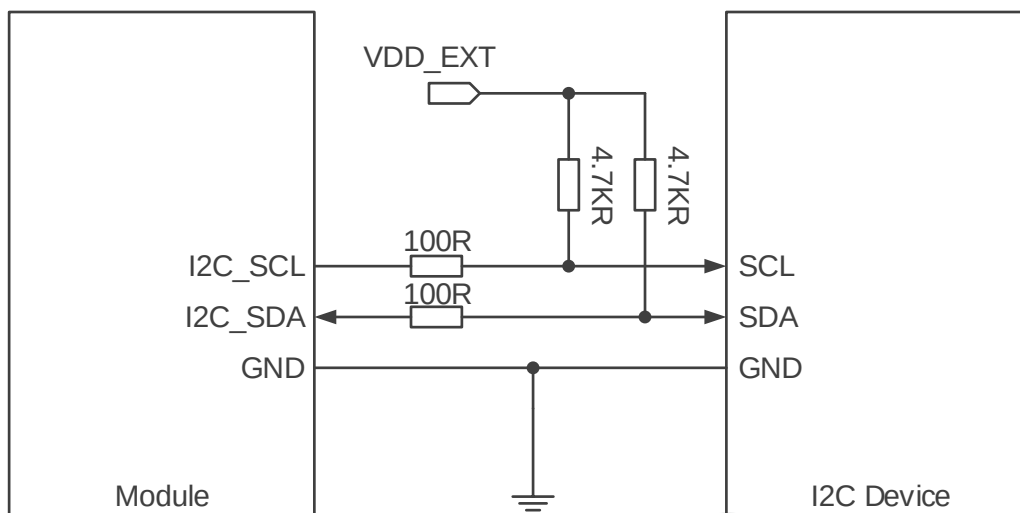


Figure 25: I2C Reference Circuit

NOTE

1. The SCL and SDA pins require pull-up resistors, and the pull-up power supply must be VDD_EXT of the module output.
2. Connecting a 100R resistor in series with the I2C signal line close to the module terminal is recommended to reduce overshoot on the signal line.

3.9. LCD Interface (Need to Customize Software)

Module supports LCD interface, only support the LCD module with 1 data line, the LCD interface of the module has no special LCD_TE signal pin, if necessary, you can choose GPIO to simulate the use.

It is recommended that the voltage stabilizer capacitor and decoupling capacitor be reserved on the LCD power supply line, and the 0Ω resistance in series be reserved for commissioning. At the same time, the data line is also reserved in series 0Ω resistance to facilitate the adjustment of signal quality, to prevent signal reflection, overshoot and other phenomena.

Table 31: LCD Interface Description

Pin Name	Pin No	Reserved Function	I/O	Description	Note
GPIO16	101	LCD_BL_PWM	DO	LCD back light PWM adjustment	
GPIO17	102	LCD_SPI_CLK	DO	LCD special SPI clock	
GPIO18	103	LCD_SPI_TXD	DIO	LCD special SPI data cable	

GPIO20	105	LCD_SPI_CS	DO	LCD special SPI chip selection
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NOTE

1. LCD function need to customize software.
2. If customer need RESET/DCX/LEDK function, please use PIN106 as LCD_RST(LCD reset), use PIN107 as LCD_DCX(LCD special SPI data cable), and use PIN126 as LEDK(LCD backlight SINK adjustment).
3. Do not use PIN106 and PIN47 simultaneously, do not use PIN107 and PIN48 simultaneously.
4. Module supports LCD backlight SINK adjustment. As a current sink pin, it can be directly connected to the LEDK pin of LCD, and the backlight can be adjusted by configuring the SINK through SW. The sink current range is 3mA~96mA, step=3mA, and the peripheral MOS tube drive circuit can be omitted. Due to chip space limitations, it is necessary to cut some other functions to implement this function, if you need it, please contact the SIMCom support team.

The recommended reference design is as follows:

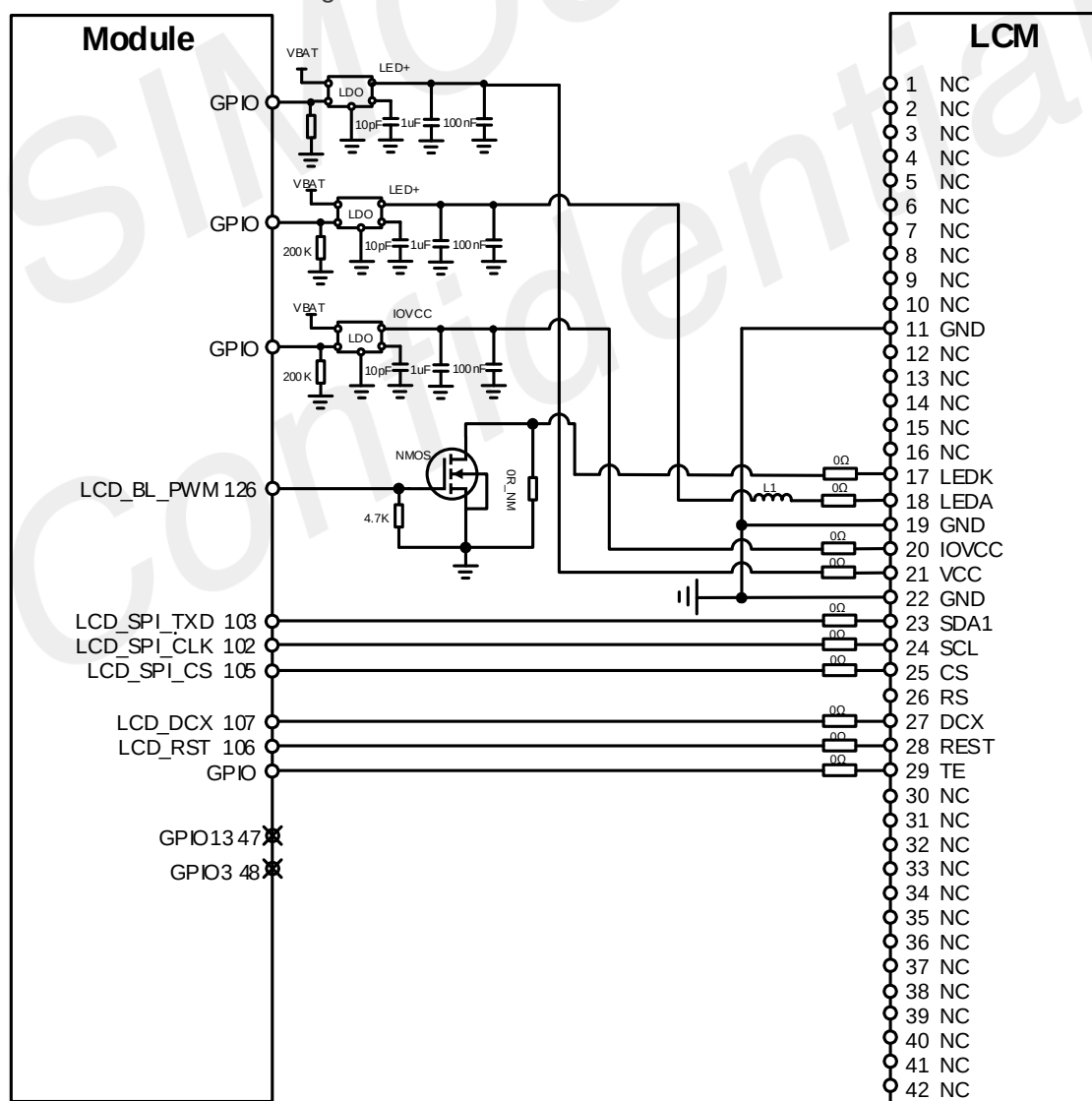


Figure 26: LCD Reference Circuit

3.10. GPIO Interface

The module provides multiple GPIOs.

Table 32: Standard GPIO Resources of A7671

Pin No.	Default Function	Power Domain	Pin Type.	Alter Function1	Alter Function2	Pad Edge Wakeup
6	USB_BOOT	1.8V	PU	GPIO_02		YES
11	GPIO5	1.8V	PD	GPIO_34	SPI_CS	YES
12	GPIO6	1.8V	PD	GPIO_35	SPI_CLK	YES
13	GPIO7	1.8V	PD	GPIO_36	SPI_MOSI	YES
14	GPIO8	1.8V	PD	GPIO_37	SPI_MISO	YES
19	GPIO1	1.8V	PD	GPIO_05	32k_out	YES
21	GPIO9	1.8V	PD	GPIO_07	USIM2_RST	YES
26	GPIO2	1.8V	PD	GPIO_17	SMART_BAT	YES
35	GPIO10	1.8V	PU	GPIO_13	I2C2_SDA	YES
36	GPIO11	1.8V	PU	GPIO_14	I2C2_SCL	YES
44	GPIO12	1.8V	PD	GPIO_15	VCXO_OUT	YES
47	GPIO13	1.8V	PD	GPIO_16		YES
48	GPIO3	1.8V	PU	GPIO_08		YES
53	GPIO4	1.8V	PU	GPIO_18		YES
67	GPIO14	1.8V	PD	GPIO_11	VCXO_REQ	YES
68	GPIO15	1.8V	PD	GPIO_12	USIM2_DATA	YES
101	GPIO16	1.8V	PD	GPIO_19	PWM3	YES
102	GPIO17	1.8V	PD	GPIO_20	SPI2_CLK	YES
103	GPIO18	1.8V	PU	GPIO_21	SPI2_MOSI	YES
104	GPIO19	1.8V	PU	GPIO_22	SPI2_MISO	YES
105	GPIO20	1.8V	PD	GPIO_23	SPI2_CS	YES

3.11. STATUS Interface

The STATUS pin can be used to determine whether the module is powered on or not. When the module is powered on and initialization is complete, the status output is high. Otherwise, it will remain low.

Table 33: STATUS Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
STATUS	66	1.8V	DO	Module operation status indication	If unused, keep it open.

The recommended reference design is as follows:

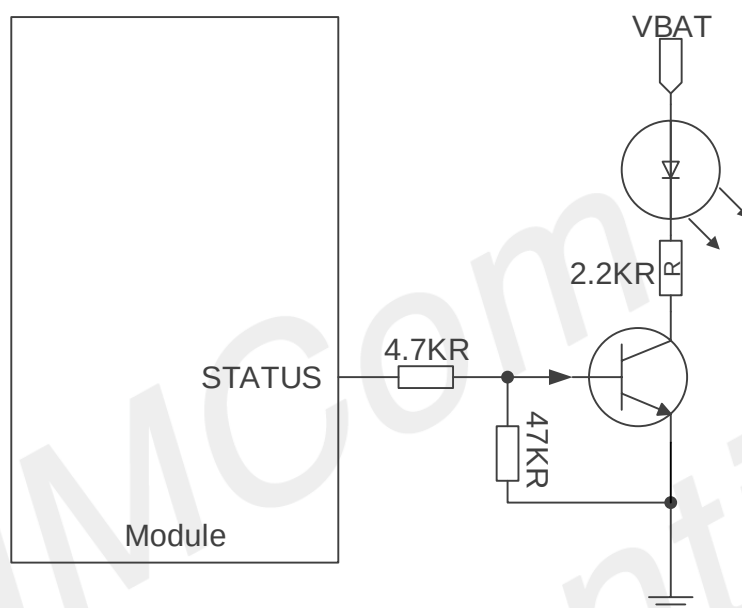


Figure 27: STATUS Reference Circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

3.12. NETLIGHT Interface

NETLIGHT can indicate the current network status. It is usually used to drive the LED light indicating the network status.

Table 34: NETLIGHT Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
NETLIGHT	52	1.8V	DO	Network registration status indicator (LED).	

The recommended reference design is as follows:

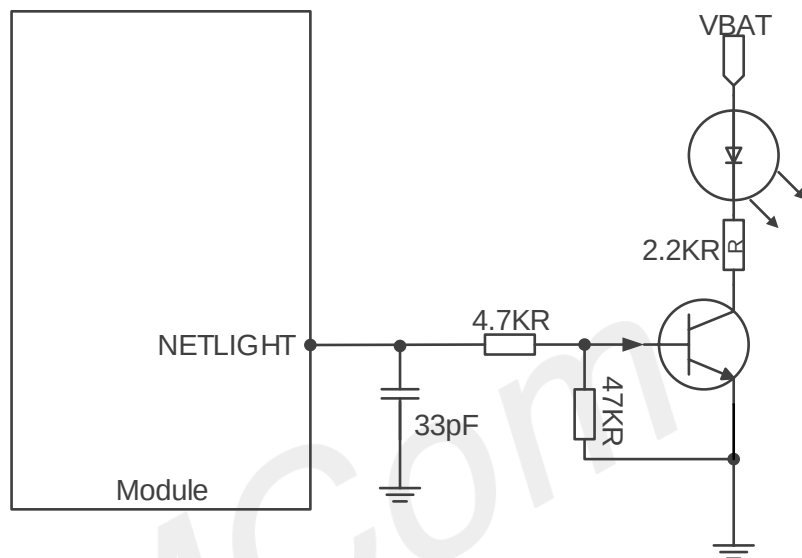


Figure 28: NETLIGHT Reference Circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

The NETLIGHT signal is used to control the LED light that indicates the status of the network. The working status of this pin is shown in the table below.

Table 35: LTE Mode NETLIGHT Pin Status

NETLIGHT Pin Status	Module Status
Always On	Searching Network
200ms ON, 200ms OFF	Data Transmit/Registered
OFF	Power off / Sleep

3.13. GNSS Interface

The module supports GNSS function interface. GNSS provides 2 power supply input interfaces, 1 GNSS power enable control switch, 1 reset interface, 1 debug interface, 1 UART interface and 1 pulse synchronous clock signal interface, which are described in detail as follows.

Table 36: GNSS Interface Pin Definition

Pin Name	Pin No	I/O	Description	Note
GNSS_VBKP	116	PI	GNSS backup power input	Power supply ranges from 1.62V to 3.6V, suggest 2.8V power supply. Cannot be open. Do not add resistor in series when the voltage bellow 2.0V.
VDD_GNSS	97	PI	GNSS main power input	The power supply voltage must be no less than 1.75V and no more than 1.9V, typically 1.8V. The cable must be as short as possible, with a cable width of more than 0.3mm.
GNSS_PWRCTL	98	PI	GNSS VCORE、VDDIO power enable control	Active high. Solution 1: Use 10K resistor in series to connect to GPIO2 (PIN20). Solution 2: Use 10K resistor in series to connect to MCU GPIO.
GNSS_RXD	96	DI	GNSS UART RXD	1.8V power domain. Solution 1: Use 1K resistor in series to connect AUX_UART_TXD (PIN50) of the module. Solution 2: Use 1K resistor in series to connect to MCU UART_TXD.
GNSS_TXD	95	DO	GNSS UART TXD	1.8V power domain. Solution 1: Use 1K resistor in series to connect AUX_UART_RXD (PIN49) of the module. Solution 2: Use 1K resistor in series to connect to MCU UART_RXD.
GNSS_RST_N	127	AI	GNSS RST interface	Internal pull up, active low.
1PPS◆	100	DO	GNSS pulse synchronous clock signal	Seconds pulse signal, do not pull up before starting GNSS. It can be used for accurate timing. Output pulse signal approximately 6 seconds after successful positioning. If unused, keep it open.
GNSS_ANT	90	AI	GNSS antenna	Refer to section 4.3

GNSS recommended reference design solution 1:

A7671 module itself provides power, power enable and UART transmission to GNSS.

The recommended reference design is as follows:

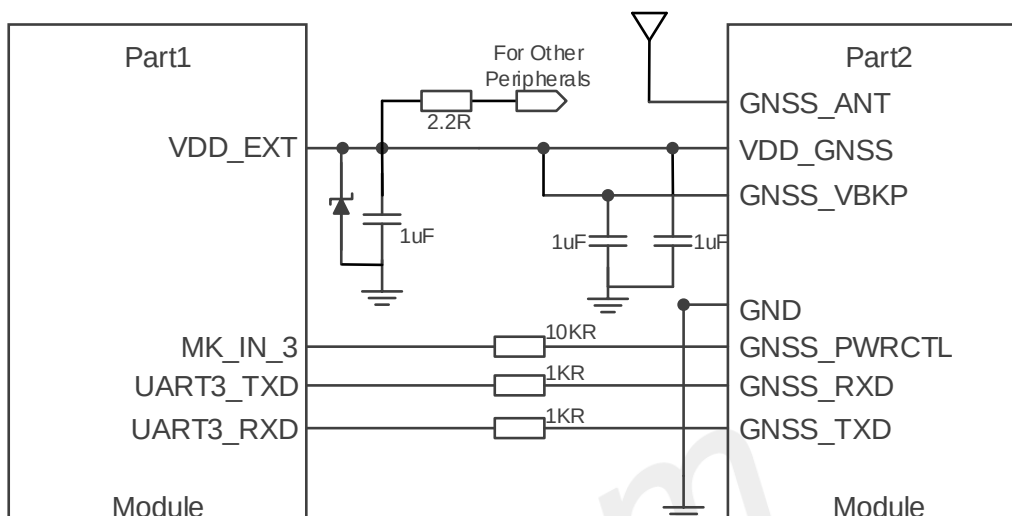


Figure 29: GNSS Reference Design (Non-Standalone GNSS Solution)

GNSS recommended reference design solution 2:

The external MCU provides power, power enable and UART transmission to GNSS, this solution is used for scenarios where GNSS can work standalone without the module powering up. The recommended reference design is as follows:

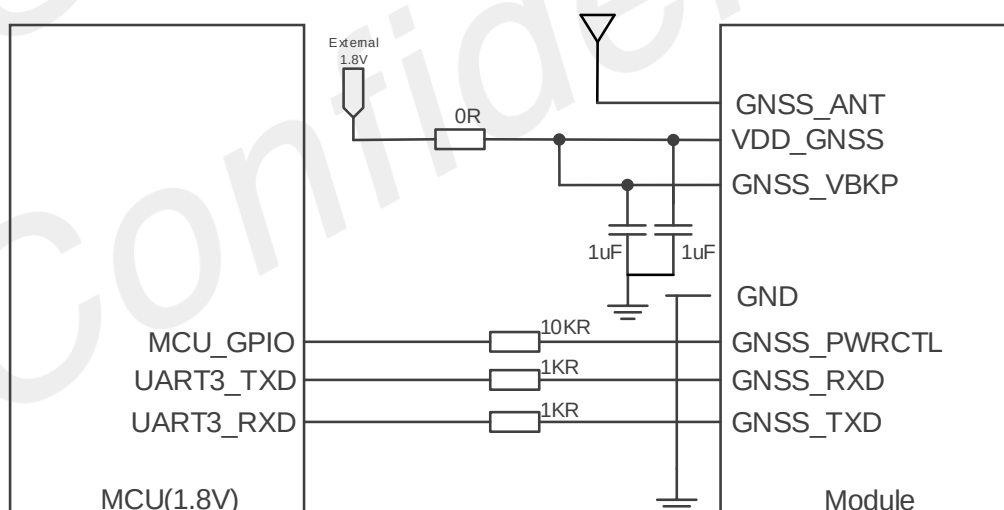


Figure 30: GNSS Reference Design (Standalone GNSS Solution)

NOTE

1. It is recommended to connect a 1K resistor in series on the GNSS serial communication line to prevent leakage of serial IO.
2. GNSS_VBKP backup power is a necessary condition for hardware normal startup, which can ensure that the performance indicators of GNSS fast startup reach the optimal state. When using VDD_EXT of

the module as GNSS backup power, module shutdown will cause VDD_EXT to power down, which cannot guarantee fast startup performance; If the customer needs to shut down the module and achieve fast startup at the same time, it is recommended to use an external constant power supply to power GNSS_VBKP.

3. GNSS_VBKP must be powered on, and it is required to be powered on before GNSS_PWRCTL. When using a 2.8V power supply, the current of GNSS_VBKP is approximately 43uA.
4. It is forbidden to pull up the 1PPS pin before powering on the GNSS, otherwise the GNSS cannot enter normal working mode.

AT commands about GNSS are as following table.

Table 37: AT Commands about GNSS

AT Command	Description
AT+CGNSSPWR=<n>	GNSS state control. <n>=1: Active GNSS. <n>=0: Close GNSS.
AT+CGNSSTST=<n>	Send data received from UART to NMEA port. <n>=1: Start sending data to NMEA port. <n>=0: Stop sending data to NMEA port.
AT+CGPSCOLD	Cold start GNSS.
AT+CGPSWARM	Warm start GNSS.
AT+CGPSHOT	Hot start GNSS.
AT+CGNSSSLEEP=<n>	<n>=0: Set GNSS into sleep mode. <n>=1: Set GNSS exit sleep mode.
AT+CGNSSFLP=<n>	<n>=0: Disable Periodic Power Saving Mode. <n>=1: Enable Periodic Power Saving Mode.
AT+CGNSSGLP=<n>	<n>=0: Set GNSS quit low-power GLP mode. <n>=1: Set GNSS into low-power GLP mode.
AT+CGNSSFITNESS=<n>	<n>=0: Set GNSS into normal mode. <n>=1: Set GNSS into fitness mode.
AT+CGNSSALP=<n>	<n>=0: Disable both adaptive low-power power saving mode and adaptive low-power performance mode. <n>=1: Enable adaptive low-power power saving mode which might sacrifice GNSS performance in favour of a reduced power consumption. <n>=2: Enable adaptive low-power performance mode which achieves relatively good performance while keeping the power consumption low.
AT+CGNSSRTC=<n>	<n>=0: Enter RTC mode and only use external wake-up.

NOTE

For more AT commands about GNSS, please refer to document [1].

3.14. Other Interface

3.14.1. ADC

The module has two general ADC pins. Built-in VBAT ADC interface.

Table 38: ADC Interface Pins Definition

Pin Name	No.	Power Domain	Type	Description	Note
ADC1	25	0V-1.2V	AI	General Purpose ADC	If unused, keep it open.
ADC2	132	0V-1.2V	AI	General Purpose ADC	

Table 39: General ADC Electronic Characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	-	12	-	Bits
Input Range	0	-	1.2	V
Input Resistance		Hi-Z		

When using the built-in VBAT ADC, attention should be paid to the voltage drop caused by the trace impedance of the VBAT power supply. The load current should be determined based on the module's peak current. The following table lists the relationship between voltage drop and VBAT trace parameters under corresponding peak currents. PCB design should be adjusted accordingly to meet the VBAT ADC accuracy requirements.

Table 40: Recommended VBAT Routing Parameters and Impedance Quick Reference Table (Room Temperature)

Trace Length (mm)	Trace Width (mm)	Copper Thickness (oz)	Trace Impedance(mΩ)	Load Current (A)	Voltage Drop (mV)
50	1.5	1	16	0.7	11.2
50	2	1	12	1	12
50	3	1	8	2	16

In addition, to improve ADC sampling accuracy, the following PCB design guidelines should be followed:

- Keep the ADC input signal traces as short as possible to reduce signal attenuation.
- Route away from high-frequency clock circuits, RF circuits, and DC-DC circuits to minimize

interference.

- Avoid running parallel to other power or analog signal traces, especially on adjacent layers.
- Ensure complete signal isolation along the entire ADC trace path, with solid ground shielding on both the same and adjacent layers.
- Place ground vias evenly on both sides of the ADC traces to reduce signal interference.
- Keep ADC circuitry and routing away from high-power heat-generating components to minimize temperature impact on sampling accuracy.

NOTE

1. "AT+CADC=2" can be used to read the voltage of the ADC1 pin.
2. "AT+CADC2=2" can be used to read the voltage of the ADC2 pin.
3. "AT+CBC" can be used to read the voltage of the VBAT.
4. For more details, please refer to document [1].

3.14.2. LDO

The module provides 2 LDO outputs: VDD_EXT and VDD_AUX.

VDD_EXT is the system IO power supply for the module, with a default output voltage of 1.8V. It can only provide a current capacity of 50mA and cannot be used as a high current drive source.

VDD_AUX is the LDO output power supply for the module, with a fixed output voltage of 3V. It can only provide a current capacity of 50mA and cannot be used as a high current drive source; It can provide power for other peripherals such as active antennas and LCDs.

Table 41: LDO Interface Pin Definition

Pin Name	No.	Type	Description	Note
VDD_EXT	15	PO	System IO power	Default on. If unused, keep it open.
VDD_AUX	99	PO	Internal LDO power	Default on. If unused, keep it open.

Table 42: VDD_EXT Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V _{DD_EXT}	Output voltage	-	1.8	-	V
I _O	Output current	-	-	50	mA

The recommended reference design is as follows:

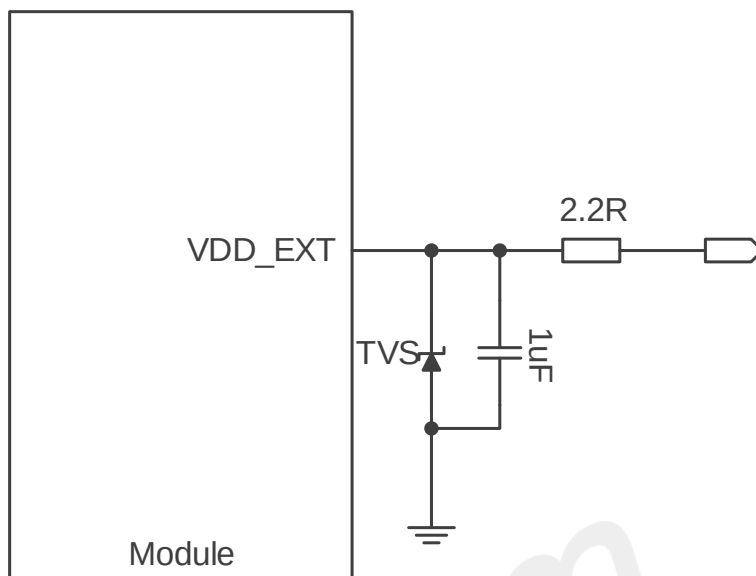


Figure 31: VDD_EXT Reference Circuit

NOTE

1. It is recommended to parallel a TVS protection tube near the VDD_EXT pin of the module for ESD protection. The recommended models are shown in the table below.
2. It is recommended to connect a 2.2R resistor in series near the VDD_EXT pin of the module for surge absorption. Due to the voltage drop caused by this resistor, if the current flowing through VDD_EXT is large, the resistance value of this resistor should be appropriately reduced.

Table 43: TVS for VDD_EXT Part Number List

Manufacturer	Part Number	V_{RWM}	$V_{C(Max)}$	$C_{J(Max)}$	Package
WILLSEMI	ESD56051N-2/TR	3.3V	10V	65F	DFN1006-2L

Table 44: VDD_AUX Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{AUX}	Output voltage	-	3.0	-	V
I_{AUX}	Output current	-	-	50	mA

NOTE

1. VDD_AUX is a fixed voltage output with an output of 3.00V,
2. VDD_AUX can control the switch state through the command "AT+CVAUXD=(0,1)".

3.14.3. PON

The module provides a PON interface, which is used to control the module to trigger automatic power on when the battery is inserted. When the PON is pulled up to VBAT and the battery is inserted, power is supplied to VBAT, and the module will automatically power on. Unlike short circuiting PWRKEY to ground to achieve automatic power on, PON only has the power on function when the battery is inserted for the first time to supply power to VBAT. After power on, it shuts down and the PON is in a pull-up state, which will not allow the module to power on again. When using this pin, it is recommended to pull up to VBAT through a 100K resistor.

Table 45: PON Interface Pin Definition

Pin Name	No.	Power Domain	Type	Description	Note
PON	134	VBAT	DI	Automatic power on control pin. If the module needs to be powered on automatically, it is recommended to pull it up to VBAT through a 100K resistor.	If unused, keep it open.

The recommended reference design is as follows:

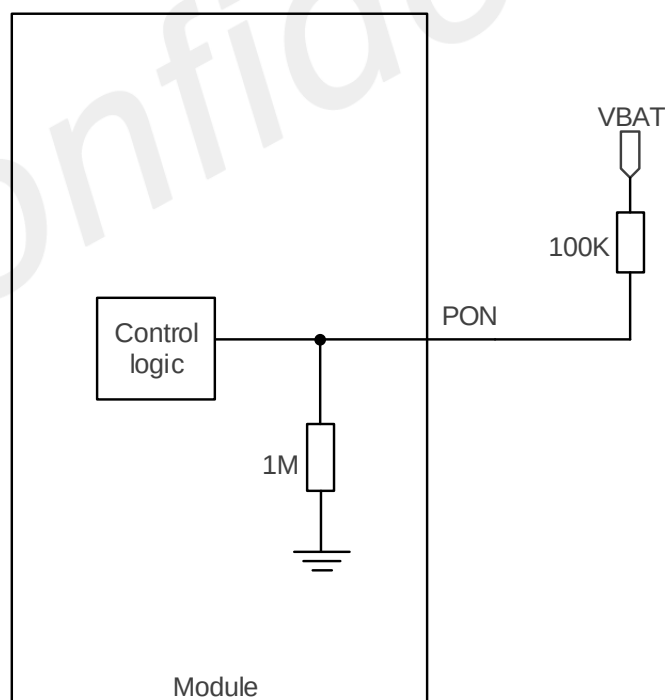


Figure 32: PON Reference Circuit

4. RF Specifications

4.1. LTE Specifications

Table 46: Conducted Transmission Power

Frequency	Power	Min.
LTE-FDD B1	23dBm +/-2.7dB	<-40dBm
LTE-FDD B2	23dBm +/-2.7dB	<-40dBm
LTE-FDD B3	23dBm +/-2.7dB	<-40dBm
LTE-FDD B4	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B7	23dBm +/-2.7dB	<-40dBm
LTE-FDD B8	23dBm +/-2.7dB	<-40dBm
LTE-FDD B12	23dBm +/-2.7dB	<-40dBm
LTE-FDD B13	23dBm +/-2.7dB	<-40dBm
LTE-FDD B18	23dBm +/-2.7dB	<-40dBm
LTE-FDD B19	23dBm +/-2.7dB	<-40dBm
LTE-FDD B20	23dBm +/-2.7dB	<-40dBm
LTE-FDD B25	23dBm +/-2.7dB	<-40dBm
LTE-FDD B26	23dBm +/-2.7dB	<-40dBm
LTE-FDD B28	23dBm +/-2.7dB	<-40dBm
LTE-FDD B66	23dBm +/-2.7dB	<-40dBm
LTE-FDD B71	23dBm +/-2.7dB	<-40dBm
LTE-TDD B34	23dBm +/-2.7dB	<-40dBm
LTE-TDD B38	23dBm +/-2.7dB	<-40dBm
LTE-TDD B39	23dBm +/-2.7dB	<-40dBm
LTE-TDD B40	23dBm +/-2.7dB	<-40dBm
LTE-TDD B41	23dBm +/-2.7dB	<-40dBm

Table 47: E-UTRA Operating Bands

E-UTRA	UL Freq.	DL Freq.	Duplex Mode
1	1920~1980 MHz	2110~2170 MHz	FDD

2	1850~1910 MHz	1930~1990 MHz	FDD
3	1710~1785 MHz	1805~1880 MHz	FDD
4	1710~1755 MHz	2110~2155 MHz	FDD
5	824~849 MHz	869~894MHz	FDD
7	2500~2570 MHz	2620~2690 MHz	FDD
8	880~915 MHz	925~960 MHz	FDD
12	699~716 MHz	729~746MHz	FDD
13	777~787 MHz	746~756 MHz	FDD
18	815~830 MHz	860~875 MHz	FDD
19	830~845 MHz	875~890MHz	FDD
20	832~862 MHz	781~821 MHz	FDD
25	1850~1915 MHz	1930~1995MHz	FDD
26	814~849 MHz	859~894 MHz	FDD
28	703~748 MHz	758~803 MHz	FDD
66	1710~1780 MHz	2110~2180 MHz	FDD
71	663~698 MHz	617~652 MHz	FDD
34	2010~2025 MHz	2010~2025 MHz	TDD
38	2570 ~2620 MHz	2570 ~2620 MHz	TDD
39	1880 ~1920 MHz	1880 ~1920 MHz	TDD
40	2300 ~2400 MHz	2300 ~2400 MHz	TDD
41	2535 ~2675 MHz	2535 ~2675 MHz	TDD

Table 48: Reference Sensitivity (QPSK)

E-UTRA Band	3GPP TS36.521-1						Actual	Duplex Mode
	1.4 MHz	3MHz	5MHz	10MHz	15 MHz	20 MHz	10 MHz	
1	-	-	-99.3	-96.3	-94.5	-93.3	-100	FDD
2	-102	-99	-97.3	-94.3	-92.5	-91.3	-98	FDD
3	-101	-98	-96.3	-93.3	-91.5	-90.3	-98.5	FDD
4	-104	-101	-99.3	-96.3	-94.5	-93.3	-99	FDD
5	-102	-99	-97.3	-94.3	-	-	-99	FDD
7	-	-	-97.3	-94.3	-92.5	-91.3	-97	FDD
8	-101	-98	-96.3	-93.3	-	-	-100	FDD
12	-101	-98	-96.3	-93.3	-	-	-96.5	FDD
13	-	-	-96.3	-93.3	-	-	-99	FDD
18	-	-	-99.3	-96.3	-94.5	-	-98	FDD
19	-102	-99	-97.3	-94.3	-	-	-99	FDD
20	-	-	-96.3	-93.3	-91.5	-90.3	-98	FDD
25	-100.5	-97.5	-95.8	-92.8	-91	-89.8	-96	FDD
26	-101.5	-98.5	-96.8	-93.8	-92	-	-98.5	FDD
28		-99.5	-97.8	-94.8	-93	-91.8	-99	FDD
66	-103.5	-100.5	-98.8	-95.8	-94	-92.8	-98.5	FDD
71	-	-	-96.5	-93.5	-91.7	-90.5	TBD	FDD

34	-	-	-99.3	-96.3	-94.5	-	-100	TDD
38	-	-	-99.3	-96.3	-94.5	-93.3	-98.5	TDD
39	-	-	-99.3	-96.3	-94.5	-93.3	-100	TDD
40	-	-	-99.3	-96.3	-94.5	-93.3	-99.5	TDD
41	-	-	-97.3	-94.3	-92.5	-91.3	-99	TDD

4.2. LTE Antenna Requirements

For better overall performance, it is recommended that the antenna design should refer to the index requirements in the following table.

Table 49: LTE Antenna Requirements

Passive	Recommended Standard
Operating band	Please refer to the table 2 and table 46
Direction	Omnidirectional
Gain	> -3dBi (Avg)
Input impedance	50 ohm
Efficiency	> 50 %
Maximum input power	50W
VSWR	< 2
Isolation	>20dB
PCB insertion loss(<1GHz)	<0.5dB
PCB insertion loss(1GHz~2.2GHz)	<1dB
PCB insertion loss(2.3GHz~2.7GHz)	<1.5dB

4.3. GNSS Specifications

Table 50: GNSS Operating Bands

Type	Frequency
GPS L1	1575.42±1.023MHz
GLONASS G1	1601.7±6.75MHz
BeiDou B1I	1561.098±2.046MHz
GALILEO E1	1575.42±1.023MHz

Table 51: GNSS Performance

GNSS	Description	Performance			
		Min	Type	Max	Unit
Horizontal Position Accuracy	Automatic position		1.49		m
Velocity Accuracy	Without Aid		0.1		m/s
	DFPS		0.05		m/s
Timing Accuracy			10		ns
Dynamic Performance	Maximum Altitude			18000	m
	Maximum Velocity			500	m/s
	Maximum Acceleration			4	G
TTFF (A-GPS off) GPS(L1)+GLONASS+BEIDOU	Hot start		0.55		s
	Warm start		19.30		s
	Cold start		18.69		s
TTFF (A-GPS off) Weak signal cold start GPS(L1)+GLONASS+BEIDOU	GSS7000=-130dB		18.69		s
	GSS7000=-140dB		24.75		s
	GSS7000=-146dB		94.07		s
	GSS7000=-147dB		-		s
TTFF (A-GPS on) Cold start (EPO in flash mode)	GPS		5.25		s
	GPS+BD		5.61		s
	GPS+GLONASS		5.78		s
	GPS+GLONASS+BD		5.64		s
Sensitivity GPS (L1)	Autonomous acquisition (cold start)		-148		dBm
	Re-acquisition		-158		dBm
	Tracking		-166		dBm
Sensitivity GPS(L1)+GLONASS	Autonomous acquisition (cold start)		-147.5		dBm
	Re-acquisition		-157.5		dBm
	Tracking		-166		dBm
Sensitivity GPS(L1)+GLONASS+BD	Autonomous acquisition (cold start)		-148		dBm
	Re-acquisition		-157.5		dBm
	Tracking		-166		dBm
Sensitivity GPS(L1)+BD	Autonomous acquisition (cold start)		-148		dBm
	Re-acquisition		-157.5		dBm
	Tracking		-166		dBm
Receiver	Channels		L1:47		
	Update rate		1	10	Hz
	Tracking L1, CA code				

Protocol support
NMEA, PAIR

4.4. GNSS Antenna Requirements

Table 52: Recommended Antenna Characteristics (GNSS)

Passive	Recommended Standard
Operating band	L1: 1559~1609MHZ
Direction	Hemisphere, face to sky
Input impedance	50 ohm
Maximum input power	50W
VSWR	<2
Plan category	RHCP or Linear
Passive antenna gain	0dBi
Active antenna gain	-2dBi
Active antenna noise figure	<1.5
Built-in antenna LNA gain	20dB(Typ.)
Total antenna gain	<18 dB
Coaxial insertion loss	<1.5dB

4.5. Antenna Reference Design

4.5.1. Passive Antenna for LTE/GNSS

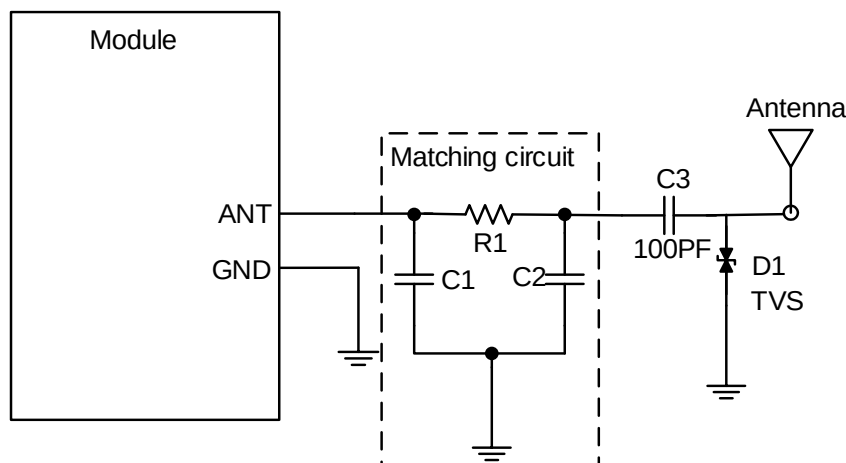


Figure 33: Passive Antenna Reference

The matching circuit R1 is labeled 0Ω by default, and C1 and C2 are reserved by default, and the specific value is determined by the antenna optimization, usually provided by the antenna manufacturer.

The antenna port is easy to introduce static electricity, to avoid the internal components of the module being damaged by static electricity, C3 is pasted with a 100pF capacitor by default to enhance ESD protection capability.

It is recommended that D1 choose a suitable two-way TVS protection device placed close to the antenna. It especially needs to pay attention to the influence of TVS junction capacitance value on RF signals. Recommended TVS models are as follows:

Table 53: TVS for RF Main Antenna Part Number List

Manufacturer	Part Number	V_{RWM}	$V_{C(Max)}$	$C_{J(Max)}$	Package
BillSEMI	BLE5V0CR05UB	5V	40V	0.05pF	DFN1006-2L

Table 54: TVS for GNSS Antenna Part Number List

manufacturer	Part Number	V_{RWM}	$V_{C(Max)}$	$P_{pp(Max)}$	$C_{J(Max.)}$	Package
WAYON	WE05DGCF-B	5V	23V	70W	0.3pF	DFN1006-2

4.5.2. Active Antenna for GNSS

The GNSS active antenna reference circuit is shown below:

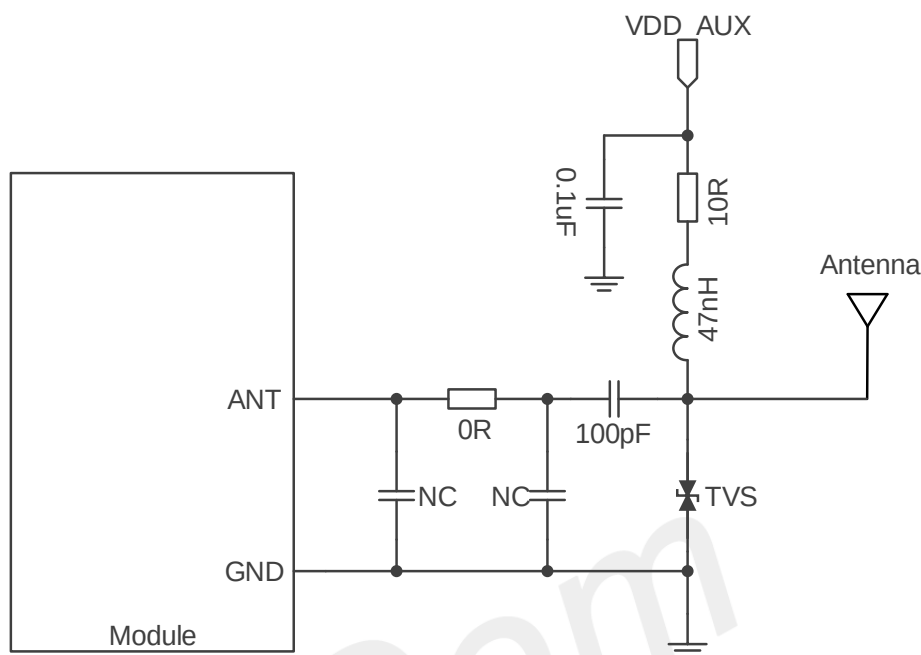


Figure 34: Active Antenna Reference

NOTE

1. GNSS adopts the active antenna design scheme by default, and C uses 100pF by default. For customers using the passive antenna scheme, it is recommended to disconnect the power supply path to avoid chip damage caused by passive antenna installation.
2. There may be parallel inductance at the antenna inside the module, showing a similar short circuit phenomenon, which is normal. Please consult SIMCom if you have any doubts about this.

4.6. PCB Layout

When routing the PCB, users should pay attention to the impedance design of the trace from the module's ANT port to the antenna connector on the PCB, controlling the impedance at 50Ω. The trace length is recommended to be kept within 20mm and should stay away from interference signals such as power supply and clock signals.

If using an IPEX connector, ensure impedance control by leaving the projection area hollow and using a reference layer.

If using an SMA connector, ensure impedance control by keeping the distance between the RF signal pad edge and the GND copper foil sufficiently far, at least 1.2mm.

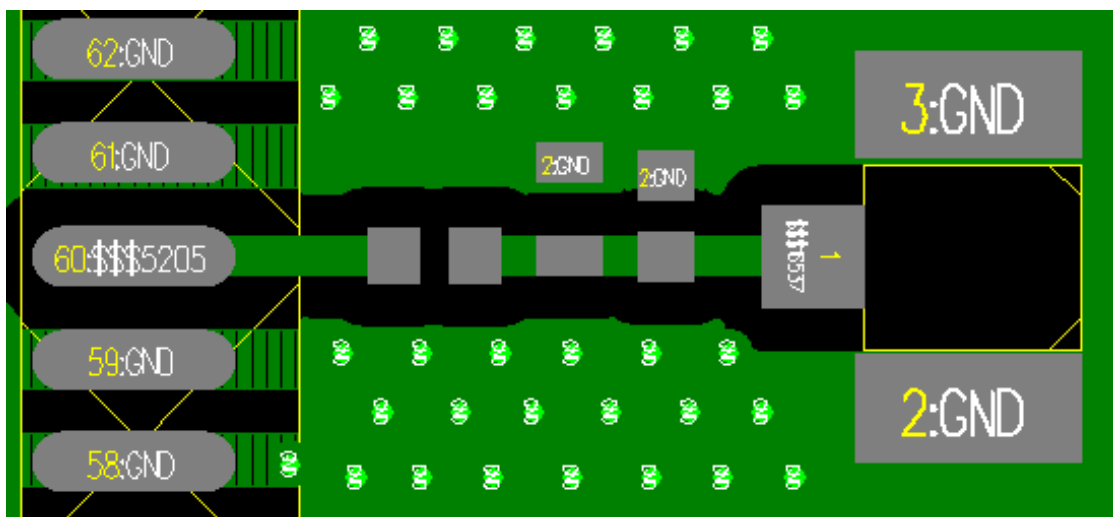


Figure 35: IPEX Connector Reference PCB layout

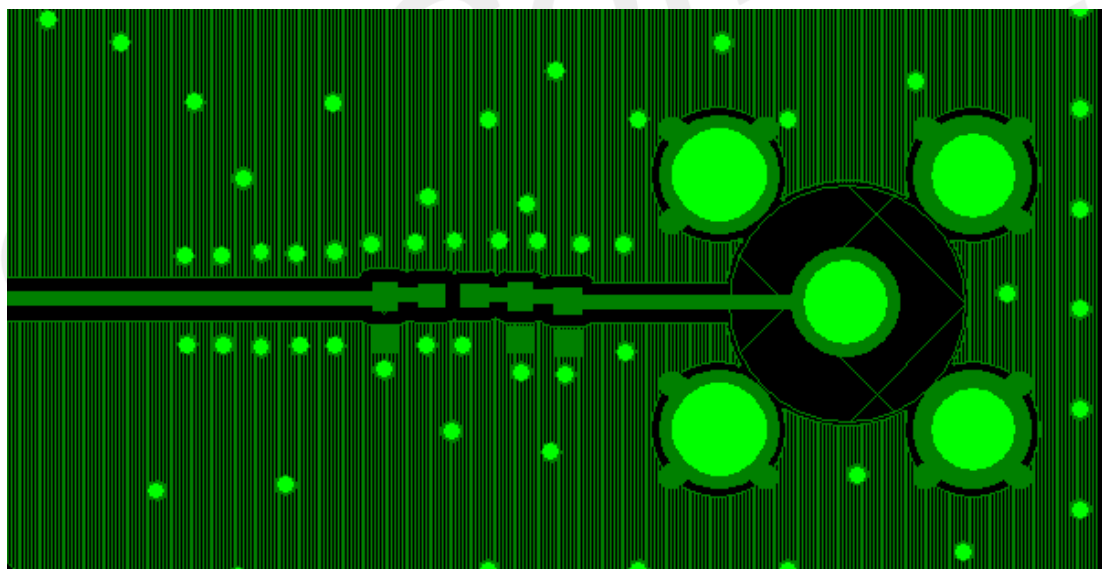


Figure 36: SMA Connector Reference PCB layout

5. Electrical Specifications

5.1. Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of A7671 are listed in the following table, exceeding these limits may cause permanent damage to the module.

Table 55: Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage on VBAT	-0.5	-	4.8	V
Voltage on USB_VBUS	-0.5	-	5.4	V
Voltage at digital pins (GPIO, I2C, UART, PCM)	-0.3	-	2.0	V
Voltage at I/O pins (USIM)	-0.3	-	2.0	V
	-0.3	-	3.9	V
Voltage at PWRKEY\RESET	-0.3	-	4.8	V

5.2. Operating Conditions

Table 56: Recommended Operating Ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	3.3	3.8	4.2	V
Voltage at USB_VBUS	3.0	5.0	5.2	V

Table 57: Operating Temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature	-30	25	75	°C
Extended operation temperature*	-40	-	85	°C
Storage temperature	-40	-	90	°C

NOTE

When Module is within the extended operation temperature range, Module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

5.3. Operating Mode

5.3.1. Operating Mode Definition

The table below summarizes the various operating modes of module.

Table 58: Operating Mode Definition

Mode		Function
Normal operation	LTE Sleep	AT command "AT+CSCLK=1" can be used to set the module to sleep mode. In this case, the current consumption of module will be reduced to the minimal level and the module can still receive paging message and SMS.
	LTE Idle	Software is active. Module is registered to the network, and the module is ready to communicate.
	LTE Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g., power control level); uplink/downlink data rates, etc.
Minimum functionality mode		AT command 'AT+CFUN=0' can be used to set the module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the module will not work and the USIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode		AT command 'AT+CFUN=4' can be used to set the module to flight mode without removing the power supply. In this mode, the RF part of the module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
PSM mode		The module can be set to PSM mode by AT command without removing the power supply. In this mode, the CPU is powered off, only the clock

	circuit inside the module works, the network is not connected, and the serial port and USB are unavailable. In this case, the power consumption of the module is reduced to the minimum.
Power off	Module will go into power off mode by sending the AT command 'AT+CPOF' or pull down the PWRKEY pin, normally. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are not accessible.

5.3.2. Sleep Mode

In sleep mode, the current consumption of module will be reduced to the minimal level, and module can still receive paging message and SMS.

Both hardware and software should meet several conditions simultaneously so that A7671 will enter into sleep mode:

- Module peripherals (GPS, Bluetooth, etc.) stop working;
- Run the AT command AT+CSCLK=<n> to set the sleep mode and wake up source.
- Disconnect the power supply from the USB_VBUS.

When the module peripheral stops working, send the AT command "AT+CSCLK=<n>" through the serial port or USB and disconnect the USB_VBUS power supply, the module will enter sleep mode.

NOTE

1. If the module enters sleep mode by sending "AT+CSCLK=1", pulling down the MAIN_DTR can wake up the module.
2. If the module enters sleep mode by sending "AT+CSCLK=2", sending data to the MAIN_RXD can wake up the module.
3. Before designing, please pay attention to how to realize sleeping/waking function and refer to document [17] for more details.

5.3.3. Minimum Functionality Mode and Flight Mode

Minimum power consumption mode ceases a majority function of Module, to enable the module enter the minimum power consumption mode, the following hardware and software conditions must be followed:

- (1) Module is in normal mode.
- (2) Send AT command "AT+CFUN=0".
- (3) Send AT command "AT+CSCLK=1".

(4) DTR pin pulled to high level and USB_VBUS pulled to low level.

This mode is set by the AT command which provides a choice of the functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If A7671 has been set to minimum functionality mode, the RF function and SIM card function will be closed. In this case, the serial port and USB are still accessible, but RF function and SIM card will be unavailable.

If A7671 has been set to flight mode, the RF function will be closed. In this case, the serial port and USB are still accessible, but RF function will be unavailable.

When A7671 is in minimum functionality or flight mode, it can return to full functionality by the AT command "AT+CFUN=1".

5.3.4. PSM Mode

The PSM mode can be set by "AT+CPSMS", and it can minimize the current consumption.

The module is initially in the RRC connect state, and it will enter idle mode after disconnecting RRC Connect by "end call", while the timer T3324/T3412 starts timing. After the timer T3324 expires, the module enters the PSM mode. The module will wake up automatically after the timer T3412 expiring, and it will enter TAU mode.

The AT command for entering the PSM mode are as follows:

AT*COMCFG=1,,,,,254//Enable the 1bis

AT+CFUN=0

AT+CPSMS=1,,,"01100101","00000101"//Open the PSM

AT+MEDCR=0,103,1

AT+MEDCR=0,71,2//Set the wake-up time to 2 minutes

AT+CFUN=1

After entering the PSM mode, the module will terminate the network connection, and unable to respond to requests. Customers can send AT command when the timer T3412 expiring or pull down the PWRKEY to wake up the module. The module will exit the PSM mode by "AT+CPSMS=0".

5.3.5. RTC Mode

Module supports RTC mode for alarm clock, timer, auto power-on by alarm clock or other functions, it can track or record the current date and time by sending "AT+CCLK?"

The following figure shows A7671 series RTC block diagram. There is an independent RC oscillator inside the PMU, RTC clock is generated by the RC oscillator directly, and it allows LDO to be turned off completely when module shuts down. Therefore, it has lower current consumption when module shuts down and enters RTC mode.

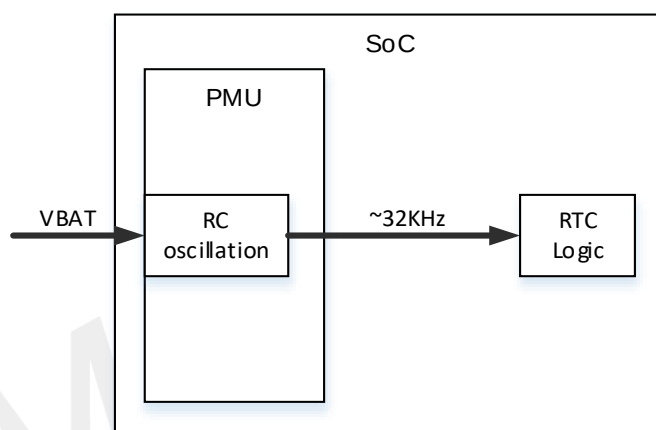


Figure 37: A7671 RTC Block Diagram

Table 59: A7671 RTC Characteristics

Operating Conditions	VBAT Current Consumption
VBAT=3.8V, Module shutdown	5uA (Typical)

5.4. Current Consumption

5.4.1. Current Consumption of VBAT

The current consumption is listed in the table below.

Table 60: A7671 Current Consumption on VBAT Pins (VBAT=3.8V)

PSM Mode	
PSM supply current	Typical: 6uA

LTE Sleep/Idle Mode

LTE supply current (Without USB connection)	Idle mode Typical: 8mA Sleep mode@DRX=0.32S typical: 1.5mA Sleep mode@DRX=0.64S typical: 1.1mA Sleep mode@DRX=1.28S typical: 1mA Sleep mode@DRX=2.56S typical: 0.9mA
--	--

Minimum Functionality Mode

AT+CFUN=0, AT+CSCLK=1	Typical: 667uA (With simcard) Typical: 620uA (Without simcard)
-----------------------	---

LTE Cat1

LTE-FDD B1	@5MHz 23dBm	Typical : 659 mA
LTE-FDD B2	@5MHz 23dBm	Typical : 635 mA
LTE-FDD B3	@5MHz 23dBm	Typical : 681 mA
LTE-FDD B4	@5MHz 23dBm	Typical : 693 mA
LTE-FDD B5	@5MHz 23dBm	Typical : 634 mA
LTE-FDD B7	@5MHz 23dBm	Typical : 768 mA
LTE-FDD B8	@5MHz 23dBm	Typical : 580 mA
LTE-FDD B12	@5MHz 23dBm	Typical : 616 mA
LTE-FDD B13	@5MHz 23dBm	Typical : 523 mA
LTE-FDD B18	@5MHz 23dBm	Typical : 635mA
LTE-FDD B19	@5MHz 23dBm	Typical : 618 mA
LTE-FDD B20	@5MHz 23dBm	Typical : 635 mA
LTE-FDD B25	@5MHz 23dBm	Typical : 626 mA
LTE-FDD B26	@5MHz 23dBm	Typical : 628 mA
LTE-FDD B28	@5MHz 23dBm	Typical : 644 mA
LTE-FDD B66	@5MHz 23dBm	Typical : 690 mA
LTE-FDD B71	@5MHz 23dBm	Typical : TBD mA
LTE-TDD B34	@5MHz 23dBm	Typical : 560 mA
LTE-TDD B38	@5MHz 23dBm	Typical : 551 mA
LTE-TDD B39	@5MHz 23dBm	Typical : 555 mA
LTE-TDD B40	@5MHz 23dBm	Typical : 562 mA
LTE-TDD B41	@5MHz 23dBm	Typical : 552 mA

5.4.2. Current Consumption of GNSS

Table 61: Current Consumption on VBAT Pins
(VBAT=3.8V, @AT+CFUN=0, AT+CSCLK=1, without USB connection)

Mode	Condition	Typical (mA)
GPS (L1)	-130dBm/Tracking	24.7

	-145dBm/Tracking	25
	-130dBm/Cold start	25.1
	-145dBm/Cold start	24.7
	Loss of lock	21.8
GPS (L1) +GLONASS	-130dBm/Tracking	26.9
	-145dBm/Tracking	27.9
	-130dBm/Cold start	27.5
	-145dBm/Cold start	25.3
	Loss of lock	25.1
GPS (L1) +BEIDOU	-130dBm/Tracking	26
	-145dBm/Tracking	25.5
	-130dBm/Cold start	25.3
	-145dBm/Cold start	26.4
	Loss of lock	23.7
Real network active antenna GPS (L1) +GALILEO+BEIDOU	Outdoor search	29.4
	Acquisition	27.8
	Loss of lock	29.3
Real network active antenna GPS (L1)	Outdoor search	25
	Acquisition	22.9
	Loss of lock	25

Table 62: GNSS Low Power Mode Current Consumption on VBAT Pins
(VBAT=3.8V, @AT+CFUN=0, AT+CSCLK=1, without USB connection)

Mode	Condition	Typical
AT+CGNSSSLEEP=0	GPS (L1) +GALILEO+BEIDOU	1.13
AT+CGNSSFITNESS=1	GPS (L1)	17
	GPS (L1) +GALILEO+BEIDOU	26.9
AT+CGNSSGLP=1	Only GPS (L1) support	7.2
AT+CGNSSFLP=1	Duty cycle 90%	25.4
	Duty cycle 75%	22.2
	Duty cycle 50%	16.2
	Duty cycle 25%	10.6
	Duty cycle 10%	6.8
AT+CGNSSALP=1		11.87
AT+CGNSSALP=2		21.7
AT+CGNSSRTC=0	V_BACKUP=3.3V, software RTC	16uA
	V_BACKUP=3.3V, hardware RTC	43uA

NOTE

1. The real network test environment should meet open-sky conditions, with the average CN0 of the top 6 satellites exceeding -40dB.
2. The-listed field power consumption values do not include the current consumption of the active antenna.

5.5. ESD Notes

A7671 is sensitive to ESD in the process of storage, transporting, and assembling. When A7671 is mounted on the customers' mother board, the ESD components should be placed beside the connectors which human body may touch, such as SIM card holder, audio jacks, switches, keys, etc. The following table shows the A7671 ESD measurement performance.

Table 63: The ESD Performance Measurement Table (Temperature: 25°C, Humidity: 45%)

Part	Contact Discharge	Air Discharge
VBAT, GND	±4KV	±8KV
Antenna port	±4KV	±8KV
Other PADS	±0.5KV	±1KV

NOTE

Test conditions:

- The external of the module has surge protection diodes and ESD protection diodes.
- The data in table above were tested using SIMCom EVB.

6. SMT Production Guide

6.1. Top and Bottom View of the module

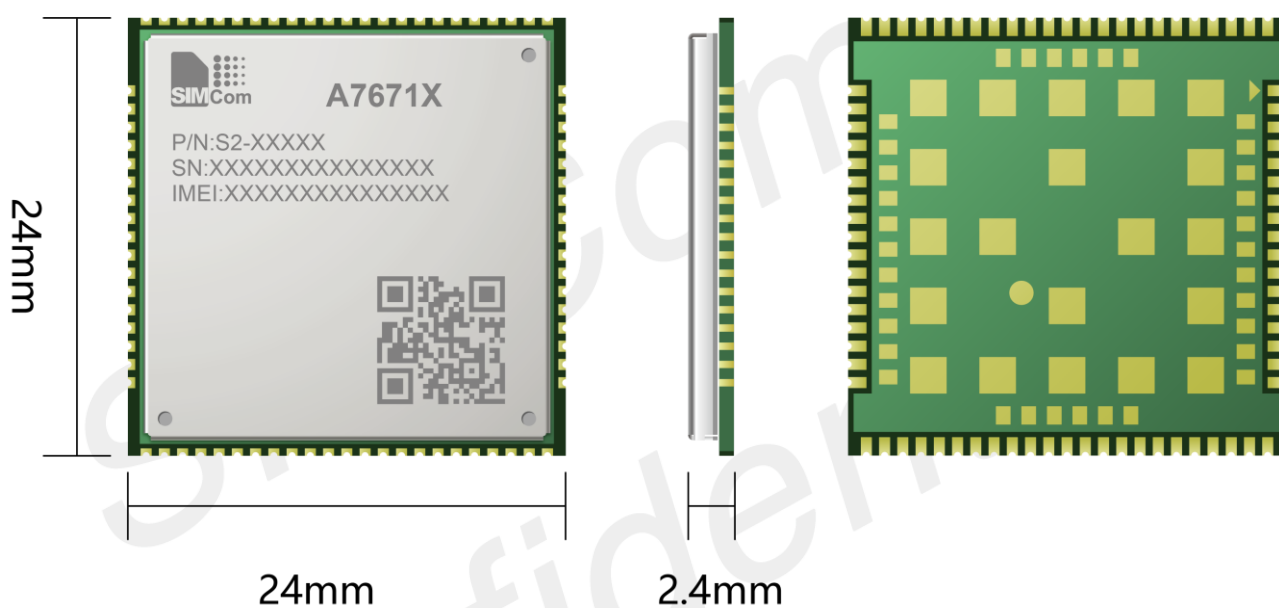


Figure 38: Top and Bottom View of the Module

NOTE

The above is the design effect diagram of the module for reference. The actual appearance is subject to the actual product.

6.2. Label Information

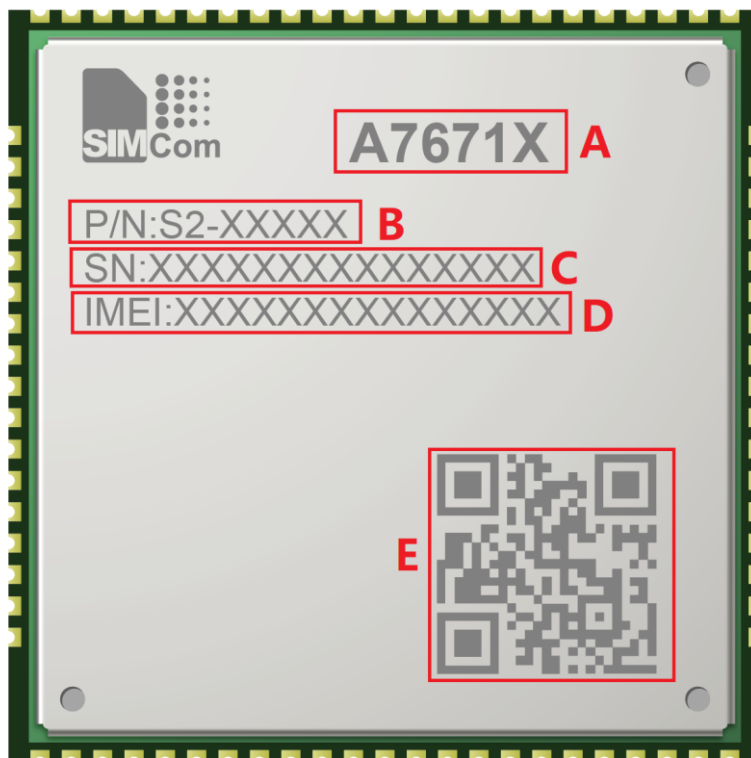


Figure 39: Label Description of the Module

Table 64: The Description of Label Information

No.	Description
A	Project name
B	Product number
C	Serial number
D	IMEI number
E	QR code

6.3. Recommended PCB Footprint

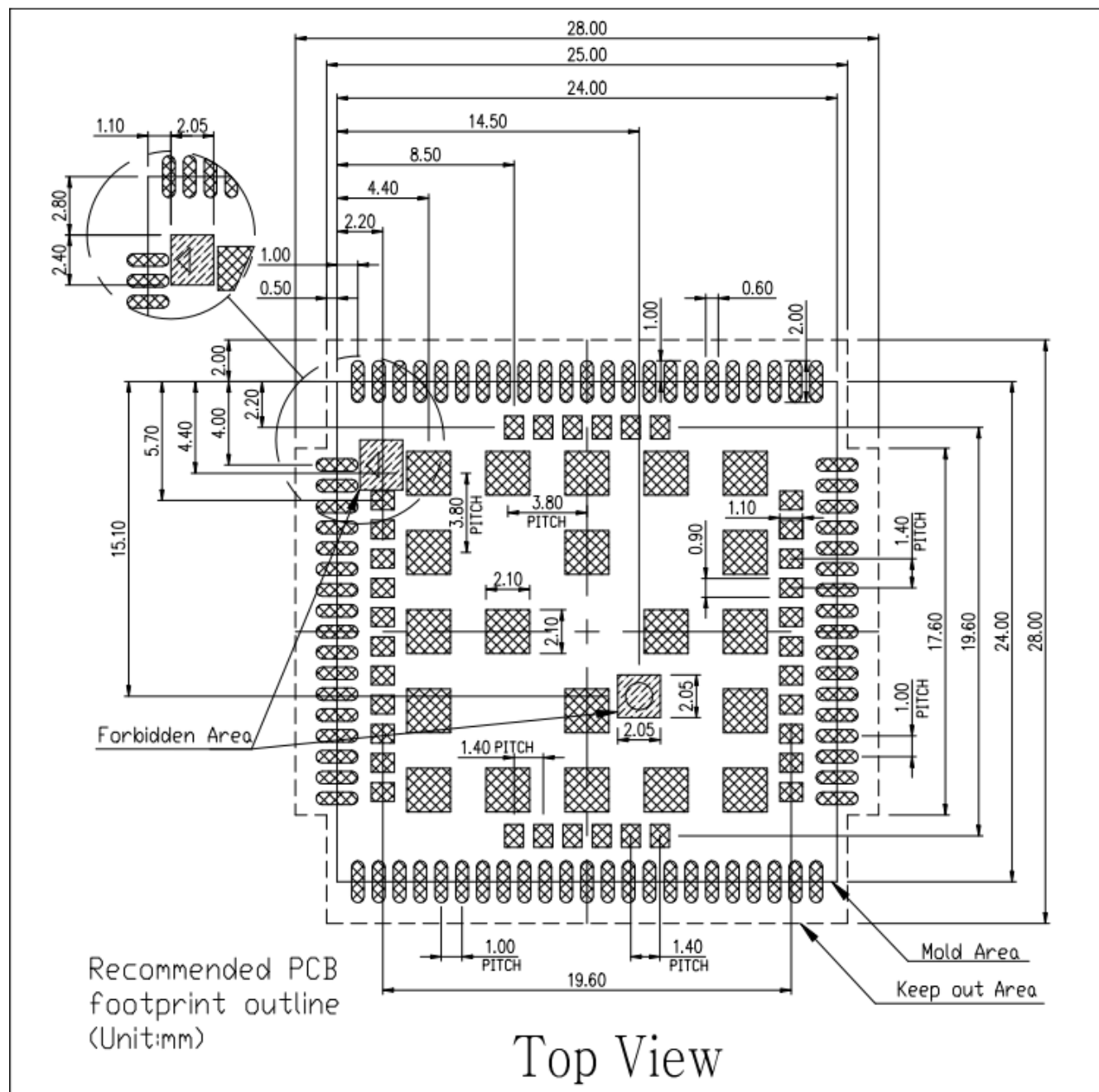


Figure 40: Footprint Recommendation (Unit: mm)

6.4. Recommended SMT Stencil

Recommend stencil thickness 0.15mm.

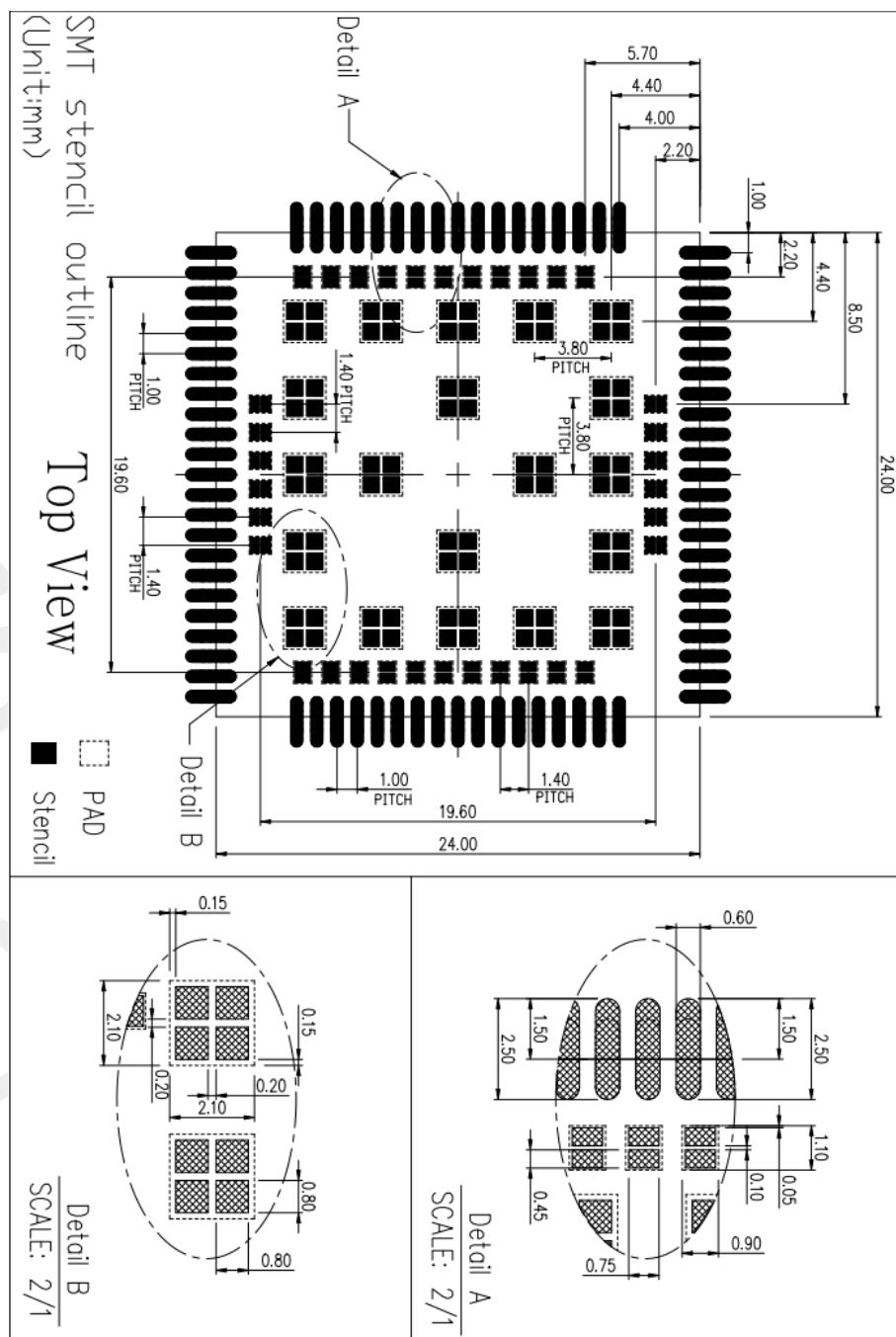


Figure 41: Recommended SMT Stencil (Unit: mm)

6.5. Recommended Reflow Furnace Temperature Curve

It is recommended to lead free.

During the furnace temperature test, the thermocouple test point should be connected to the module position to ensure that the module position reaches the required temperature. Recommended furnace temperature profile (lead-free SMT reflow) is as follows:

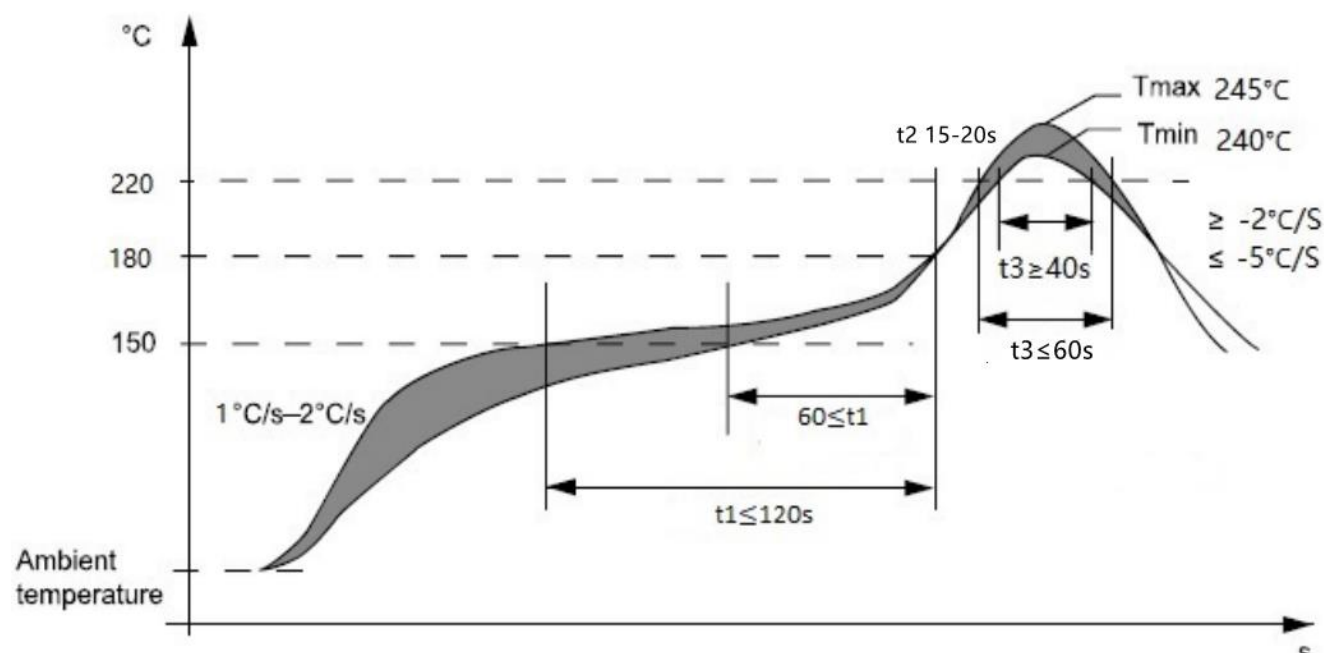


Figure 42: Recommended Reflow Furnace Temperature Curve (Lead-Free)

Table 65: The Main Board Reflux Temperature Curve Requirements (Lead-Free)

Temperature Range	Time	Critical Parameter
Preheating zone (Room temperature~150 °C)	NA	Temperature rise slope 1~2°C/s
T1(150~180°C)	60-120s	/
T2(180~220°C)	15-20s	/
T3(≥220°C)	40-60s	Peak temperature 240~245°C
Cooling Zone	NA	Cooling slope -2~-5°C/s

NOTE

- The maximum times of refluxes for the module is once.
- Recommended lead-free process.

- In the table above, the temperature testing location includes the solder mask of the module MCU pins, bottom LGA pins, and external LCC pins.
- The actual welding temperature is affected by other external factors, such as the presence of furnace carriers, solder paste, size and thickness of the substrate, and component resistance. Thermal requirements and panel design, etc. Please confirm with our engineering and technical personnel in time if the recommended parameters cannot be reached. Otherwise, the module may be damaged.
- For boards with thickness less than 1.2mm, it is recommended to use board supported by furnace carrier or materials with high Tg to prevent warping when heated. Deformation, thus affecting module welding. For modules larger than 35.0 mm *35.0 mm and 5G products, it is recommended to use the furnace carrier to pass through the furnace to reduce the cause of the bottom plate and mold. Due to the difference of Tg value of block, the phenomenon of unbalanced thermal stress appears in the process of high temperature welding reflow, resulting in the defect rate of virtual welding and little tin.
- After the module is welded, X-ray and optical inspection methods shall be used to check the welding quality. For specific standards, please refer to relevant standards of IPC-A-610H.
- For more information about shipping and manufacturing, please refer to [Module Secondary SMT Process User Guide](#).
- Due to the complexity of the SMT process, in case of uncertainty or processes not mentioned in this document (such as selective wave soldering, ultrasonic welding), please contact SIMCom support team before SMT process starts.

6.6. Moisture Sensitivity Level (MSL)

The modules are shipped in vacuum-sealed aluminum foil bag bags, vacuum packaging according to IPC/JEDEC standard J-STD-020C specification.

- Recommended storage conditions: temperature $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$, and relative humidity 35%~60%.
- Storage period: 12 months (Under recommended storage conditions and in sealed vacuum packaging).

The module meets the humidity sensitivity level 3 (MSL-3), and the storage period after unpacking is shown in table below.

The out-of-bag floor life of the module with MSL-3 is 168 hours. If the workshop temperature is $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the relative humidity is less than 60%, the module needs to be unpacked within 168 hours of reflux production or other high temperature operations. Otherwise, the module shall be stored in an environment with relative humidity less than 10% (for example, a moisture-proof cabinet) to keep the product dry.

Table 66: Moisture Sensitivity Level

MSL	Out-of-Bag Floor Life	Comment
1	Unlimited	$\leq +30^{\circ}\text{C}/85\% \text{ RH}$
2	1 year	$\leq +30^{\circ}\text{C}/60\% \text{ RH}$
2a	4 weeks	

3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	

Before using, it is necessary to confirm whether the package is in good condition. After unpacking, check the status of humidity indicator card in vacuum bag (Figure 43). The module needs to be baked before use if any of the following conditions occur.

- Explanation Humidity indicator card: 30%, 40%, and 50% of any indicator circle has discolouring.
- The module has been un-packed and the module exceeds the humidity sensitivity level corresponding to the exposed workshop time. For example, MSL=3 is 168.
- Packed, but the Shelf Life exceeds 12 months.
- Exceeds the Floor Life.
- Unable to track and determine the status of the module.

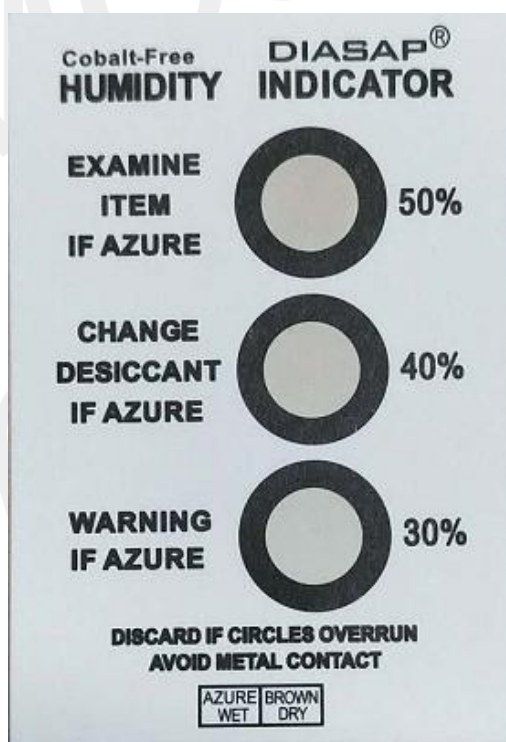


Figure 43: Humidity Card

The following conditions also need to be pre-baked.

- The storage temperature and humidity do not meet the recommended storage conditions.
- Vacuum sealed bag leak, bulk materials.
- Before repairing the module.
- After unpacking, the module failed to complete production or storage under the control of humidity sensitive level 3.

6.7. Baking Requirements

If baking is required, proceed according to the requirements in the table below. Preferentially choose a nitrogen-filled oven.

Table 67: Module Baking Requirements

Baking Conditions	Baking Time	Comment
120°C±5°C, <5% RH	8 hours	Not applicable to original packaging pallets

NOTE

- In order to prevent and reduce the occurrence of poor welding caused by moisture, such as foaming and delamination, the module should be strictly controlled. It is not recommended to expose the module to air for a long time after unpacking the vacuum package.
- Before baking, it is necessary to remove the module from the package and place the bare module on the high temperature resistant device to avoid high temperature damage to the plastic tray or coil. The modules for secondary baking must be welded within 24 hours after baking. Otherwise, they need to be stored in vacuum packaging or in a drying oven.
- Please pay attention to ESD protection when unpacking and placing modules, such as wearing anti-static gloves.

7. Packaging

A7671 module support tray packaging.

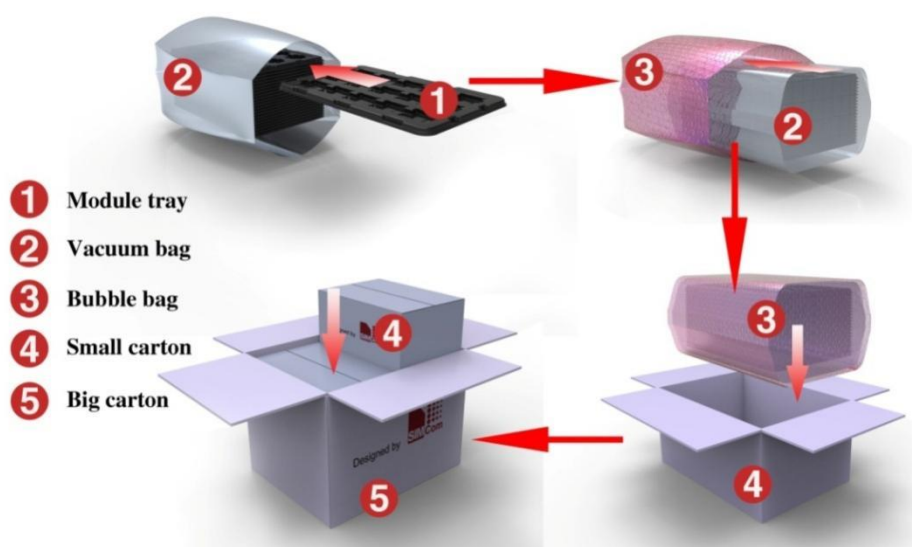


Figure 44: Packaging Diagram

Module tray drawing:

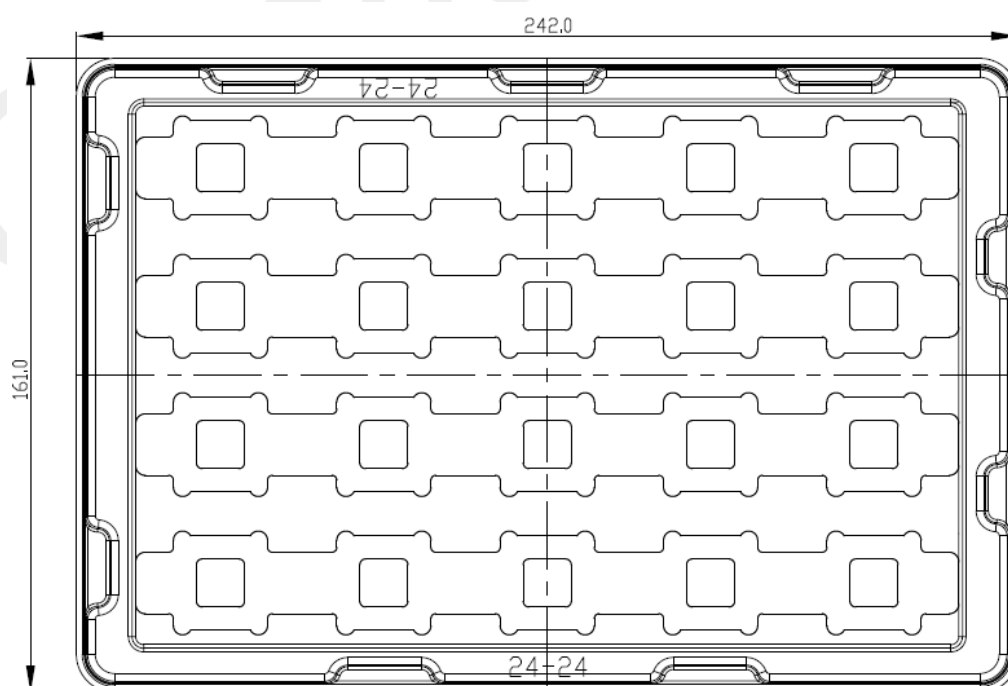


Figure 45: Tray Drawing

Table 68: Tray Size

Length ($\pm 3\text{mm}$)	Width ($\pm 3\text{mm}$)	Module Number
242.0	161.0	20

Small carton drawing:

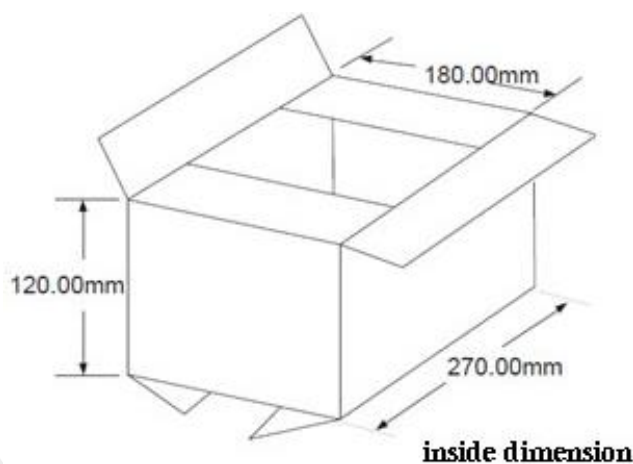


Figure 46: Small Carton Drawing

Table 69: Small Carton Size

Length ($\pm 10\text{mm}$)	Width ($\pm 10\text{mm}$)	Height ($\pm 10\text{mm}$)	Module Number
270	180	120	20*20=400

Big carton drawing:

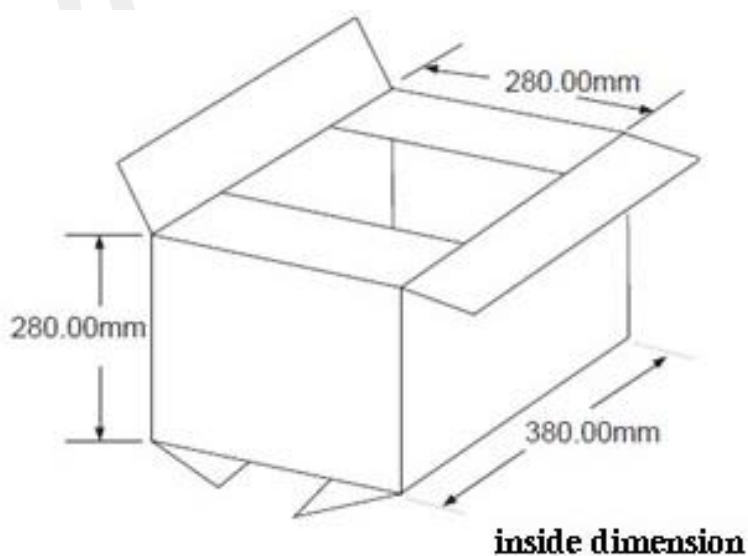


Figure 47: Big Carton Drawing

Table 70: Big Carton Size

Length ($\pm 10\text{mm}$)	Width ($\pm 10\text{mm}$)	Height ($\pm 10\text{mm}$)	Module Number
380	280	280	400*4=1600

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8. Appendix

8.1. Coding Schemes and Maximum Net Data Rates over Air Interface

Table 71: Coding Schemes and Maximum Net Data Rates over Air Interface

LTE-FDD Device Category (Downlink)	Max Data Rate (Peak)	Modulation Type
Category 1	10Mbps	QPSK/16QAM/64QAM
LTE-FDD Device Category (Uplink)	Max Data Rate (Peak)	Modulation Type
Category 1	5Mbps	QPSK/16QAM

8.2. Related Documents

Table 72: Related Documents

NO.	Title	Description
[1]	A76XX Series_AT Command Manual	AT Command Manual
[2]	ITU-T Draft new recommendation V.25ter	Serial asynchronous automatic dialing and control
[3]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[4]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[5]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[6]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[7]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.

[8]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[9]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment.
[10]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[11]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[12]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[13]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
[14]	Module Secondary SMT Process User Guide_V1.xx	Module secondary SMT Guidelines
[15]	A76XX Series_UART_Application Note	This document describes how to use UART interface of SIMCom modules.
[16]	Antenna design guidelines for diversity receiver system	Antenna design guidelines for diversity receiver system
[17]	A76XX Series_Sleep Mode_Application Note	Sleep Mode Application Note
[18]	A76XX Series_UIM HOT SWAP_Application Note	This document introduces UIM card detection and UIM hot swap.
[19]	SIMCOM_A7600_PSM&eDRX_Application guide	This document introduces the module PSM&eDRX working mode

8.3. Terms and Abbreviations

Table 73: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ARP	Antenna Reference Point
BER	Bit Error Rate
BD	BeiDou
BTS	Base Transceiver Station
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
DAM	Downloadable Application Module
DPO	Dynamic Power Optimization
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FCC	Federal Communications Commission (U.S.)
FD	SIM fix dialing phonebook
FDMA	Frequency Division Multiple Access
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global Standard for Mobile Communications
HR	Half Rate
I2C	Inter-Integrated Circuit
IMEI	International Mobile Equipment Identity
LTE	Long Term Evolution

MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
NMEA	National Marine Electronics Association
PAP	Password Authentication Protocol
PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PCS	Personal Communication System, also referred to as GSM 1900
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
SIM	Subscriber Identification Module
SMS	Short Message Service
SMPS	Switched-mode power supply
TDMA	Time Division Multiple Access
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio
EDGE	Enhanced data rates for GSM evolution
ZIF	Zero intermediate frequency
WCDMA	Wideband Code Division Multiple Access
VCTCXO	Voltage control temperature-compensated crystal oscillator
SIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system
UART	Universal asynchronous receiver transmitter
PSM	Power saving mode
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

8.4. Safety Caution

Table 74: Safety Caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	GSM cellular terminals or mobiles operating over radio frequency signals and cellular networks cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.

FCC Statements:

RF Exposure Information: To maintain compliance with FCC RF exposure requirements, use the product that maintain a 20cm separation distance between the user's body and the host.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

- (1) this device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device is intended only for OEM integrators under the following conditions:

1. The antenna must be installed such that 20 cm is maintained between the antenna and users.
2. The transmitter module may not be co-located with any other transmitter or antenna. As long as the two conditions above are met, additional transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required for the installed module.

Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Federal Communications Commission of the U.S. Government (FCC) authorizations are no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator shall be responsible for re-evaluating the end-product (including the transmitter) and obtaining a separate FCC authorization in the U.S..

OEM Integrators - End Product Labeling Considerations:

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains, FCC ID: 2AJYU-8BM0001". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

OEM Integrators - End Product Manual Provided to the End User:

The OEM integrator shall not provide information to the end user regarding how to install or remove this RF module in end product user manual. The end user manual must include all required regulatory information and warnings as outlined in this document.