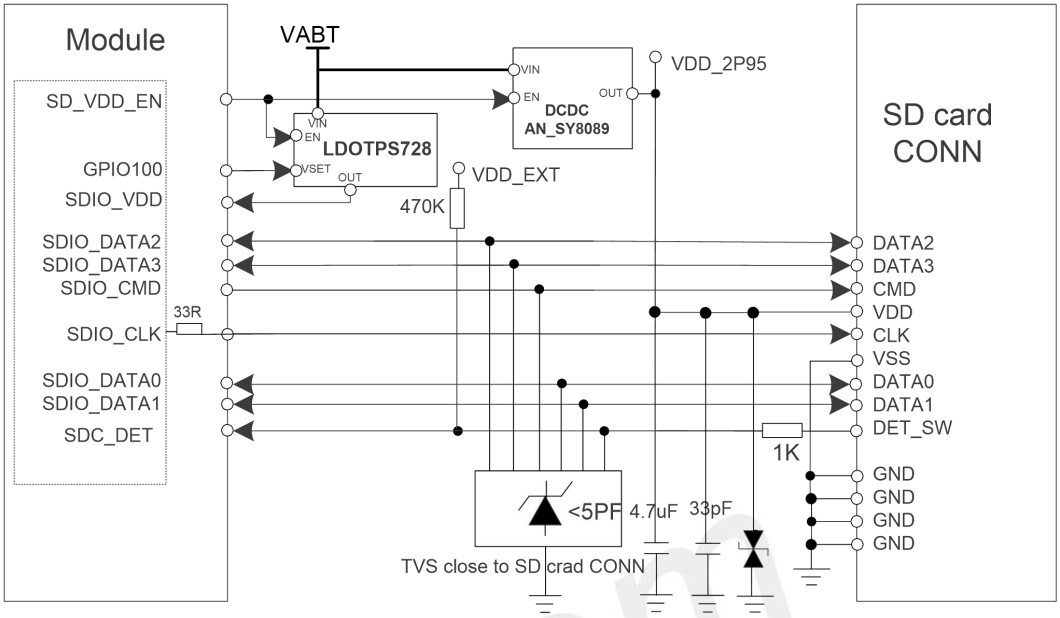

Figure 27: SD card reference circuit

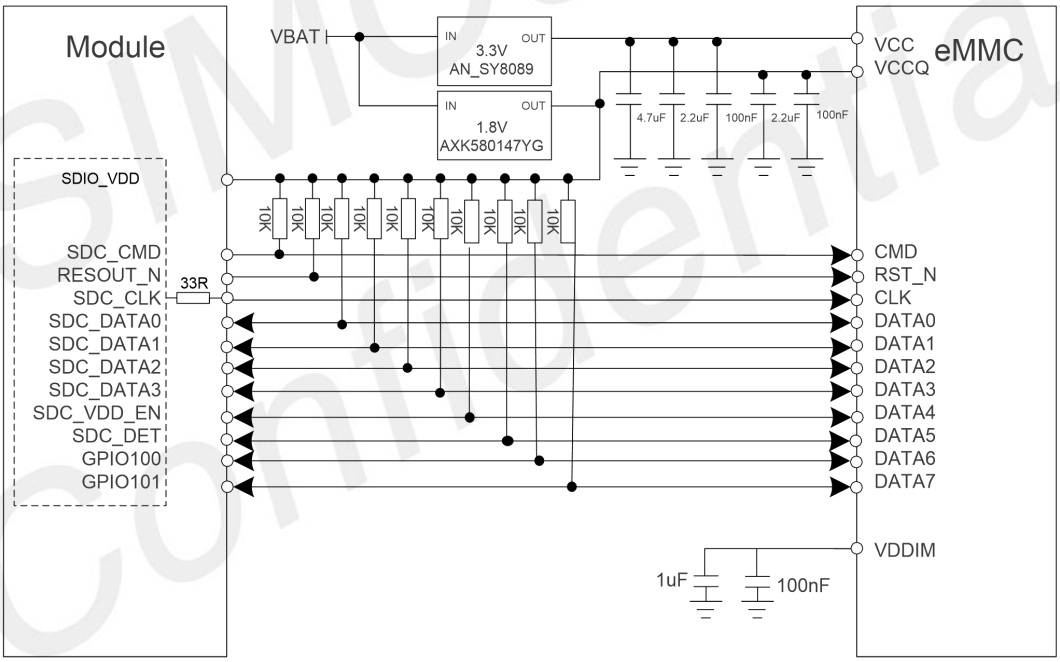

Figure 28: eMMC reference circuit

Table 28: Definition of SDIO interface

Pin name	Pin no.	Pin characteristics		Functional description	Comment
SDIO_VDD[1]	F7	PI	1.8/3.0V	Power input for internal SDIO circuit	
SDIO_DATA0	B1	DIO	P2	SDC data bit 0 or eMMC data bit 0	Required 45Ω impedance

SDIO_DATA1	C1	DIO	P2	SDC data bit 1 or eMMC data bit 1	
SDIO_DATA2	D3	DIO	P2	SDC data bit 2 or eMMC data bit 2	
SDIO_DATA3	F3	DIO	P2	SDC data bit 3 or eMMC data bit 3	
SDIO_CMD	G5	DIO	P2	SDC command output	
SDIO_CLK	E5	DO	P2	SDC clock output	
SD_VDD_EN	H7	DO	P3	Enable the SD card power or eMMC data bit 4	If used as eMMC data signals, required 45Ω impedance
SDIO_DET	E1	DI	P3	SD card insertion detect or eMMC data bit 5	
GPIO100	H3	DIO	P3	eMMC data bit 6	
GPIO101	K7	DIO	P3	eMMC data bit 7	
RESOUT_N	AW17	DO	P3	eMMC RST_N	

NOTE

- If not use SDIO interface, the SD_VDD pin should connect to VDD_EXT out of the module.

Table 29: Recommended TVS and SD card socket list

Name	Manufacturer	Model
TVS	ON	ESD9L5.0ST5G
SD card socket	ALPS	SCHA4B0400
eMMC	SanDisk	SDINBDG4_8G

SDIO interface layout guidelines:

- Require trace impedance is 45Ω.
- CLK to DATA/CMD length mismatch is less than 0.5mm.
- 33Ω termination resistance on clock be placed in module.
- Gap from other signals keeps 1.5xline width.
- Gap lane-to-lane 1.5xline width.
- Bus capacitance load is less than 5pF.
- Trace routes away from other sensitive signals.
- Maximum PCB trace length cannot exceed 30mm out of the module for 104Mbps data rate, the shorter trace and better.
- Maximum PCB trace length cannot exceed 100mm out of the module for 50Mbps data rate, the shorter trace and better.

3.8 (U)SIM Interface

SIM8260A supports two (U)SIM cards but single standby. (U)SIM1 and (U)SIM2 are dual-voltage 1.8 V or 3.0 V interfaces.

Table 30: (U)SIM electronic characteristics in 1.8V mode ((U)SIM_PWR=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
(U)SIM_VDD	Power supply for (U)SIM card	1.65	1.8	1.95	V
V_{IH}	High-level input voltage	1.26	-	1.95	V
V_{IL}	Low-level input voltage	0	-	0.36	V
V_{OH}	High-level output voltage	1.44	-	1.8	V
V_{OL}	Low-level output voltage	0	-	0.4	V

Table 31: (U)SIM electronic characteristics 3.0V mode ((U)SIM_PWR=3.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
(U)SIM_VDD	Power supply for (U)SIM card	2.7	3.0	3.05	V
V_{IH}	High-level input voltage	2.1	-	3.05	V
V_{IL}	Low-level input voltage	0	-	0.6	V
V_{OH}	High-level output voltage	2.4	-	3.0	V
V_{OL}	Low-level output voltage	0	-	0.4	V

The module supports (U)SIM card hot-swap function through the (U)SIM_DET pin, which is a level trigger pin and needs to be pulled up externally. The USIM_DET pin requires pull up externally. The following figure shows (U)SIM card reference circuit.

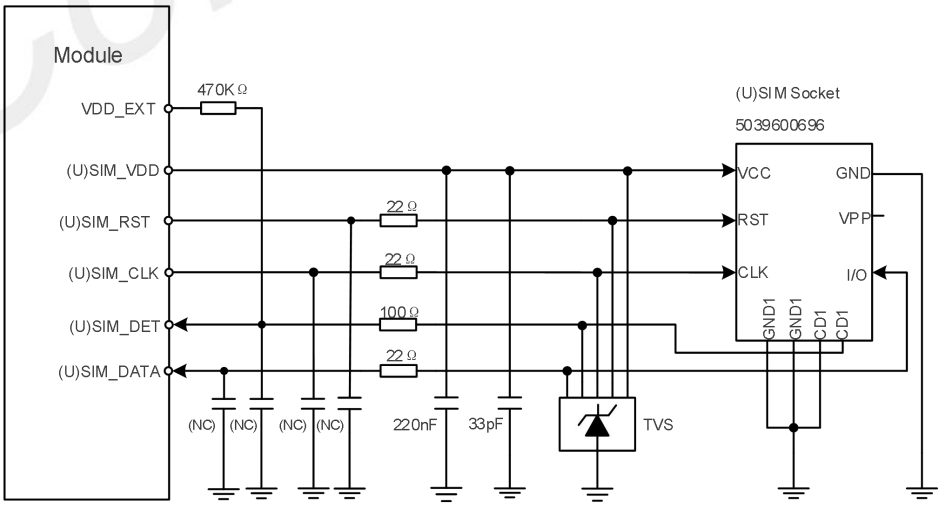

Figure 29: (U)SIM interface reference circuit

After inserting (U)SIM card, the (U)SIM_DET pin will change from low to high level. The rising edge will indicate that the (U)SIM card has been inserted. After removing the (U)SIM card, the (U)SIM_DET pin will change from high to low level. This falling edge will indicate the removal of the (U)SIM card.

Using “AT+UIMHOTSWAPON=0 or 1” and “AT+UIMHOTSWAPLEVEL=0 or 1”AT command to set module SIM card hot swap function enable and SIM card detection level, for more details, please refer to SIM8200 Series_AT Command Manual document.

Using “AT+SMSIMCFG=1,1” and “AT+SMSIMCFG=1,2” AT command to switch (U)SIM1 and (U)SIM2 function, for more details, please refer to SIM8200 Series_AT Command Manual document.

Table 32: Definition of (U)SIM interface

Pin name	Pin no.	Pin characteristics		Functional description	Comment
(U)SIM1_VDD	B51	PO	P4	Power supply for (U)SIM1 card	1.8/3.0V voltage domain, (U)SIM interface should be protected against ESD. If unused, please keep open
(U)SIM1_DATA	E51	DIO	P4	(U)SIM1 card data signal, which has been pulled up to (U)SIM1_VDD by a 20K resistor internally	
(U)SIM1_CLK	D49	DO	P4	(U)SIM1 clock signal	
(U)SIM1_RST	C51	DO	P4	(U)SIM1 reset signal	
(U)SIM1_DET	E47	DI	P3	(U)SIM1 card detect signal, which need pulled up to VDD_EXT by a 470K resistor externally	
(U)SIM2_VDD	F49	PO	P5	Power supply for (U)SIM2 card	
(U)SIM2_DATA	G47	DIO	P5	(U)SIM2 card data, which has been pulled up to (U)SIM2_VDD by a 20K resistor internally	
(U)SIM2_CLK	H49	DO	P5	(U)SIM2 clock signal	
(U)SIM2_RST	G51	DO	P5	(U)SIM2 reset signal	
(U)SIM2_DET	F45	DI	P3	(U)SIM2 card detect, which need pulled up to VDD_EXT by a 470KR resistor externally	

The following table shows recommended TVS of ESD protect and (U)SIM socket.

Table 33: Recommended TVS and (U)SIM socket list

Name	Manufacturer	Model
TVS	ST	ESDA6V1-5W6
(U)SIM socket	Suntech	5039600696

If the (U)SIM card hot-swap function is not used, customers should keep the (U)SIM_DET pin open.

The (U)SIM card layout guidelines:

- Make sure that the (U)SIM card socket should be far away from the antennas.
- (U)SIM traces should be away from RF, VBAT and high-speed signals.
- The traces should be as short as possible.
- Keep (U)SIM socket's GND pin directly connect to the main ground.
- Shielding the (U)SIM card signals by ground.
- Recommended to place a 33pF～1uF capacitor on (U)SIM_VDD net and place close to the holder.
- The rise/fall time of (U)SIM_CLK should not exceed 40ns.
- The parasitic capacitance of TVS should not exceed 60pF, and the TVS should be placed close to the (U)SIM socket.

3.9 I2S Interface

SIM8260A supports one I2S/PCM interface for external codec, which meets the requirements in the Phillips I2S bus specification.

Table 34: I2S format

Characteristics	Specification
Line interface format	Linear(fixed)
Data length	16bits(fixed)
I2S flock/sync source	Master mode(fixed)
I2S clock sate	1.536 MHz (default)
I2S MCLK rate	12.288MHz (default)
Data ordering	MSB

NOTE

- For more details about I2S AT commands, please refer to document [1] in the appendix.

3.9.1 I2S Timing

The module supports I2S sampling rate of 48 KHz and 32bit coding signal (16bit length), the timing sequence is shown in the following figure.

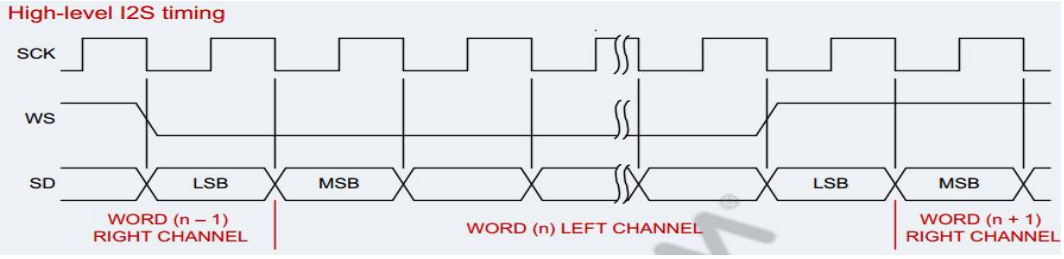

Figure 30: I2S timing

Table 35: I2S timing parameters

Signal	Parameter	Description	Min.	Typ.	Max.	Unit
I2S_MCLK	Frequency	Frequency	–	12.288	12.288	MHz
	T	Clock period	81.380	81.380	–	ns
	t(HC)	Clock high	0.45T	–	0.55T	ns
	t(LC)	Clock low	0.45T	–	0.55T	ns
I2S_CLK	Frequency	Frequency	8	48	48	KHz
	T	Clock period	20.83	20.83	125	us
	t(HC)	Clock high	0.45T	–	0.55T	ns
	t(LC)	Clock low	0.45T	–	0.55T	ns
I2S_WS	t(sr)	DIN/DOUT and WS input setup time	16.276	–	–	ns
	t(hr)	DIN/DOUT and WS input hold time	0	–	–	ns
	t(dtr)	DIN/DOUT and WS output delay	–	–	65.10	ns
	t(htr)	DIN/DOUT and WS output hold time	0	–	–	ns

3.9.2 I2S Reference Circuit

The following figure shows the external codec reference design.

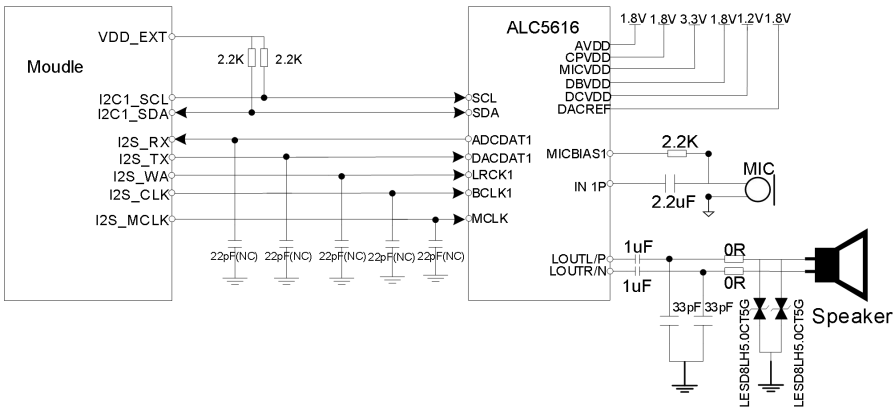

Figure 31: Audio codec reference circuit

The PCM interface is multiplexing with I2S interface. The default audio interface of the module is I2S.

Table 36: The PCM interface is multiplexing with I2S interface

Pin name	Pin no.	Electrical description		Description	Comment
I2S_DOUT/ PCM_DOUT	N1	DO	P3	I2S/PCM data output	Default is I2S interface, can be configured as PCM interface by software, If unused, please keep open
I2S_DIN/ PCM_DIN	R1	DI	P3	I2S/PCM data input	
I2S_CLK/ PCM_CLK	P3	DO	P3	I2S/PCM clock output	
I2S_WS/ PCM_SYNC	T3	DIO	P3	I2S word selection/ PCM synchronization signal	
I2S_MCLK	L1	DO	P3	I2S master clock output	

NOTE

- For more details about audio function, please refer to Document [19] in the appendix.
- Codec ALC5616 supports 5-wire I2S by default. Software can configure the internal registers of ACL5616 to configure 4-wire I2S (without I2S_MCLK signal) or 5-wire I2S (with I2S_MCLK signal) interface.

Table 37: Recommended audio list

Name	Manufacturer	Model
ALC5616	REALTEK	ALC5616-CGT

Audio layout guidelines：

Analog input

- 0.2mm trace widths; 0.2mm spacing between traces.
- Pseudo differential route for MIC.
- Isolate from noise sources, such as antenna, RF signals, SMPS, clocks, and other high speeding signals.

Analog output

- Isolate from noise sources such as antenna, RF signals, SMPS, clocks, and other digital signals with fast transients.
- Speaker output signal – route as differential pair with 0.5mm trace widths.

3.10 I2C Interface

SIM8260A default support two I2C interfaces, meet I2C specification version 5.0, and data rate up to 400 Kbps. The following figure shows the I2C bus reference circuit.

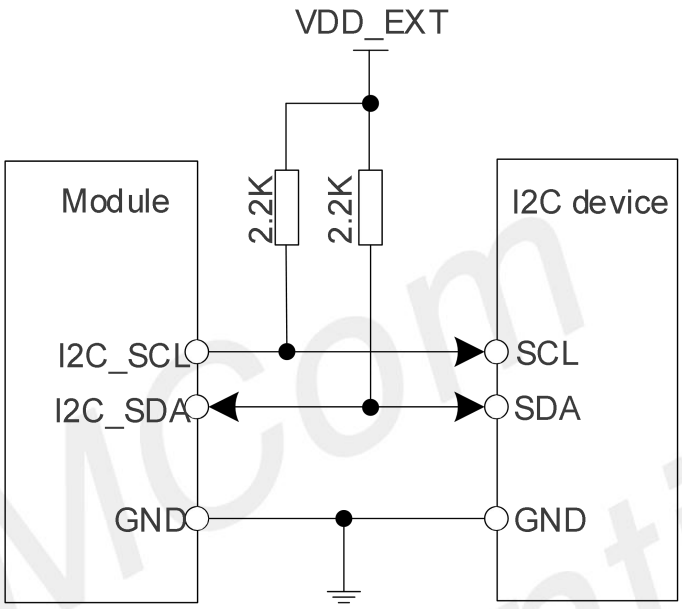

Figure 32: I2C reference circuit

Table 38: Definition of I2C interface

Pin name	Pin no.	Electrical description	description	Comment
I2C1_SCL	M7	OD	P3	I2C1 default use for codec Pull up to VDD_EXT externally
I2C1_SDA	P7	OD	P3	
I2C2_SCL	AB7	OD	P3	I2C2 default use for sensor Pull up to VDD_EXT externally
I2C2_SDA	Y7	OD	P3	

NOTE

- SDA and SCL need to pull up to VDD_EXT by a 2.2K resistor externally.
- For more details about AT commands please refer to document [1] in the appendix.

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3.11 UART Interface

SIM8260A default supports 3 UART ports for communication, which data rate up to 4Mbps. All the UART level of SIM8260A is 1.8V. If it communicates with the 3.3V serial port level, a level conversion chip needs to be added in the middle. It is recommended to use TXS0104EPWR level shift of TI, the reference circuit is as follows.

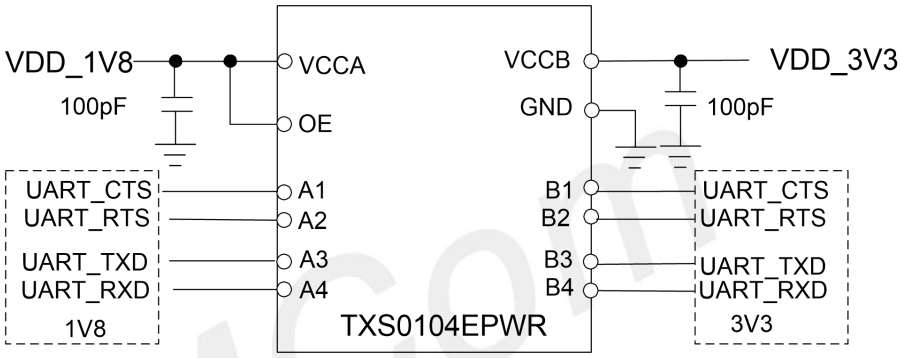

Figure 33: UART level conversion circuit

The following level shifting circuits can also be used:

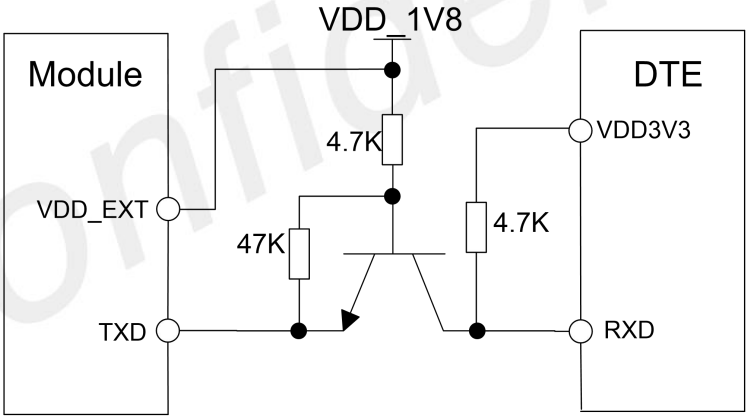

Figure 34: UART TX level conversion circuit

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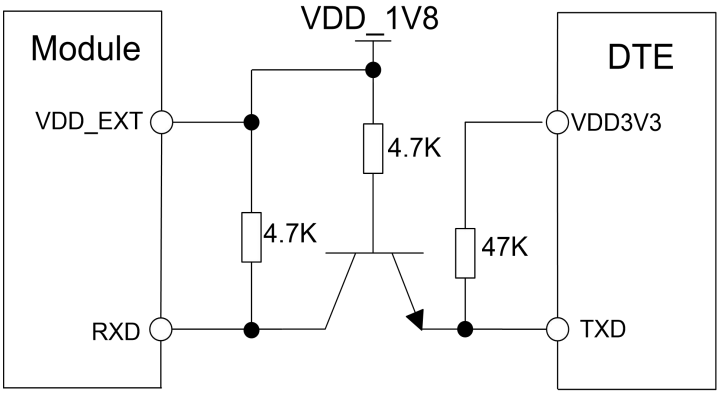

Figure 35: UART RX level conversion circuit

Table 39: Definition of UART interface

Pin name	Pin no.	Electrical description		description	Comment
UART1_CTS	AA1	DI	P3	Clear to send	Default use for AT command
UART1_RTS	AC1	DO	P3	Request to send	
UART1_TXD	AB3	DO	P3	Transmit data	
UART1_RXD	AD3	DI	P3	Receive data	
UART1_DCD	W5	DO	P3	Carrier detect	
UART1_RI	AA5	DO	P3	Ring indicator	
UART1_DTR	AC5	DI	P3	Data terminal ready	
BT_UART_CTS	R5	DI	P3	Clear to send	Default use for BT
BT_UART_RTS	U5	DO	P3	Request to send	
BT_UART_TXD	T7	DO	P3	Transmit data	
BT_UART_RXD	V7	DI	P3	Receive data	
DBG_UART_RXD	L5	DI	P3	Receive data	Used for debug only
DBG_UART_TXD	N5	DO	P3	Transmit data	

NOTE

- The 4-wire UART interface support flow control function.
- The baud rate frequency band supported by the serial port: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600,115200,203400,460800,921600. The UART rate is as high as 4MHZ. When the baud rate is greater than 460bps, it is not recommended to use a transistor for level conversion.
- The UART rate is as high as 4MHZ. When the baud rate is greater than 460Kbps, it is not recommended to use a transistor for level conversion.
- UART1 is used as AT command and DTR detection by default, it is not recommended to be used for other functions

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3.12 SPI Interface

SIM8260A SPI interface only supports master mode, data rate up to 50MHz. Usually, SPI interface is used to connect ROM or LCD and other devices. The SPI reference circuit is shown as follows:

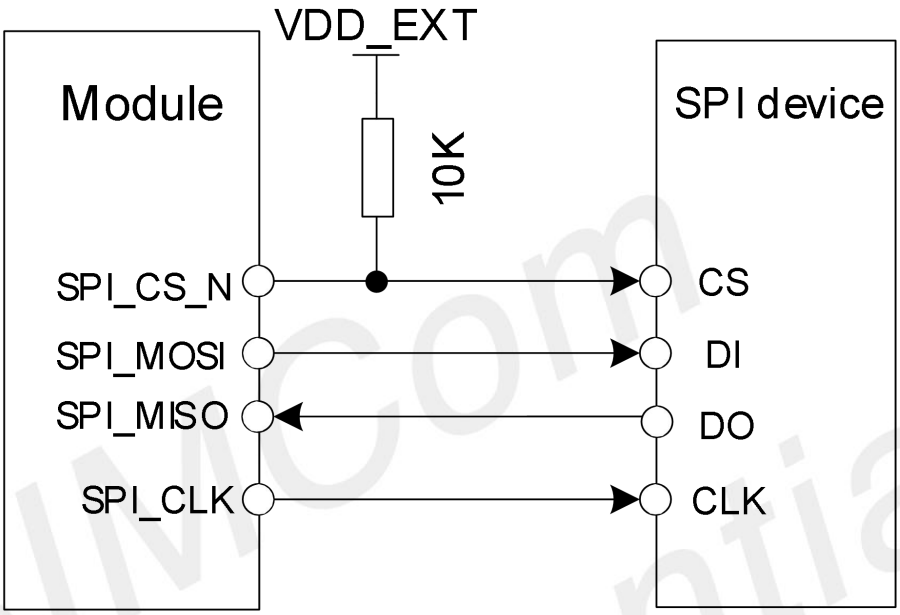

Figure 36: SPI reference circuit

Table 40: Definition of SPI interface

Pin name	Pin no.	Electrical description	description	Comment
SPI_CS_N	D18	DO	SPI chip select	
SPI_CLK	D20	DO	SPI clock	
SPI_MOSI	D14	DO	Master output slaver input	
SPI_MISO	D16	DI	Master input slaver output	

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3.13 ADC Interface

SIM8260A supports two 16bits ADC interfaces. Its performance parameters are shown as follows:

Table 41: Definition of ADC interface

Pin name	Pin no.	Electrical description	description	Comment
ADC0	AH7	AI	Analog to digital converter input0	
ADC1	AF7	AI	Analog to digital converter input1	

Table 42: ADC performance parameters

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range	Programmable	0	-	1.875	V
Resolution		-	16	-	bits
Analog input bandwidth		-	500	-	KHz
Sample rate		-	4.8	-	MHz
Accuracy		-	20	-	mV

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3.14 WLAN/BT Interface

SIM8260A supports W82 interface including PCIe, UART, GPIOs, and customers can connect to the W82 WLAN/BT module through this interface. The reference circuit is as follows:

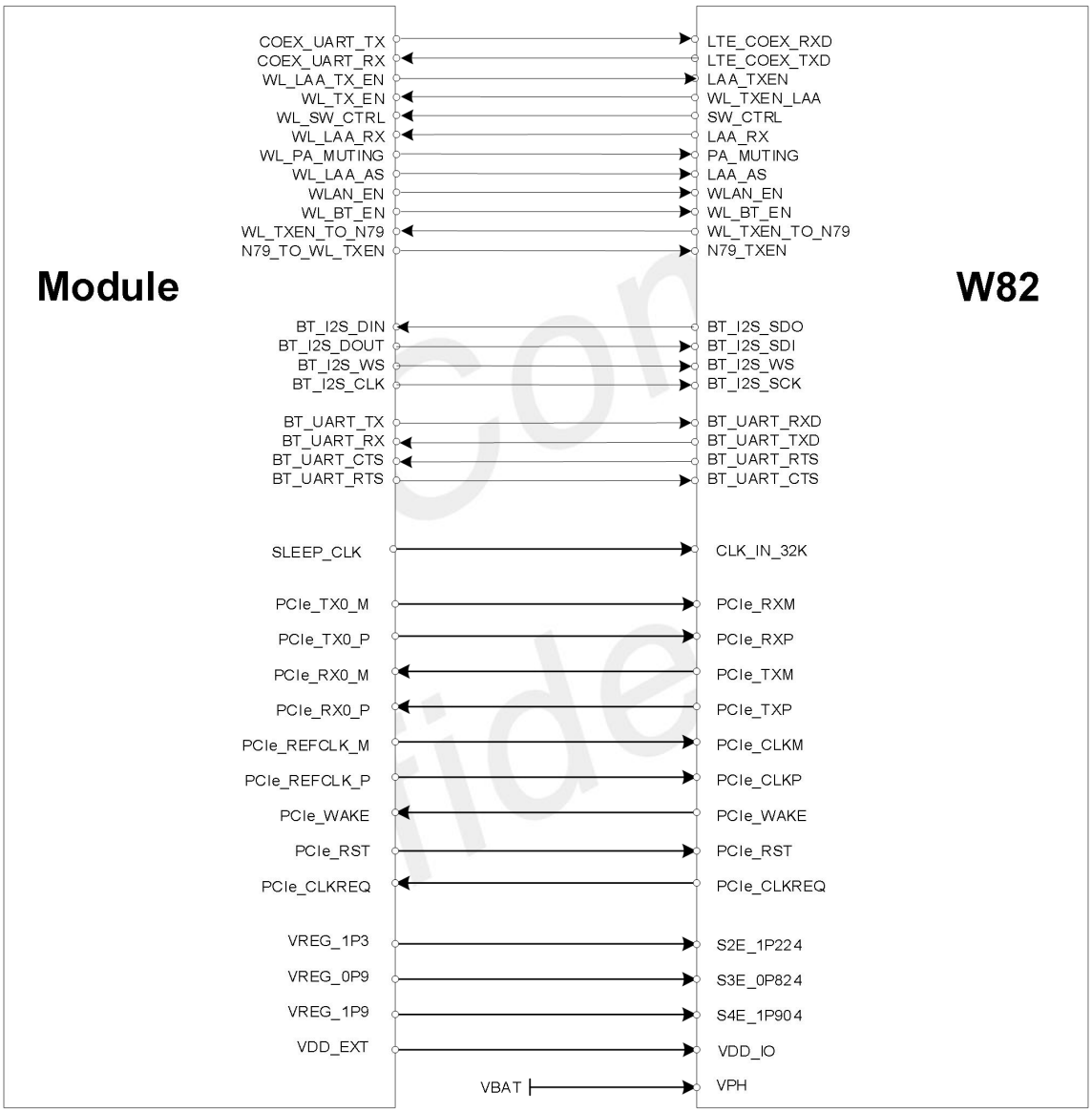

Figure 37: SIM8260A and W82 connect circuit

Table 43: Definition of WLAN/BT interface

Pin name	Pin no.	Electrical description	description	Comment
WL_SW_CTRL	K49	DO	W82 switch control	If unused, please keep open
SDX_TO_WL_CTI	M49	DO	W82 GPIO	

WL_TO_SDX_CTI	L47	DI	W82 GPIO	
WL_PA_MUTING	H45	DO	WLAN XFEM control for PA mute	
SLEEP_CLK	J51	DO	Sleep clock output for W82 only	
BT_EN	N51	DO	W82 BT enable	If unused, please PD 10k
WL_EN	K45	DO	WLAN enable	
WL_LAA_RX	J47	DI	WLAN XFEM control for LAA receiver	SIM8260C not support LAA, unused please PD 10k
WL_LAA_AS_EN	L51	DO	WLAN LAA AS enable	
COEX_UART_TXD	BA7	DO	LTE&WLAN coexistence data transmit	LTE coexistence signals
COEX_UART_RXD	BA9	DI	LTE&WLAN coexistence data receive	
WL_TXEN_TO_N79	BA37	DI	From Module N79 to the W82	SIM8260E/A, unused, please keep open
N79_TO_WL_TXEN	BA29	DO	From the W82 to Module N79	
WL_LAA_TX_EN	R51	DO	From Module to the W82	SIM8260C/E/A not supported, unused please keep open
WL_TX_EN	AY14	DI	From the W82 to Module	SIM8260C not supported.

NOTE

- For more details about WIFI function, please refer to Document [20] in the appendix.
- BT is under development.

W82 performance as follows, details please refer to the W82 hardware design.

- Compliant with IEEE 802.11a/b/g/n/ac/ax.
- Supports 2x2 Multi-User Multiple-Input Multiple-Output (MU-MIMO.)
- Tri band 2.4G/5G/6G chains.
- 20/40 MHz channel bandwidth for 2.4 GHz and 20/40/80/160 MHz channel bandwidth for 5 GHz and 6 GHz
- Dynamic Frequency Selection (DFS, radar detection).
- Offloading traffic for minimal host utilization at 11ac/ax speeds.
- Low power PCIe interface.
- Support BT 5.2

3.15 PM7250B Interface

SIM8260A supports PM7250B interface, customers can use PM7250B to manage the charge of the module. The reference circuits as follows:

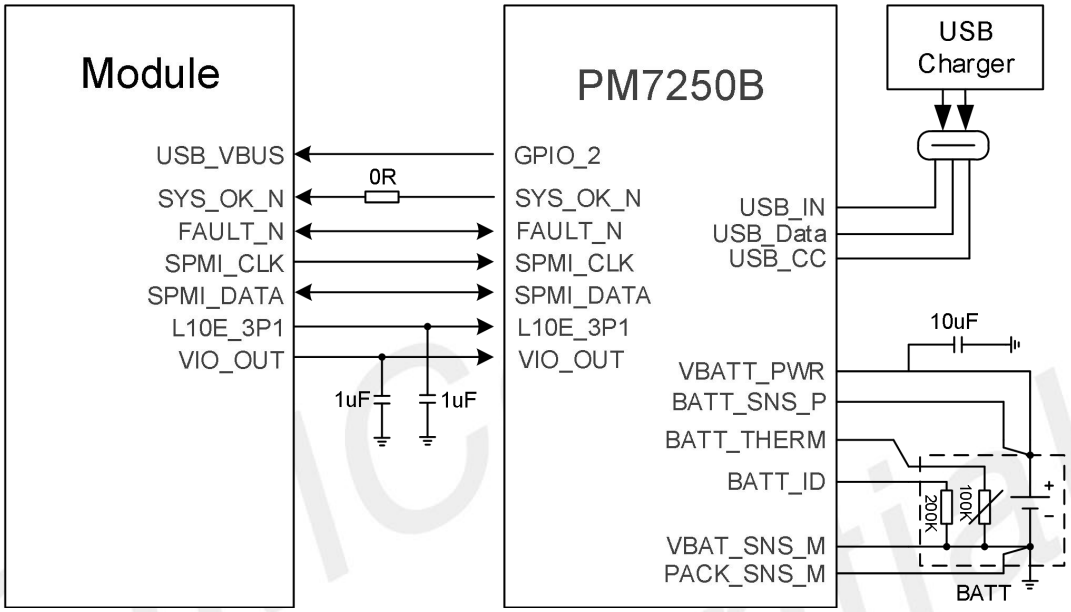

Figure 38: PM7250B interface diagram circuit

Table 44: Definition of PM7250B interface

Pin name	Pin no.	Pin characteristics	Functional description	Comment
USB_VBUS	C9	AI	USB VBUS detection	Not support charge
CHG_SYS_OK	C43	DI	When charger input is inserted PM7250B output signal to PMU. When the charging chip is not used, this pin can be connected to GND to realize the power-on function	
FAULT_N	B44	DIO	Used to send/receive the fault condition across all PMICs in the chipset	
SPMI_CLK	A47	DO	SPMI communication bus clock signal	Required 50Ω impedance
SPMI_DATA	B46	DIO	SPMI communication bus data signal	
L10E_3P1	C41	PO	Output power supply for PM7250B USB PD-PHY and USB switch	
VIO_OUT	D42	PO	Output power for PM7250B IO circuit	

PM7250B performance as follows: please refer to SIM8260A reference design for details

- Supports USB Type-C specification Rev. 3.1 and USB power delivery specification Rev. 3.0.
- Supports Qualcomm Quick Charge 2.0, Quick Charge 3.0, and Quick Charge 4.0* technology.

NOTE

- “*“means Indicates to be updated.
- For more details about charge function, please refer to Document [17] in the appendix.

SPMI interface layout guidelines:

- Require single-ended trace impedance is 50Ω ±10%.
- CLK to DATA length mismatch is less than 0.5mm.
- Bus capacitance load is less than 10PF.
- Gap to other signals keeps 3xline width.
- Gap clock-to-data keeps 2xline width.
- Trace routes away from sensitive signals.
- Maximum PCB trace length can’t exceed 50mm out of the module， The shorter trace and better.

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3.16 GPIOs Interface

The follow pins of SIM8260A can be used as GPIO function, If the customer does not want to use the GPIO default configuration, they can choose the Alternate option in the table below, but they need to contact our company for confirmation.

Table 45: GPIO list

PIN Name	PIN No.	GPIO	Default function	Alternate function 1	Alternate function 2	interrupt
I2S_WS	T3	GPIO12	I2S_WS	PCM_SYNC		✓
I2S_DIN	R1	GPIO13	I2S_DIN	PCM_DIN		✓
I2S_DOUT	N1	GPIO14	I2S_DOUT	PCM_DOUT		✓
I2S_CLK	P3	GPIO15	I2S_SCK	PCM_CLK		✓
BT_I2S_WS	G1	GPIO16	BT_I2S_WS	SPI_MOSI	UART_TX	✓
BT_I2S_DIN	M3	GPIO17	BT_I2S_DIN	SPI_MISO	UART_RX	✓
BT_I2S_DOUT	K3	GPIO18	BT_I2S_DOUT	SPI_CS_N	UART_CTS	✓
BT_I2S_CLK	J1	GPIO19	BT_I2S_SCK	SPI_CLK	UART_RTS	✓
UART1_TXD	AB3	GPIO48	UART1_TX			✓
UART1_RXD	AD3	GPIO49	UART1_RX			✓
UART1_CTS	AA1	GPIO80	UART1_CTS		SPI_MOSI	
UART1_RTS	AC1	GPIO81	UART1_RTS		SPI_MISO	✓
BT_UART_TXD	T7	GPIO63	BT_UART_TX			
BT_UART_RXD	V7	GPIO64	BT_UART_RX			✓
BT_UART_CTS	R5	GPIO65	BT_UART_CTS	I2C_SDA		✓
BT_UART_RTS	U5	GPIO66	BT_UART_RTS	I2C_SCL		
SPI_MOSI	D14	GPIO4	SPI_MOSI		UART_TX	
SPI_MISO	D16	GPIO5	SPI_MISO		UART_RX	✓
SPI_CS_N	D18	GPIO6	SPI_CS	I2C_SDA	UART_CTS	✓
SPI_CLK	D20	GPIO7	SPI_CLK	I2C_SCL	UART_RTS	
GPIO107	U1	GPIO107	GPIO107			
GPIO82	V3	GPIO82	GPIO82	I2C_SDA	SPI_CS_N	
GPIO83	Y3	GPIO83	GPIO83	I2C_SCL	SPI_CLK	✓
GPIO31	C29	GPIO31	GPIO31			
TDD_SYNC_PPS	AW21	GPIO32	TDD_SYNC_PPS			✓
GPIO47	AE5	GPIO47	ETH_1_INTN_WOL			✓
W_DISABLE	AG1	GPIO86	W_DISABLE			✓
GPIO88	AG5	GPIO88	ETH_0_INTN_WOL			✓

GPIO92	AK7	GPIO92	GPIO92			
GPIO96	AM7	GPIO96	GPIO96			✓
SLEEP_OUT	AF3	GPIO97	SLEEP_OUT			
GPIO102	D36	GPIO102	GPIO102			
GPIO105	D38	GPIO105	GPIO105			
GPIO106	AY10	GPIO106	GPIO106			
PMU_GPIO6	AP7	PMU_GPIO6	PMU_GPIO6			
STATUS	AJ5	PMU_GPIO13	STATUS			
NET_STATUS	AE1	PMU_GPIO14	NET_STATUS			

NOTE

- "✓" means the GPIO support interrupt function.
- GPIO default state is B-PD, GPIO66 cannot be pulled up externally.
- UART1 is used as AT command by default, it is not recommended to be used for other functions

3.17 Network Status

The NET_STATUS pin is used to control network status LED, its reference circuit is shown in the following figure.

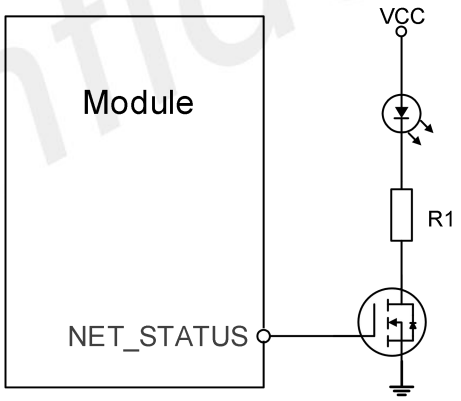

Figure 39: NET_STATUS reference circuit

Table 46: Definition of NET_STATUS pin

Pin Name	Pin No.	Electrical Description		Description	Comments
NET_STATUS	AE1	DO	P3	Indicate network activity status of the module	

NOTE

- The value of the resistor R1 depends on the LED characteristics.

The timing parameters are shown in the following table.

Table 47: NET_STATUS pin status

NET_STATUS pin status	Module status
Always On	Searching network; call connection (including 5G, VOLTE)
100ms ON, 100ms OFF	5G Data transmitting; 5G registered on network
200ms ON, 200ms OFF	3G/4G Data transmitting; 4G registered on network
800ms ON, 800ms OFF	3G registered on network
OFF	Power off; in sleep mode

3.18 Flight Mode Control

The W_DISABLE pin can be used to control SIM8260A to enter or exit the flight mode. In flight mode, the RF circuit is closed to prevent interference with other equipment's and minimize current consumption. Its reference circuit is shown in the following figure.

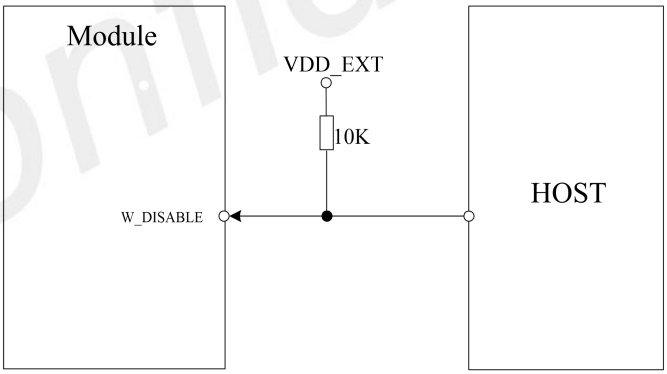

Figure 40: W_DISABLE pin reference circuit

Table 48: Definition of W_DISABLE pin

Pin Name	Pin No.	Electrical Description		Description	Comments
W_DISABLE	AG1	DI	P3	Flight mode control input active low	

Table 49: W_DISABLE pin status

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W_DISABLE pin status	Module operation
Input low level	Flight mode: RF is disabled
Input high level	AT+CFUN=0: Minimal functional mode (SIM card function is off) AT+CFUN=4: Flight mode (SIM card function is on) AT+CFUN=1: RF is enabled (Default)

Both W_DISABLE and AT commands can change the working mode of the module, but W_DISABLE has a higher priority. When W_DISABLE is low, it is forced to enter flight mode. When W_DISABLE is high, it can enter different working modes by sending AT commands.

3.19 TDD_SYNC_PPS

SIM8260A support TDD_SYNC_PPS signal, it can generate pulse use for indication NSA and SA sub6 the beginning frame flag of DL-UL, the pin level is 1.8V, customers can direct connect this pin to TDD synchronous input circuit.
Recommended reference circuit is shown in the following figure.

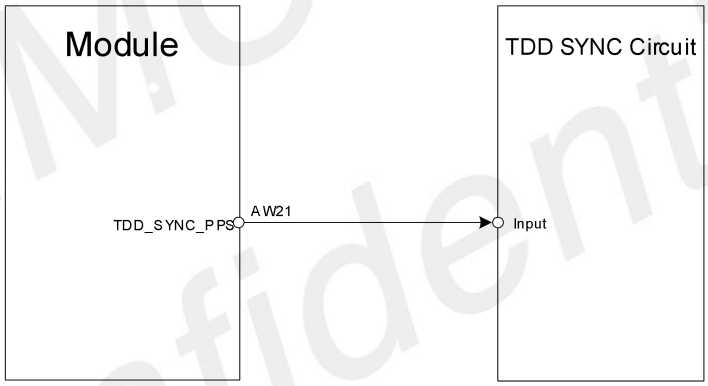

Figure 41: TDD_SYNC_PPS pin reference circuit

Table 50: Definition of TDD_SYNC_PPS pin

Pin name	Pin no.	Electrical description	Description	Comments
TDD_SYNC_PPS	AW21	DO	1. It can generate pulse use for indication NSA and SA sub6 the beginning frame flag of DL-UL 2. The TDD_SYNC_PPS pin also can be configured GPS_1PPS signal output by software	1.8V voltage domain. The TDD_SYNC_PPS and GPS_1PPS function can't be used at the same time.

NOTE

- The TDD_SYNC_PPS pin also can be configured GPS_1PPS signal output by software, the

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TDD_SYNC_PPS and GPS_1PPS function can't be used at the same time.

The following is TDD_SYNC_PPS signal design guidelines：

- This signal trace should be treated as a data transmission line, required impedance is 50 Ω.
- This signal trace should as short as possible and cannot exceed 40mm out of the module.
- This signal trace should far away from RF, power and high-speed signals.
- This signal trace should be protected completely by GND.
- The rising slew rate is no poor than 3ns, falling slew rate is no poor than 5ns, even with default lowest drive strength (2mA) being selected.

3.20 Antenna Control Interface*

ANT_CTL [0:1] and RFFE0 signals are used for tunable antenna control and should be routed to an appropriate antenna control circuitry.
The following table are the definitions for antenna control interfaces.

Table 51: Definition of antenna control interface through GPIOs

Pin Name	Pin No.	Electrical Description	Description	Comments
RFFE0_CLK	BA11	DO	Antenna tuner MIPI CLK	1.8V voltage domain. If unused, please keep open
RFFE0_DATA	BA13	DIO	Antenna tuner MIPI DATA	
ANT_CTRL0	BA15	DO	Antenna tuner control0	
ANT_CTRL1	AY16	DO	Antenna tuner control1	

NOTE

- "*" means under development, for details please contact SIMCom support teams.
- The RFFE0 signals are multiplexed with ANTCTL2 and ANTCTL3.

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4 Antenna Interfaces

SIM8260A provides four antennas for 3G/4G/5G and GNSS. The antenna ports have an RF impedance of 50Ω.

4.1 Antenna Definitions

For detailed designs about antenna and if there is a requirement for minimum antennas, please refer to the antenna design guide “SIM8200 Series_LGA Antenna Port Mapping and Design Guide”.

Table 56: The Antenna port definitions of A SIM8260A

Frequency band		Antenna	ANT0	ANT1	ANT2	ANT3	GNSS
3G/4G/5G 3G/4G/5G 5G	LB MHB n41/n77/n78/n79	TX0/DRX TX0/PRX TX0/DRX_MIMO	✓				
3G/4G/5G 5G 4G	MHB n77/n78/n79 LAA	DRX_MIMO DRX DRX		✓			
3G/4G/5G 5G 4G GNSS	MHB n77/n78/n79 LAA L1	PRX_MIMO PRX_MIMO PRX			✓		
3G/4G/5G 3G/4G/5G 5G	LB MHB n41/n77/n78/n79	TX1/PRX TX1/DRX TX1/PRX				✓	
GNSS	L1 L5*						✓

※ NOTE

- 4G LB only support 2*2 DL-MIMO, the detailed information reference document [14].
- “*” means not supported by default.

4.1.1 3G/4G/5G Operating Frequency

Table 57: 3G/4G band frequency

Frequency band	Uplink (UL)	Downlink (DL)	Duplex mode
WCDMA B2	1850 MHz ~ 1910 MHz	1930 MHz ~ 1990 MHz	WCDMA
WCDMA B4	1710 MHz ~ 1755 MHz	2110 MHz ~ 2155 MHz	WCDMA
WCDMA B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	WCDMA
LTE B2	1850 MHz ~ 1910 MHz	1930 MHz ~ 1990 MHz	FDD
LTE B4	1710 MHz ~ 1755 MHz	2110 MHz ~ 2155 MHz	FDD
LTE B5	824 MHz ~ 849 MHz	869 MHz ~ 894MHz	FDD
LTE B7	2500 MHz ~ 2570MHz	2620 MHz ~ 2690MHz	FDD
LTE B12	698 MHz ~ 716 MHz	728MHz ~ 746 MHz	FDD
LTE B13	777 MHz ~ 787 MHz	746 MHz ~ 756 MHz	FDD
LTE B14	788 MHz ~ 798 MHz	758 MHz ~ 768 MHz	FDD
LTE B17	704 MHz ~ 716 MHz	734 MHz ~746 MHz	FDD
LTE B25	1850 MHz ~ 1915MHz	1930 MHz ~ 1995MHz	FDD
LTE B26	814 MHz ~ 849 MHz	859 MHz ~ 894 MHz	FDD
LTE B66	1710 MHz ~ 1780 MHz	2110 MHz ~ 2220 MHz	FDD
LTE B71	663 MHz ~ 698 MHz	617 MHz ~ 652 MHz	FDD
LTE B41	2496 MHz ~ 2690 MHz	2496 MHz ~ 2690 MHz	TDD

Table 58: NR band frequency

Frequency band	Uplink (UL)	Downlink (DL)	Duplex mode
NR n2	1850MHz ~ 1910MHz	1930MHz ~ 1990MHz	FDD
NR n5	824MHz ~ 849MHz	869MHz ~ 894MHz	FDD
NR n7	2500MHz ~ 2570MHz	2620MHz ~ 2690MHz	FDD
NR n12	698MHz ~ 716MHz	728MHz ~ 746MHz	FDD
NR n14	788MHz ~ 798MHz	758MHz ~ 768MHz	FDD
NR n25	1850MHz ~ 1915MHz	1930MHz ~ 1995MHz	FDD
NR n26	814MHz ~ 849MHz	859MHz ~ 894MHz	FDD
NR n41	2496MHz ~ 2690MHz	2496MHz ~ 2690MHz	TDD
NR n48	3550MHz ~ 3700MHz	3550MHz ~ 3700MHz	TDD
NR n66	1710MHz ~ 1780MHz	2110MHz ~ 2220MHz	FDD
NR n71	663 MHz ~ 698 MHz	617 MHz ~ 652 MHz	FDD
NR n77	3300MHz ~ 4200MHz	3300MHz ~ 4200MHz	TDD
NR n78	3300MHz ~ 3800MHz	3300MHz ~ 3800MHz	TDD

4.1.2 GNSS Frequency

The following table shows frequency specification of GNSS antenna interface.

Table 59: GNSS frequency

Type	Frequency
GPS L1/Galileo/QZSS	1575.42±1.023MHz
GPS L5	1176.45±10.23MHz
GLONASS	1597.5~1605.8MHz
BeiDou/Compass	1561.098±2.046MHz

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4.2 Antenna Installation

4.2.1 PCB Layout Guidelines

To avoid interference, minimalize the insertion loss of the RF trace, the PCB should follow below rules:

- The coaxial cable PCB pads, RF antenna connector and other connectors which used to test contact performance of module should place as close as to the module antenna pads.
- The antenna matching network should place to antenna feed port.
- The RF trace should be as short and straight as possible, and do not routing as perpendicular line, we recommend do it as 45° corner trace.
- The RF traces should be grounded.
- RF device should place grounding wire on the nearest grounding surface.
- Between RF trace and below should avoid other signal trace or parallel trace to the RF signal.
- Recommend to more ground vias near the RF traces.

4.2.2 Antenna Tuner

When the device supports 700MHz low frequency(B12\B13\B28), it is recommended to add antenna tuner to improve RF performance. Antenna tuner contains antenna aperture tuner, antenna impedance tuner an d hybrid tuner of the two. Aperture tuning optimizes the total antenna efficiency from the free space of the antenna terminal, and can optimize antenna efficiency across multiple frequency bands. Impedance tuner adjusts the mismatch between the RF front end and the antenna to achieve maximum transmission power. Hybrid tuner combines the advantages of the two to maximize antenna RF performance. Customers can choose according to specific needs, according to the recommendations from the antenna vendor.

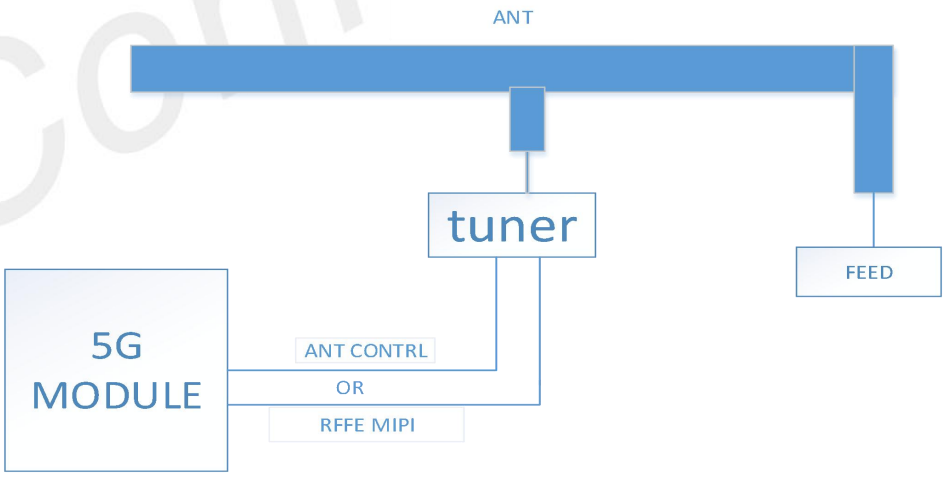

Figure 43: Aperture tuner reference block diagram

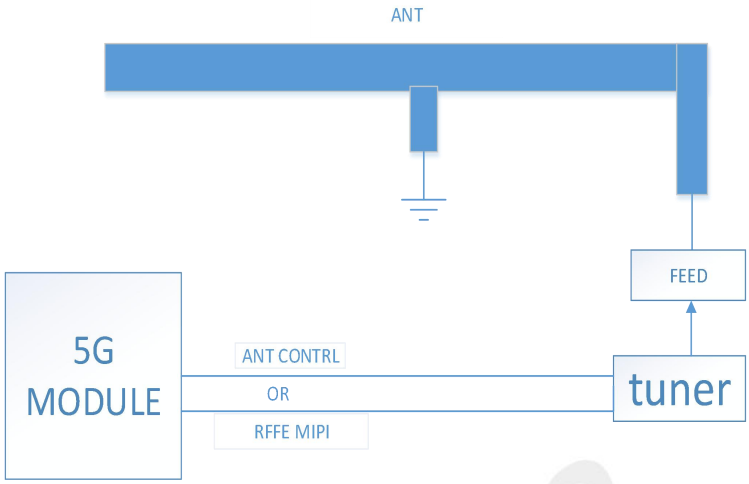

Figure 44: Impedance tuner reference block diagram

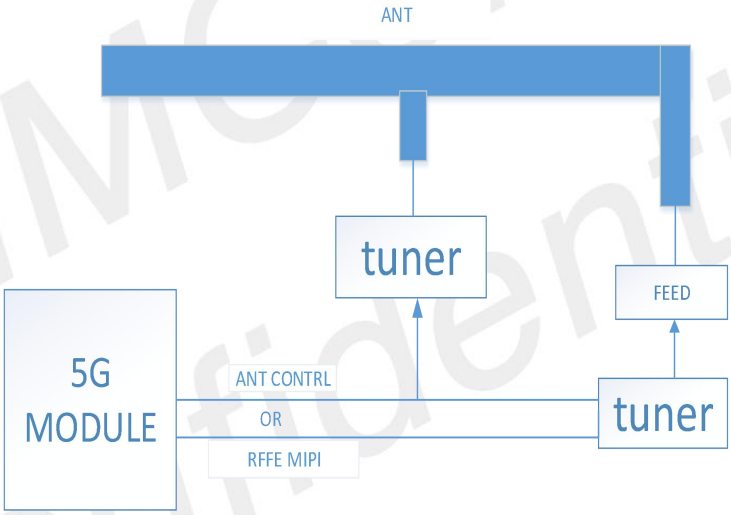

Figure 45: Hybrid tuner reference block diagram

The antenna control Tuner mipi interface of different package modules are as follows.

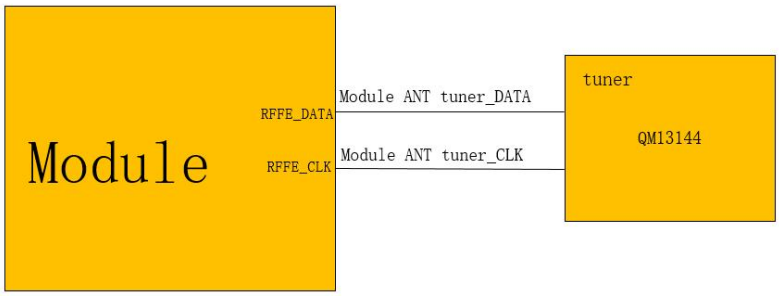

Figure 46: LGA package Tuner mipi interface

NOTE

- When multiple Tuners are needed, pay attention to the distinction of the same device USID under the same group of mipi.
- For details, please refer to the Antenna Tuner Reference Design document and contact SIMCom support teams.

4.2.3 Antenna Requirements

The following table shows the requirements on 3G/4G/5G antennas and GNSS antenna.

Table 60: 3G/4G/5G/GNSS antennas

Parameter	Requirement
Operating Frequency	See Table 7 for each antenna
Direction	Omni Directional
Gain	> -3dBi (Avg)
Impedance	50 Ω
Efficiency	> 50 %
Max. Input Power	50W
VSWR	< 2
Isolation	20dB is preferred
Cable Insertion Loss <1GHz	<1dB
Cable Insertion Loss 1GHz~2.2GHz	<1.5dB
Cable Insertion Loss 2.3GHz~2.7GHz	<2dB
Cable Insertion Loss 3.3GHz~6GHz	<2.5dB

Table 61: GNSS antenna (for dedicated GNSS antenna only)*

Parameter	Requirement
Operating Frequency	L1: 1559~1609MHZ L5: 1166~1187MHz
Direction	Hemisphere, face to sky
Antenna Gain	> 2 dB_{ic}
Impedance	50 Ω
Efficiency	> 50 %
Max. Input Power	50W
VSWR	< 2
Polarization	RHCP or Linear
Noise Figure for Active Antenna	< 1.5

Total Gain for Active Antenna	< 17 dB
Cable Insertion Loss	<1.5dB

NOTE

*: These recommendations are for dedicated GNSS antenna which the application need best of class GNSS tracking performance.

4.2.4 RF Plug Recommendation

SIM8260A is mounted with I-PEX's receptacle RF connectors 20449-001E-03, which size is 2.0mm*2.0mm*0.6mm. The connector dimensions are shown as below.

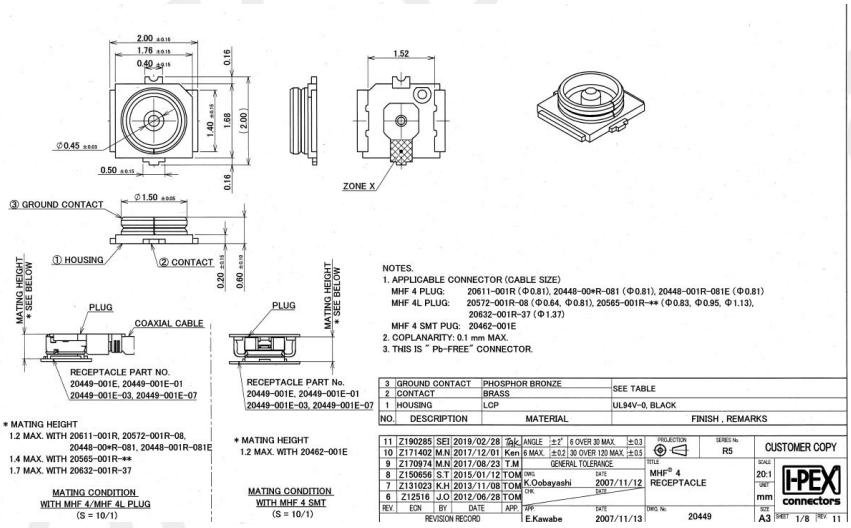

Figure 47: 3D view of 20449-001E-03

The following table shows the RF connector's electrical specifications.

Table 62: Electrical Specifications of 20449-001E-03

Item	Specification
Voltage Rating	60V r.m.s. maximum
Nominal Frequency Range	DC to 6GHz
Nominal Impedance	50Ω
Temperature Rating	-40°C to +90°C
Insulation Resistance	500 MΩ minimum
Withstanding Voltage	No evidence of breakdown

Initial Contact Resistance (Without conductor resistance)	Center contact 20.0mΩmax. Outer contact 20.0mΩmax.
Voltage Standing Wave Ratio (V.S.W.R.)	Meet the requirements of 1.3 max. (DC~3GHz) 1.45 max. (3GHz~6GHz)

To get best RF performance, the RF plug connector should be designed to match the receptacle 20449-001E-03, and the parts come from I-PEX is the recommended.

The following is the mechanical information of the I-PEX's RF coaxial cable GLJ-RH120-1901 for reference, for further technical support, the customer could visit the I-PEX's website or contact the local sales team.

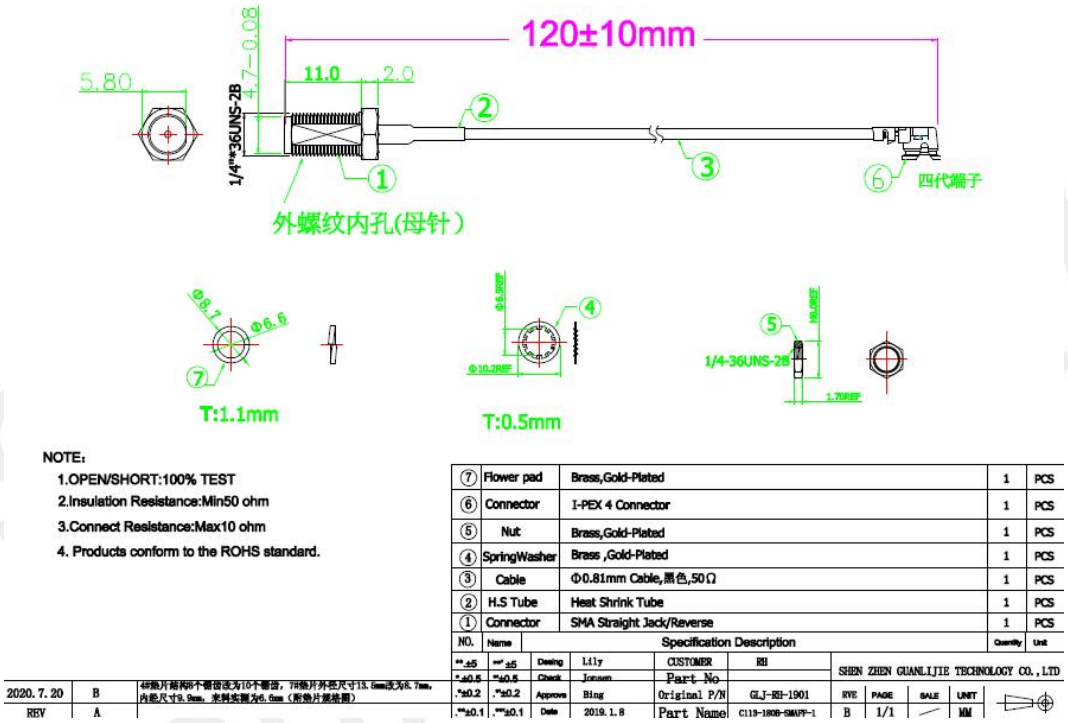

Figure 48: 3D view of 20449-001E-0

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Absolute maximum rating for digital and analog pins of module are listed in the following table:

Table 63: Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT[1] pins	-	-	4.8	V
Voltage at USB_VBUS	-	-	6	V
Voltage at PWRKEY	-	-	2.1	V
Voltage at RESIN_N	-	-	1.9	V
Voltage at digital pins (GPIO, I2C, UART, I2S)	-	-	2.1	V
Voltage at digital pins (U)SIM	-	-	3.05	V

NOTE

1.The VBAT include VBAT_BB and VBAT_RF pins.

5.2 Operating Conditions

Table 64: VBAT recommended operating ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT[1] pins	3.3	3.8	4.4	V

NOTE

1. The VBAT include VBAT_BB and VBAT_RF pins.

Table 65: 1.8V digital I/O characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage	1.17	-	2.1	V
V_{IL}	Low-level input voltage	0	-	0.63	V
V_{OH}	High-level output voltage	1.35	-	1.8	V
V_{OL}	Low-level output voltage	0	-	0.45	V
I_{OZH}	High-level, tri-state leakage current (No pull-down resistor)	-	-	1	uA
I_{OZL}	Low-level, tri-state leakage current (No pull up resistor)	-1	-	-	uA
I_{IH}	Input high leakage current (No pull-down resistor)	-	-	1	uA
I_{IL}	Input low leakage current (no pull up resistor)	-1	-	-	uA

NOTE

- These parameters are for digital interface pins, such as UART, I2C, I2S, SPI, and GPIOs (SIM_DET, SD_DET).

Table 66: Operating temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature (3GPP compliant)	-30	-	70	°C
Extended operation temperature	-40	-	85	°C
Storage temperature	-40	-	90	°C

5.3 Operating Mode

5.3.1 Operating Mode Definition

The table below summarizes the various operating modes of module.

Table 67: Operating mode definition

Mode		Function
Normal operation	UMTS/LTE/5G Sleep	AT command “AT+CSCLK=1” can be used to set the module to a sleep mode. In this case, the current consumption of module will be reduced to a very low level and the module can still receive paging message and SMS.
	UMTS/LTE/5G Idle	Software is active. Module is registered to the network and ready to communicate.
	UMTS/LTE/5G Talk	Connection between two subscribers is in progress. In this case, the power consumption depends on network settings such as DTX off/on, FR/EFR/HR, hopping sequences and antenna.
	UMTS/LTE/5G Standby	Module is ready for data transmission, but no data is currently sent or received. In this case, power consumption depends on network settings.
	UMTS/LTE/5G Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e. g. power control level); uplink/downlink data rates, etc.
Minimum functionality mode		AT command “AT+CFUN=0” can be used to set the Module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the Module will not work and the (U)SIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode		AT command “AT+CFUN=4” or pulling down the W_disable1# pin can be used to set the Module to flight mode without removing the power supply. In this mode, the RF part of the Module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Power off		Normally module will go into power off mode by sending the AT command “AT+CPOF” or pull down the FUL_CARD_POWER_OFF# pin. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are not accessible.

5.3.2 Sleep Mode

In sleep mode, the current consumption of module will be reduced to a very low level.

Several hardware and software conditions must be satisfied in order to let module enter sleep mode:
1. UART condition
2. USB condition
3. Software condition

NOTE

- Before designing, pay attention to how to realize sleeping/waking function.

5.3.3 Minimum Functionality Mode and Flight Mode

Minimum functionality mode ceases a majority function of Module, in order to minimizing the power consumption. This mode is set by the AT command which provides a choice of 3 different functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If module has been set to minimum functionality mode, the RF (U)SIM card function will be closed while the serial port and USB are still available.

If module has been set to flight mode, the RF function will be closed, while the (U)SIM card, the serial port and USB are still available.

When module is in minimum functionality or flight mode, it can return to full functionality by the AT command “AT+CFUN=1”.

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5.4 Current Consumption

The current consumptions are listed in the follows table.

Table 68: Current consumption on VBAT pins (VBAT=3.8V)

Description	Condition.	Typical	Unit
Power off mode	Power off	135*	uA
GNSS mode	(AT+CFUN=0, connection USB)	TBD	mA
Sleep mode (GNSS off, without connection USB)	WCDMA(AT+CFUN=0)	2.6	mA
	WCDMA DRX=1.28s	4.5	mA
	WCDMA DRX=2.56s	3.5	mA
	LTE-FDD(AT+CFUN=0)	2.6	mA
	LTE-FDD DRX=0.32s	10.5	mA
	LTE-FDD DRX=0.64s	6.5	mA
	LTE-FDD DRX=1.28s	4.5	mA
	LTE-FDD DRX=2.56s	4	mA
	LTE-TDD(AT+CFUN=0)	2.6	mA
	LTE-TDD DRX=0.32s	10.5	mA
	LTE-TDD DRX=0.64s	6.5	mA
	LTE-TDD DRX=1.28s	4.5	mA
	LTE-TDD DRX=2.56s	4	mA
	NR* (AT+CFUN=0)	2.6	mA
	NR DRX=0.32s	10.5	mA
	NR DRX=0.64s	6.5	mA
	NR DRX=1.28s	4.5	mA
	NR DRX=2.56s	4	mA
Idle mode (GNSS off, without connection USB)	WCDMA	28	mA
	LTE FDD	28	mA
	LTE TDD	28	mA
	5G SA	28	mA
HSDPA data*			
WCDMA B2	Max 865mA		
WCDMA B4	Max 865mA		
WCDMA B5	Max 865mA		
LTE data			
LTE-FDD B2	Max 895mA		
LTE-FDD B4	Max 895mA		
LTE-FDD B5	Max 765mA		
LTE-FDD B7	Max 945mA		

LTE-FDD B12	Max 765mA	
LTE-FDD B13	Max 765mA	
LTE-FDD B14	Max 765mA	
LTE-FDD B17	Max 765mA	
LTE-FDD B25	Max 895mA	
LTE-FDD B26	Max 765mA	
LTE-FDD B66	Max 895mA	
LTE-FDD B71	Max 765mA	
LTE-TDD B41	Max 955mA	
5G NR data		
5G n2	Max 960mA	
5G n5	Max 765mA	
5G n7	Max 985mA	
5G n12	Max 765mA	
5G n14	Max 765mA	
5G n25	Max 960mA	
5G n26	Max 765mA	
5G n41	Max 1400mA	
5G n48	Max 800mA	
5G n66	Max 960mA	
5G n71	Max 765mA	
5G n77	Max 1000mA	
5G n78	Max 1000mA	

NOTE

- The VBAT include VBAT_BB and VBAT_RF pins.
- The current consumption of the above table only for reference, please refer to actual current consumption.
- Use BAND N78 for 5G NR current test
- RF current consumption data is based on maximum power 22±0.5dBm test for PC3 and 26±1dBm test for PC2

5.5 RF Output Power

The RF output power is shown in the following table.

Table 69: Conducted output power

WCDMA	B2	RMC	QPSK	23.1±1
		HSDPA	QPSK	22.1±1
		HSUPA（Subtest1）	QPSK/16QAM	20±1
		HSUPA（Subtest2）	QPSK/16QAM	21±1
		HSUPA（Subtest3）	QPSK/16QAM	17.2±1
		HSUPA（Subtest4）	QPSK/16QAM	22.5±1
		HSUPA(Subtest5)1852.4/1907.6	QPSK/16QAM	17±1
		HSUPA（Subtest5）1880	QPSK/16QAM	21.9±1
	B4	RMC	QPSK	23.2±1
		HSDPA	QPSK	22.5±1
		HSUPA	QPSK/16QAM	22.5±1
	B5	RMC	QPSK	24.3±1
		HSDPA	QPSK	23.5±1
		HSUPA（Subtest1/2）	QPSK/16QAM	22±1
		HSUPA（Subtest3）	QPSK/16QAM	19±1
		HSUPA（Subtest4）	QPSK/16QAM	23.5±1
		HSUPA（Subtest5）	QPSK/16QAM	18±1
LTE	B2	1.4/3/5/10/15/20MHz	QPSK/16QAM	27.4±1
	B4	1.4/3/5/10/15/20MHz	QPSK/16QAM	27.8±1
	B5	1.4/3MHz	QPSK/16QAM	28.3±1
		5/10MHz	QPSK/16QAM	28.4±1
	B7	5/10/15/20MHz	QPSK/16QAM	26.7±1
	B12	1.4/3/5/10MHz	QPSK/16QAM	27.9±1
	B13	5/10MHz	QPSK/16QAM	28.3±1
	B14	5/10MHz	QPSK/16QAM	28±1
	B17	5/10MHz	QPSK/16QAM	28±1
	B25	1.4/3/5/10/15/20MHz	QPSK/16QAM	27.5±1
	B26(Part22)	1.4/3/5/10MHz	QPSK/16QAM	28±1
	B26(Part90)	1.4/3/5/10MHz	QPSK/16QAM	26.5±1
	B41	5/10/15/20MHz	QPSK	24.2±1
		5/10/15/20MHz	16QAM	23.3±1
	B66	1.4/3/5/10/15/20MHz	QPSK	24.2±1
		1.4/3/5/10/15/20MHz	16QAM	23.3±1
	B71	5/10/15/20MHz	QPSK	26±1
		5MHz	16QAM	26.2±1
		10/15MHz(L/M)	16QAM	26.1±1
		10/15MHz(H)	16QAM	25.2±1
		20MHz	16QAM	25.2±1

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	CA_41C	5+20/10+5/10+20/15+20/15+15/15+20/20+5/20+10/20+15/20+20 MHz	16QAM	24.3±1
		5+20/10+5/10+20/15+20/15+15/15+20/20+5/20+10/20+15/20+20 MHz	64QAM	23.4±1
		5+20/10+5/10+20/15+20/15+15/15+20/20+5/20+10/20+15/20+20 MHz	256QAM	20.3±1
		5+20/10+5/10+20/15+20/15+15MHz	QPSK	24.8±1
		15+20/20+5/20+10/20+15/20+20 MHz(Size1)	QPSK	25.3±1
		15+20/20+5/20+10/20+15/20+20 MHz	QPSK	23.5±1
	CA_2A-4A	1.4/3/5/10/15/20MHz PCC	QPSK	21.5±1
		1.4/3/5/10/15/20MHz PCC	Q16	21.6±1
		1.4/3/5/10/15/20MHz PCC	Q64	21.6±1
		1.4/3/5/10/15/20MHz PCC	Q256	18.8±1
		1.4/3/5/10/15/20MHz SCC	QPSK	21.2±1
		1.4/3/5/10/15/21MHz SCC	Q16	21.2±1
		1.4/3/5/10/15/22MHz SCC	Q64	21.3±1
		1.4/3/5/10/15/23MHz SCC	Q256	18.4±1
	CA_2A-12A	5/10/15/20MHz PCC	QPSK	20.6±1
		5/10/15/20MHz PCC	Q16	20.6±1
		5/10/15/20MHz PCC	Q64	20.3±1
		5/10/15/20MHz PCC	Q256	17.6±1
		5/10/15/20MHz SCC	QPSK	21.7±1
		5/10/15/20MHz SCC	Q16	21.8±1
		5/10/15/20MHz SCC	Q64	21.4±1
		5/10/15/20MHz SCC	Q256	18.5±1
	CA_2A-66A	1.4/3/5/10/15/20MHz PCC	QPSK	20.3±1
		1.4/3/5/10/15/20MHz PCC	Q16	20.4±1
		1.4/3/5/10/15/20MHz PCC	Q64	20.4±1
		1.4/3/5/10/15/20MHz PCC	Q256	17.5±1
		5/10/15/20MHz SCC	QPSK	19.9±1
		5/10/15/20MHz SCC	Q16	19.8±1
		5/10/15/20MHz SCC	Q64	20.0±1
		5/10/15/20MHz SCC	Q256	17.1±1
	CA_12A-66A	3/5/15/10MHz PCC	QPSK	21.7±1
		3/5/15/10MHz PCC	Q16	21.8±1
		3/5/15/10MHz PCC	Q64	21.3±1
		3/5/15/10MHz PCC	Q256	18.4±1
		1.4/3/5/10/15/20MHz SCC	QPSK	20.8±1

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		1.4/3/5/10/15/21MHz SCC	Q16	20.7±1
		1.4/3/5/10/15/22MHz SCC	Q64	20.4±1
		1.4/3/5/10/15/23MHz SCC	Q256	17.4±1
5G	n2,DC_7A_n2A	1852.5	QPSK	22.6±1
		1860	QPSK	22.71±1
		1900	QPSK	22.45±1
		1880	QPSK	22.56±1
		1907.5	QPSK	22.2±1
		1855	QPSK	22.59±1
		1905	QPSK	22.29±1
		1902.5	QPSK	22.42±1
		1857.5	QPSK	22.7±1
		1852.5	16QAM	22.4±1
		1855	16QAM	22.6±1
		1857.5 Outer_Full	16QAM	21.6±1
		1857.5	16QAM	22.7±1
		1860	16QAM	22.63±1
		1880	16QAM	21.6±1
		1902.5 Outer_Full	16QAM	21.6±1
		1902.5	16QAM	22.6±1
		1905	16QAM	22.4±1
		1907.5	16QAM	22±1
			64QAM	21.6±1
			256QAM	21.3±1
			pi/2 BPSK	22.9±1
	B66-n5,DC_7A_n5A,DC_66A_n5A,DC_7A-66A-66A_n5A	Inner_Full	QPSK	23.3±1
		Outer_Full CP	QPSK	21.3±1
		Outer_Full DFT	QPSK	23.4±1
		Edge_1RB_Left CP	QPSK	21.4±1
		Edge_1RB_Left DFT	QPSK	23.4±1
		Edge_1RB_Right CP	QPSK	21.2±1
		Edge_1RB_Right DFT	QPSK	23.3±1
		Inner_Full	16QAM	21.8±1
		Outer_Full	16QAM	21.82±1
		Edge_1RB_Left	16QAM	22.5±1
		Edge_1RB_Right	16QAM	22.2±1
		Inner_Full	64QAM	23.4±1
		Outer_Full	64QAM	22.35±1
		Edge_1RB_Left CP	64QAM	20.7±1
		Edge_1RB_Left DFT	64QAM	21.9±1

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		Edge_1RB_Right CP	64QAM	20.7±1
		Edge_1RB_Right DFT	64QAM	21.7±1
		Inner_Full	256QAM	21.82±1
		Outer_Full	256QAM	21.9±1
		Edge_1RB_Left	256QAM	21.7±1
		Edge_1RB_Right	256QAM	21.3±1
			pi/2 BPSK	23.3±1
	n7,DC_2A_n7A,DC_5A_n7A,DC_66A_n7A,DC_5A-7A_n7A,DC_66A-66A_n7A,DC_7C-66A-66A_n5A	inter_Full CP	QPSK	23.0±1
		inter_Full DFT (2510MHz)	QPSK	20.9±1
		inter_Full DFT	QPSK	23.3±1
		Outer_Full CP	QPSK	21.4±1
		Outer_Full DFT	QPSK	23.4±1
		Edge_1RB_Left CP	QPSK	21.5±1
		Edge_1RB_Left DFT	QPSK	21.0±1
		Edge_1RB_Left DFT 2510M	QPSK	23.5±1
		Edge_1RB_Right CP	QPSK	21.6±1
		Edge_1RB_Right DFT	QPSK	23.3±1
		Inner_Full	16QAM	23.5±1
		Outer_Full CP	16QAM	21.5±1
		Outer_Full DFT	16QAM	22.4±1
		Edge_1RB_Left CP	16QAM	21.5±1
		Edge_1RB_Left DFT	16QAM	22.5±1
		Edge_1RB_Right CP	16QAM	21.6±1
		Edge_1RB_Right DFT	16QAM	22.5±1
			64QAM	22.0±1
			256QAM	22.0±1
		Inner_Full 2510M	pi/2 BPSK	20.9±1
		Inner_Full	pi/2 BPSK	23.4±1
		Outer_Full 2510M	pi/2 BPSK	20.9±1
		Outer_Full	pi/2 BPSK	23.4±1
		Edge_1RB_Left	pi/2 BPSK	21.5±1
		Edge_1RB_Right	pi/2 BPSK	21.5±1
	n12	CP	QPSK	21.4±1
		DFT	QPSK	22.0±1
		CP	16QAM	20.9±1
		DFT	16QAM	22.0±1
		CP	64QAM	19.4±1
		DFT	64QAM	20.5±1

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		CP	256QAM	19.5±1
		Outer_Full DFT 707.5M	256QAM	20.5±1
		Outer_Full DFT	256QAM	18.3±1
		Inner_Full DFT	256QAM	20.5±1
		Edge_1RB_Left DFT 707.5M	256QAM	18.1±1
		Edge_1RB_Left DFT	256QAM	20.1±1
		Edge_1RB_RightDFT	256QAM	22.0±1
			pi/2 BPSK	21.5±1
	n14	CP	QPSK	22.4±1
		DFT	QPSK	23.0±1
		CP	16QAM	21.9±1
		DFT	16QAM	22.8±1
			64QAM	21.4±1
			256QAM	21.4±1
			pi/2 BPSK	22.9±1
	B66-n25,DC_66A_n25A,DC_7C_n5A,DC_66A-66A_n5A,DC_2A-66A_n25A,	Inner_Full CP	QPSK	22.0±1
		Outer_Full CP	QPSK	22.3±1
		Edge_1RB_Left CP	QPSK	21.4±1
		Edge_1RB_Right CP	QPSK	21.4±1
		DFT	QPSK	23.3±1
		CP	16QAM	23.03±1
		DFT	16QAM	22.0±1
		CP	64QAM	22.7±1
		DFT	64QAM	21.7±1
		CP	256QAM	20.9±1
		DFT	256QAM	20.9±1
		Outer_Full CP 1882.5MHz	256QAM	19.5±1
	n26PART22	Inner_Full CP	QPSK	22.3±1
		Outer_Full CP	QPSK	20.8±1
		Edge_1RB_Left CP	QPSK	21.0±1
		Edge_1RB_Right CP	QPSK	20.8±1
		DFT	QPSK	23.0±1
		DFT	16QAM	22.7±1
		CP	16QAM	21.8±1
			64QAM	21.4±1
			256QAM	21.4±1
			pi/2 BPSK	22.8±1
	n26 part90	CP	QPSK	22.3±1
		DFT	QPSK	22.9±1

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		Inner_Full CP	16QAM	21.9±1
		Outer_Full CP	16QAM	20.9±1
		Edge_1RB_Left CP	16QAM	20.9±1
		Edge_1RB_Right CP	16QAM	20.9±1
			16QAM	22.8±1
			64QAM	21.3±1
			256QAM	21.4±1
			pi/2 BPSK	22.8±1
	n41,DC_2A_n41A,DC_66A_n41A,DC_2A-2A_n41A,DC_2A-66A_n41A,DC_2C-66A_n41A,DC_2A-2A-66A_n41A	Outer_Full CP	QPSK	23.7±1
		Inner_Full CP	QPSK	25.2±1
		Edge_1RB_Left CP	QPSK	23.3±1
		Edge_1RB_Right CP	QPSK	23.4±1
		Outer_Full DFT	QPSK	25.7±1
		Inner_Full DFT	QPSK	25.5±1
		Edge_1RB_Left DFT	QPSK	23.3±1
		Edge_1RB_Right DFT	QPSK	23.5±1
		Outer_Full CP	16QAM	23.7±1
		Inner_Full CP	16QAM	24.8±1
		Edge_1RB_Left CP	16QAM	23.3±1
		Edge_1RB_Right CP	16QAM	23.5±1
		Outer_Full DFT	16QAM	24.6±1
		Inner_Full DFT	16QAM	25.7±1
		Edge_1RB_Left DFT	16QAM	23.3±1
		Edge_1RB_Right DFT	16QAM	23.5±1
		CP	64QAM	23.3±1
		DFT	64QAM	24.2±1
		Outer_Full CP	256QAM	23.1±1
		Inner_Full CP	256QAM	23.3±1
		Edge_1RB_Left CP 2506.02MHz	256QAM	19.5±1
		Edge_1RB_Left CP	256QAM	23.0±1
		Edge_1RB_Right CP	256QAM	23.1±1
		Outer_Full DFT	256QAM	25.2±1
		Inner_Full DFT	256QAM	24.3±1
		Edge_1RB_Left DFT	256QAM	23.0±1
		Edge_1RB_Right DFT	256QAM	23.1±1
		Outer_Full DFT	pi/2 BPSK	25.5±1
		Inner_Full DFT	pi/2 BPSK	25.7±1
		Edge_1RB_Left DFT	pi/2 BPSK	23.3±1
		Edge_1RB_Right DFT	pi/2 BPSK	23.4±1

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	n41-MIMO	Inner_Full	QPSK	25.3±1
		Outer_Full	QPSK	23.9±1
		Edge_1RB_Left	QPSK	23.3±1
		Edge_1RB_Right	QPSK	23.4±1
		Inner_Full	16QAM	24.9±1
		Outer_Full	16QAM	23.9±1
		Edge_1RB_Left	16QAM	23.3±1
		Edge_1RB_Right	16QAM	23.5±1
			64QAM	23.5±1
			256QAM	23.5±1
	n66,DC_2A_n66A,DC_5A_n66A,DC_7A_n66A,DC_12A_n66A,DC_7C_n66A,DC_2A-12A_n66A,DC_5A-7A_n66A,DC_5A-66A_n66A,DC_12A-66A_n66A,DC_7A-66A_n66A,DC_5A-7A-66A_n66A,DC_5A-7C_n66A,DC_5A-7C-66A_n66A	Inner_Full CP	QPSK	22.2±1
		Outer_Full CP	QPSK	20.7±1
		Edge_1RB_Left CP	QPSK	20.6±1
		Edge_1RB_Right CP 1767.5MHz	QPSK	21.7±1
		Edge_1RB_Right CP	QPSK	20.5±1
		Inner_Full DFT	QPSK	22.7±1
		Outer_Full DFT	QPSK	22.7±1
		Edge_1RB_Left DFT	QPSK	22.5±1
		Edge_1RB_Right DFT 1767.5MHz	QPSK	23.6±1
		Edge_1RB_Right DFT	QPSK	22.5±1
		Inner_Full CP 1722.5MHz	16QAM	20.0±1
		Inner_Full CP	16QAM	21.6±1
		Outer_Full CP	16QAM	20.7±1
		Edge_1RB_Left CP	16QAM	20.3±1
		Edge_1RB_Right CP	16QAM	21.3±1
		Inner_Full DFT	16QAM	22.7±1
		Outer_Full DFT	16QAM	21.7±1
		Edge_1RB_Left DFT	16QAM	21.6±1
		Edge_1RB_Right DFT	16QAM	22.5±1
		Inner_Full CP	64QAM	20.2±1
		Outer_Full CP	64QAM	20.2±1
		Edge_1RB_Left CP	64QAM	19.8±1
		Edge_1RB_Right CP	64QAM	19.8±1
		Edge_1RB_Right CP 1767.5MHz	64QAM	20.9±1
		Inner_Full DFT	64QAM	21.2±1
		Outer_Full DFT	64QAM	21.1±1
		Edge_1RB_Left DFT	64QAM	20.9±1
		Edge_1RB_Right DFT	64QAM	21.86±1
		Inner_Full CP	256QAM	20.2±1
		Outer_Full CP	256QAM	20.2±1
		Edge_1RB_Left CP	256QAM	19.9±1
		Edge_1RB_Right CP	256QAM	20.9±1

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		Inner_Full DFT	256QAM	21.2±1
		Outer_Full DFT	256QAM	21.2±1
		Edge_1RB_Left DFT	256QAM	20.6±1
		Edge_1RB_Right DFT	256QAM	21.6±1
		Inner_Full DFT	pi/2 BPSK	22.6±1
		Outer_Full DFT	pi/2 BPSK	22.6±1
		Edge_1RB_Left DFT	pi/2 BPSK	22.4±1
		Edge_1RB_Right DFT 1767.5MHz	pi/2 BPSK	23.5±1
		Edge_1RB_Right DFT	pi/2 BPSK	22.4±1
	n71,DC_2A_n71A,DC_66A_n71A,DC_66C_n71A,DC_2C_n71A,DC_2A-66A_n71A,DC_2A-2A_n71A,DC_2A-71A_n71A,DC_66A-71A_n71A,DC_66A-66A_n71A,DC_2C-66A_n71A,DC_2A-66C_n71A,DC_2A-2A-66A_n71A,DC_2A-66A-66A_n71A,DC_2A-66A-71A_n71A	Inner_Full CP	QPSK	22.9±1
		Outer_Full CP	QPSK	21.4±1
		Edge_1RB_Left CP	QPSK	21.4±1
		Edge_1RB_Right CP	QPSK	21.3±1
		DFT	QPSK	23.5±1
		CP	16QAM	22.5±1
		DFT	16QAM	23.5±1
			64QAM	21.9±1
			256QAM	21.9±1
			pi/2 BPSK	23.4±1
	n77L	Inner_Full CP	QPSK	24.77±1
		Inner_Full CP 70M	QPSK	20.8±1
		Outer_Full CP	QPSK	24.4±1
		Outer_Full CP 10/15/70M	QPSK	22.0±1
		Edge_1RB_Left CP	QPSK	21.93±1
		Edge_1RB_Right CP 10/70M	QPSK	20.8±1
		Edge_1RB_Right CP	QPSK	23.1±1
		Inner_Full DFT	QPSK	25.4±1
		Outer_Full DFT	QPSK	25.4±1
		Outer_Full DFT 10/15/70M	QPSK	23.9±1

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Edge_1RB_Left DFT	QPSK	23.0±1
Edge_1RB_Left DFT 10/15/70M	QPSK	21.3±1
Edge_1RB_Right DFT	QPSK	23.1±1
Edge_1RB_Right DFT 10/15/70M	QPSK	21.4±1
Inner_Full CP	16QAM	24.4±1
Inner_Full CP 10/15/70M	16QAM	22.9±1
Outer_Full CP	16QAM	23.4±1
Outer_Full CP 10/15/70M	16QAM	22.0±1
Edge_1RB_Left DFT	16QAM	21.4±1
Edge_1RB_Left DFT 10/15/70M	16QAM	22.9±1
Edge_1RB_Right DFT	16QAM	23.2±1
Edge_1RB_Right DFT 10/15/70M	16QAM	22.1±1
Inner_Full CP	16QAM	23.8±1
Inner_Full CP 10/15/70M	16QAM	22.4±1
Outer_Full CP	64QAM	23.9±1
Outer_Full CP 10/15/70M	64QAM	22.4±1
Edge_1RB_Left DFT	64QAM	23.0±1
Edge_1RB_Left DFT 10/15/70M	64QAM	21.5±1
Edge_1RB_Right DFT	64QAM	23.1±1
Edge_1RB_Right DFT 10/15/70M	64QAM	21.6±1
Inner_Full CP	256QAM	22.9±1
Inner_Full CP 10/15/70M	256QAM	21.5±1
Outer_Full CP	256QAM	22.9±1
Outer_Full CP 10/15/70M	256QAM	21.6±1
Edge_1RB_Left CP	256QAM	22.6±1
Edge_1RB_Left CP 10/15/70M	256QAM	21.1±1
Edge_1RB_Right CP	256QAM	22.8±1
Edge_1RB_Right CP 10/15/70M	256QAM	21.7±1
Inner_Full DFT	256QAM	23.9±1
Inner_Full DFT 10/15/70M	256QAM	22.4±1
Outer_Full DFT	256QAM	23.9±1
Outer_Full DFT 10/15/70M	256QAM	22.4±1
Edge_1RB_Left DFT	256QAM	22.6±1
Edge_1RB_Left DFT 10/15/70M	256QAM	21.2±1
Edge_1RB_Right DFT	256QAM	22.8±1
Edge_1RB_Right DFT 10/15/70M	256QAM	21.2±1
Inner_Full/Outer_Full DFT	pi/2 BPSK	25.4±1
Inner_Full DFT /Outer_Full10/15/70M	pi/2 BPSK	23.8±1
Edge_1RB_Left /Edge_1RB_Right DFT	pi/2 BPSK	23.0±1

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		Edge_1RB_Left/Edge_1RB_Right DFT 10/15/70M	pi/2 BPSK	21.3±1
	n77H	Inner_Full CP 10/15MHz	QPSK	24.3±1
		Inner_Full CP 70MHz	QPSK	21.91±1
		Inner_Full CP 20/30/40/50/60/80/90/100MHz	QPSK	25.1±1
		Outer_Full CP 10/15MHz	QPSK	21.9±1
		Outer_Full CP 70MHz	QPSK	19.7±1
		Outer_Full CP 20/30/40/50/60/80/90/100MHz	QPSK	23.6±1
		Edge_1RB_Left CP 10/15MHz	QPSK	22.25±1
		Edge_1RB_Left CP 70MHz	QPSK	21.5±1
		Edge_1RB_Left CP 20/30/40/50/60/80/90/100MHz	QPSK	21.2±1
		Edge_1RB_Right CP 10/15MHz	QPSK	21.5±1
		Edge_1RB_Right CP 70MHz	QPSK	20.0±1
		Edge_1RB_Right CP 20/30/40/50/60/80/90/100MHz	QPSK	23.3±1
		Inner_Full DFT 10/15MHz	QPSK	23.9±1
		Inner_Full DFT 70MHz	QPSK	22.9±1
		Inner_Full DFT 20/30/40/50/60/80/90/100MHz	QPSK	25.6±1
		Outer_Full DFT 10/15MHz	QPSK	23.0±1
		Outer_Full DFT 70MHz	QPSK	22.7±1
		Outer_Full DFT 20/30/40/50/60/80/90/100MHz	QPSK	25.6±1
		Edge_1RB_Left DFT 10/15MHz	QPSK	21.2±1
		Edge_1RB_Left DFT 70MHz	QPSK	21.6±1
		Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	QPSK	23.3±1
		Edge_1RB_Right DFT 10/15MHz	QPSK	21.5±1
		Edge_1RB_Right DFT 70MHz	QPSK	20.9±1
		Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	QPSK	23.2±1
		Inner_Full CP 10/15/70MHz	16QAM	22.94±1
		Inner_Full CP 20/30/40/50/60/80/90/100MHz	16QAM	24.6±1
		Outer_Full CP 10/15MHz	16QAM	22.0±1
		Outer_Full CP 70MHz	16QAM	19.6±1
		Outer_Full CP 20/30/40/50/60/80/90/100MHz	16QAM	23.7±1
		Edge_1RB_Left CP 10/15MHz	16QAM	21.6±1
		Edge_1RB_Left CP 70MHz	16QAM	21.2±1

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Edge_1RB_Left CP 20/30/40/50/60/80/90/100MHz	16QAM	23.3±1
Edge_1RB_Right CP 10/15MHz	16QAM	21.5±1
Edge_1RB_Right CP 70MHz	16QAM	21.0±1
Edge_1RB_Right CP 20/30/40/50/60/80/90/100MHz	16QAM	23.3±1
Inner_Full DFT 10/15MHz	16QAM	23.9±1
Inner_Full DFT 70MHz	16QAM	22.3±1
Inner_Full DFT 20/30/40/50/60/80/90/100MHz	16QAM	25.6±1
Outer_Full DFT 10/15MHz	16QAM	23.0±1
Outer_Full DFT 70MHz	16QAM	21.2±1
Outer_Full DFT 20/30/40/50/60/80/90/100MHz	16QAM	25.7±1
Edge_1RB_Left DFT 10/15MHz	16QAM	21.6±1
Edge_1RB_Left DFT 70MHz	16QAM	21.3±1
Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	16QAM	23.2±1
Edge_1RB_Right DFT 10/15MHz	16QAM	21.4±1
Edge_1RB_Right DFT 70MHz	16QAM	20.9±1
Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	16QAM	23.3±1
Inner_Full CP 10/15MHz	64QAM	21.4±1
Inner_Full CP 70MHz	64QAM	19.3±1
Inner_Full CP 20/30/40/50/60/80/90/100MHz	64QAM	23.1±1
Outer_Full CP 10/15MHz	64QAM	21.5±1
Outer_Full CP 70MHz	64QAM	19.3±1
Outer_Full CP 20/30/40/50/60/80/90/100MHz	64QAM	23.1±1
Edge_1RB_Left CP 10/15MHz	64QAM	21.3±1
Edge_1RB_Left CP 70MHz	64QAM	21.0±1
Edge_1RB_Left CP 20/30/40/50/60/80/90/100MHz	64QAM	23.1±1
Edge_1RB_Right CP 10/15MHz	64QAM	21.2±1
Edge_1RB_Right CP 70MHz	64QAM	20.8±1
Edge_1RB_Right CP 20/30/40/50/60/80/90/100MHz	64QAM	23.1±1
Inner_Full DFT 10/15MHz	64QAM	22.4±1
Inner_Full DFT 70MHz	64QAM	20.8±1
Inner_Full DFT 20/30/40/50/60/80/90/100MHz	64QAM	24.1±1
Outer_Full DFT 10/15MHz	64QAM	22.4±1
Outer_Full DFT 70MHz	64QAM	21.0±1

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Outer_Full DFT 20/30/40/50/60/80/90/100MHz	64QAM	24.2±1
Edge_1RB_Left DFT 10/15MHz	64QAM	21.5±1
Edge_1RB_Left DFT 70MHz	64QAM	21.2±1
Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.2±1
Edge_1RB_Right DFT 10/15MHz	64QAM	21.4±1
Edge_1RB_Right DFT 70MHz	64QAM	20.7±1
Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.3±1
Inner_Full CP 10/15MHz	256QAM	21.5±1
Inner_Full CP 70MHz	256QAM	19.5±1
Inner_Full CP 20/30/40/50/60/80/90/100MHz	256QAM	23.2±1
Outer_Full CP 10/15MHz	256QAM	21.5±1
Outer_Full CP 70MHz	256QAM	19.2±1
Outer_Full CP 20/30/40/50/60/80/90/100MHz	256QAM	23.1±1
Edge_1RB_Left CP 10/15MHz	256QAM	20.9±1
Edge_1RB_Left CP 70MHz	256QAM	21.2±1
Edge_1RB_Left CP 20/30/40/50/60/80/90/100MHz	256QAM	22.9±1
Edge_1RB_Right CP 10/15MHz	256QAM	21.1±1
Edge_1RB_Right CP 70MHz	256QAM	20.6±1
Edge_1RB_Right CP 20/30/40/50/60/80/90/100MHz	256QAM	23.0±1
Inner_Full DFT 10/15MHz	256QAM	22.4±1
Inner_Full DFT 70MHz	256QAM	20.8±1
Inner_Full DFT 20/30/40/50/60/80/90/100MHz	256QAM	24.2±1
Outer_Full DFT 10/15MHz	256QAM	22.6±1
Outer_Full DFT 70MHz	256QAM	20.9±1
Outer_Full DFT 20/30/40/50/60/80/90/100MHz	256QAM	24.2±1
Edge_1RB_Left DFT 10/15MHz	256QAM	21.2±1
Edge_1RB_Left DFT 70MHz	256QAM	20.9±1
Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	256QAM	22.9±1
Edge_1RB_Right DFT 10/15MHz	256QAM	21.1±1
Edge_1RB_Right DFT 70MHz	256QAM	20.3±1
Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	256QAM	23.0±1
Inner_Full/Outer_Full DFT 10/15MHz	pi/2 BPSK	23.0±1

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		Edge_1RB_Right/Edge_1RB_Left DFT 10/15MHz	pi/2 BPSK	21.5±1
		Inner_Full/Outer_Full DFT 70MHz	pi/2 BPSK	23.1±1
		Edge_1RB_Right/Edge_1RB_Left DFT 70MHz	pi/2 BPSK	21.2±1
		DFT 20/30/40/50/60/80/90/100MHz	pi/2 BPSK	25.8±1
	n78L,DC_2A_n78A,DC_7A_n78A, DC_2A-7A_n78A,	Inner_Full CP 10/15/20/30/40/50/60/80/90/100MHz	QPSK	24.3±1
		Inner_Full CP 70MHz	QPSK	22.1±1
		Outer_Full CP	QPSK	22.8±1
		Edge_1RB_Left /Edge_1RB_Right DFT	QPSK	22.5±1
		Inner_Full/Outer_Full DFT	QPSK	24.9±1
		Edge_1RB_Left /Edge_1RB_Right DFT	QPSK	22.7±1
		Inner_Full CP	16QAM	23.9±1
		Outer_Full CP	16QAM	22.8±1
		Edge_1RB_Left /Edge_1RB_Right CP	16QAM	22.6±1
		Inner_Full DFT	16QAM	24.9±1
		Outer_Full DFT	16QAM	24.0±1
		Edge_1RB_Left /Edge_1RB_Right DFT	16QAM	22.7±1
		CP	64QAM	22.4±1
		DFT 10/15/70MHz	64QAM	23.02±1
		DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.4±1
		CP	256QAM	22.4±1
		Inner_Full DFT	256QAM	23.3±1
		Outer_Full DFT	256QAM	23.3±1
		Edge_1RB_Left DFT	256QAM	22.0±1
		Edge_1RB_Right DFT	256QAM	22.2±1
		Inner_Full/Outer_Full DFT	pi/2 BPSK	25.0±1
		Edge_1RB_Left /Edge_1RB_Right DFT	pi/2 BPSK	22.5±1
	n78H	Inner_Full CP	QPSK	24.8±1
		Outer_Full CP 10/15/70MHz	QPSK	21.9±1
		Outer_Full CP 20/30/40/50/60/80/90/100MHz	QPSK	23.3±1
		Edge_1RB_Left CP	QPSK	22.6±1
		Edge_1RB_Right CP	QPSK	22.78±1

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Inner_Full DFT	QPSK	25.4±1
Outer_Full DFT 70MHz	QPSK	24.9±1
Outer_Full DFT 10/15/20/30/40/50/60/80/90/100MHz	QPSK	25.4±1
Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	QPSK	22.9±1
Edge_1RB_Left DFT 10/15/70MHz	QPSK	22.2±1
Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	QPSK	22.8±1
Edge_1RB_Right DFT 10/15/70MHz	QPSK	22.4±1
Inner_Full CP 70MHz	16QAM	24.3±1
Inner_Full CP 10/15/20/30/40/50/60/80/90/100MHz	16QAM	22.2±1
Outer_Full CP 70MHz	16QAM	20.7±1
Outer_Full CP 10/15/20/30/40/50/60/80/90/100MHz	16QAM	23.21±1
Edge_1RB_Left CP	16QAM	22.6±1
Edge_1RB_Right CP	16QAM	22.81±1
Inner_Full DFT 20/30/40/50/60/80/90/100MHz	16QAM	25.4±1
Inner_Full DFT 10/15/70MHz	16QAM	25.1±1
Outer_Full DFT 20/30/40/50/60/80/90/100MHz	16QAM	24.4±1
Outer_Full DFT 10/15/70MHz	16QAM	23.0±1
Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	16QAM	22.9±1
Edge_1RB_Left DFT 10/15/70MHz	16QAM	22.2±1
Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	16QAM	22.9±1
Edge_1RB_Right DFT 10/15/70MHz	16QAM	22.5±1
CP 10/15/70MHz	64QAM	22.1±1
CP 20/30/40/50/60/80/90/100MHz	64QAM	23.1±1
Inner_Full DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.5±1
Inner_Full DFT 10/15/70MHz	64QAM	23.4±1
Outer_Full DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.9±1
Outer_Full DFT 10/15/70MHz	64QAM	23.9±1

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		Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.9±1
		Edge_1RB_Left DFT 10/15/70MHz	64QAM	22.9±1
		Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	64QAM	23.9±1
		Edge_1RB_Right DFT 10/15/70MHz	64QAM	22.9±1
		Inner_Full CP 10/15/70MHz	256QAM	21.5±1
		Inner_Full CP 20/30/40/50/60/80/90/100MHz	256QAM	23.1±1
		Outer_Full CP 10/15/70MHz	256QAM	21.5±1
		Outer_Full CP 20/30/40/50/60/80/90/100MHz	256QAM	23.1±1
		Edge_1RB_Left CP	256QAM	22.78±1
		Edge_1RB_Left CP 60MHz 3750	256QAM	19.0±1
		Edge_1RB_Right CP	256QAM	23.0±1
		Edge_1RB_Right CP 60MHz 3750	256QAM	22.0±1
		Inner_Full DFT 10/15/70MHz	256QAM	24.0±1
		Inner_Full DFT 20/30/40/50/60/80/90/100MHz	256QAM	23.7±1
		Outer_Full DFT 10/15MHz	256QAM	21.4±1
		Outer_Full DFT 70MHz	256QAM	23.3±1
		Outer_Full DFT 20/30/40/50/60/80/90/100MHz	256QAM	23.8±1
		Edge_1RB_Left DFT 10/15/70MHz	256QAM	21.8±1
		Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	256QAM	22.6±1
		Edge_1RB_Right DFT 10/15MHz	256QAM	21.2±1
		Edge_1RB_Right DFT 20/30/40/50/60/70/80/90/100MHz	256QAM	22.6±1
		Inner_Full DFT	pi/2 BPSK	25.5±1
		Outer_Full DFT 10/15/70MHz	pi/2 BPSK	24.9±1
		Outer_Full DFT 20/30/40/50/60/80/90/100MHz	pi/2 BPSK	25.4±1
		Edge_1RB_Left DFT 10/15/70MHz	pi/2 BPSK	22.2±1
		Edge_1RB_Left DFT 20/30/40/50/60/80/90/100MHz	pi/2 BPSK	22.9±1
		Edge_1RB_Right DFT 10/15/70MHz	pi/2 BPSK	22.4±1
		Edge_1RB_Right DFT 20/30/40/50/60/80/90/100MHz	pi/2 BPSK	22.9±1
	n77L-MIMO	Inner_Full	QPSK	25.0±1

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Outer_Full/Edge_1RB_Left/Edge_1RB_Right	QPSK	23.6±1
Inner_Full	16QAM	24.6±1
Outer_Full/Edge_1RB_Left/Edge_1RB_Right	16QAM	23.6±1
	64QAM	23.2±1
10/15/20/30/40/50/60/70/80/90MHz	256QAM	23.1±1
100MHz	256QAM	22.7±1
Inner_Full 10/15/70MHz	QPSK	23.9±1
Inner_Full 20/30/40/50/6080/90/100MHz	QPSK	25.3±1
Outer_Full 10/15/70MHz	QPSK	22.4±1
Outer_Full 20/30/40/50/6080/90/100MHz	QPSK	23.8±1
Edge_1RB_Left 10/15/70MHz	QPSK	22.0±1
Edge_1RB_Left 20/30/40/50/6080/90/100MHz	QPSK	23.4±1
Edge_1RB_Right 10/15/70MHz	QPSK	21.9±1
Edge_1RB_Right 20/30/40/50/6080/90/100MHz	QPSK	23.3±1
Inner_Full 10/15/70MHz	16QAM	23.4±1
Inner_Full 20/30/40/50/6080/90/100MHz	16QAM	24.8±1
Outer_Full 10/15/70MHz	16QAM	22.5±1
Outer_Full 20/30/40/50/6080/90/100MHz	16QAM	23.8±1
Edge_1RB_Left 10/15/70MHz	16QAM	21.9±1
Edge_1RB_Left 20/30/40/50/6080/90/100MHz	16QAM	23.4±1
Edge_1RB_Right 10/15/70MHz	16QAM	21.9±1
Edge_1RB_Right 20/30/40/50/6080/90/100MHz	16QAM	23.3±1
Inner_Full 10/15/70MHz	64QAM	22.0±1
Inner_Full 20/30/40/50/6080/90/100MHz	64QAM	23.3±1
Outer_Full 10/15/70MHz	64QAM	22.0±1
Outer_Full 20/30/40/50/6080/90/100MHz	64QAM	23.2±1
Edge_1RB_Left 10/15/70MHz	64QAM	21.9±1
Edge_1RB_Left 20/30/40/50/6080/90/100MHz	64QAM	23.5±1
Edge_1RB_Right 10/15/70MHz	64QAM	21.9±1

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		Edge_1RB_Right 20/30/40/50/6080/90/100MHz	64QAM	23.3±1
		10/15/70MHz	256QAM	21.0±1
		20/30/40/50/6080/90/100MH	256QAM	23.3±1
		Inner_Full	QPSK	24.9±1
		Outer_Full/Edge_1RB_Left/Edge_1RB_Right	QPSK	23.4±1
		10/15/70MHz	16QAM	23.7±1
		20/30/40/50/6080/90/100MHz	16QAM	24.4±1
			64QAM	23.0±1
			256QAM	23.0±1
	n78H-MIMO	Inner_Full	QPSK	25.0±1
		Outer_Full/Edge_1RB_Left/Edge_1RB_Right	QPSK	23.5±1
		Inner_Full	16QAM	24.4±1
		Outer_Full/Edge_1RB_Left/Edge_1RB_Right	16QAM	23.5±1
			64QAM	23.0±1
			256QAM	23.0±1

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5.6 Conducted Receive Sensitivity

SIM8260A conducted RF receiving sensitivity is fully meet 3GPP specification. Customers can get more details by check 3GPP official website http://www.3gpp.org.

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5.7 Thermal Design

Make sure that the SIM8260A can reach maximum work performance under extended temperature or extreme conditions for a long time, thermal dissipation design is very important.

The thermal dissipation design of LGA is described in Figure as follows:

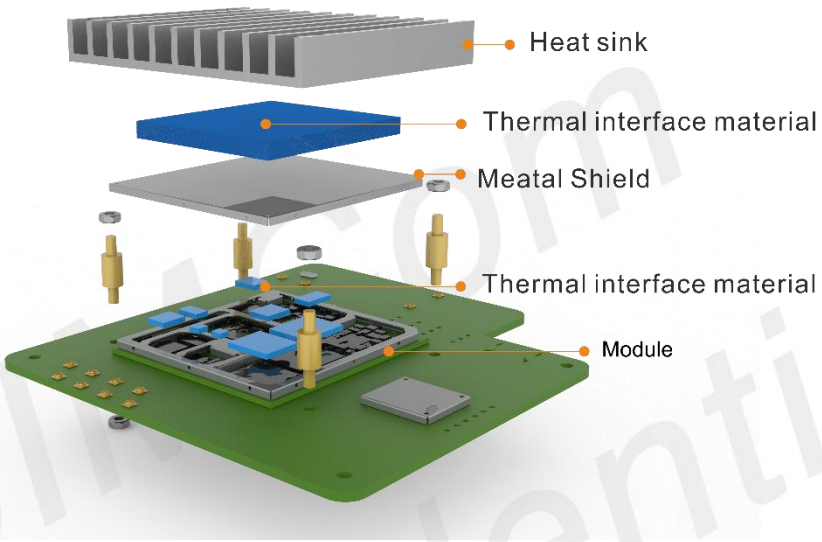

Figure 49: 3D drawing of LGA thermal dissipation design

There are some design rules to enhance thermal dissipation performance:

- Keep the module away from other heat sources such as battery, power, AP, etc.
- All the GND pins of the module should be connected.
- Add enough through GND via on the main PCB. Via material is very important solid copper and stacked via is better.
- Make sure maximize airflow around the module.
- Recommend use heat dissipation material connect to the customers' device on the top side of the module to enhance the heat dissipation. Large heat dissipation area is better.
- Chose a high effective heat dissipation material is better such as heat pipe, graphite sheets.

Table 71: Chip junction temperature table

Chip model	Junction temperature
NM4484NSPAXAE-3F	85℃
PMK65	125℃
PMX65	125℃
SDX65/SDX62	105℃
QET7100	115℃

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QPM6679	85℃
QPM6375	85℃
QPM6621	85℃
S55643-11	85℃
SDR735	105℃
SMR546	105℃
QTM545	85℃
QTM547	105℃

5.8 ESD

Module is sensitive to ESD in the process of storage, transporting, and assembling. When module is mounted on the customers' main board, the ESD components should be placed closed to the connectors which human body may touch, such as (U)SIM card socket, SD card socket, audio jacks, switches, USB interface, etc. The following table shows the module ESD measurement performance.

Table 72: The ESD performance measurement table (temperature: 25°C, humidity: 45%)

Part	Contact discharge	Air discharge
VBAT, GND	± 5kV	± 10 kV
Antenna	± 5 kV	± 10 kV
PWRKEY	± 4 kV	± 8 kV
USB	± 4 kV	± 8 kV
RESET_N	± 3 kV	± 6 kV
(U)SIM	± 3 kV	± 6 kV
Other PADs	± 3 kV	± 6 kV

NOTE

Test conditions:

- The external of the module has surge protection diodes and ESD protection diodes.
- The data in table above were tested using SIMCom EVB.

6 Manufacturing

6.1 Top and Bottom View of SIM8XX0X

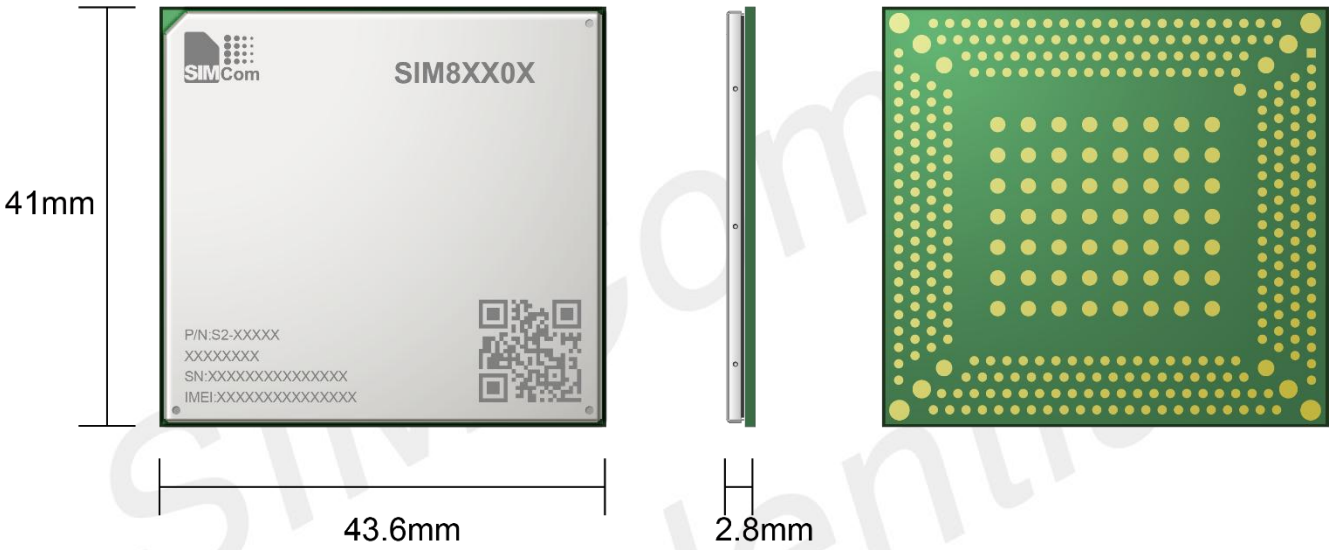

Figure 50: Top and bottom view of SIMXX0X

6.2 Label Description Information

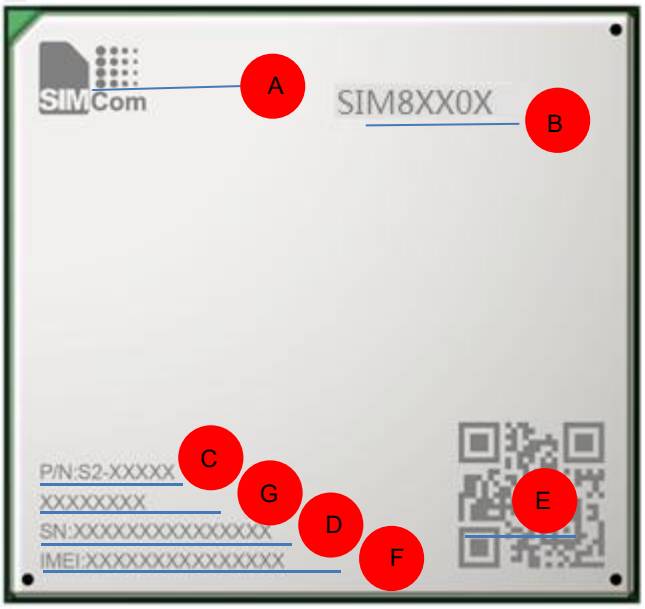

Figure 51: Label description of module

Table 73: Label description of module information

No.	Description
A	LOGO
B	Project name
C	Product code
D	Serial number
E	QR code
F	International mobile equipment identity
G	Product Details Serial Number

NOTE

- The Figure above are the effect diagrams of the module, for reference only. Please refer to the actual product for appearance.
- SIM8XX0X is Project name, Include these product names SIM8380A, SIM8280A, SIM8260C, SIM8260E, SIM8260A. For more detailed product differences, please consult the SIMCom FAE teams.

6.3 Recommended PCB Footprint

The following figure shows the PCB footprint of SIM8260A.

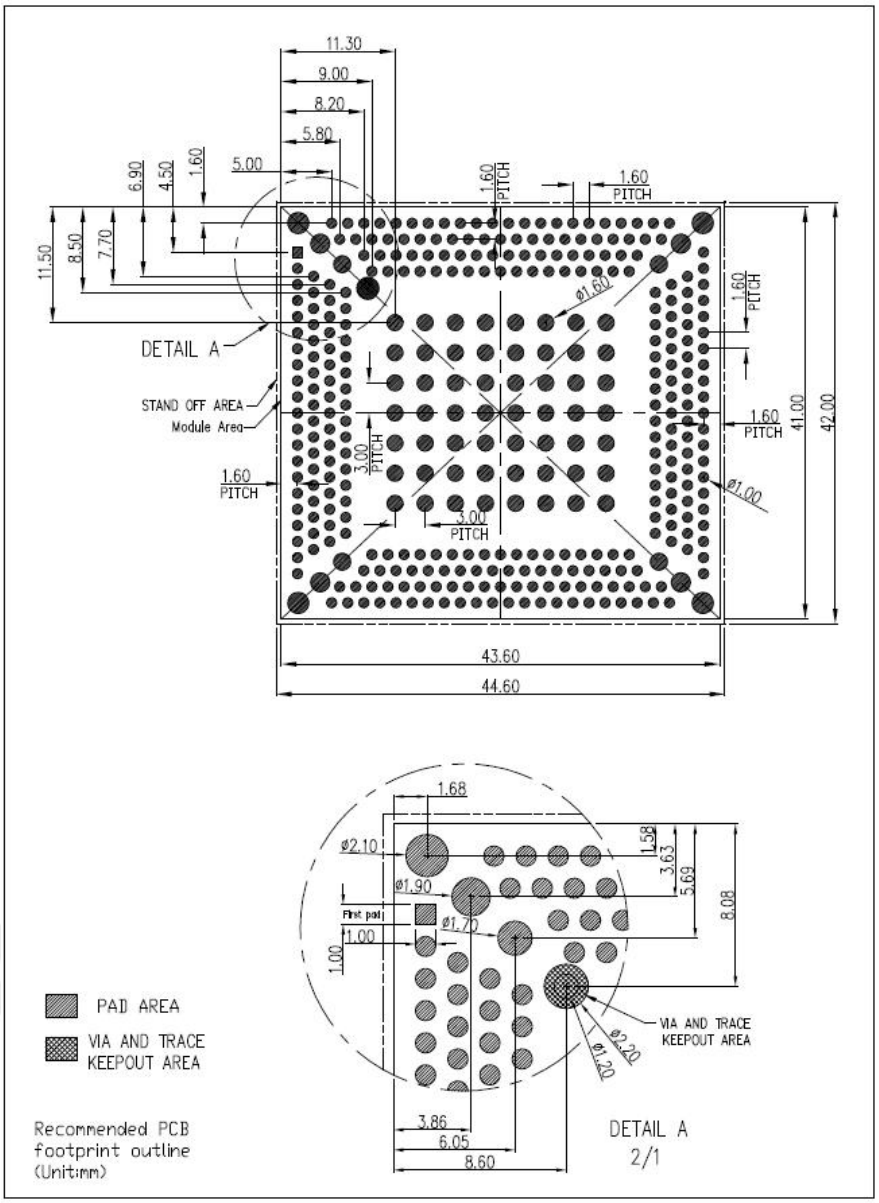

Figure 52: Recommended PCB footprint

NOTE

- Keep out Area is used for internal testing of the module; customers do not need to leave pads. See module recommended package for details

6.4 Recommended SMT Stencil

The following figure shows the SMT stencil of SIM8260A.

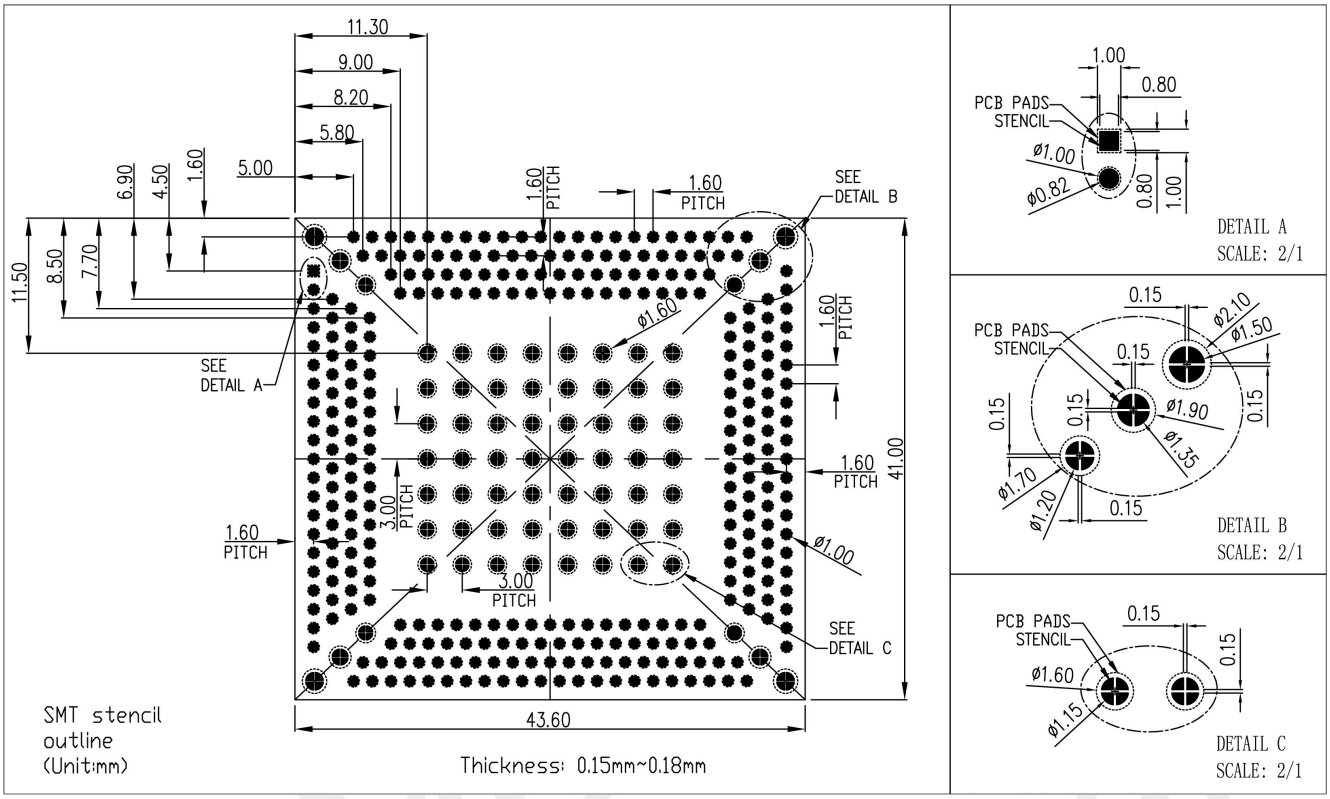

Figure 53: Recommended SMT stencil

6.5 Recommended SMT Reflow Profile

The following figure shows the SMT reflow profile of SIM8260A.

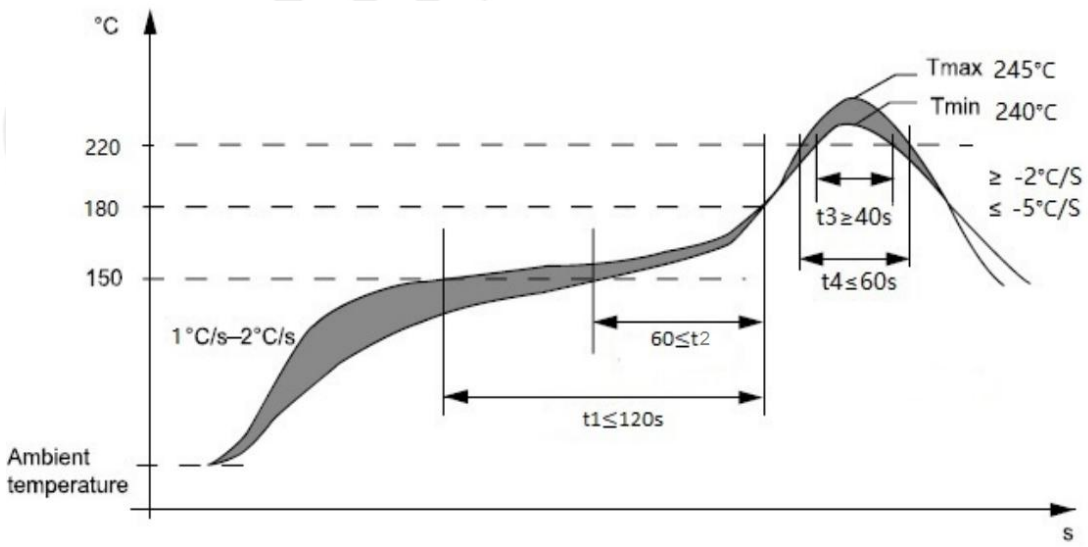

Figure 54: Recommended SMT reflow profile

NOTE

- Refer to “Module secondary-SMT-UGD” for more information about the module shipping and manufacturing.

6.6 Moisture Sensitivity Level (MSL)

SIM8260A is susceptible to damage induced by absorbed moisture and high temperature. A package’s moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized as follows.

Table 74: MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤+30°C /85% RH
2	1 year	≤+30°C /60% RH
2a	4 weeks	≤+30°C /60% RH
3	168 hours	≤+30°C /60% RH
4	72 hours	≤+30°C /60% RH
5	48 hours	≤+30°C /60% RH
5a	24 hours	≤+30°C /60% RH
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	≤+30°C /60% RH

The SIM8260A device samples are currently classified as MSL3 at 255 (+5, -0) °C, following the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

6.7 Baking Requirements

It is necessary to bake modules if the prescribed time limit has been exceeded. The baking conditions are specified in Table 71. Note that if baking is required, the devices must be transferred into trays that can be baked to at least 125°C.

The module is vacuum-packed and has a shelf life of 6 months when the temperature is less than 40 degrees and the relative humidity is less than 90%.

If any of the following three conditions are met, the module should be thoroughly baked before reflow welding, as shown in Table 71. Otherwise, the module may be permanently damaged during reflow welding.

- Vacuum packing damaged or air leakage.
- When vacuum packing is opened in good condition, the storage time is more than 6 months (from the date of packing).
- When the vacuum packaging is intact, the storage time of the vacuum packaging is not more than 6 months (calculated from the date of packaging), but the storage time of the vacuum packaging is more than 168 hours in the workshop with temperature <30° C and relative humidity <60%.

Table 75: Baking requirements

Baking conditions options	Duration	Note
40°C±5°C, <5% RH	192 hours	
120°C±5°C, <5% RH	8 hours	Original pallet is not applicable

NOTE

The tray is not resistant to high temperature. If the customer's baking temperature is 120° C, the module should be taken out of the tray for baking, otherwise the tray may be damaged by high temperature

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7 Packaging

SIM8260A module supports tray packaging. The packaging process is shown in the following figures.

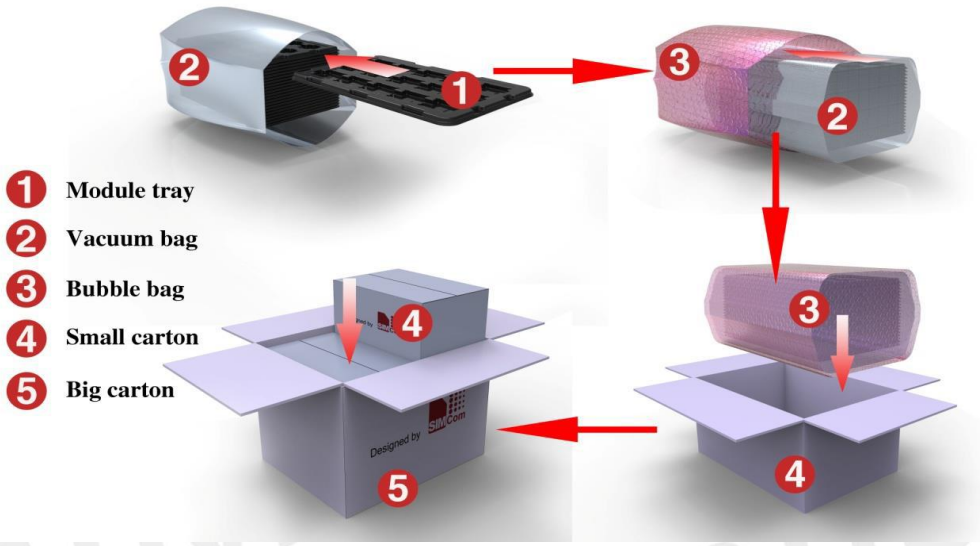

Figure 55: Packaging process

Module tray drawing：

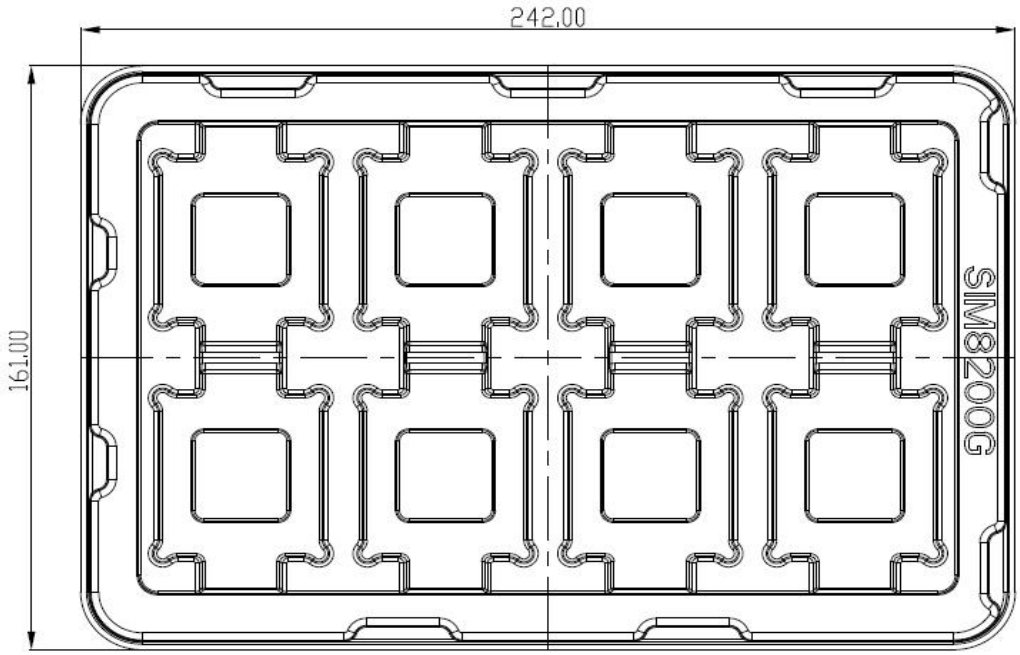

Figure 56: Module tray drawing

Table 76: Tray size

Length（±3mm）	Width（±3mm）	Number
242.0	161.0	8

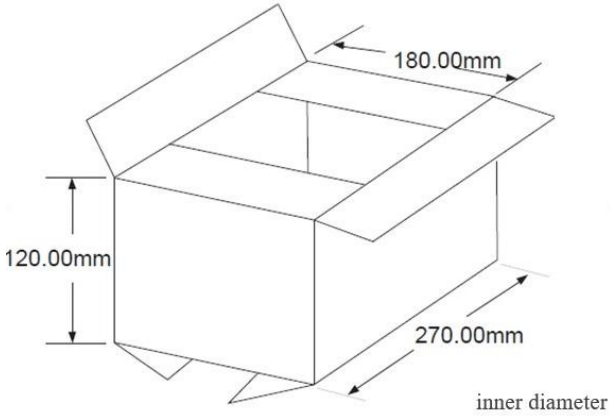

Figure 57: Small carton drawing

Table 77: Small carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
270	180	120	8*19-2=150

Big carton drawing：

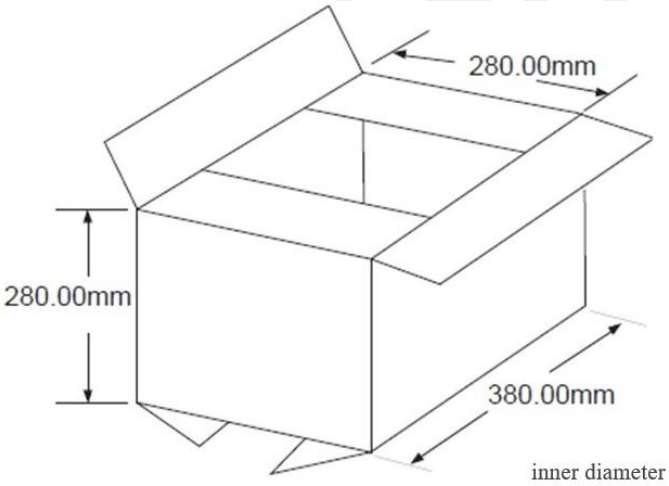

Figure 58: Big carton drawing

Table 78: Big carton size

Length（±10mm）	Width（±10mm）	Height（±10mm）	Number
380	280	280	150*4=600

8 Appendix

8.1 Coding Schemes and Maximum Net Data Rates over Air Interface

Table 79: Coding schemes and maximum net data rates over air interface

HSDPA device category	Max data rate（peak）	Modulation type
Category 1	1.2Mbps	16QAM, QPSK
Category 2	1.2Mbps	16QAM, QPSK
Category 3	1.8Mbps	16QAM, QPSK
Category 4	1.8Mbps	16QAM, QPSK
Category 5	3.6Mbps	16QAM, QPSK
Category 6	3.6Mbps	16QAM, QPSK
Category 7	7.2Mbps	16QAM, QPSK
Category 8	7.2Mbps	16QAM, QPSK
Category 9	10.2Mbps	16QAM, QPSK
Category 10	14.4Mbps	16QAM, QPSK
Category 11	0.9Mbps	QPSK
Category 12	1.8Mbps	QPSK
Category 13	17.6Mbps	64QAM
Category 14	21.1Mbps	64QAM
Category 15	23.4Mbps	16QAM
Category 16	28Mbps	16QAM
Category 17	23.4Mbps	64QAM
Category 18	28Mbps	64QAM
Category 19	35.5Mbps	64QAM
Category 20	42Mbps	64QAM
Category 21	23.4Mbps	16QAM
Category 22	28Mbps	16QAM
Category 23	35.5Mbps	64QAM
Category 24	42.2Mbps	64QAM
HSUPA device category	**Max data rate（peak）**	**Modulation type**
Category 1	0.96Mbps	QPSK
Category 2	1.92Mbps	QPSK
Category 3	1.92Mbps	QPSK
Category 4	3.84Mbps	QPSK

Category 5	3.84Mbps	QPSK
Category 6	5.76Mbps	QPSK
LTE-FDD device category (Downlink)	**Max data rate（peak）**	**Modulation type**
Category 1	10Mbps	QPSK/16QAM/64QAM
Category 2	50Mbps	QPSK/16QAM/64QAM
Category 3	100Mbps	QPSK/16QAM/64QAM
Category 4	150Mbps	QPSK/16QAM/64QAM
Category 5	300Mbps	QPSK/16QAM/64QAM
Category 6	300Mbps	QPSK/16QAM/64QAM
LTE-FDD device category (Uplink)	**Max data rate（peak）**	**Modulation type**
Category 1	5Mbps	QPSK/16QAM
Category 2	25Mbps	QPSK/16QAM
Category 3	50Mbps	QPSK/16QAM
Category 4	50Mbps	QPSK/16QAM
Category 5	75Mbps	QPSK/16QAM/64QAM
Category 6	50Mbps	QPSK/16QAM

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8.2 Related Documents

Table 80: Related documents

NO.	Title	Description
[1]	SIM8200 Series_AT Command Manual	AT Command Manual
[2]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[3]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[4]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[5]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)
[6]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[7]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (U IMT-2000. Third Generation cellular networks; Pa Harmonized EN for IMT-2000, CDMA Direct Sprea (UTRA FDD) (UE) covering essential requirements article 3.2 of the R&TTE Directive
[8]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EM standard for radio equipment and services; Part 24 Specific conditions for IMT-2000 CDMA Direct Spre (UTRA) for Mobile and portable (UE) radio and anc equipment
[9]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[10]	3GPP TS 51.010-1	Digital cellular telecommunications system (Releas Mobile Station (MS) conformance specification
[11]	GCF-CC V3.23.1	Global Certification Forum – Certification Criteria
[12]	2002/95/EC	Directive of the European Parliament and of the Co 27 January 2003 on the restriction of the use of cer hazardous substances in electrical and electronic equipment (RoHS)
[13]	SIM8260A_LGA Antenna Port Mapping and Deign Guide	Antenna design guidelines
[14]	NSA_ENDC_For_8260	ENDC list for SIM8260A
[15]	SIM8260AEA&SIM8260A_CA COMBO list	EA &CA list for SIM8260A
[16]	Antenna Tuner reference design	Antenna tuning method and antenna tuning referer design example
[17]	SIM8200 Series Ethernet RTL8125_HDK	Documents about RTL8125B

[18]	SIM8X60X Series PM7250B_HDK	Documents about charge
[19]	SIM8200 Series CODEC ALC5616_HDK	Documents about audio
[20]	SIM8260A WIFI-6 W82_HDK	Documents about W82
[21]	SIM8260 Series_KDL	SIM8260 Series LGA module reference design
[22]	SIM82X0X and SIM83X0X LGA Series_OPEN_GPIOs List	Documents about GPIO configuration
[23]	SIMCOM_Module_Thermal_Design_Guide	Documents about thermal design
[24]	SIM8260 Series QPS615_HDK	Documents about QPS615
[25]	SIM8260 Series QEP8121_HDK	Documents about QEP8121
[26]	SIM8260 Series RTL8367_HDK	Documents about RTL8367

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8.3 Terms and Abbreviations

Table 81: Terms and abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
CS	Coding Scheme
CTS	Clear to Send
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FDD	Frequency Division Dual
FR	Full Rate
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HR	Half Rate
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IMEI	International Mobile Equipment Identity
LTE	Long Term Evolution
MDIO	Management Data Input/Output
MMD	MDIO manageable device
MO	Mobile Originated
MSB	Most Significant Bit
PCB	Printed Circuit Board
PCIe	Peripheral Component Interface Express
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
SDIO	Secure Digital Input and Output
SIM	Subscriber Identification Module
SMS	Short Message Service
SPI	serial peripheral interface
TDD	Time Division Dual
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio

SM	SIM phonebook
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
WCDMA	Wideband Code Division Multiple Access
(U)SIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system
UART	Universal asynchronous receiver transmitter
LB	Low Frequency Band
MHB	Middle and High Frequency Band
UHB	Ultra-High Frequency Band
LAA	Limited Access Authorization
TRX	Transmit and Receive signal
UL-MIMO	Uplink- Multiple Input Multiple Output
DL-MIMO	Downlink- Multiple Input Multiple Output

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8.4 Safety Caution

Table 82: Safety caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	Mobiles operate over radio frequency signals and cellular networks and cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid (U)SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e. g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid (U)SIM card be properly inserted in the cellular terminal or mobile.

FCC Caution.

§ 15.19 Labelling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the condition that this device
doesnotcauseharmfulinterference.

§ 15.21 Information to user.

AnyChangesormodificationsnotexpresslyapprovedbythepartyresponsibleforcompliancecouldvoid
theuser'sauthoritytooperatetheequipment.

§ 15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device,
pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against
harmful interference in a residential installation. This equipment generates uses and can radiate radio
frequency energy and, if not installed and used in accordance with the instructions, may cause harmful
interference to radio communications. However, there is no guarantee that interference will not occur in a
particular installation. If this equipment does cause harmful interference to radio or television reception,
which can bedetermined byturning the equipment off and on,the user is encouraged to try to correctthe
interference by one or more of the following measures:
-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.
Body-worn Operation
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
This equipment should be installed and operated withmini mum distance 20cm between the radiator &
your body
C.Appendix A
A1.Requirement of FCC KDB 996369 D03 for module certification:
1.1List of applicable FCC rules:
ThemodulecomplieswithFCCPart22,24,27,90,96
1.2Summarizethespecificoperationaluseconditions
1.3Limited module procedures:

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The module does not have a standard antenna, which belong to Limited module Standard requires:
Clear and specific instructions describing the conditions, limitations and procedures for

third-parties

to use and/or integrate the module into a host device (see Comprehensive integration instructions
below).
Resolve: Supply example as follows:
Installation Notes:
1) SIM8260A Module Power supply range is DC 3.3V~4.2V, when you use SIM8260A Module design product, the power supply cannot exceed this range.
2) Whenconnec tSIM8260A Moduletothehostdevice,thehostdevicemustbepoweroff.
3) Make sure the module pins correctly installed.
4) Makesurethatthemoduledoesnotallowuserstoreplaceordemolition.

5)Alltypesofantennas thatcanbeusedwithatransmitter: External antennawithmaximum gainnot

Exceeding2.86dBi.
1.4Trace antenna designs: Not applicable.
1.5RFexposureconsiderations:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
1.6Antennas:
The module does not have a standard antenna.
1.7Label and compliance information
This device complieswith part 15 oftheFCCRules.Operation issubject to the condition that this devicedoesnotcauseharmfulinterference.AnyChangesormodificationsnotexpresslyapprovedb
y
the party responsible for compliance could void the user's authority to operate the equipment.
Note:This equipmenthas been tested and found tocomplywith the limitsfor aClassBdigital device,
pursuantto part 15 oftheFCCRules.These limits are designed to provide reasonable protection
againstharmfulinterferenceinaresidentialinstallation.Thisequipmentgeneratesusesandcanradi
ate
radio frequency energy and, if notinstalled and used in accordancewith the instructions,may cause
harmfulinterferencetoradiocommunications.However,thereisnoguarantee thatinterferencewill not occurin a particularinstallation.Ifthis equipment does cause harmful interference to radio or television reception,which can be determined by turning the equipment off and on, the useris encouraged to try to correct the interference by one ormore ofthe followingmeasures:
-Reorientorrelocate the receivingantenna.
-Increase the separationbetweenthe equipment andreceiver.
-Connect the equipment into an outlet on a circuit differentfrom that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.
Body-wornOperation

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This equipment complieswithFCCradiation exposure limitssetforth for an uncontrolled environment.This equipmentshould be installed and operatedwithminimumdistance 20cmbetween
the radiator&your bodyThe host productLabelingRequirements:
NOTICE:The host productmustmake sure that FCClabeling requirements are met.Thisincludes
clearlyvisible exteriorlabelontheoutsideofthe finalproduct housingthatdisplaysthe contents shown
in below:
Contains FCC ID:2AJYU-8XN0001
1.8Informationontestmodes andadditionaltestingrequirements:
When setting up the configuration, ifthe pairing and call box optionsfortesting do not work, the tester
needsto coordinatewith themodulemanufacturerto accessthe testmode software.
1.9Additional testing, Part 15 Subpart B disclaimer:
Themodulartransmitteris onlyFCCauthorized forthe specific rule parts(FCCPart 22,24,27,90,96)list
on the grant, and that the host product manufacturer isresponsible for compliance to any other FCC rulesthat apply to the host not covered by themodulartransmitter grant of certification.
1.10Informationontestmodes andadditionaltestingrequirements:
When testing, testers need to referto the user manual, and the sample powersupply needsto use a special adapte rpower supply.

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