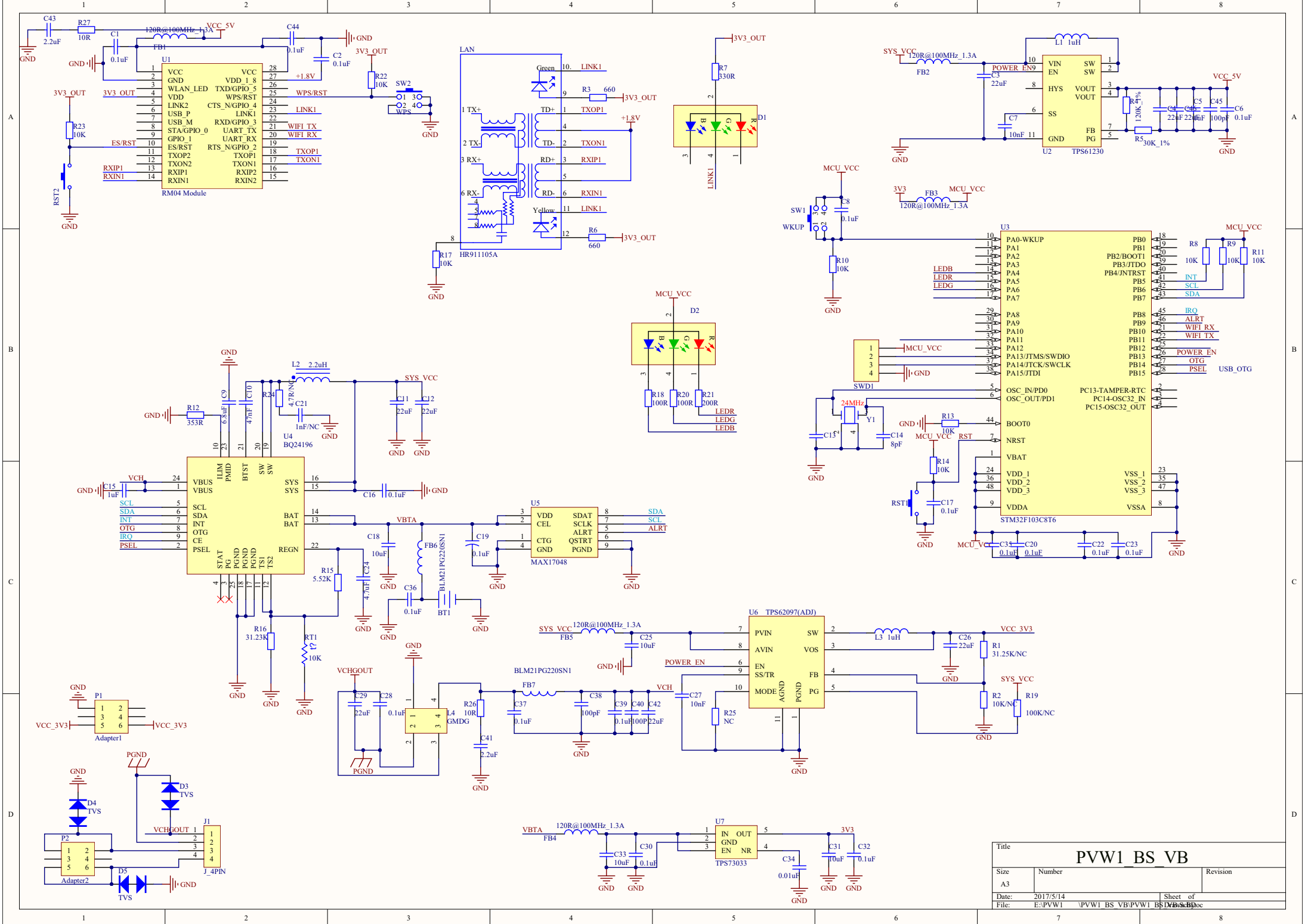
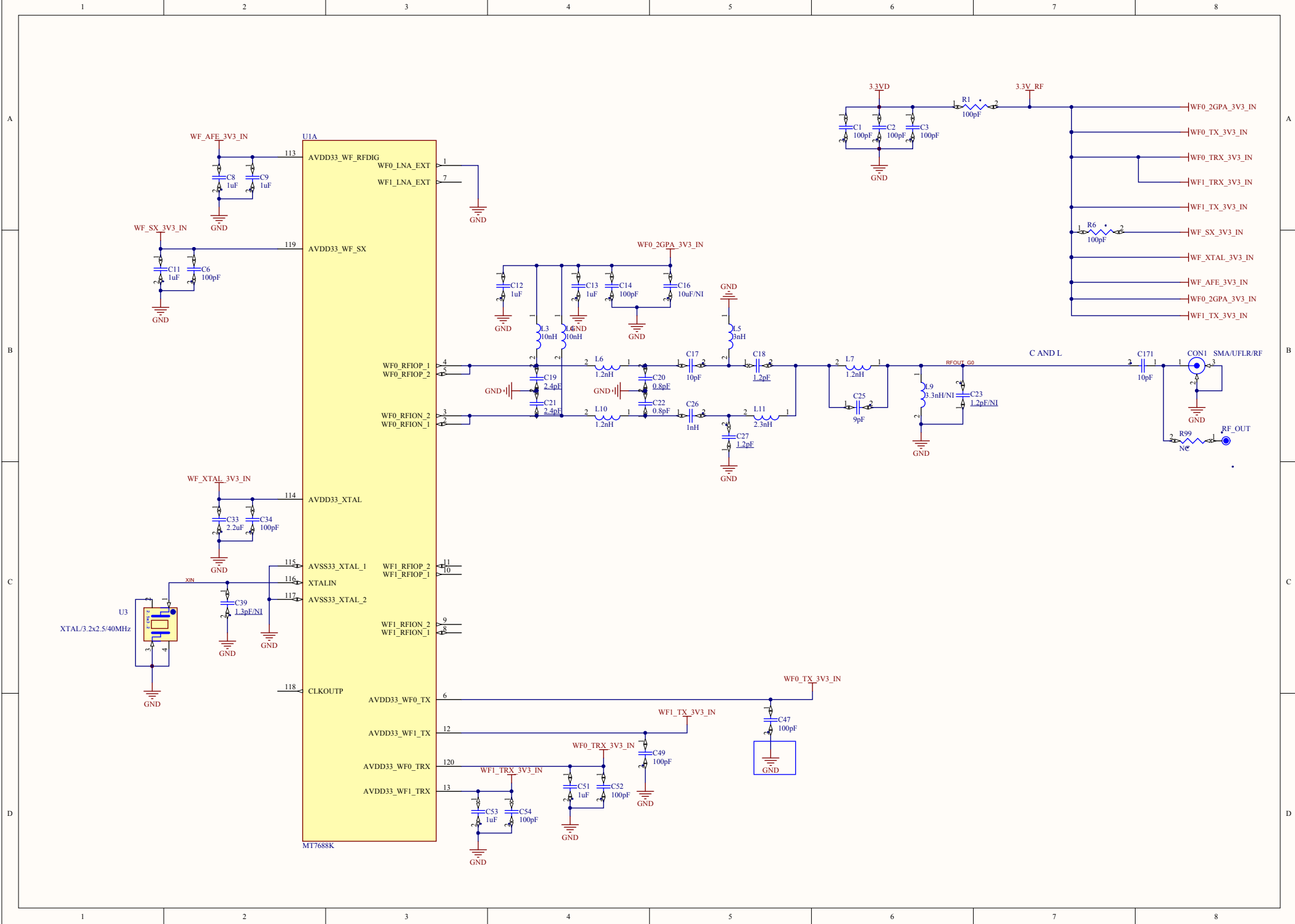




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|-------|-----------|--------|------------|----------|---|
| Title |           |        | PVW1 BS_VB |          |   |
| Size  | A3        | Number | Revision   |          |   |
| Date: | 2017/5/14 | File:  | E:\PVW1    | Sheet of | 1 |
| File: |           |        | E:\PVW1    | Sheet of | 1 |



1

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A

A

B

B

C

C

D

D

U1B

[MT7628K]  
1.8V for DDR1\_KGD(Default)

DDR\_IO\_1V8

66  
67  
78  
79

DDR\_IO\_1V8D\_1  
DDR\_IO\_1V8D\_2  
DDR\_IO\_1V8D\_3  
DDR\_IO\_1V8D\_4

DDR\_VREF

C57  
2.2uF

C58  
0.1uF

GND

GND

MT7688K

73  
76  
77

DDR\_IO\_VREF\_1  
DDR\_IO\_VREF\_2  
DDR\_IO\_VREF\_3

DDR\_IO\_VSS\_1  
DDR\_IO\_VSS\_2  
DDR\_IO\_VSS\_3

61  
62  
63

GND

DDR\_IO\_1V8

R13  
1K 1%

R14  
1K 1%

GND

C55  
0.1uF

C56  
0.1uF

DDR\_VREF

DDR\_VREF

DDR\_IO\_1V8

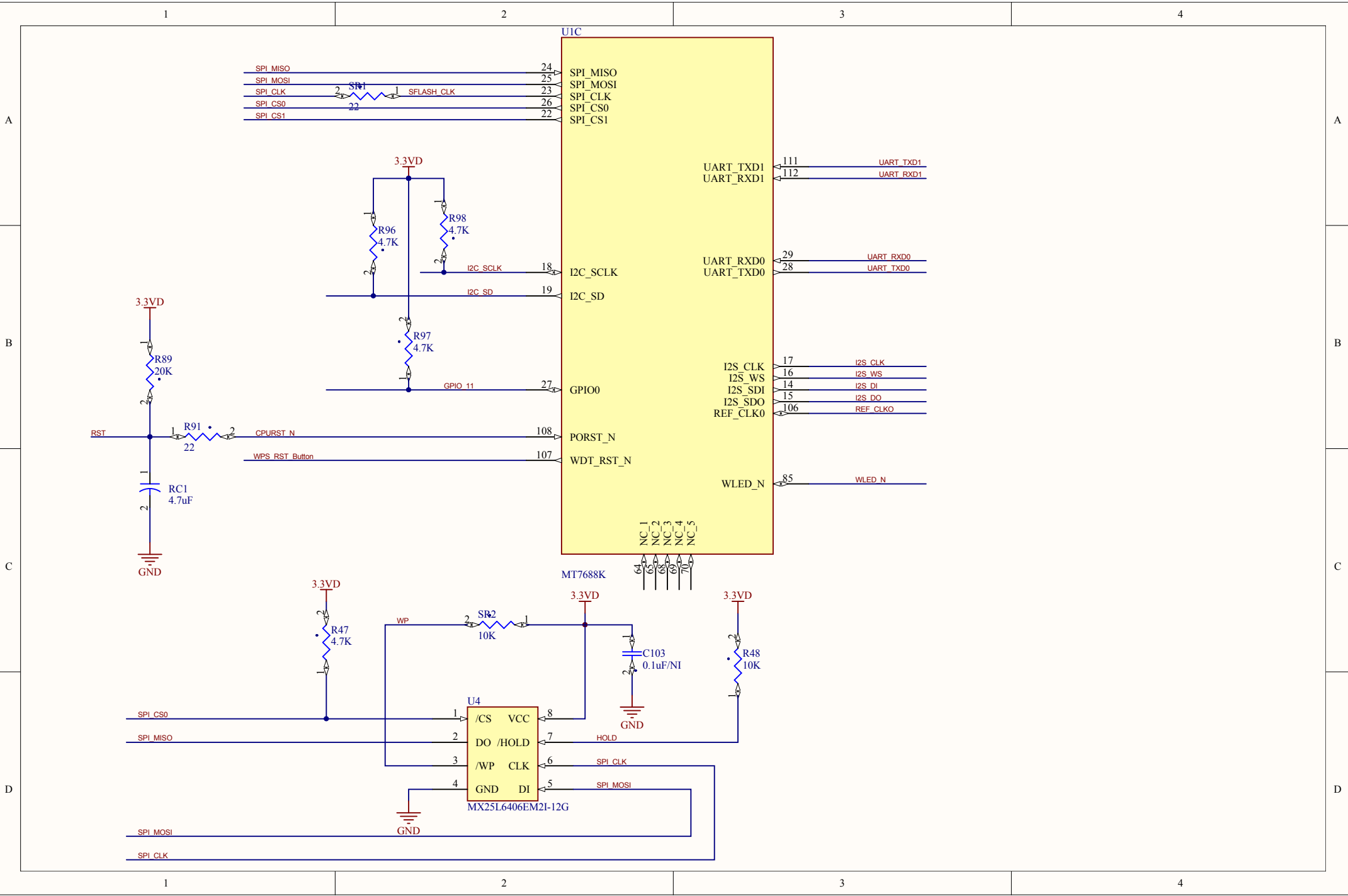
C59

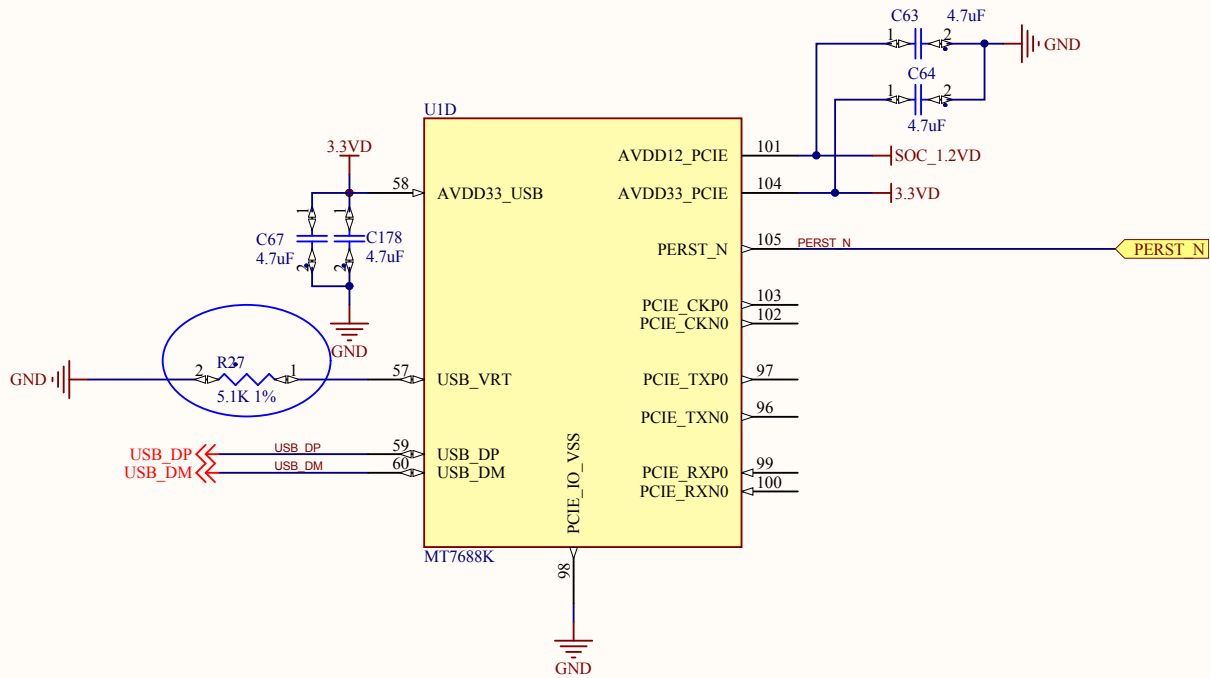
C60

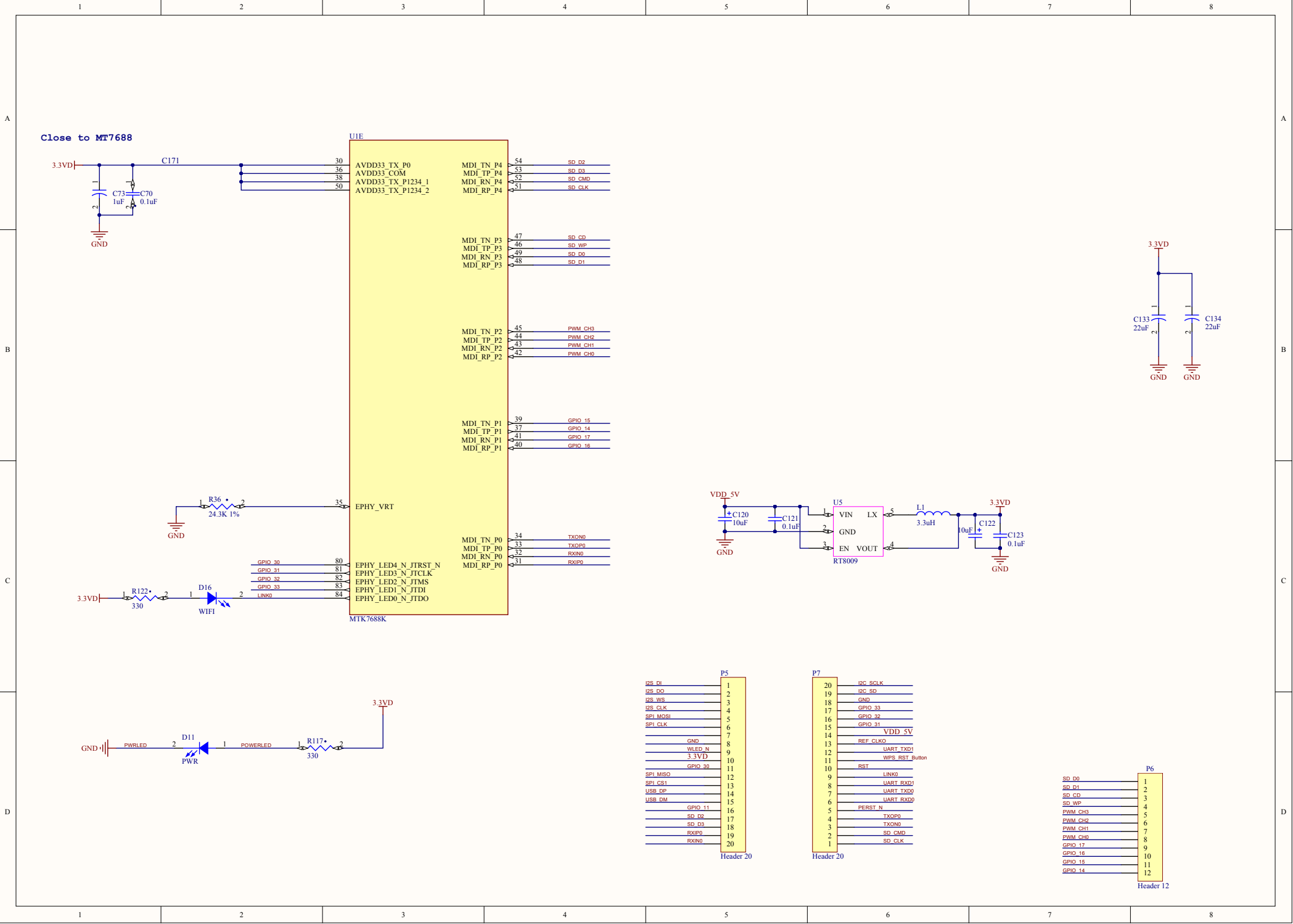
C61

0.1uF

GND

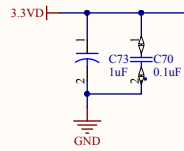






Close to MT7688

U1E



C171

C73

C70

1uF

0.1uF

GND



R36

24.3K 1%

D16

WIFI

GND

3.3V

R122

330

D16

WIFI

GND

LINK0

84

83

82

81

80

GPIO\_30

GPIO\_31

GPIO\_32

GPIO\_33

EPHY\_LED4\_N\_JTRST\_N

EPHY\_LED3\_N\_JTCLK

EPHY\_LED2\_N\_JTMS

EPHY\_LED1\_N\_JTDI

EPHY\_LED0\_N\_JTDO

MTK7688K

EPHY\_VRT

35

34

33

32

31

TXON0

TXOP0

RXIN0

RXIP0

MDI\_TP\_P0

MDI\_RN\_P0

MDI\_TP\_P1

MDI\_RN\_P1

MDI\_TP\_P2

MDI\_RN\_P2

MDI\_TP\_P3

MDI\_RN\_P3

MDI\_TP\_P4

MDI\_RN\_P4

MDI\_TP\_P5

MDI\_RN\_P5

MDI\_TP\_P6

MDI\_RN\_P6

MDI\_TP\_P7

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MDI\_TP\_P8

MDI\_RN\_P8

MDI\_TP\_P9

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MDI\_TP\_P10

MDI\_RN\_P10

MDI\_TP\_P11

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MDI\_TP\_P12

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MDI\_RN\_P126

MDI\_TP\_P127

MDI\_RN\_P127

MDI\_TP\_P128

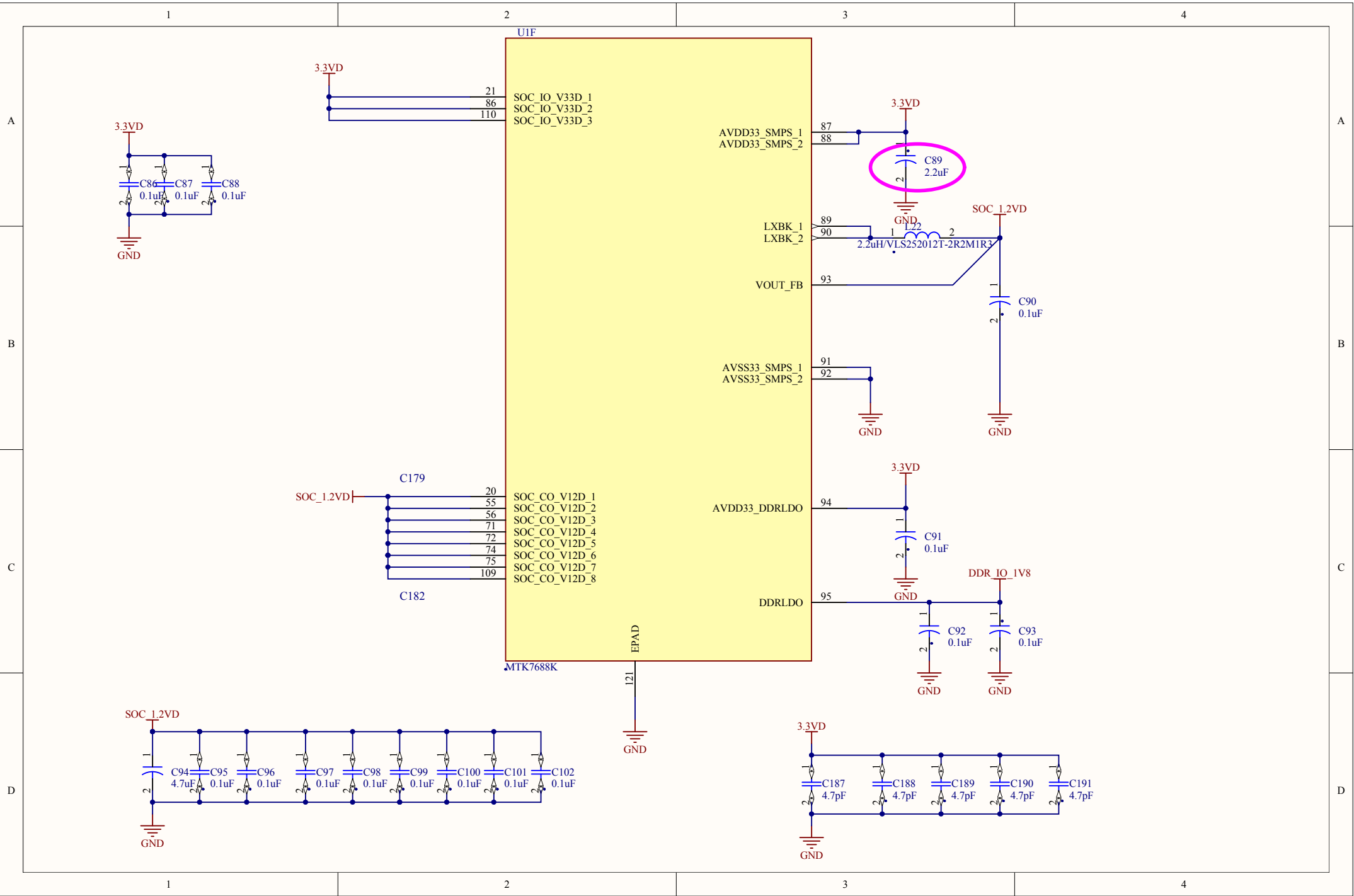
MDI\_RN\_P128

MDI\_TP\_P129

MDI\_RN\_P129

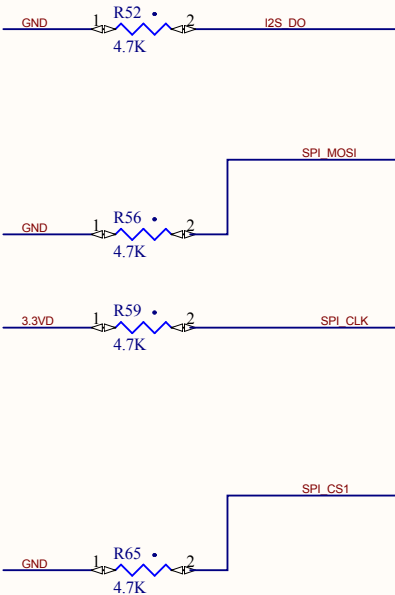
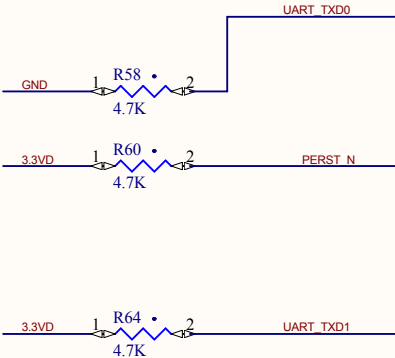
MDI\_TP\_P130

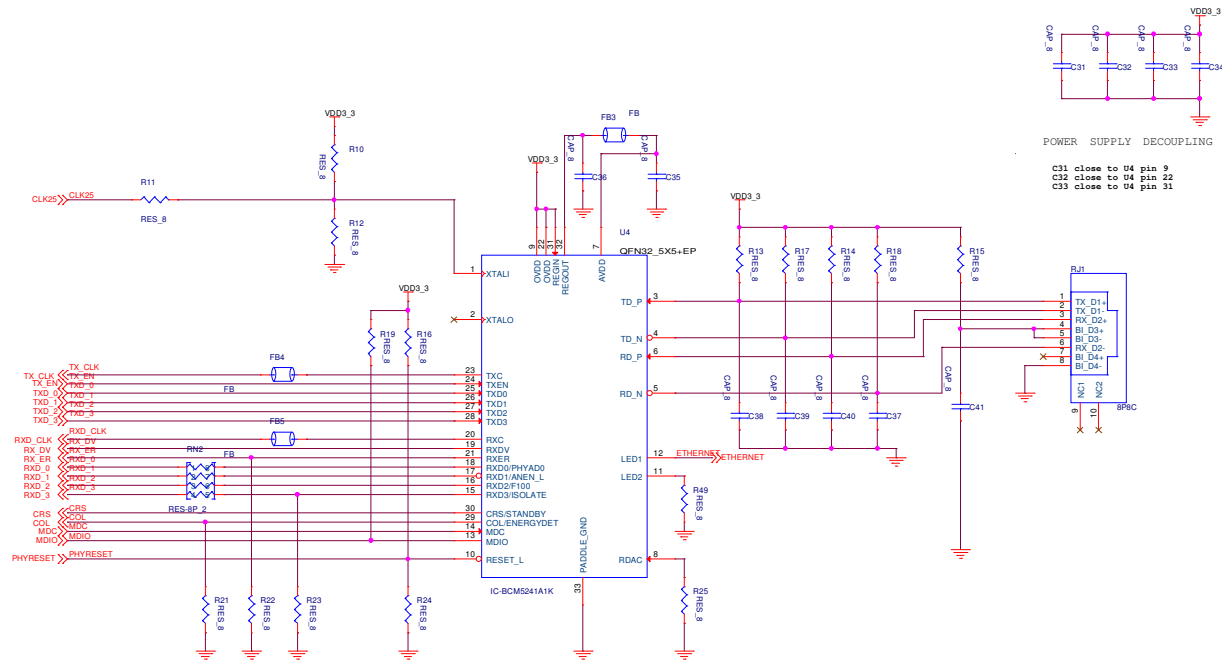
MDI\_RN\_P130



Bootstrapping Pins Description

| Pin Name                          | Boot Strapping Signal Name | Description                                                                                                                                                                                                                                               |
|-----------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| UART_TXD1                         | DBG_JTAG_MODE              | 0: JTAG_MODE<br>1: EPHY_LED (default)                                                                                                                                                                                                                     |
| PERST_N                           | XTAL_FREQ_SEL              | 0: 25 MHz DIP<br>1: 40 MHz SMD                                                                                                                                                                                                                            |
| I2S_SDO                           | DRAM_TYPE                  | 1: DDR1<br>0: DDR2<br>[note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.                                                                                                                            |
| {SPI_MOSI<br>SPI_CLK,<br>SPI_CS1} | CHIP_MODE[2:0]             | A vector to set chip function/test/debug modes.<br>000: Boot from PLL (boot from SPI 3-Byte Addr)<br>001: Boot from PLL (boot from SPI 4-Byte Addr)<br>010: Boot from XTAL (boot from SPI 3-Byte Addr)<br>011: Boot from XTAL (boot from SPI 4-Byte Addr) |
| PAD_TXD0                          | EXT_BGCK                   | 1: Test Mode<br>0: Normal (default)                                                                                                                                                                                                                       |

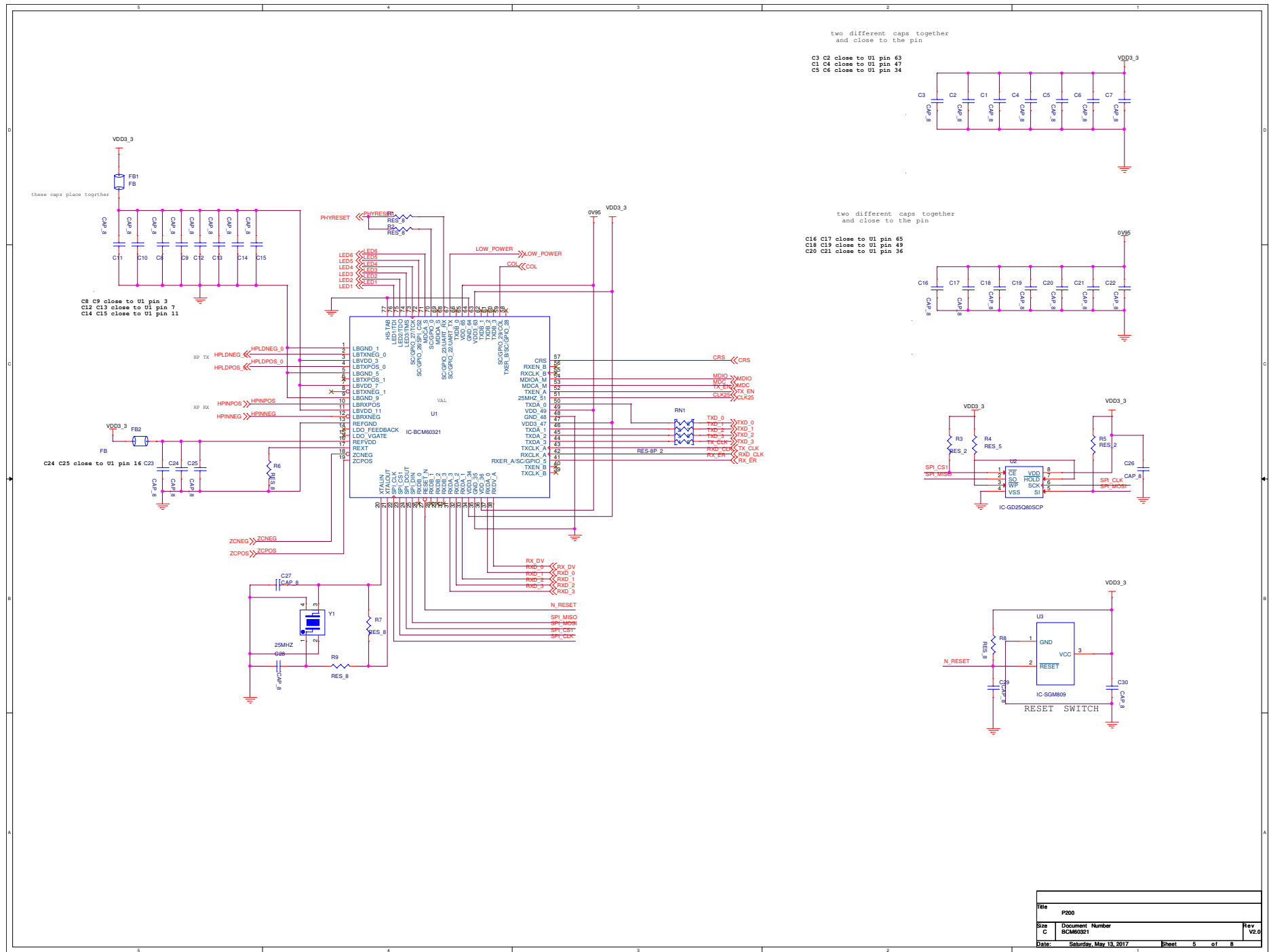


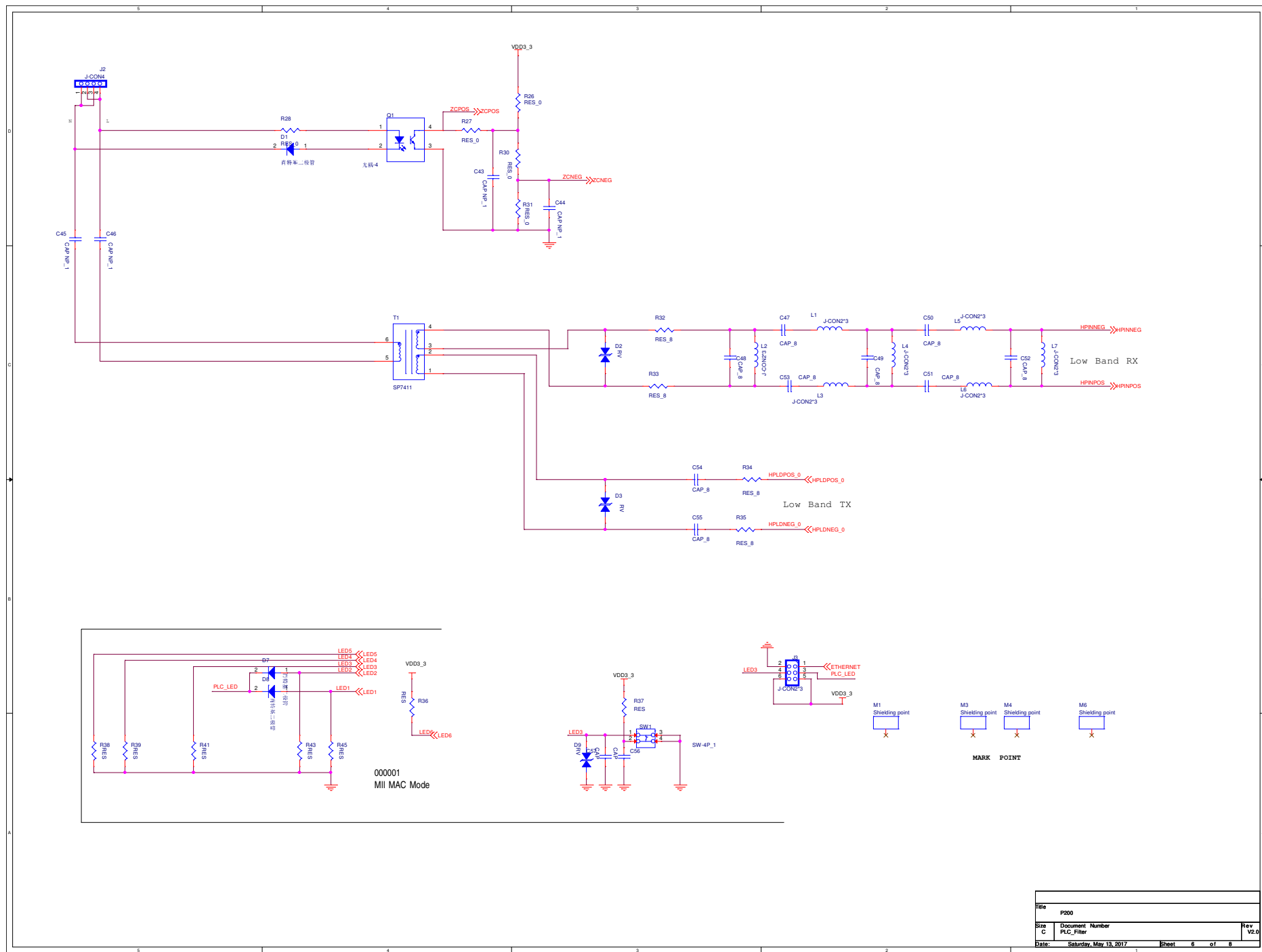


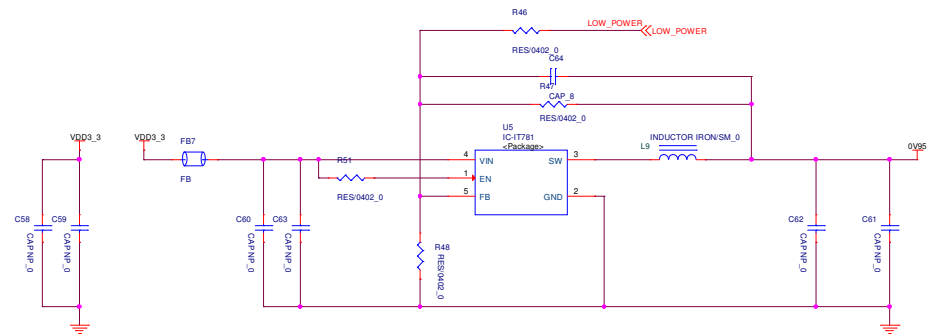
POWER SUPPLY DECOUPLING

C31 close to U4 pin 9  
C32 close to U4 pin 22  
C33 close to U4 pin 31

|       |                        |        |        |
|-------|------------------------|--------|--------|
| File  |                        |        |        |
| P200  |                        |        |        |
| Size  | Document               | Number | Rev    |
| C     | BCM5241_PWT            |        | V2.0   |
| Date: | Saturday, May 13, 2017 | Sheet  | 5 of 8 |







|       |                        |        |              |
|-------|------------------------|--------|--------------|
| Title |                        |        |              |
| P200  |                        |        |              |
| Size  | Document               | Number | Rev          |
| C     | DC-DC                  |        | V2.0         |
| Date: | Saturday, May 13, 2017 |        | Sheet 8 of 8 |