



Calterah Rhine CAL60S244-IB and CAL60S244-IB-A Datasheet

Release 1.1

Calterah Semiconductor

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INTRODUCTION

CAL60S244-IB(-A) is an antenna-in-package (AiP) radar sensor chip with 4 TX and 4 RX antenna array embedded in the package. It integrates a single-chip frequency-modulated continuous wave (FMCW) radar sensor capable of operation in 60- to 64-GHz band, and is built with advanced low-power 40-nm CMOS process and packaged with flip-chip technology. While inheriting Rhine CAL60S244-IE(-A) radar SoC features, Rhine CAL60S244-IB(-A) enables more compact and cost-efficient millimeter-wave radar solutions with its innovative design.

CAL60S244-IB(-A) utilizes a most advanced packaging technology with sophisticated antenna design. The overall size of the package is 12.2 mm × 12.2 mm. Yet its powerful antenna array and redundant channels provide flexibility in resolving angles on both azimuth and elevation planes. CAL60S244-IB(-A) can be used flexibly to cover the proper detection range and field of view (FoV), making it a perfect candidate for short and ultra-short range applications in the industrial market and future intelligent devices.

Note: *CAL60S244-IB-A* is a variant based on the part number CAL60S244-IB.

Table 1.1 summarizes the major functionality differences between the baseline part number CAL60S244-IB and the variant part number CAL60S244-IB-A. Throughout this document, pay attention to the differentiation of part numbers, which stand for different chip devices with different functions. This table applies to and rules over the whole document.

Table 1.1: Differences between *CAL60S244-IB* and *CAL60S244-IB-A*

Functionality	CAL60S244-IB	CAL60S244-IB-A
Hardware Auto Frame Mode	Not available	Available
Doppler spur randomization	Not available	Available
DMA	Not available	Available
Robust boot ²	Not available	Available

Fig. 1.1 illustrates the arrangement of CAL60S244-IB(-A) antenna array.

² Robust boot refers to the implementation with two copies of identical payload during boot. For details, see *Calterah Rhine Reference Manual*.

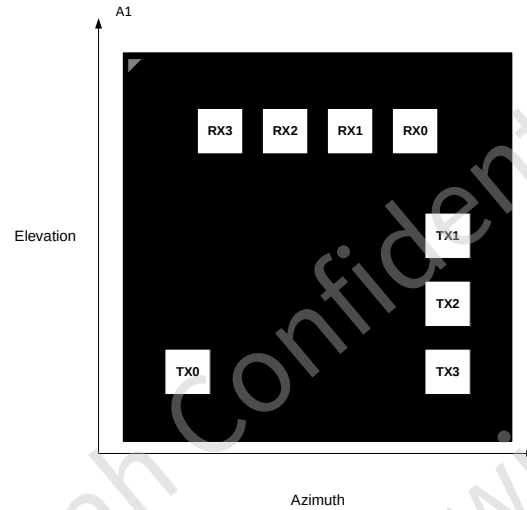


Fig. 1.1: CAL60S244-IB(-A) Antenna Array

Besides CAL60S244-IB(-A), Rhine family also includes:

- CAL60S244-IE(-A), a 4T4R radar sensor chip.

For details, refer to *Calterah Rhine CAL60S244-IE and CAL60S244-IE-A Datasheet*.

- CAL60S244-AB(-AN), an antenna-in-package (AiP) radar sensor chip with 4 TX and 4 RX antenna array embedded in the package.

The difference between CAL60S244-IB(-A) and CAL60S244-AB(-AN) is that CAL60S244-IB(-A) is an industrial-grade product and does not support CAN or CAN FD functions, while CAL60S244-AB(-AN) supports CAN and CAN FD functions.

For details, refer to *Calterah Rhine CAL60S244-AB and CAL60S244-AB-AN Datasheet*.

- CAL60S244-IH-A, another antenna-in-package (AiP) radar sensor chip with 4 TX and 4 RX antenna array embedded in the package.

For details, refer to *Calterah Rhine CAL60S244-IH-A Datasheet*.

For an overview and full feature descriptions of the whole Rhine family of mmWave radar sensor chips, refer to *Calterah Rhine Reference Manual*.

1.1 Features

- Four-channel 60-GHz transmitter with antenna
 - Maximum effective isotropic radiated power (EIRP): 21 dBm³
 - Phase shifter
 - Supports binary phase shift keying (BPSK) modulation
- Four-channel 60-GHz receiver with antenna
 - Broadside radiation with more than 2 dBi Gain

³ This value is measured in TX1-2-3 combination mode at $T_A = 25^\circ\text{C}$.

- Linearity (OP1dB) > 11 dBm
- Conversion gain 32 dB to 73 dB at 5.0 MHz
- Integrated high-pass filters
- Typical single-sideband (SSB) noise figure: 15 dB at 5.0 MHz
- Baseband IF peak detectors
- Baseband output driver
- 60-GHz frequency synthesizer
 - Bandwidth 0.8/3 MHz with integrated loop filter
 - Supports 40 MHz crystal/reference clock for 60 GHz to 64 GHz
 - Supports configurable FMCW signal generation
 - Supports output synchronization signal
- Four-channel analog-to-digital converters (ADCs)
 - Sampling rates: up to 50 MS/s
- Power management
 - Built-in low-dropout regulator (LDO) network
- Four-channel low-voltage differential signaling (LVDS) data interface
- Built-in self-test
- CPU
 - 32 KiB I-Cache
 - 32 KiB D-Cache
 - 32 KiB instruction close coupled memory (ICCM)
 - 32 KiB data close coupled memory (DCCM)
 - Timer × 2
 - Watchdog timer
 - Single precision floating point unit (FPU)
 - 16 MPU regions
- Memory
 - Baseband: 2 MiB
 - * 1 MiB could be shared with CPU in static share mode
 - CPU: 576 KiB
- Peripherals
 - Universal asynchronous receiver/transmitter (UART) × 2
 - Inter-integrated circuit (I²C) master
 - Quad serial peripheral interface (QSPI) master
 - Serial peripheral interface (SPI) master × 2
 - SPI slave/QSPI slave



1.2. Applications

- General-purpose input/output (GPIO)
- One-time programmable (OTP) memory
- Timer × 4
- Pulse width modulator (PWM) × 2
- Baseband
 - Virtual array frame
 - * Time-division modulation (TDM)
 - * Binary-phase modulation (BPM)
 - Digital decimation: up to factor of 16
 - Anti-interference
 - Configurable FFT sizes: up to 2048
 - Configurable CFAR window size: up to 21×21
 - Configurable CFAR type:
 - * Cell averaging (CA)
 - * Ordered statistics (OS)
 - * Smallest order and greatest order (SOGO)
 - * Noise reference (NR)
 - Output objects: up to 1024 objects
 - Multi-object DoA: up to 4 objects per bin
 - Super resolution support
 - Frame interleaving
- Error management unit (EMU)
- Operating conditions:
 - Junction temperature range of –40°C to 105°C

1.2 Applications

- Industrial radar systems

1.3 Chip Block Diagram

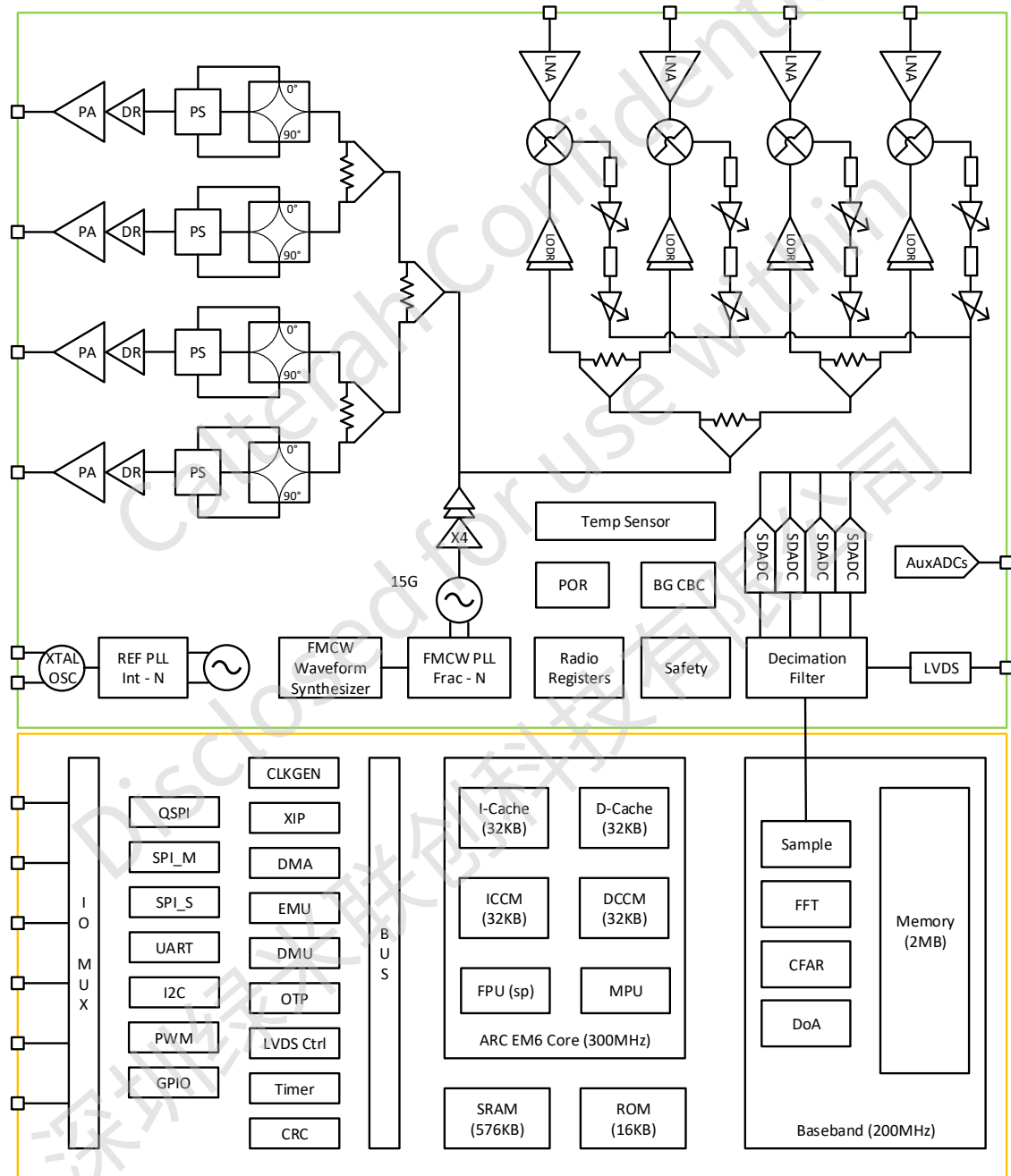


Fig. 1.2: Chip Block Diagram^{Page 9, 5}

⁵ The DMA module is *not* available in the baseline part number CAL60S244-IB, which is described in the corresponding silicon errata document.



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DEVICE INFORMATION

2.1 Pinout

Fig. 2.1 shows a top view of the layout and arrangement of the signal pads.

2.1. Pinout

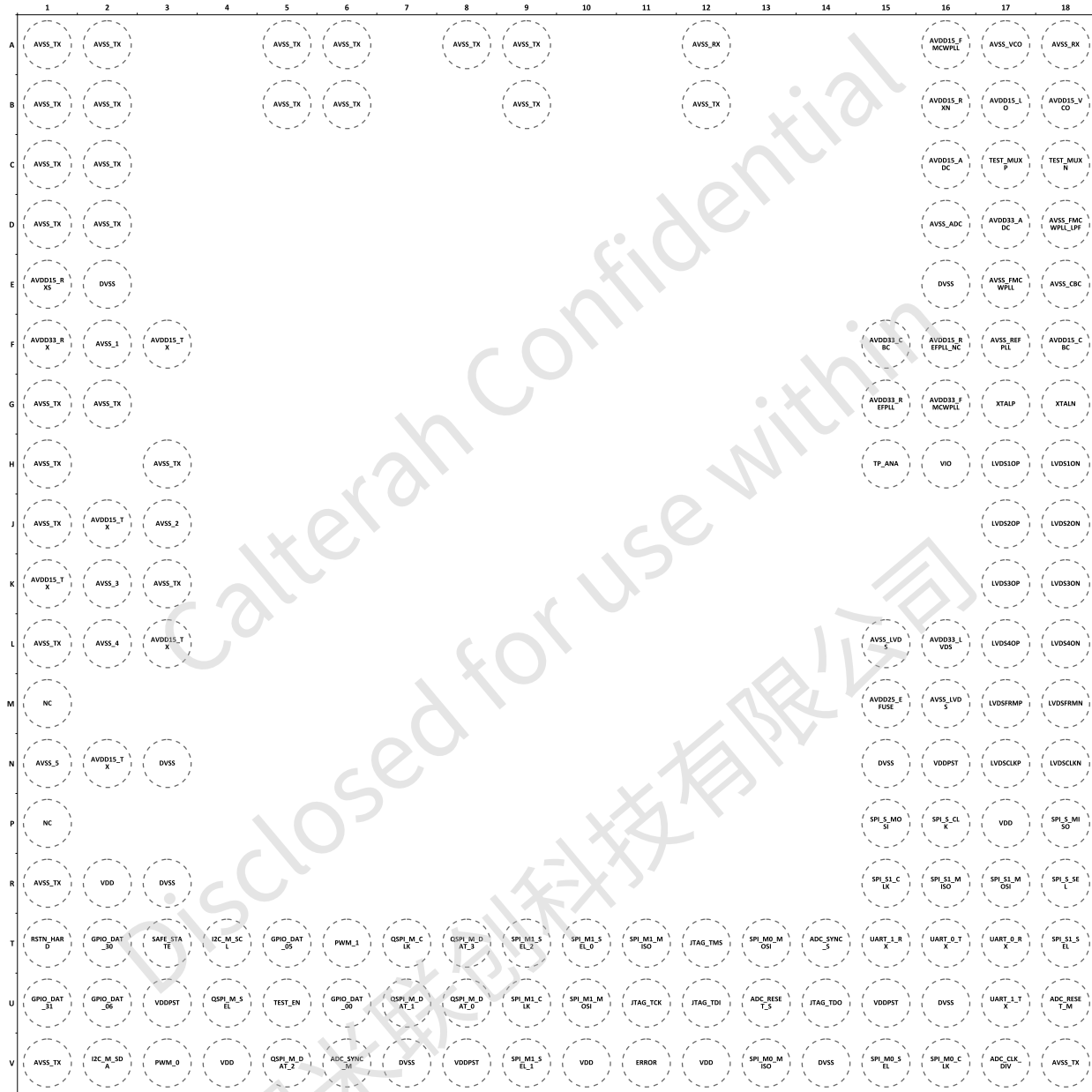


Fig. 2.1: Chip Pin Diagram (Top View)

You can view the functional description of each pin in [Table 2.1](#) and the pin multiplexing in [Table 2.2](#).

Table 2.1: Chip Signal Definitions

Pin Name	Ball Location	Description	Pin Type	Level(V)
LVDS1OP	H17	Differential IF output Channel 1 (10 KHz-20 MHz)/ Differential LVDS output Channel 1 (400 M)	AO	0-2.5
LVDS1ON	H18	Differential IF output Channel 1 (10 KHz-20 MHz)/ Differential LVDS output Channel 1 (400 M)	AO	0-2.5
LVDS2OP	J17	Differential IF output Channel 2 (10 KHz-20 MHz)/ Differential LVDS output Channel 2 (400 M)	AO	0-2.5
LVDS2ON	J18	Differential IF output Channel 2 (10 KHz-20 MHz)/ Differential LVDS output Channel 2 (400 M)	AO	0-2.5

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Table 2.1 – continued from previous page

Pin Name	Ball Location	Description	Pin Type	Level(V)
LVDS3OP	K17	Differential IF output Channel 3 (10 KHz-20 MHz)/ Differential LVDS output Channel 3 (400 M)	AO	0-2.5
LVDS3ON	K18	Differential IF output Channel 3 (10 KHz-20 MHz)/ Differential LVDS output Channel 3 (400 M)	AO	0-2.5
LVDS4OP	L17	Differential IF output Channel 4 (10 KHz-20 MHz)/ Differential LVDS output Channel 4 (400 M)	AO	0-2.5
LVDS4ON	L18	Differential IF output Channel 4 (10 KHz-20 MHz)/ Differential LVDS output Channel 4 (400 M)	AO	0-2.5
LVDSFRMP	M17	Differential LVDS output frame (20M/25M/40M/50M)	AO	0-2.5
LVDSFRMN	M18	Differential LVDS output frame (20M/25M/40M/50M)	AO	0-2.5
LVDSCLKP	N17	Differential LVDS output clock (200 M)	AO	0-2.5
LVDSCLKN	N18	Differential LVDS output clock (200 M)	AO	0-2.5
TEST_MUXN	C18	Differential test signal input	AI	0-2.5
TEST_MUXP	C17	Differential test signal input	AI	0-2.5
XTALP	G17	Crystal oscillator input	AI	0-2.5
XTALN	G18	Crystal oscillator input	AI	0-2.5
TP_ANA	H15	DC test signal	AIO	0-3.3
VIO	H16	PLL test signal output	AO	0-2.5
AVDD15_ADC	C16	1.5-V power supply	P	1.5
AVDD15_FMCWPLL	A16	1.5-V power supply	P	1.5
AVDD15_CBC	F18	1.5-V power supply	P	1.5
AVDD15_RXN	B16	1.5-V power supply	P	1.5
AVDD15_LO	B17	1.5-V power supply	P	1.5
AVDD15_REFPLL	F16	1.5-V power supply	P	1.5
AVDD15_RXS	E1	1.5-V power supply	P	1.5
AVDD15_TX	F3, J2, K1, L3, N2	1.5-V power supply	P	1.5
AVDD15_VCO	B18	1.5-V power supply	P	1.5
AVDD25_OTP	M15	2.5-V power supply	P	2.5
AVDD33_ADC	D17	3.3-V power supply	P	3.3
AVDD33_FMCWPLL	G16	3.3-V power supply	P	3.3
AVDD33_REFPLL	G15	3.3-V power supply	P	3.3
AVDD33_CBC	F15	3.3-V power supply	P	3.3
AVDD33_LVDS	L16	3.3-V power supply	P	3.3
AVDD33_RX	F1	3.3-V power supply	P	3.3
VDDPST	N16, U3, U15, V8	3.3-V power supply	P	3.3
DVDD	P17, R2, V4, V10, V12	1.15-V power supply	P	1.15
AVSS	F2, J3, K2, L2, N1	DC ground	P	0
AVSS_CBC	E18	DC ground	P	0
AVSS_LVDS	L15, M16	DC ground	P	0
AVSS_VCO	A17	DC ground	P	0
AVSS_FMCWPLL	E17, D18	DC ground	P	0
AVSS_REFPLL	F17	DC ground	P	0
AVSS_ADC	D16	DC ground	P	0
DVSS	E2, E16, N3, N15, R3, U16, V7, V14	DC ground	P	0
AVSS_RX	A12, A18	DC ground	P	0
AVSS_TX	A1, A2, A5, A6, A8, A9, B1, B2, B5, B6, B9, B12, C1, C2, D1, D2, G1, G2, H1, H3, J1, K3, L1, R1, V1, V18	DC ground	P	0
SPI_S_CLK	P16	SPIS serial clock	DIO	0-3.3
SPI_S_MISO	P18	SPIS master input slave output	DIO	0-3.3
SPI_S_SEL	R18	SPIS slave selection signal	DIO	0-3.3
SPI_S_MOSI	P15	SPIS master output slave input	DIO	0-3.3
SPI_S1_MISO	R16	SPIS master input slave output	DIO	0-3.3
SPI_S1_MOSI	R17	SPIS master output slave input	DIO	0-3.3
SPI_S1_SEL	T18	SPIS slave selection signal	DIO	0-3.3
SPI_S1_CLK	R15	SPIS serial clock	DIO	0-3.3
UART_0_TX	T16	UART0 TX signal	DIO	0-3.3
UART_0_RX	T17	UART0 RX signal	DIO	0-3.3
UART_1_TX	U17	UART1 TX signal	DIO	0-3.3
UART_1_RX	T15	UART1 RX signal	DIO	0-3.3

continues on next page



2.1. Pinout

Table 2.1 – continued from previous page

Pin Name	Ball Location	Description	Pin Type	Level(V)
ADC_RESET_M	U18	ADC reset master output	DIO	0-3.3
ADC_RESET_S	U13	ADC reset slave input	DIO	0-3.3
ADC_SYNC_M	V6	ADC sync master output	DIO	0-3.3
ADC_SYNC_S	T14	ADC sync slave input	DIO	0-3.3
ADC_CLK_DIV	V17	ADC clock	DIO	0-3.3
SPI_M0_CLK	V16	SPI M0 serial clock	DIO	0-3.3
SPI_M0_SEL	V15	SPI M0 slave selection signal	DIO	0-3.3
SPI_M0_MOSI	T13	SPI M0 master out slave in	DIO	0-3.3
SPI_M0_MISO	V13	SPI M0 master in slave out	DIO	0-3.3
JTAG_TDO	U14	JTAG test data out	DO	0-3.3
JTAG_TDI	U12	JTAG test data in	DIO	0-3.3
JTAG_TMS	T12	JTAG test mode select	DIO	0-3.3
JTAG_TCK	U11	JTAG test clock	DIO	0-3.3
ERROR	V11	Error signal output	DO	0-3.3
SPI_M1_MISO	T11	SPI M1 master in slave out	DIO	0-3.3
SPI_M1_MOSI	U10	SPI M1 master out slave in	DIO	0-3.3
SPI_M1_SEL_0	T10	SPI M1 slave selection signal	DIO	0-3.3
SPI_M1_SEL_1	V9	SPI M1 slave selection signal	DIO	0-3.3
SPI_M1_SEL_2	T9	SPI M1 slave selection signal	DIO	0-3.3
SPI_M1_CLK	U9	SPI M1 serial clock	DIO	0-3.3
QSPI_M_DAT_0	U8	QSPI input/output data	DIO	0-3.3
QSPI_M_DAT_1	U7	QSPI input/output data	DIO	0-3.3
QSPI_M_DAT_2	V5	QSPI input/output data	DIO	0-3.3
QSPI_M_DAT_3	T8	QSPI input/output data	DIO	0-3.3
QSPI_M_SEL	U4	QSPI slave selection signal	DO	0-3.3
QSPI_M_CLK	T7	QSPI serial clock	DO	0-3.3
TEST_EN	U5	Test mode enable	DI	0-3.3
GPIO_DAT_00	U6	General Purpose IO	DIO	0-3.3
PWM_1	T6	PWM1 output	DIO	0-3.3
PWM_0	V3	PWM0 output	DIO	0-3.3
I2C_M_SDA	V2	I2CM data	DIO	0-3.3
I2C_M_SCL	T4	I2CM clock	DIO	0-3.3
GPIO_DAT_05	T5	General Purpose IO	DIO	0-3.3
GPIO_DAT_06	U2	General Purpose IO	DIO	0-3.3
GPIO_DAT_30	T2	General Purpose IO	DIO	0-3.3
GPIO_DAT_31	U1	General Purpose IO	DIO	0-3.3
SAFE_STATE	T3	Safe mode status	DO	0-3.3
RSTN_HARD	T1	Hard reset on board	DI	0-3.3
NC	P1, M1	No connection	/	/

Table 2.2: Pin Multiplexing

Pin Name	Pin Control Address (Default)	Pin Control Value (0)	Pin Control Value (1)	Pin Control Value (2)	Pin Control Value (3)	Pin Control Value (4)	Reset State
TEST_EN	/	test_en_i	/	/	/	/	Input with Pull Up
QSPI_M_CLK	/	qspi_m_clk_o	/	/	/	/	Output 0
QSPI_M_SEL	/	qspi_m_sel_o	/	/	/	/	Output 1
QSPI_M_DAT_3	/	qspi_m_dat_3_io	/	/	/	/	Input with Pull Up
QSPI_M_DAT_2	/	qspi_m_dat_2_io	/	/	/	/	Input with Pull Up
QSPI_M_DAT_1	/	qspi_m_dat_1_io	/	/	/	/	Input with Pull Up
QSPI_M_DAT_0	/	qspi_m_dat_0_io	/	/	/	/	Input with Pull Up
SPI_M1_CLK	0xBA0204 (0x4)	spi_m1_clk_o	pwm_2_o	qspi_m1_clk_o	/	dbgbus_clk_o	Output 0

continues on next page



Table 2.2 – continued from previous page

Pin Name	Pin Control Address (Default)	Pin Control Value (0)	Pin Control Value (1)	Pin Control Value (2)	Pin Control Value (3)	Pin Control Value (4)	Reset State
SPI_M1_SEL_2	0xBA0204 (0x4)	spi_m1_sel_2_o	pwm_3_o	qspi_m1_dat_3_io	/	dbgbus_val_io	Input with Pull Up
SPI_M1_SEL_1	0xBA0204 (0x4)	spi_m1_sel_1_o	pwm_4_o	qspi_m1_dat_2_io	/	dbgbus_dat_16_io	Input with Pull Up
SPI_M1_SEL_0	0xBA0204 (0x4)	spi_m1_sel_0_o	pwm_5_o	qspi_m1_sel_o	/	dbgbus_dat_15_io	Input with Pull Up
SPI_M1_MOSI	0xBA0204 (0x4)	spi_m1_mosi_o	pwm_6_o	qspi_m1_dat_0_io	/	dbgbus_dat_14_io	Input with Pull Up
SPI_M1_MISO	0xBA0204 (0x4)	spi_m1_miso_i	pwm_7_o	qspi_m1_dat_1_io	/	dbgbus_dat_13_io	Input with Pull Up
SPI_S1_CLK	0xBA023C (0x0)	spi_s1_clk_i	/	fmcw_start_i	pwm_4_o	dbgbus_dat_12_io	Input with Pull Up
SPI_S1_SEL	0xBA0240 (0x0)	spi_s1_sel_i	/	/	pwm_5_o	dbgbus_dat_11_io	Input with Pull Up
SPI_S1_MOSI	0xBA0244 (0x0)	spi_s1_mosi_i	/	qspi_s_dat_3_io	pwm_6_o	dbgbus_dat_10_io	Input with Pull Up
SPI_S1_MISO	0xBA0248 (0x0)	spi_s1_miso_o	/	qspi_s_dat_2_io	pwm_7_o	dbgbus_dat_09_io	Output 0
UART_0_TX	0xBA0208 (0x0)	uart_0_tx_o	uart_1_tx_o	/	/	/	Output 1
UART_0_RX	0xBA0208 (0x0)	uart_0_rx_i	uart_1_rx_i	/	/	/	Input with Pull Up
UART_1_TX	0xBA020C (0x4)	uart_1_tx_o	/	/	uart_0_tx_o	dbgbus_dat_08_io	Input with Pull Up
UART_1_RX	0xBA020C (0x4)	uart_1_rx_i	/	/	uart_0_rx_i	dbgbus_dat_07_io	Input with Pull Up
GPIO_DAT_31	0xBA0210 (0x4)	/	/	uart_0_tx_o	pwm_2_o	dbgbus_dat_31_io	Input with Pull Up
GPIO_DAT_30	0xBA0210 (0x4)	/	/	uart_0_rx_i	pwm_3_o	dbgbus_dat_30_io	Input with Pull Up
GPIO_DAT_06	0xBA0214 (0x4)	/	uart_0_tx_o	pwm_2_o	/	dbgbus_dat_06_io	Input with Pull Up
GPIO_DAT_05	0xBA0214 (0x4)	/	uart_0_rx_i	pwm_3_o	/	dbgbus_dat_05_io	Input with Pull Up
ADC_RESET_M	0xBA0218 (0x0)	adc_reset_m_o	adc_sync_m_o	i2c_m_scl_io	pwm_0_o	dbgbus_dat_29_io	Output 1
ADC_RESET_S	0xBA0218 (0x0)	adc_reset_s_i	adc_sync_s_i	i2c_m_sda_io	pwm_1_o	dbgbus_dat_28_io	Input with Pull Up
ADC_SYNC_M	0xBA021C (0x0)	adc_sync_m_o	i2c_m_scl_io	pwm_0_o	adc_reset_m_o	dbgbus_dat_27_io	Output 0
ADC_SYNC_S	0xBA021C (0x0)	adc_sync_s_i	i2c_m_sda_io	pwm_1_o	adc_reset_s_i	dbgbus_dat_26_io	Input with Pull Up
I2C_M_SCL	0xBA0220 (0x4)	i2c_m_scl_io	pwm_0_o	adc_reset_m_o	adc_sync_m_o	dbgbus_dat_04_io	Input with Pull Up
I2C_M_SDA	0xBA0220 (0x4)	i2c_m_sda_io	pwm_1_o	adc_reset_s_i	adc_sync_s_i	dbgbus_dat_03_io	Input with Pull Up
PWM_0	0xBA0224 (0x4)	pwm_0_o	adc_reset_m_o	adc_sync_m_o	i2c_m_scl_io	dbgbus_dat_02_io	Input with Pull Up
PWM_1	0xBA0228 (0x4)	pwm_1_o	adc_reset_s_i	adc_sync_s_i	i2c_m_sda_io	dbgbus_dat_01_io	Input with Pull Up
ADC_CLK_DIV	0xBA022C (0x4)	adc_clk_div_o	/	/	/	dbgbus_dat_25_io	Input with Pull Up
GPIO_DAT_00	0xBA0230 (0x4)	/	/	/	/	dbgbus_dat_00_io	Input with Pull Up
SPI_M0_CLK	0xBA0234 (0x4)	spi_m0_clk_o	spi_s_clk_i	/	/	dbgbus_dat_24_io	Input with Pull Up
SPI_M0_SEL	0xBA0234 (0x4)	spi_m0_sel_o	spi_s_sel_i	/	/	dbgbus_dat_23_io	Input with Pull Up
SPI_M0_MOSI	0xBA0234 (0x4)	spi_m0_mosi_o	spi_s_mosi_i	/	/	dbgbus_dat_22_io	Input with Pull Up
SPI_M0_MISO	0xBA0234 (0x4)	spi_m0_miso_i	spi_s_miso_o	/	/	dbgbus_dat_21_io	Input with Pull Up

continues on next page



2.1. Pinout

Table 2.2 – continued from previous page

Pin Name	Pin Control Address (Default)	Pin Control Value (0)	Pin Control Value (1)	Pin Control Value (2)	Pin Control Value (3)	Pin Control Value (4)	Reset State
SPI_S_CLK	0xBA0238 (0x4)	spi_s_clk_i	spi_m0_clk_o	qspi_s_clk_i	/	dbgbus_dat_20_io	Input with Pull Up
SPI_S_SEL	0xBA0238 (0x4)	spi_s_sel_i	spi_m0_sel_o	qspi_s_sel_i	/	dbgbus_dat_19_io	Input with Pull Up
SPI_S_MOSI	0xBA0238 (0x4)	spi_s_mosi_i	spi_m0_mosi_o	qspi_s_dat_0_io	/	dbgbus_dat_18_io	Input with Pull Up
SPI_S_MISO	0xBA0238 (0x4)	spi_s_miso_o	spi_m0_miso_i	qspi_s_dat_1_io	/	dbgbus_dat_17_io	Input with Pull Up
ERROR	/	error_o	/	/	/	/	Output 1
JTAG_TCK	0xBA024C (0x0)	jtag_tck_i	/	pwm_4_o	/	/	Input with Pull Up
JTAG_TMS	0xBA024C (0x0)	jtag_tms_i	/	pwm_5_o	/	/	Input with Pull Up
JTAG_TDI	0xBA024C (0x0)	jtag_tdi_i	/	pwm_6_o	/	/	Input with Pull Up
JTAG_TDO	0xBA024C (0x0)	jtag_tdo_o	/	pwm_7_o	/	/	Output 0
RSTN_HARD	/	rstn_hard_i	/	/	/	/	Input with Pull Up
SAFE_STATE	/	safe_state_o	/	/	/	/	Output 1



SPECIFICATIONS

Note: All the specifications are at $T_A = 25^\circ\text{C}$, $V_{DD33} = 3.3\text{ V}$, $V_{DD25} = 2.5\text{ V}$, $V_{DD15} = 1.5\text{ V}$, and $V_{DD} = 1.15\text{ V}$, unless otherwise noted.

3.1 Absolute Maximum Ratings

Table 3.1 shows all absolute maximum ratings. Without specification, voltages are referred to ground. Exceeding the ratings may cause malfunction or permanent damage.

Table 3.1: Maximum Ratings

Symbol	Description	Min	Max	Unit
Vstatic_max	Supply voltage (static)	-0.3	3.63	V
Vdyn_max	Supply voltage (dynamic) Nominal VCC +20%, for short time. If applied for extended time, lifetime is degraded.	-0.3	4	V
Vdigio_max	Digital supply voltage for IO (static, dynamic)	-0.3	3.63	V
Vin_max	Voltage applied to all I/O pins	-0.3	3.63	V
Vdig_max	Digital supply voltage (static, dynamic)	-0.3	1.21	V
T_J	Operating junction temperature range	-40	105	$^\circ\text{C}$
$T_{\text{STG_before}}$	Storage temperature range before reflow soldering ¹	-55	150	$^\circ\text{C}$
$T_{\text{STG_after}}$	Storage temperature range after the first reflow cycle ²	-40	125	$^\circ\text{C}$

¹ Exposure for a long time to very low or very high temperatures may affect product reliability.

² Exposure for a long time to very low or very high temperatures may affect product reliability.

3.2 ESD Ratings

Table 3.2: ESD Ratings

Symbol	Description	Min	Max	Unit
HBM	ESD for human body model (HBM) digital I/O, analog, RF	-2000	2000	V
CDM	ESD for charged device model (CDM)	-450	450	V

3.3 Power Supply Specifications

Table 3.3 describes the four supply rails of Calterah Rhine CAL60S244-IB(-A) and Table 3.4 summarizes the power consumption under each supply rail.

Table 3.3: Power Supply Rails

Relevant I/Os	Blocks Powered by Supply	Min	Typ	Max	Unit
VDD33_LVDS, VDD33_ADC, VDD33_FMCWPLL, VDD33_REFPLL, VDD33_CBC, VDD33_RX	Digital I/Os, Buffers, DACs, PFD, Charge Pump, VGA1, VGA2, CBC, LVDS, PoR	3.14	3.3	3.47	V
VDD25_OTP	OTP	2.38	2.5	2.63	V
VDD15_ADC, VDD15_FMCWPLL, VDD15_REFPLL, VDD15_VCO, VDD15_LO, VDD15_CBC, VDD15_RXN, VDD15_RXS, AVDD15_TX	Amplifiers, Comparators, VCO, MMD, Mixers, LO, TIA, TX, PA, PMU	1.43	1.5	1.58	V
VDD	CPU, SRAMs, Digital Logic	1.10	1.15	1.21	V

Table 3.4: Current Consumption under Each Power Supply Rail

Parameter	Description	Min	Typ	Max	Unit
I_{DD33}	Total current under 3.3-V supply	/	140	180	mA
I_{DD25}	Total current under 2.5-V supply	/	40	/	mA
I_{DD15}	Total current under 1.5-V supply	/	1050	1300	mA
I_{DD11}	Total current under 1.15-V supply	/	260	600 ⁵	mA

⁵ Maximum instantaneous peak current is up to 850 mA.

3.4 Power Consumption

Table 3.5: Average Power Consumption

Condition	Description	Min	Typ	Max	Unit
1TX, 4RX	Sampling: 20 MS/s, 50 ms/frame, 256 chirps/frame, 30 μ s/chirp, baseband/CPU active, RX/TX/LO/ADC/FMCW/PLL off during interframe	/	0.54	/	W
2TX, 4RX		/	0.58	/	
3TX, 4RX		/	0.64	/	
4TX, 4RX		/	0.7	/	
1TX, 4RX	Sampling: 20 MS/s, 50 ms/frame, 1024 chirps/frame, 30 μ s/chirp, baseband/CPU active, RX/TX/LO/ADC/FMCW/PLL off during interframe	/	1	/	
2TX, 4RX		/	1.2	/	
3TX, 4RX		/	1.4	/	
4TX, 4RX		/	1.6	/	

3.5 Phase Locked Loop (PLL)

Table 3.6: PLL Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
f_{PLL}	PLL frequency range	60	/	64	GHz
Ramp_BW	PLL ramping bandwidth	/	4	/	GHz
Ramp_Rate_up	PLL ramping up rate	/	/	200	MHz/ μ s
Ramp_time_dn	PLL ramping down time with Ramp_BW = 2G	8	/	/	μ s
	PLL ramping down time with Ramp_BW = 4G	20	/	/	μ s
Ramp_time_idle	PLL idle time with Ramp_BW = 4G	2	/	/	μ s
PN @ 1 MHz	Phase noise at 1MHz offset	/	-93	/	dBc/Hz

3.6 Transmitter (TX)

Table 3.7: Transmitter Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
FREQUENCY AND NUMBER OF CHANNELS					
N_ch_TX	Number of TX channels	4			/
f_TX	TX output frequency range	60	/	64	GHz
Power					
Pout	TX output power per channel	/	11	/	dBm
Pout_v	Output power variation due to Vdd	/	0.5	/	dB
Pout_slope	Output power frequency slope	-0.2	0	0.05	dB/100 MHz
Pout_ctrl	Output power control	/	8	/	dB
PHASE SHIFTER					
PS_ang	Phase shifter resolution	45			degrees
LEAKAGE					
Leak_LO_TX	RF leakage at TX port. All RF channels are disabled and LO is on	/	-30	/	dBm
TX ON/OFF TIME					
Time_TX	TX on/off switching time	/	2	2.5	μs



3.7. Receiver (RX)

3.7 Receiver (RX)

Table 3.8: Receiver Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
FREQUENCY AND NUMBER OF CHANNELS					
N_ch_RX	Number of RX channels		4		/
f _{RX}	RX input frequency range	60	/	64	GHz
RXRF					
CG_typical	RX conversion gain, LNA to VGA2, TIA = 500 ohm, LNA max gain, VGA1 + VGA2 = 30 dB at IF = 5 MHz	/	56	/	dB
CG_max	Maximum RX conversion gain at IF = 5 MHz, LNA/TIA/VGA1/ VGA2 maximum gain	/	73	/	dB
CG_min	Minimum RX conversion gain at IF = 5 MHz, TIA/VGA1/VGA2 minimum gain	/	32	/	dB
G_LNA	LNA gain control range	/	4	/	dB
G_LNA_step	LNA gain step	/	2	2	dB
G_TIA	TIA gain control range	/	12	/	dB
G_TIA_step	TIA gain step	/	6	/	dB
NF_RX	Single-sideband noise figure	/	12	/	dB
IP1dB	Input P1dB Power	/	-19	/	dBm
LEAKAGE					
Leak_LO_RX	RF leakage at RX port. All RF channels are disabled and LO is on	/	-30	/	dBm
RXBB					
G_VGA1	VGA1 gain	7	/	22	dB
G_VGA2	VGA2 gain	5	/	20	dB
G_step	VGA gain step	/	3	/	dB
OP1dB_RXBB	RX baseband output power 1-dB gain compression point Baseband gain=33 dB, IF=5 MHz	/	11	/	dBm
FILTER					
HP1_freq	The 1st high pass filter corner	12	/	200	kHz
HP1_order	The 1st high pass filter order		1		/
HP2_freq	The 2nd high pass filter corner	0.3	/	1	MHz
HP2_order	The 2nd high pass filter order		1		/
LP_freq	Low pass filter corner	/	15	/	MHz
IF OUTPUT					
IF_OUT	Output swing (DC couple, differential, Vp-p)	/	2.4	/	V
IF_LOAD_C	IF load capacitance (single-ended)	/	15	/	pF



3.8 Analog-to-Digital Converter (ADC)

Table 3.9: ADC Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
N_ch_ADC	Number of ADC channels		4		/
SNR @ 20 MS/s	Signal to noise ratio at sampling rate of 20 MS/s	/	65	/	dB
SNR @ 25 MS/s	Signal to noise ratio at sampling rate of 25 MS/s	/	62	/	dB
SNR @ 40 MS/s	Signal to noise ratio at sampling rate of 40 MS/s	/	62	/	dB
SNR @ 50 MS/s	Signal to noise ratio at sampling rate of 50 MS/s	/	59	/	dB
SFDR @ 20 MS/s	Spurious-free dynamic range at sampling rate of 20 MS/s	/	68	/	dB
SFDR @ 25 MS/s	Spurious-free dynamic range at sampling rate of 25 MS/s	/	68	/	dB
SFDR @ 40 MS/s	Spurious-free dynamic range at sampling rate of 40 MS/s	/	59	/	dB
SFDR @ 50 MS/s	Spurious-free dynamic range at sampling rate of 50 MS/s	/	59	/	dB

Two auxiliary ADCs are used to measure DC voltage. Each consists of a front-end buffer, a discrete-time sigma-delta modulator and a decimation filter, covering a voltage range of 0.5 V to 2.5 V. And multiple voltages from the external of or within the chip can be multiplexed to the input of each ADC. Both ADCs have a 10-bit resolution.

Table 3.10: Auxiliary ADC Electrical Characteristics

Symbol	Description	Min	Typ	Max	Unit
N_AUXADC	Number of auxiliary ADCs		2		/
VR	Voltage range	0.5	/	2.5	V
ENOB @ 20 KS/s	Effective number of bits at the sampling rate of 20 KS/s	/	10	/	Bits
INL	Integral nonlinearity (best fit)	/	±2	/	LSB
ERR_G	Gain error	/	±0.75%	/	/
ERR_O	Offset error	/	±4	/	mV

3.9 I/O DC Electrical Specifications

Table 3.11: I/O DC Electrical Specifications

Symbol	Description	Min	Typ	Max	Unit
V _{IH}	GPIO input high voltage	2	/	3.6	V
V _{IL}	GPIO input low voltage	-0.3	/	0.8	V
V _{OH}	GPIO output high voltage	2.4	/	/	V
V _{OL}	GPIO output low voltage	/	/	0.4	V
R _{PU}	GPIO pull-up resistor	58k	86k	133k	ohm
t _r ⁶	GPIO output rise time (VDDIO = 3.3 V, C _L = 50 pF)	/	/	6.3	ns
t _f ⁷	GPIO output fall time (VDDIO = 3.3 V, C _L = 50 pF)	/	/	6.5	ns

⁶ The rise/fall time is measured as the time taken by the signal to transition from 30% and 70% of the typical input IO voltage.

⁷ The rise/fall time is measured as the time taken by the signal to transition from 30% and 70% of the typical input IO voltage.



3.10 CPU

Table 3.12: CPU Specifications

Parameter	Value	Unit
Clock Frequency	300	MHz
Address Size	24	Bits
Endianness	Little	/
I-Cache (Instruction Cache) Size	32	KiB
D-Cache (Data Cache) Size	32	KiB
ICCM (Instruction Closely Coupled Memory) Size	32	KiB
DCCM (Data Closely Coupled Memory) Size	32	KiB
Number of Timers	2	/
Number of Real Timer Counters	1	/
Watchdog Timer Width	32	Bits
FPU Type	Single precision	/
MPU Region	16	/



3.11 Baseband

Table 3.13: Baseband Specifications

Item	Value
Frame Type	Normal frame Virtual frame (TDM and BPM)
Digital Decimation	Up to factor of 16
Anti-Interference	Phase scrambling Frequency Hopping Chirp Shifting
FFT Size	Minimum FFT size is 64. Maximum range-domain FFT Size is 2048. Maximum Doppler-domain FFT size is 1024. Total 2D-FFT size needs to be less than 2 MiB. Each complex data is represented in 32 bits.
CFAR Window Size	Up to 21×21 (Rectangular Window)
CFAR Type	CA (Cell Averaging) OS (Ordered Statistics) SOGO (Smallest Order and Greatest Order) NR (Noise Reference)
CFAR Objects	Up to 1024
Multi-Object DoA	Up to 4 objects per bin
Super Resolution Support	DML (Deterministic Maximum Likelihood)
Frame Interleaving	Support up to 4 different types of frames

3.12 Thermal Resistance Characteristics for Flip-Chip Package

Table 3.14: Thermal Resistance Characteristics

Thermal Metrics	°C/W
Θ_{JA} Junction-to-Free_air	58.06
Θ_{JMA} Junction-to-Moving_Air	NA
Ψ_{JT} Junction-to-Package_top	2.39
Ψ_{JB} Junction-to-Board	3.64



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RADIATION CHARACTERISTICS

Table 4.1: AiP Radiation Characteristics

Description	TYP	Unit
TX0 to TX1/2/3 Azimuth Separation	9.8	mm
TX1/2/3 Elevation Separation	2.5	mm
RX Antenna Azimuth Separation	2.5	mm
RX Antenna Elevation Separation	0	mm
RX Antenna Gain	2	dBi
Single TX Mode		
Effective Isotropic Radiated Power (EIRP) at $T_A = 25^{\circ}\text{C}$	12	dBm
6dB Azimuth Field of View (FoV) ¹	± 40	degree
6dB Elevation FoV	± 30	degree
12dB Azimuth FoV	± 50	degree
12dB Elevation FoV	± 40	degree
TX1-2-3 Combination Mode²		
EIRP at $T_A = 25^{\circ}\text{C}$	21	dBm
6dB Azimuth FoV	± 40	degree
6dB Elevation FoV	± 20	degree
12dB Azimuth FoV	± 50	degree
12dB Elevation FoV	± 30	degree
Elevation Beamforming Scan Angle	± 30	degree

All performances are tested with an evaluation board of 6 cm × 6 cm, whose top layer is fully covered with the ground plane. For details about the device layout, see *Rhine AiP/CAL60S244-IB RDP Reference Design*.

Note: AiP radiation performances are sensitive to the surrounding structure, so the PCB must be carefully designed. For a guide to hardware design, refer to *Rhine CAL60S244-IB Hardware Design Guide*.

¹ Field of View (FoV) is measured with both transmitting and receiving antennas.

² To achieve broadside radiation under TX1-2-3 Combination Mode, the recommended phase setting is as follows: CH1: 0 deg; CH2: 0 deg; and CH3: 0 deg.

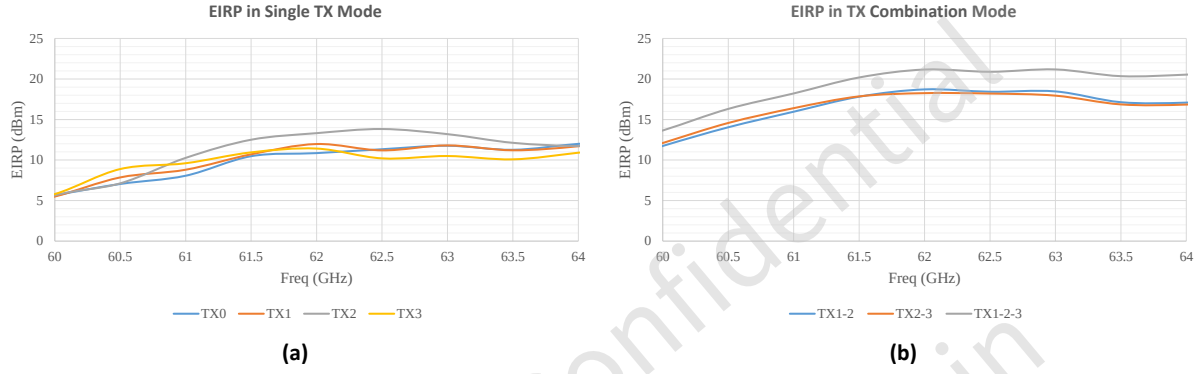


Fig. 4.1: EIRP at $T_A = 25^\circ\text{C}$: (a) Single TX Mode; (b) TX Combination Mode

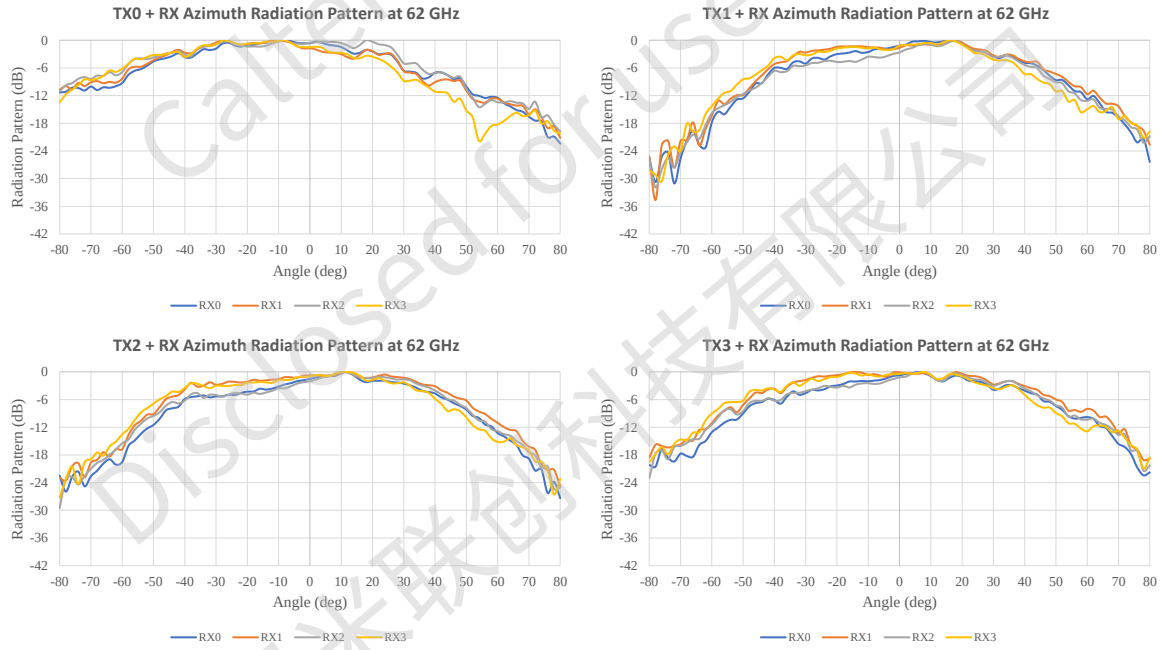


Fig. 4.2: Measured Azimuth Radiation Pattern for All TX to RX Pairs in Single TX Mode

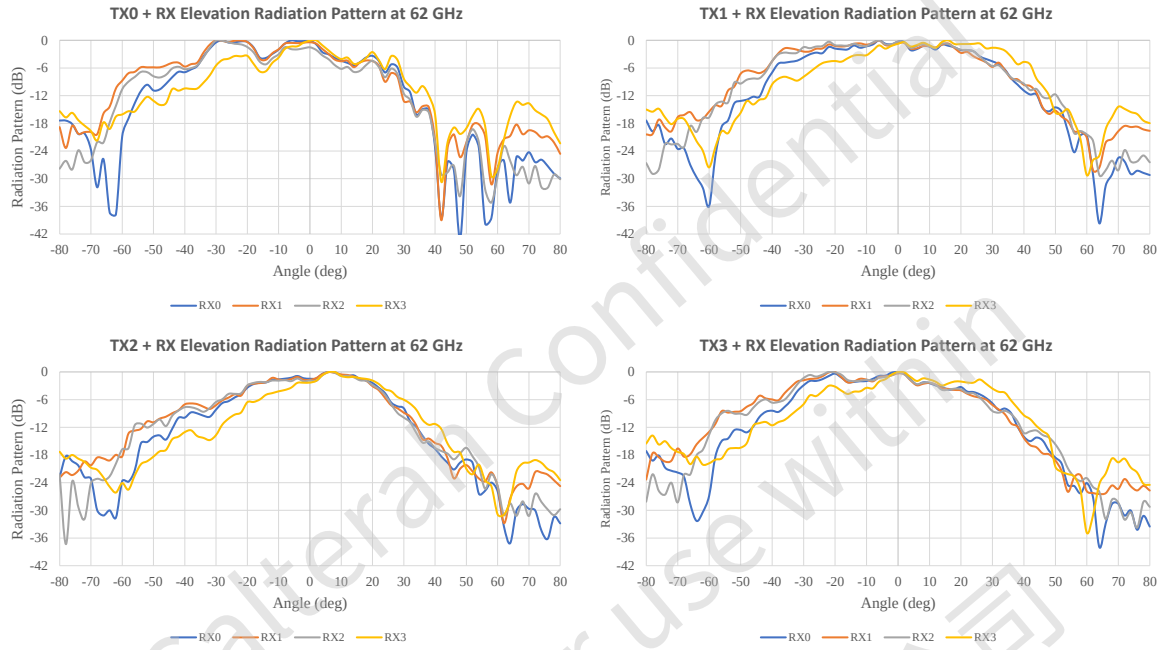


Fig. 4.3: Measured Elevation Radiation Pattern for All TX to RX Pairs in Single TX Mode

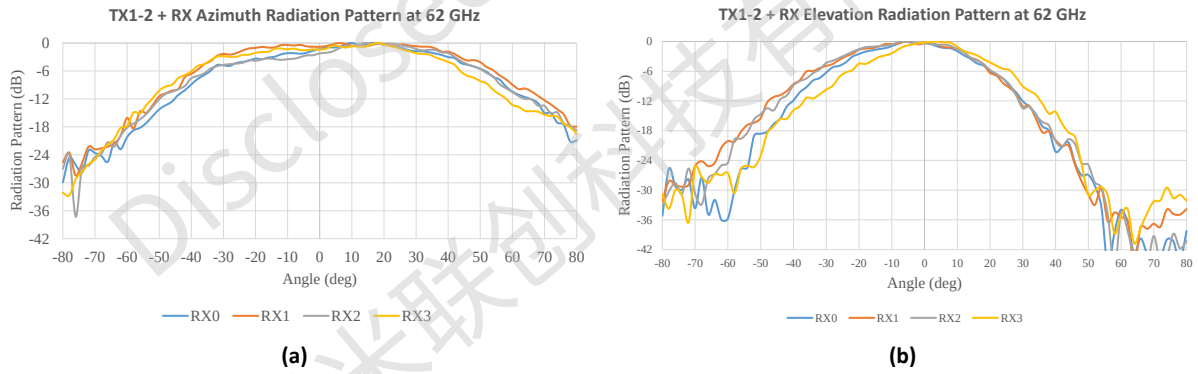


Fig. 4.4: Measured Radiation Pattern for All TX to RX Pairs in TX1-2 Combination Mode: (a) Azimuth; (b) Elevation



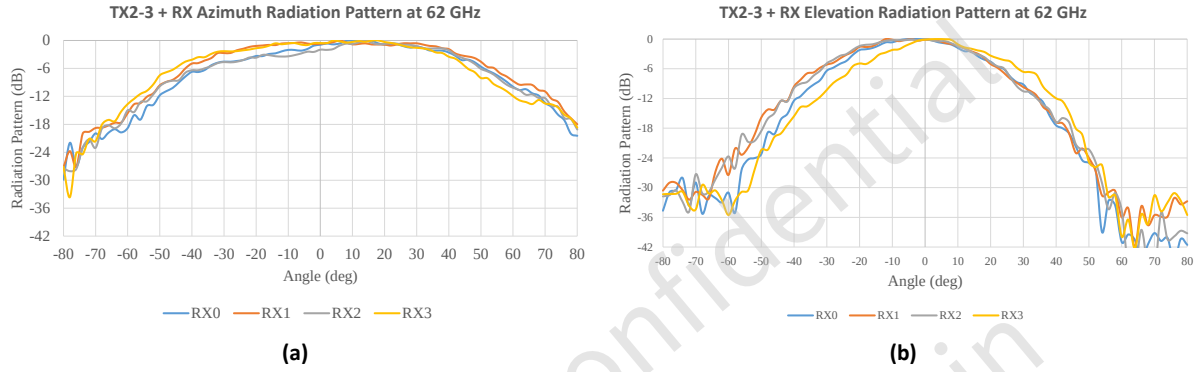


Fig. 4.5: Measured Radiation Pattern for All TX to RX Pairs in TX2-3 Combination Mode: (a) Azimuth; (b) Elevation

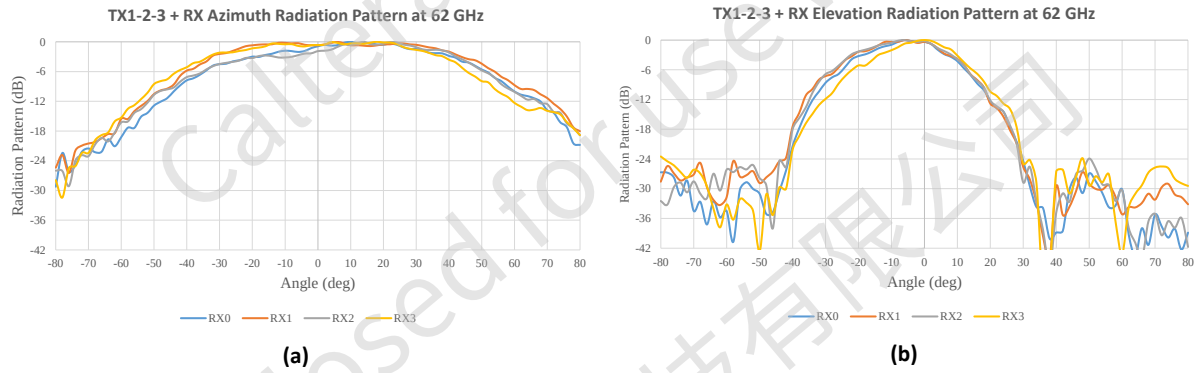


Fig. 4.6: Measured Radiation Pattern for All TX to RX Pairs in TX1-2-3 Combination Mode: (a) Azimuth; (b) Elevation

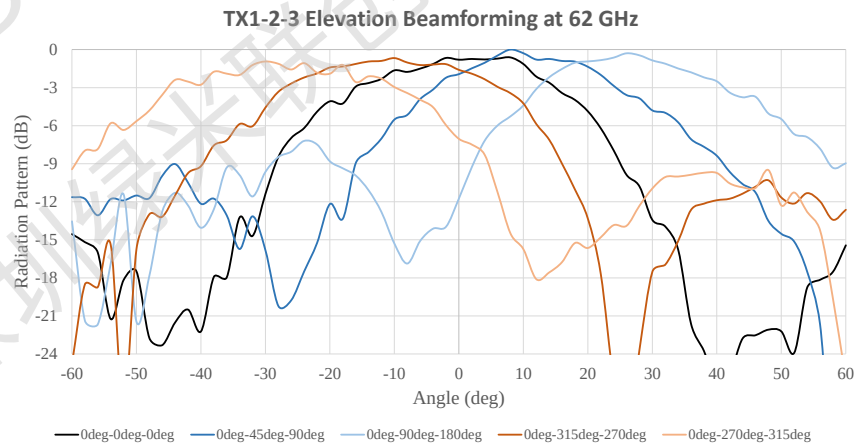


Fig. 4.7: Measured TX1-2-3 Elevation Beamforming

TIMING CHARACTERISTICS

5.1 Power on Timing

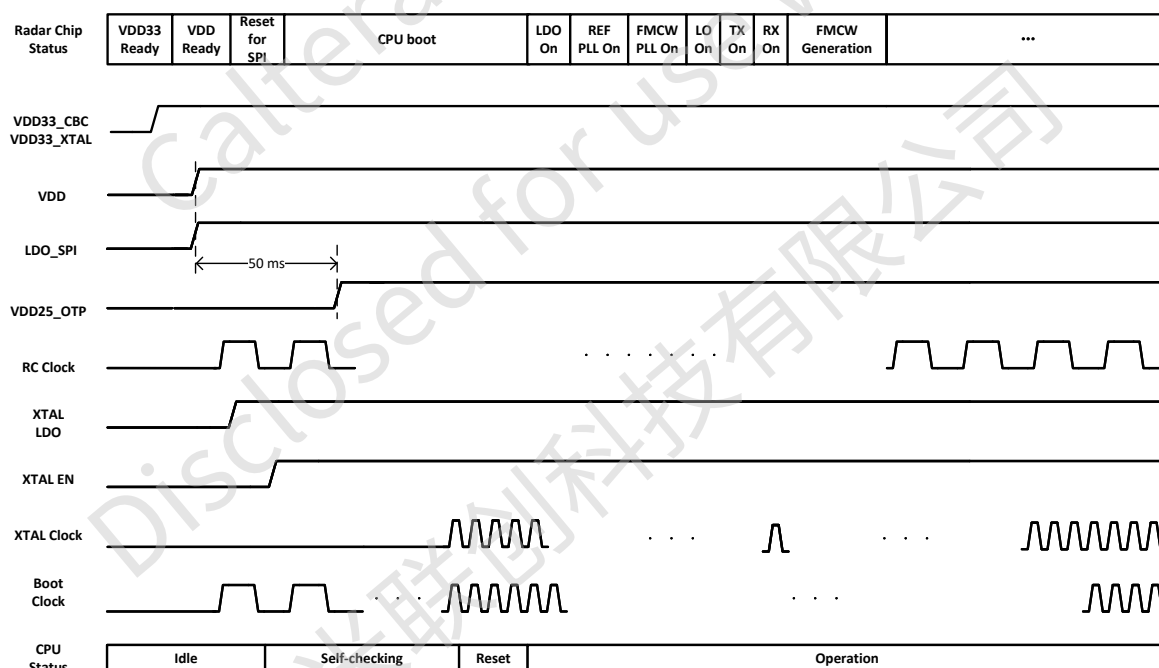


Fig. 5.1: Power on Timing

Note:

- The VDD power supply should only be powered on after VDD33 reaches its minimum requirement of being 3.14 V.
- The VDD25_OTP power supply is for OTP programming only. After the VDD gets ready, the VDD25_OTP power supply should be powered on 50 ms later.
- Powering on VDD25_OTP is not recommended for OTP read-only applications.

5.2 Low-Voltage Differential Signaling (LVDS)

Calterah Rhine CAL60S244-IB(-A) integrates a 4-channel ADC and provides two flexible interface solutions:

- For I/Os: Serializer + LVDS interface protocol
- For internal processor: Paralleled interface protocol

Fig. 5.2 shows the details of the interface solutions. The embedded LVDS of Calterah meets the ANSI/TIA/EIA-644-A standard.

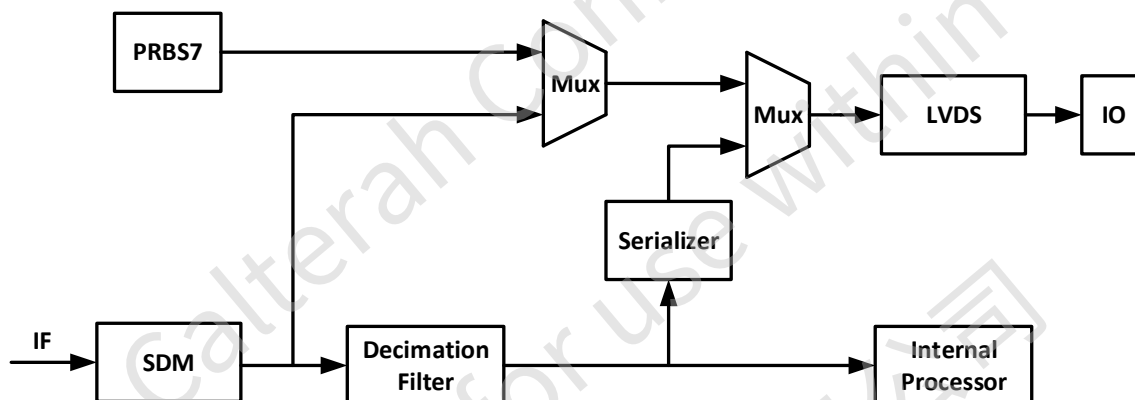


Fig. 5.2: Structure of 4-Channel ADC with Interface Solutions

The embedded ADC supports two working modes with different sampling rates and data widths.

- In one working mode, the LVDS provides two optional sampling rates: 20 MS/s and 25 MS/s. For the 20-MS/s clock, data width is 20 bits. For the 25-MS/s clock, data width is 16 bits.

Both 16-bit and 20-bit data adopt double data rate (sampling data at both falling and rising edges of the clock). Two's complement is used as the data format.

- In the other working mode, the LVDS provides another two optional sampling rates: 40 MS/s and 50 MS/s. For the 40-MS/s clock, data width is 20 bits. For the 50-MS/s clock, data width is 16 bits. And the 20-bit data is reorganized to two channels of 10-bit data, and the 16-bit data is reorganized to two channels of 8-bit data.

Both 16-bit and 20-bit data adopt double data rate (sampling data at both falling and rising edges of the clock). Two's complement is used as the data format.

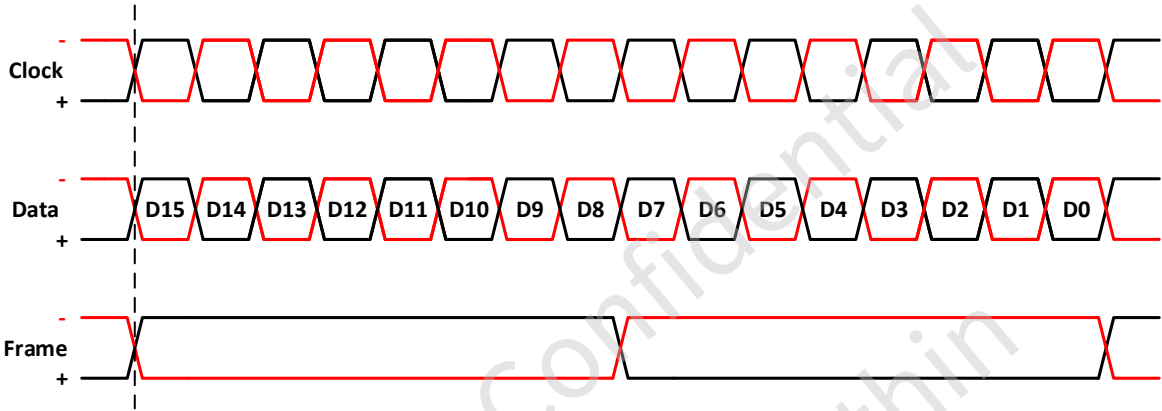


Fig. 5.3: 16-Bit Data with 25-MS/s Clock

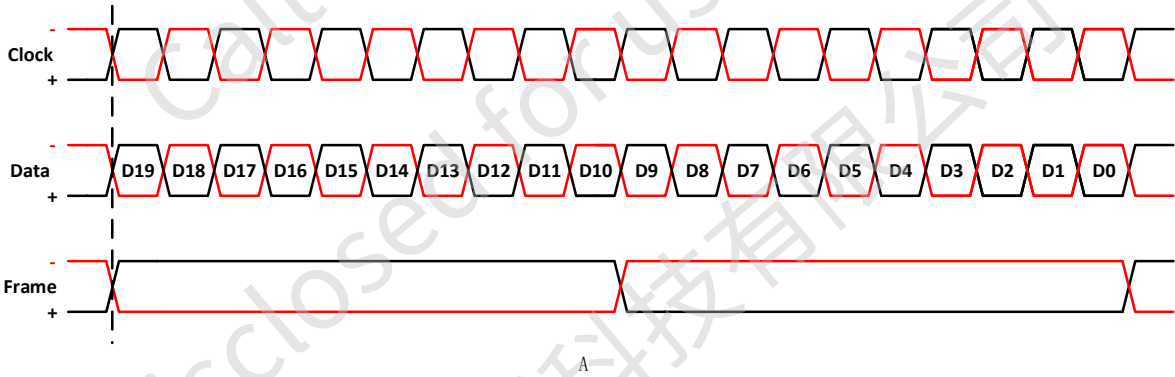


Fig. 5.4: 20-Bit Data with 20-MS/s Clock



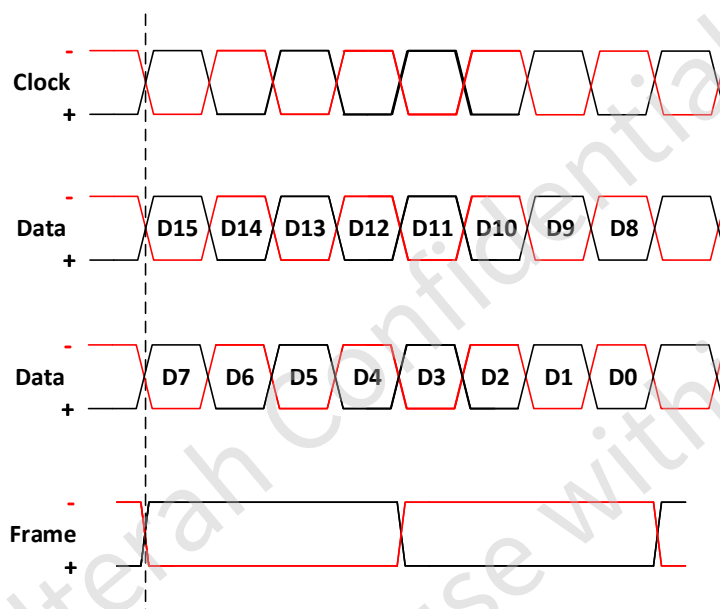


Fig. 5.5: 16-Bit Data with 50-MS/s Clock

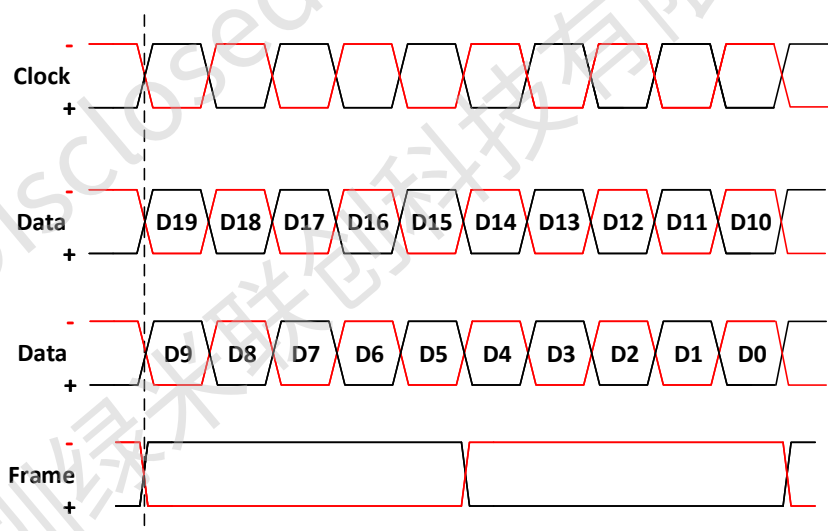


Fig. 5.6: 20-Bit Data with 40-MS/s Clock

Table 5.1: LVDS Specifications

Symbol	Description	Min	Typ	Max	Unit	Comments
DR	Data rate	/	400	/	MHz	
R_L	Resistive Load (Differential)	/	100	/	Ohm	
C_L	Capacitive Load (Differential)	/	5	7.5	pF	
V_{CM}	Common Mode Voltage	1.125	1.25	1.375	V	
V_{OUT}	Output Voltage (Differential)	250	360	450	mV	
T_r	Rising Time (20% - 80%)	260	/	0.3 UI	ps	UI (Unit Interval)= 2.5 ns, 0.3 UI = 750 ps
T_f	Falling Time (20% - 80%)	260	/	0.3 UI	ps	UI (Unit Interval)= 2.5 ns, 0.3 UI = 750 ps
V_{OH}	Output Voltage High	/	/	1.6	V	
V_{OL}	Output Voltage Low	0.9	/	/	V	

5.3 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) module is modeled after the industry-standard 16550. However, the register address space is relocated to 32-bit data boundaries for Advanced Peripheral Bus (APB) bus implementation.

5.3.1 Timing

Table 5.2: UART Timing Requirements

Description	Min	Typ	Max	Unit
Supported baud rate at 10 pF	/	921.6	/	kb/s

5.4 Inter-Integrated Circuit Interface (I²C)

Table 5.3: I²C Signal (SDA and SCL) Switching Characteristics

Symbol	Description	SS (Min)	SS (Max)	FS (Min)	FS (Max)	FS+ (Min)	FS+ (Max)	HS (Min)	HS (Max)	Unit
$f_{(SCL)}$	SCL clock frequency	/	100	/	400	/	1000	/	3400	kHz
$t_{c(SCL)}$	SCL clock cycle time	10	/	2.5	/	1	/	0.29	1	μ s
t_{LOW}	LOW period of the SCL clock	4.7	/	1.3	/	0.5	/	0.16	/	μ s
t_{HIGH}	HIGH period of the SCL clock	4	/	0.6	/	0.26	/	0.06	/	μ s
$t_{SU:STA}$	Setup time for a repeated START condition	4.7	/	0.6	/	0.26	/	0.16	/	μ s
$t_{HD:STA}$	Hold time for a (repeated) START condition	4	/	0.6	/	0.26	/	0.16	/	μ s
$t_{SU:STO}$	Setup time for STOP condition	4	/	0.6	/	0.26	/	0.16	/	μ s
t_{SP}	Spike length	/	/	/	0.05	/	0.05	/	0.01	μ s
$t_{HD:DAT}$	Data hold time	/	3.45	/	0.9	/	0.45	/	0.07	μ s
$t_{SU:DAT}$	Data setup time	0.25	/	0.1	/	0.05	/	0.01	/	μ s

Note: SS means Standard Speed mode, FS means Fast Speed mode, FS+ means Fast Speed Plus mode, and HS means High Speed mode.

- t_{LOW} can be configured by registers: IC_SS_SCL_LCNT in SS mode, IC_FS_SCL_LCNT in FS/FS+ mode, and IC_HS_SCL_LCNT in HS mode.



5.5. Serial Peripheral Interface (SPI)

- t_{HIGH} can be configured by registers: IC_SS_SCL_HCNT in SS mode, IC_FS_SCL_HCNT in FS/FS+ mode, and IC_HS_SCL_HCNT in HS mode.
- $t_{\text{SU;STA}}$ can be configured by registers: IC_SS_SCL_LCNT in SS mode, IC_FS_SCL_HCNT in FS/FS+ mode, and IC_HS_SCL_LCNT in HS mode.
- $t_{\text{HD;STA}}$ can be configured by registers: IC_SS_SCL_HCNT in SS mode, IC_FS_SCL_HCNT in FS/FS+ mode, and IC_HS_SCL_LCNT in HS mode.
- $t_{\text{SU;STO}}$ can be configured by registers: IC_SS_SCL_HCNT in SS mode, IC_FS_SCL_HCNT in FS/FS+ mode, and IC_HS_SCL_LCNT in HS mode.
- t_{SP} can be configured by registers: IC_FS_SPKLEN in SS mode, IC_FS_SPKLEN in FS/FS+ mode, and IC_HS_SPKLEN in HS mode.
- $t_{\text{HD;DAT}}$ can be configured by registers: IC_SDA_HOLD in SS, FS/FS+, and HS modes.
- $t_{\text{SU;DAT}}$ can be configured by registers: IC_SDA_SETUP in SS, FS/FS+, and HS modes.

I²C symbols are shown in Fig. 5.7.

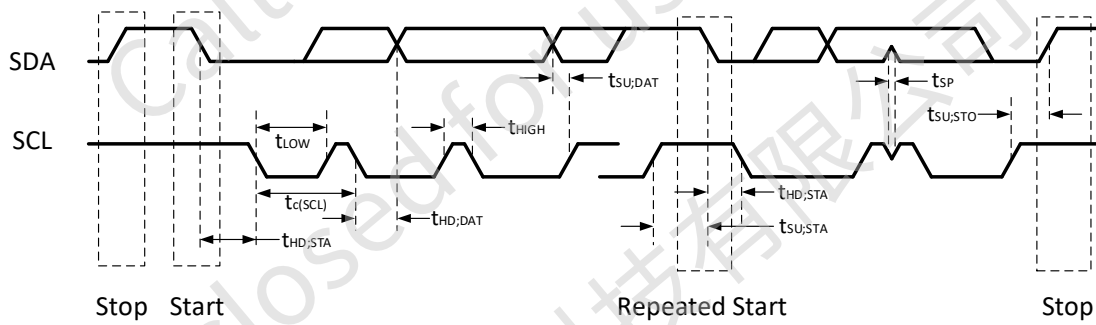


Fig. 5.7: I²C Signal Timing

5.5 Serial Peripheral Interface (SPI)

Serial Peripheral Interface (SPI) is a high-speed synchronous serial interface that allows a serial bit stream of programmed length (4 to 32 bits) to be shifted into or out of the device at an adaptive transfer rate.

5.5.1 SPI Master I/O Timing

Table 5.4: SPI Master I/O Timing

Symbol	Description	Min	Max	Unit
$t_{c(RefCLK)}$	Reference clock cycle time	5	/	ns
$t_{c(CLK)}$	Clock cycle time	20	/	ns
$t_{w(CLKH)}$	Pulse duration clock high	8	/	ns
$t_{w(CLKL)}$	Pulse duration clock low	8	/	ns
$t_{delay}(MOSI-SEL)$	Delay time, MOSI valid after falling edge of SEL	/	$t_{c(CLK)} + 1$	ns
$t_{delay}(MOSI-CLK)$	Delay time, MOSI valid after active edge of CLK	/	$0.5t_{c(CLK)} + 1$	ns
$t_{su}(MISO-CLK)$	Setup time, MISO valid before falling CLK edge	10	/	ns
$t_h(CLK-MISO)$	Hold time, MISO valid after falling CLK edge	1	/	ns

Symbols are shown in Fig. 5.8.

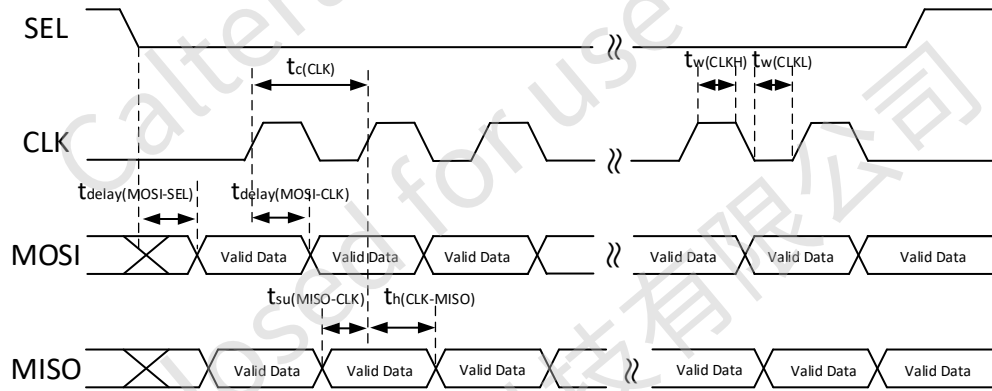


Fig. 5.8: SPI Master Timing

5.5.2 SPI Slave I/O Timing

Table 5.5: SPI Slave I/O Timing

Symbol	Description	Min	Max	Unit
$t_{c(RefCLK)}$	Reference clock cycle time	5	/	ns
$t_{c(CLK)}$	Clock cycle time	20	/	ns
$t_{w(CLKH)}$	Pulse duration clock high	10	/	ns
$t_{w(CLKL)}$	Pulse duration clock low	10	/	ns
$t_{delay}(MISO-SEL)$	Delay time, MISO valid after falling edge of SEL	/	$2t_{c(RefCLK)} + 8$	ns
$t_{delay}(MISO-CLK)$	Delay time, MISO valid after active edge of CLK	/	$0.5t_{c(CLK)} + 7$	ns
$t_{su}(MOSI-CLK)$	Setup time, MOSI valid before falling CLK edge	2	/	ns
$t_h(CLK-MOSI)$	Hold time, MOSI valid after falling CLK edge	1	/	ns

Symbols are shown in Fig. 5.9.



5.6. Quad Serial Peripheral Interface (QSPI)

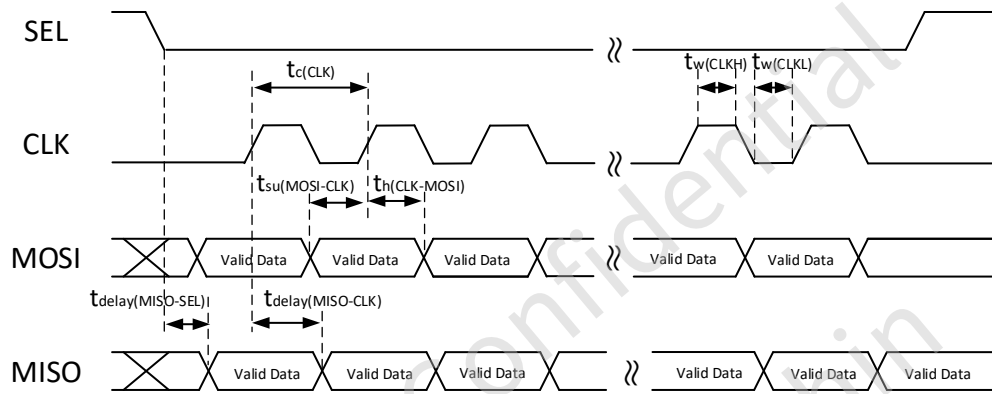


Fig. 5.9: SPI Slave Timing

5.6 Quad Serial Peripheral Interface (QSPI)

Quad Serial Peripheral Interface (QSPI) is an enhanced mode for SPI. Under this mode, the width of data line is changed to 4, so the data is shifted out and in on more than one line. Hence, the overall throughput is increased.

Table 5.6: QSPI I/O Timing

Symbol	Description	Min	Max	Unit
$t_{c(RefCLK)}$	Reference clock cycle time	2.5	/	ns
$t_c(CLK)$	Clock cycle time	20	/	ns
$t_w(CLKH)$	Pulse duration clock high	8	/	ns
$t_w(CLKL)$	Pulse duration clock low	8	/	ns
$t_{delay}(DAT-SEL)$	Delay time, DAT[3:0] output valid after falling edge of SEL	/	$0.5t_{c(CLK)}$ $t_{c(RefCLK)} + 1$	ns
$t_{delay}(DAT-CLK)$	Delay time, DAT[3:0] output valid after active edge of CLK	/	$0.5t_{c(CLK)} + 2$	ns
$t_{su}(DAT-CLK)$	Setup time, DAT[3:0] valid before falling CLK edge	9	/	ns
$t_h(CLK-DAT)$	Hold time, DAT[3:0] valid after falling CLK edge	1	/	ns

Symbols are shown in Fig. 5.10.

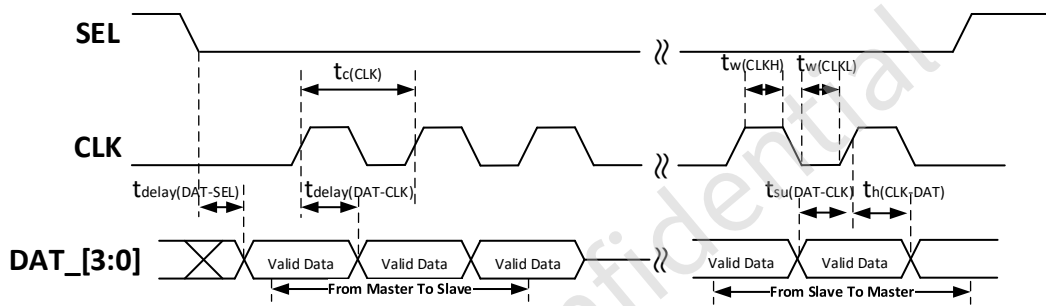


Fig. 5.10: QSPI Timing

5.7 Joint Test Action Group (JTAG)

Table 5.7: JTAG Timing

Symbol	Description	Min	Typ	Max	Unit
$t_c(\text{TCK})$	Cycle time TCK	40	/	/	ns
$t_{su}(\text{TDI-TCK})$	Input setup time TDI valid to TCK high	30	/	/	ns
$t_{su}(\text{TMS-TCK})$	Input setup time TMS valid to TCK high	30	/	/	ns
$t_h(\text{TCK-TDI})$	Input hold time TDI valid from TCK high	0	/	/	ns
$t_h(\text{TCK-TMS})$	Input hold time TMS valid from TCK high	0	/	/	ns
$t_{su}(\text{TDO-TCK})$	Input setup time TDO valid to TCK high	30	/	/	ns
$t_h(\text{TCK-TDO})$	Input hold time TDO valid from TCK high	0	/	/	ns

Symbols are shown in Fig. 5.11.

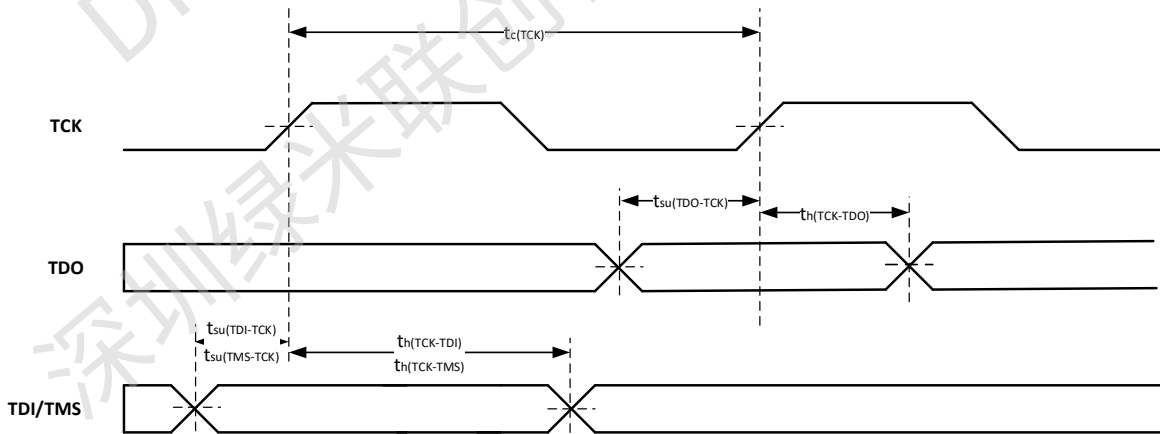


Fig. 5.11: JTAG Timing



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DETAILED DESCRIPTIONS

6.1 Radio Subsystem

The Radio subsystem integrates all the necessary RF, analog, and mixed-signal blocks for the radar frontend, including:

- 4 transmitter channels
- 4 receiver channels
- A frequency synthesizer with FMCW radar signal generator
- A reference PLL
- ADCs
- Baseband filters
- Variable-gain amplifiers
- Output drivers

6.1.1 Clock Generation

To boot up and provide a reference clock for Reference PLL, Calterah Rhine requires an external crystal whose oscillating frequency is 40 MHz. The external crystal should be connected to the device I/Os. Fig. 6.1 shows the implementation of the external crystal.

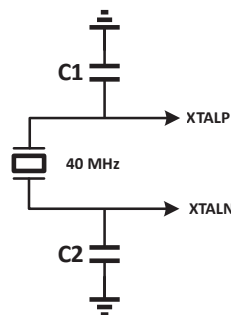


Fig. 6.1: Implementation of External Crystal

Table 6.1 lists the electrical characteristics of the clock crystal.

6.1. Radio Subsystem

Table 6.1: Crystal Electrical Characteristics

Description	Symbol	Min	Typ	Max	Unit
Nominal frequency	FL	/	40	/	MHz
Load capacitance	CL	/	4	/	pF
Operating temperature	/	-40		105	°C
Effective resistance	Rr	/	/	55	Ω
Drive level	DL	/	/	200	μW

With the presence of the 40 MHz clock produced by the external crystal, Rhine Clock Generation module generates 60- to 64- GHz clock signals for RF subsystem. The Clock Generation module contains a built-in oscillator circuit, a Reference PLL, an FMCW PLL, and a x4 frequency multiplier. The built-in oscillator circuit along with the external crystal produces a 40 MHz clock for the Reference PLL. The Reference PLL produces a 360 MHz clock for the FMCW PLL and a 400 MHz clock for ADC, a 300 MHz clock for CPU, a 5 MHz clock for auxiliary ADC (Aux ADC), which is used for safety monitoring, and a 5 MHz clock for the temperature sensor (TS). The FMCW PLL along with the x4 multiplier produces FMCW or fixed frequency clock signals for the Radio subsystem with high precision.

A built-in circuit is also included in the Clock Generation module to detect the presence of the crystal and the quality of the generated signals.

Fig. 6.2 shows the architecture of the clock generation module.

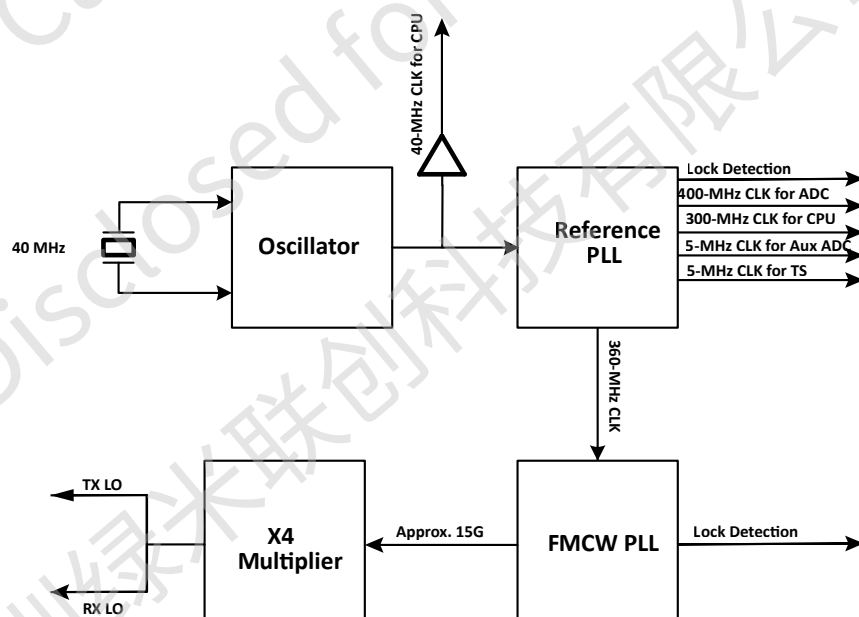


Fig. 6.2: Clock Subsystem

6.1.2 FMCW Waveform Synthesis

FMCW waveform generator in Calterah Rhine radar chip is embedded with the following features for better radar ranging and anti-interference. All these features can be programed and enabled independently.

- Virtual Array Mode (VAM)

VAM controls the on/off status and phase status of each TX channel, according to the user's configuration.

- Frequency Hopping Mode (FH)

FH enables the user to get different carrier frequencies and bandwidths for two adjacent chirps in the same frame.

- Phase Scramble Mode (PS)

PS provides the capability to rotate the phase by a degree of 180 in TX for each rotate.

- Chirp Shifting Mode (CS)

CS shifts both up ramp and down ramp by a specific time inside a chirp, while the total duration of one chirp keeps unchanged.

- Anti Velocity Ambiguity with Chirp Delay (Anti-VELAMB CD)

Anti-VELAMB CD extends some chirps' duration by a specific time, which is used for resolving velocity ambiguity.

- Frame Interleaving

FMCW waveform generator supports different frame types. Interleaving different types of frames enables achieving different applications simultaneously.

- Hardware Auto Frame Mode

In Hardware Auto Frame Mode, FMCW automatically starts the next frame after the current frame is done.

Note: This feature is available only in CAL60S244-IB-A.

- Doppler Spur Randomization

This feature provides a spur suppression method for the beat signal whose spurs are in non-zero Doppler bins.

Note: This feature is available only in CAL60S244-IB-A.

For detailed information and other features, refer to *Calterah Rhine Radar Baseband User Guide*.

6.1.3 Local Oscillator (LO)

The Local Oscillator (LO) module consists of driving amplifiers and frequency multipliers. See Fig. 6.3.



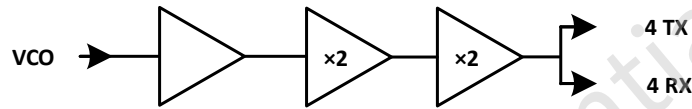


Fig. 6.3: LO Subsystem

6.1.4 Transmitter

The Transmitter module consists of 4 parallel transmitter chains, each with independent binary phase and amplitude control. All 4 transmitter channels can be operated at the same time. The device supports binary phase modulation for MIMO radar and interference mitigation. See Fig. 6.4.

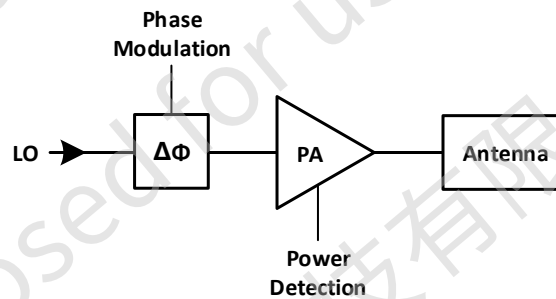


Fig. 6.4: Transmitter Subsystem (Per Channel)

6.1.5 Receiver

The Receiver module consists of 4 parallel channels. Each receiver channel consists of the following:

- A low-noise amplifier (LNA)
- A passive mixer
- A transimpedance amplifier (TIA)
- Two IF high-pass filters
- Two variable-gain amplifiers
- A sigma-delta modulator
- A decimation filter

All 4 receiver channels can be operated at the same time. An individual power-down option is also available. High-pass 1 has a 100-kHz normal cutoff frequency and can be configured to 15 kHz. High-pass 2 has a 500-kHz normal cutoff frequency. TIA, VGA1, and VGA2 are provided with an integrated saturation detector. Another saturation detector is inside the sigma-delta modulator.

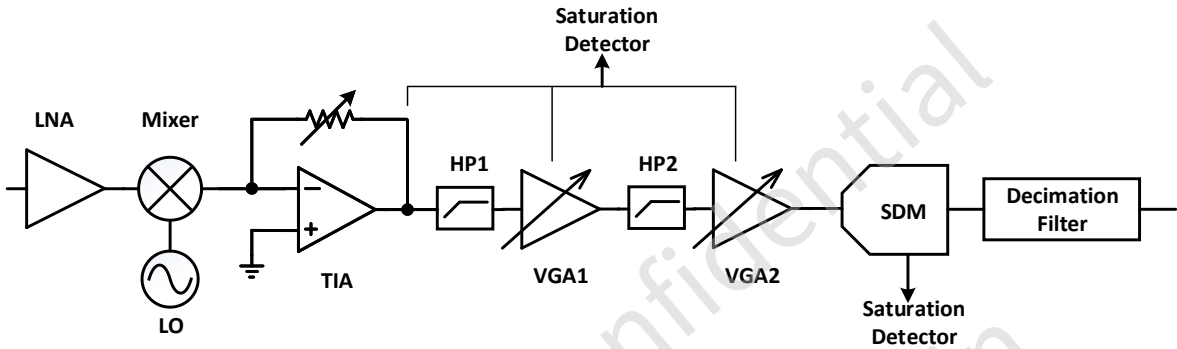


Fig. 6.5: RX Subsystem

6.1.6 Measurement Results

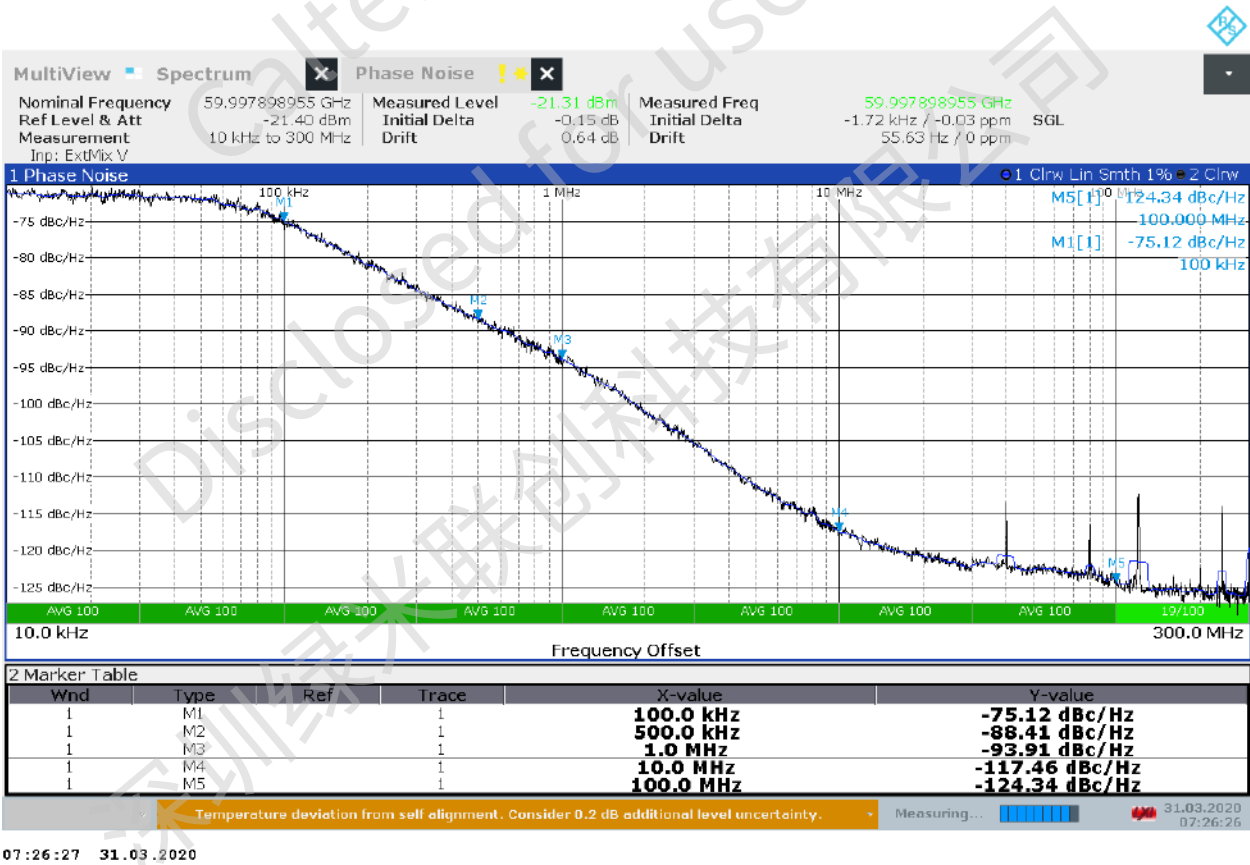


Fig. 6.6: Phase Noise at 60G



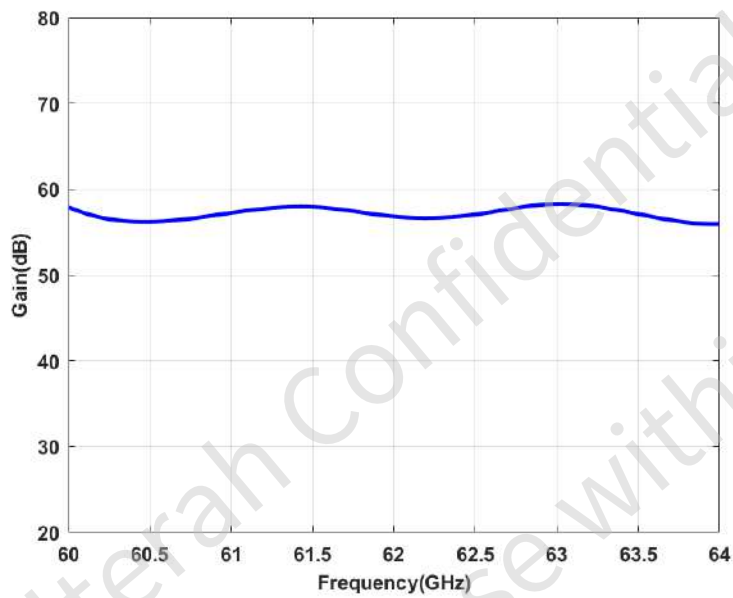


Fig. 6.7: RF Conversion Gain (CG_typical) at T_A = 25°C

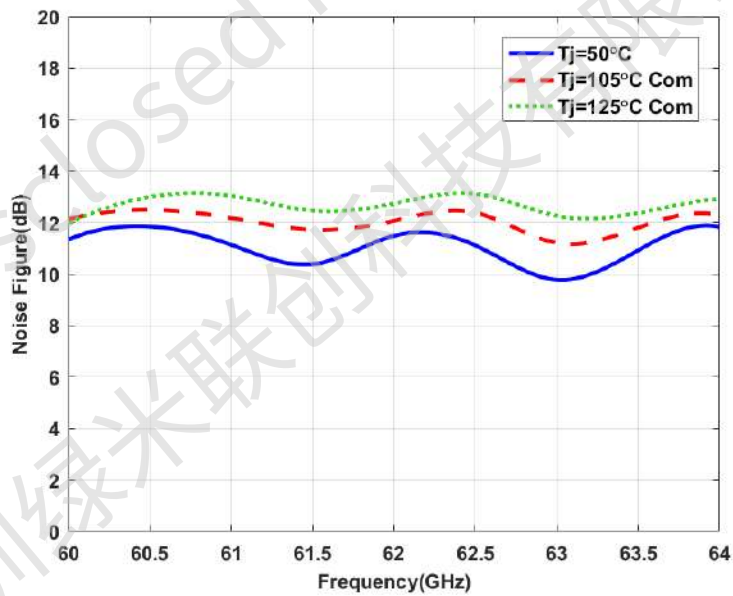


Fig. 6.8: Noise Figure (NF_RX) with Compensation vs Frequency

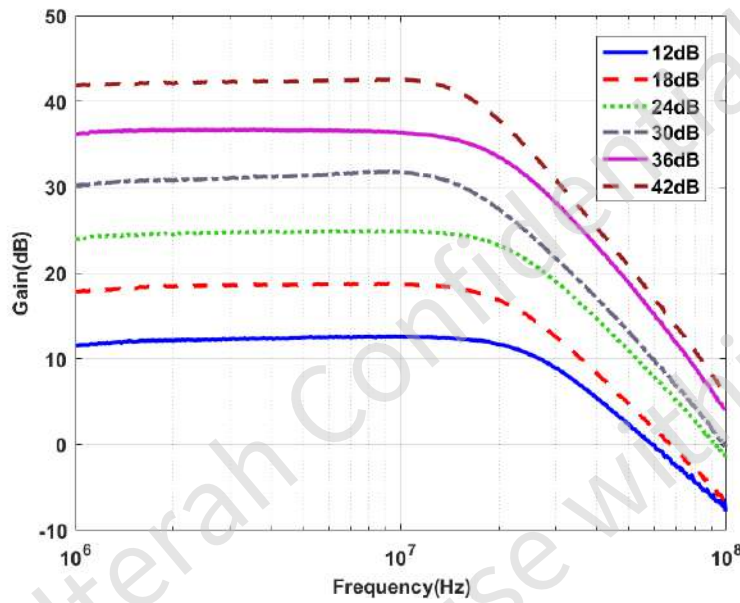


Fig. 6.9: VGA Gain (G_VGA1 + G_VGA2)

6.2 Processor Subsystem

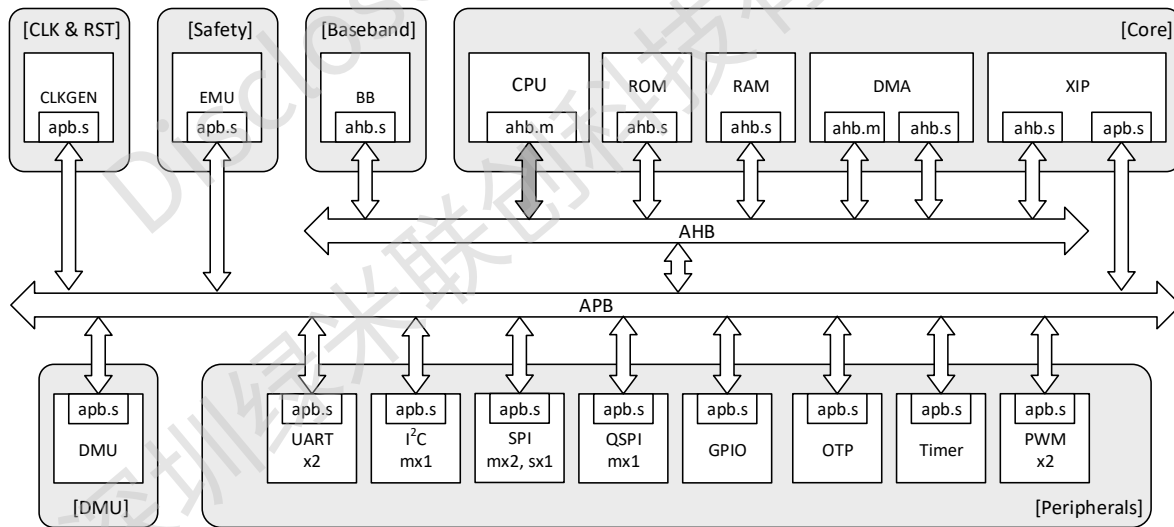
Fig. 6.10: Processor Subsystem¹

Fig. 6.10 briefly describes the processor subsystem, which can be divided into the following parts:

- Clock and reset

¹ The DMA module is *not* available in the baseline part number, which is described in the corresponding silicon errata document.



- Safety
- Core
- Baseband
- Peripherals
- IO Mux

6.2.1 Clock and Reset

All clocks in the processor subsystem are fed with three clocks from the radio subsystem, one boot clock used for boot, one 300 MHz clock, and one 400 MHz clock from PLL.

- Boot clock

The boot clock is used by the CPU to boot itself and to run programs to configure the radio subsystem. By default, the boot clock is connected to the RC clock. But there is an automatic switching from the RC clock to the XTAL clock once the XTAL clock is ready.

- 300 MHz clock

The 300 MHz clock is used as the main processor clock for the CPU, DMA, RAM, and ROM.

- 400 MHz clock

The 400 MHz clock is typically used as the reference clock for the peripherals and the baseband.

The clocks of Execute in Place (XIP), baseband (BB), and all peripherals can be individually gated, while individual soft resets for those modules are also supported.

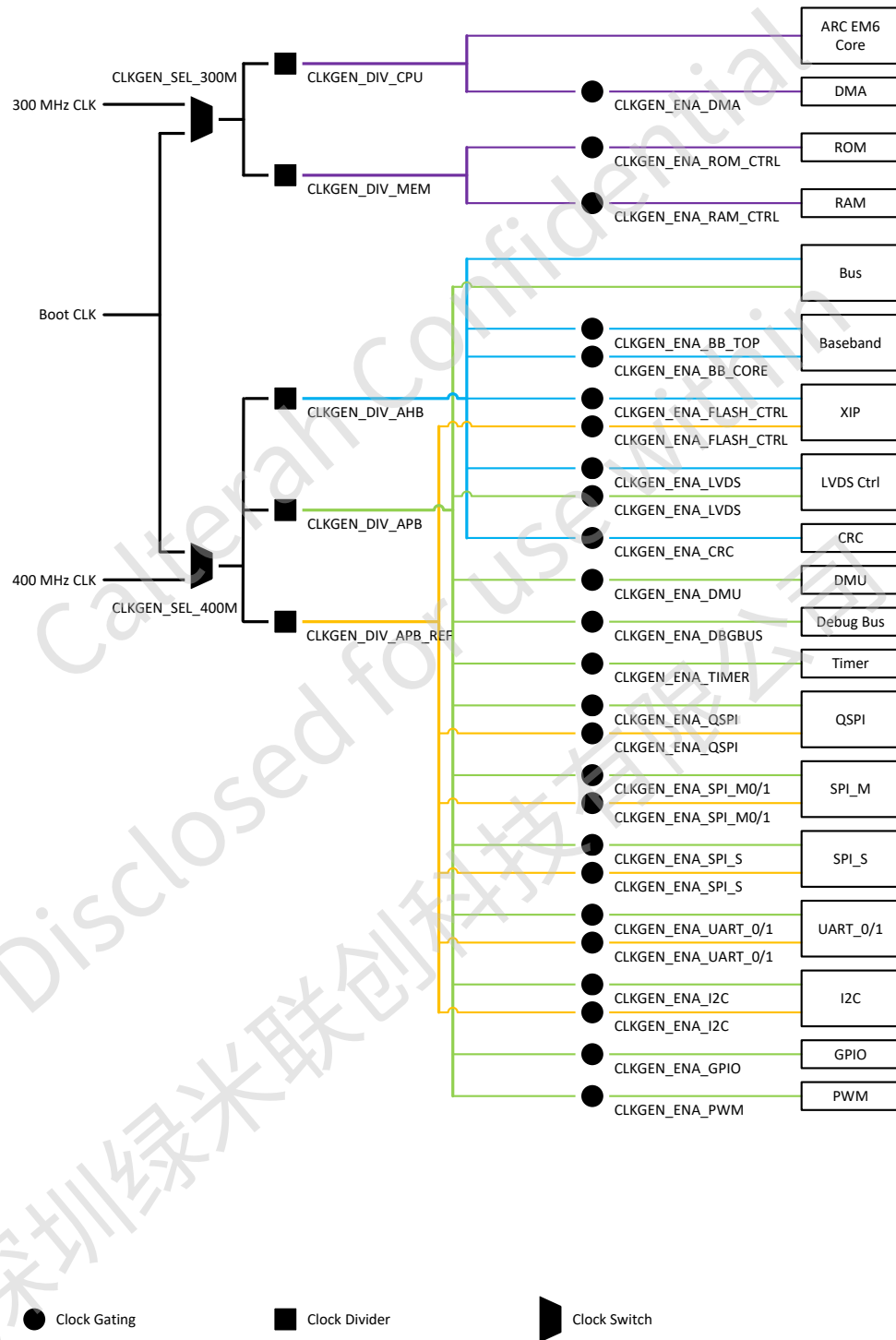


Fig. 6.11: Clock Architecture of CAL60S244-IB



6.2. Processor Subsystem

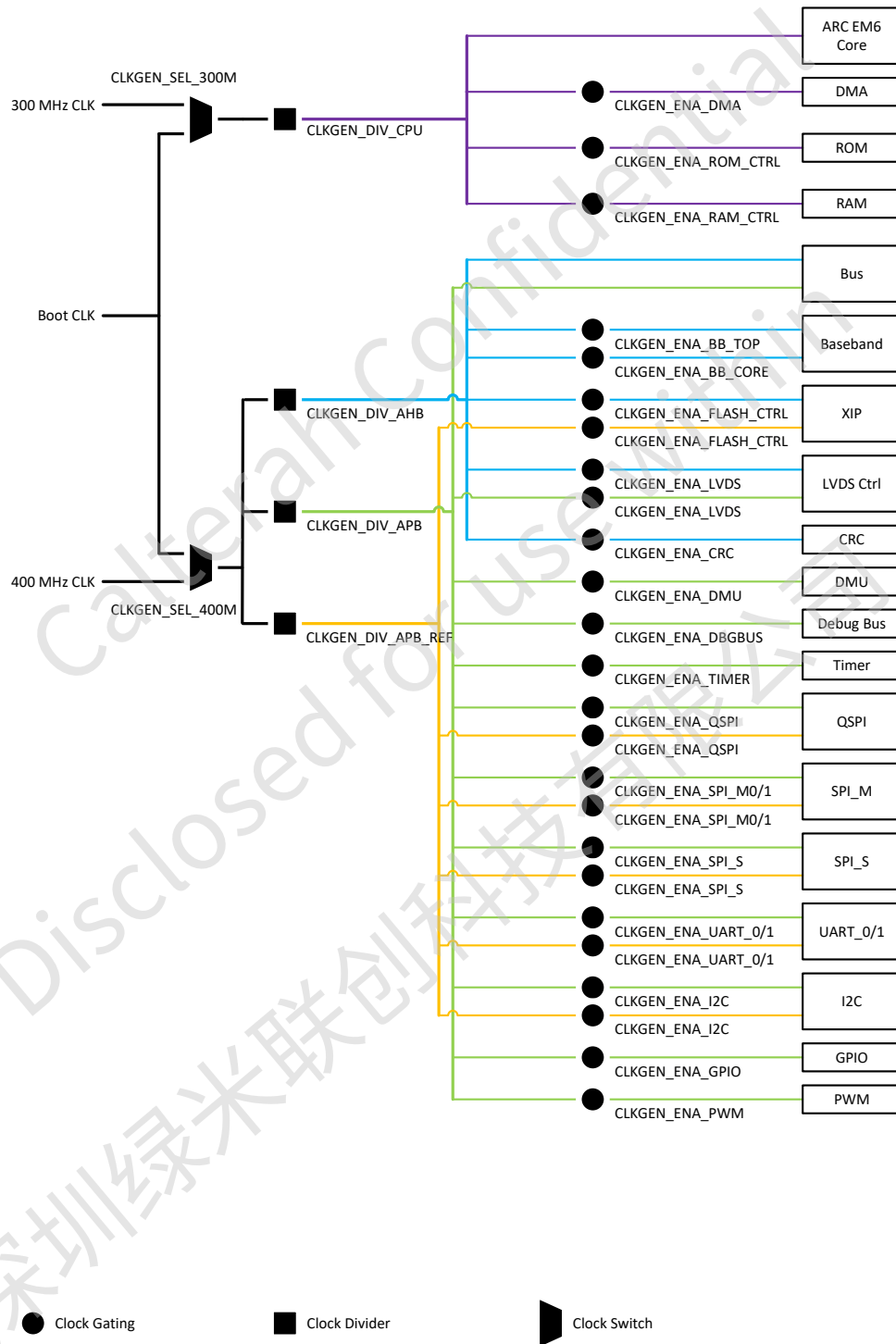


Fig. 6.12: Clock Architecture of CAL60S244-IB-A

6.2.2 Safety

The safety module Error Management Unit (EMU) is at the top of the hierarchy of Rhine. After PoR (power on reset) or external hard reset, the EMU starts the built-in self test (BIST), boots the system, and monitors the operation.

6.2.3 Core

The Core consists of one ARC CPU, one 16 KiB ROM, one 576 KiB RAM, one 8-channel DMA, and one XIP module with 4 KiB buffer. Since the ARC CPU normally runs at 300 MHz while the rest of the system runs at different frequencies, a cross-clock-domain bridge is adopted to connect them.

- ARC CPU

The ARC CPU integrated here is a little-endian CPU with a three-stage pipeline. The size of I-Cache, D-Cache, ICCM, and DCCM is all 32 KiB. One real timer counter and two normal timers are integrated, as well as a watchdog timer. A single precision FPU is integrated which takes 2 clock cycles to finish a multiplication and 17 clock cycles to finish one division.

- ROM

The 16 KiB ROM contains a pre-defined boot code. By executing it, CPU can boot from Flash, UART, and SPI.

- RAM

The RAM contains 576 KiB space.

- DMA

The DMA module has 8 channels and one AHB master interface, which supports memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers, while either hardware handshaking or software handshaking interface is provided.

- XIP

The XIP module contains one 4 KiB instruction buffer and one 512B data buffer.

The 4 KiB instruction buffer can be mapped to 8 individual 16/32/64/128/256/512-byte spaces, or 4 individual 1024-byte spaces, or 2 individual 2048-byte spaces, or 1 individual 4096-byte space in the external flash.

The 512B data buffer can be mapped to 16/32/64/128/256/512-byte space in the external flash for read, or 256/512-byte space in the external flash for write.

XIP function can be manually turned on or off.

6.2.4 Baseband

Digital baseband is responsible for the processing of IF signals from the radio subsystem. It consists of four main parts, which are data sampling, FFT, CFAR, and DoA, and other advanced features.

- Data sampling

Data sampling serves for extracting valid ADC data in each chirp. Since the lowest sampling frequency is 20 MHz, a digital decimation filter is integrated to support SRR related applications.

- FFT

The 2D-FFT engine is configurable with range-FFT size ranging from 64 to 2048 points and Doppler-FFT size from 64 to 1024. But the product of the two FFT sizes is limited by the 2-MiB FFT memory.



- CFAR

Two types of combination are supported in CFAR: coherent (or MIMO) and non-coherent (or SISO). The supported CFAR algorithms include CA, OS, SOGO, and NR. Up to 1024 objects can be reported by CFAR engine.

- DoA

DoA solves the angles of CFAR outputs. As a multi-object DoA, it searches up to 4 angles for each CFAR output.

- Advanced features

- Virtual array

This feature provides the capability to increase the resolution of DoA estimation by virtualizing more RX channels.

- Interference avoidance

This feature avoids interference during field usage by avoiding frequency and time collisions.

- Frame interleaving

This feature allows users to program up to four different types of frames at a time and use them for different application scenarios.

- Anti velocity ambiguity

This feature provides different solutions to solve the velocity ambiguity issue arising from sub-sampling at Doppler domain.

For detailed information and other features, refer to *Calterah Rhine Radar Baseband User Guide*.

6.2.5 Peripherals

The Peripherals part contains two UARTs, one master I²C, one slave SPI, two master SPIs, one master QSPI, one GPIO, one OTP memory, four timers, and two PWMs. All those peripherals are accessed through APB bus in one layer.

- UART × 2

Two individual UARTs are integrated in the processor subsystem. Each UART has a 32-byte TX FIFO and a 32-byte RX FIFO. Baud rate is configurable, while the typical baud rate is 921,600.

- I²C master

The I²C master has an 8-byte TX FIFO and an 8-byte RX FIFO.

- QSPI master

The QSPI master has a 32-byte TX FIFO and a 32-byte RX FIFO. Transfer frequency is configurable, while the highest frequency is 50 MHz (refer to [Quad Serial Peripheral Interface \(QSPI\)](#)).

- SPI master × 2

Two individual SPI masters are integrated in the processor subsystem. One SPI master has three selection lines, while the other has one selection line. Each of them has a 32-byte TX FIFO and a 32-byte RX FIFO. Transfer frequency is high configurable, while the highest frequency is 50 MHz (refer to [SPI Master I/O Timing](#)).

- SPI slave/QSPI slave

The SPI slave/QSPI slave has a 32-byte TX FIFO and a 32-byte RX FIFO. The maximum transfer frequency to which this SPI slave can respond is 50 MHz (refer to [SPI Slave I/O Timing](#)).

- GPIO

- Up to 31 independently configurable signals

- 16 configurable external interrupts
- OTP Memory
 - Accessed through multiple sources
 - ECC protection
 - Program and read locks
- Timer × 4
 - Up to four programmable timers.
 - Support for two operation modes: free-running and user-defined count.
 - Support for independent clocking of timers.
- PWM × 2
 - Programmable pulse-width modulation of timer toggle outputs.
 - Pulse width modulation of timer toggle output with 0% and 100% duty cycle.

6.2.6 DMU

The debug management unit (DMU) is responsible for:

- Radio command
- ADC control
- DAC control
- Interrupts
- IO mux configuration

6.2.7 Processor Subsystem Memory Map

Table 6.2: Memory Map of Rhine

Name	Mapping Space	Valid Size (Byte)	Bus	Cacheable	Description
ROM	0x000000-0x003FFF	16 K	AHB	Yes	Boot ROM
DMA	0x080000-0x0803FF	1 K	AHB	No	Register interface of DMA
ICCM	0x100000-0x107FFF	32 K		Yes	Instruction closely coupled memory
XIP (mem)	0x300000-0x6FFFFFFF	4 M/16 K	AHB	Yes	Memory interface of XIP; 4 M when XIP is on; 16 K when XIP is off, starting from 0x6FC000
RAM	0x770000-0x7FFFFFFF	576 K	AHB	Yes	RAM
RAM (shared)	0x800000-0x9FFFFFFF	2 M	AHB	Yes	Baseband shared memory
DCCM	0xA00000-0xA07FFF	32 K		No	Data closely coupled memory
EMU	0xB00000-0xB00FFF	4 K	APB	No	Register interface of EMU (Error Management Unit)
Timer	0xB10000-0xB100FF	256	APB	No	Register interface of Timer
CLKGEN	0xB20000-0xB20FFF	4 K	APB	No	Register interface of clock and reset management modules
UART0	0xB30000-0xB300FF	256	APB	No	Register interface of UART 0

continues on next page



6.2. Processor Subsystem

Table 6.2 – continued from previous page

Name	Mapping Space	Valid Size (Byte)	Bus	Cache-able	Description
UART1	0xB40000-0xB400FF	256	APB	No	Register interface of UART 1
I2C_M	0xB50000-0xB500FF	256	APB	No	Register interface of I ² C master
SPI_M0	0xB60000-0xB600FF	256	APB	No	Register interface of SPI master 0
SPI_M1	0xB70000-0xB700FF	256	APB	No	Register interface of SPI master 1
SPI_S	0xB80000-0xB800FF	256	APB	No	Register interface of SPI slave
QSPI_M	0xB90000-0xB900FF	256	APB	No	Register interface of QSPI master
DMU (radio_ctrl)	0xBA0000-0xBA00FF	256	APB	No	Register interface of radio configuration
DMU (debug_bus)	0xBA0100-0xBA01FF	256	APB	No	Register interface of Debug Bus
DMU (io_mux)	0xBA0200-0xBA02FF	256	APB	No	Register interface of IO mux
DMU (sys_config)	0xBA0300-0xBA03FF	256	APB	No	Register interface of system configuration
DMU (sw_interrupt)	0xBA0400-0xBA04FF	256	APB	No	Register interface of software interrupt
DMU (cpu_irq_mask)	0xBA0500-0xBA05FF	256	APB	No	Register interface of CPU interrupt mask
PWM	0xBD0000-0xBD00FF	256	APB	No	Register interface of PWM
GPIO	0xBE0000-0xBE00FF	256	APB	No	Register interface of GPIO
OTP	0xBF0000-0xBF01FF	512	APB	No	OTP memory
BB (reg)	0xC00000-0xC00FFF	4 K	AHB	No	Register interface of baseband
CRC (reg)	0xC10000-0xC100FF	256	AHB	No	Hardware CRC
XIP (reg)	0xD00000-0xD001FF	512	APB	No	Register interface of XIP
LVDS	0xD10000-0xD100FF	256	APB	No	Register interface of LVDS
BB (mem)	0xE00000-0xFFFFF	2 M	AHB	No	Memory interface of baseband

Note: The mapping space for DMA is available only in CAL60S244-IB-A.



PACKAGE

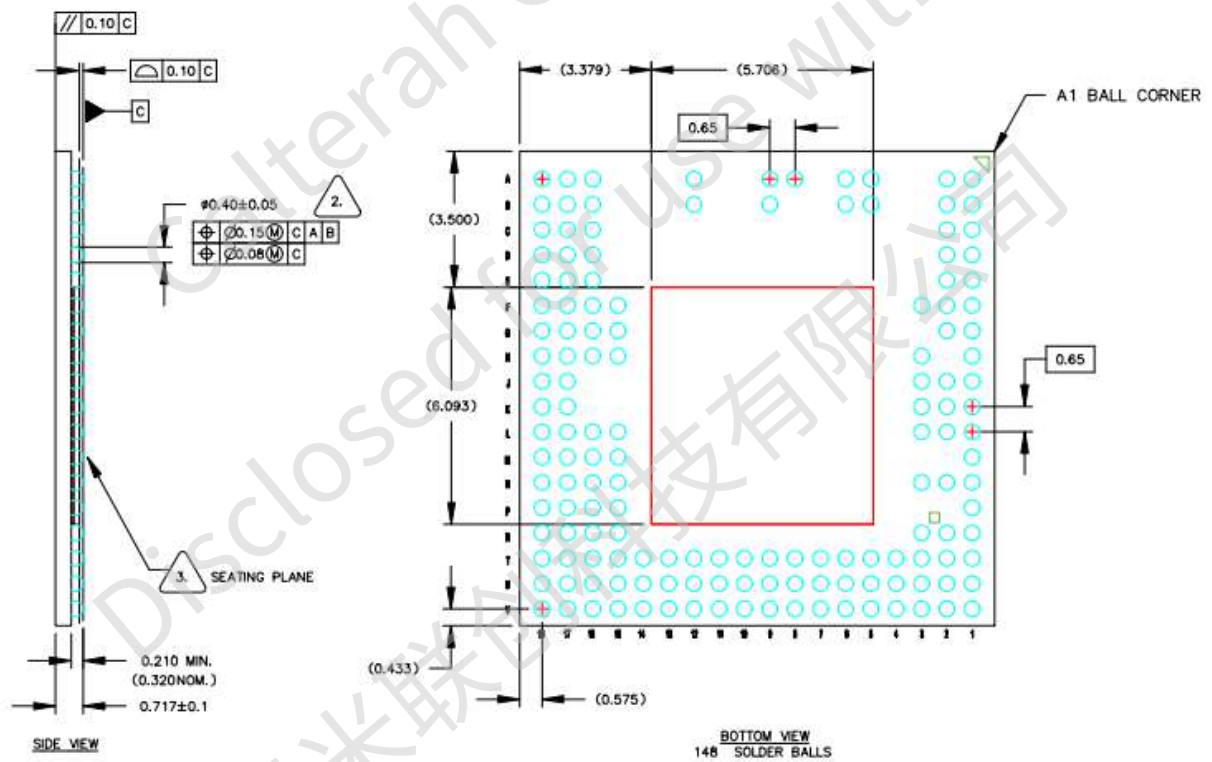
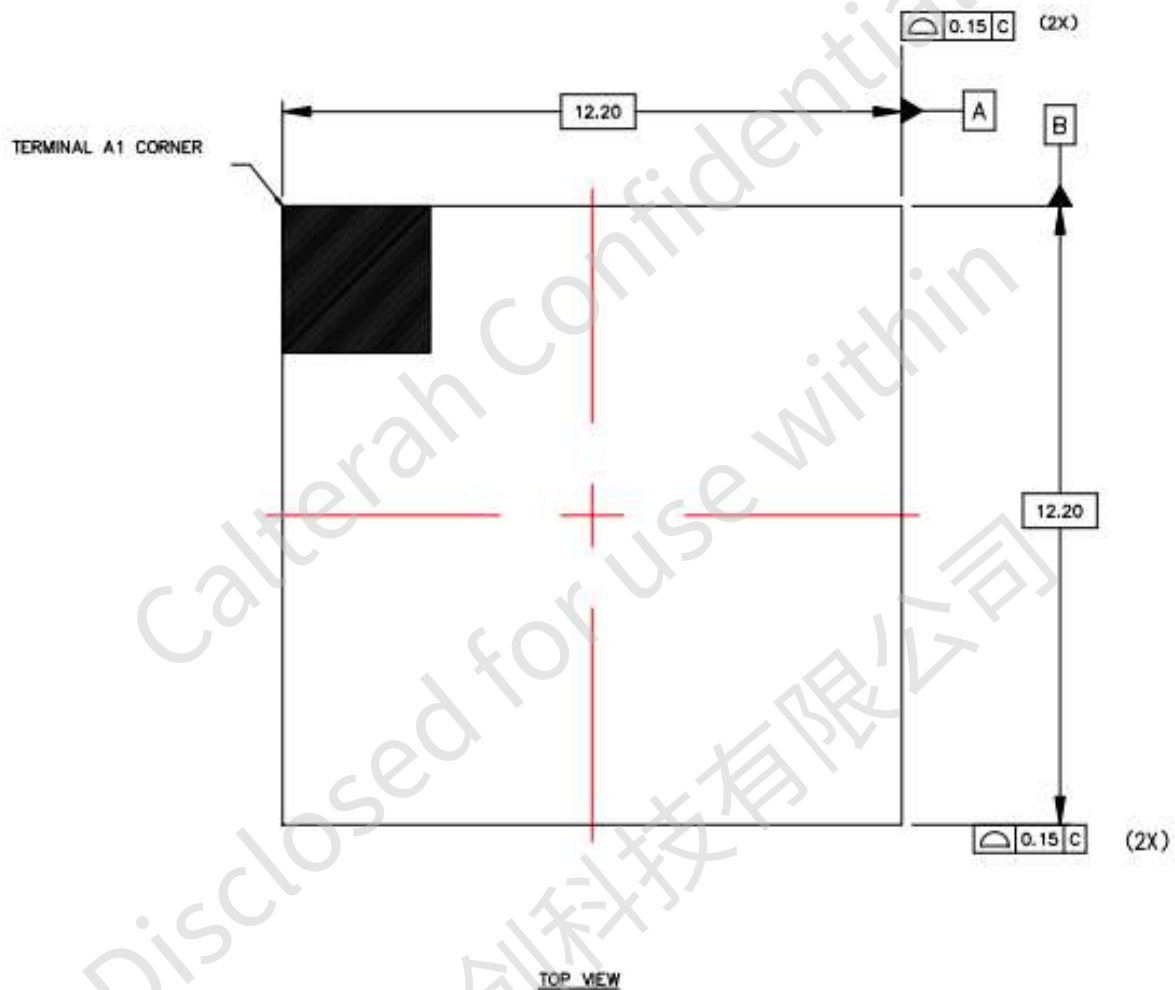


Fig. 7.1: Package Outline Drawing (POD) 1



4. REFERENCE SPECIFICATIONS:

A. AWW SPEC #001-2234: PACKING OPERATION PROCEDURE

B. AWW SPEC #001-2062: MARKING



3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS



2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5 - 2009

NOTES: UNLESS OTHERWISE SPECIFIED

Fig. 7.2: Package Outline Drawing (POD) 2

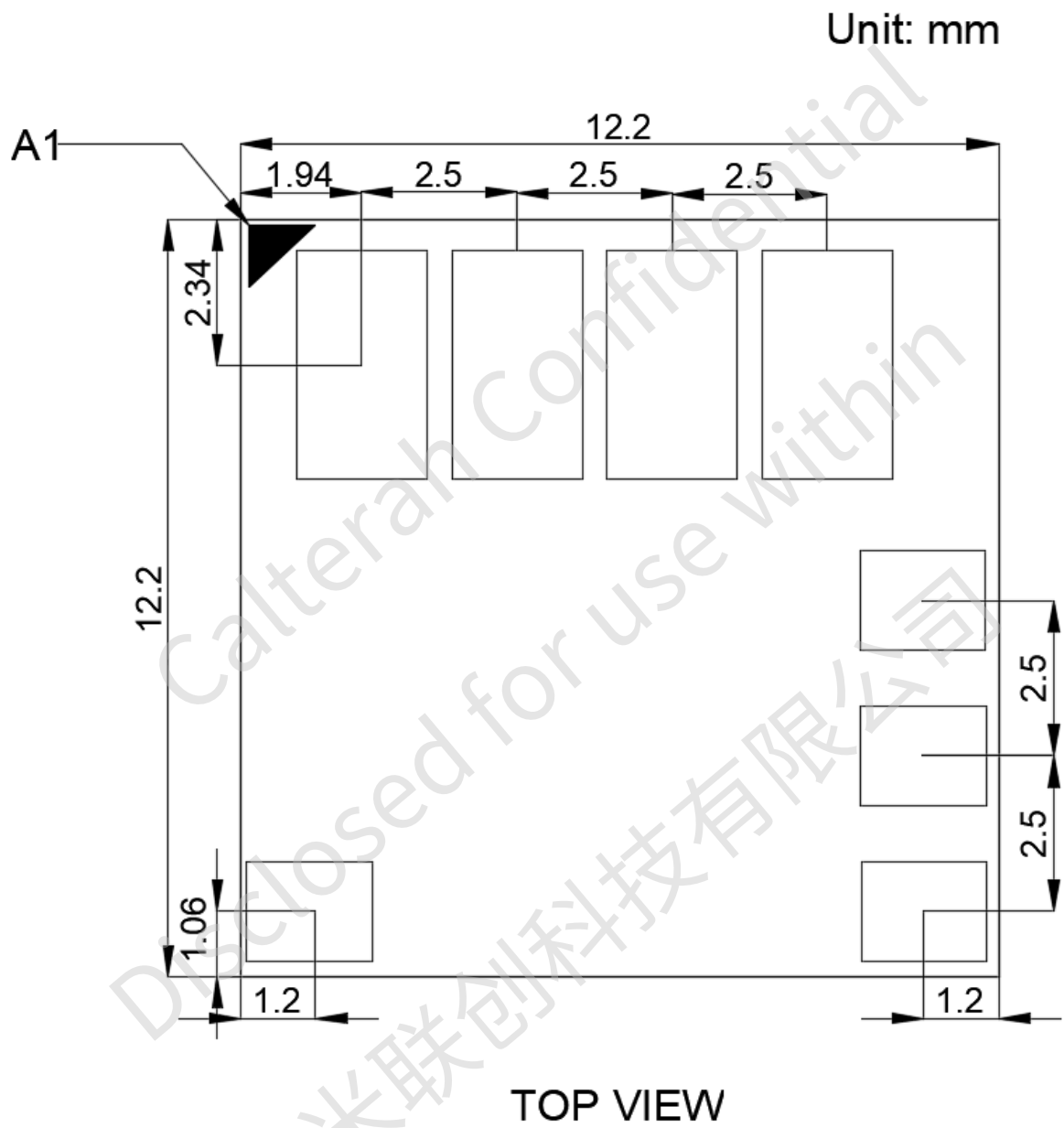


Fig. 7.3: Package Outline Drawing (POD) 3



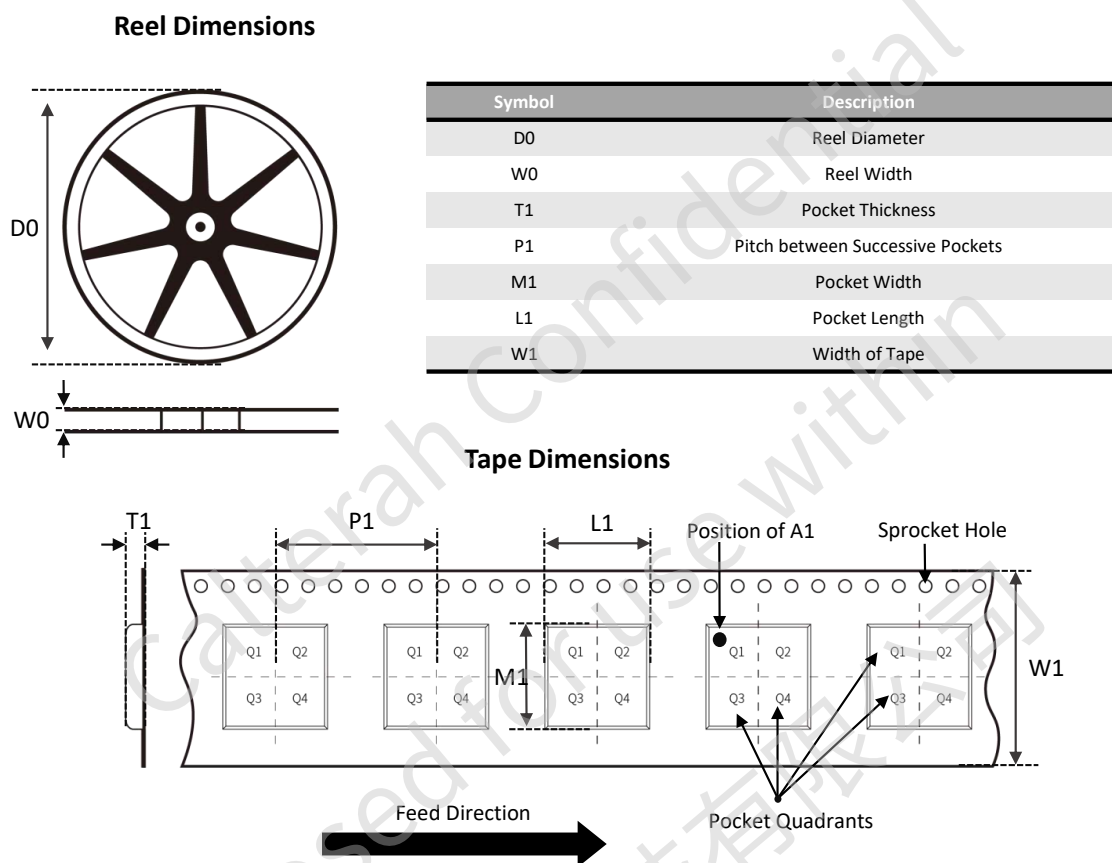


Fig. 7.4: Tape and Reel Information

Table 7.1: Detailed Tape and Reel Information

Device	CAL60S244-IB(-A)	
Package	FCCSP	
SPQ	500	
Reel Diameter D0 (mm)	178	+2 -2
Reel Width W0 (mm)	25.4	+3 -1
L1 (mm)	12.5	+0.1 -0.1
M1 (mm)	12.5	+0.1 -0.1
T1 (mm)	1.4	+0.1 -0.1
P1 (mm)	16	+0.1 -0.1
W1 (mm)	24	+0.3 -0.1
A1 Ball (Quadrant)	Q1	
Moisture Sensitivity Level (MSL)	Level-3-260 °C -168hrs	

REVISION HISTORY

Table 1.1: Revision History

Revision	Description	Author
0.9 / March 2020	Preliminary release for the mass production version.	pwang
1.0 / July 2020	Official release for the mass production version.	pwang
1.0.1 / January 2021	In the Introduction chapter, changed conversion gain range from 34~70 dB to 32~73 dB. In the Device Information chapter, - Corrected errors in the Chip Signal Definitions table. - Corrected errors in the Pin Multiplexing table. - Changed the prefix <i>gpio_</i> to <i>dbgbus_</i> in the Pin Control Value (4) column. In the Specifications chapter, - Added a note about room temperature and power supply requirements at the beginning. - Updated values for CDM in the ESD Ratings table. - Added electrical characteristics of auxiliary ADCs. In the Radiation Characteristics chapter, - Changed TX0 to TX1/2/3 azimuth separation from 10 mm to 9.8 mm. - Added descriptions of hardware design impact on radiation performances. In the Timing Characteristics chapter, updated the Power on Timing figure and added a note to it. In the Detailed Descriptions chapter, - Added electrical characteristics of the clock crystal. - Changed the clock frequency for the temperature sensor from 12.5 MHz to 5 MHz. - Updated the sizes of BB (reg) and DMA in the memory map table. In the Package chapter, added POD3. Added Important Notice and Disclaimer at the end of the document. Other minor improvements.	pwang
1.0.2 / June 2021	In the Introduction chapter, added information about CAL60S244-AB. In the Pin Multiplexing table of the Device Information chapter, updated the reset state for ADC_RESET_M. In the Package chapter, added tape and reel information. Other refinement.	pwang

continues on next page

Table 1.1 – continued from previous page

Revision	Description	Author
1.0.3 / March 2022	In the Chip Signal Definitions table, changed the pin type of TP_ANA from AO to AIO. In the Specifications chapter, added the I/O DC Electrical Specifications section. In the Timing Characteristics chapter, updated the descriptions for I²C, SPI, and QSPI. In the Peripherals section of the Detailed Descriptions chapter, updated the description of GPIO. In the Package chapter, updated the POD1 and POD2 figures to modify the body thickness and added the MSL information in the Detailed Tape and Reel Information table. Other minor improvement.	pwang
1.0.4 / December 2022	In the QSPI I/O Timing table, changed the minimum value of reference clock cycle time from 5 ns to 2.5 ns. Updated the Detailed Tape and Reel Information table. Other minor improvement.	pwang
1.1 / September 2023	Added descriptions of the variant part number CAL60S244-IB-A throughout the document, including: - In the Introduction chapter, added a note to explain the part number CAL60S244-IB-A and to summarize the major functionality differences between CAL60S244-IB and CAL60S244-IB-A. - In the Introduction chapter, added a footnote to the Chip Block Diagram figure. - In the Specifications chapter, added the table ESD Ratings for CAL60S244-IB-A. - In the Detailed Descriptions chapter, added descriptions of Hardware Auto Frame Mode and Doppler spur randomization, which are available in the variant part number CAL60S244-IB-A. - In the Detailed Descriptions chapter, added the clock architecture figure of CAL60S244-IB-A. In the Introduction chapter, removed the description of TX power detectors from the Features section. In the Timing Characteristics chapter, updated the Power on Timing figure and its corresponding note. In the Memory Map of Rhine table, updated the information about DMA. In the Detailed Tape and Reel Information table, updated MSL information.	pwang



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