FSC-BT825

4.2 Dual Mode Bluetooth Module Data Sheet

Shenzhen Feasycom Technology Co.,Ltd

Document Type: FSC-BT825

Document Version: V1.1

Release Date: Jun 21. 2019

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Release Record

Version Number	Release Date	Comments
Revision 1.0	2016-06-24	First Release
Revision 1.1	2019-06-21	1,Upgrade Bluetooth version to BT4.2 2,Modify the description of the error

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1. INTRODUCTION

FSC-BT825 is a fully integrated Bluetooth module that complies with Bluetooth 4.2 dual mode protocols (BR/EDR and LE). It supports SPP, HID, GATT, ATT, and other profiles. It integrates Baseband controller and RF antenna in a small package, so the designers can have better flexibilities for the product shapes.

FSC-BT825 can be communicated by UART port. With Feasycom's Bluetooth stack, Customers can easily transplant to their software. Please refer to Feasycom stack design guide.

1.1 Block Diagram

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1.2 Feature

- Fully qualified Bluetooth 4.2/4.0/3.0/2.1/2.0/1.2/1.1
- Postage stamp sized form factor
- Low power
- Class 1.5 support(high output power)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921.6Kbps
- UART, PCM hardware interfaces
- Bluetooth stack profiles support: SPP, HID, GATT, ATT, GAP
- Support Apple MFi (iAP2), iBeacon

1.3 Application

- Smart Watch and Bluetooth Bracelet
- Health & Medical devices
- Wireless POS
- Measurement and monitoring systems
- Industrial sensors and controls
- Asset tacking

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2. GENERAL SPECIFICATION

General Specification	
Chip Set	RTL8761
Product ID	FSC-BT825
Dimension	10.8mm(W) x 13.5mm(L) x 1.8mm(H)
Bluetooth Specification	Bluetooth V4.2 (Dual Mode)
Power Supply	3.3 Volt DC
Output Power	5.5 dBm (Class 1.5)
Sensitivity	-82dBm@0.1%BER
Frequency Band	2.402GHz -2.480GHz ISM band
Modulation	GFSK, π/4-DQPSK, 8-DPSK
Baseband Crystal OSC	40MHz
Hopping & channels	1600hops/sec, 1MHz channel space,79 Channels(BT 4.2 to 2MHz channel space)
RF Input Impedance	50 ohms
Antenna	Internal (Default) External (Option)
Interface	UART, PCM
Profile	SPP, HID, GATT, ATT, GAP
Advanced Feature	MFi, Airsync, iBeacon
Temperature	-20ºC to +70 ºC
Humidity	10%~95% Non-Condensing
Environmental	RoHS Compliant

Table 1

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3. PHYSICAL CHARACTERISTIC

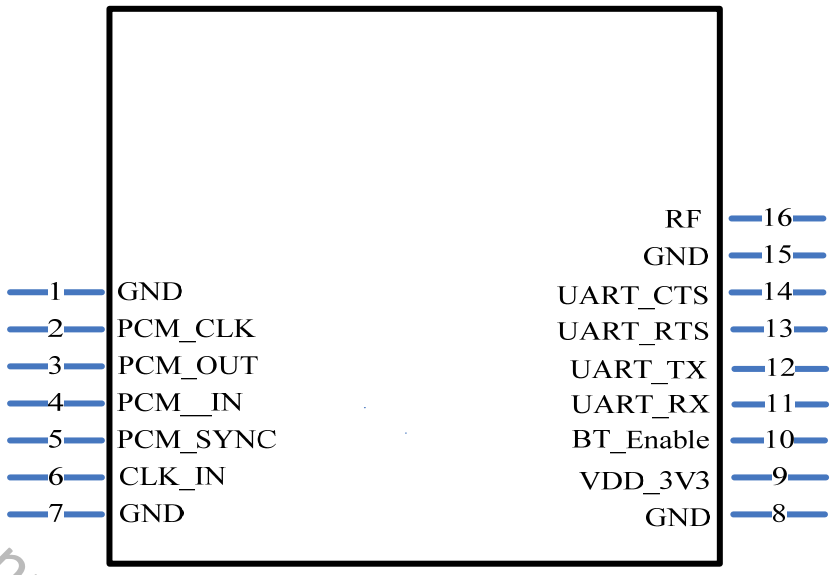

Figure 2: FSC-BT825 PIN Diagram

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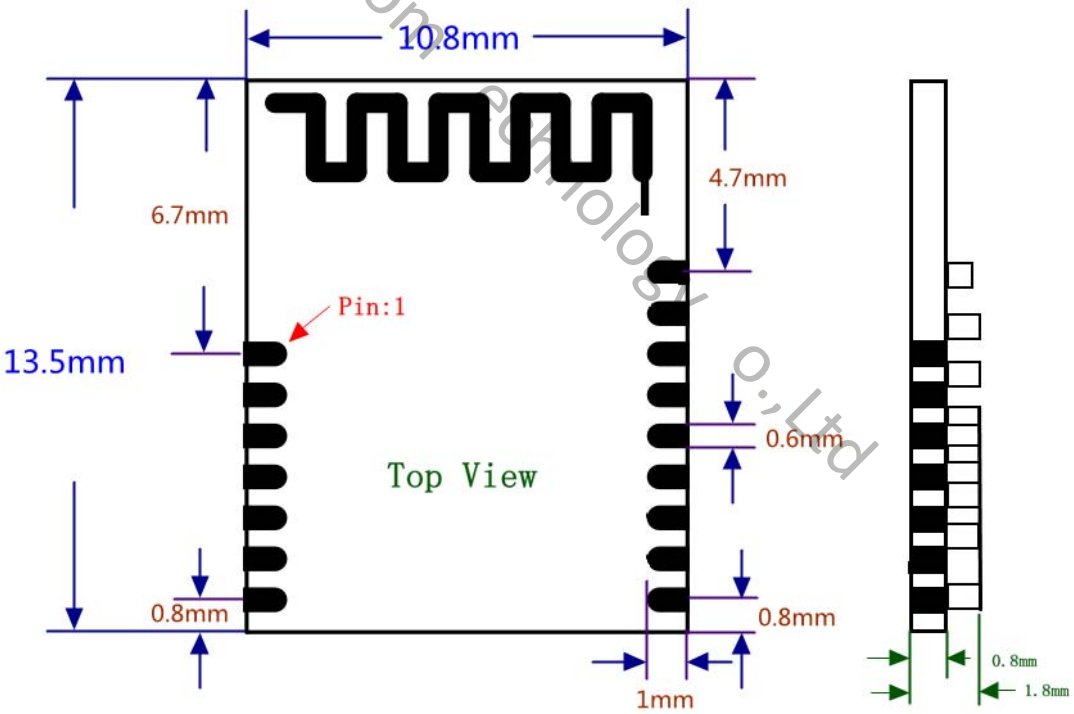

Figure 3: Pin Configuration and Package Dimensions（TOP VIEW）

4. PIN DEFINITION DESCRIPTIONS

Pin	Pin Name	Pad Type	Description
1	GND	VSS	Power Ground
2	PCM-CLK	Bi-directional	Synchronous data clock(operating votage level: 3.3V)
3	PCM_OUT	CMOS output	Synchronous data output(operating votage level: 3.3V)
4	PCM_IN	CMOS input	Synchronous data input(operating votage level: 3.3V)
5	PCM-SYNC	Bi-directional	Synchronous data sync(operating votage level: 3.3V)
6	CLK_IN	CMOS input	32.768kHZ clock in Connect to external clock(optional) NC (default)
7	GND	VSS	Power Ground
8	GND	VSS	Power Ground
9	VDD_3V3	VDD	Power supply voltage 3.3V
10	BT_Enable	CMOS input	Module enable input(active high) **Note:** VDD_3V3 must be stable before pulling up BT_Enable
11	UART_RX	CMOS input	UART data input
12	UART_TX	CMOS output	UART data output
13	UART_RTS	CMOS output	UART request to send active low
14	UART_CTS	CMOS input	UART clear to send active low
15	GND	VSS	Power Ground
16	RF	RF_IN/OUT	Bluetooth 50ohm transmitter output/receiver input NC if using internal antenna(default) Connect to external antenna(optional)

Table 2

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5. Interface Characteristics

5.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT825 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT825 module	Data from FSC-BT825 module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT825 module	Request to send output of FSC-BT825 module
UART-CTS	Host	Clear to send input of FSC-BT825 module

Table 3

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Default Data Format

Property	Possible Values
Baudrate	115. 2 Kbps
Flow Control	None
Data bit length	8bit
Parity	None
Number of Stop Bits	1

Table 4

Desired Baud Rate	Actual Baud Rate	Error (%)
300	300	0.00%
600	600	0.00%
900	900	0.00%
1200	1200	0.00%
1800	1800	0.00%
2400	2400	0.00%
3600	3601	0.03%
4800	4798	-0.04%
7200	7198	-0.03%
9600	9603	0.03%
14400	14395	-0.03%
19200	19182	-0.09%
28800	28846	0.16%
38400	38462	0.16%
56000	55970	-0.05%
57600	57692	0.16%
76800	76531	-0.35%
115200	115385	0.16%
128000	127119	-0.69%

Desired Baud Rate	Actual Baud Rate	Error (%)
153600	153061	-0.35%
230400	229167	-0.54%
460800	458333	-0.54%
500000	500000	0.00%
921600	916667	-0.54%
1000000	1000000	0.00%
1382400	1375000	-0.54%
1444444	1437500	-0.48%
1500000	1500000	0.00%
1843200	1833333	-0.54%
2000000	2000000	0.00%
2100000	2083333	-0.79%
2764800	2777778	0.47%
3000000	3000000	0.00%
3250000	3250000	0.00%
3692300	3703704	0.31%
3750000	3750000	0.00%
4000000	4000000	0.00%

Table 5. UART Interface Power-On Timing Parameters

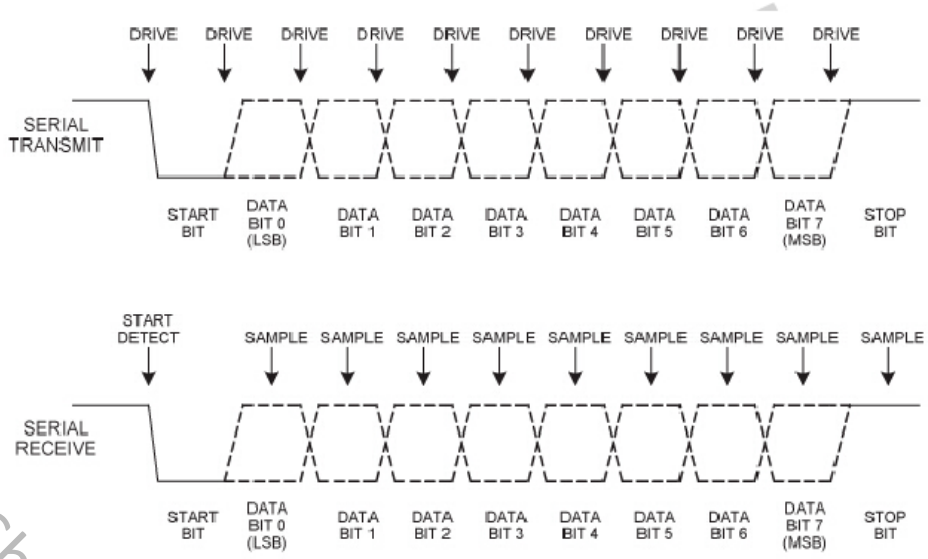

Figure 4: UART Interface Waveform PIN diagram

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5.1.1 UART Interface Power-On Sequence

The UART interface power-on sequence differs depe nding on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

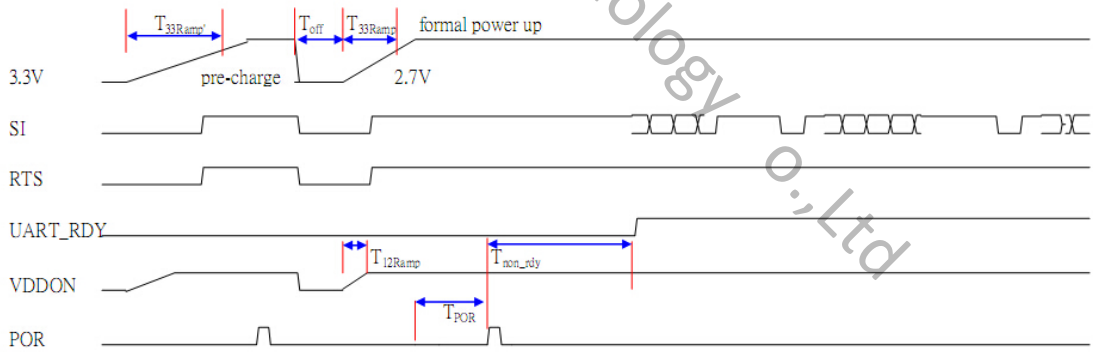

Figure 5: UART Power-On Sequence without Hardware Flow Control

UART Hardware Flow Control Supported

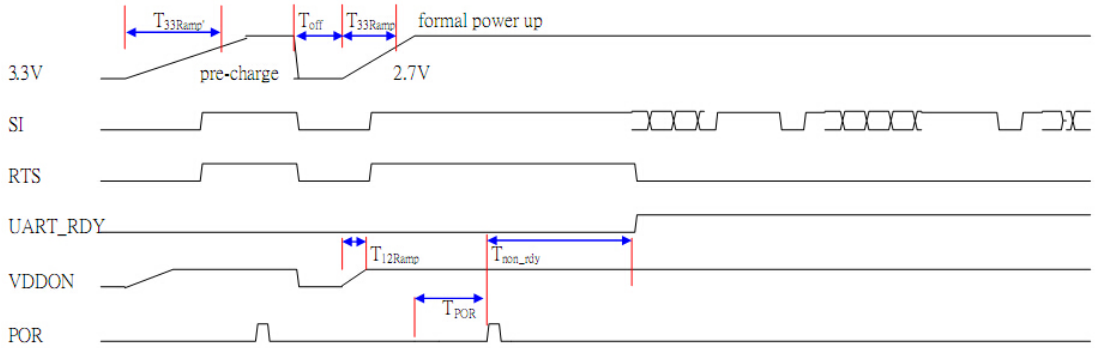

Figure 6: UART Power On Sequence with Hardware Flow Control

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the FSC-BT825 will not respond to any commands.

Table 6: UART Interface Power-On Sequence

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In this state, the FSC-BT825 will not respond to any commands. divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the Toff period. The ramp up time is specified in the T33ramp duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enable s the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to waiting the Tnon_rdy time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

	Min	Tyupical	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

Table 7: UART Interface Power On Timing Parameters

5.2 PCM CODEC Interface

The FSC-BT825 supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/u-law, and 13/16-bit linear PCM formats
- Supports Master and Slave mode
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports Master and Slave mode
- Supports SCO/ESCO link

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5.2.1 PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync, and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSnc.

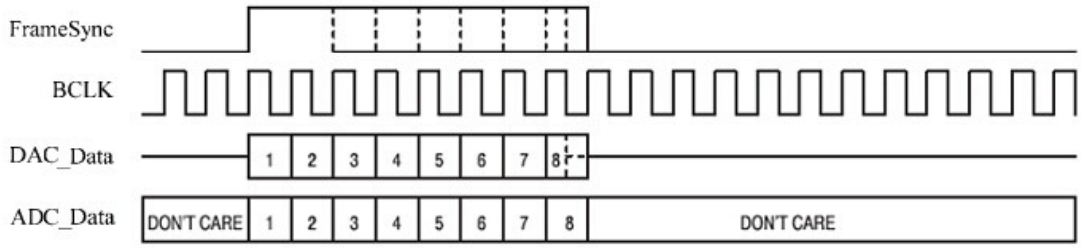

Figure 7. Long FrameSync

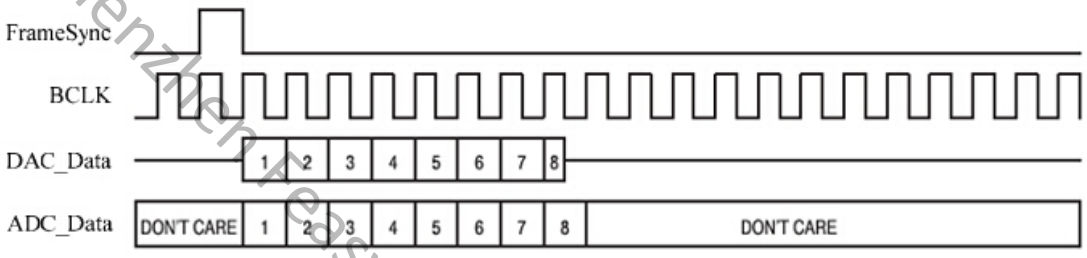

Figure 8. Short FrameSync

5.2.2 Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

◆For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

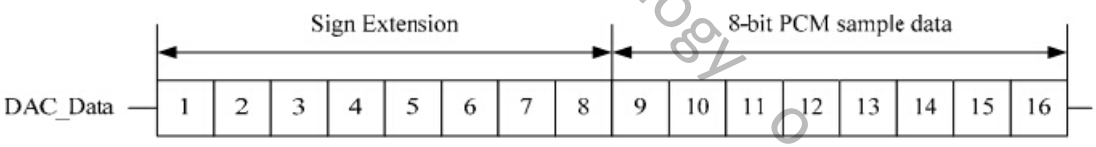

Figure 9. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

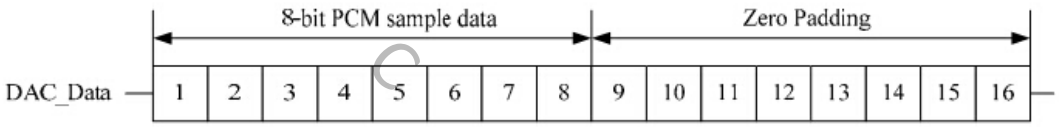

Figure 10 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

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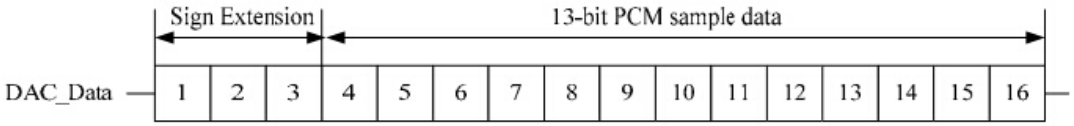

Figure 11. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

◆For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

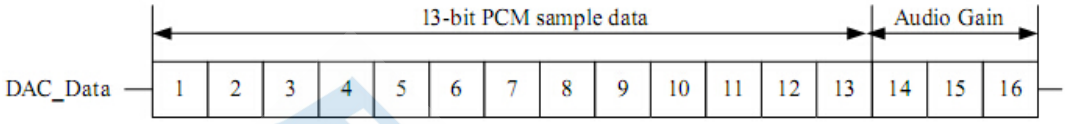

Figure 12. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

5.2.3 PCM Interface Timing

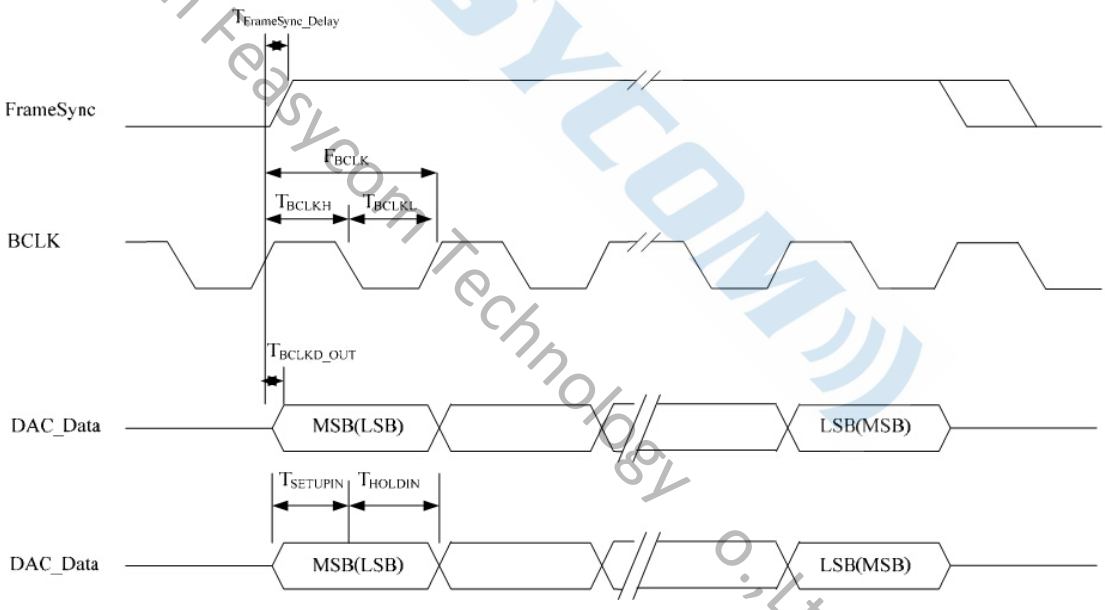

Figure 13: PCM Interface (Long FrameSync)

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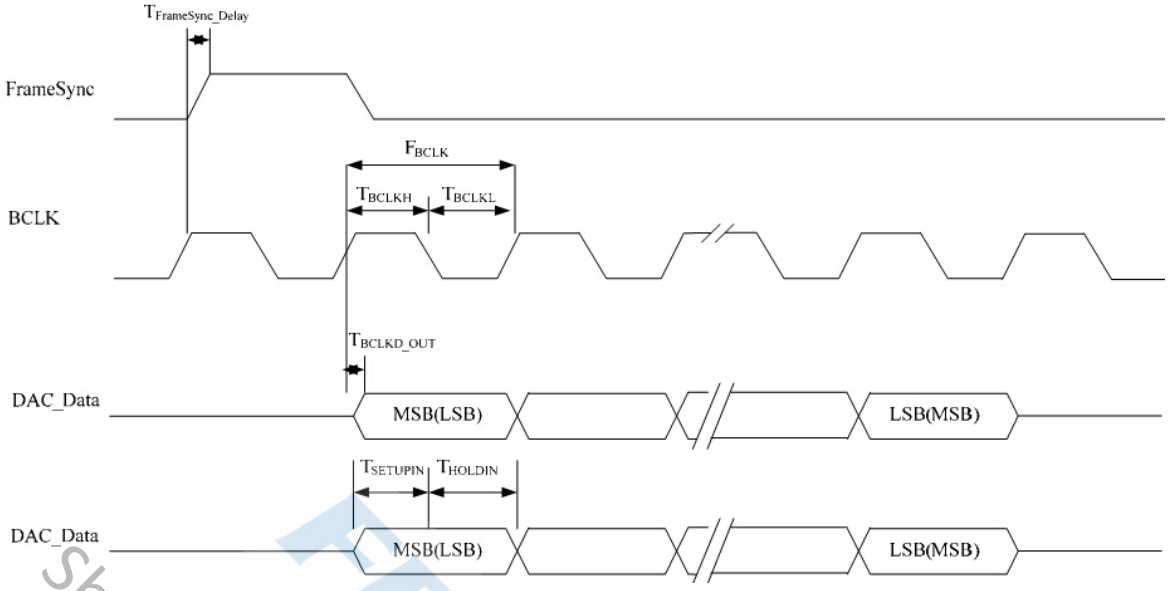

Figure 14: PCM Interface (Short FrameSync)

Symbol	Description	Min	Typ	Max	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	KHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	8	KHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	KHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	KHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

Table 8: PCM Interface Clock Specifications

Symbol	Description	Min	Typ	Max	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$F_{FrameSync_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns

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T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

Table 9: PCM Interface Timing

5.2.4 PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the FSC-BT825 PCM interface.

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6. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 14 and Figure 15 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
  - Average ramp-up rate(217℃ to peak):1~2℃/sec max.
  - Preheat:150~200C,60~180 seconds
  - Temperature maintained above 217℃:60~150 seconds
  - Time within 5℃ of actual peak temperature:20~40 sec.
  - Peak temperature:250+0/-5℃ or 260+0/-5℃
  - Ramp-down rate:3℃/sec.max.
  - Time 25℃ to peak temperature:8 minutes max
  - Cycloe interval：5 minus

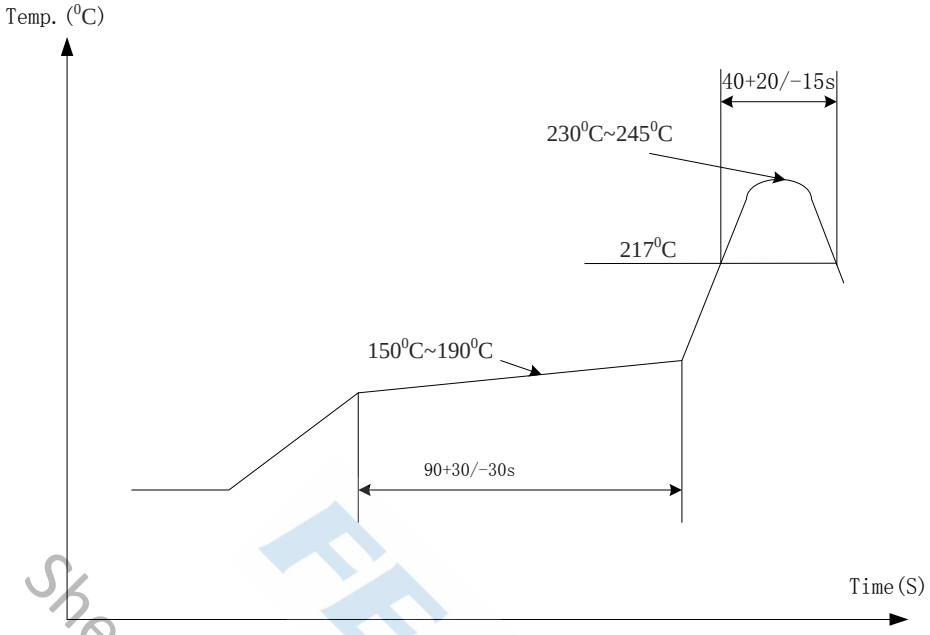

Figure 15 Typical Lead-free Re-flow Solder Profile

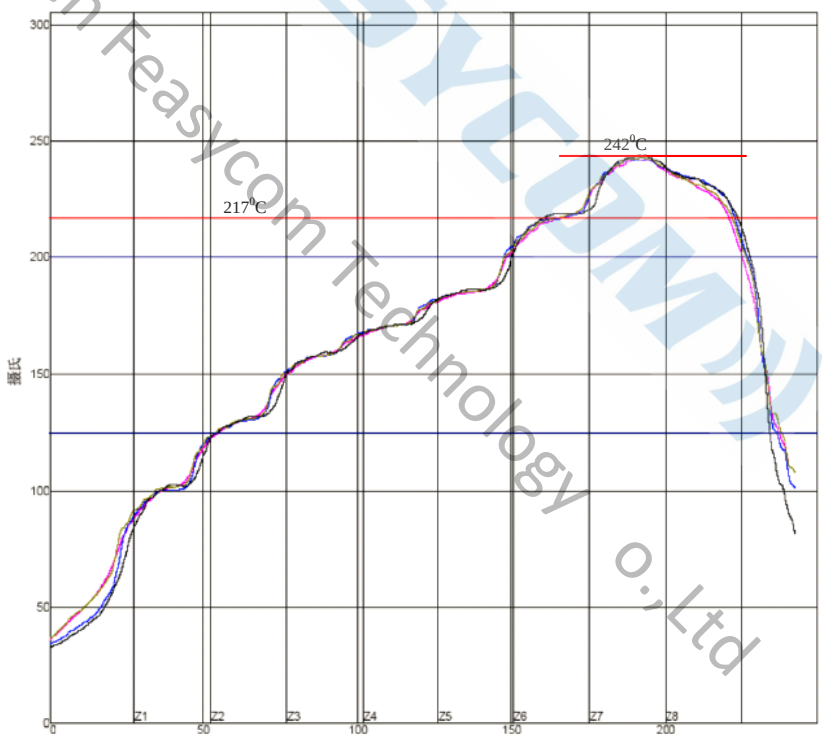

Figure16 Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT825 will withstand up to two re-flows to a maximum temperature of 245°C.

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7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －20℃ space for 1 hour and then move to +70℃ space within 1minute, after 1 hour move back to －20℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging information

After unpacking, the module should be stored in environment as follows:

Temperature: 25℃ ± 2℃

Humidity: <60%

No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

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8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT825 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

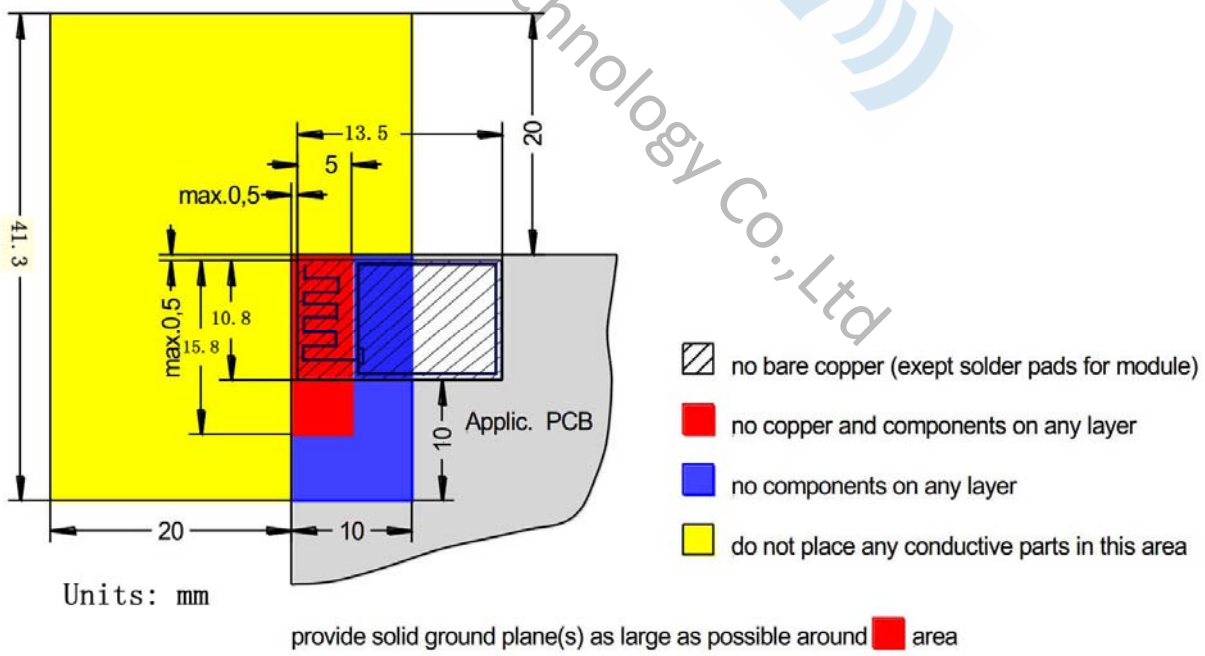

Figure 17: FSC-BT825 Restricted Area

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Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9. Application Schematic

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(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module. For 15 B (§15.107 and if applicable §15.107) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101.

Integrator is reminded to assure that these installation instructions will not be made available to the end user of the final host device.

The final host device, into which this RF Module isintegrated" has to be labelled with an auxilliary lable stating the FCC IDofthe RF Module, such as "Contains FCC ID: 2AMWOFSC-BT825

"This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1)this devicemay not cause harmful interference, and
(2)this devicemust accept any interference received, including interference thatmay cause undesired operation."

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection
against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
--Reorient or relocate the receiving antenna.
--Increase the separation between the equipment and receiver.
--Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
--Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Module statement

The single-modular transmitter is a self-contained, physically delineated, component for which compliance can be demonstrated independent of the host operating conditions, and which complies with all eight requirements of § 15.212(a)(1) as summarized below.

1) The radio elements have the radio frequency circuitry shielded.
2) The module has buffered modulation/data inputs to ensure that the device will comply with Part 15 requirements with any type of input signal.
3) The module contains power supply regulation on the module.
4) The module contains a permanently attached antenna.
5) The module demonstrates compliance in a stand-alone configuration.
6) The module is labeled with its permanently affixed FCC ID label
7) The module complies with all specific rules applicable to the transmitter, including all the conditions provided in the integration instructions by the grantee.
8) The module complies with RF exposure requirements.

This transmitter/module must not be collocated or operating in conjunction with any other antenna or transmitter.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC Part 15.247

2.3 Specific operational use conditions

This transmitter/module and its antenna(s) must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer's instruction manual.

2.4 Limited module procedures

not applicable

2.5 Trace antenna designs

not applicable

2.6 RF exposure considerations

This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This compliance to FCC radiation exposure limits for an uncontrolled environment, and minimum of 5mm separation between antenna and body.

The host product manufacturer would provide the above information to end users in their end-product manuals.

2.7 Antennas

PCB antenna; 2dBi; 2.402 GHz～2.480GHz

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