Important Instructions

WARNING

This kit is to be installed in accordance with the manufacturer's instructions and all codes and requirements of the authority having jurisdiction. In Canada, this conversion/installation shall be carried out in accordance with the requirements of the provincial authorities having jurisdiction and in accordance with the requirements of the CAN/CGA-B149.1 and CAN/CGA-B149.2 installation code. Failure to follow instructions could result in serious injury, death or property damage. The qualified agency performing this work assumes all responsibility for this kit installation.

W013R4

WARNING

To reduce the risk of electric shock, fire, explosion, serious injury or death:

- **Disconnect electric power to the machine before servicing.**
- **Close gas shut-off valve to the machine before servicing.**
- **Close steam gate valve to the machine before servicing.**
- **Never start the machine with any guards/panels removed.**
- **Whenever ground wires are removed during servicing, these ground wires must be reconnected to ensure that the machine is properly grounded.**

W017

Kit consists of:		
1	204890	Wireless Network Control
1	F8674006	Wireless Network Harness
2	D503661	Screws
2	55881	Wire Ties
1	XXXXXX	Conversion Label
1	F8673901	Network Option Diagram
1	XXXXXX	Wireless Control Label
1	8-18-253EN	Kit Instructions

Special Tools required for this kit:
Magnetic 5/16 in. Socket

IMPORTANT: This kit must be installed by a qualified service person.

NOTE: Refer to appropriate service manual to aid in the installation of this kit.

IMPORTANT: When reference is made to directions (right or left) in this instructions, it is from operator's position facing front of machine.

FCC COMPLIANCE STATEMENT

CAUTION

Changes or modifications not expressly approved could void your authority to use this equipment .

This device complies with Part 15 of the FCC Rules. Operation to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interfer-

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ence received, including interference that may cause undesired operation.

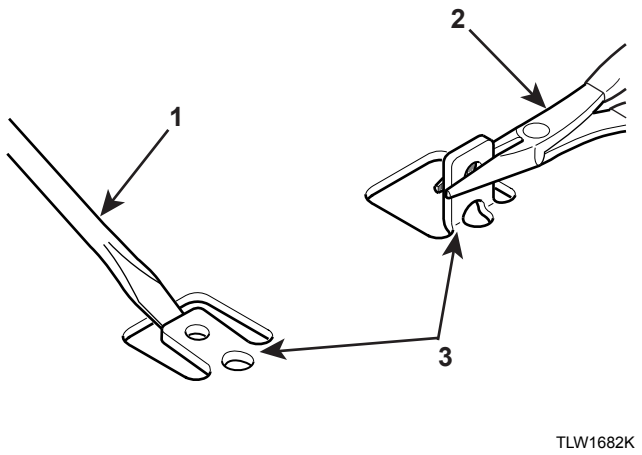
INDUSTRY CANADA STATEMENT

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

1. **IMPORTANT - Disconnect electrical power to machine.** Control will not recognize network board until power is cycled to machine.
2. Remove two control panel attaching screws and lay assembly forward on protective padding.

NOTE: There are four tabs located on backside of control panel frame. Only the two tabs closest to the control must be bent upward. Refer to *Figure 1* and *Figure 2* .

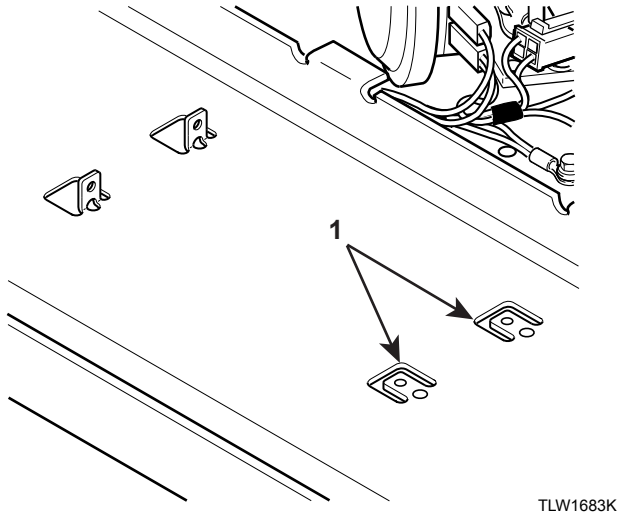


1. Screwdriver
2. Pliers
3. Tabs

Figure 1

3. Use a flat blade screwdriver and slightly bend each tab up only far enough to allow getting the jaws of a pliers under each tab and bend to 90 degrees. Make sure each tab is bent up square and straight.

IMPORTANT: Be careful not to damage control panel overlay when prying up tabs.



1. Do Not Bend

Figure 2

4. Adjust the compliance jumpers on the 204890 Wireless Network Control. Refer to *Compliance Jumper (H1)* section at the end of these instructions.
5. Remove double sided tape backing from 204890 Wireless Network Control.
6. Position 204890 Wireless Network Control so that the mounting tabs on the Network Board go in front of the tabs on the control panel and the assembly mounts to the right of the mounting tabs, as shown in *Figure 3* . (The control should be to the right of the mounting tabs.) Then attach using the (2) D503661 Screws. Refer to *Figure 3* .

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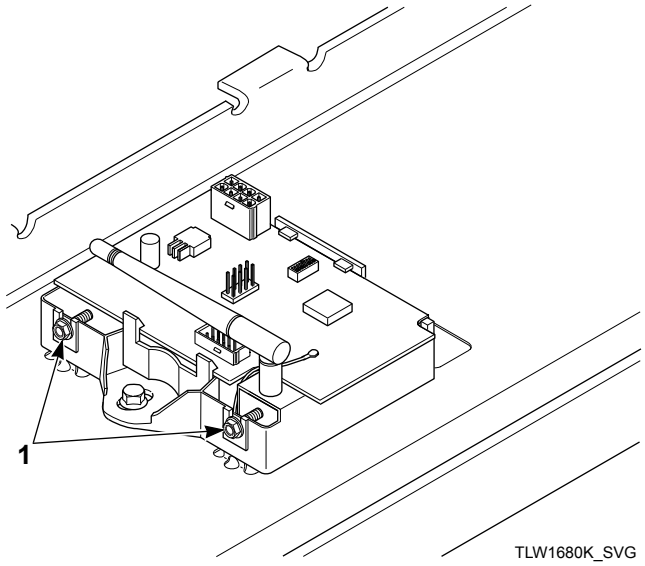
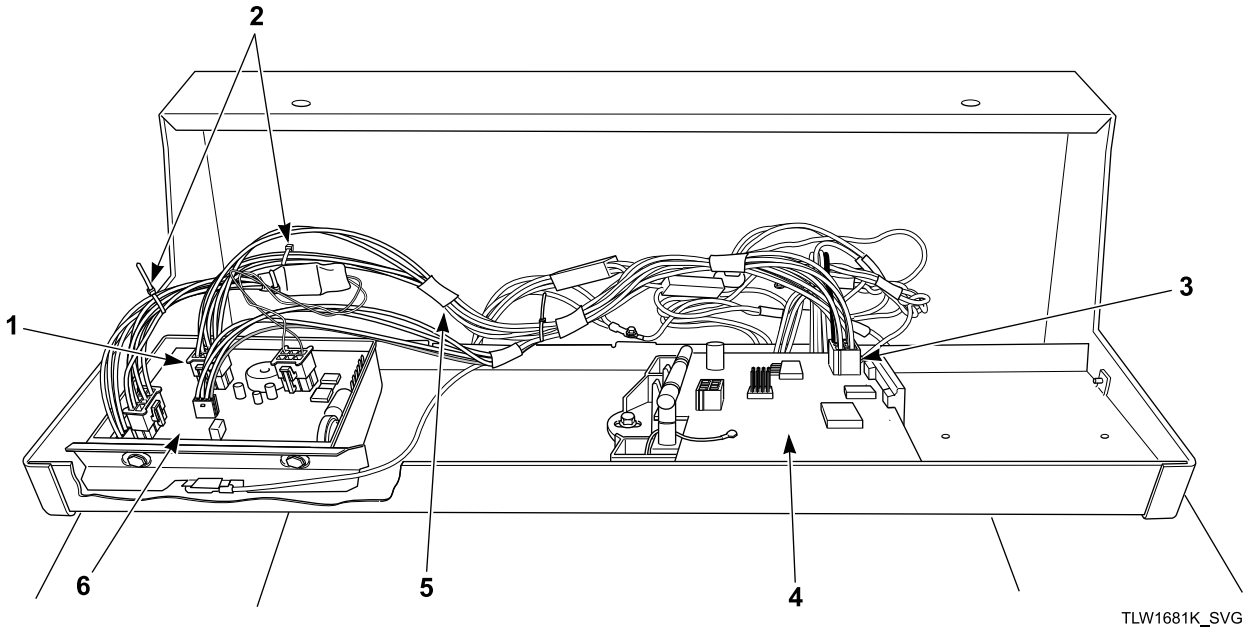


1. D503661 Screws

Figure 3

7. Install F8674006 Wireless Network Harness between network board "H3" and the electronic control "H1". Refer to *Figure 4* .
8. Secure the F8674006 Wireless Network Harness using the (2) 55881 Wire Ties as shown in *Figure 4* .
9. Place F8673901 Network Option Diagram in control cabinet with existing diagrams.
10. Place XXXXXX Wireless Control Label in the control hood be-hind the control panel.
11. Fill out and place XXXXXX Conversion Label in control hood behind control panel.
12. Reconnect electrical power to the machine.

NOTE: The machine control MUST have been powered down prior to connecting the wireless control in order for the control to recognize the board and to allow communication with it.



1. "H1"
2. 55881 Wire Ties
3. "H3"
4. 204890 Wireless Network Control
5. F8674006 Wireless Network Harness
6. Electronic Control

Figure 4

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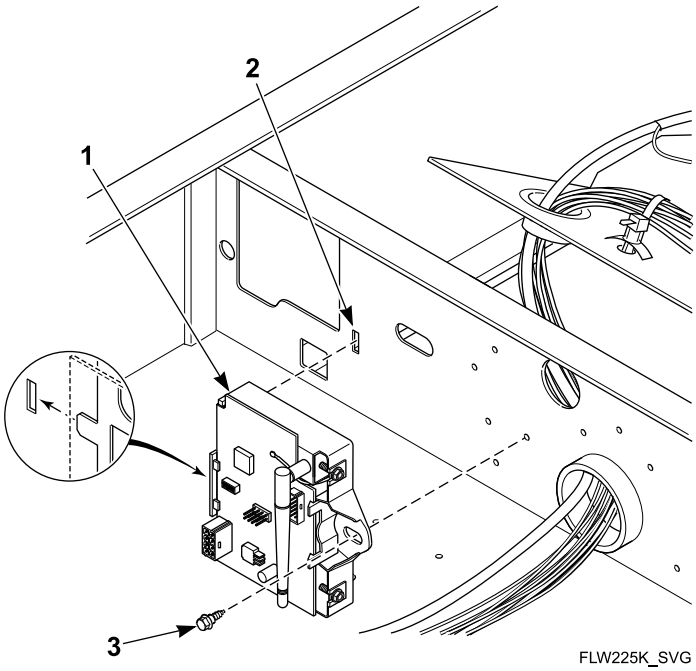
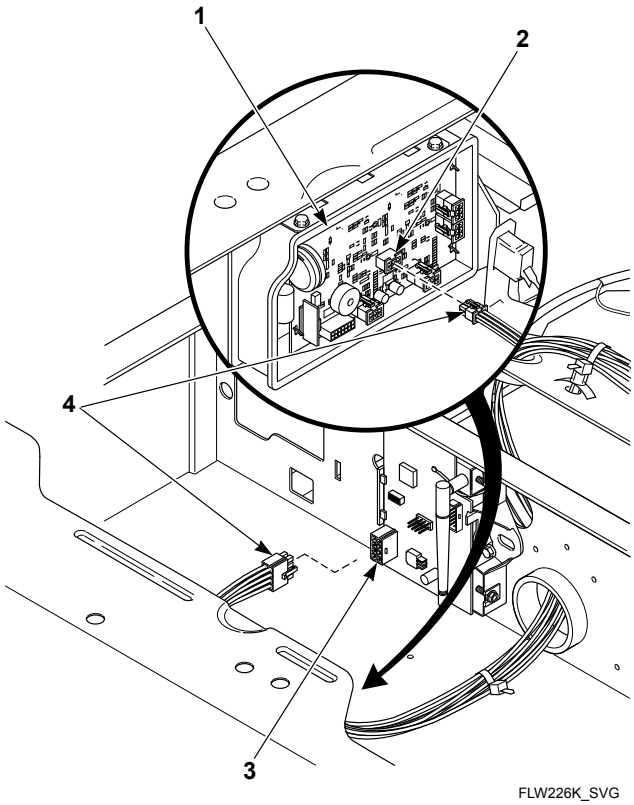
1. **IMPORTANT - Disconnect electrical power to machine.** Control will not recognize network board until power is cycled to machine.
2. Open access panel to gain access to the control area. Refer to Service Manual.
3. Adjust the compliance jumpers on the 204890 Wireless Network Control. Refer to *Compliance Jumper (H1)* section at the end of these instructions.
4. Install the F8674006 Wireless Network Harness between the network board "H3" refer to *Figure 6* , and the electronic control "H1". Refer to *Figure 7* .
5. Remove double sided tape backing from 204890 Wireless Network Control.
6. Place the tab on 204890 Wireless Network Control into slot in front bulkhead and secure opposite end with one D503661 Screw. Refer to *Figure 5* .

Washer Illustrated



1. 204890 Wireless Network Control
2. Slot
3. D503661 Screw

Figure 5



1. Electronic Control
2. "H1"
3. "H3"
4. F8674006 Wireless Network Harness

Figure 6

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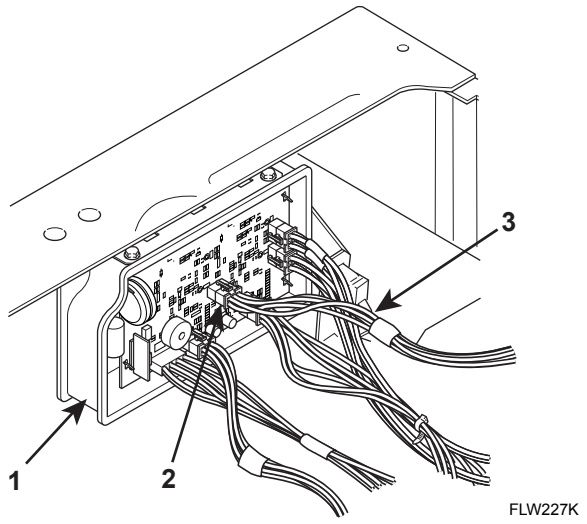


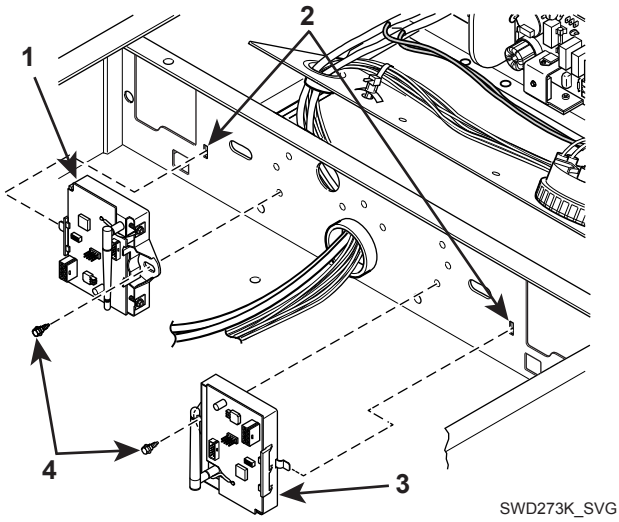
1. Electronic Control
2. "H1"
3. F8674006 Wireless Network Harness

Figure 7

7. Place F8673901 Network Option Diagram in control cabinet with existing diagrams.
8. Place XXXXXX Wireless Control Label in control cabinet be-hind control panel.
9. Fill out and place XXXXXX Conversion Label in control cabinet located behind control panel.
10. Close access panel.
11. Reconnect electrical power to the machine.

NOTE: The machine control MUST have been powered down prior to connecting the wireless control assembly in order for the control to recognize the board and to allow communication with it.

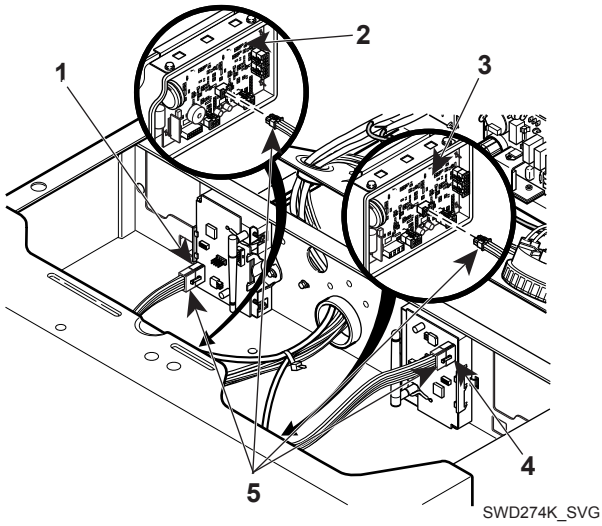
1. **IMPORTANT - Disconnect electrical power to machine.** Control will not recognize network board until power is cycled to machine.
2. Open access panel to gain access to the control area. Refer to Service Manual.
3. Adjust the compliance jumpers on the 204890 Wireless Network Control. Refer to *Compliance Jumper (H1)* section at the end of these instructions.
4. Remove double sided tape backing from 204890 Wireless Network Control.
5. Place tab on 204890 Wireless Network Control into slot in front bulkhead and secure opposite end with one D503661 Screw. Refer to *Figure 8* . Repeat for installing second network board.



1. 204890 Wireless Network Control (Washer)
2. Slot
3. 204890 Wireless Network Control (Dryer)
4. D503661 Screws

Figure 8

6. Install F8674006 Wireless Network Harness between network board "H3", refer to *Figure 9* , and electronic control "H1". Refer to *Figure 10* .



1. "H3"
2. Electronic Control (Washer)
3. Electronic Control (Dryer)
4. "H3"
5. F8674006 Wireless Network Harness

Figure 9

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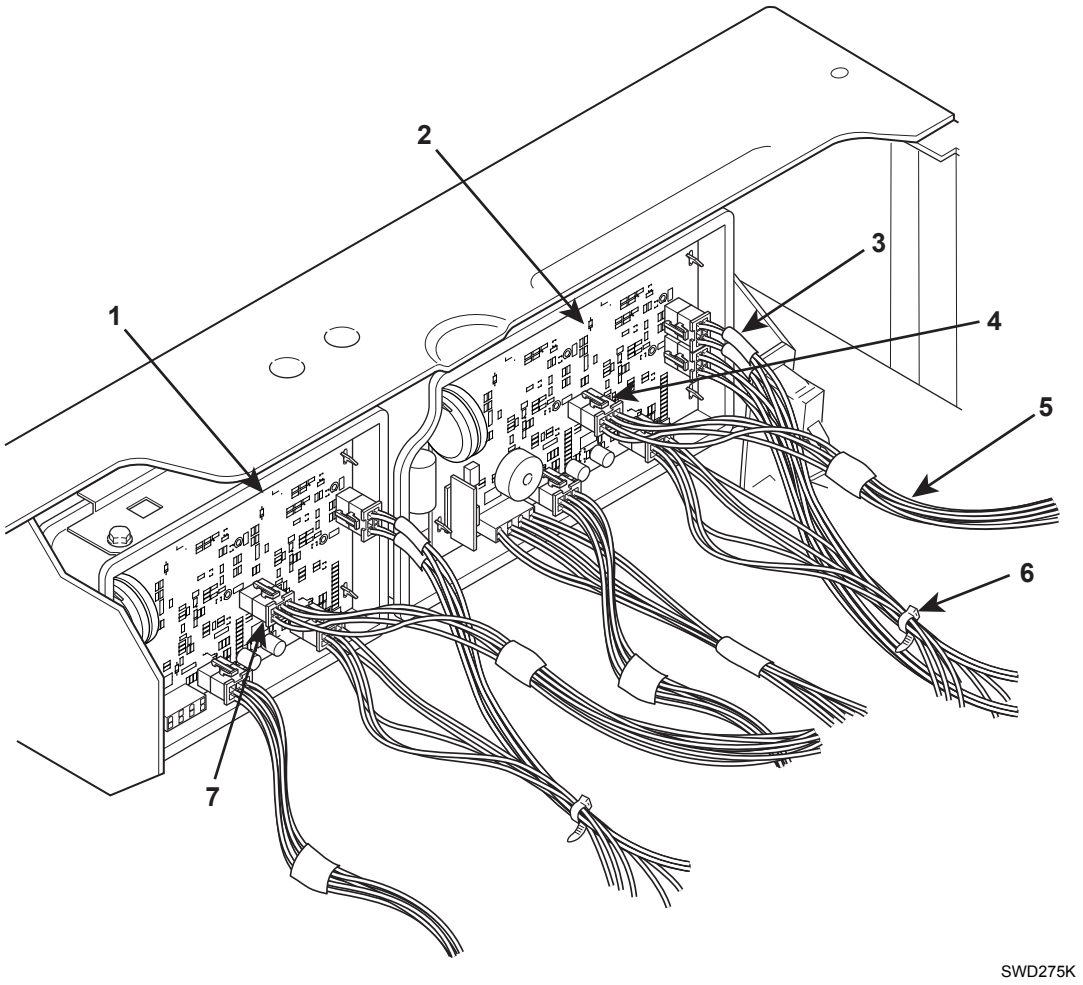
7. Add one 55881 Wire Tie to backside of electronic control as shown in *Figure 10* .
8. Place F8673901 Wiring Diagram in control cabinet with existing diagrams.
9. Place XXXXXX Wireless Control Label in the control cabinet.
10. Fill out and place XXXXXX Conversion Label in control cabinet located behind control panel.
11. Reconnect electrical power to the machine.

NOTE: The machine control MUST have been powered down prior to connecting the wireless control assembly in order for the control to recognize the board and to allow communication with it.

NOTE: Refer to network installation manual for machine connections to network.



1. Electronic Control (Dryer)
2. Electronic Control (Washer)
3. Tape
4. "H1" Connection (Washer)
5. F8674006 Wireless Network Harness
6. 55881 Wire Tie
7. "H1" Connection (Dryer)

Figure 10

Compliance Jumper (H1)

The compliance jumper is used to enforce limits set by local agencies on WiFi channel usage and output power. This jumper must be placed on the pins described in this section that correspond to the location where the Wireless Network Control will be operated. If the jumper is set incorrectly, the Wireless Network Control will be out of compliance with local agencies. If the jumper is not set at all, the Wireless Network Control will operate

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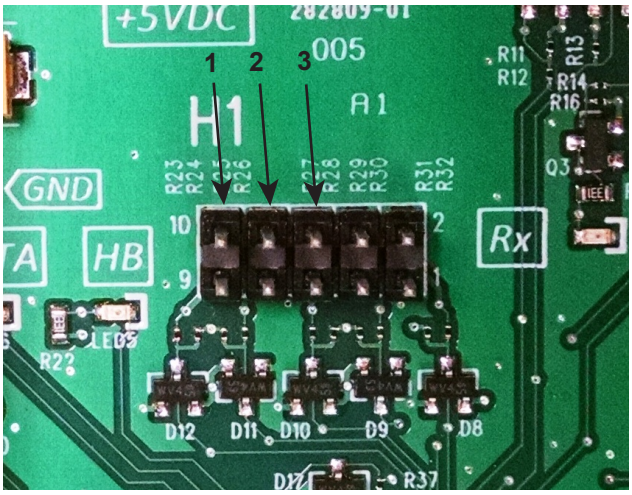
at a reduced power-level, which will reduce the performance of the Wireless Network Control.

NOTE: It is the responsibility of the installer to make sure that the Compliance Jumper is set to meet local standards. Incorrect settings will cause the board to be out of compliance and may lead to reduced range and loss of WiFi channels.

The jumper must be placed in one of three locations on header "H1". The three locations are shown in the table below and also in *Figure 11* .

Region	Hi Jumper Location	H1 Pins
US	Left Most Position	9 & 10
EU	Second From Left	7 & 8
JP	Third From Left	5, 7, 6



COM238K

1. US
2. EU Accepting
3. JP

Figure 11

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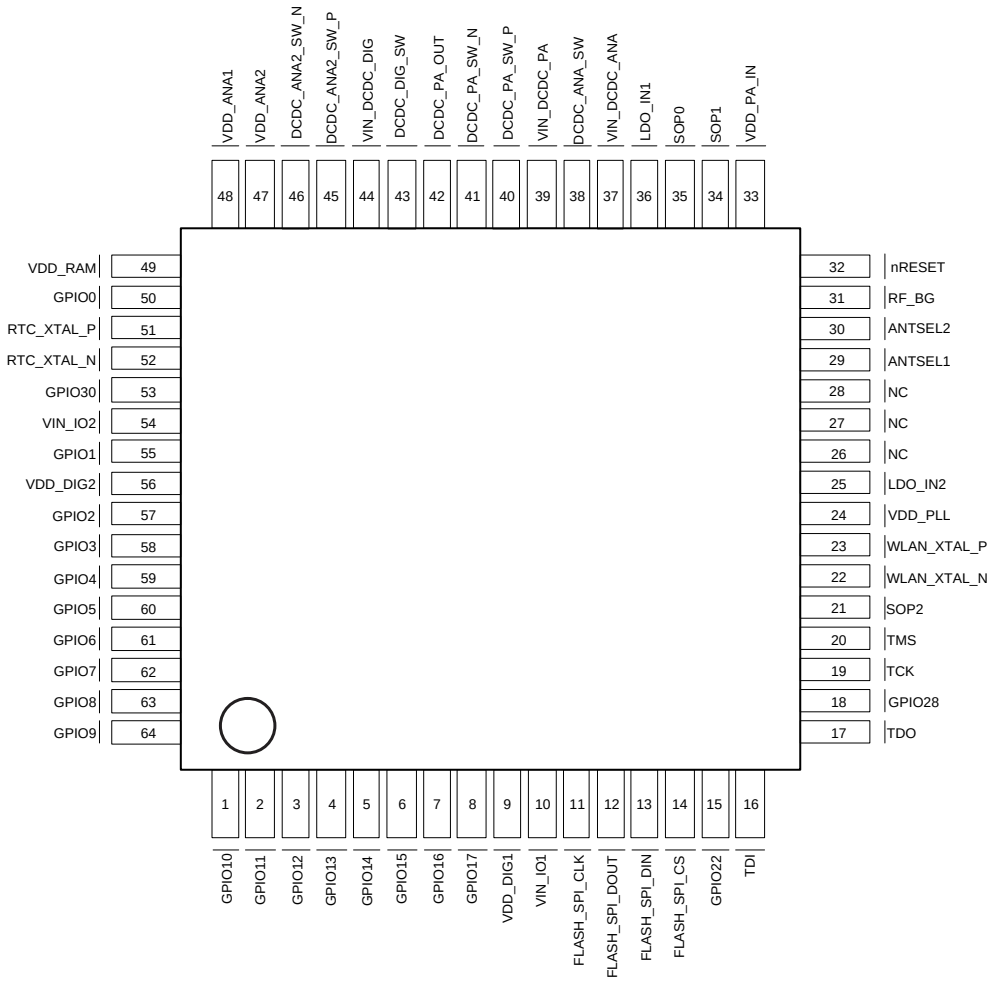
4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows pin assignments for the 64-pin VQFN package.



NC = No internal connection

Figure 4-1. VQFN 64-Pin Assignments Top View

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4.2 Pin Attributes and Pin Multiplexing

The device makes extensive use of pin multiplexing to accommodate the large number of peripheral functions in the smallest possible package. To achieve this configuration, pin multiplexing is controlled using a combination of hardware configuration (at device reset) and register control.

NOTE

TI highly recommends using *Pin Mux Tool* to obtain the desired pinout.

The board and software designers are responsible for the proper pin multiplexing configuration. Hardware does not ensure that the proper pin multiplexing options are selected for the peripherals or interface mode used.

Table 4-1 and Table 4-2 list the pin descriptions and attributes. Table 4-3 lists the signal descriptions. Table 4-4 presents an overall view of pin multiplexing. All pin multiplexing options are configurable using the pin mux registers.

The following special considerations apply:

- All I/Os support drive strengths of 2, 4, and 6 mA. The drive strength is individually configurable for each pin.
- All I/Os support 10-µA pullup and pulldown resistors.
- The V_{IO} and V_{BAT} supply must be tied together at all times.
- By default, all I/Os float in the Hibernate state. However, the default state can be changed by SW.
- All digital I/Os are nonfail-safe.

NOTE

If an external device drives a positive voltage to the signal pads and the CC3220x device is not powered, DC is drawn from the other device. If the drive strength of the external device is adequate, an unintentional wakeup and boot of the CC3220x device can occur. To prevent current draw, TI recommends any one of the following conditions:

- All devices interfaced to the CC3220x device must be powered from the same power rail as the chip.
- Use level shifters between the device and any external devices fed from other independent rails.
- The nRESET pin of the CC3220x device must be held low until the V_{BAT} supply to the device is driven and stable.
- All GPIO pins default to high impedance unless programmed by the MCU. The bootloader sets the TDI, TDO, TCK, TMS, and Flash_SPI pins to mode 1. All the other pins are left in the Hi-Z state.

Table 4-1. Pin Descriptions

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
1	GPIO10	I/O	General-purpose input or output	No	No	No
2	GPIO11	I/O	General-purpose input or output	Yes	No	No
3	GPIO12	I/O	General-purpose input or output	No	No	No
4	GPIO13	I/O	General-purpose input or output	Yes	No	No
5	GPIO14	I/O	General-purpose input or output	No	No	No
6	GPIO15	I/O	General-purpose input or output	No	No	No
7	GPIO16	I/O	General-purpose input or output	No	No	No
8	GPIO17	I/O	General-purpose input or output	Yes	No	No
9	VDD_DIG1	Power	Internal digital core voltage	N/A	N/A	N/A

Table 4-1. Pin Descriptions (continued)

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
10	VIN_IO1	Power	I/O power supply (same as battery voltage)	N/A	N/A	N/A
11	FLASH_SPI_CLK	O	Serial flash interface: SPI clock	N/A	N/A	N/A
12	FLASH_SPI_DOUT	O	Serial flash interface: SPI data out	N/A	N/A	N/A
13	FLASH_SPI_DIN	I	Serial flash interface: SPI data in	N/A	N/A	N/A
14	FLASH_SPI_CS	O	Serial flash interface: SPI chip select	N/A	N/A	N/A
15	GPIO22	I/O	General-purpose input or output	No	No	No
16	TDI	I/O	JTAG interface: data input	No	No	Muxed with JTAG TDI
17	TDO	I/O	JTAG interface: data output	Yes	No	Muxed with JTAG TDO
18	GPIO28	I/O	General-purpose input or output	No	No	No
19	TCK	I/O	JTAG/SWD interface: clock	No	No	Muxed with JTAG/ SWD-TCK
20	TMS	I/O	JTAG/SWD interface: mode select or SWDIO	No	No	Muxed with JTAG/ SWD-TMSC
21 (1)	SOP2	I	Configuration sense-on-power 2	No	No	No
22	WLAN_XTAL_N	Analog	40-MHz crystal. Pulldown if external TCXO is used.	N/A	N/A	N/A
23	WLAN_XTAL_P	Analog	40-MHz crystal or TCXO clock input	N/A	N/A	N/A
24	VDD_PLL	Power	Internal analog voltage	N/A	N/A	N/A
25	LDO_IN2	Power	Internal analog RF supply from analog DC/DC output	N/A	N/A	N/A
26	NC	—	No connect	N/A	N/A	N/A
27	NC	—	Reserved	N/A	N/A	N/A
28	NC	—	Reserved	N/A	N/A	N/A
29 (2)	ANTSEL1	O	Antenna selection control	No	User configuration not required (3)	No
30 (2)	ANTSEL2	O	Antenna selection control	No	User configuration not required (3)	No
31	RF_BG	RF	RF BG band: 2.4-GHz TX, RX	N/A	N/A	N/A
32	nRESET	I	Master chip reset input. Active low input.	N/A	N/A	N/A
33	VDD_PA_IN	Power	Internal RF power amplifier (PA) input from PA DC/DC output	N/A	N/A	N/A
34	SOP1	I	Configuration sense-on-power 1	N/A	N/A	N/A
35	SOP0	I	Configuration sense-on-power 0	N/A	N/A	N/A
36	LDO_IN1	Power	Internal Analog RF supply from analog DC/DC output	N/A	N/A	N/A
37	VIN_DCDC_ANA		Analog DC/DC supply input (same as battery voltage [V_{BAT}])	N/A	N/A	N/A
38	DCDC_ANA_SW	Power	Internal Analog DC/DC converter switching node	N/A	N/A	N/A

(1) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(2) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3220x device between two antennas. These pins must not be used for other functionalities.
(3) Device firmware automatically enables the digital path during ROM boot.

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Table 4-1. Pin Descriptions (continued)

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
39	VIN_DCDC_PA	Power	PA DC/DC converter input supply (same as battery voltage [V_{BAT}])	N/A	N/A	N/A
40	DCDC_PA_SW_P	Power	Internal PA DC/DC converter +ve switching node	N/A	N/A	N/A
41	DCDC_PA_SW_N	Power	Internal PA DC/DC converter –ve switching node	N/A	N/A	N/A
42	DCDC_PA_OUT	Power	Internal PA buck DC/DC converter output	N/A	N/A	N/A
43	DCDC_DIG_SW	Power	Internal Digital DC/DC converter switching node	N/A	N/A	N/A
44	VIN_DCDC_DIG	Power	Digital DC/DC converter supply input (same as battery voltage [V_{BAT}])	N/A	N/A	N/A
45 (4)	DCDC_ANA2_SW_P	I/O	Analog2 DC/DC converter +ve switching node	No	User configuration not required (3)	No
46	DCDC_ANA2_SW_N	Power	Internal Analog2 DC/DC converter –ve switching node	N/A	N/A	N/A
47	VDD_ANA2	Power	Internal Analog2 DC/DC output	N/A	N/A	N/A
48	VDD_ANA1	Power	Internal Analog1 power supply fed by analog2 DC/DC converter output	N/A	N/A	N/A
49	VDD_RAM	Power	Internal SRAM LDO output	N/A	N/A	N/A
50	GPIO0	I/O	General-purpose input or output	No	User configuration not required (3)	No
51	RTC_XTAL_P	Analog	32.768-kHz XTAL_P or external CMOS level clock input	N/A	N/A	N/A
52 (5)	RTC_XTAL_N	Analog	32.768-kHz XTAL_N	N/A	User configuration not required (3)(6)	No
53	GPIO30	I/O	General-purpose input or output	No	User configuration not required (3)	No
54	VIN_IO2	Power	device supply voltage (V_{BAT})	N/A	N/A	N/A
55	GPIO1	I/O	General-purpose input or output	No	No	No
56	VDD_DIG2	Power	internal digital core voltage	N/A	N/A	N/A
57 (7)	GPIO2	I/O	Analog input (up to 1.5-V) or general-purpose input or output	Yes	See (8)	No
58 (7)	GPIO3	I/O	Analog input (up to 1.5-V) or general-purpose input or output	No	See (8)	No
59 (7)	GPIO4	I/O	Analog input (up to 1.5-V) or general-purpose input or output	Yes	See (8)	No
60 (7)	GPIO5	I/O	Analog input (up to 1.5 V) or general-purpose input or output	No	See (8)	No
61	GPIO6	I/O	General-purpose input or output	No	No	No
62	GPIO7	I/O	General-purpose input or output	No	No	No
63	GPIO8	I/O	General-purpose input or output	No	No	No

(4) Pin 45 is used by an internal DC/DC converter (ANA2_DCDC). This pin will be available automatically if the serial flash is forced in the CC3220SF device. For the CC3220R and CC3220S devices, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.
(5) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for the RTC crystal in most applications. However, in some applications a 32.768-kHz square-wave clock might always be available onboard. When a 32.768-kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the device to automatically detect this configuration, a 100-kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.
(6) To use the digital functions, RTC_XTAL_N must be pulled high to the supply voltage using a 100-kΩ resistor.
(7) This pin is shared by the ADC inputs and digital I/O pad cells.
(8) Requires user configuration to enable the analog switch of the ADC channel (the switch is off by default.) The digital I/O is always connected and must be made Hi-Z before enabling the ADC switch.

Table 4-1. Pin Descriptions (continued)

PINS		TYPE	DESCRIPTION	SELECT AS WAKEUP SOURCE	CONFIGURE ADDITIONAL ANALOG MUX	MUXED WITH JTAG
NO.	NAME					
64	GPIO9	I/O	General-purpose input or output	No	No	No
GND_TAB		—	Thermal pad and electrical ground	N/A	N/A	N/A

Table 4-2. Pin Attributes

PIN NO.	SIGNAL NAME (1)	SIGNAL TYPE (2)	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS (3)	Hib (4)	nRESET = 0
1	GPIO10 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SCL		1	I/O (open drain)	Hi-Z, Pull, Drive		
	GT_PWM06		3	O	Hi-Z, Pull, Drive		
	UART1_TX		7	O	1		
	SDCARD_CLK		6	O	0		
	GT_CCP01		12	I	Hi-Z, Pull, Drive		
2	GPIO11 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		1	I/O (open drain)	Hi-Z, Pull, Drive		
	GT_PWM07		3	O	Hi-Z, Pull, Drive		
	pXCLK (XVCLK)		4	O	0		
	SDCARD_CMD		6	I/O (open drain)	Hi-Z, Pull, Drive		
	UART1_RX		7	I	Hi-Z, Pull, Drive		
	GT_CCP02		12	I	Hi-Z, Pull, Drive		
	McAFSX		13	O	Hi-Z, Pull, Drive		
3	GPIO12 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McACLK		3	O	Hi-Z, Pull, Drive		
	pVS (VSYNC)		4	I	Hi-Z, Pull, Drive		
	I2C_SCL		5	I/O (open drain)	Hi-Z, Pull, Drive		
	UART0_TX		7	O	1		
	GT_CCP03		12	I	Hi-Z, Pull, Drive		
4	GPIO13 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		5	I/O (open drain)			
	pHS (HSYNC)		4	I			
	UART0_RX		7	I			
	GT_CCP04		12	I			
5	GPIO14 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SCL		5	I/O (open drain)			
	GSPI_CLK		7	I/O			
	pDATA8 (CAM_D4)		4	I			
	GT_CCP05		12	I			

(1) Signals names with (PN) denote the default pin name.
(2) Signal Types: I = Input, O = Output, I/O = Input or Output.
(3) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.
(4) Hibernate mode: The I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

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Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
6	GPIO15 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	I2C_SDA		5	I/O (open drain)			
	GSPI_MISO		7	I/O			
	pDATA9 (CAM_D5)		4	I			
	GT_CCP06		13	I			
	SDCARD_DATA0		8	I/O			
7	GPIO16 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GSPI_MOSI		7	I/O	Hi-Z, Pull, Drive		
	pDATA10 (CAM_D6)		4	I	Hi-Z, Pull, Drive		
	UART1_TX		5	O	1		
	GT_CCP07		13	I	Hi-Z, Pull, Drive		
	SDCARD_CLK		8	O	0		
8	GPIO17 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART1_RX		5	I			
	GSPI_CS		7	I/O			
	pDATA11 (CAM_D7)		4	I			
	SDCARD_CMD		8	I/O			
9	VDD_DIG1 (PN)	—	N/A	N/A	N/A	N/A	N/A
10	VIN_IO1	—	N/A	N/A	N/A	N/A	N/A
11	FLASH_SPI_CLK	O	N/A	O	Hi-Z, Pull, Drive[5]	Hi-Z, Pull, Drive	Hi-Z
12	FLASH_SPI_DOUT	O	N/A	O	Hi-Z, Pull, Drive[5]	Hi-Z, Pull, Drive	Hi-Z
13	FLASH_SPI_DIN	I	N/A	I	Hi-Z, Pull, Drive[5]	Hi-Z	Hi-Z
14	FLASH_SPI_CS	O	N/A	O	1	Hi-Z, Pull, Drive	Hi-Z
15	GPIO22 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McAFSX	O	7	O			
	GT_CCP04	I	5	I			
16	TDI (PN)	I/O	1	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO23		0	I/O			
	UART1_TX		2	O	1		
	I2C_SCL		9	I/O (open drain)	Hi-Z, Pull, Drive		
17	TDO (PN)	I/O	1	O	Hi-Z, Pull, Drive	Driven high in SWD; driven low in 4-wire JTAG	Hi-Z
	GPIO24		0	I/O			
	PWM0		5	O			
	UART1_RX		2	I			
	I2C_SDA		9	I/O (open drain)			
	GT_CCP06		4	I			
	McAFSX		6	O			
18	GPIO28	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
19	TCK (PN)	I/O	1	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GT_PWM03		8	O			

(5) To minimize leakage in some serial flash vendors during LPDS, TI recommends that the user application always enables internal weak pulldown resistors on the FLASH_SPI_DIN, FLASH_SPI_DOUT, and FLASH_SPI_CLK pins.

Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
20	TMS (PN)	I/O	1	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO29		0				
21[6]	GPIO25	O	0	O	Hi-Z, Pull, Drive	Driven low	Hi-Z
	GT_PWM02		9	O	Hi-Z, Pull, Drive		
	McAFSX		2	O	Hi-Z, Pull, Drive		
	TCXO_EN		N/A (see [7])	O	0		
	SOP2 (PN)		N/A (see [8])	I	Hi-Z, Pull, Drive		
22	WLAN_XTAL_N	—	N/A (see [7])	N/A	N/A	N/A	N/A
23	WLAN_XTAL_P	—	N/A	N/A	N/A	N/A	N/A
24	VDD_PLL	—	N/A	N/A	N/A	N/A	N/A
25	LDO_IN2	—	N/A	N/A	N/A	N/A	N/A
26	NC	—	N/A	N/A	N/A	N/A	N/A
27	NC	—	N/A	N/A	N/A	N/A	N/A
28	NC	—	N/A	N/A	N/A	N/A	N/A
29[9]	ANTSEL1	O	0	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
30[9]	ANTSEL2	O	0	O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
31	RF_BG	—	N/A	N/A	N/A	N/A	N/A
32	nRESET	—	N/A	N/A	N/A	N/A	N/A
33	VDD_PA_IN	—	N/A	N/A	N/A	N/A	N/A
34	SOP1	—	N/A	N/A	N/A	N/A	N/A
35	SOP0	—	N/A	N/A	N/A	N/A	N/A
36	LDO_IN1	—	N/A	N/A	N/A	N/A	N/A
37	VIN_DCDC_ANA	—	N/A	N/A	N/A	N/A	N/A
38	DCDC_ANA_SW	—	N/A	N/A	N/A	N/A	N/A
39	VIN_DCDC_PA	—	N/A	N/A	N/A	N/A	N/A
40	DCDC_PA_SW_P	—	N/A	N/A	N/A	N/A	N/A
41	DCDC_PA_SW_N	—	N/A	N/A	N/A	N/A	N/A
42	DCDC_PA_OUT	—	N/A	N/A	N/A	N/A	N/A
43	DCDC_DIG_SW	—	N/A	N/A	N/A	N/A	N/A
44	VIN_DCDC_DIG	—	N/A	N/A	N/A	N/A	N/A

(6) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(7) For details on proper use, see Section 4.5.
(8) This pin is one of three that must have a passive pullup or pulldown resistor onboard to configure the device hardware power-up mode. For this reason, the pin must be output only when used for digital functions.
(9) This pin is reserved for WLAN antenna selection, controlling an external RF switch that multiplexes the RF pin of the CC3220x device between two antennas. These pins must not be used for other functionalities.

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Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
45[10]	GPIO31	I/O	0	I/O	Hi-Z	Hi-Z	Hi-Z
	UART0_RX		9	I			
	McAFSX		12	O			
	UART1_RX		2	I			
	McAXR0		6	I/O			
	GSPI_CLK		7	I/O			
	DCDC_ANA2_SW_P (PN)	—	N/A (see [7])	N/A	N/A	N/A	N/A
46	DCDC_ANA2_SW_N	—	N/A	N/A	N/A	N/A	N/A
47	VDD_ANA2	—	N/A	N/A	N/A	N/A	N/A
48	VDD_ANA1	—	N/A	N/A	N/A	N/A	N/A
49	VDD_RAM	—	N/A	N/A	N/A	N/A	N/A
50	GPIO0 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_CTS		12	I	Hi-Z, Pull, Drive		
	McAXR1		6	I/O	Hi-Z, Pull, Drive		
	GT_CCP00		7	I	Hi-Z, Pull, Drive		
	GSPI_CS		9	I/O	Hi-Z, Pull, Drive		
	UART1_RTS		10	O	1		
	UART0_RTS		3	O	1		
	McAXR0		4	I/O	Hi-Z, Pull, Drive		
51	RTC_XTAL_P	—	N/A	N/A	N/A	N/A	N/A
52[11]	RTC_XTAL_N (PN)	O	N/A	N/A	N/A	Hi-Z, Pull, Drive	Hi-Z
	GPIO32		0	O	Hi-Z, Pull, Drive		
	McACLK		2	O			
	McAXR0		4	O			
	UART0_RTS		6	O	1		
	GSPI_MOSI		8	O	Hi-Z, Pull, Drive		
53	GPIO30 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_TX		9	O	1		
	McACLK		2	O	Hi-Z, Pull, Drive		
	McAFSX		3	O			
	GT_CCP05		4	I			
	GSPI_MISO		7	I/O			
54	VIN_IO2	—	N/A	N/A	N/A	N/A	N/A
55	GPIO1 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_TX		3	O	1		
	pCLK (PIXCLK)		4	I	Hi-Z, Pull, Drive		
	UART1_TX		6	O	1		
	GT_CCP01		7	I	Hi-Z, Pull, Drive		
56	VDD_DIG2	—	N/A	N/A	N/A	N/A	N/A

(10) Pin 45 is used by an internal DC/DC (ANA2_DCDC). This pin will be available automatically if serial flash is forced in the CC3220SF device. For the CC3220R and CC3220S devices, pin 45 can be used as GPIO_31 if a supply is provided on pin 47.

(11) Pin 52 is used by the RTC crystal oscillator. These devices use automatic configuration sensing. Therefore, some board-level configuration is required to use pin 52 as a digital pad. Pin 52 is used for RTC crystal in most applications. However, in some applications a 32.768-kHz square-wave clock might always be available onboard. When a 32.768-kHz square-wave clock is available, the crystal can be removed to free pin 52 for digital functions. The external clock must then be applied at pin 51. For the chip to automatically detect this configuration, a 100-kΩ pullup resistor must be connected between pin 52 and the supply line. To prevent false detection, TI recommends using pin 52 for output-only functions.

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Table 4-2. Pin Attributes (continued)

PIN NO.	SIGNAL NAME[1]	SIGNAL TYPE[2]	PIN MUX ENCODING	SIGNAL DIRECTION	PAD STATES		
					LPDS[3]	Hib[4]	nRESET = 0
57[12]	ADC_CH0	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO2 (PN)		0	I/O			
	UART0_RX		3	I			
	UART1_RX		6	I			
	GT_CCP02		7	I			
58[12]	ADC_CH1	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO3 (PN)		0	I/O			
	UART1_TX		6	O	1		
	pDATA7 (CAM_D3)		4	I	Hi-Z, Pull, Drive		
59[12]	ADC_CH2	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO4 (PN)		0	I/O			
	UART1_RX		6	I			
	pDATA6 (CAM_D2)		4	I			
60[12]	ADC_CH3	Analog input (up to 1.5 V) or digital I/O	N/A (see [7])	I	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GPIO5 (PN)		0	I/O			
	pDATA5 (CAM_D1)		4	I			
	McAXR1		6	I/O			
	GT_CCP05		7	I			
61	GPIO6 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	UART0_RTS		5	O	1		
	pDATA4 (CAM_D0)		4	I	Hi-Z, Pull, Drive		
	UART1_CTS		3	I			
	UART0_CTS		6	I			
	GT_CCP06		7	I			
62	GPIO7 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	McACLKX		13	O			
	UART1_RTS		3	O	1		
	UART0_RTS		10	O			
	UART0_TX		11	O			
63	GPIO8 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	SDCARD_IRQ		6	I			
	McAFSX		7	O			
	GT_CCP06		12	I			
64	GPIO9 (PN)	I/O	0	I/O	Hi-Z, Pull, Drive	Hi-Z, Pull, Drive	Hi-Z
	GT_PWM05		3	O			
	SDCARD_DATA0		6	I/O			
	McAXR0		7	I/O			
	GT_CCP00		12	I			
GND_TAB		—	N/A	N/A	N/A	N/A	N/A

(12) This pin is shared by the ADC inputs and digital I/O pad cells.

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NOTE

The ADC inputs are tolerant up to 1.8 V (see Table 5-18 for more details about the usable range of the ADC). On the other hand, the digital pads can tolerate up to 3.6 V. Hence, take care to prevent accidental damage to the ADC inputs. TI recommends first disabling the output buffers of the digital I/Os corresponding to the desired ADC channel (that is, converted to Hi-Z state), and thereafter disabling the respective pass switches (S7 [Pin 57], S8 [Pin 58], S9 [Pin 59], and S10 [Pin 60]). For more information about drive strength and reset states for analog-digital multiplexed pins, see Section 4.5.

4.3 Signal Descriptions

Table 4-3. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
ADC	ADC_CH0	57	I/O	I	ADC channel 0 input (maximum of 1.5 V)
	ADC_CH1	58	I/O	I	ADC channel 1 input (maximum of 1.5 V)
	ADC_CH2	59	I/O	I	ADC channel 2 input (maximum of 1.5 V)
	ADC_CH3	60	I/O	I	ADC channel 3 input (maximum of 1.5 V)
Antenna selection	ANTSEL1	29	O	O	Antenna selection control 1
	ANTSEL2	30	O	O	Antenna selection control 2
Clock	TCX0_EN	21	O	O	Enable to optional external 40-MHz TCXO
	WLAN_XTAL_N	22	—	—	40-MHz crystal; pull down if external TCXO is used
	WLAN_XTAL_P	23	—	—	40-MHz crystal or TCXO clock input
	RTC_XTAL_P	51	—	—	Connect 32.768-kHz crystal or force external CMOS level clock
	RTC_XTAL_N	52	—	—	Connect 32.768-kHz crystal or connect 100-kΩ resistor to supply voltage
JTAG / SWD	TDI	16	I/O	I	JTAG TDI. Reset default pinout.
	TDO	17	I/O	O	JTAG TDO. Reset default pinout.
	TCK	19	I/O	I	JTAG/SWD TCK. Reset default pinout.
	TMS	20	I/O	I/O	JTAG/SWD TMS. Reset default pinout.
I^2C	I2C_SCL	1	I/O	I/O (open drain)	I^2C clock data
		3			
		5			
		16			
	I2C_SDA	2	I/O	I/O (open drain)	I^2C data
		4			
		6			
		17			

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Timers	GT_PWM06	1	I/O	O	Pulse-width modulated O/P
	GT_CCP01	1	I/O	I	Timer capture port
	GT_PWM07	2	I/O	O	Pulse-width modulated O/P
	GT_CCP02	2	I/O	I	Timer capture port
	GT_CCP03	3	I/O	I	
	GT_CCP04	4	I/O	I	
		15	I/O	I	
	GT_CCP05	5	I/O	I	
	GT_CCP06	6	I/O	I	
		17	I/O	I	
		61	I/O	I	
		63	I/O	I	
	GT_CCP07	7	I/O	I	
	PWM0	17	I/O	O	Pulse-width modulated output
	GT_PWM03	19	I/O	O	
	GT_PWM02	21	O	O	
	GT_CCP00	50	I/O	I	Timer capture port
		64	I/O	I	
	GT_CCP05	53	I/O	I	
	GT_CCP01	55	I/O	I	
	GT_CCP02	57	I/O	I	
	GT_CCP05	60	I	I	
	GT_PWM05	64	I/O	O	Pulse-width modulated output

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Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
GPIO	GPIO10	1	I/O	I/O	General-purpose input or output
	GPIO11	2	I/O	I/O	
	GPIO12	3	I/O	I/O	
	GPIO13	4	I/O	I/O	
	GPIO14	5	I/O	I/O	
	GPIO15	6	I/O	I/O	
	GPIO16	7	I/O	I/O	
	GPIO17	8	I/O	I/O	
	GPIO22	15	I/O	I/O	
	GPIO23	16	I/O	I/O	
	GPIO24	17	I/O	I/O	
	GPIO28	18	I/O	I/O	
	GPIO29	20	I/O	I/O	
	GPIO25	21	O	O	General-purpose output only
	GPIO31	45	I/O	I/O	General-purpose input or output
	GPIO0	50	I/O	I/O	
	GPIO32	52	I/O	O	General-purpose output only
	GPIO30	53	I/O	I/O	General-purpose input or output
	GPIO1	55	I/O	I/O	
	GPIO2	57	I/O	I/O	
	GPIO3	58	I/O	I/O	
	GPIO4	59	I/O	I/O	
	GPIO5	60	I/O	I/O	
	GPIO6	61	I/O	I/O	
	GPIO7	62	I/O	I/O	
	GPIO8	63	I/O	I/O	
	GPIO9	64	I/O	I/O	
McASP I^2S or PCM	McAFSX	2	I/O	O	I^2S audio port frame sync
		15			
		17			
		21			
		45			
		53			
		63			
	McACLK	3	I/O	O	I^2S audio port clock output
		52	O	O	
		53	I/O	O	
	McAXR1	50	I/O	I/O	I^2S audio port data 1 (RX and TX)
		60	I	I/O	
	McAXR0	45	I/O	I/O	I^2S audio port data 0 (RX and TX)
		50	I/O	I/O	
		52	O	O	I^2S audio port data (only output mode is supported on pin 52)
		64	I/O	I/O	I^2S audio port data (RX and TX)
	McACLKX	62	I/O	O	I^2S audio port clock

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
Multimedia card (MMC or SD)	SDCARD_CLK	1	I/O	O	SD card clock data
		7			
	SDCARD_CMD	2	I/O	I/O (open drain)	SD card command line
		8	I/O	I/O	
	SDCARD_DATA0	6	I/O	I/O	SD card data
		64			
	SDCARD_IRQ	63	I/O	I	Interrupt from SD card (future support)
Parallel interface (8-bit π)	pXCLK (XVCLK)	2	I/O	O	Free clock to parallel camera
	pVS (VSYNC)	3	I/O	I	Parallel camera vertical sync
	pHS (HSYNC)	4	I/O	I	Parallel camera horizontal sync
	pDATA8 (CAM_D4)	5	I/O	I	Parallel camera data bit 4
	pDATA9 (CAM_D5)	6	I/O	I	Parallel camera data bit 5
	pDATA10 (CAM_D6)	7	I/O	I	Parallel camera data bit 6
	pDATA11 (CAM_D7)	8	I/O	I	Parallel camera data bit 7
	pCLK (PIXCLK)	55	I/O	I	Pixel clock from parallel camera sensor
	pDATA7 (CAM_D3)	58	I/O	I	Parallel camera data bit 3
	pDATA6 (CAM_D2)	59	I/O	I	Parallel camera data bit 2
	pDATA5 (CAM_D1)	60	I	I	Parallel camera data bit 1
	pDATA4 (CAM_D0)	61	I/O	I	Parallel camera data bit 0
Power	VDD_DIG1	9	—	—	Internal digital core voltage
	VIN_IO1	10	—	—	Device supply voltage (V_{BAT})
	VDD_PLL	24	—	—	Internal analog voltage
	LDO_IN2	25	—	—	Internal analog RF supply from analog DC/DC output
	VDD_PA_IN	33	—	—	Internal PA supply voltage from PA DC/DC output
	LDO_IN1	36	—	—	Internal analog RF supply from analog DC/DC output
	VIN_DCDC_ANA	37	—	—	Analog DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA_SW	38	—	—	Internal analog DC/DC switching node
	VIN_DCDC_PA	39	—	—	PA DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_PA_SW_P	40	—	—	Internal PA DC/DC switching node
	DCDC_PA_SW_N	41	—	—	
	DCDC_PA_OUT	42	—	—	Internal PA buck converter output
	DCDC_DIG_SW	43	—	—	Internal digital DC/DC switching node
	VIN_DCDC_DIG	44	—	—	Digital DC/DC input (connected to device input supply [V_{BAT}])
	DCDC_ANA2_SW_P	45	—	—	Analog to DC/DC converter +ve switching node
	DCDC_ANA2_SW_N	46	—	—	Internal analog to DC/DC converter –ve switching node
	VDD_ANA2	47	—	—	Internal analog to DC/DC output
	VDD_ANA1	48	—	—	Internal analog supply fed by ANA2 DC/DC output
	VDD_RAM	49	—	—	Internal SRAM LDO output
	VIN_IO2	54	—	—	Device supply voltage (V_{BAT})
	VDD_DIG2	56	—	—	Internal digital core voltage

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Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NO.	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
SPI	GSPI_CLK	5	I/O	I/O	General SPI clock
		45	I/O	I/O	
	GSPI_MISO	6	I/O	I/O	General SPI MISO
		53	I/O	I/O	
	GSPI_CS	8	I/O	I/O	General SPI chip select
		50	I/O	I/O	
	GSPI_MOSI	7	I/O	I/O	General SPI MOSI
		52	O	O	
FLASH SPI	FLASH_SPI_CLK	11	O	O	Clock to SPI serial flash (fixed default)
	FLASH_SPI_DOUT	12	O	O	Data to SPI serial flash (fixed default)
	FLASH_SPI_DIN	13	I	I	Data from SPI serial flash (fixed default)
	FLASH_SPI_CS	14	O	O	Device select to SPI serial flash (fixed default)
UART	UART1_TX	1	I/O	O	UART1 TX data
		7	I/O	O	
		16	I/O	O	
		55	I/O	O	
		58	I/O	O	
	UART1_RX	2	I/O	I	UART1 RX data
		8	I/O	I	
		17	I/O	I	
		45	I/O	I	
		57	I/O	I	
		59	I/O	I	
	UART1_RTS	50	I/O	O	UART1 request-to-send (active low)
		62	I/O	O	
	UART1_CTS	61	I/O	I	UART1 clear-to-send (active low)
	UART0_TX	3	I/O	O	UART0 TX data
		53	I/O	O	
		55	I/O	O	
		62	I/O	O	
	UART0_RX	4	I/O	I	UART0 RX data
		45	I/O	I	
		57	I/O	I	
	UART0_CTS	50	I/O	I	UART0 clear-to-send input (active low)
		61	I/O	I	
	UART0_RTS	50	I/O	O	UART0 request-to-send (active low)
		52	O	O	
		61	I/O	O	
		62	I/O	O	
Sense-on-Power	SOP2	21 (1)	O	I	Sense-on-power 2
	SOP1	34	—	—	Configuration sense-on-power 1
	SOP0	35	—	—	Configuration sense-on-power 0
Reset	nRESET	32	—	—	Global master device reset (active low)
RF	RF_BG	31	—	—	WLAN analog RF 802.11 b/g bands

(1) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.

4.4 Pin Multiplexing

Table 4-4. Pin Multiplexing

REGISTER ADDRESS	REGISTER NAME	PIN	ANALOG OR SPECIAL FUNCTION	DIGITAL FUNCTION (XXX FIELD ENCODING)[1]													
			JTAG	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0x4402 E0C8	GPIO_PAD_CONFIG_10	1	—	GPIO10	I2C_SCL	—	GT_PWM06	—	—	SDCARD_ CLK	UART1_TX	—	—	—	—	GT_CCP01	—
0x4402 E0CC	GPIO_PAD_CONFIG_11	2	—	GPIO11	I2C_SDA	—	GT_PWM07	pXCLK (XVCLK)	—	SDCARD_ CMD	UART1_RX	—	—	—	—	GT_CCP02	MCAFSX
0x4402 E0D0	GPIO_PAD_CONFIG_12	3	—	GPIO12	—	—	McACLK	pVS (VSYNC)	I2C_SCL	—	UART0_TX	—	—	—	—	GT_CCP03	—
0x4402 E0D4	GPIO_PAD_CONFIG_13	4	—	GPIO13	—	—	—	pHS (HSYNC)	I2C_SDA	—	UART0_RX	—	—	—	—	GT_CCP04	—
0x4402 E0D8	GPIO_PAD_CONFIG_14	5	—	GPIO14	—	—	—	pDATA8 (CAM_D4)	I2C_SCL	—	GSPI_CLK	—	—	—	—	GT_CCP05	—
0x4402 E0DC	GPIO_PAD_CONFIG_15	6	—	GPIO15	—	—	—	pDATA9 (CAM_D5)	I2C_SDA	—	GSPI_ MISO	SDCARD_ DATA0	—	—	—	—	GT_CCP06
0x4402 E0E0	GPIO_PAD_CONFIG_16	7	—	GPIO16	—	—	—	pDATA10 (CAM_D6)	UART1_TX	—	GSPI_ MOSI	SDCARD_ CLK	—	—	—	—	GT_CCP07
0x4402 E0E4	GPIO_PAD_CONFIG_17	8	—	GPIO17	—	—	—	pDATA11 (CAM_D7)	UART1_RX	—	GSPI_CS	SDCARD_ CMD	—	—	—	—	—
0x4402 E0F8	GPIO_PAD_CONFIG_22	15	—	GPIO22	—	—	—	—	GT_CCP04	—	McAFSX	—	—	—	—	—	—
0x4402 E0FC	GPIO_PAD_CONFIG_23	16	Muxed with JTAG	GPIO23	TDI	UART1_TX	—	—	—	—	—	—	I2C_SCL	—	—	—	—
0x4402 E100	GPIO_PAD_CONFIG_24	17	Muxed with JTAG TDO	GPIO24	TDO	UART1_RX	—	GT_CCP06	PWM0	McAFSX	—	—	I2C_SDA	—	—	—	—
0x4402 E140	GPIO_PAD_CONFIG_40	18	—	GPIO28	—	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E110	GPIO_PAD_CONFIG_28	19	Muxed with JTAG or SWD and TCK	—	TCK	—	—	—	—	—	—	GT_ PWM03	—	—	—	—	—
0x4402 E114	GPIO_PAD_CONFIG_29	20	Muxed with JTAG or SWD and TMSC	GPIO29	TMS	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E104	GPIO_PAD_CONFIG_25	21[2]	—	GPIO25	—	McAFSX	—	—	—	—	—	—	GT_ PWM02	—	—	—	—
0x4402 E108	GPIO_PAD_CONFIG_26	29	—	ANTSEL1[3]	—	—	—	—	—	—	—	—	—	—	—	—	—
0x4402 E10C	GPIO_PAD_CONFIG_27	30	—	ANTSEL2[3]	—	—	—	—	—	—	—	—	—	—	—	—	—

(1) Pin mux encodings with (RD) denote the default encoding after reset release.
(2) This pin has dual functions: as a SOP[2] (device operation mode), and as an external TCXO enable. As a TXCO enable, the pin is an output on power up and driven logic high. During hibernate low-power mode, the pin is in a Hi-Z state but is pulled down for SOP mode to disable TCXO. Because of the SOP functionality, the pin must be used as an output only.
(3) LPDS state: Unused I/Os are in a Hi-Z state. Software may program the I/Os to be input with pull or drive (regardless of active pin configuration), according to the need.

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Table 4-4. Pin Multiplexing (continued)

REGISTER ADDRESS	REGISTER NAME	PIN	ANALOG OR SPECIAL FUNCTION	DIGITAL FUNCTION (XXX FIELD ENCODING)[1]													
			JTAG	0	1	2	3	4	5	6	7	8	9	10	11	12	13
0x4402 E11C	GPIO_PAD_CONFIG_31	45	—	GPIO31	—	UART1_RX	—	—	—	McAXR0	GSPI_CLK	—	UART0_RX	—	—	McAFSX	—
0x4402 E0A0	GPIO_PAD_CONFIG_0	50	—	GPIO0	—	—	UART0_ RTS	McAXR0	—	McAXR1	GT_CCP00	—	GSPI_CS	UART1_ RTS	—	UART0_ CTS	—
0x4402 E120	GPIO_PAD_CONFIG_32	52	—	GPIO32	—	McACLK	—	McAXR0	—	UART0 _ RTS	—	GSPI_ MOSI	—	—	—	—	—
0x4402 E118	GPIO_PAD_CONFIG_30	53	—	GPIO30	—	McACLK	McAFSX	GT_CCP05	—	—	GSPI_ MISO	—	UART0_TX	—	—	—	—
0x4402 E0A4	GPIO_PAD_CONFIG_1	55	—	GPIO1	—	—	UART0_TX	pCLK (PIXCLK)	—	UART1_TX	GT_CCP01	—	—	—	—	—	—
0x4402 E0A8	GPIO_PAD_CONFIG_2	57	—	GPIO2	—	—	UART0_RX	—	—	UART1_RX	GT_CCP02	—	—	—	—	—	—
0x4402 E0AC	GPIO_PAD_CONFIG_3	58	—	GPIO3	—	—	—	pDATA7 (CAM_D3)	—	UART1_TX	—	—	—	—	—	—	—
0x4402 E0B0	GPIO_PAD_CONFIG_4	59	—	GPIO4	—	—	—	pDATA6 (CAM_D2)	—	UART1_RX	—	—	—	—	—	—	—
0x4402 E0B4	GPIO_PAD_CONFIG_5	60	—	GPIO5	—	—	—	pDATA5 (CAM_D1)	—	McAXR1	GT_CCP05	—	—	—	—	—	—
0x4402 E0B8	GPIO_PAD_CONFIG_6	61	—	GPIO6	—	—	UART1_ CTS	pDATA4 (CAM_D0)	UART0_ RTS	UART0_ CTS	GT_CCP06	—	—	—	—	—	—
0x4402 E0BC	GPIO_PAD_CONFIG_7	62	—	GPIO7	—	—	UART1_ RTS	—	—	—	—	—	—	UART0_ RTS	UART0_TX	—	McACLKX
0x4402 E0C0	GPIO_PAD_CONFIG_8	63	—	GPIO8	—	—	—	—	—	SDCARD_ IRQ	McAFSX	—	—	—	—	GT_CCP06	—
0x4402 E0C4	GPIO_PAD_CONFIG_9	64	—	GPIO9	—	—	GT_PWM05	—	—	SDCARD_ DATA0	McAXR0	—	—	—	—	GT_CCP00	—

5 Specifications

All measurements are referenced at the device pins, unless otherwise indicated. All specifications are over process and voltage, unless otherwise indicated.

5.1 Absolute Maximum Ratings

All measurements are referenced at the device pins unless otherwise indicated. All specifications are over process, voltage, and operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{BAT} and V_{IO}	Pins: 37, 39, 44	–0.5	3.8	V
V_{IO} – V_{BAT} (differential)	Pins: 10, 54		V_{BAT} and V_{IO} should be tied together	V
Digital inputs		–0.5	V_{IO} + 0.5	V
RF pins		–0.5	2.1	V
Analog pins, crystal	Pins: 22, 23, 51, 52	–0.5	2.1	V
Operating temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–55	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Power-On Hours (POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

OPERATING CONDITION	POWER-ON HOURS [POH] (hours)
T_A up to 85°C(1)	87,600

(1) The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

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5.6 Current Consumption Summary (CC3220SF)

T_A = 25°C, V_{BAT} = 3.6 V

PARAMETER		TEST CONDITIONS(1) (2)			MIN	TYP	MAX	UNIT
MCU ACTIVE	NWP ACTIVE	TX	1 DSSS	TX power level = maximum		286		mA
				TX power level = maximum – 4		202		
			6 OFDM	TX power level = maximum		255		
				TX power level = maximum – 4		192		
			54 OFDM	TX power level = maximum		232		
				TX power level = maximum – 4		174		
		RX	1 DSSS			74		
			54 OFDM			74		
	NWP idle connected(3)					25.2		
MCU SLEEP	NWP ACTIVE	TX	1 DSSS	TX power level = maximum		282		mA
				TX power level = maximum – 4		198		
			6 OFDM	TX power level = maximum		251		
				TX power level = maximum – 4		188		
			54 OFDM	TX power level = maximum		228		
				TX power level = maximum – 4		170		
		RX	1 DSSS			70		
			54 OFDM			70		
	NWP idle connected(3)					21.2		
MCU LPDS	NWP active	TX	1 DSSS	TX power level = 0		266		mA
				TX power level = 4		184		
			6 OFDM	TX power level = 0		242		
				TX power level = 4		176		
			54 OFDM	TX power level = 0		217		
				TX power level = 4		154		
		RX	1 DSSS			53		
			54 OFDM			53		
	NWP LPDS(4)		120 µA at 64KB 135 µA at 256KB			135		µA
	NWP idle connected(3)					710		
MCU SHUTDOWN	MCU shutdown					1		
MCU HIBERNATE	MCU hibernate					4.5		
Peak calibration current(5)		V_{BAT} = 3.6 V				420		mA
		V_{BAT} = 3.3 V				450		
		V_{BAT} = 2.1 V				670		
		V_{BAT} = 1.85 V				700		

(1) TX power level = 0 implies maximum power (see Figure 5-1, Figure 5-2, and Figure 5-3). TX power level = 4 implies output power backed off approximately 4 dB.
(2) The CC3220x system is a constant power-source system. The active current numbers scale based on the V_{BAT} voltage supplied.
(3) DTIM = 1
(4) LPDS current does not include the external serial flash. The LPDS number of reported is with retention of 256KB of MCU SRAM. The CC3220x device can be configured to retain 0KB, 64KB, 128KB, 192KB, or 256KB of SRAM in LPDS. Each 64-KB block of MCU retained SRAM increases LPDS current by 4 µA.
(5) The complete calibration can take up to 17 mJ of energy from the battery over a period of 24 ms. Calibration is performed sparingly, typically when coming out of HIBERNATE and only if temperature has changed by more than 20°C. The calibration event can be controlled by a configuration file in the serial Flash..

Federal Communications Commission (FCC) Interference Statement

The modular transmitter is **only** FCC authorized for the specific rule part (FCC Part15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part15 of the FCC Rules.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generate, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

OEM/Host integrator is responsible for complying with the instructions and requirements for each transmitter they choose to integrate into a host product.

RF exposure warning

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This product may not be collocated or operated in conjunction with any other antenna or transmitter. This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20cm from all persons and must not be collocated or operating in conjunction with any other antenna or transmitter. Additional text needed for the host product manufacturer to provide to end users in their end-product manuals.

Industry Canada (IC)

CAN ICES-3 (B)/NMB-3(B)

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

Cetappareilestconforme à la norme RSS d'Industrie Canada. Son fonctionnementestsujet aux deux conditions suivantes:

(1) ledispositif ne doit pas produire de brouillagepréjudiciable, et

(2) cedispositifdoit accepter tout brouillagereçu, y compris un brouillage susceptible de provoquer un fonctionnementindésirable.

IMPORTANT NOTE:

Radiation Exposure Statement:

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

Déclarationd'exposition aux radiations:

Cetéquipementestconforme aux limitesd'exposition aux rayonnements IC établies pour unenvironnement non contrôlé. Cetéquipementdoitêtreinstalléetutilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

OEM Integration Instructions：

This device is intended only for OEM integrators under the following conditions：

(1). This module limit can be used to install in the host below.
Product name: Wireless Network Control Host
model: Wireless Network Control

(2). The antenna(s) used for this transmitter must be installed to the provided separation distance of at least 20cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

(3). The module shall be only used with the integral antenna(s) that has been originally tested and certified with this module.
As long as 3 conditions above are met, further transmitter test will not be required.
However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirement with this module installed (for example, digital device emission, PC peripheral requirements, etc.)

IMPORTANT NOTE：

In the event that these conditions cannot be met (for example certain laptop configuration or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these and circumstance, the OEM integrator will be responsible for re-evaluating. The end product (including the transmitter) and obtaining a separate FCC authorization. The final end product must be labeled in a visible area with the following:
"**Contains Transmitter Module FCC ID: 2ANOT-204890** or **Contains FCC ID: 2ANOT-204890**".
Antenna Specification:

Antenna Type	Manufacturer	Frequency Range (MHz)	Maximum Peak Antenna Gain(dBi)
Dipole Antenna	Pulse	2400 - 2500	2.0

Note: The device didn't support beam-forming technology and Cyclic Delay Diversity (CDD) technology, and the transmit signals are uncorrected, so no add array gain to the band power and band PSD.

IMPORTANT NOTE：

This Wireless Module (IC: 23166-204890) has been approved by Industry Canada to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

The Host Marketing Name(HMN) must be displayed (according to e-labelling requirements) or indicated at any location on the exterior of the host product or product packaging or product literature, which shall be available with the host product or online.
The host product shall be properly labelled to identify the modules within the host product. The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labelled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows: **Contains IC: 23166-204890.**
Antenna Specification:

Antenna Type	Manufacturer	Frequency Range (MHz)	Maximum Peak Antenna Gain(dBi)
Dipole Antenna	Pulse	2400 - 2500	2.0

Note: The device didn’t support beam-forming technology and Cyclic Delay Diversity (CDD) technology, and the transmit signals are uncorrected, so no add array gain to the band power and band PSD.