

nRF9151

Product Sheet

v1.1

nRF9151 features

Features

Microcontroller

- Arm® Cortex® -M33
 - 247 EEMBC CoreMark® score running from flash memory
 - Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace macrocell (ITM)
 - Serial wire debug (SWD)
 - Trace port
- 1 MB flash
- 256 KB low leakage RAM
- Arm TrustZone®
- Arm CryptoCell™ 310
- Up to four SPI controller/targets with EasyDMA
- Up to four I²C compatible two-wire controller/targets with EasyDMA
- Up to four UARTs (CTS/RTS) with EasyDMA
- I²S with EasyDMA
- Digital microphone interface (PDM) with EasyDMA
- Four pulse width modulator (PWM) units with EasyDMA
- 12-bit, 200 ksp/s ADC with EasyDMA - eight configurable channels with programmable gain
- Three 32-bit timer with counter mode
- Two real-time counter (RTC)
- Programmable peripheral interconnect (PPI)
- 32 general purpose I/O pins
- Single supply voltage from 3.0 V – 5.5 V
- Integrated clock sources
- LGA package 12.1x11.1x1.2 mm

LTE modem

- Transceiver and baseband
- 3GPP LTE release 14 Cat-M1 compliant
- 3GPP LTE release 14 Cat-NB1 and Cat-NB2 compliant
- 3GPP LTE release 17 IoT NTN compliant
- GPS receiver
 - GPS L1 C/A supported
 - QZSS L1 C/A supported
- RF transceiver for global coverage
 - Power Class 3 up to 23 dBm output power
 - Power Class 5 up to 20 dBm output power
 - -108 dBm sensitivity (Cat-M1) for low band, -107 dBm for mid band
 - Single 50 Ω antenna interface
- LTE band support in hardware
 - Cat-M1 – B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B85, B106
 - Cat-NB1/NB2 – B1, B2, B3, B4, B5, B8, B12, B13, B17, B19, B20, B25, B26, B28, B65, B66, B85, B106
 - IoT NTN – B23, B249, B252, B255, B256
- Supports SIM and eSIM with an ETSI TS 102 221 compatible UICC interface
- Power saving features include DRX, eDRX, PSM
- IP v4/v6 stack
- Secure socket (TLS/DTLS) API

DECT NR+

- Maximum transmission power 21 dBm (Class II) on bands 1, 2, 9, 22
- Maximum transmission power 19 dBm (Class III) on band 4

Current consumption @ 3.7 V

- LTE power saving mode (PSM) floor current – 2.7 µA
- eDRX @ 81.92s – 18 µA in Cat-M1, 32 µA in Cat-NB1 (UICC included)

Applications:

- Sensor networks
- Logistics and asset tracking
- Smart energy
- Smart building automation
- Smart agriculture
- Industrial
- Retail and monitor devices
- Medical devices
- Wearables

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1 Revision history

Date	Version	Description
July 2025	1.1	The following content has been added or updated: • Regulatory information on page 39 – ISED rules for RSS 102, RSS 133, and RSS 170
July 2024	1.0	First release

2 About this document

This document is organized into chapters that are based on the modules and peripherals available in the IC.

2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 1.0. This document contains target specifications for product development.
Product Specification (PS)	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

2.2 Peripheral chapters

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the Arm Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

The chapters describing peripherals may include the following information:

- A detailed functional description of the peripheral.
- The register configuration for the peripheral.
- The electrical specification tables, containing performance data which apply for the operating conditions described in [Operating conditions](#) on page 36.

2.2.2 Peripheral instantiation

The peripherals have a set of security capabilities listed in the instantiation tables.

The following table describes the abbreviations used.

Abbreviation	Description
NS	Trustzone/security attribute is Non-secure - The peripheral is always accessible as a Non-secure peripheral.
S	Trustzone/security attribute is Secure - The peripheral is always accessible as a Secure peripheral.
US	Trustzone Map is user selectable - The Trustzone/security attribute of the peripheral is configurable.
HF	Trustzone Map is Hardware Fixed - The Trustzone/security attribute of the peripheral cannot be changed.
NA	Not Applicable - Peripheral has no DMA capability.
NSA	NoSeparateAttribute - Peripheral with DMA and DMA transfer has the same security attribute as assigned to the peripheral.
SA	SeparateAttribute - Peripheral with DMA and DMA transfers can have a different security attribute than the one assigned to the peripheral.

Table 2: Instantiation table abbreviations

The Secure mapping column in the peripheral instantiation table defines configuration capabilities for the Arm TrustZone for Armv8-M secure attribute. The DMA security column describes the DMA capabilities of the peripheral.

The instantiation table has the following columns:

- Instance Column - Indicates the peripheral instance name followed by optional Trustzone attribute. A corresponding address is listed in Base address column indicating the base address for Secure and Non-secure Trustzone attribute. This optional Trustzone attribute is separated by a colon (:).
- Trustzone Column - This has 3 sub-columns indicating the Trustzone map, Trustzone attribute and DMA capability. The options are as listed in [Instantiation table abbreviations](#) on page 7.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as 0 to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a 0x prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.

- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.3.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

Access	Description	Hardware behavior
RO	Read-only	Field can only be read. A write will be ignored.
WO	Write-only	Field can only be written. A read will return an undefined value.
RW	Read-write	Field can be read and written multiple times.
W1	Write-once	Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value.
RW1	Read-write-once	Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.
W1C	Write 1 to clear	Field can be read multiple times. A one clears (set to zero) the corresponding bit in the register. Bits set to zero are ignored.
W1S	Write 1 to set	Field can be read multiple times. A one sets the corresponding bit in the register. Bits set to zero are ignored.

Table 3: Register field permission schemes

2.4 Registers

Register overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				D D D D								C C C								B								A							
Reset 0x00050002				0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0																															
ID	R/W	Field	Value ID	Value		Description																													
-A	RW	FIELD0				Example of a read-write field with several enumerated values																													
			Disabled	0	The example feature is disabled																														
			NormalMode	1	The example feature is enabled in normal mode																														
			ExtendedMode	2	The example feature is enabled along with extra functionality																														
B	RW	FIELD1				Example of a deprecated read-write field																													
					This field is deprecated.																														
			Disabled	0	The override feature is disabled																														
			Enabled	1	The override feature is enabled																														
C	RW	FIELD2				Example of a read-write field with a valid range of values																													
			ValidRange	[2..7]	Example of allowed values for this field																														
D	RW	FIELD3				Example of a read-write field with no restriction on the values																													

3 Product overview

The nRF9151 System-in-Package (SiP) is a low-power Internet of Things (IoT) solution integrating an Arm Cortex-M33 processor with advanced security features, a range of peripherals and a Low-Power Wide-Area (LPWA) network processor. The LPWA network processor can operate as a 5G DECT NR+ (NR+) device, independent of cellular network provider or as an LTE modem compliant with 3GPP LTE release 14 Cat-M1 and Cat-NB1/NB2 standards.

The LPWA network processor integrates a flexible transceiver with frequency range 700 MHz to 2200 MHz, through a single 50 Ω antenna pin and a baseband processor. NR+ or LTE operation is supported depending on which network protocol firmware the customer installs on the LPWA network processor of the nRF9151. Nordic Semiconductor provides firmware to support NR+ or LTE, layers L1-L3 and upper IP layers, providing a secure socket API to the application.

The nRF9151 LPWA network processor also integrate a GPS receiver, enabling local positioning support when supported by the installed firmware.

The Arm Cortex-M33 processor is exclusively for the user application, with 1 MB of flash and 256 kB of RAM dedicated for this. The M33 application processor shares the power, clock, and peripheral architecture with Nordic Semiconductor nRF5 Series of PAN/LAN SoCs, ensuring minimal porting efforts.

The peripheral set offers a variety of analog and digital functionality enabling single-chip implementation of a wide range of IoT applications. Arm TrustZone technology, CryptoCell 310 and supporting blocks for system protection and key management, are embedded to enable advanced security needed for IoT applications.

3.1 Block diagram

The block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

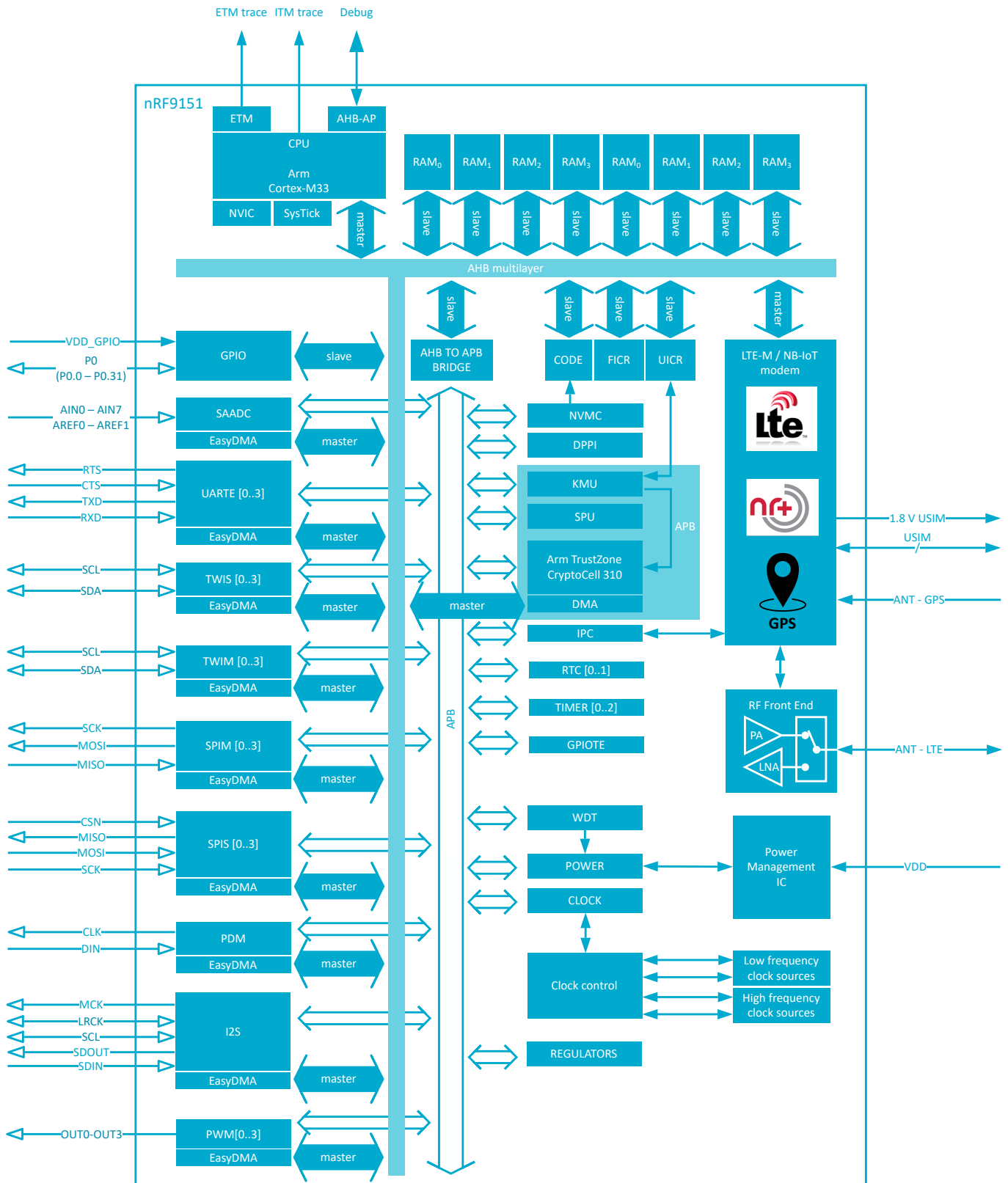


Figure 1: Block diagram

3.2 Peripheral interface

Peripherals are controlled by the CPU through configuration registers, as well as task and event registers. Task registers are inputs, enabling the CPU and other peripherals to initiate a functionality. Event registers

are outputs, enabling a peripheral to trigger tasks in other peripherals and/or the CPU by tying events to CPU interrupts.

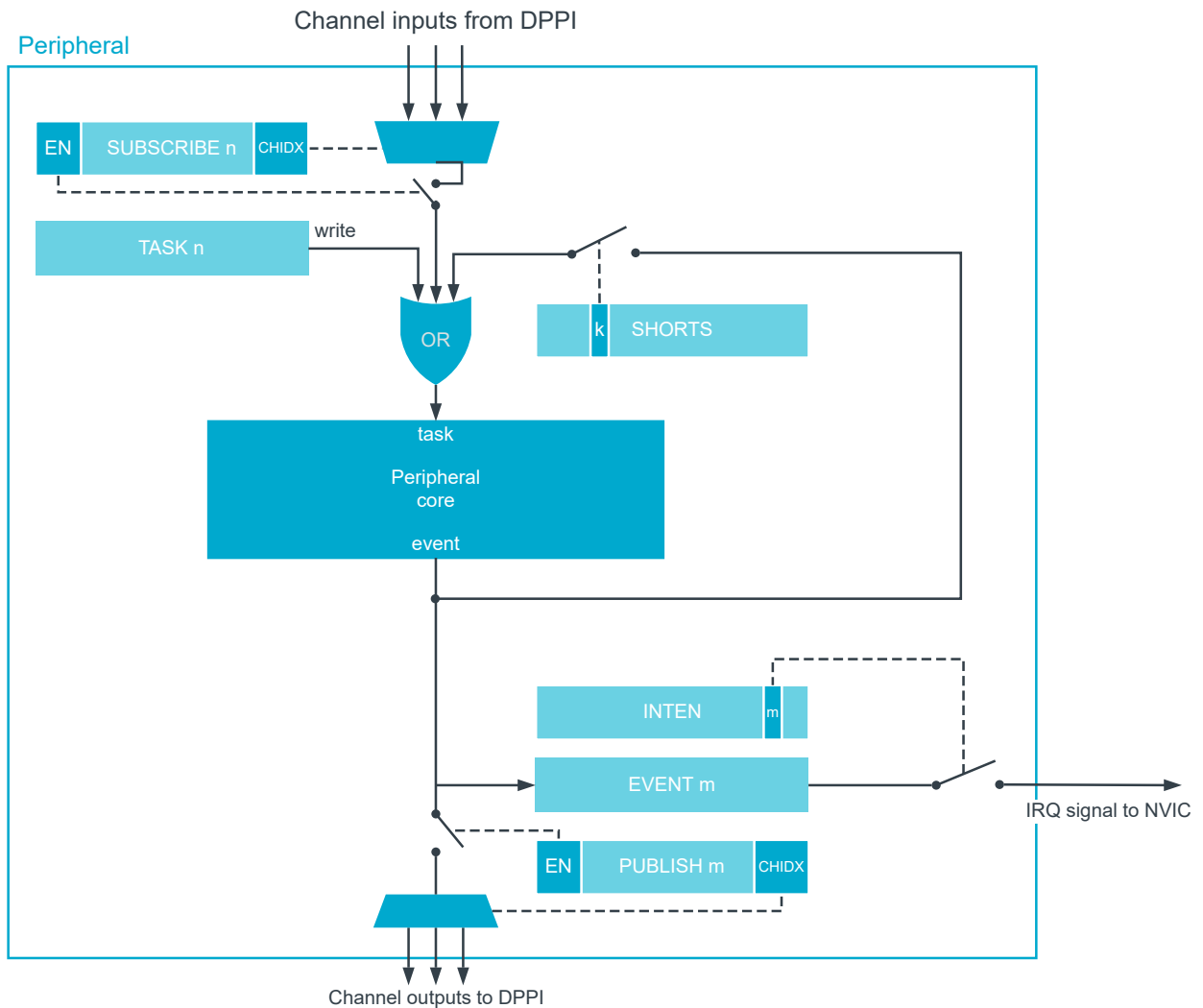


Figure 2: Peripheral interface

The distributed programmable peripheral interconnect (DPPI) feature enables peripherals to connect events to tasks without CPU intervention. For more information on DPPI and the DPPI channels, see .

3.2.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32-bit registers.

See [Instantiation](#) for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Shared registers or common resources
- Limited availability due to mutually exclusive operation; only one peripheral in use at a time

- Enforced peripheral behavior when switching between peripherals (disable the first peripheral before enabling the second)

3.2.2 Peripherals with shared ID

Peripherals sharing an ID and a base address can not be used simultaneously. Only one peripheral can be enabled per ID.

When switching between two peripherals sharing an ID, the following should be performed to prevent unwanted behavior:

1. Disable the previously used peripheral.
2. Disable any publish/subscribe connection to the DPPI system for the peripheral that is being disabled.
3. Clear all bits in the INTEN register. (For example, `INTENCLR = 0xFFFFFFFF`).
4. Configure the peripheral being enabled. Do not rely on the inherited configuration from the disabled peripheral.
5. Enable the configured peripheral.

For a list of peripherals that share an ID, see [Instantiation](#).

3.2.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified, the peripheral registers must be configured before enabling the peripheral.

PSEL registers need to be set before a peripheral is enabled or started. Updating PSEL registers while the peripheral is running has no effect. To connect a peripheral to a different GPIO, the following must be performed:

1. Disable the peripheral.
2. Update the PSEL register.
3. Re-enable the peripheral.

It takes four CPU cycles between the PSEL register update and the connection between a peripheral and a GPIO becoming effective.

Note: The peripheral must be enabled before tasks and events can be used.

Most of the register values are lost during System OFF or when a reset is triggered. Some registers will retain their values in System OFF or for some specific reset sources. These registers are marked as retained in the register description for a given peripheral. For more information on their behavior, see chapter .

3.2.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the set-and-clear pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map, where the main register is followed by dedicated SET and CLR registers (in that exact order).

In the main register, the SET register sets individual bits and the CLR register clears them. Writing 1 to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing 0 to a bit in the SET or CLR register has no effect. Reading the SET or CLR register returns the value of the main register.

Note: The main register may not be visible and therefore not directly accessible in all cases.

3.2.5 Tasks

Tasks are used to trigger actions in a peripheral, such as to start a particular behavior. A peripheral can implement multiple tasks, with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes 1 to the task register, or when the peripheral itself or another peripheral toggles the corresponding task signal. See the figure [Peripheral interface](#) on page 11.

3.2.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example a state change in a peripheral. A peripheral may generate multiple events, where each event has a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated, see figure [Peripheral interface](#) on page 11. An event register is cleared when a 0 is written to it by firmware. Events can be generated by the peripheral even when the event register is set to 1.

3.2.7 Publish and subscribe

Events and tasks from different peripherals can be connected together through the DPPI system using the PUBLISH and SUBSCRIBE registers in each peripheral. See [Peripheral interface](#) on page 11. An event can be published to a DPPI channel by configuring the event's PUBLISH register. Similarly, a task can subscribe to a DPPI channel by configuring the task's SUBSCRIBE register.

See [for details](#).

3.2.8 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, the associated task is automatically triggered when its associated event is generated.

Using shortcuts is equivalent to making the connection outside the peripheral and through the DPPI. However, the propagation delay when using shortcuts is usually shorter than the propagation delay through the DPPI.

Shortcuts are predefined, which means that their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

3.2.9 Interrupts

All peripherals support interrupts which are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC).

Using registers INTEN, INTENSET, and INTENCLR, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR registers, and the INTEN register is not available on those peripherals. See the individual peripheral chapters for details. In all cases, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET, and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is illustrated in figure [Peripheral interface](#) on page 11.

3.2.9.1 Interrupt clearing and disabling

Interrupts should always be cleared by writing 0 to the corresponding EVENT register.

Until cleared, interrupts will immediately be re-triggered and cause software interrupt service routines to be executed repeatedly.

Because the clearing of the EVENT register may take a number of CPU clock cycles, the program should perform a read from the EVENT register that has been cleared before exiting the interrupt service routine. This will ensure that the EVENT clearing has taken place before the interrupt service routine is exited. Care should be taken to ensure that the compiler does not remove the read operation as an optimization.

Similarly, when disabling an interrupt inside an interrupt service routine, the program should perform a read from the INTEN or INTENCLR registers to ensure that the interrupt is disabled before exiting the interrupt service routine.

3.2.10 Secure/non-secure peripherals

For some peripherals, the security configuration can change from secure to non-secure, or vice versa. Care must be taken when changing the security configuration of a peripheral, to prevent security information leakage and ensure correct operation.

The following sequence should be followed, where applicable, when configuring and changing the security settings of a peripheral in the .

1. Stop peripheral operation.
2. Disable the peripheral.
3. Remove pin connections.
4. Disable DPPI connections.
5. Clear sensitive registers (e.g. writing back default values).
6. Change peripheral security setting in the .
7. Re-enable the peripheral.

4 LTE modem

The nRF9151 SiP contains a Low-Power Wide-Area (LPWA) network processor with dedicated flash memory and RAM, which controls the radio and baseband hardware components. After installing Nordic Semiconductor firmware, long term evolution (LTE) capabilities are available and comply with release 14 of the 3GPP LTE Cat-M1 and Cat-NB1/NB2 standards and release 17 of the 3GPP IoT NTN standard.

The key features of the LTE modem are the following:

- Complete modem with baseband and RF transceiver
- 3GPP release 14 compliant LTE categories:
 - Cat-M1 (eMTC – enhanced machine type communication)
 - Cat-NB1 (NB-IoT – narrowband Internet of things)
 - Cat-NB2 (NB-IoT)
- 3GPP release 17 compliant LTE categories:
 - Internet of Things Non-Terrestrial Network (IoT NTN)
 - IoT NTN is based on Cat-NB1/NB2
- Power saving modes
- Supports LTE bands from 700 MHz to 2.2 GHz through a single 50 Ω antenna pin
- 1.8 V MIPI RF Front-End (MIPI RFFE) digital control interface and MAGPIO control interface for external RF applications
- LTE modem internal ADC for some AT command interface services
- 1.8 V UICC (universal integrated circuit card) interface, based on ISO/IEC 7816-3 that is compliant with the following:
 - UICC (ETSI TS 102 221)
 - eUICC (ETSI TS 103 383)

The following figure is an overview of the key components of the LTE modem.

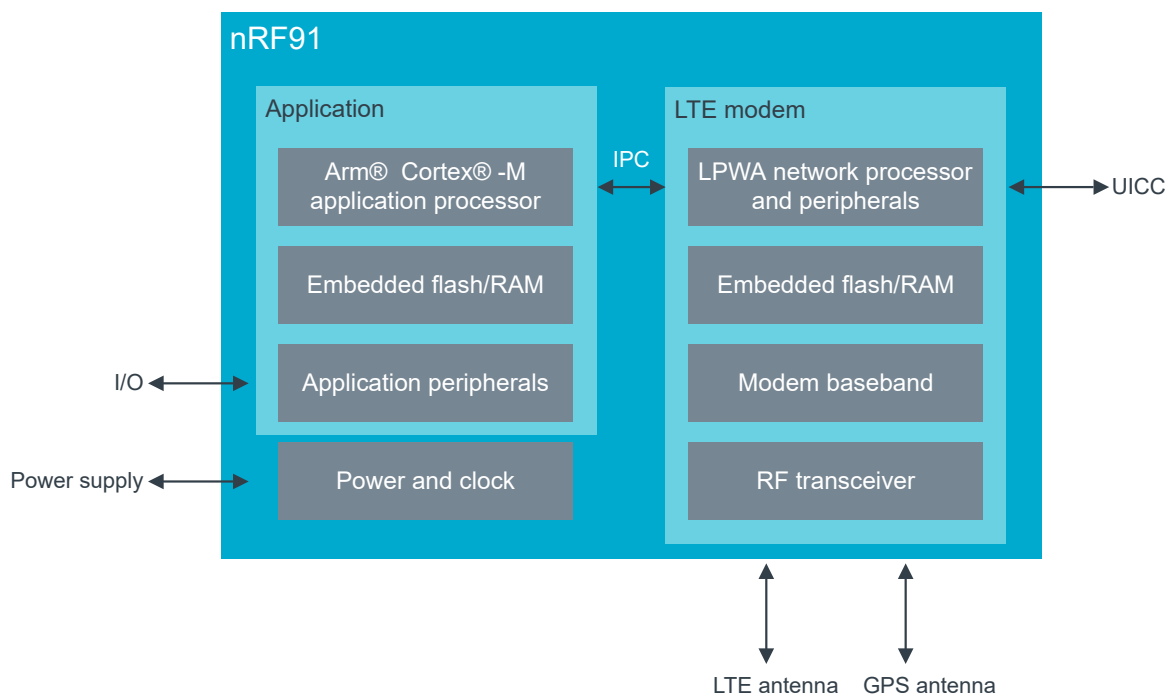


Figure 3: nRF9151 LTE modem functional overview

These components provide functions for the LTE L1, L2, and L3 (layers 1, 2, and 3 respectively), as well as IP communication layers. Peripherals provide hardware services for the LPWA network processor operating system and ensure a secure execution environment.

Application and LPWA network domains interact through the interprocessor communication (IPC) mechanism. The LTE modem is accessible through the modem API.

The application processor is the system manager and is responsible for starting and stopping the LTE modem. The LPWA network processor enables the clocks and power required for operation while the platform handles shared resources, such as clocks. When a hard fault is detected in the modem, the application domain will perform a hard reset of the modem.

The nRF9151 LTE modem feature set is dependent on the modem firmware version and the application firmware. For more information on the LTE modem API, see [nRF Connect SDK API documentation](#) and [nRF91 AT Commands](#).

4.1 Non-Terrestrial Network

The LTE modem supports 3GPP Internet of Things Non-Terrestrial Network (IoT NTN) based on Cat-NB1/NB2. This feature is available after installing firmware that implements the modified Cat-NB1/NB2 physical layer (PHY) and layer 2 and 3 level operation of the NTN radio protocol stack according to 3GPP specifications.

The IoT NTN radio layer extends cellular radio capabilities. The following are key features of IoT NTN:

- Supports major global Mobile Satellite Service (MSS) bands, including B249 in TDD mode
- Built-in coexistence of terrestrial networks in the same location
- Full integration into 3GPP network architectures and ecosystem
- Cat-NB1 and Cat-NB2 support
- Single-tone and multi-tone transmission
- UE location from an external GNSS source
- Support for different satellite deployment models, with simultaneous UE support
- UE ability to pre-compensate its Timing Advance and the frequency Doppler shift relative to the satellite position and satellite velocity through the network provided satellite ephemeris and a valid UE GNSS position
- Skylo proprietary optimisations

See [3GPP TS 36.300](#) and [3GPP TS 36.306](#) for more information.

IoT NTN operates on the global MSS bands, which are distinct from terrestrial bands. A satellite cell may cover a large geographical area up to hundreds of kilometres in diameter. The large earth fixed cells, and specifically moving cells, can cross country borders or cover areas with no territorial claims. Therefore, regulatory aspects also need to be carefully considered (see 3GPP TR 22.926).

IoT NTN is based on Cat-NB1/NB2 cellular radio standard that is included as part of the 3GPP R17 and later, with a priority on non-terrestrial (satellite) access. The standard covers both the transparent payload (non-regenerative) and the non-transparent (regenerative) payload deployment cases.

Support for non-terrestrial networks encompasses platforms that provide radio access through Geosynchronous Orbit (GSO) and Non-Geosynchronous Orbit (NGSO), which includes Low Earth Orbit (LEO) and Medium Earth Orbit (MEO). Typical orbiting altitudes above the Earth's equator are the following:

- LEO – 500 km to 2000 km
- MEO – 8000 km to 20,000 km
- GSO – 35,786 km

UEs equipped with normal terrestrial antenna design can communicate with LEO satellites, and depending on the antenna design, GSO satellites.

Depending on the satellite system and the constellation that is used, the following three types of service links between the UE and the satellite are supported:

- Earth fixed – provisioned by beam(s) continuously covering the same geographical areas all the time (for example, GSO satellites)
- Quasi Earth fixed – provisioned by beam(s) covering one geographic area for a limited period and a different geographic area during another period (for example, NGSO satellites generating steerable beams)
- Earth moving – provisioned by beam(s) whose coverage area slides over the Earth's surface (for example, NGSO satellites generating fixed or non-steerable beams)

IoT NTN on nRF9151

Nordic Semiconductor provides 3GPP IoT NTN enabled firmware that implements a modified Cat-NB1/NB2 PHY, Layer 2, and Layer 3 level operation of the NTN radio protocol stack for Cat-NB1/NB2 according to 3GPP R17 and later specifications. The stack provides support for all GSO and NGSO satellite systems operating above an altitude of 500 km.

Note: While running the IoT NTN enabled firmware, the nRF9151 supports switching between terrestrial and non-terrestrial radio access. While accessing another radio technology, the UE/NW context of non-terrestrial access can be preserved allowing rapid and low (zero) signalling overhead switch between terrestrial and non-terrestrial access technologies.

Supported IoT NTN bands

E UTRA operating band	Duplex mode	Common name	Uplink (MHz)	Downlink (MHz)	Duplex spacing (MHz)
249	TDD		1616 to 1626.5	1616 to 1626.5	-
23/252	FDD	S-BAND NTN	2000 to 2020	2180 to 2200	160
255	FDD	L-Band (global) NTN	1626.5 to 1660.5	1525 to 1559	-101.5
256	FDD	S-band (Europe) NTN	1980 to 2010	2170 to 2200	190

Table 4: Supported IoT NTN bands

See [3GPP TS 36.102](#) for more information.

Supported 3GPP IoT NTN Satellite Systems

Satellite System	Notes
GSO	3GPP R17 support Skylo specific features
NGSO	3GPP R17 LEO/MEO 3GPP R19 LEO in TDD Mode

Table 5: Supported 3GPP IoT NTN Satellite Systems

4.2 SIM card interface

The LTE modem supports the universal integrated circuit card (UICC) interface.

Only UICCs with electrical interfaces specified in ISO/IEC 7816-3 are supported. UICCs with IC-USB, CLF or MMC interfaces are not supported.

The supported UICC/eUICC interface is compliant with:

- ETSI TS 102 221: Smart Cards; UICC-Terminal interface; Physical and logical characteristics
- ETSI TS 103 383: Smart Cards; Embedded UICC; Requirements Specification

The physical interface towards the eUICC is the same as that towards the removable UICC.

By default, only the class C (supply voltage 1.8 V nominal) operation is supported. Support for legacy class B (supply voltage 3.0 V nominal) operation must be built with external components, including an external power supply and the level shifters towards the LTE modem UICC interface.

The LTE modem supports powering down the UICC during PSM and eDRX idle mode if the UICC supports this feature as specified in 3GPP TS 24.301. To reach the lowest total power consumption of the complete cellular IoT product, only UICCs supporting power down mode during PSM and eDRX idle mode sleep intervals should be considered.

The LTE modem controls the physical interfaces towards the UICC and implements the transport protocol over the four-pin ISO/IEC 7816-3 interface:

- VCC (power supply) – LTE modem drives this
- CLK (clock signal) – LTE modem drives this
- RST (reset signal) – LTE modem drives this
- I/O (input/output serial data) – Bi-directional

The interface between the LTE modem, the UICC (SIM card) connector, and the ESD device is shown in the following figure.

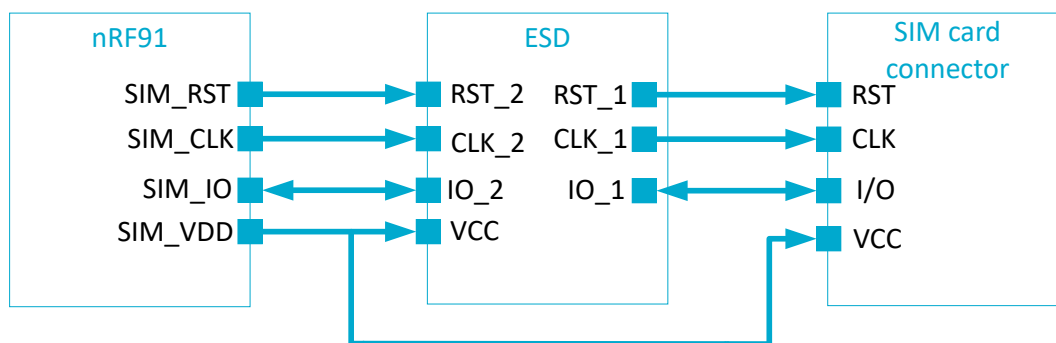


Figure 4: Connections between LTE modem, card connector, and the ESD device

Only standard transmission speeds are supported as specified in ETSI TS 102 221.

Note: Before removing the UICC, the LTE modem must be stopped through the modem API.

An electrostatic discharge (ESD) protection device compatible with UICC cards must be used between the removable card and the LTE modem, to protect LTE modem against harmful ESD from the card connector.

4.3 LTE coexistence interface

The LTE modem uses a dedicated three-pin interface for RF interference avoidance towards a companion radio device such as an external positioning device or *Bluetooth*® Low Energy device.

The interface has the following outputs:

- COEX0 – Output from the LTE modem to the external device. When internal GPS is used, COEX0 can be used as active high control for the external LNA component.
- COEX1 – Output from the LTE modem to the external device. When internal GPS is used, COEX1 delivers the GPS 1PPS (one pulse per second) time mark pulse. The 1PPS feature must not be used when LTE is enabled.
- COEX2 – Output from the LTE modem to the external device. When active high, this indicates that the LTE modem transceiver is turned on. COEX2 can also be treated as an active low grant from the LTE modem to the external device, indicating permission to transmit and receive.

Note: Using the COEX2 pin requires an external pull-down resistor in the 100 kΩ size range.

The COEX interface timing in relation to the LTE modem state is shown in the following figure.

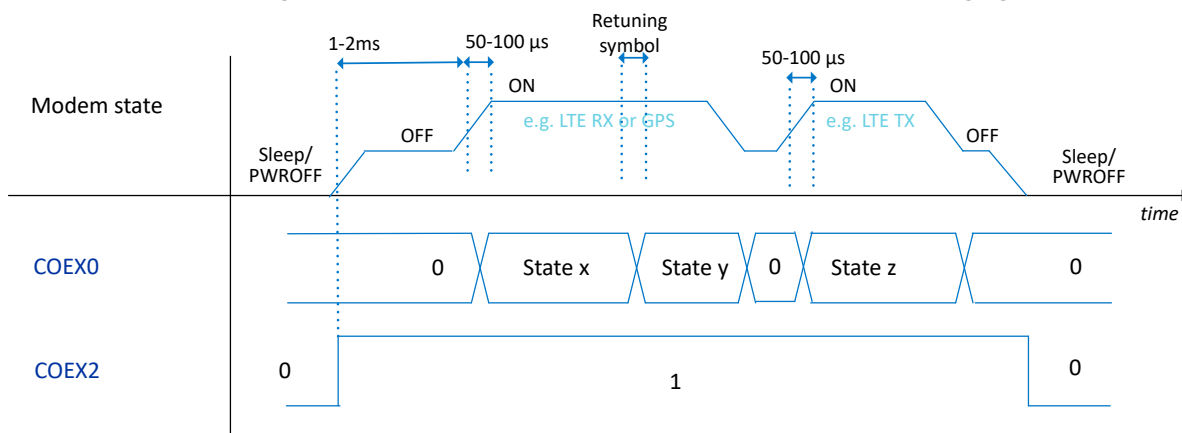


Figure 5: COEX interface timing

4.4 LTE RF control external interface

The LTE modem provides dedicated 1.8 V digital interfaces for controlling external RF applications, such as antenna tuner devices.

The LTE modem supports the following pins:

- MIPI RFFE interface pins – **VIO**, **SCLK**, and **SDATA**
 - Only one connected RFFE component supported at a time
- **MAGPIO** [0 . . 2] interface pins

The LTE modem drives the timing of these applications according to the LTE protocol. The LTE modem API must be used to inform the LTE modem about an external RF application, before the LTE modem can drive it.

Note: The MIPI RFFE capacitive load on the **SCLK** or **SDATA** pin must not exceed 15 pF.

The MIPI RFFE interface timing in relation to modem state is shown in the following figure.

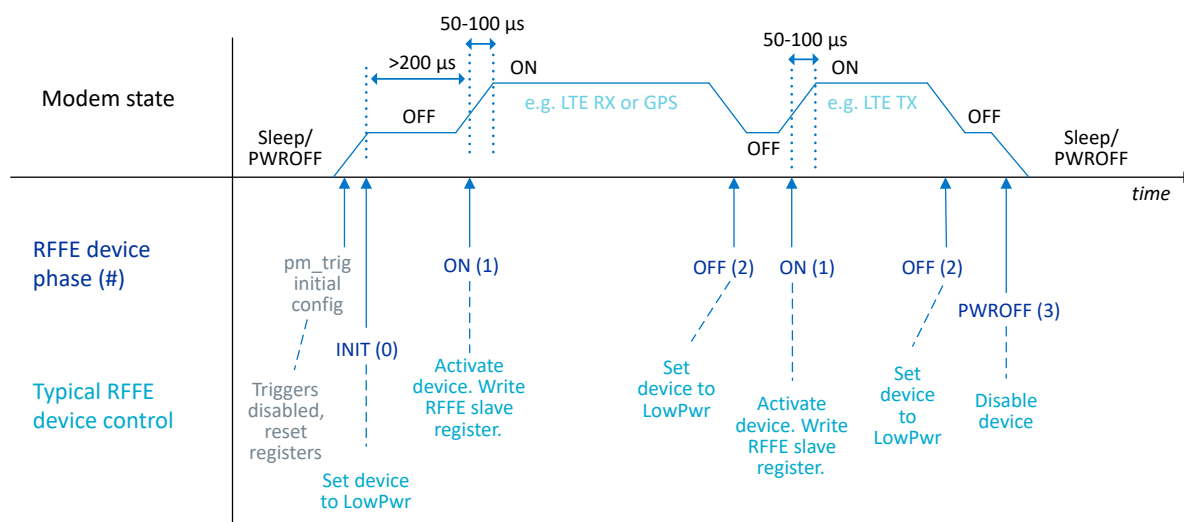


Figure 6: MIPI RFFE interface timing

The MAGPIO interface timing in relation to the LTE modem state is shown in the following figure.

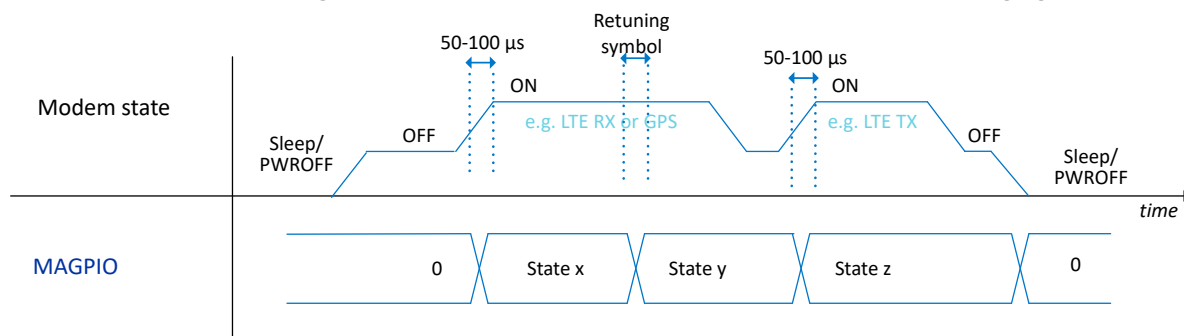


Figure 7: MAGPIO interface timing

4.5 RF front-end interface

The nRF9151 has a single-ended (SE) 50 Ω antenna interface to which an antenna is directly connected.

4.6 Electrical specification

4.6.1 Key RF parameters for Cat-M1

Note: For certification status, please refer to [Regulatory information](#) on page 39.

Symbol	Description	Min.	Typ.	Max.	Units
Supported LTE	Supported LTE standards		LTE Rel-14 Cat-M1 HD- FDD		
Bands supported	Bands supported		B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B85, B106		
Transmission bandwidth	Maximum bandwidth		1.4		MHz

4.6.2 Key RF parameters for Cat-NB1 and Cat-NB2

Note: For certification status, please refer to [Regulatory information](#) on page 39.

Note: There is no foreseen NB-IoT network deployment for FCC bands closer than 200 kHz from band edge, hence our device will not transmit in FCC bands on channels that are closer than 200kHz to band edge.

Symbol	Description	Min.	Typ.	Max.	Units
Supported LTE	Supported LTE standards		LTE Rel-14 Cat-NB1 and Cat- NB2 HD- FDD		
Bands supported	Bands supported		B1, B2, B3, B4, B5, B8, B12, B13, B17, B19, B20, B25, B26, B28, B65, B66, B85, B106		
Transmission bandwidth	Maximum bandwidth		200		kHz

4.6.3 Key RF parameters for IoT NTN

Note: For certification status, please refer to [Regulatory information](#) on page 39.

Note: There is no foreseen IoT NTN network deployment for FCC bands closer than 200 kHz from band edge, hence our device will not transmit in FCC bands on channels that are closer than 200kHz to band edge.

Symbol	Description	Min.	Typ.	Max.	Units
Supported LTE	Supported LTE standards		LTE Rel-17 IoT NTN		
Bands supported	Bands supported		B23, B249, B252, B255, B256		
Transmission bandwidth	Maximum bandwidth		200		kHz

4.6.4 Receiver parameters for Cat-M1

Symbol	Description	Min.	Typ.	Max.	Units
Freq _{range_ANT_RX}	RX operation frequency range at ANT pin	728		2200	MHz
Z _{in}	Input impedance, single-ended		50		Ω
Sensitivity, low band	LTE 1.4 MHz without coverage extension	-103	-108		dBm
Sensitivity, mid band	LTE 1.4 MHz without coverage extension	-103	-107		dBm

4.6.5 Receiver parameters for Cat-NB1 and Cat-NB2

Symbol	Description	Min.	Typ.	Max.	Units
Freq _{range_ANT_RX}	RX operation frequency range at ANT pin	728		2200	MHz
Z _{in}	Input impedance, single-ended		50		Ω
Sensitivity, low band	NB 200 kHz without coverage extension	-108	-114		dBm
Sensitivity, mid band	NB 200 kHz without coverage extension	-108	-113		dBm

4.6.6 Receiver parameters for IoT NTN

Symbol	Description	Min.	Typ.	Max.	Units
Freq _{range_ANT_RX}	RX operation frequency range at ANT pin	728		2200	MHz
Z _{in}	Input impedance, single-ended		50		Ω
Sensitivity, mid band	NB 200 kHz without coverage extension	-108	-113		dBm

4.6.7 Transmitter parameters for Cat-M1

Symbol	Description	Min.	Typ.	Max.	Units
Freq _{range_ANT_TX}	TX operation frequency range at ANT pin	698		1980	MHz
Z _{out}	Output impedance, single-ended		50		Ω
PC3 maximum output power	Power Class 3 maximum output power		23		dBm
PC5 maximum output power	Power Class 5 maximum output power		20		dBm
Minimum output power	Minimum output power		-40		dBm
Pout maximum accuracy	Pout maximum accuracy		±2		dB

4.6.8 Transmitter parameters for Cat-NB1 and Cat-NB2

Symbol	Description	Min.	Typ.	Max.	Units
Freq _{range_ANT_TX}	TX operation frequency range at ANT pin	698		2010	MHz
Z _{out}	Output impedance, single-ended		50		Ω
PC3 maximum output power	Power Class 3 maximum output power		23		dBm
PC5 maximum output power	Power Class 5 maximum output power		20		dBm
Minimum output power	Minimum output power		-40		dBm
Pout maximum accuracy	Pout maximum accuracy		±2		dB

4.6.9 Transmitter parameters for IoT NTN

Symbol	Description	Min.	Typ.	Max.	Units
Freq _{range_ANT_TX}	TX operation frequency range at ANT pin	1616		2020	MHz
Z _{out}	Output impedance, single-ended		50		Ω
PC3 maximum output power	Power Class 3 maximum output power		23		dBm
PC5 maximum output power	Power Class 5 maximum output power		20		dBm
Minimum output power	Minimum output power		-40		dBm
Pout maximum accuracy	Pout maximum accuracy		±2		dB

5 DECT NR+

The nRF9151 SiP contains a Low-Power Wide-Area (LPWA) network processor with dedicated flash/RAM, which controls the radio and baseband hardware components. DECT NR+ (NR+) capabilities are provided by installing Nordic Semiconductor firmware, that implements the physical layer (PHY) level operation of the NR+ radio protocol stack according to ETSI specifications (TS 103 636-2 and TS 103 636-3). Current implementation supports standard v1.5.1.

NR+ runs an alternative modem firmware that is separately available from Nordic Semiconductor. When using NR+, the LTE and GPS functionality cannot be used.

NR+ is a non-cellular radio standard included as part of the 5G standards by the International Telecommunication Union (ITU). It is designed for massive Machine Type Communication (mMTC) and for Ultra-Reliable Low Latency Communication (URLLC).

NR+ operates on the global and license-exempt 1.9 GHz band, which significantly cuts deployment costs by eliminating the need for frequency planning or heavy certification. The NR+ device developer can design optimal radio behavior since there is no need for third-party cellular infrastructure. Additionally, the range and dense topology properties of NR+ make it highly scalable. A square kilometer can be covered by as little as 100 devices or scaled up to over 1 million devices while maintaining the same reliable, low-latency communication.

The physical radio layer in NR+ reuses known techniques from cellular radios, reaching the same level of reliability that is proven by billions of devices already in the field.

The following are key features of NR+:

- License-exempt global band
- Built-in coexistence of multiple networks in the same location
- Flexible, low-latency system and network architectures
- High reliability, using hybrid ARQ
- Possibility of hiding the network, using AES-128 encryption and integrity protection
- Peak data rate up to 3.4 Mbps, depending on modulation

See [ETSI TS 103 636-1](#) for more information.

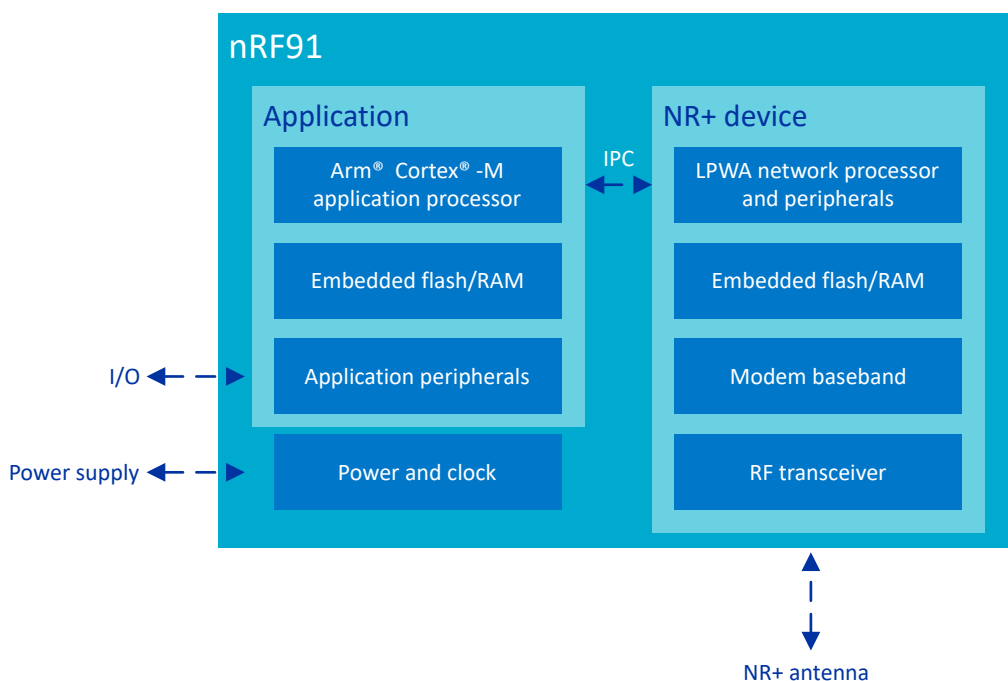


Figure 8: nRF9151 NR+ device functional overview

Application and LPWA network domains interact through the interprocessor communication (IPC) mechanism. The application processor is the system master and is responsible for starting and stopping the NR+ device. The LPWA network processor enables the clocks and power required for its own operation. The platform handles shared resources, such as clocks, and does not need user participation.

5.1 massive Machine Type Communication (mMTC)

mMTC is used for large networks with machine-type devices, connecting tens of billions of nodes that operate for many years using small batteries and transmit small amounts of data.

Typical use cases involve collecting measurements from many sensors, such as smart metering, which requires a low-maintenance and low-cost autonomous network structure.

A key feature of NR+ is its self-healing and self-organizing properties. Each node can function as a router to an access point with a connection to the internet. Nodes can change to a routing role based on the needs of the network. Multiple access points to the internet can be supported in a single network. These properties eliminates single points of failure and resolves high-traffic situations that can occur in dense IoT networks.

5.2 Ultra-Reliable Low-Latency Communication (URLLC)

URLLC enables mission-critical wireless use cases where failure is not an option.

Examples include management of self-driving factory vehicles, high-speed robots working alongside human operators in warehouses, and critical infrastructure in buildings, cities, and utilities.

NR+ is designed to reach one-millisecond latency between devices, opening the possibility for low-latency systems to consider wireless operation, even where ranges are over a kilometer. This makes NR+ an open, standardized alternative to existing proprietary technology.

5.3 DECT NR+ on the nRF9151

Nordic Semiconductor provides NR+ firmware that implements the physical layer (PHY) level operation of the NR+ radio protocol stack according to ETSI specifications (*TS 103 636-2 and TS 103 636-3*).

The antenna interface and recommendations are the same as for the LTE modem. NR+ does not require a SIM or eSIM.

Note: While running DECT NR+ firmware, the nRF9151 SiP does not support the LTE modem or GPS receiver. See the [LTE modem](#) section for more information on alternative firmware.

5.4 Key RF Parameters

NR+ RF performance parameters are shown in the following table.

Description	Min	Typ	Max	Unit
Bands supported		1, 2, 4, 9, 22		
Transmission Bandwidth		1.728		MHz
Occupied Bandwidth		1.539		MHz
Antenna impedance, single-ended		50		Ω
RX: Sensitivity		-105 dBm, PLCF Type 1 (beacon reception, MCS 0) -103 dBm, PLCF Type 2 (unicast reception, MCS 1)		dBm
TX: Maximum output power		19 dBm on band 4 21 dBm on bands 1, 2, 9, 22		dBm
TX: Minimum output power		-40		dBm

Table 6: Common parameters

Note: The RX sensitivity level has not been measured using the same method as described in *ETSI TS 103 636-2* chapter "7.2 Reference sensitivity". The reported sensitivity level is the signal level where 10% packet error rate (PER) occurs. This measurement method does not measure the throughput and does not include HARQ., modulation MCS1.

5.5 DECT NR+ coexistence interface

NR+ uses a dedicated two-pin coexistence interface to avoid RF interference to a companion radio device such as an external positioning device or a Bluetooth Low Energy device.

The user can configure COEX0 and COEX2 pin functions through the [NR+ AT commands](#).

Note: Using the COEX2 pin requires an external pull-down resistor in the 100 k Ω range.

6 GPS receiver

The LPWA network processor supports GPS reception, if the onboard network protocol firmware supports it.

GPS receiver operation is time multiplexed with the LTE modem, and GPS and QZSS position can be received while the LTE modem is in RRC Idle mode, power saving mode (PSM), or completely deactivated.

The application processor is the system master and responsible for starting and stopping the GPS receiver. GPS can be run standalone or concurrently with QZSS. The GPS and QZSS reception can be configured through the GNSS interface API.

Note: For details regarding the GNSS API, refer to [nRF Connect SDK API documentation](#).

Key features of the GPS receiver are as follows:

- GPS L1 C/A reception
- QZSS L1 C/A reception
- Optimized for low-power and low-cost IoT applications
- Modes of operation:
 - Single shot
 - Position fix per fixed interval, configurable to a value between 10 s to 65536 s
 - Continuous tracking
- Power saving mode:
 - Duty-cycled continuous tracking operation
- One pulse per second (1PPS) signal:
 - A pulse repeating once per second, accurately synchronized to coordinated universal time (UTC) full seconds
 - For more details on 1PPS programmability and power vs. accuracy trade-offs, see GNSS API documentation
 - Available on device COEX1 pin
 - For more details, see [LTE modem](#) on page 15, coexistence interface
- Antenna interface:
 - External low-noise amplifier (LNA) with SAW filter recommended on the GPS antenna input
 - Dedicated GPS antenna, or shared antenna with LTE
 - GPS antenna pin is DC grounded

Note: There must be minimum 27dB attenuation to out of band power to avoid blocking high power RF signals to GPS receiver input. This can be achieved by using a SAW filter, for example, at the external LNA output.

6.1 Electrical specification

The following is a summary of GPS receiver performance parameters.

Condition	Value
Environment	Open sky
Temperature	25°C
GPS clock source	TCXO

Table 7: Common typical conditions

Note: Local and temporal conditions might lead to considerable variation in TTFF, positioning accuracy, 1PPS signal accuracy.

The figures in the following table assume the use of an external low-noise amplifier (LNA) with SAW filter.

Symbol	Description	Value	Unit
Sensitivity, cold	Acquisition sensitivity, cold start	-146.5	dBm
Sensitivity, hot	Acquisition sensitivity, hot start	-152.5	dBm
Sensitivity, tracking	Tracking sensitivity	-156.5	dBm
TTFF, cold	Time to first fix (TTFF), cold start	30.5	s
TTFF, hot	TTFF, hot start	1.3	s
TTFF, A-GPS	TTFF, A-GPS start	1.3	s
Accuracy, 2D, periodic	Positioning accuracy (CEP50), periodic tracking ¹	3.4	m
Accuracy, 2D, periodic, A-GPS	Positioning accuracy (CEP50), periodic tracking ¹ with A-GPS ²	3.1	m
Accuracy, 2D, continuous	Positioning accuracy (CEP50), continuous tracking	2.0	m
Accuracy, 2D, continuous, A-GPS	Positioning accuracy (CEP50), continuous tracking with A-GPS ²	1.8	m
1PPS accuracy	1PPS signal accuracy, continuous tracking	±35	ns

Table 8: GPS electrical specification

¹ Fix interval 2 min.

² Including NeQuick ionospheric model parameters.

7 Hardware and layout

The following sections describe nRF9151 hardware and layout specifications.

7.1 Pin assignments

This section describes the pin assignment and the pin functions of the nRF9151.

The device provides flexibility when it comes to routing and configuration of the GPIO pins. However, for some pins there are recommendations on pin usage and configuration. See following table for more information about this.

7.1.1 LGA pin assignments

The pin assignment table and figure describe the assignments.

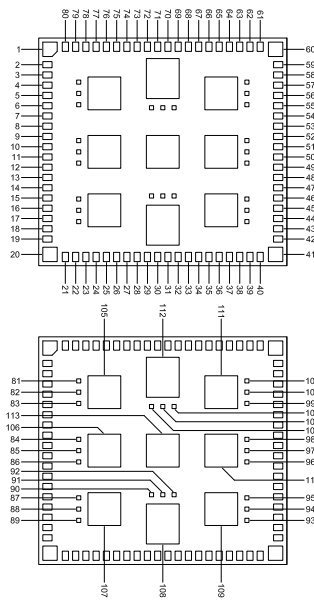


Figure 9: LGA pin assignments, top view

Pin no	Pin name	Function	Description
1	GND	Power	Ground
2	P0.20	Digital I/O (SoC)	General purpose I/O.
	AIN7	Analog input	Analog input.
3	SWDCLK	Digital input	Serial wire debug clock input for debug and programming
4	SWDIO	Digital I/O	Serial wire debug I/O for debug and programming
5	P0.21	Digital I/O (SoC)	General purpose I/O.
	TRACECLK	Trace clock	Trace buffer clock (optional).
6	P0.22	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[0]	Trace data	Trace buffer TRACEDATA[0] (optional).
7	GND	Power	Ground
8	P0.23	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[1]	Trace data	Trace buffer TRACEDATA[1] (optional).

Pin no	Pin name	Function	Description
9	nRESET	Digital I/O (SoC)	SoC reset pin ^{3,4}
10	ENABLE		Enable for the SiP internal regulator for the nRF91 SoC. Note: The nRF9151 will not start until this pin is enabled.
11	P0.24	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[2]	Trace data	Trace buffer TRACEDATA[2] (optional).
12	P0.25	Digital I/O (SoC)	General purpose I/O.
	TRACEDATA[3]	Trace data	Trace buffer TRACEDATA[3] (optional).
13	GND	Power	Ground
14	VDD	Power	Supply voltage
15	GND	Power	Ground
16	SIM_RST	Digital I/O (SoC)	SIM reset
17	SIM_IO	Digital I/O (SoC)	SIM data
18	SIM_CLK	Digital I/O (SoC)	SIM clock
19	SIM_1V8	Power	SIM 1.8 V power supply output
20	GND	Power	Ground
21	MAGPIO0	Digital I/O (SoC)	1.8 V general purpose I/O
22	MAGPIO1	Digital I/O (SoC)	1.8 V general purpose I/O
23	MAGPIO2	Digital I/O (SoC)	1.8 V general purpose I/O
24	DEC0	Power	Power supply decoupling. Reserved for Nordic use.
25	GND	Power	Ground
26	SIM_DET	Digital I/O (SoC)	SIM detect Not used. Must be left floating.
27	SDATA	Digital I/O (SoC)	MIPI RFFE control interface
28	SCLK	Digital I/O (SoC)	MIPI RFFE control interface
29	VIO	Power	MIPI RFFE control interface
30	GND	Power	Ground
31	RESERVED		Connect thermally and mechanically to the application board but leave electrically unconnected.
32	RESERVED		Connect thermally and mechanically to the application board but leave electrically unconnected.
33	RESERVED		Connect thermally and mechanically to the application board but leave electrically unconnected.
34	GND	Power	Ground
35	ANT	RF	Single-ended 50 Ω LTE antenna pin
36	GND	Power	Ground
37	AUX	RF	Single-ended 50 Ω ANT loop-back pin
38	GND	Power	Ground
39	GND	Power	Ground
40	GND	Power	Ground
41	GND	Power	Ground
42	GPS	RF	Single-ended 50 Ω GPS input pin
43	GND	Power	Ground
44	P0.26	Digital I/O (SoC)	General purpose I/O
45	P0.27	Digital I/O (SoC)	General purpose I/O
46	GND	Power	Ground
47	P0.28	Digital I/O (SoC)	General purpose I/O

³ External pull-up not allowed.

⁴ For implementations that require the ERASEALL functionality, enable access to the nRESET pin. See for more information.

Pin no	Pin name	Function	Description
48	P0.29	Digital I/O (SoC)	General purpose I/O
49	P0.30	Digital I/O (SoC)	General purpose I/O
50	P0.31	Digital I/O (SoC)	General purpose I/O
51	GND	Power	Ground
52	COEX0	Digital I/O (SoC)	Coexistence interface
53	COEX1	Digital I/O (SoC)	Coexistence interface
54	COEX2	Digital I/O (SoC)	Coexistence interface
55	GND	Power	Ground
56	P0.00	Digital I/O (SoC)	General purpose I/O
57	P0.01	Digital I/O (SoC)	General purpose I/O
58	P0.02	Digital I/O (SoC)	General purpose I/O
59	P0.03	Digital I/O (SoC)	General purpose I/O
60	GND	Power	Ground
61	P0.04	Digital I/O (SoC)	General purpose I/O
62	P0.05	Digital I/O (SoC)	General purpose I/O
63	P0.06	Digital I/O (SoC)	General purpose I/O
64	P0.07	Digital I/O (SoC)	General purpose I/O
65	VDD_GPIO	Power	GPIO power supply input and logic level
66	GND	Power	Ground
67	P0.08	Digital I/O (SoC)	General purpose I/O
68	P0.09	Digital I/O (SoC)	General purpose I/O
69	P0.10	Digital I/O (SoC)	General purpose I/O
70	P0.11	Digital I/O (SoC)	General purpose I/O
71	GND	Power	Ground
72	P0.12	Digital I/O (SoC)	General purpose I/O
73	P0.13	Digital I/O (SoC)	General purpose I/O.
74	AIN0	Analog input	Analog input.
	P0.14	Digital I/O (SoC)	General purpose I/O.
	AIN1	Analog input	Analog input.
75	P0.15	Digital I/O (SoC)	General purpose I/O.
	AIN2	Analog input	Analog input.
76	GND	Power	Ground
77	P0.16	Digital I/O (SoC)	General purpose I/O.
	AIN3	Analog input	Analog input.
	P0.17	Digital I/O (SoC)	General purpose I/O.
78	AIN4	Analog input	Analog input.
	P0.18	Digital I/O (SoC)	General purpose I/O.
79	AIN5	Analog input	Analog input.
	P0.19	Digital I/O (SoC)	General purpose I/O.
	AIN6	Analog input	Analog input.
80	P0.19	Digital I/O (SoC)	General purpose I/O.
81	RESERVED		Do not connect/reserved for future use
82	RESERVED		Do not connect/reserved for future use
83	RESERVED		Do not connect/reserved for future use
84	RESERVED		Do not connect/reserved for future use
85	RESERVED		Do not connect/reserved for future use
86	RESERVED		Do not connect/reserved for future use
87	RESERVED		Do not connect/reserved for future use
88	RESERVED		Do not connect/reserved for future use
89	RESERVED		Do not connect/reserved for future use
90	RESERVED		Do not connect/reserved for future use
91	RESERVED		Do not connect/reserved for future use

Pin no	Pin name	Function	Description
92	RESERVED		Do not connect/reserved for future use
93	RESERVED		Do not connect/reserved for future use
94	RESERVED		Do not connect/reserved for future use
95	RESERVED		Do not connect/reserved for future use
96	RESERVED		Do not connect/reserved for future use
97	RESERVED		Do not connect/reserved for future use
98	RESERVED		Do not connect/reserved for future use
99	RESERVED		Do not connect/reserved for future use
100	RESERVED		Do not connect/reserved for future use
101	RESERVED		Do not connect/reserved for future use
102	RESERVED		Do not connect/reserved for future use
103	RESERVED		Do not connect/reserved for future use
104	RESERVED		Do not connect/reserved for future use
105	GND	Power	Ground
106	GND	Power	Ground
107	GND	Power	Ground
108	GND	Power	Ground
109	GND	Power	Ground
110	GND	Power	Ground
111	GND	Power	Ground
112	GND	Power	Ground
113	GND	Power	Ground

Table 9: LGA pin assignments

7.2 Mechanical specifications

The mechanical specifications show the package dimensions in millimeters.

7.2.1 12.1 x 11.1 mm package

Dimensions in millimeters for the nRF9151 LGA 12.1 x 11.1 x 1.2 mm package.

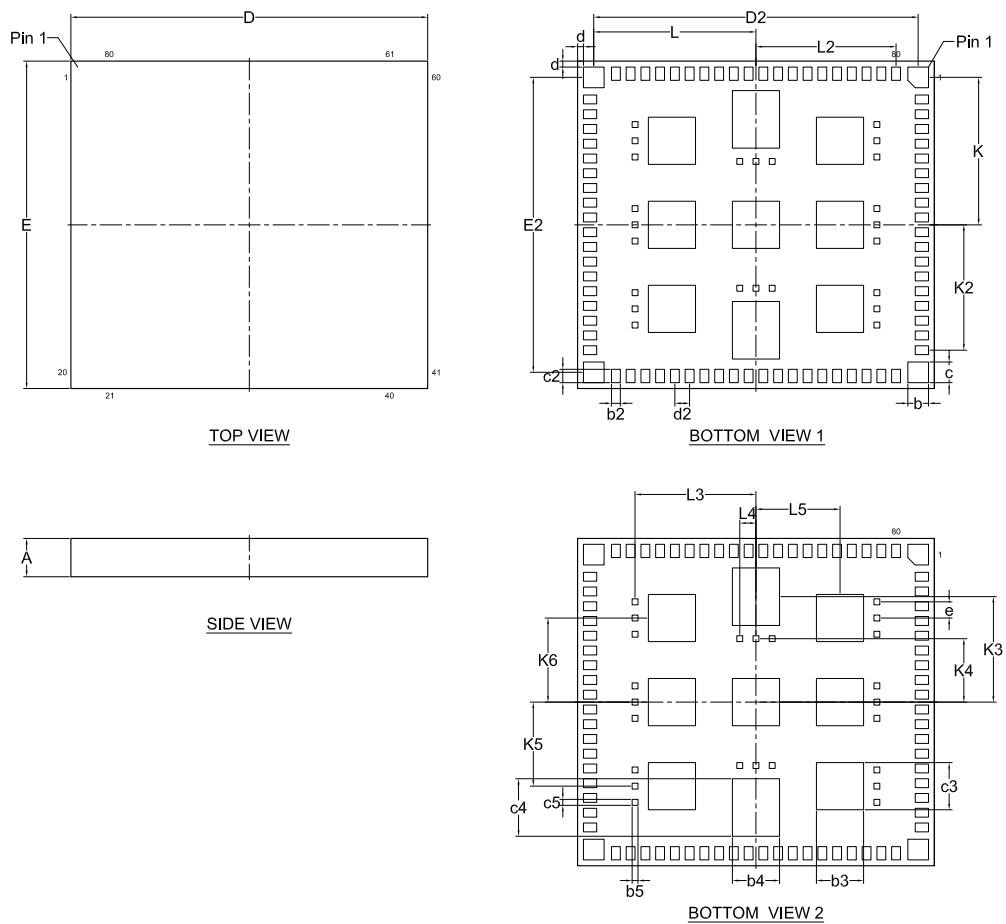


Figure 10: LGA 12.1 x 11.1 mm package

	Min.	Nom.	Max.
A	1.099	1.156	1.3
b	0.65	0.7	0.75
b2	0.25	0.3	0.35
b3	1.55	1.6	1.65
b4	1.55	1.6	1.65
b5	0.15	0.2	0.25
c	0.65	0.7	0.75
c2	0.4	0.45	0.5
c3	1.55	1.6	1.65
c4	1.9	1.95	2.0
c5	0.15	0.2	0.25
D	12	12.1	12.2
D2		11.0	
d		0.2	
d2		0.5	
E	11	11.1	11.2
E2		10.0	
e		0.55	
K		5.0	
K2		4.25	
K3		3.575	
K4		2.15	
K5		2.85	
K6		2.85	
L		5.50	
L2		4.75	
L3		4.1	
L4		0.55	
L5		2.85	

Table 10: LGA dimensions in millimeters

7.3 Reference circuitry

To ensure good RF performance when designing PCBs, using the PCB layouts and component values provided by Nordic Semiconductor is highly recommended .

Documentation for the different package reference circuits, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from the product page at www.nordicsemi.com/nRF9151.

This section contains reference circuitry showing the components to support the design of on-chip features.

Note: This is not a complete list of configurations, but all required circuitry is shown for further configurations.

7.3.1 nRF9151 reference design

Circuit configuration schematic for the nRF9151 SiP.

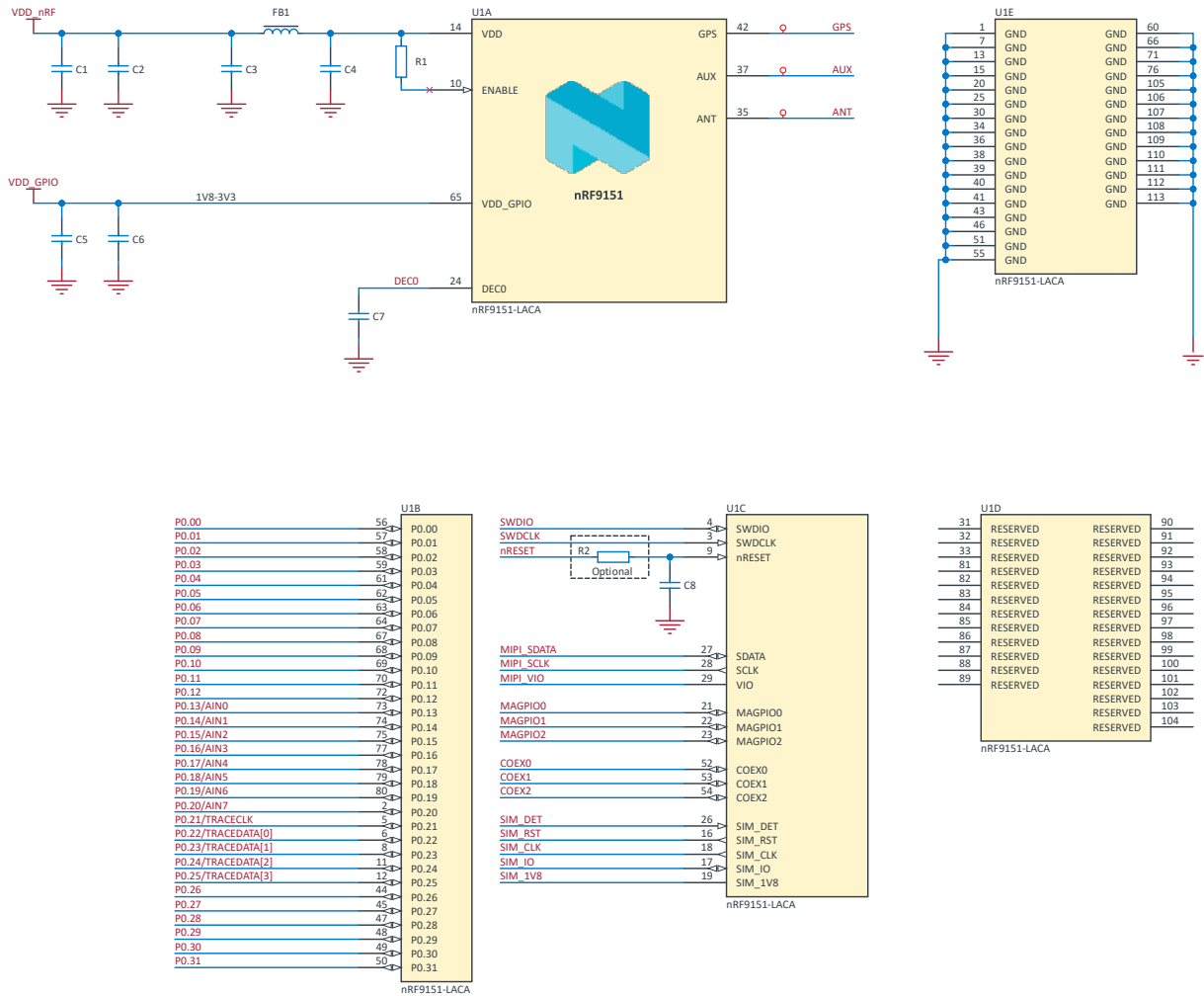


Figure 11: nRF9151 reference design

For Bill of Materials (BOM), PCB layout and thermal design, see the [nRF9151 Hardware Design Guidelines](#).

7.4 Reflow conditions

The recommended reflow profile is JEDEC J-STD-020D.

7.5 Shelf and floor life

If floor life is exceeded, see [Shelf Life of Dry Packed Integrated Circuits](#) for shelf and floor life and recommended baking (drying of parts) requirements.

7.6 Assembly-related instructions

For more detailed instructions related to assembly, see the [nRF9151 Hardware Design Guidelines](#).

8 Operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Notes	Min.	Nom.	Max.	Units
VDD	Battery input voltage	Including voltage drop, ripple and spikes.	3.0	3.7	5.5	V
VDD_GPIO	GPIO input voltage		1.7		3.6	V
GPIO _H	GPIO high level voltage				VDD_GPIO	V
MAGPIO _H	MAGPIO high level voltage	Supply from internal LDO	1.7	1.8	1.9	V
VIO	VIO high level voltage	Supply from internal LDO	1.7	1.8	1.9	V
TA	Operating temperature		-40	25	85	°C
COEX	COEX high level voltage				VDD_GPIO	V
SIMIF	SIMIF output high level voltage	Supply from internal LDO	1.7	1.8	1.9	V

Table 11: Operating conditions

Note: There can be excessive leakage at VDD and/or VDD_GPIO if any of these supply voltages is outside its range given in the table above.

Note: It is not recommended to use high voltage, high drive GPIO outputs ($V_{OH,HDH}$ and $V_{OH,HDL}$) with high frequency, high capacitance loads unless needed, as this may increase noise level and affect radio receiver performance. High drive/high load should especially be avoided on GPIO pins close to the radio front end.

8.1 VDD_GPIO considerations

VDD_GPIO is the supply to the general purpose I/O.

The following restrictions should be taken into considerations:

- VDD_GPIO should be applied after VDD has been supplied
- VDD_GPIO should be removed before removing VDD
- If VDD is supplied and VDD_GPIO is grounded, an extra current consumption can be generated on VDD
- If ENABLE is low, VDD_GPIO should also be low

9 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Note	Min.	Max.	Unit
VDD		-0.3	5.5	V
VDD_GPIO		-0.3	3.9	V
SIM_1V8		1.65	1.95	V
VSS			0	V

Table 12: Supply voltage

	Note	Min.	Max.	Unit
$V_{I/O}, VDD_GPIO \leq 3.6\text{ V}$		-0.3	$VDD_GPIO + 0.3$	V
$V_{I/O}, VDD_GPIO > 3.6\text{ V}$		-0.3	3.9	V

Table 13: I/O pin voltage

	Note	Min.	Max.	Unit
ANT antenna input level			10	dBm
GPS antenna input level	LNA turned on, max gain		-15	dBm
RF port ruggedness	Maximum deviation from 50 Ω without damaging the module		10:1	VSWR

Table 14: Radio

	Note	Min.	Max.	Unit
Storage temperature		-40	95	°C
Reflow conditions	The recommended reflow profile is JEDEC J-STD-020D with 3 maximum reflow cycles.			
MSL	Moisture Sensitivity Level		3	
ESD HBM AUX	AUX pin Human Body Model ¹		500	V
ESD HBM AUX Class	AUX pin Human Body Model Class ¹		1B	
ESD HBM	Human Body Model ²		1.5	kV
ESD HBM Class	Human Body Model Class ²		1C	
ESD CDM	Charged Device Model		250	V
ESD CDM Class	Charged Device Model Class		C1	

Table 15: Environmental (LGA package)

¹The AUX pin is intended for production test.

²AUX pin excluded.

	Note	Min.	Max.	Unit
Endurance		10,000		Write/ erase cycles
Retention		10 years at 85°C		y
No internal voltage boost converters				

Table 16: Flash memory

10 Regulatory information

The nRF9151 undergoes regulatory certifications, ensuring both regional compliances and compatibility with the LTE 3GPP specification.

10.1 Certified bands

The following table shows the FCC and ISED certified Cat-M1 bands for nRF9151.

Band	FCC certification	ISED certification
Band 2	Yes	Yes
Band 4	Yes	Yes
Band 5	Yes	Yes
Band 8	Yes	Yes ⁵
Band 12	Yes	Yes
Band 13	Yes	Yes
Band 25	Yes	Yes
Band 26	Yes	No
Band 66	Yes	Yes
Band 85	Yes	Yes
Band 106	Yes	Yes

Table 17: FCC and ISED certified Cat-M1 bands

The following table shows the FCC and ISED certified Cat-NB1 and Cat-NB2 bands for nRF9151.

⁵ The Band 8 is not supported in Canada.

Band	FCC certification	ISED certification
Band 2	Yes	Yes
Band 4	Yes	Yes
Band 5	Yes	Yes
Band 8	Yes	Yes ⁵
Band 12	Yes	Yes
Band 13	Yes	Yes
Band 17	Yes	Yes
Band 23	Yes	Yes
Band 25	Yes	Yes
Band 26	Yes	No
Band 66	Yes	Yes
Band 85	Yes	Yes
Band 106	Yes	Yes
Band 255	Yes	Yes

Table 18: FCC and ISED certified Cat-NB1/NB2 bands

10.2 Supported FCC/ISED rules

The nRF9151 module has been certified to comply with FCC and ISED rules.

The nRF9151 SiP has been certified to comply with the following FCC rules.

- 47 CFR Part 22
- 47 CFR Part 24
- 47 CFR Part 25
- 47 CFR Part 27
- 47 CFR Part 90
- 47 CFR Part 2.1091

The nRF9151 SiP has been certified to comply with the following ISED rules.

- RSS-102 Issue 6
- RSS-130 Issue 2
- RSS-132 Issue 4
- RSS-133 Issue 7
- RSS-139 Issue 4
- RSS-170 Issue 4

A host manufacturer who integrates the nRF9151 SiP to a host device, can apply the certifications to the host device, except for FCC Part 15 Subpart B which must be retested.

The host manufacturer can use nRF9151's FCC ID if the device meets the conditions of the FCC certificate. Normally, the conditions are the following:

- A minimum of 20 cm distance from the human body.
- No colocation with other transmitters. Typically, this condition needs to be reviewed by the FCC lab.

- Antenna gain below the requirements.

10.3 FCC/ISED regulatory notices

FCC/ISED regulatory notices cover modification and interference statements, wireless and FCC Class B digital device notices, permitted antennas and labeling requirements.

Modification statement

Nordic Semiconductor has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Nordic Semiconductor n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada's licence-exempt RSS standards. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This equipment complies with FCC and ISED radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet appareil est conforme aux limites d'exposition aux rayonnements de l'ISDE pour un environnement non contrôlé. L'antenne doit être installée de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

Permitted antenna

This radio transmitter has been approved by FCC and ISED to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Band	Max gain
Band 2	9.0 dBi
Band 4	6.0 dBi
Band 5	7.1 dBi
Band 8	10.78 dBi
Band 12	6.6 dBi
Band 13	6.9 dBi
Band 17 (Cat-NB1/NB2)	6.6 dBi
Band 23 (Cat-NB1/NB2)	9.0 dBi
Band 25	9.0 dBi
Band 26	7.0 dBi
Band 66	6.0 dBi
Band 85	6.6 dBi
Band 106	10.78 dBi
Band 255 (Cat-NB1/NB2)	6.0 dBi

Le présent émetteur radio a été approuvé par ISDE pour fonctionner avec les types d'antenne énumérés ci dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Bande	Gain maximal
Bande 2	9.0 dBi
Bande 4	6.0 dBi
Bande 5	7.1 dBi
Band 8	10.78 dBi
Bande 12	6.6 dBi
Bande 13	6.9 dBi
Bande 17 (Cat-NB1/NB2)	6.6 dBi
Bande 23 (Cat-NB1/NB2)	9.0 dBi
Bande 25	9.0 dBi
Bande 26	7.0 dBi
Bande 66	6.0 dBi
Bande 85	6.6 dBi
Bande 106	10.78 dBi
Bande 255 (Cat-NB1/NB2)	6.0 dBi

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

CAN ICES-3 (B)/NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

Labeling requirements for the host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as shown in the following examples:

Contains FCC ID: 2ANPO00NRF9151

Contains IC: 24529-NRF9151

L'équipement hôte doit être correctement étiqueté pour identifier les modules dans l'équipement. L'étiquette de certification du module doit être clairement visible en tout temps lorsqu'il est installé dans l'hôte, l'équipement hôte doit être étiqueté pour afficher le FCC ID et IC du module, précédé des mots "Contient le module émetteur", ou le mot "Contient", ou un libellé similaire exprimant la même signification, comme suit:

Contient FCC ID: 2ANPO00NRF9151

Contient IC: 24529-NRF9151

10.4 Anatel regulatory information

Anatel (Brazil) certified device

- Model: nRF9151
- Manufacturer: Nordic Semiconductor
- Country of origin: Norway
- ANATEL ID: 09163-24-16661

10.5 RF exposure considerations

The nRF9151 has been tested and certified as a mobile device for use of a minimum of 20 cm distance from the human body with no colocation with other transmitters. If the device is to be used closer than 20 cm from the human body and/or with other transmitters simultaneously, the host product manufacturer is required to perform additional evaluation, testing, or testing and Class 2 permissive change. It is required to take responsibility of the module through a change in the FCC ID (new application). The host product manufacturer must also inform the end user about RF Exposure conditions.

10.6 Host device manufacturer responsibility

The nRF9151 device is only authorized for the rules listed in [Supported FCC/ISED rules](#) on page 40. The host device manufacturer is responsible for compliance to any other FCC rules that apply to the host device not covered by the nRF9151 grant of certification. It is mandatory for the host device manufacturer to assure the final device's compliance with FCC Part 15 Subpart B even if certification has been granted to nRF9151.

10.7 Antenna interface

The nRF9151 module has a single-ended 50 Ω antenna port where the antenna solution shall be connected. nRF9151 is evaluated with a 50 Ω antenna load. To ensure good overall RF performance, antenna impedance and the characteristic impedance of the transmission line (i.e. cable) connecting the antenna and antenna port must be 50 Ω . Impedance mismatch may lead to performance degradation. Maximum antenna VSWR 2:1 is recommended but VSWR 3:1 can still be accepted in the final device. Respective minimum return loss values are 9.5 dB and 6.0 dB.

The length of the transmission line from the antenna to the nRF9151 antenna port should be kept as short as possible to minimize losses, as this loss is directly deteriorating the module's transmitted and received power. Additionally, low-loss matching circuit between the antenna and the nRF9151 antenna port is recommended to minimize loss caused by antenna and PCB routing mismatch. Reserving space from device manufacturer's application board for matching components (e.g. π -circuit) is recommended. This is because, for example, catalog antennas are typically tuned on reference board and differences to device mechanics may impact antenna impedance. It is also possible that device mechanics change during the development phase of the final device, and these modifications may impact antenna performance. Matching components can be used to compensate the impact of mechanics change to antenna impedance, and thus it may not be mandatory to modify the antenna itself.

The nRF9151 module has an internal ESD circuit in the antenna port, but additional ESD components at device manufacturer's application board may be used. The design of the ESD circuit shall be such that the impact on RF frequencies is negligible

Note: ESD filtering may be necessary for some active components that can be used at antenna path. Such components can be, for example, RF switches and antenna tuners. For further ESD requirements, see the RF switch and antenna tuner datasheets.

10.8 Antenna port test connector

To run conductive RF tests, a test connector nearby the nRF9151 antenna port in the RF transmission line is needed. The 50 Ω impedance requirement applies also to the test connector, and VSWR and insertion loss should be minimal. Regardless of whether the nRF9151 antenna port is connected to an actual antenna or test equipment, the load at the nRF9151 antenna should remain as close to 50 Ω as possible.

For a test connector, microwave coaxial switch connectors (for example, Murata MM8130-2600) are a good choice for this purpose. For conductive tests, a test cable is plugged in which connects the nRF9151

antenna port to the test equipment instead of the antenna. When the test cable is plugged off, the nRF9151 antenna port is connected to the antenna for real use case or radiated testing. The layout for the connector must be carefully designed to fulfil the 50 Ω requirement. For detailed guidance on this, see the coaxial switch connectors datasheets.

10.9 Reference design

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor. See Hardware Design Guidelines for details.

The information on layout of trace design is confidential; host manufacturer shall need to contact module's grantee to obtain this information.

This module can only be used when installed in a host device that follows the required instructions for use of the layout of trace design. Any deviation(s) from the defined parameters of the layout of trace design, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the layout of trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application).

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