nRF9161

Objective Product Specification

v0.7

4510_014 v0.7 / 2023-05-15

NORDIC SEMICONDUCTOR

nRF9161 features

Features:

Microcontroller:

- Arm® Cortex®-M33
  - 247 EEMBC CoreMark score running from flash memory
  - Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace macrocell (ITM)
  - Serial wire debug (SWD)
  - Trace port
- 1 MB flash
- 256 kB low leakage RAM
- Arm TrustZone®
- Arm CryptoCell™ 310
- Up to 4x SPI master/slave with EasyDMA
- Up to 4x I2C compatible two-wire master/slave with EasyDMA
- Up to 4x UART (CTS/RTS) with EasyDMA
- I2S with EasyDMA
- Digital microphone interface (PDM) with EasyDMA
- 4x pulse width modulator (PWM) unit with EasyDMA
- 12-bit, 200 ksps ADC with EasyDMA - eight configurable channels with programmable gain
- 3x 32-bit timer with counter mode
- 2x real-time counter (RTC)
- Programmable peripheral interconnect (PPI)
- 32 general purpose I/O pins
- Single supply voltage: 3.0 – 5.5 V
- All necessary clock sources integrated
- Package: 10 × 16 x 1.04 mm LGA

LTE modem:

- Transceiver and baseband
- 3GPP LTE release 14 Cat-M1 compliant
- 3GPP LTE release 14 Cat-NB1 and Cat-NB2 compliant
- GPS receiver
  - GPS L1 C/A supported
  - QZSS L1 C/A supported
- RF transceiver for global coverage
  - Up to 23 dBm output power
  - -108 dBm sensitivity (Cat-M1) for low band, -107 dBm for mid band
  - Single 50 Ω antenna interface
- LTE band support in hardware:
  - Cat-M1: B1, B2, B3, B4, B5, B8, B12, B13, B18, B19, B20, B25, B26, B28, B66, B85
  - Cat-NB1/NB2: B1, B2, B3, B4, B5, B8, B12, B13, B17, B19, B20, B25, B26, B28, B65, B66, B85
- Supports SIM and eSIM with an ETSI TS 102 221 compatible UICC interface
- Power saving features: DRX, eDRX, PSM
- IP v4/v6 stack
- Secure socket (TLS/DTLS) API

DECT NR+:

- NR+ band: 1, 2, 9

Current consumption @ 3.7 V:

- LTE power saving mode (PSM) floor current: 2.7 µA
- eDRX @ 81.92s: 18 µA in Cat-M1, 32 µA in Cat-NB1 (UICC included)

Applications:

- Sensor networks
- Logistics and asset tracking
- Smart energy
- Smart building automation
- Smart agriculture
- Industrial
- Retail and monitor devices
- Medical devices
- Wearables

Contents

nRF9161 features . . . ii

1 Revision history . . . 10

2 About this document . . . 11

2.1 Document status . . . 11
2.2 Peripheral chapters . . . 11
2.2.2 Peripheral instantiation . . . 11
2.3 Register tables . . . 12
2.3.1 Fields and values . . . 12
2.3.2 Permissions . . . 13
2.4 Registers . . . 13
2.4.1 DUMMY . . . 13

3 Product overview . . . 14

3.1 Block diagram . . . 14
3.2 Peripheral interface . . . 15
3.2.1 Peripheral ID . . . 16
3.2.2 Peripherals with shared ID . . . 17
3.2.3 Peripheral registers . . . 17
3.2.4 Bit set and clear . . . 17
3.2.5 Tasks . . . 18
3.2.6 Events . . . 18
3.2.7 Publish and subscribe . . . 18
3.2.8 Shortcuts . . . 18
3.2.9 Interrupts . . . 18
3.2.10 Secure/non-secure peripherals . . . 19

4 Application core . . . 20

4.1 CPU . . . 20
4.1.1 Floating-point interrupt . . . 20
4.1.2 CPU and support module configuration . . . 20
4.1.3 Electrical specification . . . 21
4.2 Memory . . . 21
4.2.1 Memory map . . . 23
4.2.2 Instantiation . . . 25
4.2.3 Peripheral access control capabilities . . . 27
4.3 VMC — Volatile memory controller . . . 28
4.3.1 Registers . . . 28
4.4 NVMC — Non-volatile memory controller . . . 29
4.4.1 Writing to flash . . . 29
4.4.2 Erasing a secure page in flash . . . 30
4.4.3 Erasing a non-secure page in flash . . . 30
4.4.4 Writing to user information configuration registers (UICR) . . . 30
4.4.5 Erase all . . . 30
4.4.6 NVMC protection mechanisms . . . 31
4.4.7 Cache . . . 31
4.4.8 Registers . . . 32
4.4.9 Electrical specification . . . 35

4.5 FICR — Factory information configuration registers . . . 35
4.5.1 Registers . . . 36
4.6 UICR — User information configuration registers . . . 39
4.6.1 Registers . . . 39
4.7 EasyDMA . . . 43
4.7.1 EasyDMA error handling . . . 45
4.7.2 EasyDMA array list . . . 45
4.8 AHB multilayer interconnect . . . 46
4.8.1 AHB multilayer priorities . . . 46

5 Power and clock management . . . 47

5.1 Power management . . . 47
5.1.1 System Disabled mode . . . 47
5.1.2 System OFF mode . . . 48
5.1.3 System ON mode . . . 49
5.1.4 Registers . . . 49
5.1.5 Electrical specification . . . 49
5.2 Power supply . . . 49
5.2.1 General purpose I/O supply . . . 50
5.3 Power supply monitoring . . . 50
5.3.1 Power supply supervisor . . . 50
5.3.2 External power failure warning . . . 51
5.3.3 Battery monitoring on VDD . . . 52
5.3.4 Registers . . . 52
5.3.5 Electrical specification . . . 52
5.4 Clock management . . . 53
5.4.1 HFCLK clock controller . . . 54
5.4.2 LFCLK clock controller . . . 55
5.4.3 Registers . . . 55
5.4.4 Electrical specification . . . 55
5.5 Reset . . . 56
5.5.1 Power-on reset . . . 56
5.5.2 Pin reset . . . 56
5.5.3 Wakeup from System OFF mode reset . . . 57
5.5.4 Soft reset . . . 57
5.5.5 Watchdog reset . . . 57
5.5.6 Brownout reset . . . 57
5.5.7 Retained registers . . . 57
5.5.8 Reset behavior . . . 57
5.5.9 Registers . . . 58
5.5.10 Electrical specification . . . 58
5.6 Current consumption . . . 58
5.6.1 Electrical specification . . . 59
5.7 Register description . . . 63
5.7.1 POWER — Power control . . . 63
5.7.2 CLOCK — Clock control . . . 70
5.7.3 REGULATORS — Voltage regulators control . . . 77

6 Peripherals . . . 79

6.1 CRYPTOCELL — ARM TrustZone CryptoCell 310 . . . 79
6.1.1 Usage . . . 80
6.1.2 Always-on (AO) power domain . . . 80
6.1.3 Lifecycle state (LCS) . . . 80

6.1.4 Cryptographic key selection . . . 81
6.1.5 Direct memory access (DMA) . . . 81
6.1.6 Standards . . . 81
6.1.7 Registers . . . 82
6.1.8 Host interface . . . 83
6.2 DPPI - Distributed programmable peripheral interconnect . . . 86
6.2.1 Subscribing to and publishing on channels . . . 87
6.2.2 DPPI configuration (DPPIC) . . . 89
6.2.3 Connection examples . . . 89
6.2.4 Special considerations for a system implementing TrustZone for Cortex-M processors . . . 90
6.2.5 Registers . . . 91
6.3 EGU — Event generator unit . . . 94
6.3.1 Registers . . . 95
6.3.2 Electrical specification . . . 97
6.4 GPIO — General purpose input/output . . . 97
6.4.1 Pin configuration . . . 98
6.4.2 Pin sense mechanism . . . 99
6.4.3 GPIO security . . . 100
6.4.4 Registers . . . 102
6.4.5 Electrical specification . . . 106
6.5 GPIOTE — GPIO tasks and events . . . 107
6.5.1 Pin events and tasks . . . 107
6.5.2 Port event . . . 108
6.5.3 Tasks and events pin configuration . . . 108
6.5.4 Registers . . . 109
6.6 IPC — Interprocessor communication . . . 113
6.6.1 IPC and PPI connections . . . 115
6.6.2 Registers . . . 116
6.6.3 Electrical specification . . . 119
6.7 I2S — Inter-IC sound interface . . . 119
6.7.1 Mode . . . 120
6.7.2 Transmitting and receiving . . . 120
6.7.3 Left right clock (LRCK) . . . 121
6.7.4 Serial clock (SCK) . . . 121
6.7.5 Master clock (MCK) . . . 122
6.7.6 Width, alignment, and format . . . 123
6.7.7 EasyDMA . . . 124
6.7.8 Module operation . . . 126
6.7.9 Pin configuration . . . 128
6.7.10 Registers . . . 128
6.7.11 Electrical specification . . . 139
6.8 KMU — Key management unit . . . 139
6.8.1 Functional view . . . 140
6.8.2 Access control . . . 140
6.8.3 Protecting the UICR content . . . 141
6.8.4 Usage . . . 141
6.8.5 Registers . . . 145
6.9 PDM — Pulse density modulation interface . . . 149
6.9.1 Master clock generator . . . 149
6.9.2 Module operation . . . 150
6.9.3 Decimation filter . . . 150
6.9.4 EasyDMA . . . 150
6.9.5 Hardware example . . . 151
6.9.6 Pin configuration . . . 152

6.9.7 Registers . . . 152
6.9.8 Electrical specification . . . 161
6.10 PWM — Pulse width modulation . . . 161
6.10.1 Wave counter . . . 162
6.10.2 Decoder with EasyDMA . . . 165
6.10.3 Limitations . . . 173
6.10.4 Pin configuration . . . 173
6.10.5 Registers . . . 173
6.11 RTC — Real-time counter . . . 184
6.11.1 Clock source . . . 185
6.11.2 Resolution versus overflow and the prescaler . . . 185
6.11.3 Counter register . . . 186
6.11.4 Overflow . . . 186
6.11.5 Tick event . . . 187
6.11.6 Event control . . . 187
6.11.7 Compare . . . 187
6.11.8 Task and event jitter/delay . . . 189
6.11.9 Registers . . . 191
6.12 SAADC — Successive approximation analog-to-digital converter . . . 199
6.12.1 Overview . . . 199
6.12.2 Digital output . . . 200
6.12.3 Analog inputs and channels . . . 201
6.12.4 Operation modes . . . 201
6.12.5 EasyDMA . . . 203
6.12.6 Resistor ladder . . . 204
6.12.7 Reference . . . 205
6.12.8 Acquisition time . . . 205
6.12.9 Limits event monitoring . . . 206
6.12.10 Registers . . . 207
6.12.11 Electrical specification . . . 224
6.12.12 Performance factors . . . 225
6.13 SPIM — Serial peripheral interface master with EasyDMA . . . 225
6.13.1 SPI master transaction sequence . . . 226
6.13.2 Master mode pin configuration . . . 227
6.13.3 Shared resources . . . 228
6.13.4 EasyDMA . . . 228
6.13.5 Low power . . . 228
6.13.6 Registers . . . 229
6.13.7 Electrical specification . . . 240
6.14 SPIS — Serial peripheral interface slave with EasyDMA . . . 241
6.14.1 Shared resources . . . 242
6.14.2 EasyDMA . . . 242
6.14.3 SPI slave operation . . . 242
6.14.4 Semaphore operation . . . 244
6.14.5 Pin configuration . . . 245
6.14.6 Registers . . . 245
6.14.7 Electrical specification . . . 255
6.15 SPU — System protection unit . . . 257
6.15.1 General concepts . . . 257
6.15.2 Flash access control . . . 258
6.15.3 RAM access control . . . 261
6.15.4 Peripheral access control . . . 264
6.15.5 Pin access control . . . 266
6.15.6 DPPI access control . . . 266

6.15.7 External domain access control . . . 268
6.15.8 TrustZone for Cortex-M ID allocation . . . 269
6.15.9 Registers . . . 270
6.16 TIMER — Timer/counter . . . 279
6.16.1 Capture . . . 280
6.16.2 Compare . . . 280
6.16.3 Task delays . . . 280
6.16.4 Task priority . . . 280
6.16.5 Registers . . . 281
6.17 TWIM — I^2C compatible two-wire interface master with EasyDMA . . . 288
6.17.1 Shared resources . . . 289
6.17.2 EasyDMA . . . 289
6.17.3 Master write sequence . . . 290
6.17.4 Master read sequence . . . 290
6.17.5 Master repeated start sequence . . . 291
6.17.6 Low power . . . 292
6.17.7 Master mode pin configuration . . . 292
6.17.8 Registers . . . 293
6.17.9 Electrical specification . . . 307
6.17.10 Pullup resistor . . . 308
6.18 TWIS — I^2C compatible two-wire interface slave with EasyDMA . . . 308
6.18.1 Shared resources . . . 310
6.18.2 EasyDMA . . . 310
6.18.3 TWI slave responding to a read command . . . 311
6.18.4 TWI slave responding to a write command . . . 312
6.18.5 Master repeated start sequence . . . 313
6.18.6 Terminating an ongoing TWI transaction . . . 314
6.18.7 Low power . . . 314
6.18.8 Slave mode pin configuration . . . 314
6.18.9 Registers . . . 314
6.18.10 Electrical specification . . . 328
6.19 UARTE — Universal asynchronous receiver/transmitter with EasyDMA . . . 328
6.19.1 EasyDMA . . . 329
6.19.2 Transmission . . . 329
6.19.3 Reception . . . 330
6.19.4 Error conditions . . . 332
6.19.5 Using the UARTE without flow control . . . 332
6.19.6 Parity and stop bit configuration . . . 332
6.19.7 Low power . . . 332
6.19.8 Pin configuration . . . 333
6.19.9 Registers . . . 333
6.19.10 Electrical specification . . . 351
6.20 WDT — Watchdog timer . . . 351
6.20.1 Reload criteria . . . 351
6.20.2 Temporarily pausing the watchdog . . . 352
6.20.3 Watchdog reset . . . 352
6.20.4 Registers . . . 352
6.20.5 Electrical specification . . . 356

7 LTE modem . . . 357

7.1 SIM card interface . . . 358
7.2 LTE coexistence interface . . . 359
7.3 LTE RF control external interface . . . 360
7.4 RF front-end interface . . . 361

7.5 Registers . . . 361
7.6 Electrical specification . . . 361
7.6.1 Key RF parameters for Cat-M1 . . . 361
7.6.2 Key RF parameters for Cat-NB1 and Cat-NB2 . . . 361
7.6.3 Receiver parameters for Cat-M1 . . . 362
7.6.4 Receiver parameters for Cat-NB1 and Cat-NB2 . . . 362
7.6.5 Transmitter parameters for Cat-M1 . . . 362
7.6.6 Transmitter parameters for Cat-NB1 and Cat-NB2 . . . 362

8 DECT NR+ . . . 363

8.1 massive Machine Type Communication (mMTC) . . . 364
8.2 Ultra-Reliable Low-Latency Communication (URLLC) . . . 364
8.3 DECT NR+ on the nRF9161 . . . 364
8.4 Key RF Parameters . . . 364
8.5 DECT NR+ coexistence interface . . . 365

9 GPS receiver . . . 366

9.1 Electrical specification . . . 366

10 Debug and trace . . . 368

10.1 DAP - Debug access port . . . 368
10.2 Access port protection . . . 369
10.2.2 Registers . . . 371
10.3 Debug interface mode . . . 373
10.4 Real-time debug . . . 373
10.5 Registers . . . 373
10.5.1 TARGETID . . . 373
10.6 Electrical specification . . . 374
10.6.1 Trace port . . . 374
10.7 Trace . . . 374
10.7.1 ATB Funnel . . . 375
10.7.2 ATB Replicator . . . 382
10.7.3 ETB — Embedded trace buffer . . . 389
10.7.4 ETM — Embedded trace macrocell . . . 402
10.7.5 TPIU — Trace port interface unit . . . 423
10.8 CTRL-AP - Control access port . . . 437
10.8.1 Reset request . . . 438
10.8.2 Erase all . . . 438
10.8.3 Mailbox interface . . . 438
10.8.4 Disabling erase protection . . . 439
10.8.5 Debugger registers . . . 439
10.8.6 Registers . . . 443
10.9 TAD - Trace and debug control . . . 445
10.9.1 Registers . . . 445

11 Hardware and layout . . . 450

11.1 Pin assignments . . . 450
11.1.1 LGA pin assignments . . . 450
11.2 Mechanical specifications . . . 453
11.2.1 16.0 x 10.5 mm package . . . 453
11.3 Reference circuitry . . . 453
11.3.1 nRF9161 reference design . . . 454

11.4 Reflow conditions . . . 454
11.5 Shelf and floor life . . . 454

12 Operating conditions . . . 455
12.1 VDD_GPIO considerations . . . 455

13 Absolute maximum ratings . . . 456

14 Ordering information . . . 457
14.1 SiP marking . . . 457
14.2 Box labels . . . 457
14.3 Order code . . . 458
14.4 Code ranges and values . . . 459
14.5 Ordering options . . . 460

15 Regulatory information . . . 461
15.1 Certified bands . . . 461
15.2 Supported FCC/ISED rules . . . 462
15.3 FCC/ISED regulatory notices . . . 462
15.4 RF exposure considerations . . . 465
15.5 Host device manufacturer responsibility . . . 465
15.6 Antenna interface . . . 465
15.7 Antenna port test connector . . . 466
15.8 Reference Circuitry . . . 467

16 Legal notices . . . 487

1 Revision history

Date	Version	Description
May 2023	0.7	Limited release

2 About this document

This document is organized into chapters that are based on the modules and peripherals available in the IC.

2.1 Document status

The document status reflects the level of maturity of the document.

Document name	Description
Objective Product Specification (OPS)	Applies to document versions up to 1.0. This document contains target specifications for product development.
Product Specification (PS)	Applies to document versions 1.0 and higher. This document contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Table 1: Defined document names

2.2 Peripheral chapters

Every peripheral has a unique capitalized name or an abbreviation of its name, e.g. TIMER, used for identification and reference. This name is used in chapter headings and references, and it will appear in the Arm Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer to identify the peripheral.

The peripheral instance name, which is different from the peripheral name, is constructed using the peripheral name followed by a numbered postfix, starting with 0, for example, TIMER0. A postfix is normally only used if a peripheral can be instantiated more than once. The peripheral instance name is also used in the CMSIS to identify the peripheral instance.

The chapters describing peripherals may include the following information:

- A detailed functional description of the peripheral.
- The register configuration for the peripheral.
- The electrical specification tables, containing performance data which apply for the operating conditions described in Operating conditions on page 455.

2.2.2 Peripheral instantiation

The peripherals have a set of security capabilities listed in the instantiation tables.

The following table describes the abbreviations used.

Abbreviation	Description
NS	Trustzone/security attribute is Non-secure - The peripheral is always accessible as a Non-secure peripheral.
S	Trustzone/security attribute is Secure - The peripheral is always accessible as a Secure peripheral.
US	Trustzone Map is user selectable - The Trustzone/security attribute of the peripheral is configurable.
HF	Trustzone Map is Hardware Fixed - The Trustzone/security attribute of the peripheral cannot be changed.
NA	Not Applicable - Peripheral has no DMA capability.
NSA	NoSeparateAttribute - Peripheral with DMA and DMA transfer has the same security attribute as assigned to the peripheral.
SA	SeparateAttribute - Peripheral with DMA and DMA transfers can have a different security attribute than the one assigned to the peripheral.

Table 2: Instantiation table abbreviations

The Secure mapping column in the peripheral instantiation table defines configuration capabilities for the Arm TrustZone for Armv8-M secure attribute. The DMA security column describes the DMA capabilities of the peripheral.

The instantiation table has the following columns:

- Instance Column - Indicates the peripheral instance name followed by optional Trustzone attribute. A corresponding address is listed in Base address column indicating the base address for Secure and Non-secure Trustzone attribute. This optional Trustzone attribute is separated by a colon (:).
- Trustzone Column - This has 3 sub-columns indicating the Trustzone map, Trustzone attribute and DMA capability. The options are as listed in Instantiation table abbreviations on page 12.

2.3 Register tables

Individual registers are described using register tables. These tables are built up of two sections. The first three colored rows describe the position and size of the different fields in the register. The following rows describe the fields in more detail.

2.3.1 Fields and values

The **Id (Field Id)** row specifies the bits that belong to the different fields in the register. If a field has enumerated values, then every value will be identified with a unique value id in the **Value Id** column.

A blank space means that the field is reserved and read as undefined, and it also must be written as `0` to secure forward compatibility. If a register is divided into more than one field, a unique field name is specified for each field in the **Field** column. The **Value Id** may be omitted in the single-bit bit fields when values can be substituted with a Boolean type enumerator range, e.g. true/false, disable(d)/enable(d), on/off, and so on.

Values are usually provided as decimal or hexadecimal. Hexadecimal values have a `0x` prefix, decimal values have no prefix.

The **Value** column can be populated in the following ways:

- Individual enumerated values, for example 1, 3, 9.
- Range of values, e.g. [0..4], indicating all values from and including 0 and 4.

- Implicit values. If no values are indicated in the **Value** column, all bit combinations are supported, or alternatively the field's translation and limitations are described in the text instead.

If two or more fields are closely related, the **Value Id**, **Value**, and **Description** may be omitted for all but the first field. Subsequent fields will indicate inheritance with '..'.

A feature marked **Deprecated** should not be used for new designs.

2.3.2 Permissions

Different fields in a register might have different access permissions enforced by hardware.

The access permission for each register field is documented in the **Access** column in the following ways:

Access	Description	Hardware behavior
RO	Read-only	Field can only be read. A write will be ignored.
WO	Write-only	Field can only be written. A read will return an undefined value.
RW	Read-write	Field can be read and written multiple times.
W1	Write-once	Field can only be written once per reset. Any subsequent write will be ignored. A read will return an undefined value.
RW1	Read-write-once	Field can be read multiple times, but only written once per reset. Any subsequent write will be ignored.
W1C	Write 1 to clear	Field can be read multiple times. A one clears (set to zero) the corresponding bit in the register. Bits set to zero are ignored.
W1S	Write 1 to set	Field can be read multiple times. A one sets the corresponding bit in the register. Bits set to zero are ignored.

Table 3: Register field permission schemes

2.4 Registers

Register overview

Register	Offset	Description
DUMMY	0x514	Example of a register controlling a dummy feature

2.4.1 DUMMY

Address offset: 0x514

Example of a register controlling a dummy feature

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID								D	D	D	D						C	C	C								B							A	
Reset 0x00050002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field		Value ID				Value								Description																			
-A	RW	FIELD0														Example of a read-write field with several enumerated values																			
				Disabled				0								The example feature is disabled																			
				NormalMode				1								The example feature is enabled in normal mode																			
				ExtendedMode				2								The example feature is enabled along with extra functionality																			
B	RW	FIELD1														Example of a deprecated read-write field This field is deprecated.																			
				Disabled				0								The override feature is disabled																			
				Enabled				1								The override feature is enabled																			
C	RW	FIELD2														Example of a read-write field with a valid range of values																			
				ValidRange				[2..7]								Example of allowed values for this field																			
D	RW	FIELD3														Example of a read-write field with no restriction on the values																			

3 Product overview

The nRF9161 System-in-Package (SiP) is a low-power IoT (Internet of Things) solution integrating an Arm Cortex-M33 processor with advanced security features, a range of peripherals and a Low-Power Wide-Area (LPWA) network processor. The LPWA network processor can operate as a 5G DECT NR+ (NR+) device, independent of cellular network provider or as an LTE modem compliant with 3GPP LTE release 14 Cat-M1 and Cat-NB1/NB2 standards.

The LPWA network processor integrates a flexible transceiver with frequency range 700 MHz to 2200 MHz, through a single 50 Ω antenna pin and a baseband processor. NR+ or LTE operation is supported depending on which network protocol firmware the customer installs on the LPWA network processor of the nRF9161. Nordic Semiconductor provides firmware to support NR+ or LTE, layers L1-L3 and upper IP layers, providing a secure socket API to the application.

The nRF9161 LPWA network processor also integrate a GPS receiver, enabling local positioning support when supported by the installed firmware.

The Arm Cortex-M33 processor is exclusively for the user application, with 1 MB of flash and 256 kB of RAM dedicated for this. The M33 application processor shares the power, clock, and peripheral architecture with Nordic Semiconductor nRF5 Series of PAN/LAN SoCs, ensuring minimal porting efforts.

The peripheral set offers a variety of analog and digital functionality enabling single-chip implementation of a wide range of IoT applications. Arm TrustZone technology, CryptoCell 310 and supporting blocks for system protection and key management, are embedded to enable advanced security needed for IoT applications.

3.1 Block diagram

The block diagram illustrates the overall system. Arrows with white heads indicate signals that share physical pins with other signals.

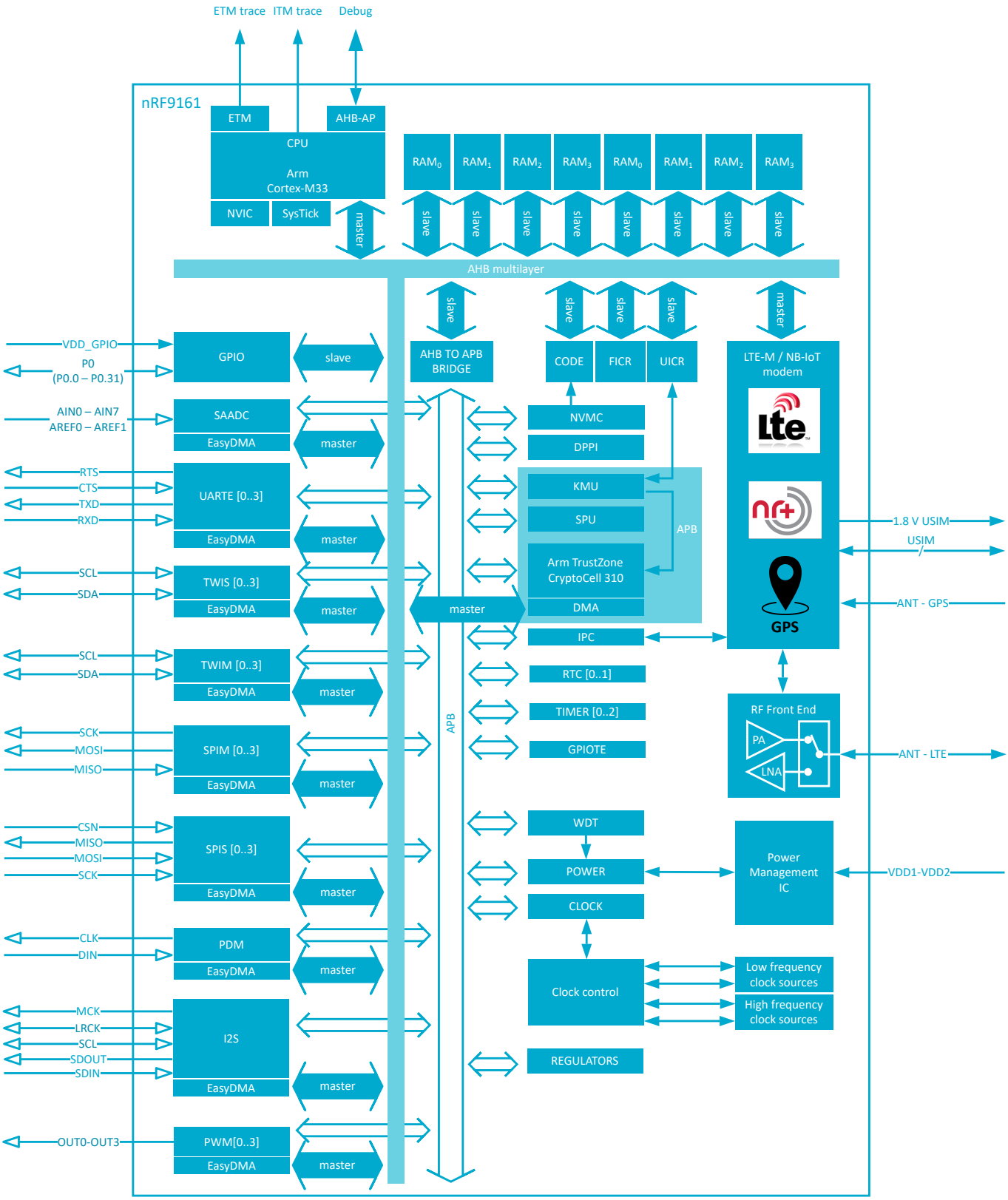

Figure 1: Block diagram

3.2 Peripheral interface

Peripherals are controlled by the CPU through configuration registers, as well as task and event registers. Task registers are inputs, enabling the CPU and other peripherals to initiate a functionality. Event registers

are outputs, enabling a peripheral to trigger tasks in other peripherals and/or the CPU by tying events to CPU interrupts.

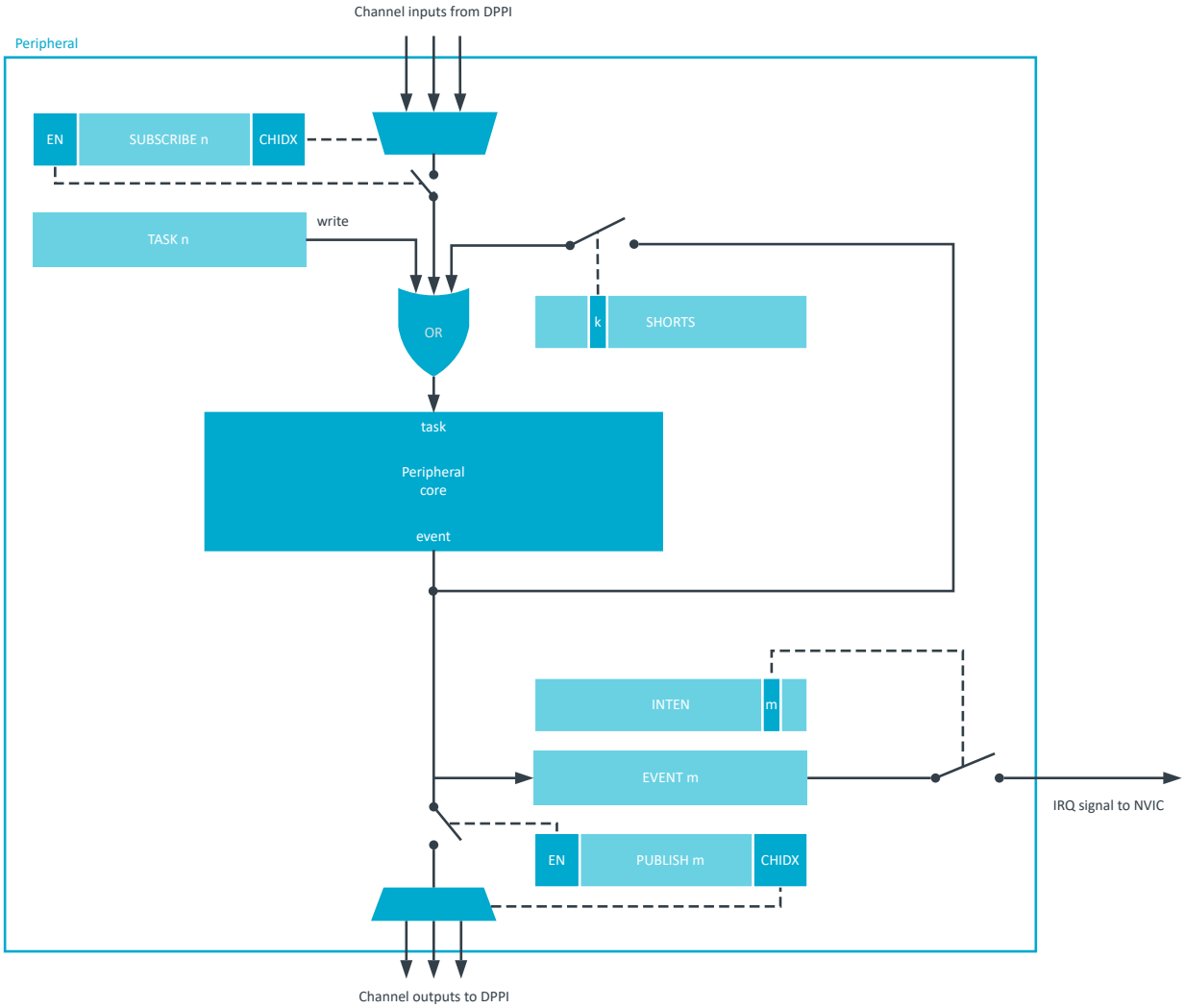

Figure 2: Peripheral interface

The distributed programmable peripheral interconnect (DPPI) feature enables peripherals to connect events to tasks without CPU intervention. For more information on DPPI and the DPPI channels, see DPPI - Distributed programmable peripheral interconnect on page 86.

3.2.1 Peripheral ID

Every peripheral is assigned a fixed block of 0x1000 bytes of address space, which is equal to 1024 x 32-bit registers.

See Instantiation on page 25 for more information about which peripherals are available and where they are located in the address map.

There is a direct relationship between peripheral ID and base address. For example, a peripheral with base address 0x40000000 is assigned ID=0, a peripheral with base address 0x40001000 is assigned ID=1, and a peripheral with base address 0x4001F000 is assigned ID=31.

Peripherals may share the same ID, which may impose one or more of the following limitations:

- Shared registers or common resources
- Limited availability due to mutually exclusive operation; only one peripheral in use at a time

- Enforced peripheral behavior when switching between peripherals (disable the first peripheral before enabling the second)

3.2.2 Peripherals with shared ID

In general (with the exception of ID 0), peripherals sharing an ID and base address may not be used simultaneously. Only one peripheral can be enabled at a given ID.

When switching between two peripherals sharing an ID, the following should be performed to prevent unwanted behavior:

1. Disable the previously used peripheral.
2. Disable any publish/subscribe connection to the DPPI system for the peripheral that is being disabled.
3. Clear all bits in the INTEN register, i.e. INTENCLR = 0xFFFFFFFF.
4. Explicitly configure the peripheral being enabled. Do not rely on inherited configuration from the disabled peripheral.
5. Enable the now configured peripheral.

For a list of which peripherals that share an ID see Instantiation on page 25.

3.2.3 Peripheral registers

Most peripherals feature an ENABLE register. Unless otherwise specified, the peripheral registers must be configured before enabling the peripheral.

PSEL registers need to be set before a peripheral is enabled or started. Updating PSEL registers while the peripheral is running has no effect. To connect a peripheral to a different GPIO, the following must be performed:

1. Disable the peripheral.
2. Update the PSEL register.
3. Re-enable the peripheral.

It takes four CPU cycles between the PSEL register update and the connection between a peripheral and a GPIO becoming effective.

> **Note:** The peripheral must be enabled before tasks and events can be used.

Most of the register values are lost during System OFF or when a reset is triggered. Some registers will retain their values in System OFF or for some specific reset sources. These registers are marked as retained in the register description for a given peripheral. For more information on their behavior, see chapter Reset on page 56.

3.2.4 Bit set and clear

Registers with multiple single-bit bit fields may implement the set-and-clear pattern. This pattern enables firmware to set and clear individual bits in a register without having to perform a read-modify-write operation on the main register.

This pattern is implemented using three consecutive addresses in the register map, where the main register is followed by dedicated SET and CLR registers (in that exact order).

In the main register, the SET register sets individual bits and the CLR register clears them. Writing `1` to a bit in the SET or CLR register will set or clear the same bit in the main register respectively. Writing `0` to a bit in the SET or CLR register has no effect. Reading the SET or CLR register returns the value of the main register.

> **Note:** The main register may not be visible and therefore not directly accessible in all cases.

3.2.5 Tasks

Tasks are used to trigger actions in a peripheral, such as to start a particular behavior. A peripheral can implement multiple tasks with each task having a separate register in that peripheral's task register group.

A task is triggered when firmware writes `1` to the task register, or when the peripheral itself or another peripheral toggles the corresponding task signal. See the figure Peripheral interface on page 16.

3.2.6 Events

Events are used to notify peripherals and the CPU about events that have happened, for example a state change in a peripheral. A peripheral may generate multiple events, where each event has a separate register in that peripheral's event register group.

An event is generated when the peripheral itself toggles the corresponding event signal, and the event register is updated to reflect that the event has been generated, see figure Peripheral interface on page 16. An event register is cleared when a `0` is written to it by firmware. Events can be generated by the peripheral even when the event register is set to `1`.

3.2.7 Publish and subscribe

Events and tasks from different peripherals can be connected together through the DPPI system using the PUBLISH and SUBSCRIBE registers in each peripheral. See Peripheral interface on page 16. An event can be published onto a DPPI channel by configuring the event's PUBLISH register. Similarly, a task can subscribe to a DPPI channel by configuring the task's SUBSCRIBE register.

See DPPI - Distributed programmable peripheral interconnect on page 86 for details.

3.2.8 Shortcuts

A shortcut is a direct connection between an event and a task within the same peripheral. If a shortcut is enabled, the associated task is automatically triggered when its associated event is generated.

Using shortcuts is equivalent to making the connection outside the peripheral and through the DPPI. However, the propagation delay when using shortcuts is usually shorter than the propagation delay through the DPPI.

Shortcuts are predefined, which means that their connections cannot be configured by firmware. Each shortcut can be individually enabled or disabled through the shortcut register, one bit per shortcut, giving a maximum of 32 shortcuts for each peripheral.

3.2.9 Interrupts

All peripherals support interrupts which are generated by events.

A peripheral only occupies one interrupt, and the interrupt number follows the peripheral ID. For example, the peripheral with ID=4 is connected to interrupt number 4 in the nested vectored interrupt controller (NVIC).

Using registers INTEN, INTENSET, and INTENCLR, every event generated by a peripheral can be configured to generate that peripheral's interrupt. Multiple events can be enabled to generate interrupts simultaneously. To resolve the correct interrupt source, the event registers in the event group of peripheral registers will indicate the source.

Some peripherals implement only INTENSET and INTENCLR registers, and the INTEN register is not available on those peripherals. See the individual peripheral chapters for details. In all cases, reading back the INTENSET or INTENCLR register returns the same information as in INTEN.

Each event implemented in the peripheral is associated with a specific bit position in the INTEN, INTENSET, and INTENCLR registers.

The relationship between tasks, events, shortcuts, and interrupts is illustrated in figure Peripheral interface on page 16.

3.2.9.1 Interrupt clearing and disabling

Interrupts should always be cleared by writing 0 to the corresponding EVENT register.

Until cleared, interrupts will immediately be re-triggered and cause software interrupt service routines to be executed repeatedly.

Because the clearing of the EVENT register may take a number of CPU clock cycles, the program should perform a read from the EVENT register that has been cleared before exiting the interrupt service routine. This will ensure that the EVENT clearing has taken place before the interrupt service routine is exited. Care should be taken to ensure that the compiler does not remove the read operation as an optimization.

Similarly, when disabling an interrupt inside an interrupt service routine, the program should perform a read from the INTEN or INTENCLR registers to ensure that the interrupt is disabled before exiting the interrupt service routine.

3.2.10 Secure/non-secure peripherals

For some peripherals, the security configuration can change from secure to non-secure, or vice versa. Care must be taken when changing the security configuration of a peripheral, to prevent security information leakage and ensure correct operation.

The following sequence should be followed, where applicable, when configuring and changing the security settings of a peripheral in the SPU — System protection unit on page 257.

1. Stop peripheral operation.
2. Disable the peripheral.
3. Remove pin connections.
4. Disable DPPI connections.
5. Clear sensitive registers (e.g. writing back default values).
6. Change peripheral security setting in the SPU — System protection unit on page 257.
7. Re-enable the peripheral.

Note: Changing security settings on a peripheral during runtime is not advisable.

4 Application core

The nRF9161 application core has a modern and powerful Arm Cortex-M33 with on-chip flash and RAM exclusively for application use.

4.1 CPU

The Arm Cortex-M33 processor has a 32-bit instruction set (Thumb®-2 technology) that implements a superset of 16 and 32-bit instructions to maximize code density and performance.

This processor implements several features that enable energy-efficient arithmetic and high-performance signal processing, including:

- Digital signal processing (DSP) instructions
- Single-cycle multiply and accumulate (MAC) instructions
- Hardware divide
- 8- and 16-bit single instruction, multiple data (SIMD) instructions
- Single-precision floating-point unit (FPU)
- Memory Protection Unit (MPU)
- Arm TrustZone for ARMv8-M

The Arm Cortex Common Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the Arm Cortex processor series is implemented and available for the M33 CPU.

Real-time execution is highly deterministic in thread mode, to and from sleep modes, and when handling events at configurable priority levels via the nested vectored interrupt controller (NVIC).

Executing code from internal or external flash will have a wait state penalty. The instruction cache can be enabled to minimize flash wait states when fetching instructions. For more information on cache, see Cache on page 31. The section Electrical specification on page 21 shows CPU performance parameters including the wait states in different modes, CPU current and efficiency, and processing power and efficiency based on the CoreMark® benchmark.

4.1.1 Floating-point interrupt

The floating-point unit (FPU) might generate exceptions when used (for example, due to overflow or underflow), which trigger the FPU interrupt.

See Instantiation on page 25 for more information about which exception number (peripheral ID) is triggered by an FPU exception.

The FPU is not affected by any security configuration. It is presented as non-secure in register PERIPHID[n].PERM. See SPU — System protection unit on page 257 for more information.

To clear the IRQ (interrupt request) line when an exception occurs, the relevant exception bit within the floating-point status and control register (FPSCR) must be cleared. For more information about the FPSCR or other FPU registers, see the *Arm Cortex-M33 Devices Generic User Guide*.

4.1.2 CPU and support module configuration

The Arm Cortex-M33 processor has a number of CPU options and support modules implemented on the device.

Option / Module	Description	Implemented
Core options		
NVIC	Nested vectored interrupt controller	YES
PRIORITIES	Priority bits	3
WIC	Wake-up interrupt controller	NO
Endianness	Memory system endianness	Little endian
DWT	Data watchpoint and trace	YES
Modules		
MPU_NS	Number of non-secure memory protection unit (MPU) regions	16
MPU_S	Number of secure MPU regions	16
SAU	Number of security attribution unit (SAU) regions	0, see SPU for more information about secure regions.
FPU	Floating-point unit	YES
DSP	Digital signal processing extension	YES
ARMv8-M TrustZone	ARMv8-M security extensions	YES
CPIF	Co-processor interface	NO
ETM	Embedded trace macrocell	YES
ITM	Instrumentation trace macrocell	YES
MTB	Micro trace buffer	NO
CTI	Cross trigger interface	YES
BPU	Breakpoint unit	YES
HTM	AMBA® AHB trace macrocell	NO

4.1.3 Electrical specification

4.1.3.1 CPU performance

The CPU clock speed is 64 MHz. Current and efficiency data is taken when in System ON and the CPU is executing the CoreMark benchmark. It includes power regulator and clock base currents. All other blocks are IDLE.

Symbol	Description	Min.	Typ.	Max.	Units
W_{FLASH}	CPU wait states, running from flash, cache disabled	0		4	
$W_{FLASHCACHE}$	CPU wait states, running from flash, cache enabled	0		2	
W_{RAM}	CPU wait states, running from RAM			0	
CM_{FLASH}	CoreMark[1], running from flash, cache enabled		247		CoreMark
$CM_{FLASH/MHz}$	CoreMark per MHz, running from flash, cache enabled		3.86		CoreMark/MHz
$CM_{FLASH/mA}$	CoreMark per mA, running from flash, cache enabled		91		CoreMark/mA

4.2 Memory

The application microcontroller has embedded 1024 kB flash and 256 kB RAM for application code and data storage.

As illustrated in Memory layout on page 22, both CPU and EasyDMA are able to access RAM via the AHB multilayer interconnect. See AHB multilayer interconnect on page 46 and EasyDMA on page 43 for more information about AHB multilayer interconnect and EasyDMA respectively. The LTE modem can access all application MCU memory, but typically a small portion of RAM is dedicated to data exchange between application MCU and the modem baseband controller.

[1] Using armclang compiler

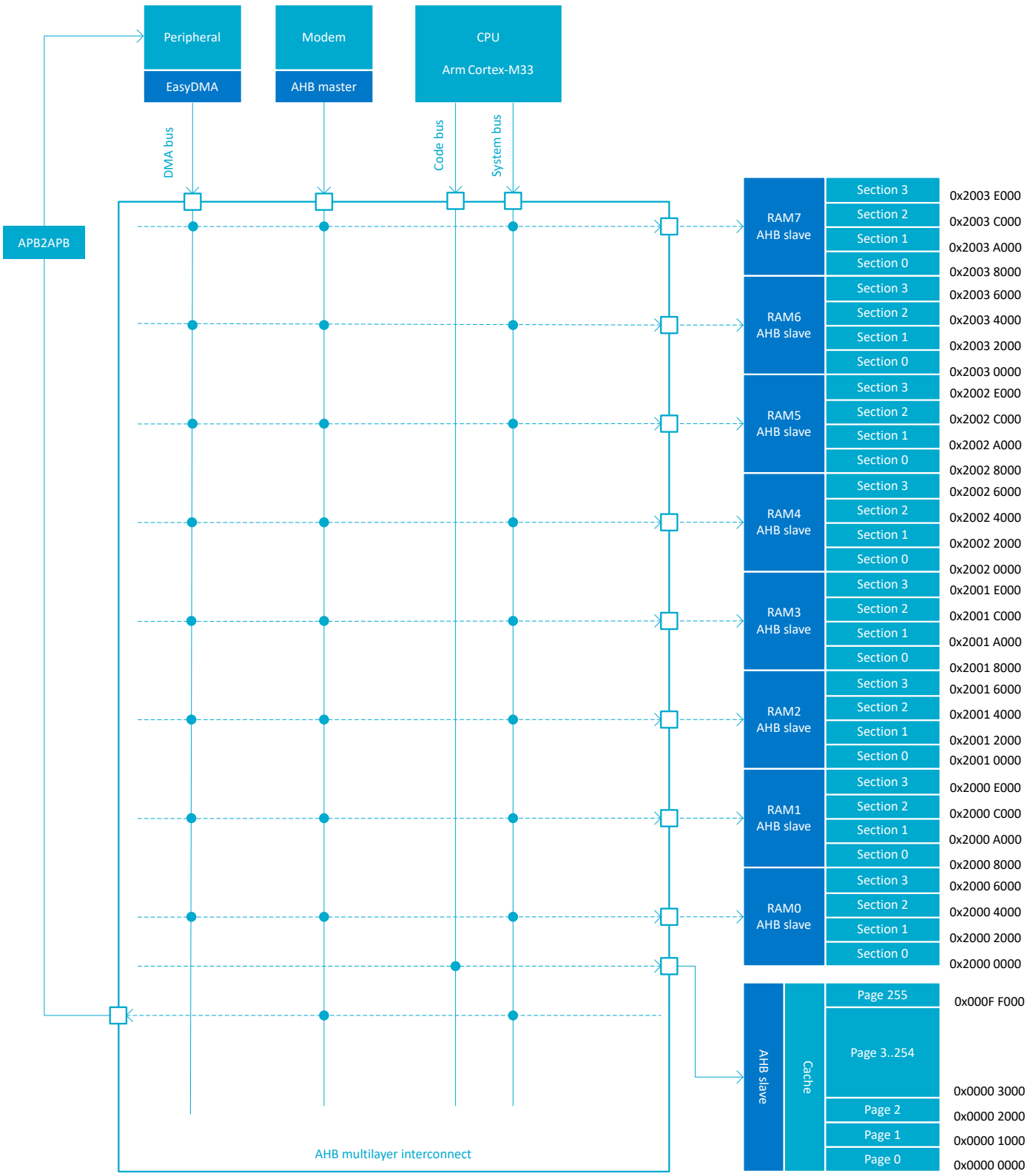

Figure 3: Memory layout

RAM - Random access memory

RAM can be read and written an unlimited number of times by the CPU and the EasyDMA.

Each RAM AHB slave is connected to one or more RAM sections. See Memory layout on page 22 for more information.

The RAM blocks power states and retention states in System ON and System OFF modes are controlled by the VMC.

Flash - Non-volatile memory

Flash can be read an unlimited number of times by the CPU and is accessible via the AHB interface connected to the CPU, see Memory layout on page 22 for more information. There are restrictions on the number of times flash can be written and erased, and also on how it can be written. For more information, see Absolute maximum ratings on page 456. Writing to flash is managed by the non-volatile memory controller (NVMC).

4.2.1 Memory map

All memory and registers are found in the same address space, as illustrated in the device memory map below.

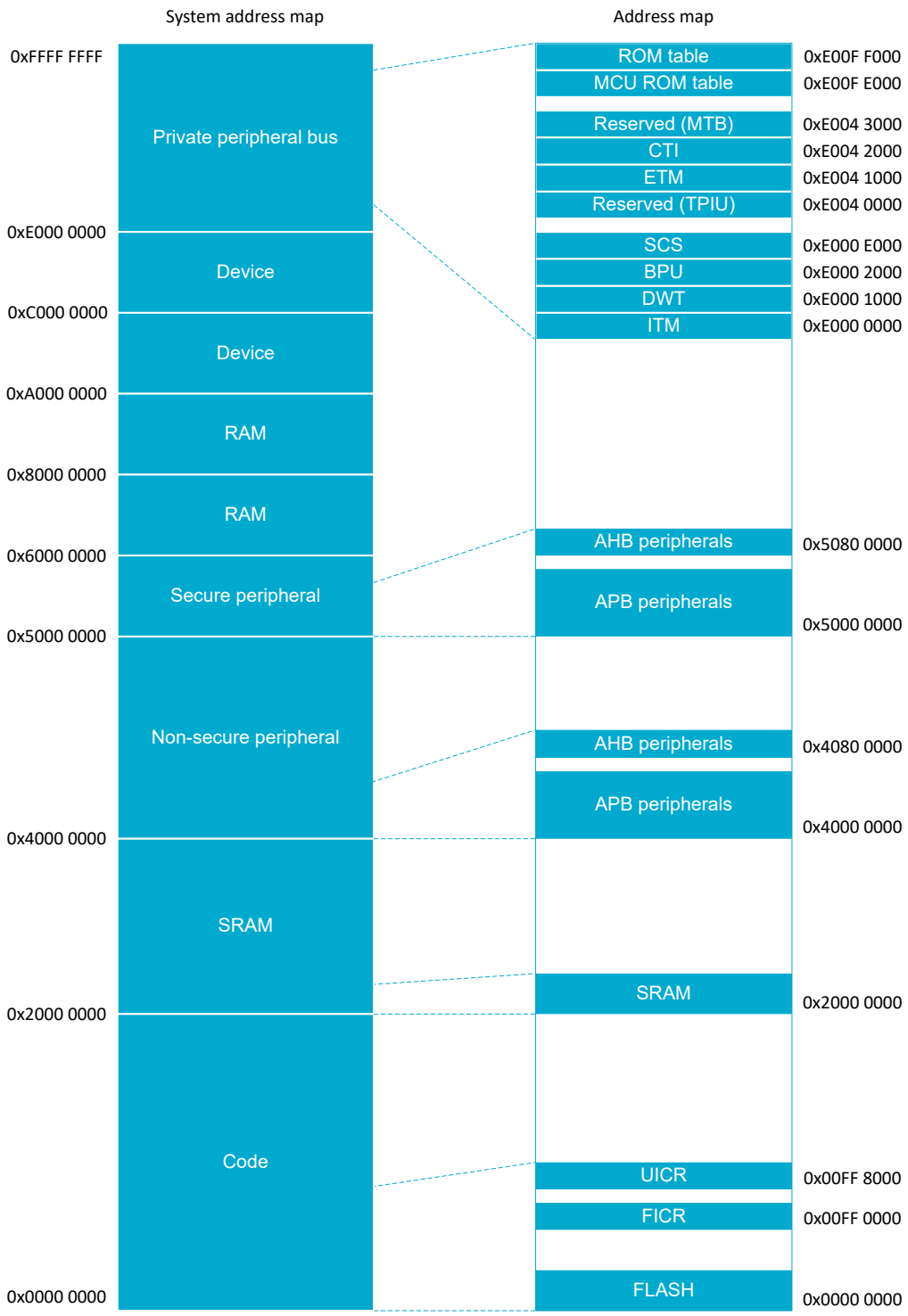

Figure 4: Memory map

Some of the registers are retained (their values kept). Read more about retained registers in Retained registers on page 57 and Reset behavior on page 57.

4.2.2 Instantiation

ID	Base address	Instance	TrustZone			Split access	Description
			Map	Att	DMA		
3	0x50003000	SPU	HF	S	NA	No	System Protection Unit
4	0x50004000 0x40004000	REGULATORS : S REGULATORS : NS	US	NS	NA	No	Regulator configuration
5	0x50005000 0x40005000	CLOCK : S CLOCK : NS	US	NS	NA	No	Clock control
5	0x50005000 0x40005000	POWER : S POWER : NS	US	NS	NA	No	Power control
6	0x50006000	CTRL_AP_PERI	HF	S	NA	No	CTRL-AP-PERI
8	0x50008000 0x40008000	SPIM0 : S SPIM0 : NS	US	NS	SA	No	SPI master 0
8	0x50008000 0x40008000	SPIS0 : S SPIS0 : NS	US	NS	SA	No	SPI slave 0
8	0x50008000 0x40008000	TWIM0 : S TWIM0 : NS	US	NS	SA	No	Two-wire interface master 0
8	0x50008000 0x40008000	TWIS0 : S TWIS0 : NS	US	NS	SA	No	Two-wire interface slave 0
8	0x50008000 0x40008000	UARTE0 : S UARTE0 : NS	US	NS	SA	No	Universal asynchronous receiver/transmitter with EasyDMA 0
9	0x50009000 0x40009000	SPIM1 : S SPIM1 : NS	US	NS	SA	No	SPI master 1
9	0x50009000 0x40009000	SPIS1 : S SPIS1 : NS	US	NS	SA	No	SPI slave 1
9	0x50009000 0x40009000	TWIM1 : S TWIM1 : NS	US	NS	SA	No	Two-wire interface master 1
9	0x50009000 0x40009000	TWIS1 : S TWIS1 : NS	US	NS	SA	No	Two-wire interface slave 1
9	0x50009000 0x40009000	UARTE1 : S UARTE1 : NS	US	NS	SA	No	Universal asynchronous receiver/transmitter with EasyDMA 1
10	0x5000A000 0x4000A000	SPIM2 : S SPIM2 : NS	US	NS	SA	No	SPI master 2
10	0x5000A000 0x4000A000	SPIS2 : S SPIS2 : NS	US	NS	SA	No	SPI slave 2
10	0x5000A000 0x4000A000	TWIM2 : S TWIM2 : NS	US	NS	SA	No	Two-wire interface master 2
10	0x5000A000 0x4000A000	TWIS2 : S TWIS2 : NS	US	NS	SA	No	Two-wire interface slave 2
10	0x5000A000 0x4000A000	UARTE2 : S UARTE2 : NS	US	NS	SA	No	Universal asynchronous receiver/transmitter with EasyDMA 2
11	0x5000B000 0x4000B000	SPIM3 : S SPIM3 : NS	US	NS	SA	No	SPI master 3
11	0x5000B000 0x4000B000	SPIS3 : S SPIS3 : NS	US	NS	SA	No	SPI slave 3
11	0x5000B000 0x4000B000	TWIM3 : S TWIM3 : NS	US	NS	SA	No	Two-wire interface master 3
11	0x5000B000 0x4000B000	TWIS3 : S TWIS3 : NS	US	NS	SA	No	Two-wire interface slave 3
11	0x5000B000 0x4000B000	UARTE3 : S UARTE3 : NS	US	NS	SA	No	Universal asynchronous receiver/transmitter with EasyDMA 3
13	0x5000D000	GPIOTE0	HF	S	NA	No	Secure GPIO tasks and events

ID	Base address	Instance	TrustZone			Split access	Description
			Map	Att	DMA		
14	0x5000E000 0x4000E000	SAADC : S SAADC : NS	US	NS	SA	No	Analog to digital converter
15	0x5000F000 0x4000F000	TIMER0 : S TIMER0 : NS	US	NS	NA	No	Timer 0
16	0x50010000 0x40010000	TIMER1 : S TIMER1 : NS	US	NS	NA	No	Timer 1
17	0x50011000 0x40011000	TIMER2 : S TIMER2 : NS	US	NS	NA	No	Timer 2
20	0x50014000 0x40014000	RTC0 : S RTC0 : NS	US	NS	NA	No	Real time counter 0
21	0x50015000 0x40015000	RTC1 : S RTC1 : NS	US	NS	NA	No	Real time counter 1
23	0x50017000 0x40017000	DPPIC : S DPPIC : NS	HF	NS	NA	Yes	DPPI configuration
24	0x50018000 0x40018000	WDT : S WDT : NS	US	NS	NA	No	Watchdog timer
27	0x5001B000 0x4001B000	EGU0 : S EGU0 : NS	US	NS	NA	No	Event generator unit 0
28	0x5001C000 0x4001C000	EGU1 : S EGU1 : NS	US	NS	NA	No	Event generator unit 1
29	0x5001D000 0x4001D000	EGU2 : S EGU2 : NS	US	NS	NA	No	Event generator unit 2
30	0x5001E000 0x4001E000	EGU3 : S EGU3 : NS	US	NS	NA	No	Event generator unit 3
31	0x5001F000 0x4001F000	EGU4 : S EGU4 : NS	US	NS	NA	No	Event generator unit 4
32	0x50020000 0x40020000	EGU5 : S EGU5 : NS	US	NS	NA	No	Event generator unit 5
33	0x50021000 0x40021000	PWM0 : S PWM0 : NS	US	NS	SA	No	Pulse width modulation unit 0
34	0x50022000 0x40022000	PWM1 : S PWM1 : NS	US	NS	SA	No	Pulse width modulation unit 1
35	0x50023000 0x40023000	PWM2 : S PWM2 : NS	US	NS	SA	No	Pulse width modulation unit 2
36	0x50024000 0x40024000	PWM3 : S PWM3 : NS	US	NS	SA	No	Pulse width modulation unit 3
38	0x50026000 0x40026000	PDM : S PDM : NS	US	NS	SA	No	Pulse density modulation (digital microphone) interface
40	0x50028000 0x40028000	I2S : S I2S : NS	US	NS	SA	No	Inter-IC Sound
42	0x5002A000 0x4002A000	IPC : S IPC : NS	US	NS	NA	No	Interprocessor communication
44	0x4002C000	FPU	HF	NS	NA	No	Floating-point unit
49	0x40031000	GPIOTE1	HF	NS	NA	No	Non Secure GPIO tasks and events
57	0x50039000 0x40039000	APPROTECT : S APPROTECT : NS	HF	NS	NA	Yes	APPROTECT control
57	0x50039000 0x40039000	KMU : S KMU : NS	HF	NS	NA	Yes	Key management unit
57	0x50039000 0x40039000	NVMC : S NVMC : NS	HF	NS	NA	Yes	Non-volatile memory controller
58	0x5003A000 0x4003A000	VMC : S VMC : NS	US	NS	NA	No	Volatile memory controller

ID	Base address	Instance	TrustZone			Split access	Description
			Map	Att	DMA		
64	0x50840000	CC_HOST_RGF	HF	S	NSA	No	Host platform interface
64	0x50840000	CRYPTOCELL	HF	S	NSA	No	CryptoCell sub-system control interface
66	0x50842500 0x40842500	P0 : S P0 : NS	HF	NS	NA	Yes	General purpose input and output
N/A	0x00FF0000	FICR	HF	S	NA	No	Factory information configuration
N/A	0x00FF8000	UICR	HF	S	NA	No	User information configuration
N/A	0xE0041000	ETM	HF	NS	NA	No	ETM
N/A	0xE0051000	ETB	HF	NS	NA	No	ETB
N/A	0xE0054000	TPIU	HF	NS	NA	No	TPIU
N/A	0xE0058000	ATBREPLICATOR	HF	NS	NA	No	ATBREPLICATOR
N/A	0xE005A000	ATBFUNNEL1	HF	NS	NA	No	ATBFUNNEL unit 1
N/A	0xE005B000	ATBFUNNEL2	HF	NS	NA	No	ATBFUNNEL unit 2
N/A	0xE0080000	TAD	HF	S	NA	No	Trace and debug control

Table 4: Instantiation table

4.2.3 Peripheral access control capabilities

Information about the peripheral access control capabilities can be found in the instantiation table.

The instantiation table has two columns containing the information about access control capabilities for a peripheral:

- Secure mapping: This column defines configuration capabilities for TrustZone-M secure attribute.
- DMA security: This column indicates whether the peripheral has DMA capabilities, and if DMA transfer can be assigned to a different security attribute than the peripheral itself.

For details on options in secure mapping column and DMA security column, see the following tables respectively.

Abbreviation	Description
NS	Non-secure: This peripheral is always accessible as a non-secure peripheral.
S	Secure: This peripheral is always accessible as a secure peripheral.
US	User-selectable: Non-secure or secure attribute for this peripheral is defined by the PERIPHID[0].PERM register.
SPLIT	Both non-secure and secure: The same resource is shared by both secure and non-secure code.

Table 5: Secure mapping column options

Abbreviation	Description
NA	Not applicable: Peripheral has no DMA capability.
NSA	No separate attribute: Peripheral has DMA, and DMA transfers always have the same security attribute as assigned to the peripheral.
SA	Separate attribute: Peripheral has DMA, and DMA transfers can have a different security attribute than the one assigned to the peripheral.

Table 6: DMA security column options

4.3 VMC — Volatile memory controller

The volatile memory controller (VMC) provides power control of RAM blocks.

Each of the available RAM blocks, which can contain multiple RAM sections, can be turned on or off independently in System ON mode, using the RAM[n]registers. These registers also control if a RAM block, or some of its sections, is retained in System OFF mode. See Memory chapter for more information about RAM blocks and sections.

> **Note:** Powering up a RAM block takes typically 10 cycles. Thus, it is recommended reading the POWER register before accessing a RAM block that has been recently powered on.

4.3.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
VMC : S	0x5003A000	US	NS	NA	No	Volatile memory controller
VMC : NS	0x4003A000					

Register overview

Register	Offset	TZ	Description
RAM[n].POWER	0x600		RAMn power control register
RAM[n].POWERSET	0x604		RAMn power control set register
RAM[n].POWERCLR	0x608		RAMn power control clear register

4.3.1.1 RAM[n].POWER (n=0..7)

Address offset: 0x600 + (n × 0x10)

RAMn power control register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID													H	G	F	E													D	C	B	A
Reset 0x0000FFFF	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	R/W	Field	Value ID	Value	Description
A-D	RW	S[i]POWER (i=0..3)			Keep RAM section Si of RAM n on or off in System ON mode All RAM sections will be switched off in System OFF mode
			Off	0	Off
			On	1	On
E-H	RW	S[i]RETENTION (i=0..3)			Keep retention on RAM section Si of RAM n when RAM section is switched off
			Off	0	Off
			On	1	On

4.3.1.2 RAM[n].POWERSET (n=0..7)

Address offset: 0x604 + (n × 0x10)

RAMn power control set register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																H	G	F	E													D	C	B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A-D	W	S[i]POWER (i=0..3)																																	
			On	1																															
E-H	W	S[i]RETENTION (i=0..3)																																	
			On	1																															

Keep RAM section Si of RAM n on or off in System ON mode

On

Keep retention on RAM section Si of RAM n when RAM section is switched off

On

4.3.1.3 RAM[n].POWERCLR (n=0..7)

Address offset: 0x608 + (n × 0x10)

RAMn power control clear register

When read, this register will return the value of the POWER register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																H	G	F	E													D	C	B	A
Reset 0x0000FFFF				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A-D	W	S[i]POWER (i=0..3)																																	
			Off	1																															
E-H	W	S[i]RETENTION (i=0..3)																																	
			Off	1																															

Keep RAM section Si of RAM n on or off in System ON mode

Off

Keep retention on RAM section Si of RAM n when RAM section is switched off

Off

4.4 NVMC — Non-volatile memory controller

The non-volatile memory controller (NVMC) is used for writing and erasing of the internal flash memory and the user information configuration register (UICR).

The NVMC is a split security peripheral. This means that when the NVMC is configured as non-secure, only a subset of the registers is available from the non-secure code. See SPU — System protection unit on page 257 and Registers on page 32 for more details.

When the NVMC is configured to be a secure peripheral, only secure code has access.

Before a write can be performed, the NVMC must be enabled for writing in CONFIG.WEN. Similarly, before an erase can be performed, the NVMC must be enabled for erasing in CONFIG.EEN, see CONFIG on page 33. The user must make sure that writing and erasing are not enabled at the same time. Failing to do so may result in unpredictable behavior.

4.4.1 Writing to flash

When writing is enabled, in CONFIG register for secure region, or in CONFIGNS register for non-secure region, flash is written by writing a full 32-bit word to a word-aligned address in flash.

Secure code has access to both secure and non-secure regions, by using the appropriate configuration of CONFIG and CONFIGNS registers. Non-secure code, in contrast, has access to non-secure regions only. Thus, non-secure code only needs CONFIGNS.

The NVMC is only able to write '0' to erased bits in flash, that is bits set to '1'. It cannot write a bit back to '1'.

As illustrated in Memory on page 21, flash is divided into multiple pages. The same address in flash can only be written n_{WRITE} number of times before a page erase must be performed.

Only full 32-bit words can be written to flash using the NVMC interface. To write less than 32 bits to flash, write the data as a word, and set all the bits that should remain unchanged in the word to '1'. Note that the restriction about the number of writes (see above) still applies in this case.

The time it takes to write a word to flash is specified by t_{WRITE}. If CPU executes code from flash while the NVMC is writing to flash, the CPU will be stalled.

Only word-aligned writes are allowed. Byte or half-word-aligned writes will result in a bus fault.

4.4.2 Erasing a secure page in flash

When secure region erase is enabled (in CONFIG register), a flash page can be erased by writing 0xFFFFFFFF into the first 32-bit word in a flash page.

Page erase is only applicable to the code area in the flash and does not work with UICR.

After erasing a flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is stalled if the CPU executes code from the flash while the NVMC performs the erase operation.

See Partial erase of a page in flash for information on splitting the erase time in smaller chunks.

4.4.3 Erasing a non-secure page in flash

When non-secure region erase is enabled, a non-secure flash page can be erased by writing 0xFFFFFFFF into the first 32-bit word of the flash page.

Page erase is only applicable to the code area in the flash and does not work with UICR.

After erasing a flash page, all bits in the page are set to '1'. The time it takes to erase a page is specified by $t_{ERASEPAGE}$. The CPU is stalled if the CPU executes code from the flash while the NVMC performs the erase operation.

4.4.4 Writing to user information configuration registers (UICR)

User information configuration registers (UICR) are written in the same way as flash. After UICR has been written, the new UICR configuration only takes effect after a reset.

UICR is only accessible by secure code. Any write from non-secure code will be faulted.

In order to lock the chip after uploading non-secure code, a simple sequence must be followed:

1. Block access to secure code by setting UICR register SECUREAPPROTECT on page 41 to protected
2. Use the WRITEUICRNS on page 35 register, via non-secure debugger, in order to set APPROTECT (APPROTECT is automatically written to 0x00000000 by the NVMC)

UICR can only be written n_{WRITE} number of times before an erase must be performed using ERASEALL.

The time it takes to write a word to the UICR is specified by t_{WRITE}. The CPU is stalled if the CPU executes code from the flash while the NVMC is writing to the UICR.

4.4.5 Erase all

When erase is enabled, the whole flash and UICR can be erased in one operation by using the ERASEALL register. ERASEALL does not erase the factory information configuration registers (FICR).

This functionality can be blocked by some configuration of the UICR protection bits, see the table NVMC protection (1 - Enabled, 0 - Disabled, X - Don't care) on page 31.

The time it takes to perform an ERASEALL on page 33 command is specified by $t_{ERASEALL}$. The CPU is stalled if the CPU executes code from the flash while the NVMC performs the erase operation.

4.4.6 NVMC protection mechanisms

This chapter describes the different protection mechanisms for the non-volatile memory.

4.4.6.1 NVMC blocking

UICR integrity is assured through use of multiple levels of protection. UICR protection bits can be configured to allow or block certain operations.

The table below shows the different statuses of UICR protection bits, and which operations are allowed or blocked.

UICR protection bit status			NVMC protection	
SECUREAPPROTECT	APPROTECT	ERASEPROTECT	CTRL-AP ERASEALL	NVMC ERASEALL
0	0	0	Available	Available
1	X	0	Available	Blocked
X	1	0	Available	Blocked
X	X	1	Blocked	Blocked

Table 7: NVMC protection (1 - Enabled, 0 - Disabled, X - Don't care)

Note: Erase can still be performed through CTRL-AP, regardless of the above settings. See CTRL-AP - Control access port on page 437 for more information.

Uploading code with secure debugging blocked

Non-secure code can program non-secure flash regions. In order to perform these operations, the NVMC has the following non-secure registers: CONFIGNS, READY and READYNEXT.

Register CONFIGNS on page 34 works as the CONFIG register but it is used only for non-secure transactions. Both page erase and writing to flash require a write transaction (see Erasing a secure page in flash on page 30 or Erasing a non-secure page in flash on page 30). The SPU — System protection unit on page 257 prevents non-secure code from writing to a secure page since the transaction will never reach the NVMC controller.

4.4.6.2 NVMC power failure protection

NVMC power failure protection is possible using a power-fail comparator which monitors the power supply. If the power-fail comparator is enabled, and the power supply voltage is below V_{POF} threshold, the comparator prevents the NVMC from performing erase or write operations in non-volatile memory (NVM).

If a power failure warning is present at the start of an NVM write or erase operation, the NVMC blocks the operation and a bus error is signaled.

If the power failure warning occurs during an ongoing NVM write operation, the NVMC will try to finish the operation. However, if the power failure warning persists, consecutive NVM write operations are blocked by the NVMC, and a bus error is signaled.

If a power failure warning occurs during an NVM erase operation, the operation is aborted and a bus error is signaled.

4.4.7 Cache

An instruction cache (I-Cache) can be enabled for the ICODE bus in the NVMC.

See Memory map on page 23 for the location of flash.

A cache hit is an instruction fetch from the cache, and it has a 0 wait-state delay. The number of wait-states for a cache miss, where the instruction is not available in the cache and needs to be fetched from flash, depends on the processor frequency, see CPU parameter W_FLASHCACHE.

Enabling the cache can increase the CPU performance and reduce power consumption, by reducing the number of wait cycles and the number of flash accesses. This depends on the cache hit rate. Cache draws current when enabled. If the reduction in average current due to reduced flash accesses is larger than the cache power requirement, the average current to execute the program code is reduced.

When disabled, the cache does not draw current and its content is not retained.

It is possible to enable cache profiling to analyze the performance of the cache for your program using the register ICACHECNF. When profiling is enabled, registers IHIT and IMISS are incremented for every instruction cache hit or miss respectively.

4.4.8 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
NVMC : S	0x50039000	HF	NS	NA	Yes	Non-volatile memory controller
NVMC : NS	0x40039000					

Register overview

Register	Offset	TZ	Description
READY	0x400	NS	Ready flag
READYNEXT	0x408	NS	Ready flag
CONFIG	0x504	S	Configuration register
ERASEALL	0x50C	S	Register for erasing all non-volatile user memory
ERASEPAGEPARTIALCFG	0x51C	S	Register for partial erase configuration
ICACHECNF	0x540	S	I-code cache configuration register
IHIT	0x548	S	I-code cache hit counter
IMISS	0x54C	S	I-code cache miss counter
CONFIGNS	0x584	NS	
WRITEUICRNS	0x588	NS	Non-secure APPROTECT enable register

4.4.8.1 READY

Address offset: 0x400

Ready flag

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000001	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

ID	R/W	TZ	Field	Value ID	Value	Description
A	R		READY			NVMC is ready or busy
				Busy	0	NVMC is busy (on-going write or erase operation)
				Ready	1	NVMC is ready

4.4.8.2 READYNEXT

Address offset: 0x408

Ready flag

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000001	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

ID	R/W	TZ	Field	Value ID	Value	Description
A	R		READYNEXT			NVMC can accept a new write operation
				Busy	0	NVMC cannot accept any write operation
				Ready	1	NVMC is ready

4.4.8.3 CONFIG

Address offset: 0x504

Configuration register

Note: This register is one hot

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	RW		WEN			Program memory access mode. It is strongly recommended to only activate erase and write modes when they are actively used. Enabling write or erase will invalidate the cache and keep it invalidated.
				Ren	0	Read only access
				Wen	1	Write enabled
				Een	2	Erase enabled
				PEen	4	Partial erase enabled

4.4.8.4 ERASEALL

Address offset: 0x50C

Register for erasing all non-volatile user memory

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	W		ERASEALL			Erase all non-volatile memory including UICR registers. Note that erasing must be enabled by setting CONFIG.WEN = Een before the non-volatile memory can be erased.
				NoOperation	0	No operation
				Erase	1	Start chip erase

4.4.8.5 ERASEPAGEPARTIALCFG

Address offset: 0x51C

Register for partial erase configuration

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																										A	A	A	A	A	A	A
Reset 0x0000000A	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	RW		DURATION			Duration of the partial erase in milliseconds The user must ensure that the total erase time is long enough for a complete erase of the flash page

4.4.8.6 ICACHECNF

Address offset: 0x540

I-code cache configuration register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																								B								A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	RW		CACHEEN			Cache enable
				Disabled	0	Disable cache. Invalidates all cache entries.
				Enabled	1	Enable cache
B	RW		CACHEPROFEN			Cache profiling enable
				Disabled	0	Disable cache profiling
				Enabled	1	Enable cache profiling

4.4.8.7 IHIT

Address offset: 0x548

I-code cache hit counter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	RW		HITS			Number of cache hits Write zero to clear

4.4.8.8 IMISS

Address offset: 0x54C

I-code cache miss counter

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	RW		MISSES			Number of cache misses Write zero to clear

4.4.8.9 CONFIGNS

Address offset: 0x584

Note: This register is one hot

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	RW		WEN			Program memory access mode. It is strongly recommended to only activate erase and write modes when they are actively used. Enabling write or erase will invalidate the cache and keep it invalidated.
				Ren	0	Read only access
				Wen	1	Write enabled
				Een	2	Erase enabled

4.4.8.10 WRITEUICRNS

Address offset: 0x588

Non-secure APPROTECT enable register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	TZ	Field	Value ID	Value	Description
A	W		SET			Allow non-secure code to set APPROTECT
				Set	1	Set value
B	W		KEY			Key to write in order to validate the write operation
				Keyvalid	0xAFBE5A7	Key value

4.4.9 Electrical specification

4.4.9.1 Flash programming

Symbol	Description	Min.	Typ.	Max.	Units
n_{WRITE}	Number of times a 32-bit word can be written before erase			2	
$n_{ENDURANCE}$	Erase cycles per page	10,000			
t_{WRITE}	Time to write one 32-bit word			43	µs
$t_{ERASEPAGE}$	Time to erase one page			87	ms
$t_{ERASEALL}$	Time to erase all flash			173	ms
$t_{ERASEPAGEPARTIAL,setup}$	Setup time for one partial erase			1.08	ms

4.4.9.2 Cache size

Symbol	Description	Min.	Typ.	Max.	Units
$Size_{ICODE}$	I-Code cache size		2048		Bytes

4.5 FICR — Factory information configuration registers

Factory information configuration registers (FICR) are pre-programmed in factory and cannot be erased by the user. These registers contain chip-specific information and configuration.

4.5.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
FICR	0x00FF0000	HF	S	NA	No	Factory information configuration

Register overview

Register	Offset	TZ	Description
SIPINFO.PARTNO	0x140		SIP part number
SIPINFO.HWREVISION[n]	0x144		SIP hardware revision, encoded in ASCII, for example B0A or B1A
SIPINFO.VARIANT[n]	0x148		SIP VARIANT, encoded in ASCII, for example LACA. See Ordering information for details.
INFO.DEVICEID[n]	0x204		Device identifier
INFO.RAM	0x218		RAM variant
INFO.FLASH	0x21C		Flash variant
INFO.CODEPAGESIZE	0x220		Code memory page size
INFO.CODESIZE	0x224		Code memory size
INFO.DEVICETYPE	0x228		Device type
TRIMCNF[n].ADDR	0x300		Address
TRIMCNF[n].DATA	0x304		Data

4.5.1.1 SIPINFO

SIP-specific device information is provided in the following chapters.

4.5.1.1.1 SIPINFO.PARTNO

Address offset: 0x140

SIP part number

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

ID	R/W	Field	Value ID	Value	Description
A	R	PARTNO			
			9161	0x00009161	Device is an nRF9161 sip
			9160	0x00009160	Device is an nRF9160 sip
			9131	0x00009131	Device is an nRF9131 sip

4.5.1.1.2 SIPINFO.HWREVISION[n] (n=0..3)

Address offset: 0x144 + (n × 0x1)

SIP hardware revision, encoded in ASCII, for example B0A or B1A

Note: When treated as a c-string, content is not NULL-terminated

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xFF						**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	R	HWREVISION											

4.5.1.1.3 SIPINFO.VARIANT[n] (n=0..3)

Address offset: 0x148 + (n × 0x1)

SIP VARIANT, encoded in ASCII, for example LACA. See Ordering information for details.

> **Note:** When treated as a c-string, content is not NULL-terminated

Bit number						7	6	5	4	3	2	1	0
ID						A	A	A	A	A	A	A	A
Reset 0xFF						**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description								
A	R	VARIANT			VARIANT[0] contains the most significant character of the SIP VARIANT. VARIANT[3] contains the least significant character of the SIP VARIANT.								
			A	0x41									
			B	0x42									
			C	0x43									
			I	0x49									
			L	0x4C									
			S	0x53									

4.5.1.2 INFO

Device info

4.5.1.2.1 INFO.DEVICEID[n] (n=0..1)

Address offset: 0x204 + (n × 0x4)

Device identifier

Bit number					31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF					**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value	Description																															
A	R	DEVICEID			64 bit unique device identifier DEVICEID[0] contains the least significant bits of the device identifier. DEVICEID[1] contains the most significant bits of the device identifier.																																	

4.5.1.2.2 INFO.RAM

Address offset: 0x218

RAM variant

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000100				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	RAM																																	
			K256	0x100																															
			Unspecified	0xFFFFFFFF																															

4.5.1.2.3 INFO.FLASH

Address offset: 0x21C

Flash variant

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000400				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	FLASH																																	
			K1024	0x400																															

4.5.1.2.4 INFO.CODEPAGESIZE

Address offset: 0x220

Code memory page size

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00001000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	CODEPAGESIZE																																	
			K4096	0x1000																															

4.5.1.2.5 INFO.CODESIZE

Address offset: 0x224

Code memory size

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000100				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	CODESIZE																																	
			P256	256																															

4.5.1.2.6 INFO.DEVICETYPE

Address offset: 0x228

Device type

Code memory size in number of pages

Total code space is: CODEPAGESIZE * CODESIZE

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	R	DEVICETYPE										Device type																							
			Die	0x0000000								Device is an physical DIE																							
			FPGA	0xFFFFFFFF								Device is an FPGA																							

4.5.1.3 TRIMCNF[n].ADDR (n=0..255)

Address offset: 0x300 + (n × 0x8)

Address

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	R	Address										Address																							

4.5.1.4 TRIMCNF[n].DATA (n=0..255)

Address offset: 0x304 + (n × 0x8)

Data

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	R	Data										Data																							

4.6 UICR — User information configuration registers

The user information configuration registers (UICRs) are non-volatile memory (NVM) registers for configuring user specific settings.

For information on writing UICR registers, see the NVMC — Non-volatile memory controller on page 29 and Memory on page 21 chapters.

4.6.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
UICR	0x00FF8000	HF	S	NA	No	User information configuration

Register overview

Register	Offset	TZ	Description
APPROTECT	0x000		Access port protection

Register	Offset	TZ	Description
XOSC32M	0x014		Oscillator control
HFXOSRC	0x01C		HFXO clock source selection
HFXOCNT	0x020		HFXO startup counter
APPNVMCPOFGUARD	0x024		Enable blocking NVM WRITE and aborting NVM ERASE for Application NVM in POFWARN condition.
SECUREAPPROTECT	0x02C		Secure access port protection
ERASEPROTECT	0x030		Erase protection
OTP[n]	0x108		One time programmable memory
KEYSLOT.CONFIG[n].DEST	0x400		Destination address where content of the key value registers (KEYSLOT.KEYn.VALUE[0-3]) will be pushed by KMU. Note that this address must match that of a peripheral's APB mapped write-only key registers, otherwise the KMU can push this key value into an address range which the CPU can potentially read.
KEYSLOT.CONFIG[n].PERM	0x404		Define permissions for the key slot. Bits 0-15 and 16-31 can only be written when equal to 0xFFFF.
KEYSLOT.KEY[n].VALUE[o]	0x800		Define bits [31+o*32:0+o*32] of value assigned to KMU key slot.

4.6.1.1 APPROTECT

Address offset: 0x000

Access port protection

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PALL										Blocks debugger read/write access to all CPU registers and memory mapped addresses Any value different to HwUnprotected will make access port protected.																							
			HwUnprotected	0x50FA50FA								HwUnprotected																							
			Protected	0x00000000								Protected																							

4.6.1.2 XOSC32M

Address offset: 0x014

Oscillator control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														A	A	A	A	A	A
Reset 0xFFFFFFCF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	CTRL										Pierce current DAC control signals																							

4.6.1.3 HFXOSRC

Address offset: 0x01C

HFXO clock source selection

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	HFXOSRC																																	
			XTAL	1																															
			TCXO	0																															

Description

HFXO clock source selection

32 MHz crystal oscillator

32 MHz temperature compensated crystal oscillator (TCXO)

4.6.1.4 HFXOCNT

Address offset: 0x020

HFXO startup counter

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	HFXOCNT																																	
			MinDebounceTime	0																															
			MaxDebounceTime	255																															

Description

HFXO startup counter. Total debounce time = HFXOCNT*64 us + 0.5 us

Min debounce time = (0*64 us + 0.5 us)

Max debounce time = (255*64 us + 0.5 us)

4.6.1.5 APPNVMCPOFGUARD

Address offset: 0x024

Enable blocking NVM WRITE and aborting NVM ERASE for Application NVM in POFWARN condition.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	NVMCPOFGUARDEN																																	
			Disabled	0																															
			Enabled	1																															

Description

Enable blocking NVM WRITE and aborting NVM ERASE in POFWARN condition

NVM WRITE and NVM ERASE are not blocked in POFWARN condition

NVM WRITE and NVM ERASE are blocked in POFWARN condition

4.6.1.6 SECUREAPPROTECT

Address offset: 0x02C

Secure access port protection

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	PALL																																	
			HwUnprotected	0x50FA50FA																															
			Protected	0x00000000																															

Description

Blocks debugger read/write access to all secure CPU registers and secure memory mapped addresses

Any value different to HwUnprotected will make access port protected.

HwUnprotected

Protected

4.6.1.7 ERASEPROTECT

Address offset: 0x030

Erase protection

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PALL										Blocks NVMC ERASEALL and CTRLAP ERASEALL functionality																							
			Unprotected	0xFFFFFFFF								Unprotected																							
			Protected	0x00000000								Protected																							

4.6.1.8 OTP[n] (n=0..189)

Address offset: 0x108 + (n × 0x4)

One time programmable memory

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW1	LOWER										Lower half word																							
												Note: Can only be written to a non 0xFFFF value once.																							
B	RW1	UPPER										Upper half word																							
												Note: Can only be written to a non 0xFFFF value once.																							

4.6.1.9 KEYSLOT.CONFIG[n].DEST (n=0..127)

Address offset: 0x400 + (n × 0x8)

Destination address where content of the key value registers (KEYSLOT.KEYn.VALUE[0-3]) will be pushed by KMU. Note that this address must match that of a peripheral's APB mapped write-only key registers, otherwise the KMU can push this key value into an address range which the CPU can potentially read.

Note: Writing/reading this register requires the KMU SELECTKEYSLOT register to be set to n+1.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	DEST										Secure APB destination address																							

4.6.1.10 KEYSLOT.CONFIG[n].PERM (n=0..127)

Address offset: 0x404 + (n × 0x8)

Define permissions for the key slot. Bits 0-15 and 16-31 can only be written when equal to 0xFFFF.

Note: Writing/reading this register requires the KMU SELECTKEYSLOT register to be set to n+1.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																			D														C	B	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	WRITE																																	
			Disabled	0																															
			Enabled	1																															
B	RW	READ																																	
			Disabled	0																															
			Enabled	1																															
C	RW	PUSH																																	
			Disabled	0																															
			Enabled	1																															
D	RW	STATE																																	
			Revoked	0																															
			Active	1																															

Revocation state for the key slot

Note that it is not possible to undo a key revocation by writing the value '1' to this field

Key value registers can no longer be read or pushed

Key value registers are readable (if enabled) and can be pushed (if enabled)

4.6.1.11 KEYSLOT.KEY[n].VALUE[o] (n=0..127) (o=0..3)

Address offset: 0x800 + (n × 0x10) + (o × 0x4)

Define bits [31+o*32:0+o*32] of value assigned to KMU key slot.

Note: Writing/reading this register requires the KMU SELECTKEYSLOT register to be set to n+1.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	VALUE																																	

Define bits [31+o*32:0+o*32] of value assigned to KMU key slot

4.7 EasyDMA

EasyDMA is a module implemented by some peripherals to gain direct access to Data RAM.

EasyDMA is an AHB bus master similar to CPU and is connected to the AHB multilayer interconnect for direct access to Data RAM. EasyDMA is not able to access flash.

A peripheral can implement multiple EasyDMA instances to provide dedicated channels. For example, for reading and writing of data between the peripheral and RAM. This concept is illustrated in EasyDMA example on page 44.

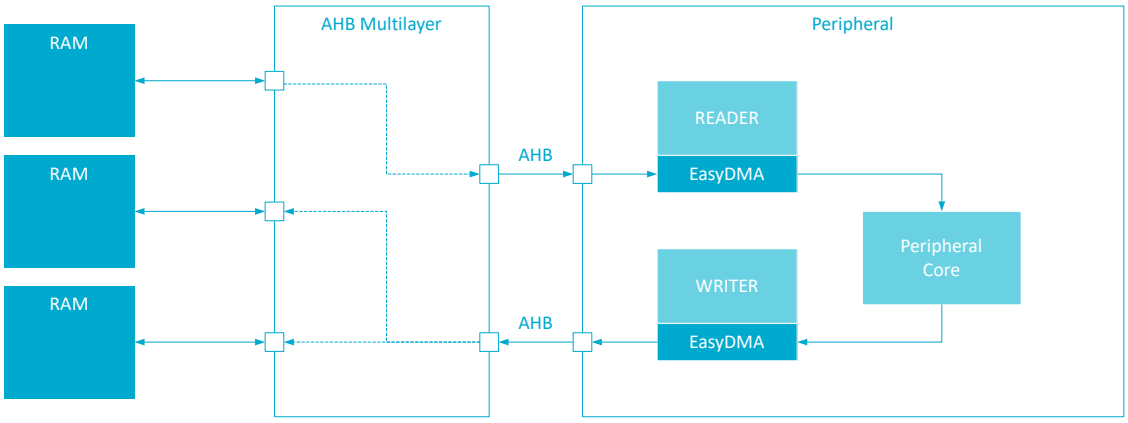

Figure 5: EasyDMA example

An EasyDMA channel is implemented in the following way, but some variations may occur:

```
READERBUFFER_SIZE 5
WRITERBUFFER_SIZE 6

uint8_t readerBuffer[READERBUFFER_SIZE]  __at__ 0x20000000;
uint8_t writerBuffer[WRITERBUFFER_SIZE]  __at__ 0x20000005;

// Configuring the READER channel
MYPERIPHERAL->READER.MAXCNT = READERBUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &readerBuffer;

// Configure the WRITER channel
MYPERIPHERAL->WRITER.MAXCNT = WRITEERBUFFER_SIZE;
MYPERIPHERAL->WRITER.PTR = &writerBuffer;
```

This example shows a peripheral called MYPERIPHERAL that implements two EasyDMA channels - one for reading called READER, and one for writing called WRITER. When the peripheral is started, it is assumed that the peripheral will perform the following tasks:

- Read 5 bytes from the readerBuffer located in RAM at address 0x20000000
- Process the data
- Write no more than 6 bytes back to the writerBuffer located in RAM at address 0x20000005

The memory layout of these buffers is illustrated in EasyDMA memory layout on page 44.

0x20000000	readerBuffer[0]	readerBuffer[1]	readerBuffer[2]	readerBuffer[3]
0x20000004	readerBuffer[4]	writerBuffer[0]	writerBuffer[1]	writerBuffer[2]
0x20000008	writerBuffer[3]	writerBuffer[4]	writerBuffer[5]	

Figure 6: EasyDMA memory layout

The WRITER.MAXCNT register should not be specified larger than the actual size of the buffer (writerBuffer). Otherwise, the channel would overflow the writerBuffer.

Once an EasyDMA transfer is completed, the AMOUNT register can be read by the CPU to see how many bytes were transferred. For example, CPU can read MYPERIPHERAL->WRITER.AMOUNT register to see how many bytes WRITER wrote to RAM.

Note: The PTR register of a READER or WRITER must point to a valid memory region before use. The reset value of a PTR register is not guaranteed to point to valid memory. See Memory on page 21 for more information about the different memory regions and EasyDMA connectivity.

4.7.1 EasyDMA error handling

Some errors may occur during DMA handling.

If READER.PTR or WRITER.PTR is not pointing to a valid memory region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Memory on page 21 for more information about the different memory regions.

If several AHB bus masters try to access the same AHB slave at the same time, AHB bus congestion might occur. An EasyDMA channel is an AHB master. Depending on the peripheral, the peripheral might either stall and wait for access to be granted, or lose data.

4.7.2 EasyDMA array list

EasyDMA can operate in Array List mode.

The Array List mode is implemented in channels where the LIST register is available.

The array list does not provide a mechanism to explicitly specify where the next item in the list is located. Instead, it assumes that the list is organized as a linear array where items are located one after the other in RAM.

The EasyDMA Array List can be implemented by using the data structure ArrayList_type as illustrated in the code example below using a READER EasyDMA channel as an example:

```
#define BUFFER_SIZE  4

typedef struct ArrayList
{
  uint8_t buffer[BUFFER_SIZE];
} ArrayList_type;

ArrayList_type ReaderList[3]  __at__ 0x20000000;

MYPERIPHERAL->READER.MAXCNT = BUFFER_SIZE;
MYPERIPHERAL->READER.PTR = &ReaderList;
MYPERIPHERAL->READER.LIST = MYPERIPHERAL_READER_LIST_ArrayList;
```

The data structure only includes a buffer of size equal to the size of READER.MAXCNT register. EasyDMA uses the READER.MAXCNT register to determine when the buffer is full.

READER.PTR = &ReaderList

0x20000000 : ReaderList[0]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000004 : ReaderList[1]	buffer[0]	buffer[1]	buffer[2]	buffer[3]
0x20000008 : ReaderList[2]	buffer[0]	buffer[1]	buffer[2]	buffer[3]

Figure 7: EasyDMA array list

4.8 AHB multilayer interconnect

On the AHB multilayer interconnect, the application CPU and all EasyDMA instances are AHB bus masters while RAM, cache, and peripherals are AHB slaves. External MCU subsystems can be seen both as master and slave on the AHB multilayer interconnect.

Multiple AHB masters can access slave resources within the AHB multilayer interconnect as illustrated in Memory on page 21. Access rights to each of the AHB slaves are resolved using the default natural priority of the different bus masters in the system.

4.8.1 AHB multilayer priorities

Each master connected to the AHB multilayer is assigned a default natural priority.

Bus master name	Natural relative priority	In/Out
System (CPU)	Highest priority	I/O
LTE Modem		I/O
I2S		I/O
PDM		I
SPIM0/SPIS0/TWIM0/TWIS0/UARTE0		I/O
SPIM1/SPIS1/TWIM1/TWIS1/UARTE1		I/O
SPIM2/SPIS2/TWIM2/TWIS2/UARTE2		I/O
SPIM3/SPIS3/TWIM3/TWIS3/UARTE3		I/O
SAADC		I
PWM0		O
PWM1		O
PWM2		O
PWM3		O
CC310	Lowest priority	I/O

Table 8: AHB bus masters (listed from highest to lowest priority)

5 Power and clock management

The power and clock management system automatically ensures maximum power efficiency.

The nRF9161 has three power modes - System Disabled, System ON and System OFF. The System ON and System OFF are internal (automatically handled by the device) and the System Disabled is external (driven by the ENABLE pin and overriding internal ones).

The core of the automatic power and clock management is the power management unit (PMU) illustrated in the following image.

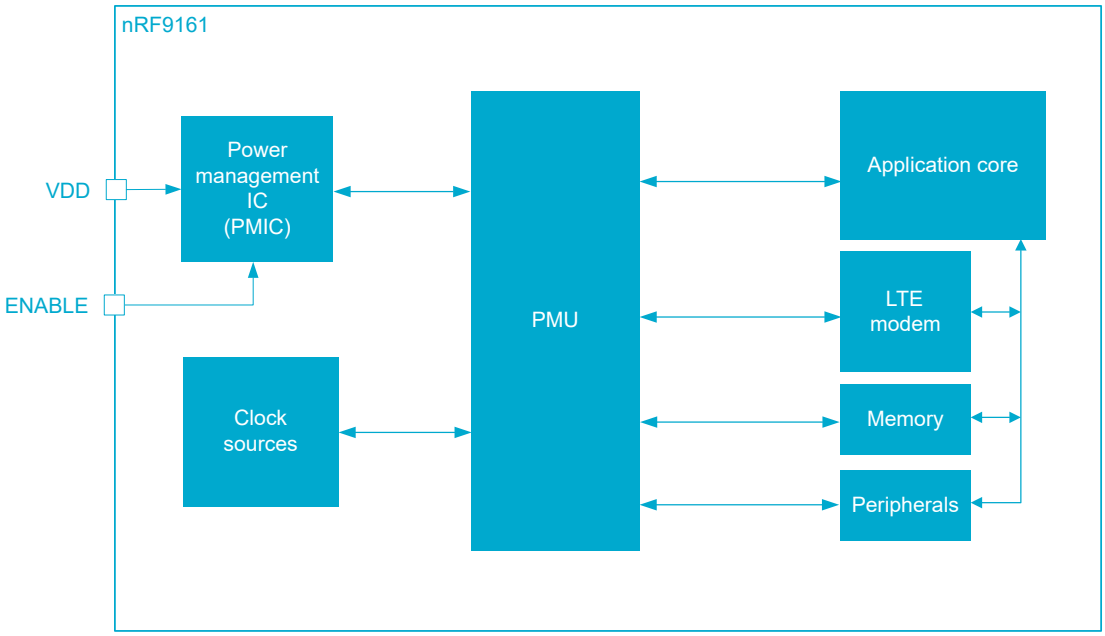

Figure 8: Power management unit

When the device is powered and enabled, the PMU automatically tracks the power and clock resources required by the different components in the system. It then starts/stops and chooses operation modes in supply regulators and clock sources, without user interaction, to achieve the lowest power consumption possible.

5.1 Power management

The two internal modes are handled by the power management unit (PMU), whereas the external is handled by the user via the ENABLE pin.

The System Disabled mode provides a way to override the PMU by manipulating voltages presented to the ENABLE pin.

The PMU steers system-wide clock and power in order to provide the power modes - System ON and System OFF. Under the various modes, internal blocks are automatically powered by the PMU as required by the application.

5.1.1 System Disabled mode

The entire device can be powered down by presenting the appropriate voltage to the externally available ENABLE pin.

The nRF9161 provides a feature to be able disable power throughout the entire device externally. This can be useful when the device is operating as slave processor where it does not need to be powered on at all times, then it is possible to avoid unnecesary current leaking by driving the ENABLE pin to low. The nRF9161 will not start if is not enabled. Moreover, a change from disable to enable, will result in a power-on-reset behavior inside the device.

Note: VDD_GPIO input must be driven low when device is disabled, failing to do so could result in increased leakage. For more information, see VDD_GPIO considerations in Operating conditions on page 455.

Note: In case the System Disabled mode is not used, ENABLE must be connected to VDD.

Pin Value	Power status	description
Low	Disabled	Device's internal power regulator disabled
High	Enabled	Device's internal power regulator enabled

Table 9: ENABLE pin configuration

5.1.2 System OFF mode

System OFF is the deepest internal power saving mode the system can enter.

In this mode, the core system functionality is powered down and ongoing tasks terminated, and only the reset and the wakeup functions are available and responsive.

The device is put into System OFF mode using the REGULATORS register interface. When in System OFF mode, one of the following signals/actions will wake up the device:

1. DETECT signal, generated by the GPIO peripheral
2. RESET
3. Debug session start

When the device wakes up from System OFF mode, a system reset is performed.

One or more RAM blocks can be retained in System OFF mode depending on the settings in the RAM[n].POWER registers in VMC. RAM[n].POWER are retained registers, see Reset behavior on page 57. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

Before entering System OFF mode, the user must make sure that all on-going EasyDMA transactions have completed. This can be done by making sure that EasyDMA enabled peripherals have stopped and END events from them received. The LTE modem must also be stopped, by issuing a command through the modem API, before entering System OFF mode. Once the command is issued, wait for the modem to respond that it actually has stopped, as there may be a delay until the modem is disconnected from the network.

5.1.2.1 Emulated System OFF mode

If the device is in debug interface mode, System OFF will be emulated to ensure that all resources required for debugging are available during System OFF.

See Debug and trace on page 368 chapter for more information. Resources required for debugging include the following key components: Debug and trace on page 368, CLOCK — Clock control on page 70, POWER — Power control on page 63, NVMC — Non-volatile memory controller on page 29, CPU on page 20, flash, and RAM. To prevent the CPU from executing unwanted code, an infinite loop must be added directly after entering System OFF mode.

5.1.3 System ON mode

System ON is the power mode entered after a power-on reset.

While in System ON, the system can reside in one of two sub modes:

- Low power
- Constant latency

The low power mode is default after power-on reset.

In low power mode, whenever no application or wireless activity takes place, function blocks like the application CPU, LTE modem and all peripherals are in IDLE state. That particular state is referred to as System ON IDLE. In this state, all function blocks retain their state and configuration, so they are ready to become active once configured by the CPU.

If any application or modem activity occurs, the system leaves the System ON IDLE state. Once a given activity in a function block is completed, the system automatically returns to IDLE, retaining its configuration.

As long as the system resides in low power mode, the PMU ensures that the appropriate regulators and clock sources are started or stopped based on the needs of the function blocks active at any given time.

This automatic power management can be overridden by switching to constant latency mode. In this mode, the CPU wakeup latency and the PPI task response are constant and kept at a minimum. This is secured by keeping a set of base resources that are always enabled. The advantage of having a constant and predictable latency will be at the cost of having significantly increased power consumption compared to the low power mode. The constant latency mode is enabled by triggering the CONSTLAT task (TASKS_CONSTLAT on page 64).

While the system is in constant latency mode, the low power mode can be enabled by triggering LOWPWR task (TASKS_LOWPWR on page 64).

To reduce power consumption while in System ON IDLE, RAM blocks can be turned off in System ON mode while enabling the retention of these RAM blocks in RAM[n].POWER registers in VMC. RAM[n].POWER are retained registers, see Reset behavior on page 57. Note that these registers are usually overwritten by the startup code provided with the nRF application examples.

5.1.4 Registers

5.1.5 Electrical specification

5.1.5.1 ENABLE pin

Symbol	Description	Min.	Typ.	Max.	Units
$V_{SYSTEM\_DISABLED\_ON}$	Operational voltage to enforce System-Disabled power mode.	0.8*VDD			V
$V_{SYSTEM\_DISABLED\_OFF}$	Operational voltage to cancel System-Disabled power mode.			0.4	V
$t_{HOLDENABLE}$	ENABLE pin hold time	TBA			ms

5.2 Power supply

The nRF9161 has a single main power supply VDD, and the internal components are powered by integrated voltage regulators. The PMU manages these regulators automatically, no voltage regulator control needs to be included in application firmware.

5.2.1 General purpose I/O supply

The input/output (I/O) drivers of P0.00 - P0.31 pins are supplied independently of VDD through VDD_GPIO. This enables easy match to signal voltage levels in the printed circuit board design.

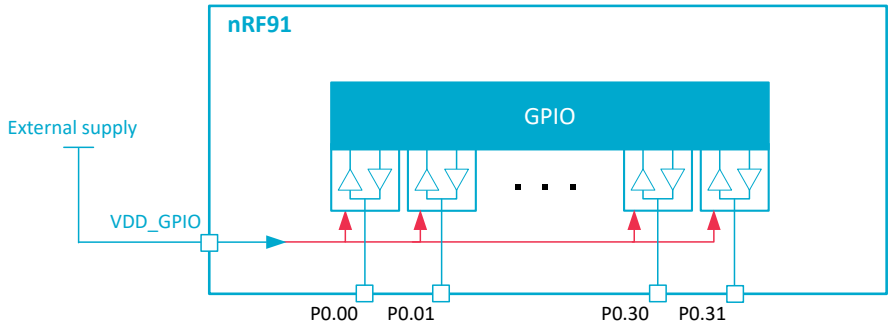

Figure 9: GPIO supply input (VDD_GPIO)

The I/Os are supplied via VDD_GPIO pin as shown in figure above. VDD_GPIO pin supports voltage levels within range given in table Operating conditions on page 455. See VDD_GPIO considerations on page 455 for more information on how to control VDD_GPIO power supply.

5.3 Power supply monitoring

Power monitor solutions are available in the device, in order to survey the VDD (battery voltage).

5.3.1 Power supply supervisor

The power supply supervisor enables monitoring of the connected power supply.

Two functionalities are implemented:

- Power-on reset (POR): Generates a reset when the supply is applied to the device, and ensures that the device starts up in a known state
- Brownout reset (BOR): Generates a reset when the supply drops below the minimum voltage required for safe operations

Two BOR levels are used:

- V_{BOROFF}, used in System OFF
- V_{BORON}, used in System ON

The power supply supervisor is illustrated in the image below.

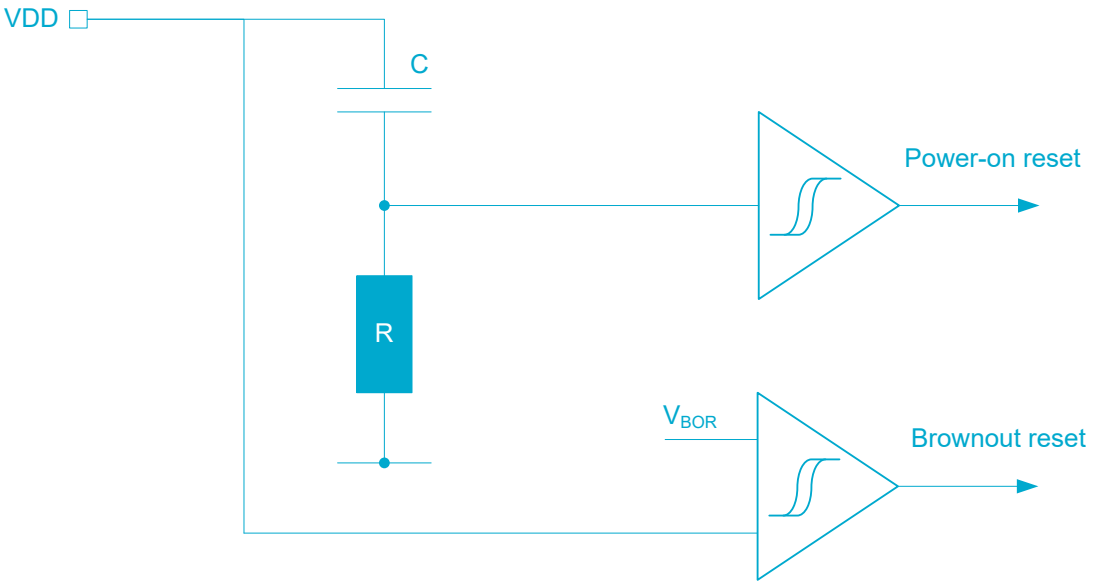

Figure 10: Power supply supervisor

5.3.2 External power failure warning

The external power failure (EXTPOF) warning can provide the CPU an early warning of an imminent power failure. It does not reset the system, but gives the CPU time to prepare for an orderly power-down. EXTPOF detects power failures external to PMU from the device internal PMIC.

> **Note:** All nRF9161 modem firmware versions support this feature.

The user can start and stop the PMIC EXTPOF feature and set the battery voltage low threshold level through the modem API.

For application core to receive the power failure warning events, EXTPOFCON on page 78 register in REGULATORS — Voltage regulators control on page 77 must be enabled. If this is disabled, the state of the PMIC warning input is ignored and the power failure warning events are not delivered to application core.

The available time for the CPU to prepare for a power-down depends on the set warning threshold level, the load of the running tasks, and the type of power source used.

> **Note:** For details on services provided by the modem AT command interface, see nRF Connect SDK AT interface and nRF91 AT Commands.

The EXTPOF functional overview is shown in the following figure.

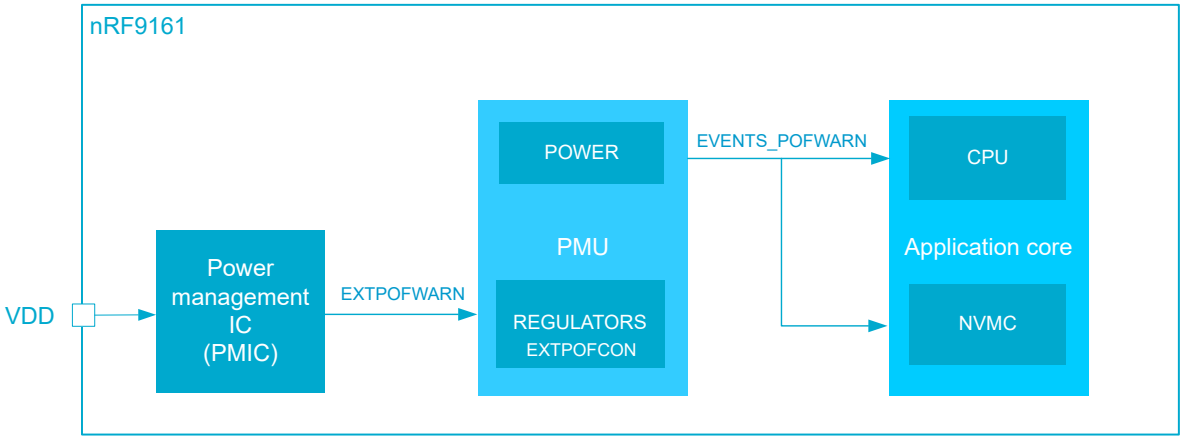

Figure 11: External power failure warning arrangement

If EXTPOF is enabled and the device's internal PMIC detects that battery voltage has dropped below the low threshold level, an POFWARN event is generated (see EVENTS_POFWARN on page 65). The POFWARN event to the CPU can be cleared in the event register, however the PMIC input continues to indicate a warning as long as the battery voltage remains below the low threshold level.

POFWARN event also sets the LTE modem in offline mode.

> **Note:** If a power failure warning occurs during an ongoing NVM write operation, the NVMC tries to finish the operation. Consecutive NVM write operations will be blocked by the NVMC as long as the PMIC input indicates a warning. The CPU interprets a blocked NVM write as a fault, which needs to be handled by the application. If a power failure warning occurs during an ongoing NVM erase operation, the operation will be aborted. Blocking NVM writes and aborting NVM erase operations can be disabled in APPNVMCPOFGUARD on page 41.

The external power failure warning doesn't trigger wakeup from System OFF.

The external power failure warning is disabled in System OFF mode.

5.3.3 Battery monitoring on VDD

A battery voltage (VDD) monitoring capability is provided via a modem API.

> **Note:** For details on services provided by the modem AT command interface, see nRF Connect SDK AT interface and nRF91 AT Commands.

5.3.4 Registers

5.3.5 Electrical specification

5.3.5.1 Device startup times

Symbol	Description	Min.	Typ.	Max.	Units
t_{POR}	Time in power-on reset after VDD has reached 3V, ENABLE is tied to VDD.		1.2		ms
t_{PINR}	The maximum time taken to pull up the nRESET pin and release reset after power-on reset. Dependent on the pin capacitive load (C)[2]: t=TRC; Typical: T=2 R=13 kΩ; Max: T=5 R=16 kΩ.	..	..	..	

[2] To decrease the maximum time a device can be held in reset, a strong external pull-up resistor can be used.

Symbol	Description	Min.	Typ.	Max.	Units
$t_{PINR,500nF}$	C=500 nF		13	40	ms
$t_{PINR,10uF}$	C=10 µF		260	800	ms
t_{R2ON}	Time from reset to ON (CPU execute)		127	135	µs
t_{OFF2ON}	Time from OFF to CPU execute		73	92	µs
$t_{WFE2CPU}$	Time from WFE to CPU execute		70	90	µs
$t_{WFI2CPU}$	Time from WFI to CPU execute		69	90	µs
$t_{EVTSET,CL1}$	Time from HW event to PPI event in constant latency System ON mode		0.1	0.1	µs
$t_{EVTSET,CL0}$	Time from HW event to PPI event in low power System ON mode		0.1	0.7	µs
$t_{LTEMODEM,TYP}$	LTE modem typical startup time. Time from application core powering up the modem until the modem is ready to receive the first AT command.			200	ms
$t_{LTEMODEM,WORSTCASE}$	LTE modem worst case startup time. Time from application core powering up the modem until the modem is ready to receive the first AT command, with modem firmware variable elements included.			250	ms
$t_{LTEMODEM,FOTA}$	LTE modem startup time after modem FOTA update. Time from application core powering up the modem after a modem FOTA update until the modem is ready to receive the first AT command.			7.5	s
$t_{LTEMODEM,FOTAREJECT}$	LTE modem startup time after a rejected modem FOTA update. Time from application core powering up the modem after a rejected modem FOTA update until the modem is ready to receive the first AT command. Modem will revert back to original firmware image.			90	s
$t_{LTEMODEM,STOP,TYP}$	LTE modem typical shutdown time. Time from application core calling bsd_shutdown command until bsd_shutdown returns.			1.6	s
$t_{LTEMODEM,STOP,WORSTCASE}$	LTE modem worst case shutdown time. Time from application core calling bsd_shutdown command until bsd_shutdown returns, including modem firmware variable elements.			79	s

5.3.5.2 Power supply supervisor

Symbol	Description	Min.	Typ.	Max.	Units
V_{BOR}	Brownout reset voltage threshold.		2.80		V
V_{POR}	Voltage threshold at which the device enters power-on reset (POR) when VDD is ramping up.			3.0	V

5.4 Clock management

The clock control system can source the system clocks from a range of high and low frequency oscillators, and distribute them to modules based upon a module's individual requirements.

Clock generation and distribution is handled automatically by PMU to optimize current consumption. This optimization will affect the predictability of the oscillators' startup times under different device operating conditions. However, it is possible to bypass some of the power saving mechanisms by explicitly keeping the system on constant latency sub mode (more about constant latency in System ON mode on page 49) and/or manipulating START/STOP clock task registers.

The following are the available clock signal sources:

- 64 MHz oscillator (HFINT)
- 64 MHz high accuracy oscillator (HFXO)
- 32.768 kHz RC oscillator (LFRC)
- 32.768 kHz high accuracy oscillator (LFXO)

The clock and oscillator resources are configured and controlled via the CLOCK peripheral as illustrated below.

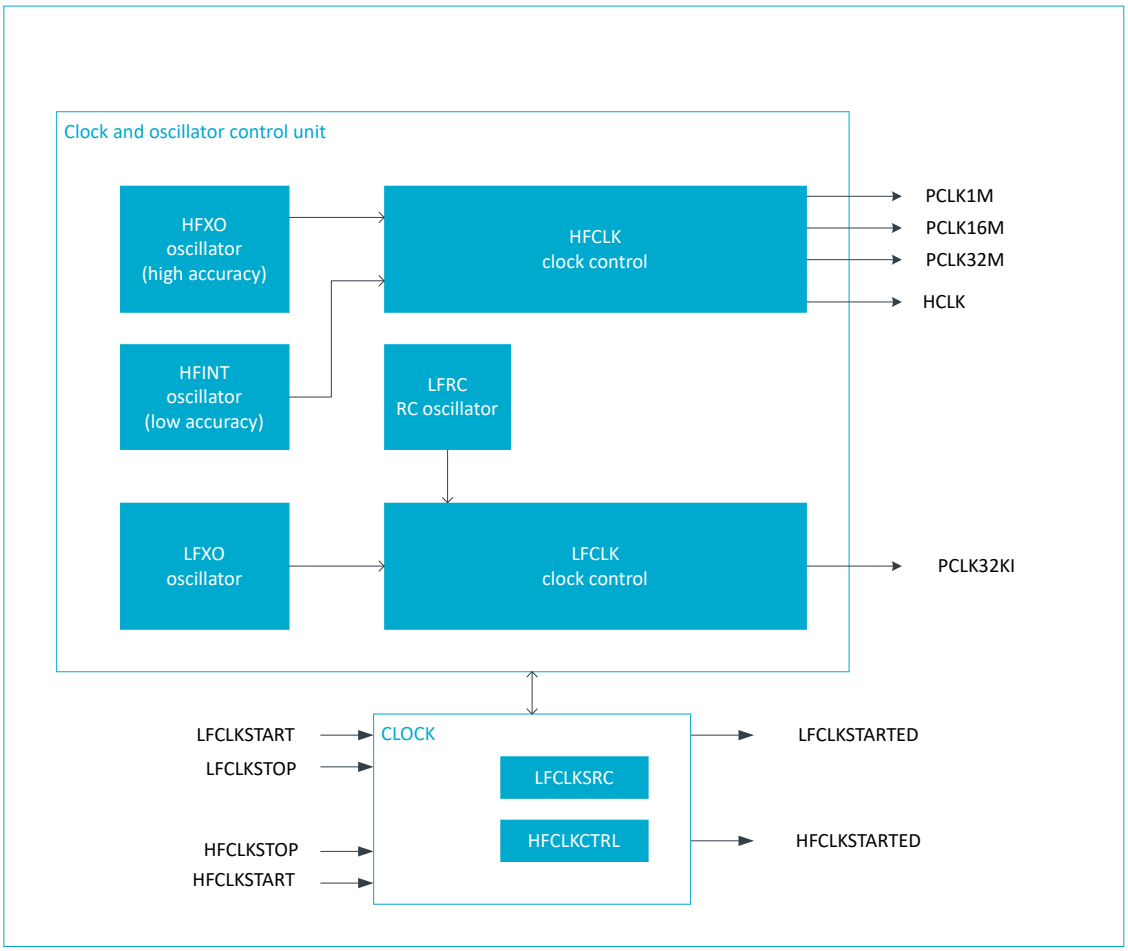

Figure 12: Clock and oscillator setup

5.4.1 HFCLK clock controller

The HFCLK clock controller provides several clocks in the system.

These are as follows:

- HCLK: 64 MHz CPU clock
- PCLK1M: 1 MHz peripheral clock
- PCLK16M: 16 MHz peripheral clock
- PCLK32M: 32 MHz peripheral clock

The HFCLK controller uses the following high frequency clock (HFCLK) sources:

- 64 MHz oscillator (HFINT)
- 64 MHz high accuracy oscillator (HFXO)

For illustration, see Clock and oscillator setup on page 54.

The HFCLK controller automatically provides the clock(s) requested by the system. If the system does not request any clocks from the HFCLK controller, the controller switches off all its clock sources and enters a power saving mode.

The HFINT source is used when HFCLK is requested and HFXO has not been started.

The HFXO is started by triggering the HFCLKSTART task and stopped using the HFCLKSTOP task. A HFCLKSTARTED event is generated when the HFXO has started and its frequency is stable.

5.4.2 LFCLK clock controller

The system supports several low frequency clock sources.

As illustrated in Clock and oscillator setup on page 54, the system supports the following low frequency clock sources:

- LFXO: 32.768 kHz high accuracy oscillator
- LFRC: 32.768 kHz RC oscillator

The LFCLK clock controller and all LFCLK clock sources are always switched off when in System OFF mode.

The LFCLK clock is started by first selecting the preferred clock source in the LFCLKSRC on page 77 register and then triggering the LFCLKSTART task. LFXO is highly recommended as the LFCLK clock source, since the LFRC has a large frequency variation.

> **Note:** The LTE modem requires use of LFXO as the LFCLK source.

Switching between LFCLK clock sources can be done without stopping the LFCLK clock. A LFCLK clock source which is running prior to triggering the LFCLKSTART task continues to run until the selected clock source is available. After that the clock sources will be switched. Switching between clock sources will stretch a clock pulse by 0.5 to 1.0 clock cycle (i.e. will delay rising edge by 0.5 to 1.0 clock cycle).

> **Note:** If the watchdog timer (WDT) is running, the default LFCLK clock source (LFRC - see LFCLKSRC on page 77) is started automatically (LFCLKSTART task doesn't have to be triggered).

A LFCLKSTARTED event will be generated when the selected LFCLK clock source has started.

> **Note:** The first time LFXO is selected, LFRC quality is provided until LFXO is stable.

A LFCLKSTOP task will prevent global requesting of the LFCLK clock, unless a system component such as WDT or modem requires the LFCLK, in which case the clock is not stopped. The LFCLKSTOP task should only be triggered after the STATE field in the LFCLKSTAT register indicates a LFCLK running state.

5.4.2.1 32.768 kHz RC oscillator (LFRC)

The default source of the low frequency clock (LFCLK) is the 32.768 kHz RC oscillator (LFRC).

The LFRC frequency is affected by variation in temperature.

5.4.3 Registers

5.4.4 Electrical specification

5.4.4.1 64 MHz internal oscillator (HFINT)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_HFINT}	Nominal output frequency		64		MHz
f_{TOL_HFINT}	Frequency tolerance		±1	±5	%
t_{START_HFINT}	Startup time		3.2		µs

5.4.4.2 64 MHz high accuracy oscillator (HFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_HFXO}	Nominal output frequency		64		MHz
f_{TOL_HFXO}	Frequency tolerance		±1		ppm
t_{START_HFXO}	Startup time		2		ms

5.4.4.3 32.768 kHz high accuracy oscillator (LFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFXO}	Frequency		32.768		kHz
f_{TOL_LFXO}	Frequency tolerance		±20		ppm
t_{START_LFXO}	Startup time		450		ms

5.4.4.4 32.768 kHz RC oscillator (LFRC)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f_{TOL_LFRC}	Frequency tolerance		30		%
t_{START_LFRC}	Startup time		600		µs

5.5 Reset

A system reset can be triggered by multiple sources. After a reset the CPU can query the RESETREAS (reset reason register) to find out which source generated the reset.

5.5.1 Power-on reset

The power-on reset generator initializes the system at power-on. The system is held in reset state until the supply has reached the minimum operating voltage and the internal voltage regulators have started.

5.5.2 Pin reset

A pin reset is generated when the physical reset pin (nRESET) on the device is pulled low.

To ensure that reset is issued correctly, the reset pin should be held low for the time specified in Pin reset on page 58.

nRESET pin has an always-on internal pull-up resistor connected to nRF9161 internal voltage typically of 2.2 V level, as illustrated in the following figure. The value of the pull-up resistor is given in Pin reset on page 58.

Note: Driving nRESET high with a voltage lower than 2.2V will result in additional leakage.

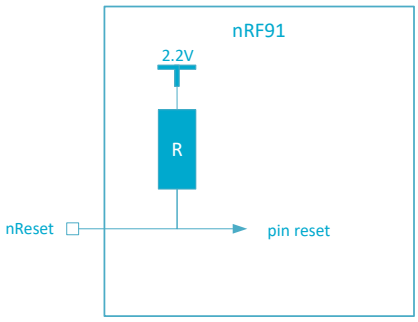

Figure 13: Pin reset internal generation

5.5.3 Wakeup from System OFF mode reset

The device is reset when it wakes up from System OFF mode.

The Debug access port is not reset following a wake up from System OFF mode if the device is in debug interface mode, see Debug and trace on page 368 chapter for more information.

5.5.4 Soft reset

A soft reset is generated when the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR register) in the Arm core is set.

5.5.5 Watchdog reset

A watchdog reset is generated when the watchdog timer (WDT) times out.

See WDT — Watchdog timer on page 351 chapter for more information.

5.5.6 Brownout reset

The brownout reset generator puts the system in reset state if the supply voltage drops below the brownout reset threshold.

5.5.7 Retained registers

A retained register is a register that will retain its value in System OFF mode, and through a reset depending on reset source. For information on which peripheral registers are retained, see the corresponding peripheral's chapter.

5.5.8 Reset behavior

Reset behavior depends on the reset source.

The reset behavior is summarized in the table below.

Reset source	Reset target							
	CPU	Modem	Debug[3]	SWJ-DP	Not retained RAM[4]	Retained RAM[4]	WDT	RESETREAS
CPU lockup [5]	x	x						
Soft reset	x	x						
Wakeup from System OFF mode reset	x	x	x [6]		x		x	
Watchdog reset [7]	x	x	x		x	x	x	
Pin reset	x	x	x	x	x	x	x	
Brownout reset	x	x	x	x	x	x	x	x
Power-on reset	x	x	x	x	x	x	x	

Table 10: Reset behavior for the main components

[3] All debug components excluding SWJ-DP. See Debug and trace on page 368 chapter for more information about the different debug components in the system.
[4] RAM can be configured to be retained using registers in VMC — Volatile memory controller on page 28
[5] Reset from CPU lockup is disabled if the device is in debug interface mode. CPU lockup is not possible in System OFF.
[6] The debug components will not be reset if the device is in debug interface mode.
[7] Watchdog reset is not available in System OFF.

Note: The RAM is never reset but its content might be corrupted after reset in the cases given in the table above.

Reset source	Reset target					
	Regular peripheral registers	GPIO, SPU	NVMC WAITSTATENUM	NVMC IFCREADDELAY	REGULATORS, OSCILLATORS	POWER.GPREGRET
CPU lockup[5]	x	x	x			
Soft reset	x	x	x			
Wakeup from System OFF mode reset	x		x			
Watchdog reset[7]	x	x	x		x	
Pin reset	x	x	x		x	
Brownout reset	x	x	x	x	x	x
Power-on reset	x	x	x	x	x	x

Table 11: Reset behavior for the retained registers

5.5.9 Registers

5.5.10 Electrical specification

5.5.10.1 Pin reset

Symbol	Description	Min.	Typ.	Max.	Units
$t_{HOLDRESET}$	Hold time for reset pin when doing a pin reset	5			µs
$R_{PULL-UP}$	Value of the internal pull-up resistor		13		kΩ

5.6 Current consumption

As the system is constantly tuned by the PMU described in Power and clock management on page 47, estimating the current consumption of an application can be challenging if the designer cannot perform measurements directly on the hardware. To facilitate the estimation process, a set of current consumption scenarios are provided to show the typical current drawn from the VDD supply.

Each scenario specifies a set of operations and conditions that apply to the given scenario. The following table shows a set of common conditions used in all scenarios, unless otherwise is stated in the scenario's description. Similarly, Current consumption scenarios, common conditions for LTE modem on page 59 describes the conditions used for the modem current consumption specifications. For a list of all scenarios, see Electrical specification on page 59.

Peripherals typically share one or more power sources. This results in a current consumption that does not scale linearly with the number of peripherals enabled. For example, the current consumption for an application with two peripherals enabled, is not the sum of the currents reported by their individual peripherals.

Condition	Value
Supply	3.7 V
Temperature	25 °C
CPU	WFI (wait for interrupt)/WFE (wait for event) sleep
Peripherals	All idle[8]
Clock	HFCLK=HFINT Not running LFCLK=Not running
RAM	No retention
Cache enabled	Yes

Table 12: Current consumption scenarios, common conditions

Condition
Cat-M1 and Cat-NB1 HD FDD mode
Good channel, RF cable, no errors in DL/UL communication
Minimum network response times
Output power at antenna port, single-ended 50 Ω
Modem eDRX current consumption quoted with UICC that allows UICC supply shut down at eDRX intervals. [9] [10] [11]
Modem PSM TAU event energy is measured from the modem PSM wake-up until end of RX inactivity time
All LTE modem current consumption numbers include application core idle mode consumption [12]

Table 13: Current consumption scenarios, common conditions for LTE modem

5.6.1 Electrical specification

5.6.1.1 Current consumption during System Disabled

Symbol	Description	Min.	Typ.	Max.	Units
$I_{SYSTEM\_DISABLED}$	ENABLE and VDD_GPIO pins grounded		150		nA

[8] Except for currents reported for a given peripheral. Peripherals' currents are estimated during momentary transmission.

[9] Required UICC restart current consumption is included.

[10] If the UICC used does not support supply shut down, then UICC will remain in clock stop mode. Depending on the UICC used, a clock stop current in the range of 20 µA to 60 µA@3.7 V must be added to get the total average consumption.

[11] Minimum UICC supply shut down interval and clock stop mode current consumption must be obtained from the UICC supplier.

[12] Application RAM leakage not included. Application RAM leakage quoted separately under Sleep on page 60

5.6.1.2 Sleep

Symbol	Description	Min.	Typ.	Max.	Units
$I_{MCUOFF0}$	MCU off, modem off, wake on GPIO and reset		1.4		µA
I_{MCUON0}	MCU on IDLE, modem off, RTC off		1.8		µA
I_{MCUON1}	MCU on IDLE, modem off, RTC on		2.2		µA
I_{MCUON2}	MCU on IDLE, modem off, wake on GPIOTE input (event mode), Constant latency System ON mode		600		µA
I_{MCUON3}	MCU on IDLE, modem off, wake on GPIOTE input (event mode), Low power System ON mode		18		µA
I_{MCUON4}	MCU on IDLE, modem off, wake on GPIOTE input (port event)		1.8		µA
I_{RAM}	RAM retention leakage current of a 32kB block		0.1		µA

5.6.1.3 Application CPU active current consumption

The application CPU running parameters are obtained using the following compiler version:

Compiler: Arm version 6.16 (armclang)

Compiler flags:

```
-Wno-unused-command-line-argument --target=arm-arm-none-eabi -c -g -masm=auto -Wno-unused-value -mcpu=cortex-m33 -mfpu=fpv5-sp-d16 -mfloat-abi=hard -fno-rtti -flto -funsigned-char -mcmse -Omax -ffunction-sections
```

Symbol	Description	Min.	Typ.	Max.	Units
I_{CPU0_FLASH}	CPU running CoreMark @64 MHz from flash, clock = HFINT, cache enabled		2.7		mA
$I_{COREMARK\_PER\_MA\_FLASH}$	CoreMark per mA, executing from flash, CoreMark=247		91		CoreMark/mA
I_{CPU0_RAM}	CPU running CoreMark @64 MHz from RAM, clock = HFINT		2.1		mA
$I_{COREMARK\_PER\_MA\_RAM}$	CoreMark per mA, executing from RAM, CoreMark=239		114		CoreMark/mA

5.6.1.4 I2S

Symbol	Description	Min.	Typ.	Max.	Units
I_{I2S0}	I2S transferring data left-channel (mono) @ 16 bit x 16 kHz (CONFIG.MCKFREQ = 32MDIV8, CONFIG.RATIO = 256X), Clock = HFINT		600		µA
I_{I2S1}	I2S transferring data left-channel (mono) @ 16 bit x 16 kHz (CONFIG.MCKFREQ = 32MDIV8, CONFIG.RATIO = 256X), Clock = HFXO		1620		µA

5.6.1.5 PDM

Symbol	Description	Min.	Typ.	Max.	Units
I_{PDM}	PDM receiving and processing data 16KHz, with FREQ = 1.28MHz, MODE.OPERATION = mono		620		µA
I_{PDM}	PDM receiving and processing data 16KHz, with FREQ = 1.28MHz, MODE.OPERATION = mono, clock HFXO		1630		µA

5.6.1.6 PWM

Symbol	Description	Min.	Typ.	Max.	Units
I_{PWM0}	PWM running @ 125 kHz, fixed duty cycle		510		µA
I_{PWM1}	PWM running @ 16 MHz, fixed duty cycle		680		µA

5.6.1.7 SAADC

Symbol	Description	Min.	Typ.	Max.	Units
I_{SAADC_HFXO}	SAADC sampling @ 16 ksps, with high accuracy clock HFXO, acquisition time = 20 µs		1550		µA
I_{SAADC_HFINT}	SAADC sampling @ 16 ksps, with low accuracy clock HFINT, acquisition time = 20 µs		540		µA

5.6.1.8 TIMER

Symbol	Description	Min.	Typ.	Max.	Units
I_{TIMER0}	TIMER running @ 1 MHz		390		µA
I_{TIMER1}	TIMER running @ 16 MHz		440		µA

5.6.1.9 SPIM

Symbol	Description	Min.	Typ.	Max.	Units
I_{SPIM0}	SPIM transferring data @ 2 Mbps, Clock = HFINT		610		µA
I_{SPIM1}	SPIM transferring data @ 2 Mbps, Clock = HFXO		1620		µA
I_{SPIM2}	SPIM transferring data @ 8 Mbps, Clock = HFINT		640		µA
I_{SPIM3}	SPIM transferring data @ 8 Mbps, Clock = HFXO		1660		µA

5.6.1.10 SPIS

Symbol	Description	Min.	Typ.	Max.	Units
I_{SPIS_2M}	SPIS receiving data @ 2 Mbps, Clock=HFINT		500		µA
I_{SPIS_2MXO}	SPIS receiving data @ 2 Mbps, Clock=HFXO		1510		µA
I_{SPIS_8M}	SPIS receiving data @ 8 Mbps, Clock=HFINT		510		µA
I_{SPIS_8MXO}	SPIS receiving data @ 8 Mbps, Clock=HFXO		1520		µA

5.6.1.11 TWIM

Symbol	Description	Min.	Typ.	Max.	Units
I_{TWIM_100}	TWIM running @ 100 kbps, Clock=HFINT		590		µA
I_{TWIM_400}	TWIM running @ 400 kbps, Clock = HFINT		590		µA
I_{TWIM_100XO}	TWIM running @ 100 kbps, Clock = HFXO		1600		µA
I_{TWIM_400XO}	TWIM running @ 400 kbps, Clock = HFXO		1610		µA

5.6.1.12 TWIS

Symbol	Description	Min.	Typ.	Max.	Units
I_{TWIS,RUN_100}	TWIS transferring data @ 100 kbps, Clock=HFINT		590		µA
I_{TWIS1,RUN_400}	TWIS transferring data @ 400 kbps, Clock=HFINT		510		µA
I_{TWIS,RUN_100XO}	TWIS transferring data @ 100 kbps, Clock = HFXO		1480		µA
I_{TWIS,RUN_400XO}	TWIS transferring data @ 400 kbps, Clock = HFXO		1370		µA

5.6.1.13 UARTE

Symbol	Description	Min.	Typ.	Max.	Units
$I_{UARTE,1M}$	UARTE transferring data @ 1Mbps		700		µA
$I_{UARTE,115K}$	UARTE transferring data @ 115200 bps		510		µA

5.6.1.14 WDT

Symbol	Description	Min.	Typ.	Max.	Units
I_{WDT}	WDT started		2.5		µA

5.6.1.15 Modem current consumption

To estimate specific use cases, see Online Power Profiler for LTE

Symbol	Description	B13 (typ.)	B20 (typ.)	B3 (typ.)	B4 (typ.)	Units
Sleep current consumption, Cat-M1 and Cat-NB1						
I_{PSM}	PSM floor current	2.7	2.7	2.7	2.7	µA
PSM TAU event energy and duration, Cat-M1						
E_{PSM_TAU}	Pout 23 dBm, QPSK, resource blocks 6, TBS index 9, UICC included	93	94	99	99	mJ
T_{PSM_TAU}	Pout 23 dBm, QPSK, resource blocks 6, TBS index 9, UICC included	1.3	1.3	1.3	1.3	s
PSM TAU event energy and duration, Cat-NB1						
E_{PSM_TAU}	Pout 23 dBm, QPSK, UICC included; UL: 12SC, MCS Index 5 Resource Units 1, Repetitions 1; DL, 12SC, MCS Index 6, Subframes 3, Repetitions 1	306	319	315	335	mJ
T_{PSM_TAU}	Pout 23 dBm, QPSK, UICC included; UL: 12SC, MCS Index 5 Resource Units 1, Repetitions 1; DL, 12SC, MCS Index 6, Subframes 3, Repetitions 1	2.7	2.7	2.7	2.7	s
Average current consumption, radio resource control (RRC) mode, Cat-M1						
I_{EDRX}	eDRX average current, 81.92 s, one PO/PTW, PTW = 2.56 s	19	-	19	-	µA
I_{IEDRX}	Idle eDRX average current, 655 s, one PO/PTW, PTW = 2.56 s	6	-	6	-	µA
I_{RMC_0DBM}	Uplink 180 kbit/s, Pout 0 dBm, RMC settings as per 3GPP TS 36.521-1 Annex A.2	45	45	47	46	mA
I_{RMC_10DBM}	Uplink 180 kbit/s, Pout 10 dBm, RMC settings as per 3GPP TS 36.521-1 Annex A.2	49	50	51	54	mA
I_{RMC_23DBM}	Uplink 180 kbit/s, Pout 23 dBm, RMC settings as per 3GPP TS 36.521-1 Annex A.2	102	114	118	117	mA
Average current consumption, radio resource control (RRC) mode, Cat-NB1						
I_{EDRX}	eDRX average current, 81.92 s, one PO/PTW, PTW = 2.56 s	33	-	33	-	µA
I_{IEDRX}	Idle eDRX average current, 655 s, one PO/PTW, PTW = 2.56 s	8	-	8	-	µA
I_{RMC_0DBM}	Pout 0 dBm, QPSK, 1SC, 15 kHz, TX 33% RX 33% ("balanced TX and RX"), RMC settings as per 3GPP TS 36.101 Annex A.2.4	30	30	30	30	mA
I_{RMC_10DBM}	Pout 10 dBm, QPSK, 1SC, 15 kHz, TX 33% RX 33% ("balanced TX and RX"), RMC settings as per 3GPP TS 36.101 Annex A.2.4	30	30	35	35	mA
I_{RMC_23DBM}	Pout 23 dBm, QPSK, 1SC, 15 kHz, TX 33% RX 33% ("balanced TX and RX"), RMC settings as per 3GPP TS 36.101 Annex A.2.4	90	100	105	100	mA
I_{RMC_0DBM}	Pout 0 dBm, BPSK, 1SC, 3.75 kHz, TX 80% RX 10% ("TX intensive"), RMC settings as per 3GPP TS 36.101 Annex A.2.4	50	50	50	50	mA
I_{RMC_10DBM}	Pout 10 dBm, BPSK, 1SC, 3.75 kHz, TX 80% RX 10% ("TX intensive"), RMC settings as per 3GPP TS 36.101 Annex A.2.4	55	55	60	60	mA
I_{RMC_23DBM}	Pout 23 dBm, BPSK, 1SC, 3.75 kHz, TX 80% RX 10% ("TX intensive"), RMC settings as per 3GPP TS 36.101 Annex A.2.4	180	200	225	205	mA

5.6.1.16 DECT NR+ current consumption

Symbol	Description	Typ.	Units
Average current consumption, nominal operating conditions			
I_{TX_-40DBM}	TX measured over one slot, Pout -40 dBm	TBA	mA
I_{TX_-20DBM}	TX measured over one slot, Pout -20 dBm	TBA	mA
I_{TX_0DBM}	TX measured over one slot, Pout 0 dBm	TBA	mA
I_{TX_10DBM}	TX measured over one slot, Pout 10 dBm	TBA	mA
I_{TX_19DBM}	TX measured over one slot, Pout 19 dBm	TBA	mA
I_{RX_-90DBM}	RX measured over one slot, Pin -90 dBm	TBA	mA

5.6.1.17 GPS current consumption

Symbol	Description	Min.	Typ.	Max.	Units
$I_{GPS\_CONTINUOUS}$	Continuous tracking, without power saving mode		43.1		mA
$I_{GPS\_CONTINUOUS\_PSM}$	Continuous tracking, power saving mode		7.8		mA
$I_{GPS\_PERIODIC}$	Periodic fix average current with A-GPS[13], one fix every 2 minutes		0.5		mA

5.7 Register description

5.7.1 POWER — Power control

The POWER module provides an interface to tasks, events, interrupt, and reset related configuration settings of the power management unit.

> **Note:** Registers INTEN on page 67, INTENSET on page 67, and INTENCLR on page 67 are the same registers (at the same address) as corresponding registers in CLOCK — Clock control on page 70.

5.7.1.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
POWER : S	0x50005000	US	NS	NA	No	Power control
POWER : NS	0x40005000					

Register overview

Register	Offset	TZ	Description
TASKS_CONSTLAT	0x78		Enable constant latency mode.
TASKS_LOWPWR	0x7C		Enable low power mode (variable latency)
SUBSCRIBE_CONSTLAT	0xF8		Subscribe configuration for task CONSTLAT
SUBSCRIBE_LOWPWR	0xFC		Subscribe configuration for task LOWPWR
EVENTS_POFWARN	0x108		Power failure warning
EVENTS_SLEEPENTER	0x114		CPU entered WFI/WFE sleep

[13] Including LTE current consumption.

Register	Offset	TZ	Description
EVENTS_SLEEPEXIT	0x118		CPU exited WFI/WFE sleep
PUBLISH_POFWARN	0x188		Publish configuration for event POFWARN
PUBLISH_SLEEPENTER	0x194		Publish configuration for event SLEEPENTER
PUBLISH_SLEEPEXIT	0x198		Publish configuration for event SLEEPEXIT
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
RESETREAS	0x400		Reset reason
POWERSTATUS	0x440		Modem domain power status
GPREGRET[n]	0x51C		General purpose retention register
LTEMODEM.STARTN	0x610		Start LTE modem
LTEMODEM.FORCEOFF	0x614		Force off LTE modem

5.7.1.1.1 TASKS_CONSTLAT

Address offset: 0x78

Enable constant latency mode.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_CONSTLAT			Enable constant latency mode.
			Trigger	1	Trigger task

5.7.1.1.2 TASKS_LOWPWR

Address offset: 0x7C

Enable low power mode (variable latency)

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_LOWPWR			Enable low power mode (variable latency)
			Trigger	1	Trigger task

5.7.1.1.3 SUBSCRIBE_CONSTLAT

Address offset: 0xF8

Subscribe configuration for task CONSTLAT

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																								A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task CONSTLAT will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

5.7.1.1.4 SUBSCRIBE_LOWPWR

Address offset: 0xFC

Subscribe configuration for task LOWPWR

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

5.7.1.1.5 EVENTS_POFWARN

Address offset: 0x108

Power failure warning

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_POFWARN																																	
			NotGenerated	0																															
			Generated	1																															

5.7.1.1.6 EVENTS_SLEEPENTER

Address offset: 0x114

CPU entered WFI/WFE sleep

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_SLEEPENTER																																	
			NotGenerated	0																															
			Generated	1																															

5.7.1.1.7 EVENTS_SLEEPEXIT

Address offset: 0x118

CPU exited WFI/WFE sleep

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_SLEEPEXIT																																	
			NotGenerated	0																															
			Generated	1																															

5.7.1.1.8 PUBLISH_POFWARN

Address offset: 0x188

Publish configuration for event POFWARN

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

5.7.1.1.9 PUBLISH_SLEEPENTER

Address offset: 0x194

Publish configuration for event SLEEPENTER

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

5.7.1.1.10 PUBLISH_SLEEPEXIT

Address offset: 0x198

Publish configuration for event SLEEPEXIT

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

5.7.1.1.11 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													E	D			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	POFWARN																											Enable or disable interrupt for event POFWARN						
			Disabled	0																									Disable						
			Enabled	1																									Enable						
D	RW	SLEEPENTER																											Enable or disable interrupt for event SLEEPENTER						
			Disabled	0																									Disable						
			Enabled	1																									Enable						
E	RW	SLEEPEXIT																											Enable or disable interrupt for event SLEEPEXIT						
			Disabled	0																									Disable						
			Enabled	1																									Enable						

5.7.1.1.12 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													E	D			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	POFWARN																											Write '1' to enable interrupt for event POFWARN						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
D	RW	SLEEPENTER																											Write '1' to enable interrupt for event SLEEPENTER						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
E	RW	SLEEPEXIT																											Write '1' to enable interrupt for event SLEEPEXIT						
			Set	1																									Enable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						

5.7.1.1.13 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													E	D			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	POFWARN																											Write '1' to disable interrupt for event POFWARN						
			Clear	1																									Disable						

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													E	D			A		
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
D	RW	SLEEPENTER																											Write '1' to disable interrupt for event SLEEPENTER						
			Clear	1																									Disable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						
E	RW	SLEEPEXIT																											Write '1' to disable interrupt for event SLEEPEXIT						
			Clear	1																									Disable						
			Disabled	0																									Read: Disabled						
			Enabled	1																									Read: Enabled						

5.7.1.1.14 RESETREAS

Address offset: 0x400

Reset reason

Note: Unless cleared, the RESETREAS register will be cumulative. A field is cleared by writing '1' to it. If none of the reset sources are flagged, this indicates that the chip was reset from the on-chip reset generator, which will indicate a power-on reset or a brownout reset.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																	G	F	E												D		C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	RESETPIN																											Reset from pin reset detected						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						
B	RW	DOG																											Reset from global watchdog detected						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						
C	RW	OFF																											Reset due to wakeup from System OFF mode, when wakeup is triggered by DETECT signal from GPIO						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						
D	RW	DIF																											Reset due to wakeup from System OFF mode, when wakeup is triggered by entering debug interface mode						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						
E	RW	SREQ																											Reset from AIRCR.SYSRESETREQ detected						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						
F	RW	LOCKUP																											Reset from CPU lock-up detected						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						
G	RW	CTRLAP																											Reset triggered through CTRL-AP						
			NotDetected	0																									Not detected						
			Detected	1																									Detected						

5.7.1.1.15 POWERSTATUS

Address offset: 0x440

Modem domain power status

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	LTEMODEM																																	
			OFF	0																															
			ON	1																															

5.7.1.1.16 GPREGRET[n] (n=0..1)

Address offset: 0x51C + (n × 0x4)

General purpose retention register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	GPREGRET																																	

General purpose retention register

This register is a retained register

5.7.1.1.17 LTEMODEM

LTE Modem

5.7.1.1.17.1 LTEMODEM.STARTN

Address offset: 0x610

Start LTE modem

> **Note:** Starting and stopping LTE modem must only be done through the LTE modem API to guarantee correct sequence in FW and HW and to avoid possible malfunctions.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	STARTN																																	
			Start	0																															
			Hold	1																															

5.7.1.1.17.2 LTEMODEM.FORCEOFF

Address offset: 0x614

Force off LTE modem

> **Note:** Starting and stopping LTE modem must only be done through the LTE modem API to guarantee correct sequence in FW and HW and to avoid possible malfunctions.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	FORCEOFF			Force off LTE modem
			Release	0	Release force off
			Hold	1	Hold force off active

5.7.2 CLOCK — Clock control

The CLOCK module provides one of the interfaces to power and clock management configuration settings.

Through CLOCK module it is able to configure the following:

- LFCLK clock source setup
- LFCLK and HFCLK status
- Tasks and events
- Interrupts
- Reset

Note: Registers INTEN on page 74, INTENSET on page 74, and INTENCLR on page 74 are the same registers (at the same address) as corresponding registers in POWER — Power control on page 63.

5.7.2.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
CLOCK : S	0x50005000	US	NS	NA	No	Clock control
CLOCK : NS	0x40005000					

Register overview

Register	Offset	TZ	Description
TASKS_HFCLKSTART	0x000		Start HFCLK source
TASKS_HFCLKSTOP	0x004		Stop HFCLK source
TASKS_LFCLKSTART	0x008		Start LFCLK source
TASKS_LFCLKSTOP	0x00C		Stop LFCLK source
SUBSCRIBE_HFCLKSTART	0x080		Subscribe configuration for task HFCLKSTART
SUBSCRIBE_HFCLKSTOP	0x084		Subscribe configuration for task HFCLKSTOP
SUBSCRIBE_LFCLKSTART	0x088		Subscribe configuration for task LFCLKSTART
SUBSCRIBE_LFCLKSTOP	0x08C		Subscribe configuration for task LFCLKSTOP
EVENTS_HFCLKSTARTED	0x100		HFCLK oscillator started
EVENTS_LFCLKSTARTED	0x104		LFCLK started
PUBLISH_HFCLKSTARTED	0x180		Publish configuration for event HFCLKSTARTED
PUBLISH_LFCLKSTARTED	0x184		Publish configuration for event LFCLKSTARTED
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
INTPEND	0x30C		Pending interrupts
HFCLKRUN	0x408		Status indicating that HFCLKSTART task has been triggered

Register	Offset	TZ	Description
HFCLKSTAT	0x40C		The register shows if HFXO has been requested by triggering HFCLKSTART task and if it has been started (STATE)
LFCLKRUN	0x414		Status indicating that LFCLKSTART task has been triggered
LFCLKSTAT	0x418		The register shows which LFCLK source has been requested (SRC) when triggering LFCLKSTART task and if the source has been started (STATE)
LFCLKSRCCOPY	0x41C		Copy of LFCLKSRC register, set after LFCLKSTART task has been triggered
LFCLKSRC	0x518		Clock source for the LFCLK. LFCLKSTART task starts a clock source selected with this register.

5.7.2.1.1 TASKS_HFCLKSTART

Address offset: 0x000

Start HFCLK source

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_HFCLKSTART			Start HFCLK source
			Trigger	1	Trigger task

5.7.2.1.2 TASKS_HFCLKSTOP

Address offset: 0x004

Stop HFCLK source

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_HFCLKSTOP			Stop HFCLK source
			Trigger	1	Trigger task

5.7.2.1.3 TASKS_LFCLKSTART

Address offset: 0x008

Start LFCLK source

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_LFCLKSTART			Start LFCLK source
			Trigger	1	Trigger task

5.7.2.1.4 TASKS_LFCLKSTOP

Address offset: 0x00C

Stop LFCLK source

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	TASKS_LFCLKSTOP																																	
			Trigger	1																															

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_LFCLKSTOP			Stop LFCLK source
			Trigger	1	Trigger task

5.7.2.1.5 SUBSCRIBE_HFCLKSTART

Address offset: 0x080

Subscribe configuration for task HFCLKSTART

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task HFCLKSTART will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

5.7.2.1.6 SUBSCRIBE_HFCLKSTOP

Address offset: 0x084

Subscribe configuration for task HFCLKSTOP

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task HFCLKSTOP will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

5.7.2.1.7 SUBSCRIBE_LFCLKSTART

Address offset: 0x088

Subscribe configuration for task LFCLKSTART

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task LFCLKSTART will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

5.7.2.1.8 SUBSCRIBE_LFCLKSTOP

Address offset: 0x08C

Subscribe configuration for task LFCLKSTOP

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task LFCLKSTOP will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

5.7.2.1.9 EVENTS_HFCLKSTARTED

Address offset: 0x100

HFCLK oscillator started

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_HFCLKSTARTED			HFCLK oscillator started
			NotGenerated	0	Event not generated
			Generated	1	Event generated

5.7.2.1.10 EVENTS_LFCLKSTARTED

Address offset: 0x104

LFCLK started

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_LFCLKSTARTED			LFCLK started
			NotGenerated	0	Event not generated
			Generated	1	Event generated

5.7.2.1.11 PUBLISH_HFCLKSTARTED

Address offset: 0x180

Publish configuration for event HFCLKSTARTED

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event HFCLKSTARTED will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

5.7.2.1.12 PUBLISH_LFCLKSTARTED

Address offset: 0x184

Publish configuration for event LFCLKSTARTED

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

5.7.2.1.13 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	HFCLKSTARTED																																	
			Disabled	0																															
			Enabled	1																															
B	RW	LFCLKSTARTED																																	
			Disabled	0																															
			Enabled	1																															

5.7.2.1.14 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	HFCLKSTARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	LFCLKSTARTED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

5.7.2.1.15 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	HFCLKSTARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
B	RW	LFCLKSTARTED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

Write '1' to disable interrupt for event HFCLKSTARTED

Write '1' to disable interrupt for event LFCLKSTARTED

5.7.2.1.16 INTPEND

Address offset: 0x30C

Pending interrupts

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	HFCLKSTARTED																																	
			NotPending	0																															
			Pending	1																															
B	R	LFCLKSTARTED																																	
			NotPending	0																															
			Pending	1																															

Read pending status of interrupt for event HFCLKSTARTED

Read pending status of interrupt for event LFCLKSTARTED

5.7.2.1.17 HFCLKRUN

Address offset: 0x408

Status indicating that HFCLKSTART task has been triggered

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	STATUS																																	
			NotTriggered	0																															
			Triggered	1																															

HFCLKSTART task triggered or not

5.7.2.1.18 HFCLKSTAT

Address offset: 0x40C

The register shows if HFXO has been requested by triggering HFCLKSTART task and if it has been started (STATE)

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																			B																A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	SRC																																	
			HFINT	0																															
			HFXO	1																															
B	R	STATE																																	
			NotRunning	0																															
			Running	1																															

ID	R/W	Field	Value ID	Value	Description
A	R	SRC			Active clock source
			HFINT	0	HFINT - 64 MHz on-chip oscillator
			HFXO	1	HFXO - 64 MHz clock derived from external 32 MHz crystal oscillator
B	R	STATE			HFCLK state
			NotRunning	0	HFXO has not been started or HFCLKSTOP task has been triggered
			Running	1	HFXO has been started (HFCLKSTARTED event has been generated)

5.7.2.1.19 LFCLKRUN

Address offset: 0x414

Status indicating that LFCLKSTART task has been triggered

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	STATUS																																	
			NotTriggered	0																															
			Triggered	1																															

ID	R/W	Field	Value ID	Value	Description
A	R	STATUS			LFCLKSTART task triggered or not
			NotTriggered	0	Task not triggered
			Triggered	1	Task triggered

5.7.2.1.20 LFCLKSTAT

Address offset: 0x418

The register shows which LFCLK source has been requested (SRC) when triggering LFCLKSTART task and if the source has been started (STATE)

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																			B															A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	SRC																																	
			RFU	0																															
			LFRC	1																															
			LFXO	2																															
B	R	STATE																																	
			NotRunning	0																															
			Running	1																															

ID	R/W	Field	Value ID	Value	Description
A	R	SRC			Active clock source
			RFU	0	Reserved for future use
			LFRC	1	32.768 kHz RC oscillator
			LFXO	2	32.768 kHz crystal oscillator
B	R	STATE			LFCLK state
			NotRunning	0	Requested LFCLK source has not been started or LFCLKSTOP task has been triggered
			Running	1	Requested LFCLK source has been started (LFCLKSTARTED event has been generated)

5.7.2.1.21 LFCLKSRCCOPY

Address offset: 0x41C

Copy of LFCLKSRC register, set after LFCLKSTART task has been triggered

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	SRC																																	
			RFU	0																															
			LFRC	1																															
			LFXO	2																															

Clock source

Reserved for future use

32.768 kHz RC oscillator

32.768 kHz crystal oscillator

5.7.2.1.22 LFCLKSRC

Address offset: 0x518

Clock source for the LFCLK. LFCLKSTART task starts a clock source selected with this register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		A	A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	SRC																																	
			RFU	0																															
			LFRC	1																															
			LFXO	2																															

Clock source

Reserved for future use (equals selecting LFRC)

32.768 kHz RC oscillator

32.768 kHz crystal oscillator

5.7.3 REGULATORS — Voltage regulators control

The REGULATORS module provides an interface to certain configuration settings of on-chip voltage regulators.

5.7.3.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
REGULATORS : S	0x50004000	US	NS	NA	No	Regulator configuration
REGULATORS : NS	0x40004000					

Register overview

Register	Offset	TZ	Description
SYSTEMOFF	0x500		System OFF register
EXTPOFCON	0x514		External power failure warning configuration
DCDCEN	0x578		Enable a step-down DC/DC voltage regulator

5.7.3.1.1 SYSTEMOFF

Address offset: 0x500

System OFF register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	SYSTEMOFF																																	
			Enable	1																															

5.7.3.1.2 EXTPOFCON

Address offset: 0x514

External power failure warning configuration

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	POF																																	
			Disabled	0																															
			Enabled	1																															

5.7.3.1.3 DCDCEN

Address offset: 0x578

Enable a step-down DC/DC voltage regulator

Note: DCDCEN must be set to 1 (enabled) before the LTE modem is started.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	DCDCEN																																	
			Disabled	0																															
			Enabled	1																															

6 Peripherals

The nRF9161 application core peripherals are found in Instantiation on page 25.

6.1 CRYPTOCELL — ARM TrustZone CryptoCell 310

ARM TrustZone CryptoCell 310 (CRYPTOCELL) is a security subsystem which provides root of trust (RoT) and cryptographic services for a device.

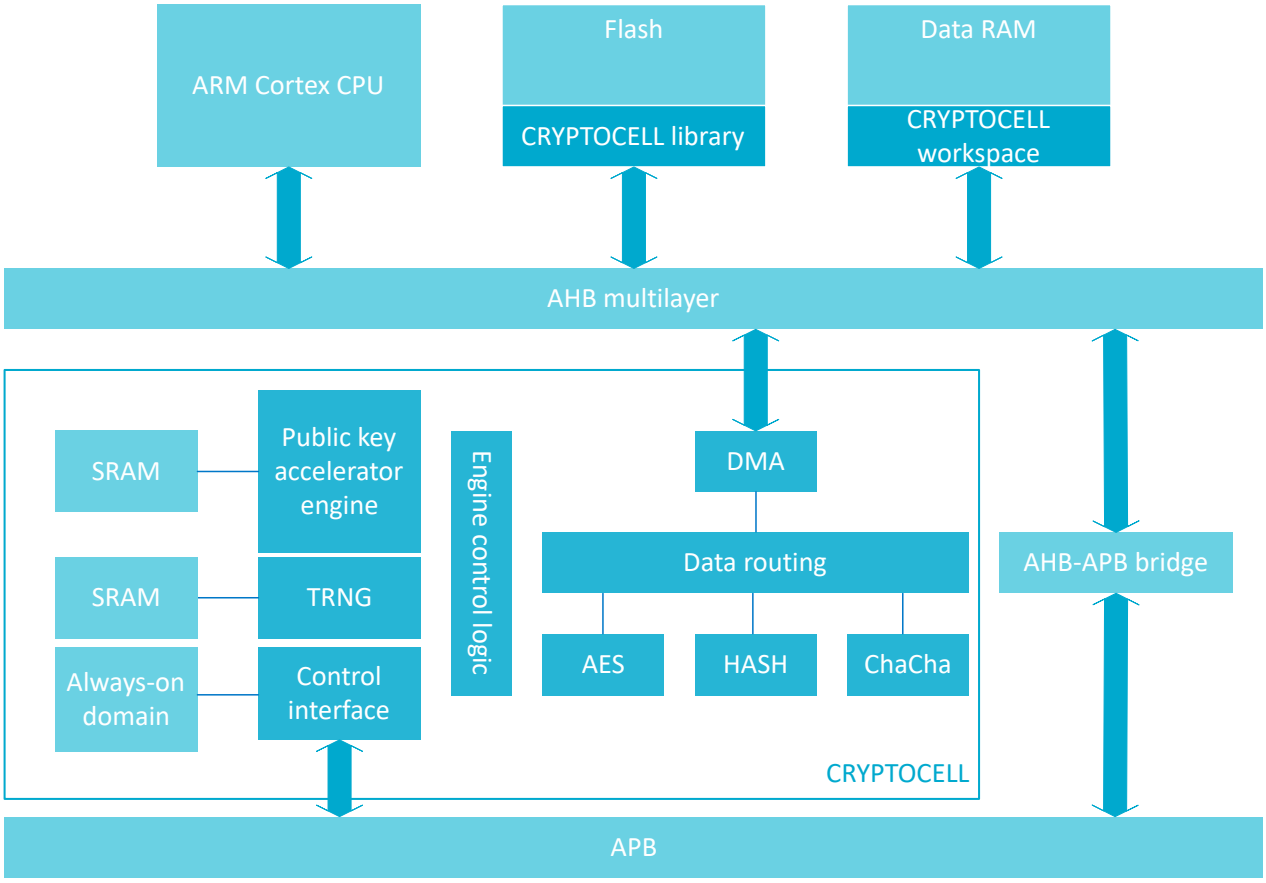

Figure 14: Block diagram for CRYPTOCELL

The following cryptographic features are provided:

- True random number generator (TRNG) compliant with NIST 800-90B, AIS-31, and FIPS 140-2
- Pseudorandom number generator (PRNG) using underlying AES engine compliant with NIST 800-90A
- RSA public key cryptography
  - Up to 2048-bit key size
  - PKCS#1 v2.1/v1.5
  - Optional CRT support
- Elliptic curve cryptography (ECC)
  - NIST FIPS 186-4 recommended curves using pseudorandom parameters, up to 521 bits:
    - Prime field: P-192, P-224, P-256, P-384, P-521
  - SEC 2 recommended curves using pseudorandom parameters, up to 521 bits:

    - Prime field: secp160r1, secp192r1, secp224r1, secp256r1, secp384r1, secp521r1
  - Koblitz curves using fixed parameters, up to 256 bits:
    - Prime field: secp160k1, secp192k1, secp224k1, secp256k1
  - Edwards/Montgomery curves:
    - Ed25519, Curve25519
  - ECDH/ECDSA support
- Secure remote password protocol (SRP)
  - Up to 3072-bit operations
- Hashing functions
  - SHA-1, SHA-2 up to 256 bits
  - Keyed-hash message authentication code (HMAC)
- AES symmetric encryption
  - General purpose AES engine (encrypt/decrypt, sign/verify)
  - 128-bit key size
  - Supported encryption modes: ECB, CBC, CMAC/CBC-MAC, CTR, CCM/CCM* (CCM* is a minor variation of CCM)
- ChaCha20/Poly1305 symmetric encryption
  - Supported key size: 128 and 256 bits
  - Authenticated encryption with associated data (AEAD) mode

6.1.1 Usage

The CRYPTOCELL state is controlled via a register interface. The cryptographic functions of CRYPTOCELL are accessible by using a software library provided in the device SDK, not directly via a register interface.

To enable CRYPTOCELL, use register ENABLE on page 83.

> **Note:** Keeping the CRYPTOCELL subsystem enabled will prevent the device from reaching the System ON, All Idle state.

6.1.2 Always-on (AO) power domain

The CRYPTOCELL subsystem has an internal always-on (AO) power domain for retaining device secrets when CRYPTOCELL is disabled.

The following information is retained by the AO power domain:

- 4 bits indicating the configured CRYPTOCELL lifecycle state (LCS)
- 1 bit indicating if the hard-coded RTL key, K_{PRTL} (see RTL key on page 81), is available for use
- 128-bit device root key, K_{DR} (see Device root key on page 81)

A reset from any reset source will erase the content in the AO power domain.

6.1.3 Lifecycle state (LCS)

Lifecycle refers to multiple states a device goes through during its lifetime. Two valid lifecycle states are offered for the device - debug and secure.

The CRYPTOCELL subsystem lifecycle state (LCS) is controlled through register HOST_IOT_LCS on page 85. A valid LCS is configured by writing either value `Debug` or `Secure` into the LCS field of this register. A correctly configured LCS can be validated by reading back the read-only field LCS_IS_VALID from the abovementioned register. The LCS_IS_VALID field value will change from `Invalid` to `Valid` once a valid LCS value has been written.

LCS field value	LCS_IS_VALID field value	Description
Secure	Invalid	Default reset value indicating that LCS has not been configured.
Secure	Valid	LCS set to secure mode, and LCS is valid. Registers HOST_IOT_KDR[0..3] can only be written once per reset cycle. Any additional writes will be ignored.
Debug	Valid	LCS set to debug mode, and LCS is valid. Registers HOST_IOT_KDR[0..3] can be written multiple times.

Table 14: Lifecycle states

6.1.4 Cryptographic key selection

The CRYPTOCELL subsystem can be instructed to operate on different cryptographic keys.

Through register HOST_CRYPTOKEY_SEL on page 83, the following key types can be selected for cryptographic operations:

- RTL key K_{PRTL}
- Device root key K_{DR}
- Session key

K_{PRTL} and K_{DR} are configured as part of the CRYPTOCELL initialization process, while session keys are provided by the application through the software library API.

6.1.4.1 RTL key

The ARM TrustZone CryptoCell 310 contains one hard-coded RTL key referred to as K_{PRTL}. This key is set to the same value for all devices with the same part code in the hardware design and cannot be changed.

The K_{PRTL} key can be requested for use in cryptographic operations by the CRYPTOCELL, without revealing the key value itself. Access to use of K_{PRTL} in cryptographic operations can be disabled until next reset by writing to register HOST_IOT_KPRTL_LOCK on page 84. If a locked K_{PRTL} key is requested for use, a zero vector key will be routed to the AES engine instead.

6.1.4.2 Device root key

The device root key K_{DR} is a 128-bit AES key programmed into the CRYPTOCELL subsystem using firmware. It is retained in the AO power domain until the next reset.

Once configured, it is possible to perform cryptographic operations using the CRYPTOCELL subsystem where K_{DR} is selected as key input without having access to the key value itself. The K_{DR} key value must be written to registers HOST_IOT_KDR[0..3]. These 4 registers are write-only if LCS is set to debug mode, and write-once if LCS is set to secure mode. The K_{DR} key value is successfully retained when the read-back value of register HOST_IOT_KDR0 on page 84 changes to 1.

6.1.5 Direct memory access (DMA)

The CRYPTOCELL subsystem implements direct memory access (DMA) for accessing memory without CPU intervention.

Any data stored in memory type(s) not accessible by the DMA engine must be copied to SRAM before it can be processed by the CRYPTOCELL subsystem. Maximum DMA transaction size is limited to 2^{16}-1 bytes.

6.1.6 Standards

ARM TrustZone CryptoCell 310 (CRYPTOCELL) supports a number of cryptography standards.

Algorithm family	Identification code	Document title
TRNG	NIST SP 800-90B	*Recommendation for the Entropy Sources Used for Random Bit Generation*
	AIS-31	*A proposal for: Functionality classes and evaluation methodology for physical random number generators*
	FIPS 140-2	*Security Requirements for Cryptographic Modules*
PRNG	NIST SP 800-90A	*Recommendation for Random Number Generation Using Deterministic Random Bit Generators*
Stream cipher	Chacha	*ChaCha, a variant of Salsa20*, Daniel J. Bernstein, January 28th 2008
MAC	Poly1305	*The Poly1305-AES message-authentication code*, Daniel J. Bernstein *Cryptography in NaCl*, Daniel J. Bernstein
Key agreement	SRP	*The Secure Remote Password Protocol*, Thomas Wu, November 11th 1997
AES	FIPS-197	*Advanced Encryption Standard (AES)*
	NIST SP 800-38A	*Recommendation for Block Cipher Modes of Operation - Methods and Techniques*
	NIST SP 800-38B	*Recommendation for Block Cipher Modes of Operation: The CMAC Mode for Authentication*
	NIST SP 800-38C	*Recommendation for Block Cipher Modes of Operation: The CCM Mode for Authentication and Confidentiality*
	ISO/IEC 9797-1	AES CBC-MAC per ISO/IEC 9797-1 MAC algorithm 1
	IEEE 802.15.4-2011	*IEEE Standard for Local and metropolitan area networks - Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs)*, Annex B.4: *Specification of generic CCM* mode of operation*
Hash	FIPS 180-3	Secure Hash Standard (SHA1, SHA-224, SHA-256)
	RFC2104	*HMAC: Keyed-Hashing for Message Authentication*
RSA	PKCS#1	*Public-Key Cryptography Standards (PKCS) #1: RSA Cryptography Specifications* v1.5/2.1
Diffie-Hellman	ANSI X9.42	*Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography*
	PKCS#3	*Diffie-Hellman Key-Agreement Standard*
ECC	ANSI X9.63	*Public Key Cryptography for the Financial Services Industry - Key Agreement and Key Transport Using Elliptic Curve Cryptography*
	IEEE 1363	*Standard Specifications for Public-Key Cryptography*
	ANSI X9.62	*Public Key Cryptography For The Financial Services Industry: The Elliptic Curve Digital Signature Algorithm (ECDSA)*
	Ed25519	Edwards-curve, *Ed25519: high-speed high-security signatures*, Daniel J. Bernstein, Niels Duif, Tanja Lange, Peter Schwabe, and Bo-Yin Yang
	Curve25519	Montgomery curve, *Curve25519: new Diffie-Hellman speed records*, Daniel J. Bernstein
	FIPS 186-4	*Digital Signature Standard (DSS)*
	SEC 2	*Recommended Elliptic Curve Domain Parameters*, Certicom Research
	NIST SP 800-56A rev. 2	*Recommendation for Pair-Wise Key Establishment Schemes Using Discrete Logarithm Cryptography*

Table 15: CRYPTOCELL cryptography standards

6.1.7 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
CRYPTOCELL	0x50840000	HF	S	NSA	No	CryptoCell sub-system control interface

Register overview

Register	Offset	TZ	Description
ENABLE	0x500		Enable CRYPTOCELL subsystem

6.1.7.1 ENABLE

Address offset: 0x500

Enable CRYPTOCELL subsystem

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			Enable or disable the CRYPTOCELL subsystem
			Disabled	0	CRYPTOCELL subsystem disabled
			Enabled	1	CRYPTOCELL subsystem enabled. When enabled the CRYPTOCELL subsystem can be initialized and controlled through the CryptoCell firmware API.

6.1.8 Host interface

This chapter describes host registers used to control the CRYPTOCELL subsystem behavior.

6.1.8.1 HOST_RGF block

The HOST_RGF block contains registers for configuring LCS and device root key K_{DR}, in addition to selecting which cryptographic key is connected to the AES engine.

6.1.8.1.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
CC_HOST_RGF	0x50840000	HF	S	NSA	No	Host platform interface

Register overview

Register	Offset	TZ	Description
HOST_CRYPTOKEY_SEL	0x1A38		AES hardware key select
HOST_IOT_KPRTL_LOCK	0x1A4C		This write-once register is the K_PRTL lock register. When this register is set, K_PRTL cannot be used and a zeroed key will be used instead. The value of this register is saved in the CRYPTOCELL AO power domain.
HOST_IOT_KDR0	0x1A50		This register holds bits 31:0 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain. Reading from this address returns the K_DR valid status indicating if K_DR is successfully retained.
HOST_IOT_KDR1	0x1A54		This register holds bits 63:32 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain.
HOST_IOT_KDR2	0x1A58		This register holds bits 95:64 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain.
HOST_IOT_KDR3	0x1A5C		This register holds bits 127:96 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain.
HOST_IOT_LCS	0x1A60		Controls lifecycle state (LCS) for CRYPTOCELL subsystem

6.1.8.1.1.1 HOST_CRYPTOKEY_SEL

Address offset: 0x1A38

AES hardware key select

> **Note:** If the HOST_IOT_KPRTL_LOCK register is set, and the HOST_CRYPTOKEY_SEL register set to 1, then the HW key that is connected to the AES engine is zero

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	HOST_CRYPTOKEY_SEL																																	
			K_DR	0																															
			K_PRTL	1																															
			Session	2																															

Select the source of the HW key that is used by the AES engine

Use device root key K_DR from CRYPTOCELL AO power domain

Use hard-coded RTL key K_PRTL

Use provided session key

6.1.8.1.1.2 HOST_IOT_KPRTL_LOCK

Address offset: 0x1A4C

This write-once register is the K_PRTL lock register. When this register is set, K_PRTL cannot be used and a zeroed key will be used instead. The value of this register is saved in the CRYPTOCELL AO power domain.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	HOST_IOT_KPRTL_LOCK																																	
			Disabled	0																															
			Enabled	1																															

This register is the K_PRTL lock register. When this register is set, K_PRTL cannot be used and a zeroed key will be used instead. The value of this register is saved in the CRYPTOCELL AO power domain.

K_PRTL can be selected for use from register HOST_CRYPTOKEY_SEL

K_PRTL has been locked until next power-on reset (POR). If K_PRTL is selected anyway, a zeroed key will be used instead.

6.1.8.1.1.3 HOST_IOT_KDR0

Address offset: 0x1A50

This register holds bits 31:0 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain. Reading from this address returns the K_DR valid status indicating if K_DR is successfully retained.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	HOST_IOT_KDR0																																	

Write: K_DR bits 31:0.

Read: 0x00000000 when 128-bit K_DR key value is not yet retained in the CRYPTOCELL AO power domain.

Read: 0x00000001 when 128-bit K_DR key value is successfully retained in the CRYPTOCELL AO power domain.

6.1.8.1.1.4 HOST_IOT_KDR1

Address offset: 0x1A54

This register holds bits 63:32 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	HOST_IOT_KDR1			K_DR bits 63:32

6.1.8.1.1.5 HOST_IOT_KDR2

Address offset: 0x1A58

This register holds bits 95:64 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	HOST_IOT_KDR2			K_DR bits 95:64

6.1.8.1.1.6 HOST_IOT_KDR3

Address offset: 0x1A5C

This register holds bits 127:96 of K_DR. The value of this register is saved in the CRYPTOCELL AO power domain.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	HOST_IOT_KDR3			K_DR bits 127:96

6.1.8.1.1.7 HOST_IOT_LCS

Address offset: 0x1A60

Controls lifecycle state (LCS) for CRYPTOCELL subsystem

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																								B						A	A	A
Reset 0x00000002	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	LCS			Lifecycle state value. This field is write-once per reset.
			Debug	0	CC310 operates in debug mode
			Secure	2	CC310 operates in secure mode
B	RW	LCS_IS_VALID			Read-only field. Indicates if CRYPTOCELL LCS has been successfully configured since last reset.
			Invalid	0	Valid LCS not yet retained in the CRYPTOCELL AO power domain
			Valid	1	Valid LCS successfully retained in the CRYPTOCELL AO power domain

6.2 DPPI - Distributed programmable peripheral interconnect

The distributed programmable peripheral interconnect (DPPI) enables peripherals to interact autonomously with each other by using tasks and events, without any intervention from the CPU. DPPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU involvement to implement behavior which can be predefined using the DPPI.

> **Note:** For more information on tasks, events, publish/subscribe, interrupts, and other concepts, see Peripheral interface on page 15.

The DPPI has the following features:

- Peripheral tasks can subscribe to channels
- Peripheral events can be published on channels
- Publish/subscribe pattern enabling multiple connection options that include the following:
  - One-to-one
  - One-to-many
  - Many-to-one
  - Many-to-many

The DPPI consists of several PPIBus modules, which are connected to a fixed number of DPPI channels and a DPPI configuration (DPPIC).

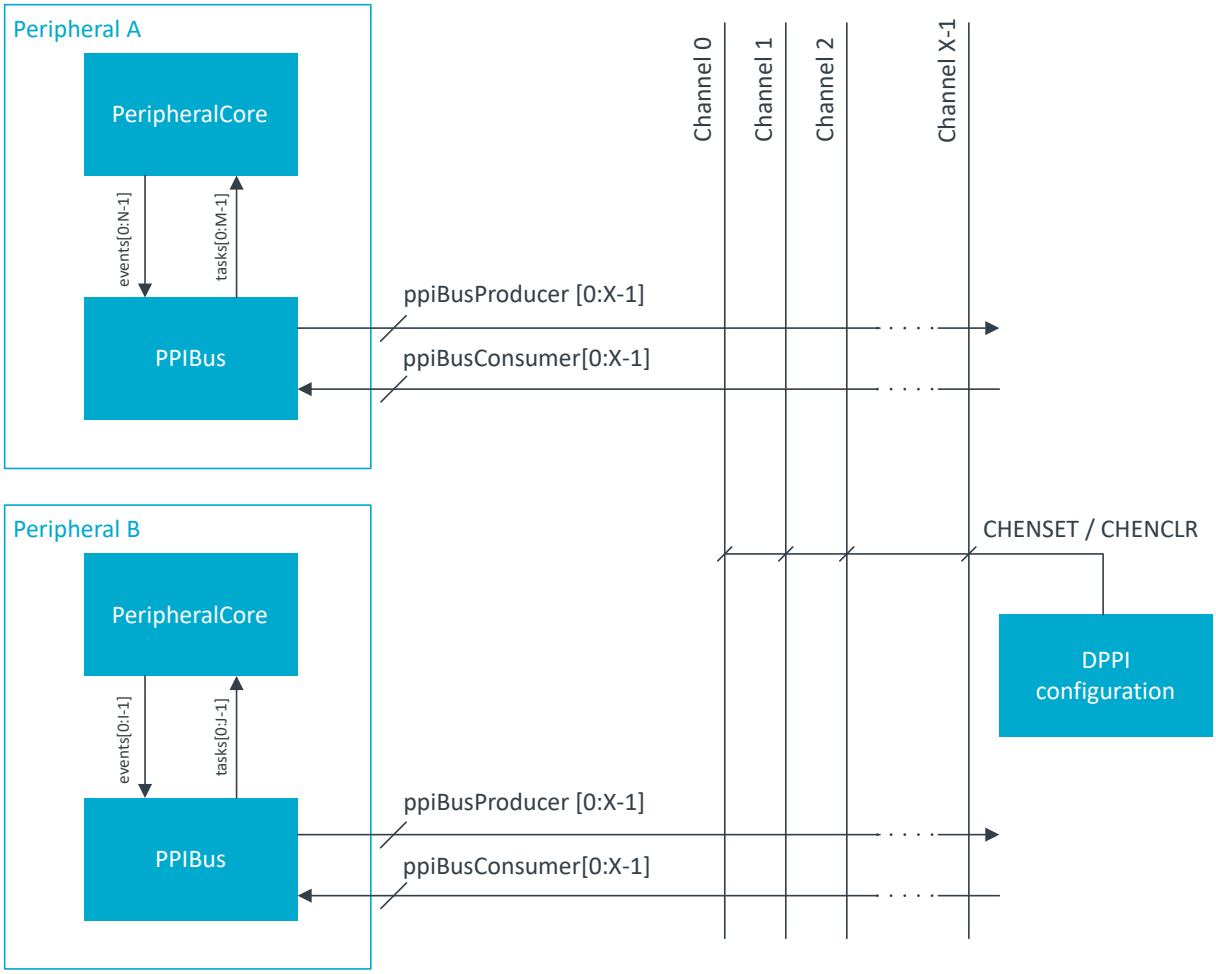

Figure 15: DPPI overview

6.2.1 Subscribing to and publishing on channels

The PPIBus can route peripheral events onto the channels (publishing), or route events from the channels into peripheral tasks (subscribing).

All peripherals include the following:

- One subscribe register per task
- One publish register per event

Publish and subscribe registers use a channel index field to determine the channel to which the event is published or tasks subscribed. In addition, there is an enable bit for the subscribe and publish registers that needs to be enabled before the subscription or publishing takes effect.

Writing non-existing channel index (CHIDX) numbers into a peripheral's publish or subscribe registers will yield unexpected results.

One event can trigger multiple tasks by subscribing different tasks to the same channel. Similarly, one task can be triggered by multiple events by publishing different events to the same channel. For advanced use cases, multiple events and multiple tasks can connect to the same channel forming a many-to-many connection. If multiple events are published on the same channel at the same time, the events are merged and only one event is routed through the DPPI.

How peripheral events are routed onto different channels based on publish registers is illustrated in the following figure.

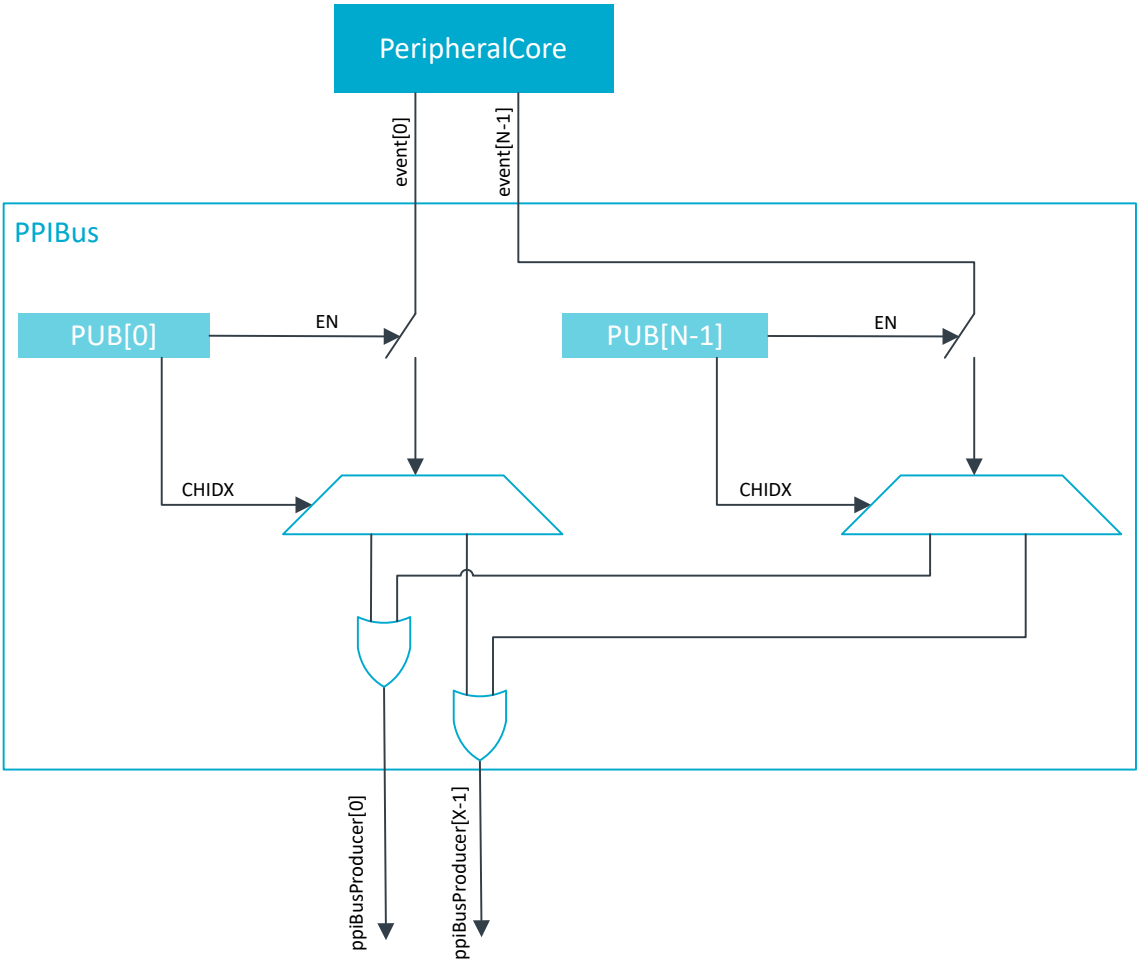

Figure 16: DPPI events flow

The following figure illustrates how peripheral tasks are triggered from different channels based on subscribe registers.

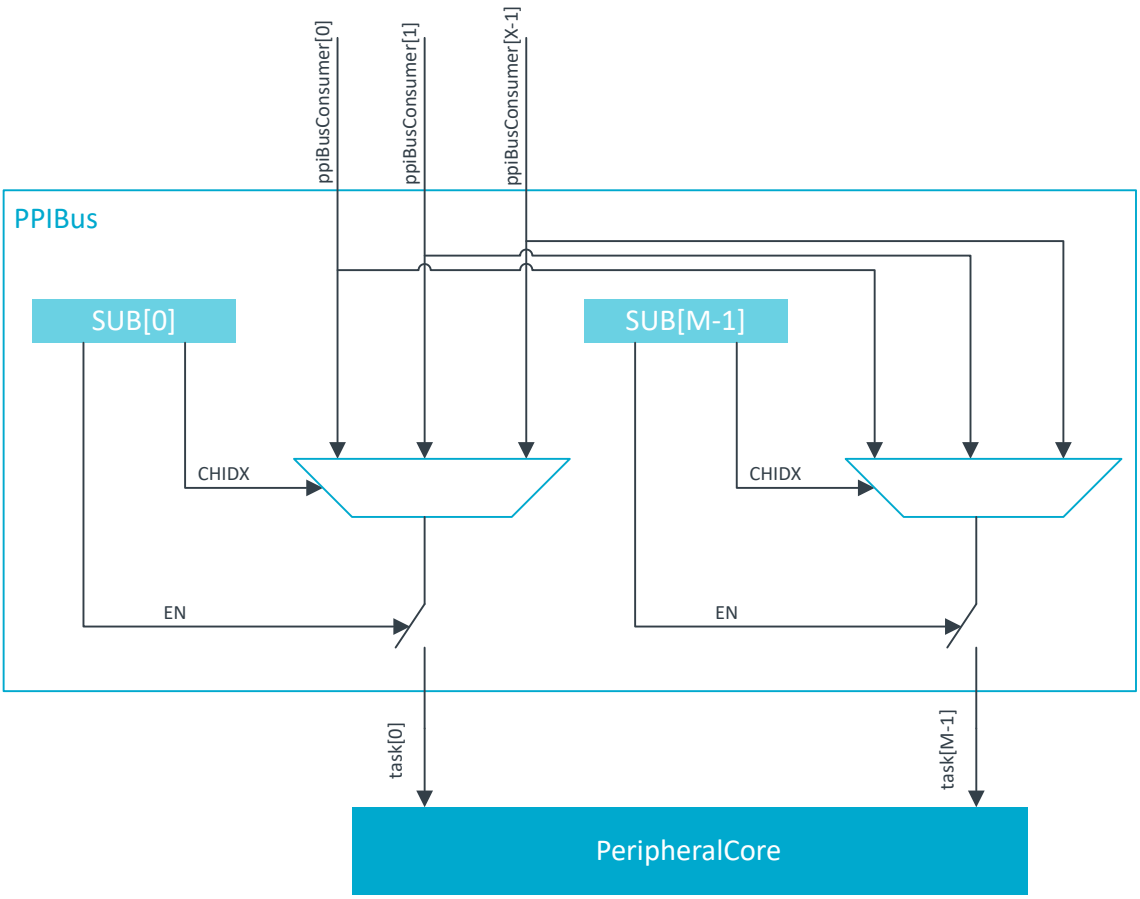

Figure 17: DPPI tasks flow

6.2.2 DPPI configuration (DPPIC)

Enabling and disabling of channels globally is handled through the DPPI configuration (DPPIC). Connection (connect/disconnect) between a channel and a peripheral is handled locally by the PPIBus.

There are two ways of enabling and disabling global channels using the DPPI configuration:

- Enable or disable channels individually using registers CHEN, CHENSET, and CHENCLR.
- Enable or disable channels in channel groups using the groups' tasks ENABLE and DISABLE. It needs to be defined which channels belong to which channel groups before these tasks are triggered.

> **Note:** ENABLE tasks are prioritized over DISABLE tasks. When a channel belongs to two or more groups, for example group m and n, and the tasks CHG[m].EN and CHG[n].DIS occur simultaneously (m and n can be equal or different), the CHG[m].EN task on that channel is prioritized.

The DPPI configuration tasks (for example CHG[0].EN) can be triggered through DPPI like any other task, which means they can be linked to a DPPI channel through the subscribe registers.

In order to write to CHG[x], the corresponding CHG[x].EN and CHG[x].DIS subscribe registers must be disabled. Writes to CHG[x] are ignored if any of the two subscribe registers are enabled.

6.2.3 Connection examples

DPPI offers several connection options. Examples are given for how to create one-to-one and many-to-many connections.

One-to-one connection

This example shows how to create a one-to-one connection between TIMER compare register and SAADC start task.

The channel configuration is set up first. TIMER0 will publish its COMPARE0 event on channel 0, and SAADC will subscribe its START task to events on the same channel. After that, the channel is enabled through the DPPIC.

```
NRF_TIMER0->PUBLISH_COMPARE0 = (DPPI_PUB_CHIDX_Ch0) |
                               (DPPI_PUB_EN_Msk);
NRF_SAADC->SUBSCRIBE_START   = (DPPI_SUB_CHIDX_Ch0) |
                               (DPPI_SUB_EN_Msk);

NRF_DPPIC->CHENSET = (DPPI_CHENSET_CH0_Set << DPPI_CHENSET_CH0_Pos);
```

Many-to-many connection

The example shows how to create a many-to-many connection, showcasing the DPPIC's channel group functionality.

A channel group that includes only channel 0 is set up first. Then the GPIOTE and TIMER0 configure their IN0 and COMPARE0 events respectively to be published on channel 0, while the SAADC configures its START task to subscribe to events on channel 0. Through DPPIC, the CHG0 DISABLE task is configured to subscribe to events on channel 0. After an event is received on channel 0 it will be disabled. Finally, channel 0 is enabled using the DPPIC task to enable a channel group.

```
NRF_DPPIC->CHG[0] = (DPPI_CHG_CH0_Included << PPI_CHG_CH0_Pos);

NRF_GPIOTE->PUBLISH_IN0         = (DPPI_PUB_CHIDX_Ch0) |
                                  (DPPI_PUB_EN_Msk);
NRF_TIMER0->PUBLISH_COMPARE0    = (DPPI_PUB_CHIDX_Ch0) |
                                  (DPPI_PUB_EN_Msk);
NRF_SAADC->SUBSCRIBE_START      = (DPPI_SUB_CHIDX_Ch0) |
                                  (DPPI_SUB_EN_Msk);
NRF_DPPIC->SUBSCRIBE_CHG[0].DIS = (DPPI_SUB_CHIDX_Ch0) |
                                  (DPPI_SUB_EN_Msk);

NRF_DPPIC->TASK_CHG[0].EN = 1;
```

6.2.4 Special considerations for a system implementing TrustZone for Cortex-M processors

DPPI is implemented with split security, meaning it handles both secure and non-secure accesses. In a system implementing the TrustZone for Cortex-M technology, DPPI channels can be defined as secure or non-secure using the SPU.

A peripheral configured as non-secure will only be able to subscribe to or publish on non-secure DPPI channels. A peripheral configured as secure will be able to access all DPPI channels. DPPI handles both secure and non-secure accesses, but behaves differently depending on the access type:

- A non-secure peripheral access can only configure and control the DPPI channels defined as non-secure in the SPU.DPPI.PERM[] register(s)

- A secure peripheral access can control all the DPPI channels, independently of the SPU.DPPI.PERM[] register(s)

A group of channels can be created, making it possible to simultaneously enable or disable all channels within the group. The security attribute of a group of channels (secure or non-secure) is defined as follows:

- If all channels (enabled or not) within a group are non-secure, then the group is considered non-secure
- If at least one of the channels (enabled or not) within the group is secure, then the group is considered secure

A non-secure access to a DPPI register, or a bit field, controlling a channel marked as secure in SPU.DPPI[].PERM register(s) will be ignored. Write accesses will have no effect, and read accesses will always return a zero value.

No exceptions are triggered when non-secure accesses target a register or a bit field controlling a secure channel. For example, if the bit `i` is set in the SPU.DPPI[0].PERM register (declaring DPPI channel i as secure), then:

- Non-secure write accesses to registers CHEN, CHENSET, and CHENCLR cannot write bit `i` of these registers
- Non-secure write accesses to TASK_CHG[j].EN and TASK_CHG[j].DIS registers are ignored if the channel group `j` contains at least one channel defined as secure (it can be the channel i itself or any channel declared as secure)
- Non-secure read accesses to registers CHEN, CHENSET, and CHENCLR always read 0 for the bit at position `i`

For the channel configuration registers (CHG[]), access from non-secure code is only possible if the included channels are all non-secure, whether the channels are enabled or not. If a CHG[g] register included one or more secure channel(s), then the group `g` is considered as secure, and only secure transfers can read to or write from CHG[g]. A non-secure write access is ignored, and a non-secure read access returns 0.

The DPPI can subscribe to secure and non-secure channels through the SUBSCRIBE_CHG[] registers, in order to trigger the task for enabling or disabling groups of channels. An event from a secure channel will be ignored if the group subscribing to this channel is non-secure. A secure group can subscribe to a non-secure channel or a secure channel.

6.2.5 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
DPPIC : S	0x50017000	HF	NS	NA	Yes	DPPI configuration
DPPIC : NS	0x40017000					

Register overview

Register	Offset	TZ	Description
TASKS_CHG[n].EN	0x000		Enable channel group n
TASKS_CHG[n].DIS	0x004		Disable channel group n
SUBSCRIBE_CHG[n].EN	0x080		Subscribe configuration for task CHG[n].EN
SUBSCRIBE_CHG[n].DIS	0x084		Subscribe configuration for task CHG[n].DIS
CHEN	0x500		Channel enable register
CHENSET	0x504		Channel enable set register
CHENCLR	0x508		Channel enable clear register
CHG[n]	0x800		Channel group n Note: Writes to this register are ignored if either SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is enabled

6.2.5.1 TASKS_CHG[n] (n=0..5)

Channel group tasks

6.2.5.1.1 TASKS_CHG[n].EN (n=0..5)

Address offset: 0x000 + (n × 0x8)

Enable channel group n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	EN			Enable channel group n
			Trigger	1	Trigger task

6.2.5.1.2 TASKS_CHG[n].DIS (n=0..5)

Address offset: 0x004 + (n × 0x8)

Disable channel group n

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	DIS			Disable channel group n
			Trigger	1	Trigger task

6.2.5.2 SUBSCRIBE_CHG[n] (n=0..5)

Subscribe configuration for tasks

6.2.5.2.1 SUBSCRIBE_CHG[n].EN (n=0..5)

Address offset: 0x080 + (n × 0x8)

Subscribe configuration for task CHG[n].EN

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	CHIDX		[0..255]																								DPPI channel that task CHG[n].EN will subscribe to							
B	RW	EN																																	
			Disabled	0																								Disable subscription							
			Enabled	1																								Enable subscription							

6.2.5.2.2 SUBSCRIBE_CHG[n].DIS (n=0..5)

Address offset: 0x084 + (n × 0x8)

Subscribe configuration for task CHG[n].DIS

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	CHIDX		[0..255]																								DPPI channel that task CHG[n].DIS will subscribe to							
B	RW	EN																																	
			Disabled	0																								Disable subscription							
			Enabled	1																								Enable subscription							

6.2.5.3 CHEN

Address offset: 0x500

Channel enable register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A-P	RW	CH[i] (i=0..15)																										Enable or disable channel i							
			Disabled	0																								Disable channel							
			Enabled	1																								Enable channel							

6.2.5.4 CHENSET

Address offset: 0x504

Channel enable set register

Note: Read: Reads value of CHi field in CHEN register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																Description															
A-P	RW	CH[i] (i=0..15)																		Channel i enable set register. Writing 0 has no effect.															
	W1S																																		
			Disabled	0																Read: Channel disabled															
			Enabled	1																Read: Channel enabled															
			Set	1																Write: Enable channel															

6.2.5.5 CHENCLR

Address offset: 0x508

Channel enable clear register

Note: Read: Reads value of CHi field in CHEN register

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																Description															
A-P	RW	CH[i] (i=0..15)																		Channel i enable clear register. Writing 0 has no effect.															
	W1C																																		
			Disabled	0																Read: Channel disabled															
			Enabled	1																Read: Channel enabled															
			Clear	1																Write: Disable channel															

6.2.5.6 CHG[n] (n=0..5)

Address offset: 0x800 + (n × 0x4)

Channel group n

Note: Writes to this register are ignored if either SUBSCRIBE_CHG[n].EN or SUBSCRIBE_CHG[n].DIS is enabled

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																				P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																Description															
A-P	RW	CH[i] (i=0..15)																		Include or exclude channel i															
			Excluded	0																Exclude															
			Included	1																Include															

6.3 EGU — Event generator unit

Event generator unit (EGU) provides support for interlayer signaling. This means providing support for atomic triggering of both CPU execution and hardware tasks, from both firmware (by CPU) and hardware (by PPI). This feature can, for instance, be used for triggering CPU execution at a lower priority execution from a higher priority execution, or to handle a peripheral's interrupt service routine (ISR) execution at a lower priority for some of its events. However, triggering any priority from any priority is possible.

Listed here are the main EGU features:

- Software-enabled interrupt triggering
- Separate interrupt vectors for every EGU instance
- Up to 16 separate event flags per interrupt for multiplexing

Each instance of EGU implements a set of tasks which can individually be triggered to generate the corresponding event, for example, the corresponding event for TASKS_TRIGGER[n] is EVENTS_TRIGGERED[n]. See Instances on page 95 for a list of EGU instances.

6.3.1 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
EGU0 : S EGU0 : NS	0x5001B000 0x4001B000	US	NS	NA	No	Event generator unit 0
EGU1 : S EGU1 : NS	0x5001C000 0x4001C000	US	NS	NA	No	Event generator unit 1
EGU2 : S EGU2 : NS	0x5001D000 0x4001D000	US	NS	NA	No	Event generator unit 2
EGU3 : S EGU3 : NS	0x5001E000 0x4001E000	US	NS	NA	No	Event generator unit 3
EGU4 : S EGU4 : NS	0x5001F000 0x4001F000	US	NS	NA	No	Event generator unit 4
EGU5 : S EGU5 : NS	0x50020000 0x40020000	US	NS	NA	No	Event generator unit 5

Register overview

Register	Offset	TZ	Description
TASKS_TRIGGER[n]	0x000		Trigger n for triggering the corresponding TRIGGERED[n] event
SUBSCRIBE_TRIGGER[n]	0x080		Subscribe configuration for task TRIGGER[n]
EVENTS_TRIGGERED[n]	0x100		Event number n generated by triggering the corresponding TRIGGER[n] task
PUBLISH_TRIGGERED[n]	0x180		Publish configuration for event TRIGGERED[n]
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt

6.3.1.1 TASKS_TRIGGER[n] (n=0..15)

Address offset: 0x000 + (n × 0x4)

Trigger n for triggering the corresponding TRIGGERED[n] event

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_TRIGGER			Trigger n for triggering the corresponding TRIGGERED[n] event
			Trigger	1	Trigger task

6.3.1.2 SUBSCRIBE_TRIGGER[n] (n=0..15)

Address offset: 0x080 + (n × 0x4)

Subscribe configuration for task TRIGGER[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																								A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task TRIGGER[n] will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

6.3.1.3 EVENTS_TRIGGERED[n] (n=0..15)

Address offset: 0x100 + (n × 0x4)

Event number n generated by triggering the corresponding TRIGGER[n] task

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_TRIGGERED			Event number n generated by triggering the corresponding TRIGGER[n] task
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.3.1.4 PUBLISH_TRIGGERED[n] (n=0..15)

Address offset: 0x180 + (n × 0x4)

Publish configuration for event TRIGGERED[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																								A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event TRIGGERED[n] will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

6.3.1.5 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-P	RW	TRIGGERED[i] (i=0..15)			Enable or disable interrupt for event TRIGGERED[i]
			Disabled	0	Disable
			Enabled	1	Enable

6.3.1.6 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-P	RW	TRIGGERED[i] (i=0..15)			Write '1' to enable interrupt for event TRIGGERED[i]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.3.1.7 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-P	RW	TRIGGERED[i] (i=0..15)			Write '1' to disable interrupt for event TRIGGERED[i]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.3.2 Electrical specification

6.3.2.1 EGU Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$t_{EGU,EVT}$	Latency between setting an EGU event flag and the system setting an interrupt		1		cycles

6.4 GPIO — General purpose input/output

The general purpose input/output pins (GPIOs) are grouped as one or more ports with each port having up to 32 GPIOs.

The number of ports and GPIOs per port may vary with product variant and package. Refer to Registers on page 102 and Pin assignments on page 450 for more information about the number of GPIOs that are supported.

GPIO has the following user-configurable features:

- Up to 32 GPIO pins per GPIO port
- Configurable output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on state changes on any pin
- All pins can be used by the PPI task/event system
- One or more GPIO outputs can be controlled through PPI and GPIOTE channels
- All pins can be individually mapped to interface blocks for layout flexibility
- GPIO state changes captured on SENSE signal can be stored by LATCH register
- Support for secure and non-secure attributes for pins in conjunction with the system protection unit (SPU — System protection unit on page 257)

GPIO port and the GPIO pin details on page 98 illustrates the GPIO port containing 32 individual pins, where `PIN0` is illustrated in more detail as a reference. All signals on the left side in the illustration are used by other peripherals in the system and therefore not directly available to the CPU.

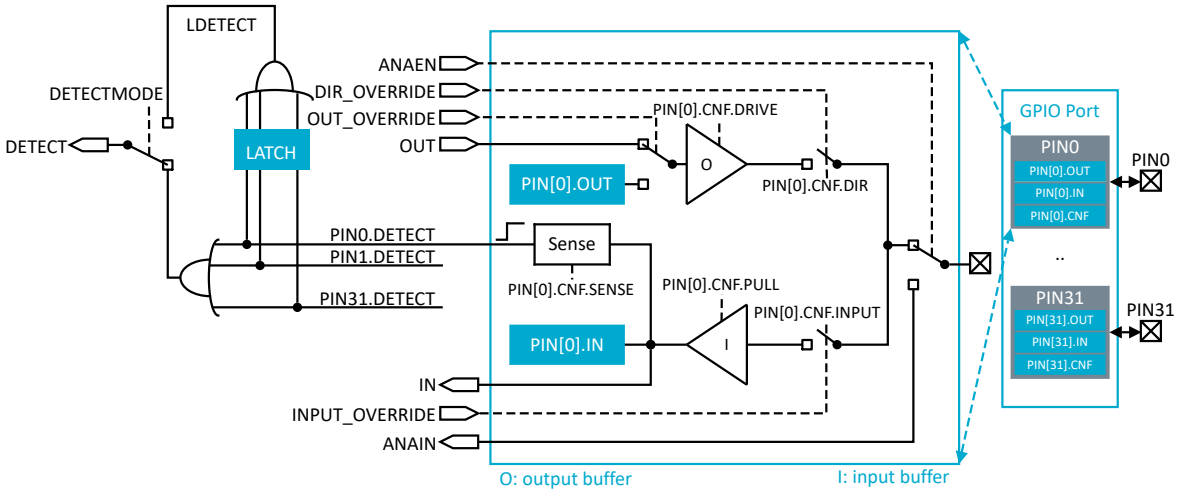

Figure 18: GPIO port and the GPIO pin details

6.4.1 Pin configuration

The GPIO port peripheral implements up to 32 pins, `PIN0` through `PIN31`. Each of these pins can be individually configured in the PIN_CNF[n] registers (n=0..31).

The following parameters can be configured through these registers:

- Direction
- Drive strength
- Enabling of pull-up and pull-down resistors
- Pin sensing
- Input buffer disconnect
- Analog input (for selected pins)

Note: All write-capable registers are retained registers, see POWER — Power control on page 63 for more information.

The input buffer of a GPIO pin can be disconnected from the pin to enable power savings when the pin is not used as an input, see GPIO port and the GPIO pin details on page 98. Inputs must be connected to get a valid input value in the IN register, and for the sense mechanism to get access to the pin.

Other peripherals in the system can connect to GPIO pins and override their output value and configuration, or read their analog or digital input value. See GPIO port and the GPIO pin details on page 98.

Selected pins also support analog input signals, see ANAIN in GPIO port and the GPIO pin details on page 98. The assignment of the analog pins can be found in Pin assignments on page 450.

The following delays should be taken into considerations:

- There is a delay of 2 CPU clock cycles from the GPIO pad to the IN register.
- The GPIO pad must be low (or high depending on the SENSE polarity) for 3 CPU clock cycles after DETECT has gone high to generate a new DETECT signal.

Note: When a pin is configured as digital input, care has been taken to minimize increased current consumption when the input voltage is between V_{IL} and V_{IH}. However, it is a good practice to ensure that the external circuitry does not drive that pin to levels between V_{IL} and V_{IH} for a long period of time.

6.4.2 Pin sense mechanism

Pins sensitivity can be individually configured, through the SENSE field in the PIN_CNF[n] register, to detect either a high level or a low level on their input.

When the correct level is detected on any such configured pin, the sense mechanism will set the DETECT signal high. Each pin has a separate DETECT signal. Default behavior, defined by the DETECTMODE register, is that the DETECT signals from all pins in the GPIO port are combined into one common DETECT signal that is routed throughout the system, which then can be utilized by other peripherals. This mechanism is functional in both System ON and System OFF modes.

DETECTMODE and DETECTMODE_SEC are provided to handle secure and non-secure pins. DETECTMODE_SEC register is available to control the behavior associated to pin marked as secure, while the DETECTMODE register is restricted to pin marked as non-secure. Please refer to GPIO security on page 100 for more details.

Make sure that a pin is in a level that cannot trigger the sense mechanism before enabling it. The DETECT signal will go high immediately if the SENSE condition configured in the PIN_CNF registers is met when the sense mechanism is enabled. This will trigger a PORT event if the DETECT signal was low before enabling the sense mechanism.

The DETECT signal is also used by power and clock management system to exit from System OFF mode, and by GPIOTE to generate the PORT event. In addition GPIOTE_SEC is used for PORT event related to secure pins). See POWER — Power control on page 63 and GPIOTE — GPIO tasks and events on page 107 for more information about how the DETECT signal is used.

When a pin's PINx.DETECT signal goes high, a flag will be set in the LATCH register. For example, when the PIN0.DETECT signal goes high, bit 0 in the LATCH register will be set to '1'. If the CPU performs a clear operation on a bit in the LATCH register when the associated PINx.DETECT signal is high, the bit in the LATCH register will not be cleared. The LATCH register will only be cleared if the CPU explicitly clears it by writing a '1' to the bit that shall be cleared, i.e. the LATCH register will not be affected by a PINx.DETECT signal being set low.

The LDETECT signal will be set high when one or more bits in the LATCH register are '1'. The LDETECT signal will be set low when all bits in the LATCH register are successfully cleared to '0'.

If one or more bits in the LATCH register are '1' after the CPU has performed a clear operation on the LATCH registers, a rising edge will be generated on the LDETECT signal. This is illustrated in DETECT signal behavior on page 100.

> **Note:** The CPU can read the LATCH register at any time to check if a SENSE condition has been met on one or more of the GPIO pins, even if that condition is no longer met at the time the CPU queries the LATCH register. This mechanism will work even if the LDETECT signal is not used as the DETECT signal.

The LDETECT signal is by default not connected to the GPIO port's DETECT signal, but via the DETECTMODE register it is possible to change from default behavior to DETECT signal being derived directly from the LDETECT signal instead. See GPIO port and the GPIO pin details on page 98. DETECT signal behavior on page 100 illustrates the DETECT signal behavior for these two alternatives.

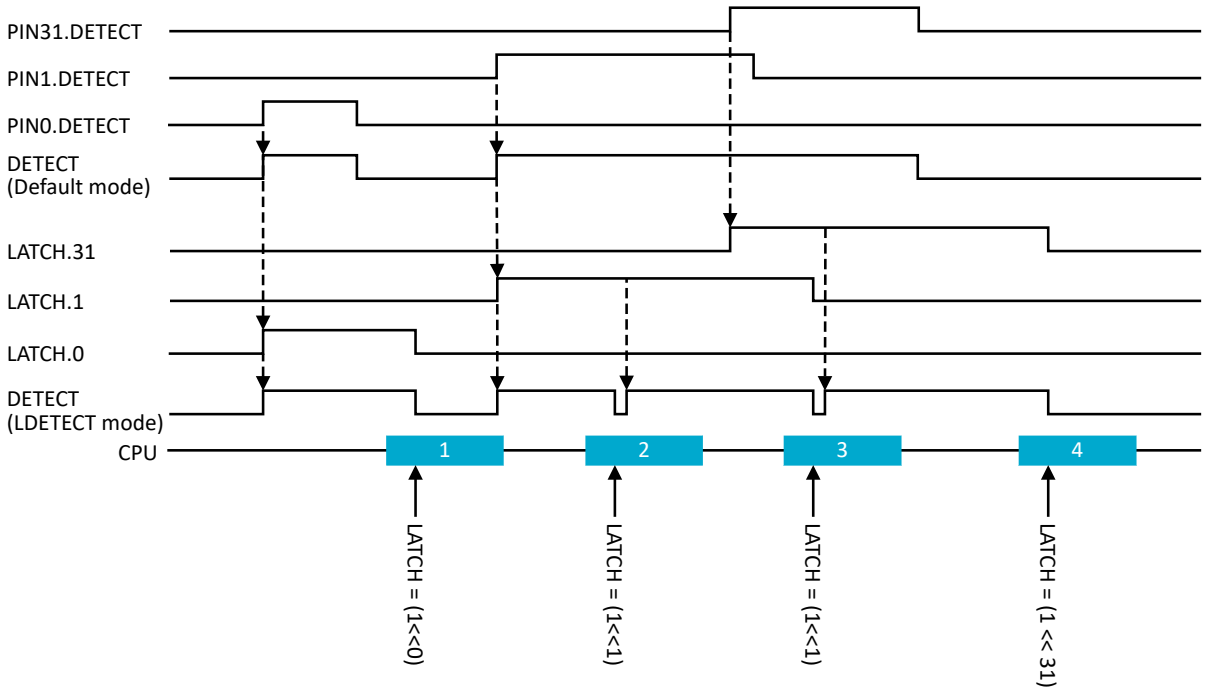

Figure 19: DETECT signal behavior

6.4.3 GPIO security

The general purpose input/output (GPIO) peripheral is implemented as a *split-security* peripheral. If marked as non-secure, it can be accessed by both secure and non-secure accesses but will behave differently depending on the access type.

A non-secure peripheral access will only be able to configure and control pins defined as non-secure in the system protection unit (SPU) GPIOPORT.PERM[] register(s).

A non-secure access to a register or a bitfield controlling a pin marked as secure in GPIO.PERM[] register(s) will be ignored. Write access will have no effect and read access will return a zero value.

No exception is triggered when a non-secure access targets a register or bitfield controlling a secure pin. For example, if the bit `i` is set in the SPU.GPIO.PERM[0] register (declaring Pin P0.`i` as secure), then

- non-secure write accesses to OUT, OUTSET, OUTCLR, DIR, DIRSET, DIRCLR and LATCH registers will not be able to write to bit `i` of those registers
- non-secure write accesses to registers PIN[`i`].OUT and PIN_CNF[`i`] will be ignored

- non-secure read accesses to registers OUT, OUTSET, OUTCLR, IN, DIR, DIRSET, DIRCLR and LATCH will always read a '0' for the bit at position `i`
- non-secure read accesses to registers PIN[`i`].OUT, PIN[`i`].OUT and PIN_CNF[`i`] will always return 0

The GPIO.DETECTMODE and GPIO.DETECTMODE_SEC registers are handled differently than the other registers mentioned before. When accessed by a secure access, the DETECTMODE_SEC register control the source for the DETECT_SEC signal for the pins marked as secure. When accessed by a non-secure access, the DETECTMODE_SEC is read as zero and write accesses are ignored. The GPIO.DETECTMODE register controls the source for the DETECT_NSEC signal for the pins defined as non-secure.

The DETECT_NSEC signal is routed to the GPIOTE peripheral, allowing generation of events and interrupts from pins marked as non-secure. The DETECT_SEC signal is routed to the GPIOTESEC peripheral, allowing generation of events and interrupts from pins marked as secure. Principle of direct pin access on page 101 illustrates how the DETECT_NSEC and DETECT_SEC signals are generated from the GPIO PIN[].DETECT signals.

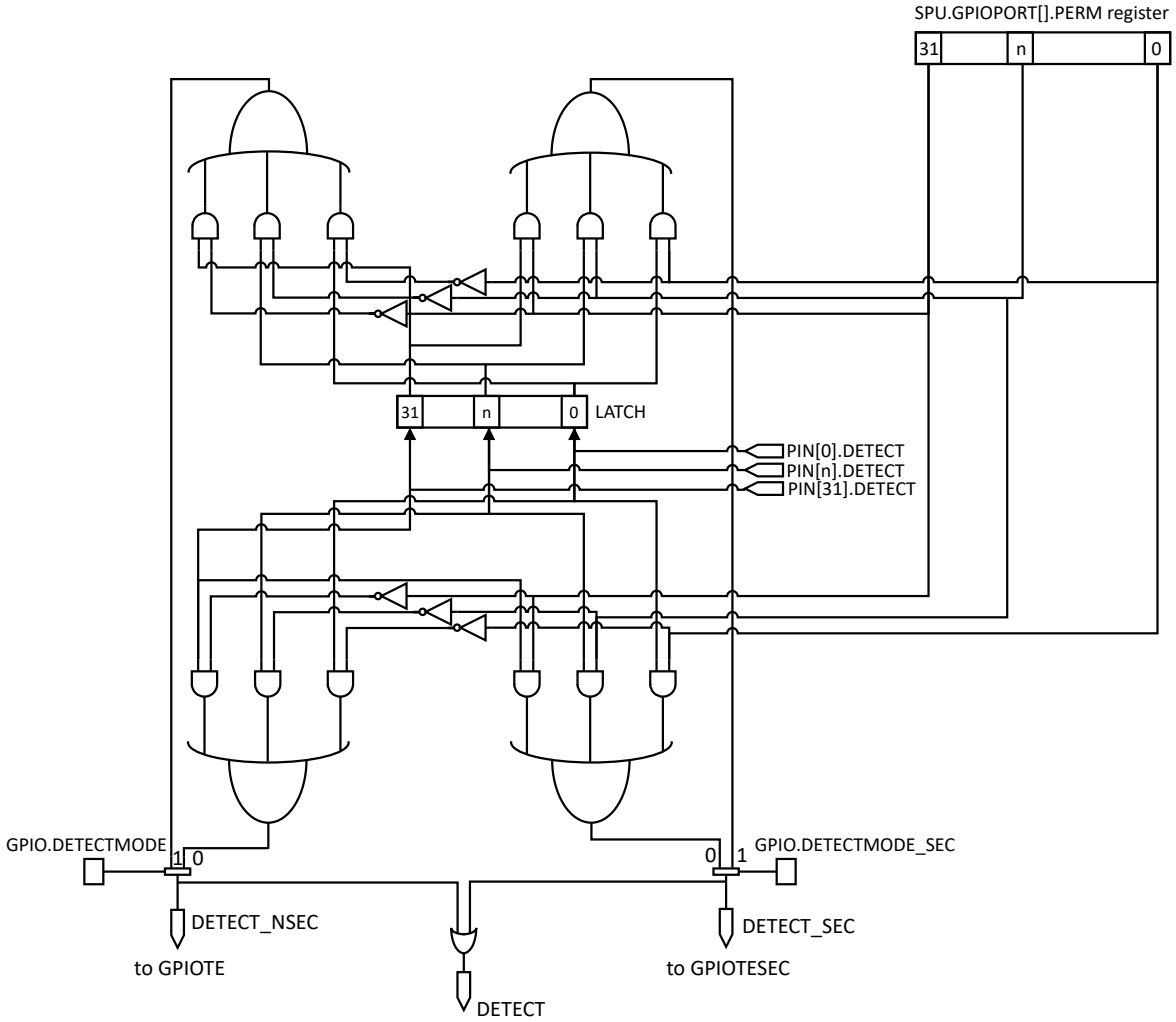

Figure 20: Principle of direct pin access

6.4.4 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
P0 : S P0 : NS	0x50842500 0x40842500	HF	NS	NA	Yes	General purpose input and output

Register overview

Register	Offset	TZ	Description
OUT	0x004		Write GPIO port This register is retained.
OUTSET	0x008		Set individual bits in GPIO port
OUTCLR	0x00C		Clear individual bits in GPIO port
IN	0x010		Read GPIO port
DIR	0x014		Direction of GPIO pins This register is retained.
DIRSET	0x018		DIR set register
DIRCLR	0x01C		DIR clear register
LATCH	0x020		Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers This register is retained.
DETECTMODE	0x024		Select between default DETECT signal behavior and LDETECT mode (For non-secure pin only) This register is retained.
DETECTMODE_SEC	0x028		Select between default DETECT signal behavior and LDETECT mode (For secure pin only) This register is retained.
PIN_CNF[n]	0x200		Configuration of GPIO pins This register is retained.

6.4.4.1 OUT (Retained)

Address offset: 0x004

Write GPIO port

This register is retained.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-f	RW	PIN[i] (i=0..31)			Pin i
			Low	0	Pin driver is low
			High	1	Pin driver is high

6.4.4.2 OUTSET

Address offset: 0x008

Set individual bits in GPIO port

Read: reads value of OUT register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-f	RW	PIN[i] (i=0..31)																																	
	W1S																																		
			Low	0																															
			High	1																															
			Set	1																															

6.4.4.3 OUTCLR

Address offset: 0x00C

Clear individual bits in GPIO port

Read: reads value of OUT register.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-f	RW	PIN[i] (i=0..31)																																	
	W1C																																		
			Low	0																															
			High	1																															
			Clear	1																															

6.4.4.4 IN

Address offset: 0x010

Read GPIO port

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-f	R	PIN[i] (i=0..31)																																	
			Low	0																															
			High	1																															

6.4.4.5 DIR (Retained)

Address offset: 0x014

Direction of GPIO pins

This register is retained.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-f	RW	PIN[i] (i=0..31)			Pin i
			Input	0	Pin set as input
			Output	1	Pin set as output

6.4.4.6 DIRSET

Address offset: 0x018

DIR set register

Read: reads value of DIR register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-f	RW	PIN[i] (i=0..31)			Set as output pin i
	W1S				
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Set	1	Write: writing a '1' sets pin to output; writing a '0' has no effect

6.4.4.7 DIRCLR

Address offset: 0x01C

DIR clear register

Read: reads value of DIR register.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-f	RW	PIN[i] (i=0..31)			Set as input pin i
	W1C				
			Input	0	Read: pin set as input
			Output	1	Read: pin set as output
			Clear	1	Write: writing a '1' sets pin to input; writing a '0' has no effect

6.4.4.8 LATCH (Retained)

Address offset: 0x020

Latch register indicating what GPIO pins that have met the criteria set in the PIN_CNF[n].SENSE registers

This register is retained.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				f	e	d	c	b	a	Z	Y	X	W	V	U	T	S	R	Q	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A-f	RW	PIN[i] (i=0..31)																																	
			NotLatched	0																															
			Latched	1																															

Status on whether PIN[i] has met criteria set in PIN_CNF[i].SENSE register.

Write '1' to clear.

Criteria has not been met

Criteria has been met

6.4.4.9 DETECTMODE (Retained)

Address offset: 0x024

Select between default DETECT signal behavior and LDETECT mode (For non-secure pin only)

This register is retained.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	DETECTMODE																																	
			Default	0																															
			LDETECT	1																															

Select between default DETECT signal behavior and LDETECT mode

DETECT directly connected to PIN DETECT signals

Use the latched LDETECT behavior

6.4.4.10 DETECTMODE_SEC (Retained)

Address offset: 0x028

Select between default DETECT signal behavior and LDETECT mode (For secure pin only)

This register is retained.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	DETECTMODE																																	
			Default	0																															
			LDETECT	1																															

Select between default DETECT signal behavior and LDETECT mode

DETECT directly connected to PIN DETECT signals

Use the latched LDETECT behavior

6.4.4.11 PIN_CNF[n] (n=0..31) (Retained)

Address offset: 0x200 + (n × 0x4)

Configuration of GPIO pins

This register is retained.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																		E	E						D	D	D					C	C	B	
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value																															
	RW	DIR																																	
			Input	0																															
			Output	1																															

Pin direction. Same physical register as DIR register

Configure pin as an input pin

Configure pin as an output pin

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																		E	E						D	D	D					C	C	B	
Reset 0x00000002				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
ID	R/W	Field	Value ID	Value																															
B	RW	INPUT																																	
			Connect	0																															
			Disconnect	1																															
C	RW	PULL																																	
			Disabled	0																															
			Pulldown	1																															
			Pullup	3																															
D-	RW	DRIVE																																	
			S0S1	0																															
			H0S1	1																															
			S0H1	2																															
			H0H1	3																															
			D0S1	4																															
			D0H1	5																															
			S0D1	6																															
			H0D1	7																															
E	RW	SENSE																																	
			Disabled	0																															
			High	2																															
			Low	3																															

6.4.5 Electrical specification

6.4.5.1 GPIO Electrical Specification

Note: VDD in the following table refers to VDD_GPIO.

Symbol	Description	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 x VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 x VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD ≥ 1.7 V	VDD-0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD ≥ 2.7 V	VDD-0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD ≥ 1.7 V	VDD-0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥ 1.7 V	VSS		VSS+0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD ≥ 2.7 V	VSS		VSS+0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD ≥ 1.7 V	VSS		VSS+0.4	V
$I_{OL,SD}$	Current at VSS + 0.4 V, output set low, standard drive, VDD ≥ 1.7 V	1	2	4	mA
$I_{OL,HDH}$	Current at VSS + 0.4 V, output set low, high drive, VDD ≥ 2.7 V	6	10	15	mA
$I_{OL,HDL}$	Current at VSS + 0.4 V, output set low, high drive, VDD ≥ 1.7 V	3			mA
$I_{OH,SD}$	Current at VDD - 0.4 V, output set high, standard drive, VDD ≥1.7	1	2	4	mA
$I_{OH,HDH}$	Current at VDD - 0.4 V, output set high, high drive, VDD ≥ 2.7 V	6	9	14	mA
$I_{OH,HDL}$	Current at VDD - 0.4 V, output set high, high drive, VDD ≥ 1.7 V	3			mA
$t_{RF,15pF}$	Rise/fall time, standard drive mode, 10 to 90%, 15 pF load[1]	6	9	19	ns
$t_{RF,25pF}$	Rise/fall time, standard drive mode, 10 to 90%, 25 pF load[1]	10	13	30	ns
$t_{RF,50pF}$	Rise/fall time, standard drive mode, 10 to 90%, 50 pF load[1]	18	25	61	ns
$t_{HRF,15pF}$	Rise/Fall time, high drive mode, 10 to 90%, 15 pF load[1]	2	4	8	ns

[1] Rise and fall times based on simulations

Symbol	Description	Min.	Typ.	Max.	Units
$t_{HRF,25pF}$	Rise/Fall time, high drive mode, 10 to 90%, 25 pF load[1]	3	5	11	ns
$t_{HRF,50pF}$	Rise/Fall time, high drive mode, 10 to 90%, 50 pF load[1]	5	8	19	ns
R_{PU}	Pull-up resistance	11	13	16	kΩ
R_{PD}	Pull-down resistance	11	13	16	kΩ
C_{PAD}	Pad capacitance		3		pF

6.5 GPIOTE — GPIO tasks and events

The GPIO tasks and events (GPIOTE) module provides functionality for accessing GPIO pins using tasks and events. Each GPIOTE channel can be assigned to one pin.

A GPIOTE block enables GPIOs to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Tasks and events are briefly introduced in Peripheral interface on page 15, and GPIO is described in more detail in GPIO — General purpose input/output on page 97.

Low power detection of pin state changes is possible when in System ON or System OFF.

Instance	Number of GPIOTE channels
GPIOTE	8

Table 16: GPIOTE properties

Up to three tasks can be used in each GPIOTE channel for performing write operations to a pin. Two tasks are fixed (SET and CLR), and one (OUT) is configurable to perform following operations:

- Set
- Clear
- Toggle

An event can be generated in each GPIOTE channel from one of the following input conditions:

- Rising edge
- Falling edge
- Any change

6.5.1 Pin events and tasks

The GPIOTE module has a number of tasks and events that can be configured to operate on individual GPIO pins.

The tasks SET[n], CLR[n], and OUT[n] can write to individual pins, and events IN[n] can be generated from input changes of individual pins.

The SET task will set the pin selected in GPIOTE.CONFIG[n].PSEL to high. The CLR task will set the pin low.

The effect of the OUT task on the pin is configurable in CONFIG[n].POLARITY. It can set the pin high, set it low, or toggle it.

Tasks and events are configured using the CONFIG[n] registers. One CONFIG[n] register is associated with a set of SET[n], CLR[n], and OUT[n] tasks and IN[n] events.

As long as a SET[n], CLR[n], and OUT[n] task or an IN[n] event is configured to control pin **n**, the pin's output value will only be updated by the GPIOTE module. The pin's output value, as specified in the GPIO, will be ignored as long as the pin is controlled by GPIOTE. Attempting to write to the pin as a normal GPIO pin will have no effect. When the GPIOTE is disconnected from a pin, the associated pin gets the output and configuration values specified in the GPIO module, see MODE field in CONFIG[n] register.

When conflicting tasks are triggered simultaneously (i.e. during the same clock cycle) in one channel, the priority of the tasks is as described in the following table.

Priority	Task
1	OUT
2	CLR
3	SET

Table 17: Task priorities

When setting the CONFIG[n] registers, MODE=Disabled does not have the same effect as MODE=Task and POLARITY=None. In the latter case, a CLR or SET task occurring at the exact same time as OUT will end up with no change on the pin, based on the priorities described in the table above.

When a GPIOTE channel is configured to operate on a pin as a task, the initial value of that pin is configured in the OUTINIT field of CONFIG[n].

6.5.2 Port event

PORT is an event that can be generated from multiple input pins using the GPIO DETECT signal.

The event will be generated on the rising edge of the DETECT signal. See GPIO — General purpose input/output on page 97 for more information about the DETECT signal.

The GPIO DETECT signal will not wake the system up again if the system is put into System ON IDLE while the DETECT signal is high. Clear all DETECT sources before entering sleep. If the LATCH register is used as a source, a new rising edge will be generated on DETECT if any bit in LATCH is still high after clearing all or part of the register. This could occur if one of the PINx.DETECT signals is still high, for example. See Pin sense mechanism on page 99 for more information.

Setting the system to System OFF while DETECT is high will cause a wakeup from System OFF reset.

This feature can be used to wake up the CPU from a WFI or WFE type sleep in System ON when all peripherals and the CPU are idle, meaning the lowest power consumption in System ON mode.

To prevent spurious interrupts from the PORT event while configuring the sources, the following steps must be performed:

1. Disable interrupts on the PORT event (through INTENCLR.PORT).
2. Configure the sources (PIN_CNF[n].SENSE).
3. Clear any potential event that could have occurred during configuration (write `0` to EVENTS_PORT).
4. Enable interrupts (through INTENSET.PORT).

6.5.3 Tasks and events pin configuration

Each GPIOTE channel is associated with one physical GPIO pin through the CONFIG.PSEL field.

When Event mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an input, overriding the DIR setting in GPIO. Similarly, when Task mode is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will be configured as an output overriding the DIR setting and OUT value in GPIO. When Disabled is selected in CONFIG.MODE, the pin specified by CONFIG.PSEL will use its configuration from the PIN[n].CNF registers in GPIO. CONFIG.MODE must be disabled in order to be able to change the value of the PSEL field.

Note: A pin can only be assigned to one GPIOTE channel at a time. Failing to do so may result in unpredictable behavior.

6.5.4 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
GPIOTE0	0x5000D000	HF	S	NA	No	Secure GPIO tasks and events
GPIOTE1	0x40031000	HF	NS	NA	No	Non Secure GPIO tasks and events

Register overview

Register	Offset	TZ	Description
TASKS_OUT[n]	0x000		Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY.
TASKS_SET[n]	0x030		Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.
TASKS_CLR[n]	0x060		Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.
SUBSCRIBE_OUT[n]	0x080		Subscribe configuration for task OUT[n]
SUBSCRIBE_SET[n]	0x0B0		Subscribe configuration for task SET[n]
SUBSCRIBE_CLR[n]	0x0E0		Subscribe configuration for task CLR[n]
EVENTS_IN[n]	0x100		Event generated from pin specified in CONFIG[n].PSEL
EVENTS_PORT	0x17C		Event generated from multiple input GPIO pins with SENSE mechanism enabled
PUBLISH_IN[n]	0x180		Publish configuration for event IN[n]
PUBLISH_PORT	0x1FC		Publish configuration for event PORT
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
CONFIG[n]	0x510		Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event

6.5.4.1 TASKS_OUT[n] (n=0..7)

Address offset: 0x000 + (n × 0x4)

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_OUT			Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is configured in CONFIG[n].POLARITY.
			Trigger	1	Trigger task

6.5.4.2 TASKS_SET[n] (n=0..7)

Address offset: 0x030 + (n × 0x4)

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	TASKS_SET																																	
			Trigger	1																															

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it high.

Trigger task

6.5.4.3 TASKS_CLR[n] (n=0..7)

Address offset: 0x060 + (n × 0x4)

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	TASKS_CLR																																	
			Trigger	1																															

Task for writing to pin specified in CONFIG[n].PSEL. Action on pin is to set it low.

Trigger task

6.5.4.4 SUBSCRIBE_OUT[n] (n=0..7)

Address offset: 0x080 + (n × 0x4)

Subscribe configuration for task OUT[n]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

DPPI channel that task OUT[n] will subscribe to

Disable subscription

Enable subscription

6.5.4.5 SUBSCRIBE_SET[n] (n=0..7)

Address offset: 0x0B0 + (n × 0x4)

Subscribe configuration for task SET[n]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

DPPI channel that task SET[n] will subscribe to

Disable subscription

Enable subscription

6.5.4.6 SUBSCRIBE_CLR[n] (n=0..7)

Address offset: 0x0E0 + (n × 0x4)

Subscribe configuration for task CLR[n]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task CLR[n] will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

6.5.4.7 EVENTS_IN[n] (n=0..7)

Address offset: 0x100 + (n × 0x4)

Event generated from pin specified in CONFIG[n].PSEL

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_IN			Event generated from pin specified in CONFIG[n].PSEL
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.5.4.8 EVENTS_PORT

Address offset: 0x17C

Event generated from multiple input GPIO pins with SENSE mechanism enabled

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_PORT			Event generated from multiple input GPIO pins with SENSE mechanism enabled
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.5.4.9 PUBLISH_IN[n] (n=0..7)

Address offset: 0x180 + (n × 0x4)

Publish configuration for event IN[n]

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B A A A A A A A
Reset 0x00000000				**0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0**
ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event IN[n] will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

6.5.4.10 PUBLISH_PORT

Address offset: 0x1FC

Publish configuration for event PORT

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	CHIDX		[0..255]																								DPPI channel that event PORT will publish to							
B	RW	EN																																	
			Disabled	0																								Disable publishing							
			Enabled	1																								Enable publishing							

6.5.4.11 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				I																								H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A-H	RW	IN[i] (i=0..7)																										Write '1' to enable interrupt for event IN[i]							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
I	RW	PORT																										Write '1' to enable interrupt for event PORT							
			Set	1																								Enable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

6.5.4.12 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				I																								H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A-H	RW	IN[i] (i=0..7)																										Write '1' to disable interrupt for event IN[i]							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							
I	RW	PORT																										Write '1' to disable interrupt for event PORT							
			Clear	1																								Disable							
			Disabled	0																								Read: Disabled							
			Enabled	1																								Read: Enabled							

6.5.4.13 CONFIG[n] (n=0..7)

Address offset: 0x510 + (n × 0x4)

Configuration for OUT[n], SET[n], and CLR[n] tasks and IN[n] event

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID												D			C	C				B	B	B	B	B							A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MODE			Mode
			Disabled	0	Disabled. Pin specified by PSEL will not be acquired by the GPIOTE module.
			Event	1	Event mode The pin specified by PSEL will be configured as an input and the IN[n] event will be generated if operation specified in POLARITY occurs on the pin.
			Task	3	Task mode The GPIO specified by PSEL will be configured as an output and triggering the SET[n], CLR[n] or OUT[n] task will perform the operation specified by POLARITY on the pin. When enabled as a task the GPIOTE module will acquire the pin and the pin can no longer be written as a regular output pin from the GPIO module.
B	RW	PSEL		[0..31]	GPIO number associated with SET[n], CLR[n], and OUT[n] tasks and IN[n] event
C	RW	POLARITY			When In task mode: Operation to be performed on output when OUT[n] task is triggered. When In event mode: Operation on input that shall trigger IN[n] event.
			None	0	Task mode: No effect on pin from OUT[n] task. Event mode: no IN[n] event generated on pin activity.
			LoToHi	1	Task mode: Set pin from OUT[n] task. Event mode: Generate IN[n] event when rising edge on pin.
			HiToLo	2	Task mode: Clear pin from OUT[n] task. Event mode: Generate IN[n] event when falling edge on pin.
			Toggle	3	Task mode: Toggle pin from OUT[n]. Event mode: Generate IN[n] when any change on pin.
D	RW	OUTINIT			When in task mode: Initial value of the output when the GPIOTE channel is configured. When in event mode: No effect.
			Low	0	Task mode: Initial value of pin before task triggering is low
			High	1	Task mode: Initial value of pin before task triggering is high

6.6 IPC — Interprocessor communication

The interprocessor communication (IPC) peripheral is used to send and receive events between MCUs in the system.

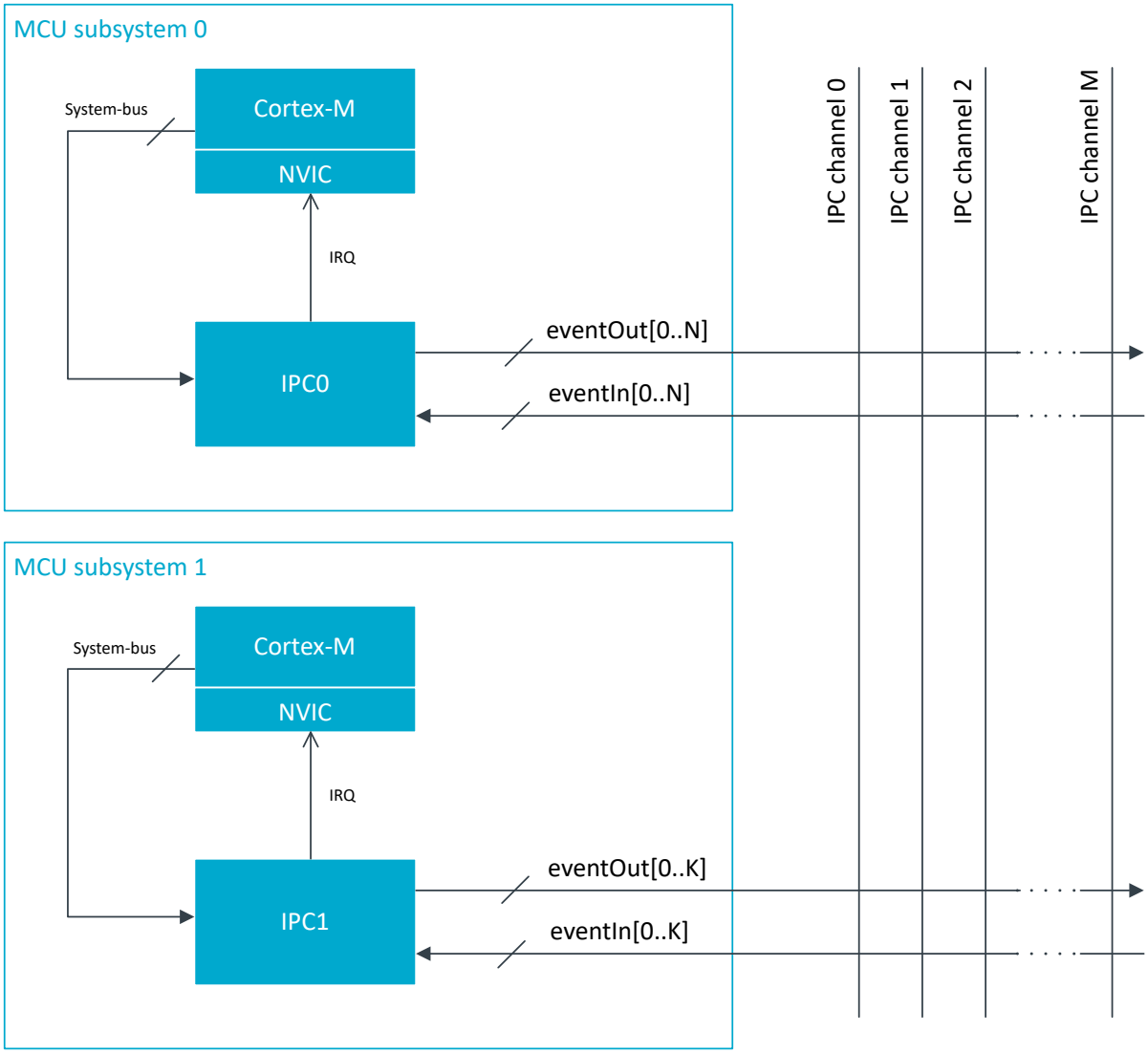

Figure 21: IPC block diagram

Functional description

IPC block diagram on page 114 illustrates the interprocessor communication (IPC) peripheral. In a multi-MCU system, each MCU has one dedicated IPC peripheral. The IPC peripheral can be used to send and receive events to and from other IPC peripherals. An instance of the IPC peripheral can have multiple SEND tasks and RECEIVE events. A single SEND task can be configured to signal an event on one or more IPC channels, and a RECEIVE event can be configured to listen on one or more IPC channels. The IPC channels that are triggered in a SEND task can be configured through the SEND_CNF registers, and the IPC channels that trigger a RECEIVE event are configured through the RECEIVE_CNF registers. The figure below illustrates how the SEND_CNF and RECEIVE_CNF registers work. Both the SEND task and the RECEIVE event can be connected to all IPC channels.

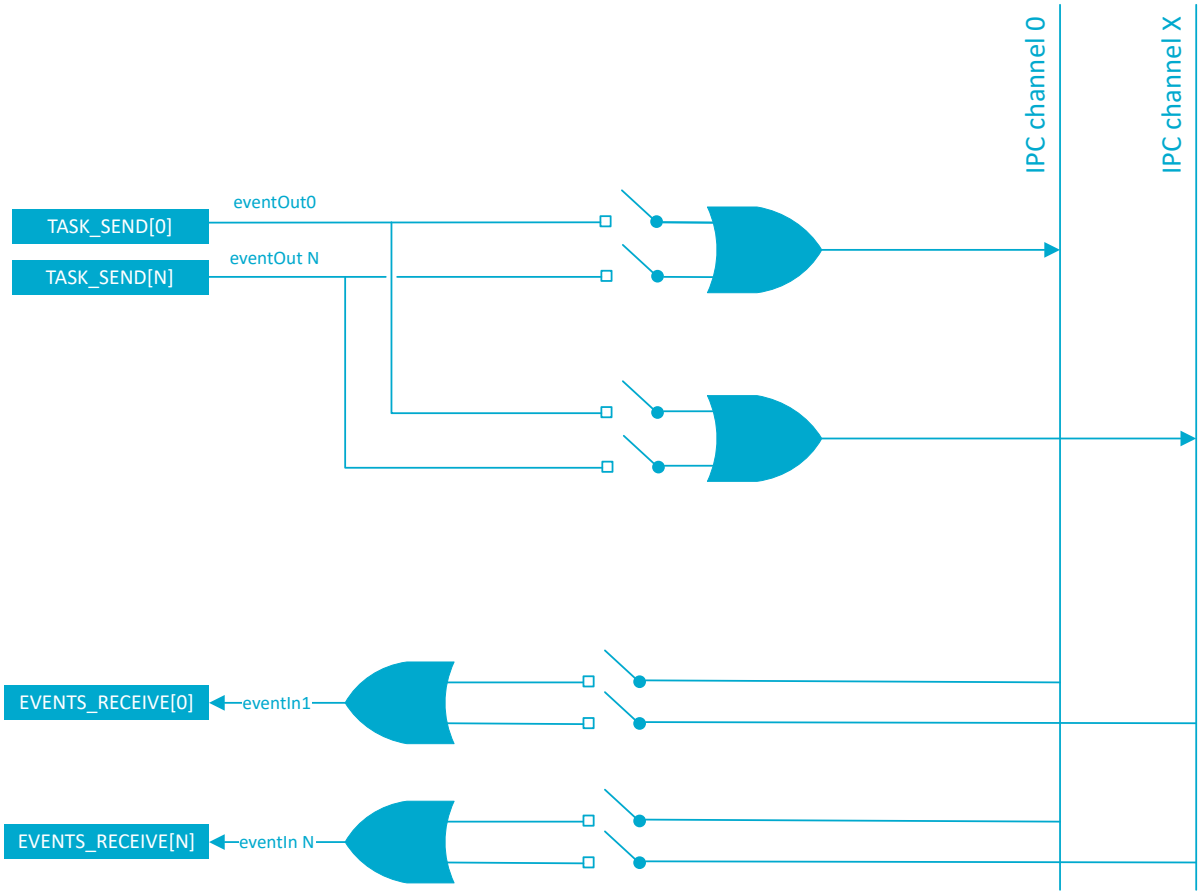

Figure 22: IPC registers SEND_CNF and RECEIVE_CNF

A SEND task can be viewed as broadcasting events onto one or more IPC channels, and a RECEIVE event can be seen as subscribing to a subset of IPC channels. It is possible for multiple IPCs to trigger events onto the same channel at the same time. When two or more events on the same channel occur within t_{IPC}, the events may be merged into a single event seen from the IPC receiver. One of the events can therefore be lost. To prevent this, the user must ensure that events on the same IPC channel do not occur within t_{IPC} of each other. When implementing firmware data structures, such as queues or mailboxes, this can be done by using one channel for acknowledgements.

An IPC event often does not contain any data itself, it is used to signal other MCUs that something has occurred. Data can be shared through shared memory, for example in the form of a software implemented mailbox, or command/event queues. It is up to software to assign a logical functionality to an IPC channel. For instance, one IPC channel can be used to signal that a command is ready to be executed, and any processor in the system can subscribe to that particular channel and decode/execute the command.

General purpose memory

The GPMEM registers can be used freely to store information. These registers are accessed like any other of the IPC peripheral's registers.

6.6.1 IPC and PPI connections

The IPC SEND tasks and RECEIVE events can be connected through PPI channels. This makes it possible to relay events from peripherals in one MCU to another, without CPU involvement.

Figure below illustrates a timer COMPARE event that is relayed from one MCU to IPC using PPI, then back into a timer CAPTURE event in another MCU.

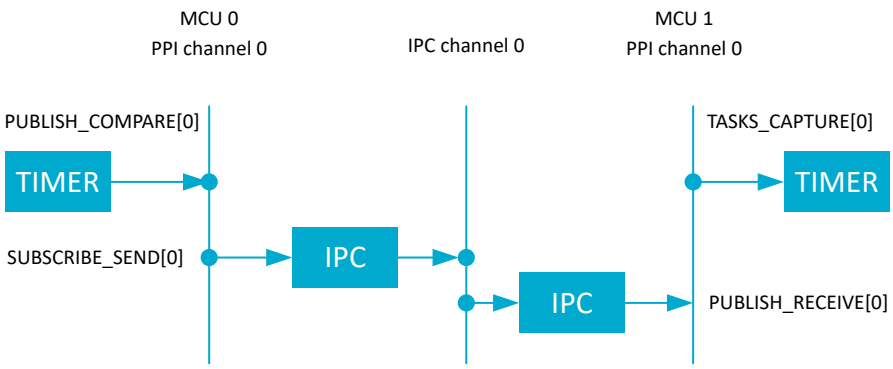

Figure 23: Example of PPI and IPC connections

6.6.2 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
IPC : S IPC : NS	0x5002A000 0x4002A000	US	NS	NA	No	Interprocessor communication

Register overview

Register	Offset	TZ	Description
TASKS_SEND[n]	0x000		Trigger events on IPC channel enabled in SEND_CNF[n]
SUBSCRIBE_SEND[n]	0x080		Subscribe configuration for task SEND[n]
EVENTS_RECEIVE[n]	0x100		Event received on one or more of the enabled IPC channels in RECEIVE_CNF[n]
PUBLISH_RECEIVE[n]	0x180		Publish configuration for event RECEIVE[n]
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
INTPEND	0x30C		Pending interrupts
SEND_CNF[n]	0x510		Send event configuration for TASKS_SEND[n]
RECEIVE_CNF[n]	0x590		Receive event configuration for EVENTS_RECEIVE[n]
GPMEM[n]	0x610		General purpose memory

6.6.2.1 TASKS_SEND[n] (n=0..7)

Address offset: 0x000 + (n × 0x4)

Trigger events on IPC channel enabled in SEND_CNF[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_SEND			Trigger events on IPC channel enabled in SEND_CNF[n]
			Trigger	1	Trigger task

6.6.2.2 SUBSCRIBE_SEND[n] (n=0..7)

Address offset: 0x080 + (n × 0x4)

Subscribe configuration for task SEND[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																								A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task SEND[n] will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

6.6.2.3 EVENTS_RECEIVE[n] (n=0..7)

Address offset: 0x100 + (n × 0x4)

Event received on one or more of the enabled IPC channels in RECEIVE_CNF[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_RECEIVE			Event received on one or more of the enabled IPC channels in RECEIVE_CNF[n]
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.6.2.4 PUBLISH_RECEIVE[n] (n=0..7)

Address offset: 0x180 + (n × 0x4)

Publish configuration for event RECEIVE[n]

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																								A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event RECEIVE[n] will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

6.6.2.5 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-H	RW	RECEIVE[i] (i=0..7)			Enable or disable interrupt for event RECEIVE[i]
			Disabled	0	Disable
			Enabled	1	Enable

6.6.2.6 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-H	RW	RECEIVE[i] (i=0..7)			Write '1' to enable interrupt for event RECEIVE[i]
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.6.2.7 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-H	RW	RECEIVE[i] (i=0..7)			Write '1' to disable interrupt for event RECEIVE[i]
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.6.2.8 INTPEND

Address offset: 0x30C

Pending interrupts

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									H	G	F	E	D	C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A-H	R	RECEIVE[i] (i=0..7)			Read pending status of interrupt for event RECEIVE[i]
			NotPending	0	Read: Not pending
			Pending	1	Read: Pending

6.6.2.9 SEND_CNF[n] (n=0..7)

Address offset: 0x510 + (n × 0x4)

Send event configuration for TASKS_SEND[n]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A-H	RW	CHEN[i] (i=0..7)																										Enable broadcasting on IPC channel i							
			Disable	0																								Disable broadcast							
			Enable	1																								Enable broadcast							

6.6.2.10 RECEIVE_CNF[n] (n=0..7)

Address offset: 0x590 + (n × 0x4)

Receive event configuration for EVENTS_RECEIVE[n]

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																												H	G	F	E	D	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A-H	RW	CHEN[i] (i=0..7)																										Enable subscription to IPC channel i							
			Disable	0																								Disable events							
			Enable	1																								Enable events							

6.6.2.11 GPMEM[n] (n=0..3)

Address offset: 0x610 + (n × 0x4)

General purpose memory

Retained only in System ON mode

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	GPMEM																										General purpose memory							

6.6.3 Electrical specification

6.6.3.1 IPC Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
t_{IPC}	Time window during which IPC events can be merged			165	µs

6.7 I2S — Inter-IC sound interface

The I2S (Inter-IC Sound) module, supports the original two-channel I2S format, and left or right-aligned formats. It implements EasyDMA for sample transfer directly to and from RAM without CPU intervention.

The I2S peripheral has the following main features:

- Master and Slave mode

- Simultaneous bi-directional (TX and RX) audio streaming
- Original I2S and left- or right-aligned format
- 8, 16 and 24-bit sample width
- Low-jitter Master Clock generator
- Various sample rates

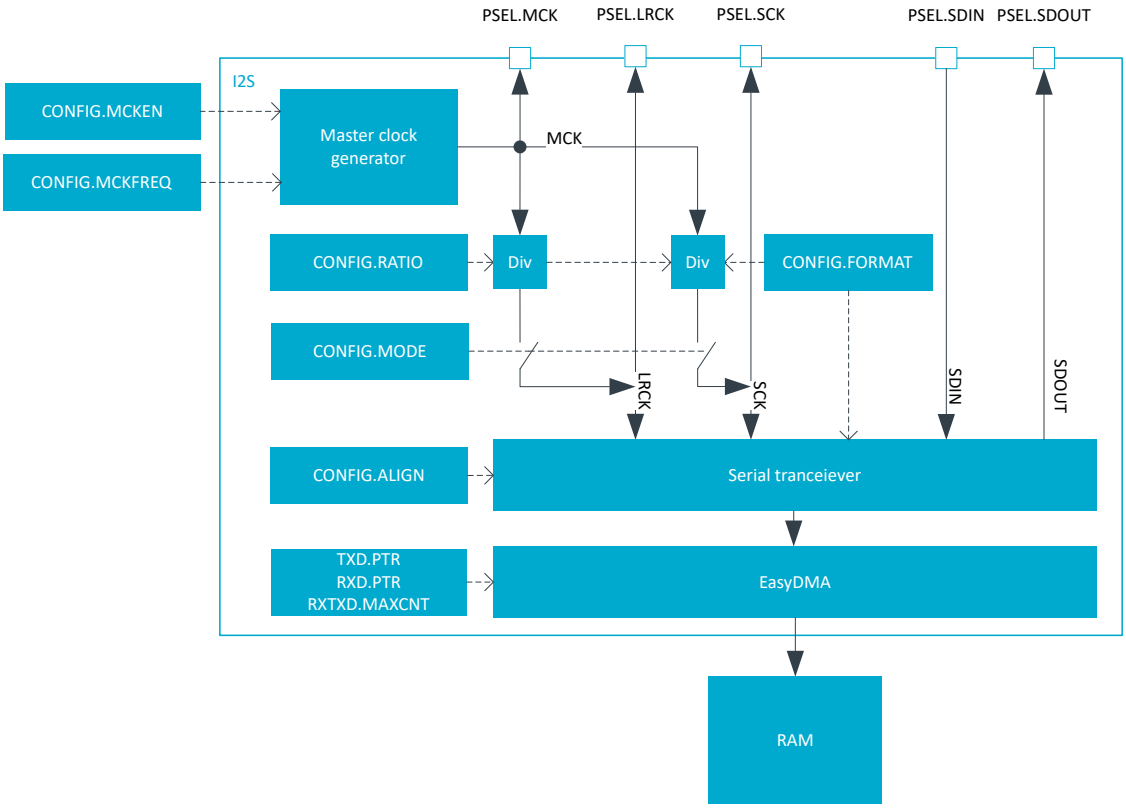

Figure 24: I2S master

6.7.1 Mode

The I2S protocol specification defines two modes of operation, Master and Slave.

The I2S mode decides which of the two sides (Master or Slave) shall provide the clock signals LRCK and SCK, and these signals are always supplied by the Master to the Slave.

6.7.2 Transmitting and receiving

The I2S module supports both transmission (TX) and reception (RX) of serial data. In both cases the serial data is shifted synchronously to the clock signals SCK and LRCK.

TX data is written to the SDOUT pin on the falling edge of SCK, and RX data is read from the SDIN pin on the rising edge of SCK. The most significant bit (MSB) is always transmitted first.

> **Note:** When starting a transmission in master mode, two frames (two left-and-right sample pairs) of value zero will be transmitted after triggering the START task, prior to the RXTXD.MAXCNT samples specified by the TXD.PTR pointer.

TX and RX are available in both Master and Slave modes and can be enabled/disabled independently in the CONFIG.TXEN on page 134 and CONFIG.RXEN on page 134.

Transmission and/or reception is started by triggering the START task. When started and transmission is enabled (in CONFIG.TXEN on page 134), the TXPTRUPD event will be generated for every

RXTXD.MAXCNT on page 137 number of transmitted data words (containing one or more samples). Similarly, when started and reception is enabled (in CONFIG.RXEN on page 134), the RXPTRUPD event will be generated for every RXTXD.MAXCNT on page 137 received data words.

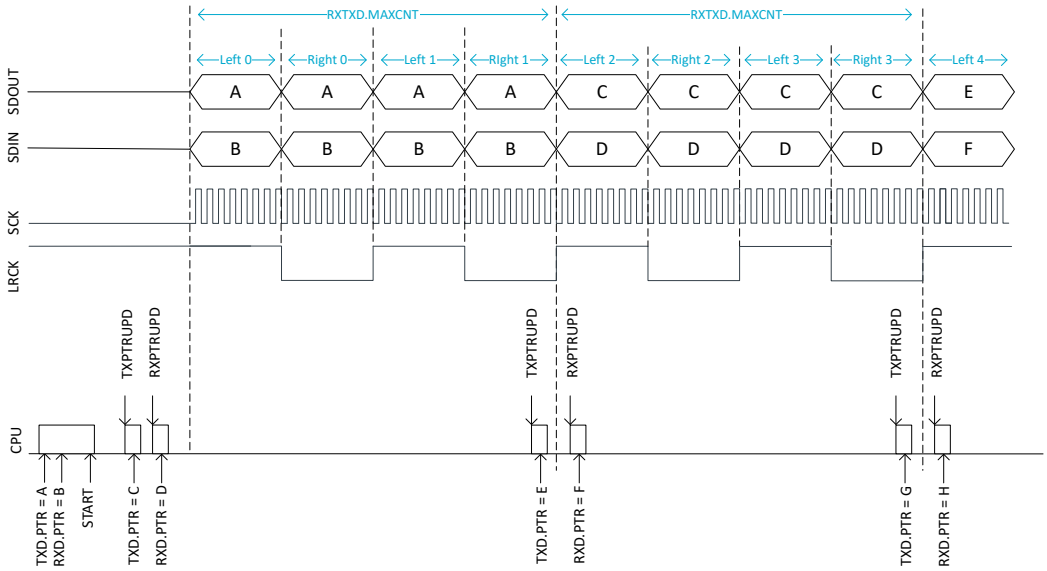

Figure 25: Transmitting and receiving. CONFIG.FORMAT = Aligned, CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo, RXTXD.MAXCNT = 1.

6.7.3 Left right clock (LRCK)

The Left Right Clock (LRCK), often referred to as "word clock", "sample clock" or "word select" in I2S context, is the clock defining the frames in the serial bit streams sent and received on SDOUT and SDIN, respectively.

In I2S mode, each frame contains one left and right sample pair, with the left sample being transferred during the low half period of LRCK followed by the right sample being transferred during the high period of LRCK.

In Aligned mode, each frame contains one left and right sample pair, with the left sample being transferred during the high half period of LRCK followed by the right sample being transferred during the low period of LRCK.

Consequently, the LRCK frequency is equivalent to the audio sample rate.

When operating in Master mode, the LRCK is generated from the MCK, and the frequency of LRCK is then given as:

```
LRCK = MCK / CONFIG.RATIO
```

LRCK always toggles around the falling edge of the serial clock SCK.

6.7.4 Serial clock (SCK)

The serial clock (SCK), often referred to as the serial bit clock, pulses once for each data bit being transferred on the serial data lines SDIN and SDOUT.

When operating in Master mode the SCK is generated from the MCK, and the frequency of SCK is then given as:

```
SCK = 2 * LRCK * CONFIG.SWIDTH
```

The falling edge of the SCK falls on the toggling edge of LRCK.

When operating in Slave mode SCK is provided by the external I2S master.

6.7.5 Master clock (MCK)

The master clock (MCK) is the clock from which LRCK and SCK are derived when operating in Master mode.

The MCK is generated by an internal MCK generator. This generator always needs to be enabled when in Master mode, but the generator can also be enabled when in Slave mode. Enabling the generator when in slave mode can be useful in the case where the external Master is not able to generate its own master clock.

The MCK generator is enabled/disabled in the register CONFIG.MCKEN on page 134, and the generator is started or stopped by the START or STOP tasks.

In Master mode the LRCK and the SCK frequencies are closely related, as both are derived from MCK and set indirectly through CONFIG.RATIO on page 135 and CONFIG.SWIDTH on page 136.

When configuring these registers, the user is responsible for fulfilling the following requirements:

1. SCK frequency can never exceed the MCK frequency, which can be formulated as:

```
CONFIG.RATIO >= 2 * CONFIG.SWIDTH
```

2. The MCK/LRCK ratio shall be a multiple of 2 * CONFIG.SWIDTH, which can be formulated as:

```
Integer = (CONFIG.RATIO / (2 * CONFIG.SWIDTH))
```

The MCK signal can be routed to an output pin (specified in PSEL.MCK) to supply external I2S devices that require the MCK to be supplied from the outside.

When operating in Slave mode, the I2S module does not use the MCK and the MCK generator does not need to be enabled.

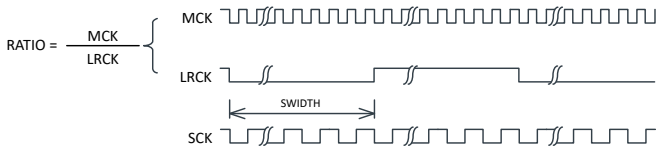

Figure 26: Relation between RATIO, MCK and LRCK.

Desired LRCK [Hz]	CONFIG.SWID	CONFIG.RATIO	CONFIG.MCKF	MCK [Hz]	LRCK [Hz]	LRCK error [%]
16000	16Bit	32X	32MDIV63	507936.5	15873.0	-0.8
16000	16Bit	64X	32MDIV31	1032258.1	16129.0	0.8
16000	16Bit	256X	32MDIV8	4000000.0	15625.0	-2.3
32000	16Bit	32X	32MDIV31	1032258.1	32258.1	0.8
32000	16Bit	64X	32MDIV16	2000000.0	31250.0	-2.3
44100	16Bit	32X	32MDIV23	1391304.3	43478.3	-1.4
44100	16Bit	64X	32MDIV11	2909090.9	45454.5	3.1

Table 18: Configuration examples

6.7.6 Width, alignment, and format

The CONFIG.SWIDTH register primarily defines the sample width of the data written to memory. In master mode, it then also sets the amount of bits per frame. In Slave mode it controls padding/trimming if required. Left, right, transmitted, and received samples always have the same width. The CONFIG.FORMAT register specifies the position of the data frames with respect to the LRCK edges in both Master and Slave modes.

When using I2S format, the first bit in a half-frame (containing one left or right sample) gets sampled on the second rising edge of the SCK after a LRCK edge. When using Aligned mode, the first bit in a half-frame gets sampled on the first rising edge of SCK following a LRCK edge.

For data being received on SDIN the sample value can be either right or left-aligned inside a half-frame, as specified in CONFIG.ALIGN on page 136. CONFIG.ALIGN on page 136 affects only the decoding of the incoming samples (SDIN), while the outgoing samples (SDOUT) are always left-aligned (or justified).

When using left-alignment, each half-frame starts with the MSB of the sample value (both for data being sent on SDOUT and received on SDIN).

When using right-alignment, each half-frame of data being received on SDIN ends with the LSB of the sample value, while each half-frame of data being sent on SDOUT starts with the MSB of the sample value (same as for left-alignment).

In Master mode, the size of a half-frame (in number of SCK periods) equals the sample width (in number of bits), and in this case the alignment setting does not care as each half-frame in any case will start with the MSB and end with the LSB of the sample value.

In slave mode, however, the sample width does not need to equal the frame size. This means you might have extra or fewer SCK pulses per half-frame than what the sample width specified in CONFIG.SWIDTH requires.

In the case where we use **left-alignment** and the number of SCK pulses per half-frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits after the LSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0.

In the case where we use **left-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data sent and received on SDOUT and SDIN will be truncated with the LSBs being removed first.

In the case where we use **right-alignment** and the number of SCK pulses per frame is **higher** than the sample width, the following will apply:

- For data received on SDIN, all bits before the MSB of the sample value will be discarded.
- For data sent on SDOUT, all bits after the LSB of the sample value will be 0 (same behavior as for left-alignment).

In the case where we use **right-alignment** and the number of SCK pulses per frame is **lower** than the sample width, the following will apply:

- Data received on SDIN will be sign-extended to "sample width" number of bits before being written to memory.
- Data sent on SDOUT will be truncated with the LSBs being removed first (same behavior as for left-alignment).

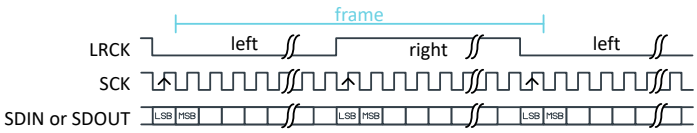

Figure 27: I2S format. CONFIG.SWIDTH equaling half-frame size.

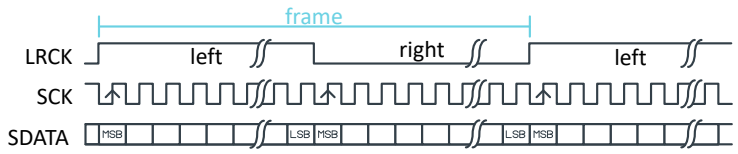

Figure 28: Aligned format. CONFIG.SWIDTH equaling half-frame size.

6.7.7 EasyDMA

The I2S module implements EasyDMA for accessing internal Data RAM without CPU intervention.

The source and destination pointers for the TX and RX data are configured in TXD.PTR on page 137 and RXD.PTR on page 137. The memory pointed to by these pointers will only be read or written when TX or RX are enabled in CONFIG.TXEN on page 134 and CONFIG.RXEN on page 134.

The addresses written to the pointer registers TXD.PTR on page 137 and RXD.PTR on page 137 are double-buffered in hardware, and these double buffers are updated for every RXTXD.MAXCNT on page 137 words (containing one or more samples) read/written from/to memory. The events TXPTRUPD and RXPTRUPD are generated whenever the TXD.PTR and RXD.PTR are transferred to these double buffers.

If TXD.PTR on page 137 is not pointing to the Data RAM region when transmission is enabled, or RXD.PTR on page 137 is not pointing to the Data RAM region when reception is enabled, an EasyDMA transfer may result in a HardFault and/or memory corruption. See Memory on page 21 for more information about the different memory regions.

Due to the nature of I2S, where the number of transmitted samples always equals the number of received samples (at least when both TX and RX are enabled), one common register RXTXD.MAXCNT on page 137 is used for specifying the sizes of these two memory buffers. The size of the buffers is specified in a number of 32-bit words. Such a 32-bit memory word can either contain four 8-bit samples, two 16-bit samples or one right-aligned 24-bit sample sign extended to 32 bit.

In stereo mode (CONFIG.CHANNELS=Stereo), the samples are stored as "left and right sample pairs" in memory. Figure Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo. on page 124, Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo. on page 125 and Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo. on page 125 show how the samples are mapped to memory in this mode. The mapping is valid for both RX and TX.

In mono mode (CONFIG.CHANNELS=Left or Right), RX sample from only one channel in the frame is stored in memory, the other channel sample is ignored. Illustrations Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left. on page 125, Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left. on page 125 and Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left. on page 126 show how RX samples are mapped to memory in this mode.

For TX, the same outgoing sample read from memory is transmitted on both left and right in a frame, resulting in a mono output stream.

	31 24	23 16	15 8	7 0
x.PTR	Right sample 1	Left sample 1	Right sample 0	Left sample 0
x.PTR + 4	Right sample 3	Left sample 3	Right sample 2	Left sample 2
x.PTR + (n*2) - 4	Right sample n-1	Left sample n-1	Right sample n-2	Left sample n-2

Figure 29: Memory mapping for 8 bit stereo. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Stereo.

	31 24	23 16	15 8	7 0
x.PTR	Left sample 3	Left sample 2	Left sample 1	Left sample 0
x.PTR + 4	Left sample 7	Left sample 6	Left sample 5	Left sample 4
x.PTR + n - 4	Left sample n-1	Left sample n-2	Left sample n-3	Left sample n-4

Figure 30: Memory mapping for 8 bit mono. CONFIG.SWIDTH = 8Bit, CONFIG.CHANNELS = Left.

	31 16	15 0
x.PTR	Right sample 0	Left sample 0
x.PTR + 4	Right sample 1	Left sample 1
x.PTR + (n*4) - 4	Right sample n - 1	Left sample n - 1

Figure 31: Memory mapping for 16 bit stereo. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Stereo.

	31 16	15 0
x.PTR	Left sample 1	Left sample 0
x.PTR + 4	Left sample 3	Left sample 2
x.PTR + (n*2) - 4	Left sample n - 1	Left sample n - 2

Figure 32: Memory mapping for 16 bit mono, left channel only. CONFIG.SWIDTH = 16Bit, CONFIG.CHANNELS = Left.

	31 23	23 0
x.PTR	Sign ext.	Left sample 0
x.PTR + 4	Sign ext.	Right sample 0
x.PTR + (n*8) - 8	Sign ext.	Left sample n - 1
x.PTR + (n*8) - 4	Sign ext.	Right sample n - 1

Figure 33: Memory mapping for 24 bit stereo. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Stereo.

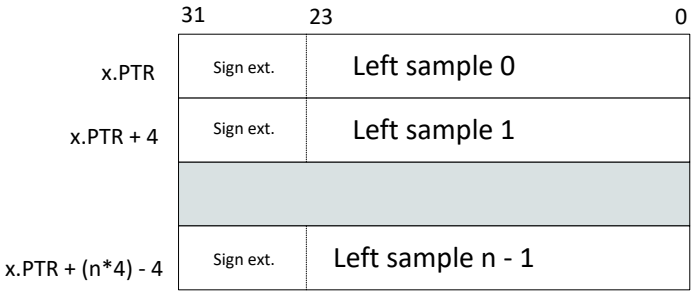

Figure 34: Memory mapping for 24 bit mono, left channel only. CONFIG.SWIDTH = 24Bit, CONFIG.CHANNELS = Left.

6.7.8 Module operation

Described here is a typical operating procedure for the I2S module.

1. Configure the I2S module using the CONFIG registers

```
// Enable reception
NRF_I2S->CONFIG.RXEN = (I2S_CONFIG_RXEN_RXEN_Enabled <<
                                        I2S_CONFIG_RXEN_RXEN_Pos);
// Enable transmission
NRF_I2S->CONFIG.TXEN = (I2S_CONFIG_TXEN_TXEN_Enabled <<
                                        I2S_CONFIG_TXEN_TXEN_Pos);
// Enable MCK generator
NRF_I2S->CONFIG.MCKEN = (I2S_CONFIG_MCKEN_MCKEN_Enabled <<
                                        I2S_CONFIG_MCKEN_MCKEN_Pos);
// MCKFREQ = 4 MHz
NRF_I2S->CONFIG.MCKFREQ = I2S_CONFIG_MCKFREQ_MCKFREQ_32MDIV8 <<
                                        I2S_CONFIG_MCKFREQ_MCKFREQ_Pos;
// Ratio = 256
NRF_I2S->CONFIG.RATIO = I2S_CONFIG_RATIO_RATIO_256X <<
                                        I2S_CONFIG_RATIO_RATIO_Pos;
// MCKFREQ = 4 MHz and Ratio = 256 gives sample rate = 15.625 ks/s
// Sample width = 16 bit
NRF_I2S->CONFIG.SWIDTH = I2S_CONFIG_SWIDTH_SWIDTH_16Bit <<
                                        I2S_CONFIG_SWIDTH_SWIDTH_Pos;
// Alignment = Left
NRF_I2S->CONFIG.ALIGN = I2S_CONFIG_ALIGN_ALIGN_Left <<
                                        I2S_CONFIG_ALIGN_ALIGN_Pos;
// Format = I2S
NRF_I2S->CONFIG.FORMAT = I2S_CONFIG_FORMAT_FORMAT_I2S <<
                                        I2S_CONFIG_FORMAT_FORMAT_Pos;
// Use stereo
NRF_I2S->CONFIG.CHANNELS = I2S_CONFIG_CHANNELS_CHANNELS_Stereo <<
                                        I2S_CONFIG_CHANNELS_CHANNELS_Pos;
```

2. Map IO pins using the PINSEL registers

```
// MCK routed to pin 0
NRF_I2S->PSEL.MCK = (0 << I2S_PSEL_MCK_PIN_Pos) |
                    (I2S_PSEL_MCK_CONNECT_Connected <<
                                                I2S_PSEL_MCK_CONNECT_Pos);
// SCK routed to pin 1
NRF_I2S->PSEL.SCK = (1 << I2S_PSEL_SCK_PIN_Pos) |
                    (I2S_PSEL_SCK_CONNECT_Connected <<
                                                I2S_PSEL_SCK_CONNECT_Pos);
// LRCK routed to pin 2
NRF_I2S->PSEL.LRCK = (2 << I2S_PSEL_LRCK_PIN_Pos) |
                     (I2S_PSEL_LRCK_CONNECT_Connected <<
                                                I2S_PSEL_LRCK_CONNECT_Pos);
// SDOUT routed to pin 3
NRF_I2S->PSEL.SDOUT = (3 << I2S_PSEL_SDOUT_PIN_Pos) |
                      (I2S_PSEL_SDOUT_CONNECT_Connected <<
                                                I2S_PSEL_SDOUT_CONNECT_Pos);
// SDIN routed on pin 4
NRF_I2S->PSEL.SDIN = (4 << I2S_PSEL_SDIN_PIN_Pos) |
                     (I2S_PSEL_SDIN_CONNECT_Connected <<
                                                I2S_PSEL_SDIN_CONNECT_Pos);
```

3. Configure TX and RX data pointers using the TXD, RXD and RXTXD registers

```
NRF_I2S->TXD.PTR = my_tx_buf;
NRF_I2S->RXD.PTR = my_rx_buf;
NRF_I2S->TXD.MAXCNT = MY_BUF_SIZE;
```

4. Enable the I2S module using the ENABLE register

```
NRF_I2S->ENABLE = 1;
```

5. Start audio streaming using the START task

```
NRF_I2S->TASKS_START = 1;
```

6. Handle received and transmitted data when receiving the TXPTRUPD and RXPTRUPD events

```
if(NRF_I2S->EVENTS_TXPTRUPD  != 0)
{
    NRF_I2S->TXD.PTR = my_next_tx_buf;
    NRF_I2S->EVENTS_TXPTRUPD = 0;
}

if(NRF_I2S->EVENTS_RXPTRUPD != 0)
{
    NRF_I2S->RXD.PTR = my_next_rx_buf;
    NRF_I2S->EVENTS_RXPTRUPD = 0;
}
```

6.7.9 Pin configuration

The MCK, SCK, LRCK, SDIN and SDOUT signals associated with the I2S module are mapped to physical pins according to the pin numbers specified in the PSEL.x registers.

These pins are acquired whenever the I2S module is enabled through the register ENABLE on page 133.

When a pin is acquired by the I2S module, the direction of the pin (input or output) will be configured automatically, and any pin direction setting done in the GPIO module will be overridden. The directions for the various I2S pins are shown below in GPIO configuration before enabling peripheral (master mode) on page 128 and GPIO configuration before enabling peripheral (slave mode) on page 128.

To secure correct signal levels on the pins when the system is in OFF mode, and when the I2S module is disabled, these pins must be configured in the GPIO peripheral directly.

I2S signal	I2S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Output	0	
SCK	As specified in PSEL.SCK	Output	0	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

Table 19: GPIO configuration before enabling peripheral (master mode)

I2S signal	I2S pin	Direction	Output value	Comment
MCK	As specified in PSEL.MCK	Output	0	
LRCK	As specified in PSEL.LRCK	Input	Not applicable	
SCK	As specified in PSEL.SCK	Input	Not applicable	
SDIN	As specified in PSEL.SDIN	Input	Not applicable	
SDOUT	As specified in PSEL.SDOUT	Output	0	

Table 20: GPIO configuration before enabling peripheral (slave mode)

6.7.10 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
I2S : S I2S : NS	0x50028000 0x40028000	US	NS	SA	No	Inter-IC Sound

Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Starts continuous I2S transfer. Also starts MCK generator when this is enabled.
TASKS_STOP	0x004		Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the STOPPED event to be generated.
SUBSCRIBE_START	0x080		Subscribe configuration for task START
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP
EVENTS_RXPTRUPD	0x104		The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on the SDIN pin.

Register	Offset	TZ	Description
EVENTS_STOPPED	0x108		I2S transfer stopped.
EVENTS_TXPTRUPD	0x114		The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the SDOUT pin.
PUBLISH_RXPTRUPD	0x184		Publish configuration for event RXPTRUPD
PUBLISH_STOPPED	0x188		Publish configuration for event STOPPED
PUBLISH_TXPTRUPD	0x194		Publish configuration for event TXPTRUPD
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
ENABLE	0x500		Enable I2S module.
CONFIG.MODE	0x504		I2S mode.
CONFIG.RXEN	0x508		Reception (RX) enable.
CONFIG.TXEN	0x50C		Transmission (TX) enable.
CONFIG.MCKEN	0x510		Master clock generator enable.
CONFIG.MCKFREQ	0x514		Master clock generator frequency.
CONFIG.RATIO	0x518		MCK / LRCK ratio.
CONFIG.SWIDTH	0x51C		Sample width.
CONFIG.ALIGN	0x520		Alignment of sample within a frame.
CONFIG.FORMAT	0x524		Frame format.
CONFIG.CHANNELS	0x528		Enable channels.
RXD.PTR	0x538		Receive buffer RAM start address.
TXD.PTR	0x540		Transmit buffer RAM start address.
RXTXD.MAXCNT	0x550		Size of RXD and TXD buffers.
PSEL.MCK	0x560		Pin select for MCK signal.
PSEL.SCK	0x564		Pin select for SCK signal.
PSEL.LRCK	0x568		Pin select for LRCK signal.
PSEL.SDIN	0x56C		Pin select for SDIN signal.
PSEL.SDOUT	0x570		Pin select for SDOUT signal.

6.7.10.1 TASKS_START

Address offset: 0x000

Starts continuous I2S transfer. Also starts MCK generator when this is enabled.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_START			Starts continuous I2S transfer. Also starts MCK generator when this is enabled.
			Trigger	1	Trigger task

6.7.10.2 TASKS_STOP

Address offset: 0x004

Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the STOPPED event to be generated.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	W	TASKS_STOP																																	
			Trigger	1																															

Stops I2S transfer. Also stops MCK generator. Triggering this task will cause the STOPPED event to be generated.

Trigger task

6.7.10.3 SUBSCRIBE_START

Address offset: 0x080

Subscribe configuration for task START

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

DPPI channel that task START will subscribe to

6.7.10.4 SUBSCRIBE_STOP

Address offset: 0x084

Subscribe configuration for task STOP

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

DPPI channel that task STOP will subscribe to

6.7.10.5 EVENTS_RXPTRUPD

Address offset: 0x104

The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on the SDIN pin.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_RXPTRUPD																																	
			NotGenerated	0																															
			Generated	1																															

The RXD.PTR register has been copied to internal double-buffers. When the I2S module is started and RX is enabled, this event will be generated for every RXTXD.MAXCNT words that are received on the SDIN pin.

Event not generated

Event generated

6.7.10.6 EVENTS_STOPPED

Address offset: 0x108

I2S transfer stopped.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_STOPPED																																	
			NotGenerated	0																															
			Generated	1																															

6.7.10.7 EVENTS_TXPTRUPD

Address offset: 0x114

The TDX.PTR register has been copied to internal double-buffers. When the I2S module is started and TX is enabled, this event will be generated for every RXTXD.MAXCNT words that are sent on the SDOUT pin.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_TXPTRUPD																																	
			NotGenerated	0																															
			Generated	1																															

6.7.10.8 PUBLISH_RXPTRUPD

Address offset: 0x184

Publish configuration for event RXPTRUPD

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

6.7.10.9 PUBLISH_STOPPED

Address offset: 0x188

Publish configuration for event STOPPED

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

6.7.10.10 PUBLISH_TXPTRUPD

Address offset: 0x194

Publish configuration for event TXPTRUPD

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

6.7.10.11 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														F			C	B	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
B	RW	RXPTRUPD																																	
			Disabled	0																															
			Enabled	1																															
C	RW	STOPPED																																	
			Disabled	0																															
			Enabled	1																															
F	RW	TXPTRUPD																																	
			Disabled	0																															
			Enabled	1																															

6.7.10.12 INTENSET

Address offset: 0x304

Enable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														F			C	B	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
B	RW	RXPTRUPD																																	

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														F			C	B	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
			Set	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	STOPPED																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	TXPTRUPD																																	
			Set	1																															
			Disabled	0																															
			Enabled	1																															

6.7.10.13 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														F			C	B	
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
B	RW	RXPTRUPD																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	STOPPED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
F	RW	TXPTRUPD																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

6.7.10.14 ENABLE

Address offset: 0x500

Enable I2S module.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	ENABLE																																	
			Disabled	0																															
			Enabled	1																															

6.7.10.15 CONFIG.MODE

Address offset: 0x504

I2S mode.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MODE			I2S mode.
			Master	0	Master mode. SCK and LRCK generated from internal master clcok (MCK) and output on pins defined by PSEL.xxx.
			Slave	1	Slave mode. SCK and LRCK generated by external master and received on pins defined by PSEL.xxx

6.7.10.16 CONFIG.RXEN

Address offset: 0x508

Reception (RX) enable.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	RXEN			Reception (RX) enable.
			Disabled	0	Reception disabled and now data will be written to the RXD.PTR address.
			Enabled	1	Reception enabled.

6.7.10.17 CONFIG.TXEN

Address offset: 0x50C

Transmission (TX) enable.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000001	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

ID	R/W	Field	Value ID	Value	Description
A	RW	TXEN			Transmission (TX) enable.
			Disabled	0	Transmission disabled and now data will be read from the RXD.TXD address.
			Enabled	1	Transmission enabled.

6.7.10.18 CONFIG.MCKEN

Address offset: 0x510

Master clock generator enable.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000001				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	MCKEN																																	
			Disabled	0																															
			Enabled	1																															

ID	R/W	Field	Value ID	Value	Description
A	RW	MCKEN			Master clock generator enable.
			Disabled	0	Master clock generator disabled and PSEL.MCK not connected(available as GPIO).
			Enabled	1	Master clock generator running and MCK output on PSEL.MCK.

6.7.10.19 CONFIG.MCKFREQ

Address offset: 0x514

Master clock generator frequency.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x20000000				**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	MCKFREQ																																	
			32MDIV8	0x20000000																															
			32MDIV10	0x18000000																															
			32MDIV11	0x16000000																															
			32MDIV15	0x11000000																															
			32MDIV16	0x10000000																															
			32MDIV21	0x0C000000																															
			32MDIV23	0x0B000000																															
			32MDIV30	0x08800000																															
			32MDIV31	0x08400000																															
			32MDIV32	0x08000000																															
			32MDIV42	0x06000000																															
			32MDIV63	0x04100000																															
			32MDIV125	0x020C0000																															

ID	R/W	Field	Value ID	Value	Description
A	RW	MCKFREQ			Master clock generator frequency.
			32MDIV8	0x20000000	32 MHz / 8 = 4.0 MHz
			32MDIV10	0x18000000	32 MHz / 10 = 3.2 MHz
			32MDIV11	0x16000000	32 MHz / 11 = 2.9090909 MHz
			32MDIV15	0x11000000	32 MHz / 15 = 2.1333333 MHz
			32MDIV16	0x10000000	32 MHz / 16 = 2.0 MHz
			32MDIV21	0x0C000000	32 MHz / 21 = 1.5238095
			32MDIV23	0x0B000000	32 MHz / 23 = 1.3913043 MHz
			32MDIV30	0x08800000	32 MHz / 30 = 1.0666667 MHz
			32MDIV31	0x08400000	32 MHz / 31 = 1.0322581 MHz
			32MDIV32	0x08000000	32 MHz / 32 = 1.0 MHz
			32MDIV42	0x06000000	32 MHz / 42 = 0.7619048 MHz
			32MDIV63	0x04100000	32 MHz / 63 = 0.5079365 MHz
			32MDIV125	0x020C0000	32 MHz / 125 = 0.256 MHz

6.7.10.20 CONFIG.RATIO

Address offset: 0x518

MCK / LRCK ratio.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A	A	A	A
Reset 0x00000006				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	RATIO																																	
			32X	0																															
			48X	1																															
			64X	2																															
			96X	3																															
			128X	4																															
			192X	5																															
			256X	6																															
			384X	7																															
			512X	8																															

ID	R/W	Field	Value ID	Value	Description
A	RW	RATIO			MCK / LRCK ratio.
			32X	0	LRCK = MCK / 32
			48X	1	LRCK = MCK / 48
			64X	2	LRCK = MCK / 64
			96X	3	LRCK = MCK / 96
			128X	4	LRCK = MCK / 128
			192X	5	LRCK = MCK / 192
			256X	6	LRCK = MCK / 256
			384X	7	LRCK = MCK / 384
			512X	8	LRCK = MCK / 512

6.7.10.21 CONFIG.SWIDTH

Address offset: 0x51C

Sample width.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															A	A
Reset 0x00000001	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

ID	R/W	Field	Value ID	Value	Description
A	RW	SWIDTH			Sample width.
			8Bit	0	8 bit.
			16Bit	1	16 bit.
			24Bit	2	24 bit.

6.7.10.22 CONFIG.ALIGN

Address offset: 0x520

Alignment of sample within a frame.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ALIGN			Alignment of sample within a frame.
			Left	0	Left-aligned.
			Right	1	Right-aligned.

6.7.10.23 CONFIG.FORMAT

Address offset: 0x524

Frame format.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	FORMAT			Frame format.
			I2S	0	Original I2S format.
			Aligned	1	Alternate (left- or right-aligned) format.

6.7.10.24 CONFIG.CHANNELS

Address offset: 0x528

Enable channels.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																															A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHANNELS			Enable channels.
			Stereo	0	Stereo.
			Left	1	Left only.
			Right	2	Right only.

6.7.10.25 RXD.PTR

Address offset: 0x538

Receive buffer RAM start address.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PTR			Receive buffer Data RAM start address. When receiving, words containing samples will be written to this address. This address is a word aligned Data RAM address.

6.7.10.26 TXD.PTR

Address offset: 0x540

Transmit buffer RAM start address.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	PTR			Transmit buffer Data RAM start address. When transmitting, words containing samples will be fetched from this address. This address is a word aligned Data RAM address.

6.7.10.27 RXTXD.MAXCNT

Address offset: 0x550

Size of RXD and TXD buffers.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																			A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	MAXCNT			Size of RXD and TXD buffers in number of 32 bit words.

6.7.10.28 PSEL.MCK

Address offset: 0x560

Pin select for MCK signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.7.10.29 PSEL.SCK

Address offset: 0x564

Pin select for SCK signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.7.10.30 PSEL.LRCK

Address offset: 0x568

Pin select for LRCK signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.7.10.31 PSEL.SDIN

Address offset: 0x56C

Pin select for SDIN signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.7.10.32 PSEL.SDOUT

Address offset: 0x570

Pin select for SDOUT signal.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.7.11 Electrical specification

6.7.11.1 I2S timing specification

Symbol	Description	Min.	Typ.	Max.	Units
t_{S_SDIN}	SDIN setup time before SCK rising	20			ns
t_{H_SDIN}	SDIN hold time after SCK rising	15			ns
t_{S_SDOUT}	SCK falling edge to SDOUT valid	40			ns
t_{H_SDOUT}	SDOUT hold time after SCK falling	6			ns
t_{SCK_LRCK}	SCLK falling to LRCK edge	-5	0	5	ns
f_{MCK}	MCK frequency			4000	kHz
f_{LRCK}	LRCK frequency			48	kHz
f_{SCK}	SCK frequency			2000	kHz
DC_{CK}	Clock duty cycle (MCK, LRCK, SCK)	45		55	%

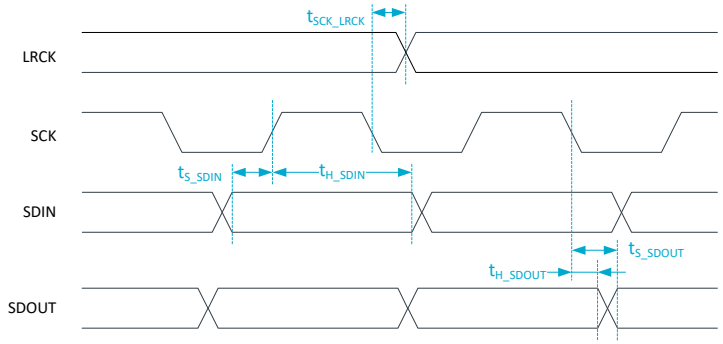

Figure 35: I2S timing diagram

6.8 KMU — Key management unit

The key management unit (KMU) enforces access policies to a subset region of user information configuration register (UICR). This subset region is used for storing cryptographic key values inside the key slots, which the CPU has no access to.

In total there are 128 key slots available, where each key slot can store one 128-bit key value together with an access policy and a destination address for the key value. Multiple key slots can be combined in order to support key sizes larger than 128 bits. The access policy of a key slot governs if and how a key value can

be used, while the destination address determines where in the memory map the KMU pushes the key value upon a request from the CPU.

Key slots can be configured to be pushed directly into write-only key registers in cryptographic accelerators, like e.g. CryptoCell, without exposing the key value itself to the CPU. This enables the CPU to use the key values stored inside the key slots for cryptographic operations without being exposed to the key value.

Access to the KMU, and the key slots in the UICR, is only allowed from secure mode.

6.8.1 Functional view

From a functional view the UICR is divided into two different regions, one-time programmable (OTP) memory and key storage.

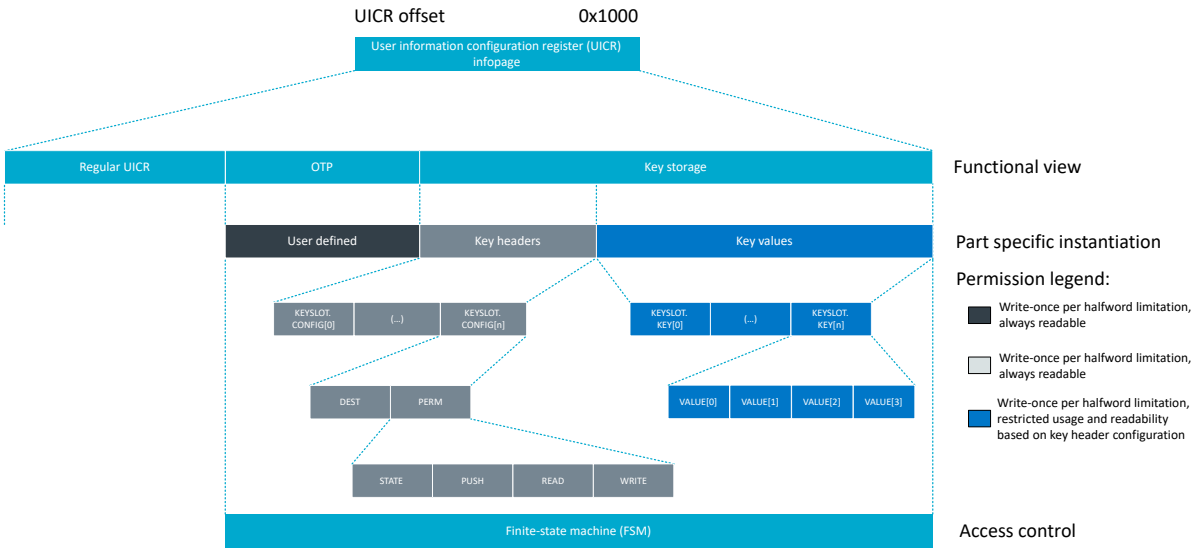

Figure 36: Memory map overview

OTP

One-time programmable (OTP) memory is typically used for holding values that are written once, and then never to be changed again throughout the product lifetime. The OTP region of UICR is emulated by placing a write-once per halfword limitation on registers defined here.

Key storage

The key storage region contains multiple key slots, where each slot consists of a key header and an associated key value. The key value is limited to 128 bits. Any key size greater than 128 bits must be divided and distributed over multiple key slot instances.

Key headers are allocated an address range of 0x400 in the UICR memory map, allowing a total of 128 keys to be addressable inside the key storage region.

> **Note:** The use of the key storage region in UICR should be limited to keys with a certain life span, and not per-session derived keys where the CPU is involved in the key exchange.

6.8.2 Access control

Access control to the underlying UICR infopage in flash is enforced by a hardware finite-state machine (FSM). The FSM can allow or block transactions, depending both on the security of the transaction (secure or non-secure) and on the type of register being written and/or read.

Access type	Key headers	Key values
Read	Allowed	Restricted
Write	Restricted	Restricted

Table 21: Access control

Any restricted access requires an explicit key slot selection through the KMU register interface. Any illegal access to restricted key slot registers will be blocked and word `0xDEADDEAD` will be returned on the AHB.

The OTP region has individual access control behavior, while access control to the key storage region is configured on a per key slot basis. The KMU FSM operates on only one key slot instance at a time, and the permissions and the usage restriction for a key value associated with a key slot can be configured individually.

Note: Even if the KMU can be configured as non-secure, all non-secure transactions will be blocked.

6.8.3 Protecting the UICR content

The UICR content can be protected against device-internal NVMC.ERASEALL requests, in addition to device-external ERASEALL requests, through the CTRL-AP interface. This feature is useful if the firmware designers want to prevent the OTP region from being erased.

Since enabling this step will permanently disable erase for the UICR, the procedure requires an implementation defined 32-bit word to be written into the UICR's ERASEPROTECT register.

In case of a field return handling, it is still possible to erase the UICR even if the ERASEPROTECT is set. If this functionality is desired, the secure boot code must implement a secure communication channel over the CTRL-AP mailbox interface. Upon successful authentication of the external party, the secure boot code can temporarily re-enable the CTRL-AP ERASEALL functionality.

6.8.4 Usage

This section describes the specific KMU and UICR behavior in more detail, to help the reader get a better overview of KMU's features and the intended usage.

6.8.4.1 OTP

The OTP region of the UICR contains a user-defined static configuration of the device. The KMU emulates the OTP functionality by placing a write-once per halfword limitation of registers defined in this region, i.e. only halfwords containing all '1's can be written.

An OTP write transaction must consist of a full 32-bit word. Both halfwords can either be written simultaneously or one at a time. The KMU FSM will block any write to a halfword in the OTP region, if the initial value of this halfword is not 0xFFFF. When writing halfwords one at a time, the non-active halfword must be masked as 0xFFFF, otherwise the request will be blocked. For example, writing 0x1234XXXX to an OTP destination address which already contains the value 0xFFFFAABB, must be configured as 0x1234FFFF. The OTP destination address will contain the value 0x1234AABB after both write transactions have been processed.

The KMU will also only allow secure AHB write transactions into the OTP region of the UICR. Any AHB write transaction to this region that does not satisfy the above requirements will be ignored, and the STATUS.BLOCKED register will be set to '1'.

6.8.4.2 Key storage

The key storage region of the UICR can contain multiple keys of different type, including symmetrical keys, hashes, public/private key pairs and other device secrets. One of the key features of the KMU, is that these

device secrets can be installed and made available for use in cryptographic operations without revealing the actual secret values.

Keys in this region will typically have a certain life span. The region is not designed to be used for per-session derived keys where the non-secure side (i.e. application) is participating in the key exchange.

All key storage is done through the concept of multiple key slots, where each key slot instance consists of one key header and an associated key value. Each key header supports the configuration of usage permissions and an optional secure destination address.

The key header secure destination address option enables the KMU to push the associated key value over a dedicated secure APB to a pre-configured secure location within the memory map. Such locations typically include a write-only key register of the hardware cryptographic accelerator, allowing the KMU to distribute keys within the system without compromising the key values.

One key slot instance can store a key value of maximum 128 bits. If a key size exceeds this limit, the key value itself must be split over multiple key slot instances.

The following usage and read permissions scheme is applicable for each key slot:

State	Push	Read	Write	Description
Active (1)	Enabled (1)	Enabled (1)	Enabled (1)	Default flash erase value. Key slot cannot be pushed, write is enabled.
Active (1)	Enabled (1)	Enabled (1)	Disabled (0)	Key slot is active, push is enabled. Key slot VALUE registers can be read, but write is disabled.
Active (1)	Enabled (1)	Disabled (0)	Disabled (0)	Key slot is active, push is enabled. Read and write to key slot VALUE registers are disabled.
Active (1)	Disabled (0)	Enabled (1)	Disabled (0)	Key slot is active, push is disabled. Key slot VALUE registers can be read, but write is disabled.
Revoked (0)	-	-	-	Key slot is revoked. Cannot be read or pushed over secure APB regardless of the permission settings.

Table 22: Valid key slot permission schemes

6.8.4.2.1 Selecting a key slot

The KMU FSM is designed to process only one key slot at a time, effectively operating as a memory protection unit for the key storage region. Whenever a key slot is selected, the KMU will allow access to writing, reading, and/or pushing the associated key value according to the selected slot configuration.

A key slot must be selected prior to use, by writing the key slot ID into the KMU SELECTKEYSLOT register. Because the reset value of this register is 0x00000000, there is no key slot associated with ID=0 and no slot is selected by default. All key slots are addressed using IDs from 1 to 128.

SELECTED status is set when a key slot is selected, and a read or write access to that keyslot occurs.

BLOCKED status is set when any illegal access to key slot registers is detected.

When the use of the particular key slot is stopped, the key slot selection in SELECTKEYSLOT must be set back to '0'.

By default, all KMU key slots will consist of a 128-bit key value of '1's, where the key headers have no secure destination address, or any usage and read restrictions.

6.8.4.2.2 Writing to a key slot

Writing a key slot into UICR is a five-step process.

1. Select which key slot the KMU shall operate on by writing the desired key slot ID into KMU->SELECTKEYSLOT. The selected key slot must be empty in order to add a new entry to UICR.
2. If the key value shall be pushable over secure APB, the destination address of the recipient must be configured in register KEYSLOT.CONFIG[ID-1].DEST.

3. Write the 128-bit key value into KEYSLOT.KEY[ID-1].VALUE[0-3].
4. Write the desired key slot permissions into KEYSLOT.CONFIG[ID-1].PERM, including any applicable usage restrictions.
5. Select key slot 0.

In case the total key size is greater than 128 bits, the key value itself must be split into 128-bit segments and written to multiple key slot instances. Steps 1 through 5 above must be repeated for the entire key size.

Note: If a key slot is configured as readable, and KEYSLOT.CONFIG[ID-1].DEST is not to be used, it is recommended to disable the push bit in KEYSLOT.CONFIG[ID-1].PERM when configuring key slot permissions.

Note: A key value distributed over multiple key slots should use the same key slot configuration in its key headers, but the secure destination address for each key slot instance must be incremented by 4 words (128 bits) for each key slot instance spanned.

Note: Write to flash must be enabled in NVMC->CONFIG prior to writing keys to flash, and subsequently disabled once writing is complete.

Steps 1 through 5 above will be blocked if any of the following violations are detected:

- No key slot selected
- Non-empty key slot selected
- NVM destination address not empty
- AHB write to KEYSLOT.KEY[ID-1].VALUE[0-3] registers not belonging to selected key slot

6.8.4.2.3 Reading a key value

Key slots that are configured as readable can have their key value read directly from the UICR memory map by the CPU.

Readable keys are typically used during the secure boot sequence, where the CPU is involved in falsifying or verifying the integrity of the system. Since the CPU is involved in this decision process, it makes little sense not to trust the CPU having access to the actual key value but ultimately trust the decision of the integrity check. Another use-case for readable keys is if the key type in question does not have a HW peripheral in the platform that is able to accept such keys over secure APB.

Reading a key value from the UICR is a three-step process:

1. Select the key slot which the KMU shall operate on by writing the desired key slot ID into KMU->SELECTKEYSLOT.
2. If STATE and READ permission requirements are fulfilled as defined in KEYSLOT.CONFIG[ID-1].PERM, the key value can be read from region KEYSLOT.KEY[ID-1].VALUE[0-3] for selected key slot.
3. Select key slot 0.

Step 2 will be blocked and word 0xDEADDEAD will be returned on AHB if any of the following violations are detected:

- No key slot selected
- Key slot not configured as readable
- Key slot is revoked
- AHB read to KEYSLOT.KEY[ID-1].VALUE[0-3] registers not belonging to selected key slot

6.8.4.2.4 Push over secure APB

Key slots that are configured as non-readable cannot be read by the CPU regardless of the mode the system is in and must be pushed over secure APB in order to use the key value for cryptographic operations.

The secure APB destination address is set in the key slot configuration DEST register. Such destination addresses are typically write-only key registers in a hardware cryptographic accelerators memory map. The secure APB allows key slots to be utilized by the software side, without exposing the key value itself.

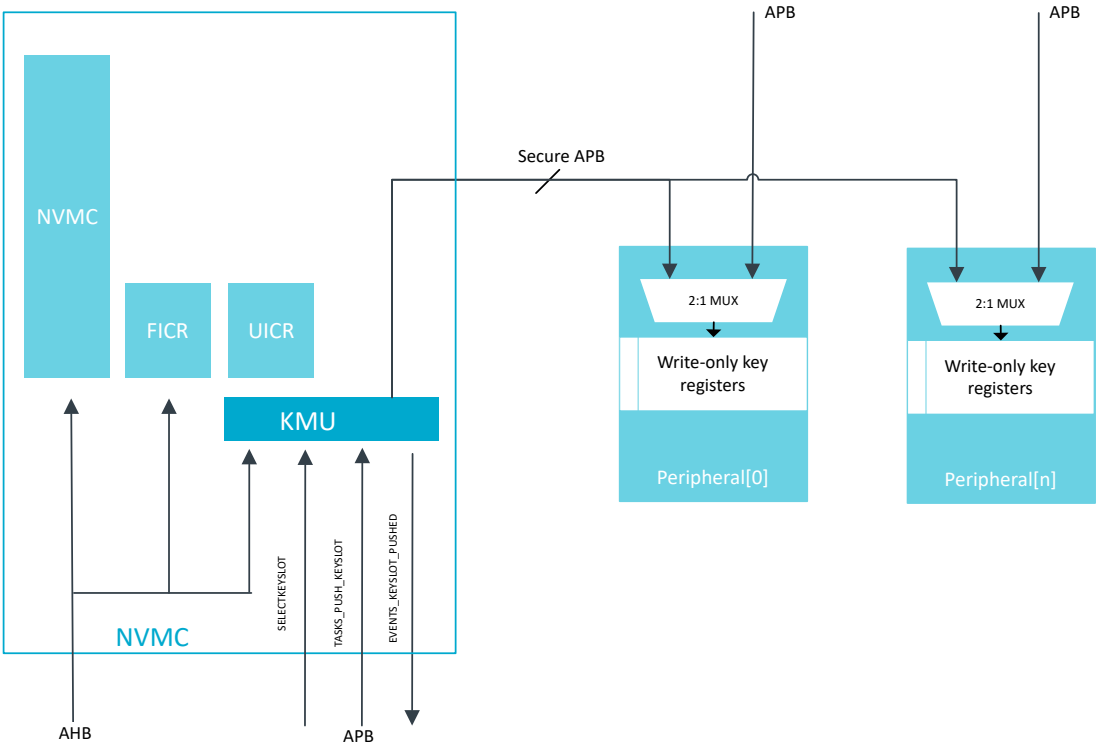

Figure 37: Tasks and events pattern for key slots

Pushing a key slot over secure APB is a four-step process:

1. Select the key slot on which the KMU shall operate by writing the desired key slot ID into KMU->SELECTKEYSLOT.
2. Start TASKS_PUSH_KEYSLOT to initiate a secure APB transaction, writing the 128-bit key value associated with the selected key slot into address defined in KEYSLOT.CONFIG[ID-1].DEST.
3. After completing the secure APB transaction, the 128-bit key value is ready for use by the peripheral and EVENTS_KEYSLOT_PUSHED is triggered.
4. Select key slot 0.

> **Note:** If a key value is distributed over multiple key slots due to its key size, exceeding the maximum 128-bit key value limitation, then each distributed key slot must be pushed individually in order to transfer the entire key value over secure APB.

Step 3 will trigger other events than EVENTS_KEYSLOT_PUSHED if the following violations are detected:

- EVENTS_KEYSLOT_ERROR:
  - If no key slot is selected
  - If a key slot has no destination address configured
  - If when pushing a key slot, flash, or peripheral returns an error
  - If pushing a key slot when push permissions are disabled

- If attempting to push a key slot with default permissions
- EVENTS_KEYSLOT_REVOKED if a key slot is marked as revoked in its key header configuration

6.8.4.2.5 Revoking the key slots

All key slots within the key storage area can be marked as revoked.

To revoke any key slots, write to the STATE field in the KEYSLOT.CONFIG[ID-1].PERM register. The following rules apply to keys that have been revoked:

1. Key slots that have the PUSH field enabled in PERM register can no longer be pushed. If a revoked key slot is selected and task TASKS_PUSH_KEYSLOT is started, the event EVENTS_KEYSLOT_REVOKED is triggered.
2. Key slots that have the READ field enabled in PERM register can no longer be read. Any read operation to a revoked key value will return word 0xDEADDEAD.
3. Previously pushed key values stored in a peripheral write-only key register are not affected by key revocation. If secure code wants to enforce that a revoked key is no longer usable by a peripheral for cryptographic operations, the secure code should disable or reset the peripheral in question.

6.8.4.3 STATUS register

The KMU uses a STATUS register to indicate its status of operation. The SELECTED bit will be asserted whenever the currently selected key slot is successfully read from or written to.

All read or write operations to other key slots than what is currently selected in KMU->SELECTKEYSLOT will assert the BLOCKED bit. The BLOCKED bit will also be asserted if the KMU fails to select a key slot, or if a request has been blocked due to an access violation. Normal operation using the KMU should never trigger the BLOCKED bit. If this bit is triggered during the development phase, it indicates that the code is using the KMU incorrectly.

The STATUS register is reset every time register SELECTKEYSLOT is written.

6.8.5 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
KMU : S KMU : NS	0x50039000 0x40039000	HF	NS	NA	Yes	Key management unit

Register overview

Register	Offset	TZ	Description
TASKS_PUSH_KEYSLOT	0x0000		Push a key slot over secure APB
EVENTS_KEYSLOT_PUSHED	0x100		Key slot successfully pushed over secure APB
EVENTS_KEYSLOT_REVOKED	0x104		Key slot has been revoked and cannot be tasked for selection
EVENTS_KEYSLOT_ERROR	0x108		No key slot selected, no destination address defined, or error during push operation
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
INTPEND	0x30C		Pending interrupts
STATUS	0x40C		Status bits for KMU operation
SELECTKEYSLOT	0x500		Select key slot to be read over AHB or pushed over secure APB when TASKS_PUSH_KEYSLOT is started

6.8.5.1 TASKS_PUSH_KEYSLOT

Address offset: 0x0000

Push a key slot over secure APB

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_PUSH_KEYSLOT			Push a key slot over secure APB
			Trigger	1	Trigger task

6.8.5.2 EVENTS_KEYSLOT_PUSHED

Address offset: 0x100

Key slot successfully pushed over secure APB

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_KEYSLOT_PUSHED			Key slot successfully pushed over secure APB
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.8.5.3 EVENTS_KEYSLOT_REVOKED

Address offset: 0x104

Key slot has been revoked and cannot be tasked for selection

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_KEYSLOT_REVOKED			Key slot has been revoked and cannot be tasked for selection
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.8.5.4 EVENTS_KEYSLOT_ERROR

Address offset: 0x108

No key slot selected, no destination address defined, or error during push operation

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	EVENTS_KEYSLOT_ERROR			No key slot selected, no destination address defined, or error during push operation
			NotGenerated	0	Event not generated
			Generated	1	Event generated

6.8.5.5 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	KEYSLOT_PUSHED			Enable or disable interrupt for event KEYSLOT_PUSHED
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	KEYSLOT_REVOKED			Enable or disable interrupt for event KEYSLOT_REVOKED
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	KEYSLOT_ERROR			Enable or disable interrupt for event KEYSLOT_ERROR
			Disabled	0	Disable
			Enabled	1	Enable

6.8.5.6 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	KEYSLOT_PUSHED			Write '1' to enable interrupt for event KEYSLOT_PUSHED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	KEYSLOT_REVOKED			Write '1' to enable interrupt for event KEYSLOT_REVOKED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	KEYSLOT_ERROR			Write '1' to enable interrupt for event KEYSLOT_ERROR
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.8.5.7 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	KEYSLOT_PUSHED			Write '1' to disable interrupt for event KEYSLOT_PUSHED
			Clear	1	Disable

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
			Disabled	0																															
			Enabled	1																															
B	RW	KEYSLOT_REVOKED																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															
C	RW	KEYSLOT_ERROR																																	
			Clear	1																															
			Disabled	0																															
			Enabled	1																															

6.8.5.8 INTPEND

Address offset: 0x30C

Pending interrupts

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																	C	B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	KEYSLOT_PUSHED																																	
			NotPending	0																															
			Pending	1																															
B	R	KEYSLOT_REVOKED																																	
			NotPending	0																															
			Pending	1																															
C	R	KEYSLOT_ERROR																																	
			NotPending	0																															
			Pending	1																															

6.8.5.9 STATUS

Address offset: 0x40C

Status bits for KMU operation

This register is reset and re-written by the KMU whenever SELECTKEYSLOT is written

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	R	SELECTED																																	
			Disabled	0																															
			Enabled	1																															
B	R	BLOCKED																																	
			Disabled	0																															
			Enabled	1																															

6.8.5.10 SELECTKEYSLOT

Address offset: 0x500

Select key slot to be read over AHB or pushed over secure APB when TASKS_PUSH_KEYSLOT is started

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																									A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ID			Select key slot ID to be read over AHB, or pushed over secure APB, when TASKS_PUSH_KEYSLOT is started. NOTE: ID=0 is not a valid key slot ID. The 0 ID should be used when the KMU is idle or not in use. NOTE: Index N in UICR->KEYSLOT.KEY[N] and UICR->KEYSLOT.CONFIG[N] corresponds to KMU key slot ID=N+1.

6.9 PDM — Pulse density modulation interface

The pulse density modulation (PDM) module enables input of pulse density modulated signals from external audio frontends, for example, digital microphones. The PDM module generates the PDM clock and supports single-channel or dual-channel (left and right) data input. Data is transferred directly to RAM buffers using EasyDMA.

Listed here are the main features for PDM:

- Up to two PDM microphones configured as a left/right pair using the same data input
- 16 kHz output sample rate, 16-bit samples
- EasyDMA support for sample buffering
- HW decimation filters
- Selectable ratio of 64 or 80 between PDM_CLK and output sample rate

The PDM module illustrated below is interfacing up to two digital microphones with the PDM interface. EasyDMA is implemented to relieve the real-time requirements associated with controlling of the PDM slave from a low priority CPU execution context. It also includes all the necessary digital filter elements to produce pulse code modulation (PCM) samples. The PDM module allows continuous audio streaming.

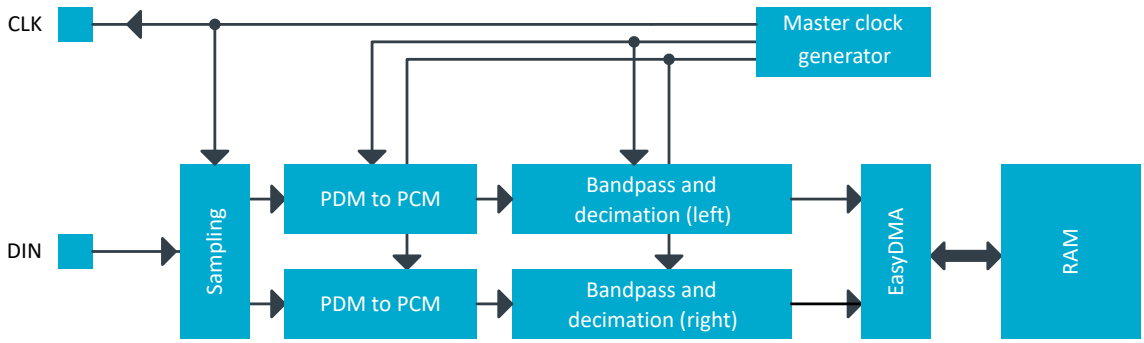

Figure 38: PDM module

6.9.1 Master clock generator

The master clock generator's PDMCLKCTRL register allows adjusting the PDM clock's frequency.

The master clock generator does not add any jitter to the HFCLK source chosen. It is recommended (but not mandatory) to use the Xtal as HFCLK source.

6.9.2 Module operation

By default, bits from the left PDM microphone are sampled on PDM_CLK falling edge, and bits for the right are sampled on the rising edge of PDM_CLK, resulting in two bitstreams. Each bitstream is fed into a digital filter which converts the PDM stream into 16-bit PCM samples, then filters and down-samples them to reach the appropriate sample rate.

The EDGE field in the MODE register allows swapping left and right, so that left will be sampled on rising edge, and right on falling.

The PDM module uses EasyDMA to store the samples coming out from the filters into one buffer in RAM. Depending on the mode chosen in the OPERATION field in the MODE register, memory either contains alternating left and right 16-bit samples (Stereo), or only left 16-bit samples (Mono). To ensure continuous PDM sampling, it is up to the application to update the EasyDMA destination address pointer as the previous buffer is filled.

The continuous transfer can be started or stopped by sending the START and STOP tasks. STOP becomes effective after the current frame has finished transferring, which will generate the STOPPED event. The STOPPED event indicates that all activity in the module is finished, and that the data is available in RAM (EasyDMA has finished transferring as well). Attempting to restart before receiving the STOPPED event may result in unpredictable behavior.

6.9.3 Decimation filter

In order to convert the incoming data stream into PCM audio samples, a decimation filter is included in the PDM interface module.

The input of the filter is the two-channel PDM serial stream (with left channel on clock high, right channel on clock low). Depending on the RATIO selected, its output is 2 × 16-bit PCM samples at a sample rate either 64 times or 80 times (depending on the RATIO register) lower than the PDM clock rate.

The filter stage of each channel is followed by a digital volume control, to attenuate or amplify the output samples in a range of -20 dB to +20 dB around the default (reset) setting, defined by $G_{PDM,default}$. The gain is controlled by the GAINL and GAINR registers.

As an example, if the goal is to achieve 2500 RMS output samples (16-bit) with a 1 kHz 90 dBA signal into a -26 dBFS sensitivity PDM microphone, do the following:

- Sum the PDM module's default gain ($G_{PDM,default}$) and the gain introduced by the microphone and acoustic path of his implementation (an attenuation would translate into a negative gain)
- Adjust GAINL and GAINR by the above summed amount. Assuming that only the PDM module influences the gain, GAINL and GAINR must be set to $-G_{PDM,default}$ dB to achieve the requirement.

With $G_{PDM,default}$=3.2 dB, and as GAINL and GAINR are expressed in 0.5 dB steps, the closest value to program would be 3.0 dB, which can be calculated as:

```
GAINL = GAINR = (DefaultGain - (2 * 3))
```

Remember to check that the resulting values programmed into GAINL and GAINR fall within MinGain and MaxGain.

6.9.4 EasyDMA

Samples will be written directly to RAM, and EasyDMA must be configured accordingly.

The address pointer for the EasyDMA channel is set in SAMPLE.PTR register. If the destination address set in SAMPLE.PTR is not pointing to the Data RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Memory on page 21 for more information about the different memory regions.

DMA supports Stereo (Left+Right 16-bit samples) and Mono (Left only) data transfer, depending on the setting in the OPERATION field in the MODE register. The samples are stored little endian.

MODE.OPERATION	Bits per sample	Result stored per RAM word	Physical RAM allocated (32-bit words)	Result boundary indexes in RAM	Note
Stereo	32 (2x16)	L+R	ceil(SAMPLE.MAXCNT/2)	R0=[31:16]; L0=[15:0]	Default
Mono	16	2xL	ceil(SAMPLE.MAXCNT/2)	L1=[31:16]; L0=[15:0]	

Table 23: DMA sample storage

The destination buffer in RAM consists of one block, the size of which is set in SAMPLE.MAXCNT register. Format is number of 16-bit samples. The physical RAM allocated is always:

```
(RAM allocation, in bytes) = SAMPLE.MAXCNT * 2;
```

(but the mapping of the samples depends on MODE.OPERATION).

If OPERATION=Stereo, RAM will contain a succession of left and right samples.

If OPERATION=Mono, RAM will contain a succession of left only samples.

For a given value of SAMPLE.MAXCNT, the buffer in RAM can contain half the stereo sampling time as compared to the mono sampling time.

The PDM acquisition can be started by the START task, after the SAMPLE.PTR and SAMPLE.MAXCNT registers have been written. When starting the module, it will take some time for the filters to start outputting valid data. Transients from the PDM microphone itself may also occur. The first few samples (typically around 50) might hence contain invalid values or transients. It is therefore advised to discard the first few samples after a PDM start.

As soon as the STARTED event is received, the firmware can write the next SAMPLE.PTR value (this register is double-buffered), to ensure continuous operation.

When the buffer in RAM is filled with samples, an END event is triggered. The firmware can start processing the data in the buffer. Meanwhile, the PDM module starts acquiring data into the new buffer pointed to by SAMPLE.PTR, and sends a new STARTED event, so that the firmware can update SAMPLE.PTR to the next buffer address.

6.9.5 Hardware example

PDM can be configured with a single microphone (mono), or with two microphones.

When a single microphone is used, connect the microphone clock to CLK, and data to DIN.

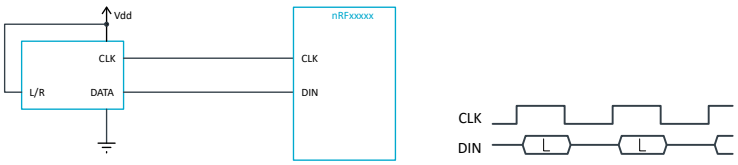

Figure 39: Example of a single PDM microphone, wired as left

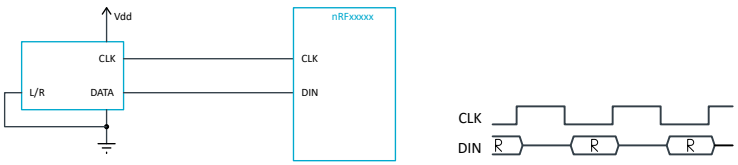

Figure 40: Example of a single PDM microphone, wired as right

Note that in a single-microphone (mono) configuration, depending on the microphone's implementation, either the left or the right channel (sampled at falling or rising CLK edge respectively) will contain reliable data.

If two microphones are used, one of them must be set as left, the other as right (L/R pin tied high or to GND on the respective microphone). It is strongly recommended to use two microphones of exactly the same brand and type so that their timings in left and right operation match.

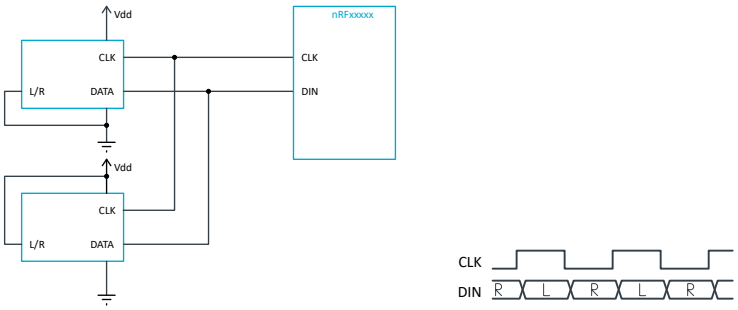

Figure 41: Example of two PDM microphones

6.9.6 Pin configuration

The CLK and DIN signals associated to the PDM module are mapped to physical pins according to the configuration specified in the PSEL.CLK and PSEL.DIN registers respectively. If the CONNECT field in any PSEL register is set to Disconnected, the associated PDM module signal will not be connected to the required physical pins and will not operate properly.

The PSEL.CLK and PSEL.DIN registers and their configurations are only used as long as the PDM module is enabled, and retained only as long as the device is in System ON mode. See POWER — Power control on page 63 for more information about power modes. When the peripheral is disabled, the pins will behave as regular GPIOs, and use the configuration in their respective OUT bit field and PIN_CNF[n] register.

To ensure correct behavior in the PDM module, the pins used by the PDM module must be configured in the GPIO peripheral as described in GPIO configuration before enabling peripheral on page 152 before enabling the PDM module. This is to ensure that the pins used by the PDM module are driven correctly if the PDM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected I/Os as long as the PDM module is supposed to be connected to an external PDM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

PDM signal	PDM pin	Direction	Output value	Comment
CLK	As specified in PSEL.CLK	Output	0	
DIN	As specified in PSEL.DIN	Input	Not applicable	

Table 24: GPIO configuration before enabling peripheral

6.9.7 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
PDM : S PDM : NS	0x50026000 0x40026000	US	NS	SA	No	Pulse density modulation (digital microphone) interface

Register overview

Register	Offset	TZ	Description
TASKS_START	0x000		Starts continuous PDM transfer
TASKS_STOP	0x004		Stops PDM transfer
SUBSCRIBE_START	0x080		Subscribe configuration for task START
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP
EVENTS_STARTED	0x100		PDM transfer has started
EVENTS_STOPPED	0x104		PDM transfer has finished
EVENTS_END	0x108		The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP task has been received) to Data RAM
PUBLISH_STARTED	0x180		Publish configuration for event STARTED
PUBLISH_STOPPED	0x184		Publish configuration for event STOPPED
PUBLISH_END	0x188		Publish configuration for event END
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
ENABLE	0x500		PDM module enable register
PDMCLKCTRL	0x504		PDM clock generator control
MODE	0x508		Defines the routing of the connected PDM microphones' signals
GAINL	0x518		Left output gain adjustment
GAINR	0x51C		Right output gain adjustment
RATIO	0x520		Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly.
PSEL.CLK	0x540		Pin number configuration for PDM CLK signal
PSEL.DIN	0x544		Pin number configuration for PDM DIN signal
SAMPLE.PTR	0x560		RAM address pointer to write samples to with EasyDMA
SAMPLE.MAXCNT	0x564		Number of samples to allocate memory for in EasyDMA mode

6.9.7.1 TASKS_START

Address offset: 0x000

Starts continuous PDM transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value								Description																							
A	W	TASKS_START										Starts continuous PDM transfer																							
			Trigger	1								Trigger task																							

6.9.7.2 TASKS_STOP

Address offset: 0x004

Stops PDM transfer

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value								Description																							
A	W	TASKS_STOP										Stops PDM transfer																							
			Trigger	1								Trigger task																							

6.9.7.3 SUBSCRIBE_START

Address offset: 0x080

Subscribe configuration for task START

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	CHIDX		[0..255]																								DPPI channel that task START will subscribe to							
B	RW	EN																																	
			Disabled	0																								Disable subscription							
			Enabled	1																								Enable subscription							

6.9.7.4 SUBSCRIBE_STOP

Address offset: 0x084

Subscribe configuration for task STOP

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	CHIDX		[0..255]																								DPPI channel that task STOP will subscribe to							
B	RW	EN																																	
			Disabled	0																								Disable subscription							
			Enabled	1																								Enable subscription							

6.9.7.5 EVENTS_STARTED

Address offset: 0x100

PDM transfer has started

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																								Description							
A	RW	EVENTS_STARTED																										PDM transfer has started							
			NotGenerated	0																								Event not generated							
			Generated	1																								Event generated							

6.9.7.6 EVENTS_STOPPED

Address offset: 0x104

PDM transfer has finished

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_STOPPED																																	
			NotGenerated	0																															
			Generated	1																															

6.9.7.7 EVENTS_END

Address offset: 0x108

The PDM has written the last sample specified by SAMPLE.MAXCNT (or the last sample after a STOP task has been received) to Data RAM

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	EVENTS_END																																	
			NotGenerated	0																															
			Generated	1																															

6.9.7.8 PUBLISH_STARTED

Address offset: 0x180

Publish configuration for event STARTED

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

6.9.7.9 PUBLISH_STOPPED

Address offset: 0x184

Publish configuration for event STOPPED

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																								A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	CHIDX		[0..255]																															
B	RW	EN																																	
			Disabled	0																															
			Enabled	1																															

6.9.7.10 PUBLISH_END

Address offset: 0x188

Publish configuration for event END

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID	B																								A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that event END will publish to
B	RW	EN			
			Disabled	0	Disable publishing
			Enabled	1	Enable publishing

6.9.7.11 INTEN

Address offset: 0x300

Enable or disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	STARTED			Enable or disable interrupt for event STARTED
			Disabled	0	Disable
			Enabled	1	Enable
B	RW	STOPPED			Enable or disable interrupt for event STOPPED
			Disabled	0	Disable
			Enabled	1	Enable
C	RW	END			Enable or disable interrupt for event END
			Disabled	0	Disable
			Enabled	1	Enable

6.9.7.12 INTENSET

Address offset: 0x304

Enable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	STARTED			Write '1' to enable interrupt for event STARTED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	STOPPED			Write '1' to enable interrupt for event STOPPED
			Set	1	Enable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	END			Write '1' to enable interrupt for event END
			Set	1	Enable

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.9.7.13 INTENCLR

Address offset: 0x308

Disable interrupt

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														C	B	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	STARTED			Write '1' to disable interrupt for event STARTED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
B	RW	STOPPED			Write '1' to disable interrupt for event STOPPED
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled
C	RW	END			Write '1' to disable interrupt for event END
			Clear	1	Disable
			Disabled	0	Read: Disabled
			Enabled	1	Read: Enabled

6.9.7.14 ENABLE

Address offset: 0x500

PDM module enable register

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	ENABLE			Enable or disable PDM module
			Disabled	0	Disable
			Enabled	1	Enable

6.9.7.15 PDMCLKCTRL

Address offset: 0x504

PDM clock generator control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x08400000				**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	FREQ																																	
			1000K	0x08000000																															
			Default	0x08400000																															
			1067K	0x08800000																															
			1231K	0x09800000																															
			1280K	0x0A000000																															
			1333K	0x0A800000																															

	PDM_CLK frequency configuration.
	PDM_CLK = 32 MHz / 32 = 1.000 MHz
	PDM_CLK = 32 MHz / 31 = 1.032 MHz. Nominal clock for RATIO=Ratio64.
	PDM_CLK = 32 MHz / 30 = 1.067 MHz
	PDM_CLK = 32 MHz / 26 = 1.231 MHz
	PDM_CLK = 32 MHz / 25 = 1.280 MHz. Nominal clock for RATIO=Ratio80.
	PDM_CLK = 32 MHz / 24 = 1.333 MHz

6.9.7.16 MODE

Address offset: 0x508

Defines the routing of the connected PDM microphones' signals

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																		B	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																															
A	RW	OPERATION																																	
			Stereo	0																															
			Mono	1																															
B	RW	EDGE																																	
			LeftFalling	0																															
			LeftRising	1																															

	Mono or stereo operation
	Sample and store one pair (left + right) of 16-bit samples per RAM word R=[31:16]; L=[15:0]
	Sample and store two successive left samples (16 bits each) per RAM word L1=[31:16]; L0=[15:0]
	Defines on which PDM_CLK edge left (or mono) is sampled
	Left (or mono) is sampled on falling edge of PDM_CLK
	Left (or mono) is sampled on rising edge of PDM_CLK

6.9.7.17 GAINL

Address offset: 0x518

Left output gain adjustment

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													A	A	A	A	A	A	A
Reset 0x00000028				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	GAINL																											Left output gain adjustment, in 0.5 dB steps, around the default module gain (see electrical parameters)						
																													0x00 -20 dB gain adjust						
																													0x01 -19.5 dB gain adjust						
																													(...)						
																													0x27 -0.5 dB gain adjust						
																													0x28 0 dB gain adjust						
																													0x29 +0.5 dB gain adjust						
																													(...)						
																													0x4F +19.5 dB gain adjust						
																													0x50 +20 dB gain adjust						
			MinGain	0x00																									-20 dB gain adjustment (minimum)						
			DefaultGain	0x28																									0 dB gain adjustment						
			MaxGain	0x50																									+20 dB gain adjustment (maximum)						

6.9.7.18 GAINR

Address offset: 0x51C

Right output gain adjustment

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																													A	A	A	A	A	A	A
Reset 0x00000028				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	GAINR																											Right output gain adjustment, in 0.5 dB steps, around the default module gain (see electrical parameters)						
			MinGain	0x00																									-20 dB gain adjustment (minimum)						
			DefaultGain	0x28																									0 dB gain adjustment						
			MaxGain	0x50																									+20 dB gain adjustment (maximum)						

6.9.7.19 RATIO

Address offset: 0x520

Selects the ratio between PDM_CLK and output sample rate. Change PDMCLKCTRL accordingly.

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																			A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value																									Description						
A	RW	RATIO																											Selects the ratio between PDM_CLK and output sample rate						
			Ratio64	0																									Ratio of 64						
			Ratio80	1																									Ratio of 80						

6.9.7.20 PSEL.CLK

Address offset: 0x540

Pin number configuration for PDM CLK signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.9.7.21 PSEL.DIN

Address offset: 0x544

Pin number configuration for PDM DIN signal

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				B																											A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	PIN		[0..31]								Pin number																							
B	RW	CONNECT										Connection																							
			Disconnected	1								Disconnect																							
			Connected	0								Connect																							

6.9.7.22 SAMPLE.PTR

Address offset: 0x560

RAM address pointer to write samples to with EasyDMA

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	SAMPLEPTR										Address to write PDM samples to over DMA																							

Note: See the memory chapter for details about which memories are available for EasyDMA.

6.9.7.23 SAMPLE.MAXCNT

Address offset: 0x564

Number of samples to allocate memory for in EasyDMA mode

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																					A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000				**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
ID	R/W	Field	Value ID	Value								Description																							
A	RW	BUFFSIZE		[0..32767]								Length of DMA RAM allocation in number of samples																							

6.9.8 Electrical specification

6.9.8.1 PDM Electrical Specification

Symbol	Description	Min.	Typ.	Max.	Units
$f_{PDM,CLK,64}$	PDM clock speed. PDMCLKCTRL = Default (Setting needed for 16 MHz sample frequency @ RATIO = Ratio64)		1.032		MHz
$f_{PDM,CLK,80}$	PDM clock speed. PDMCLKCTRL = 1280K (Setting needed for 16 MHz sample frequency @ RATIO = Ratio80)		1.28		MHz
$t_{PDM,JITTER}$	Jitter in PDM clock output			20	ns
$T_{dPDM,CLK}$	PDM clock duty cycle	40	50	60	%
$t_{PDM,DATA}$	Decimation filter delay			5	ms
$t_{PDM,cv}$	Allowed clock edge to data valid			125	ns
$t_{PDM,ci}$	Allowed (other) clock edge to data invalid	0			ns
$t_{PDM,s}$	Data setup time at $f_{PDM,CLK}$=1.024 MHz or 1.280 MHz	65			ns
$t_{PDM,h}$	Data hold time at $f_{PDM,CLK}$=1.024 MHz or 1.280 MHz	0			ns
$G_{PDM,default}$	Default (reset) absolute gain of the PDM module		3.2		dB

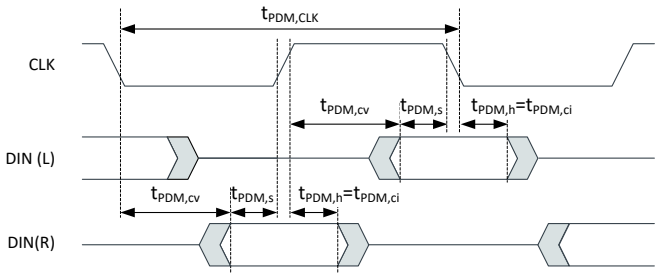

Figure 42: PDM timing diagram

6.10 PWM — Pulse width modulation

The pulse width modulation (PWM) module enables the generation of pulse width modulated signals on GPIO. The module implements an up or up-and-down counter with four PWM channels that drive assigned GPIOs.

The following are the main features of a PWM module:

- Programmable PWM frequency
- Up to four PWM channels with individual polarity and duty cycle values
- Edge or center-aligned pulses across PWM channels
- Multiple duty cycle arrays (sequences) defined in RAM
- Autonomous and glitch-free update of duty cycle values directly from memory through EasyDMA (no CPU involvement)
- Change of polarity, duty cycle, and base frequency possibly on every PWM period
- RAM sequences can be repeated or connected into loops

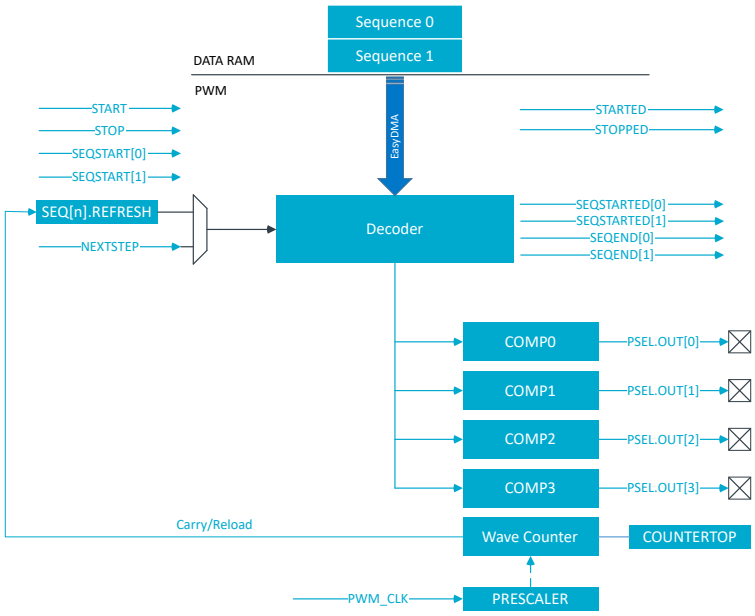

Figure 43: PWM module

6.10.1 Wave counter

The wave counter is responsible for generating the pulses, at a duty cycle that depends on the compare values and at a frequency that depends on COUNTERTOP.

There is one common 15-bit counter with four compare channels. Thus, all four channels will share the same period (PWM frequency) but can have individual duty cycle and polarity. The polarity is set by the most significant bit (MSB) of the value read from RAM (see figure Decoder memory access modes on page 165). When the MSB bit is high (FallingEdge polarity), OUT[n] starts high to become low during the given PWM cycle, whereas the inverse occurs for RisingEdge polarity. Whether the counter counts up, or up and down, is controlled by the MODE register.

The timer top value is controlled by the COUNTERTOP register. This register value, in conjunction with the selected PRESCALER of the PWM_CLK, will result in a given PWM period. A COUNTERTOP value smaller than the compare setting will result in a state where no PWM edges are generated. OUT[n] is held high, given that the polarity is set to FallingEdge. All compare registers are internal and can only be configured through decoder presented later. COUNTERTOP can be safely written at any time.

Sampling follows the START task. If DECODER.LOAD=WaveForm, the register value is ignored and taken from RAM instead (see section Decoder with EasyDMA on page 165 for more details). If DECODER.LOAD is anything else than the WaveForm, it is sampled following a STARTSEQ[n] task and when loading a new value from RAM during a sequence playback.

The following figure shows the counter operating in up mode (MODE=PWM_MODE_Up), with two PWM channels with the same frequency but different duty cycle:

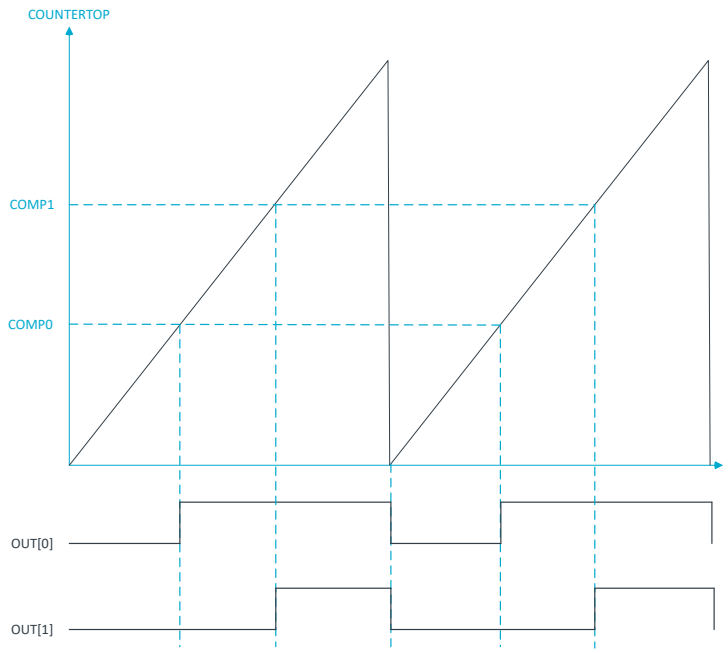

Figure 44: PWM counter in up mode example - RisingEdge polarity

The counter is automatically reset to zero when COUNTERTOP is reached and OUT[n] will invert. OUT[n] is held low if the compare value is 0 and held high if set to COUNTERTOP, given that the polarity is set to FallingEdge. Counter running in up mode results in pulse widths that are edge-aligned. The following is the code for the counter in up mode example:

```
uint16_t pwm_seq[4] = {PWM_CH0_DUTY, PWM_CH1_DUTY, PWM_CH2_DUTY, PWM_CH3_DUTY};
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->PSEL.OUT[1] = (second_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Individual << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(pwm_seq) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

When the counter is running in up mode, the following formula can be used to compute the PWM period and the step size:

PWM period: $T_{PWM(Up)} = T_{PWM\_CLK} * COUNTERTOP$

Step width/Resolution: $T_{steps} = T_{PWM\_CLK}$

The following figure shows the counter operating in up-and-down mode (MODE=PWM_MODE_UpAndDown), with two PWM channels with the same frequency but different duty cycle and output polarity:

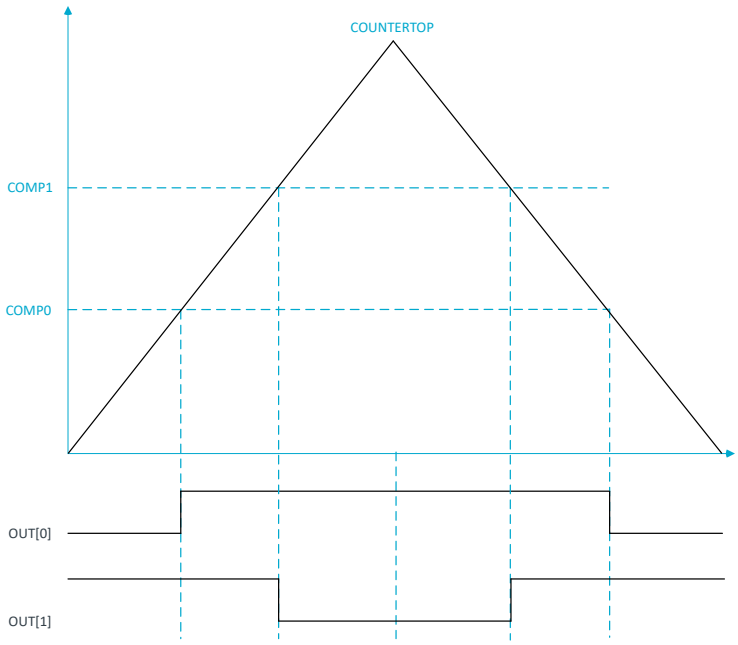

Figure 45: PWM counter in up-and-down mode example

The counter starts decrementing to zero when COUNTERTOP is reached and will invert the OUT[n] when compare value is hit for the second time. This results in a set of pulses that are center-aligned. The following is the code for the counter in up-and-down mode example:

```
uint16_t pwm_seq[4] = {PWM_CH0_DUTY, PWM_CH1_DUTY, PWM_CH2_DUTY, PWM_CH3_DUTY};
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->PSEL.OUT[1] = (second_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_UpAndDown << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Individual << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(pwm_seq) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(pwm_seq) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

When the counter is running in up-and-down mode, the following formula can be used to compute the PWM period and the step size:

$$T_{PWM(Up\ And\ Down)} = T_{PWM\_CLK} * 2 * COUNTERTOP$$

Step width/Resolution: $T_{steps} = T_{PWM\_CLK} * 2$

6.10.2 Decoder with EasyDMA

The decoder uses EasyDMA to take PWM parameters stored in RAM and update the internal compare registers of the wave counter, based on the mode of operation.

PWM parameters are organized into a sequence containing at least one half word (16 bit). Its most significant bit[15] denotes the polarity of the OUT[n] while bit[14:0] is the 15-bit compare value.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Id																	B	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Id	RW	Field	Value Id	Value	Description
A	RW	COMPARE			Duty cycle setting - value loaded to internal compare register
B	RW	POLARITY			Edge polarity of GPIO.
			RisingEdge	0	First edge within the PWM period is rising
			FallingEdge	1	First edge within the PWM period is falling

The DECODER register controls how the RAM content is interpreted and loaded into the internal compare registers. The LOAD field controls if the RAM values are loaded to all compare channels, or to update a group or all channels with individual values. The following figure illustrates how parameters stored in RAM are organized and routed to various compare channels in different modes:

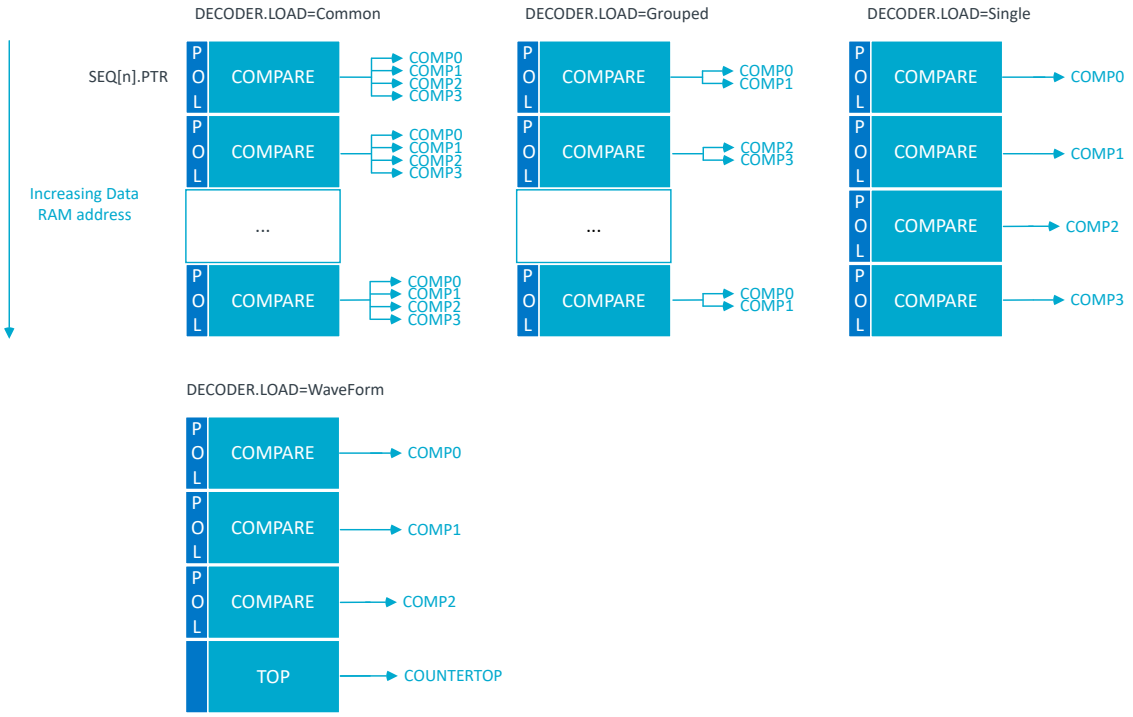

Figure 46: Decoder memory access modes

A special mode of operation is available when DECODER.LOAD is set to WaveForm. In this mode, up to three PWM channels can be enabled - OUT[0] to OUT[2]. In RAM, four values are loaded at a time: the first, second and third location are used to load the values, and the fourth RAM location is used to load

the COUNTERTOP register. This way one can have up to three PWM channels with a frequency base that changes on a per PWM period basis. This mode of operation is useful for arbitrary wave form generation in applications, such as LED lighting.

The register SEQ[n].REFRESH=N (one per sequence n=0 or 1) will instruct a new RAM stored pulse width value on every $(N+1)^{th}$ PWM period. Setting the register to zero will result in a new duty cycle update every PWM period, as long as the minimum PWM period is observed.

Note that registers SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored when DECODER.MODE=NextStep. The next value is loaded upon every received NEXTSTEP task.

SEQ[n].PTR is the pointer used to fetch COMPARE values from RAM. If the SEQ[n].PTR is not pointing to a RAM region, an EasyDMA transfer may result in a HardFault or RAM corruption. See Memory on page 21 for more information about the different memory regions. After the SEQ[n].PTR is set to the desired RAM location, the SEQ[n].CNT register must be set to the number of 16-bit half words in the sequence. It is important to observe that the Grouped mode requires one half word per group, while the Single mode requires one half word per channel, thus increasing the RAM size occupation. If PWM generation is not running when the SEQSTART[n] task is triggered, the task will load the first value from RAM and then start the PWM generation. A SEQSTARTED[n] event is generated as soon as the EasyDMA has read the first PWM parameter from RAM and the wave counter has started executing it. When LOOP.CNT=0, sequence n=0 or 1 is played back once. After the last value in the sequence has been loaded and started executing, a SEQEND[n] event is generated. The PWM generation will then continue with the last loaded value. The following figure illustrates an example of a simple playback.

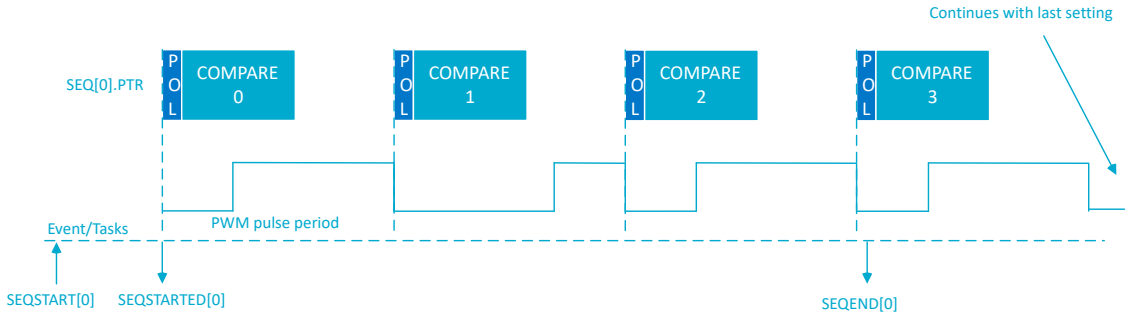

Figure 47: Simple sequence example

The following source code is used for configuration and timing details in a sequence where only sequence 0 is used and only run once with a new PWM duty cycle for each period.

```
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (PWM_LOOP_CNT_Disabled << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 0;
NRF_PWM0->SEQ[0].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

To completely stop the PWM generation and force the associated pins to a defined state, a STOP task can be triggered at any time. A STOPPED event is generated when the PWM generation has stopped at the end of the currently running PWM period, and the pins go into their idle state as defined in GPIO OUT register. PWM generation can then only be restarted through a SEQSTART[n] task. SEQSTART[n] will resume PWM generation after having loaded the first value from the RAM buffer defined in the SEQ[n].PTR register.

The following table indicates when specific registers get sampled by the hardware. Care should be taken when updating these registers to avoid that values are applied earlier than expected.

Register	Taken into account by hardware	Recommended (safe) update
SEQ[n].PTR	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[n].CNT	When sending the SEQSTART[n] task	After having received the SEQSTARTED[n] event
SEQ[0].ENDDELAY	When sending the SEQSTART[0] task Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	Before starting sequence [0] through a SEQSTART[0] task When no more value from sequence [0] gets loaded from RAM (indicated by the SEQEND[0] event) At any time during sequence [1] (which starts when the SEQSTARTED[1] event is generated)
SEQ[1].ENDDELAY	When sending the SEQSTART[1] task Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	Before starting sequence [1] through a SEQSTART[1] task When no more value from sequence [1] gets loaded from RAM (indicated by the SEQEND[1] event) At any time during sequence [0] (which starts when the SEQSTARTED[0] event is generated)
SEQ[0].REFRESH	When sending the SEQSTART[0] task Every time a new value from sequence [0] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	Before starting sequence [0] through a SEQSTART[0] task At any time during sequence [1] (which starts when the SEQSTARTED[1] event is generated)
SEQ[1].REFRESH	When sending the SEQSTART[1] task Every time a new value from sequence [1] has been loaded from RAM and gets applied to the Wave Counter (indicated by the PWMPERIODEND event)	Before starting sequence [1] through a SEQSTART[1] task At any time during sequence [0] (which starts when the SEQSTARTED[0] event is generated)
COUNTERTOP	In DECODER.LOAD=WaveForm: this register is ignored. In all other LOAD modes: at the end of current PWM period (indicated by the PWMPERIODEND event)	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been triggered, and the STOPPED event has been received.
MODE	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been triggered, and the STOPPED event has been received.
DECODER	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been triggered, and the STOPPED event has been received.
PRESCALER	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been triggered, and the STOPPED event has been received.
LOOP	Immediately	Before starting PWM generation through a SEQSTART[n] task After a STOP task has been triggered, and the STOPPED event has been received.
PSEL.OUT[n]	Immediately	Before enabling the PWM instance through the ENABLE register

Table 25: When to safely update PWM registers

Note: SEQ[n].REFRESH and SEQ[n].ENDDELAY are ignored at the end of a complex sequence, indicated by a LOOPSDONE event. The reason for this is that the last value loaded from RAM is maintained until further action from software (restarting a new sequence or stopping PWM generation).

The following figure shows a more complex example using the register LOOP on page 183.

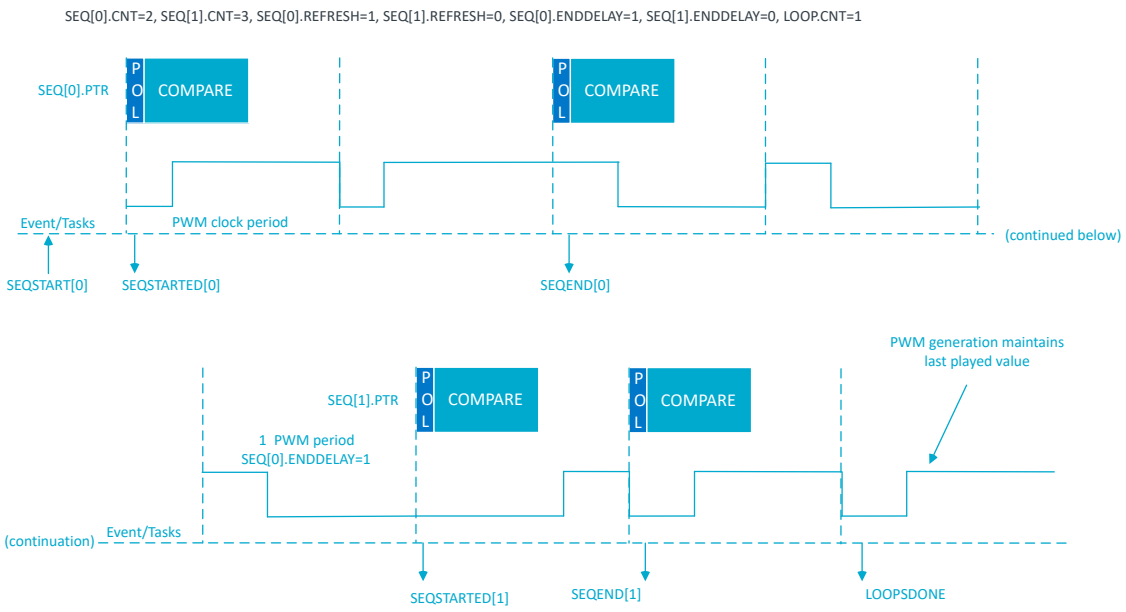

Figure 48: Example using two sequences

In this case, an automated playback takes place, consisting of SEQ[0], delay 0, SEQ[1], delay 1, then again SEQ[0], etc. The user can choose to start a complex playback with SEQ[0] or SEQ[1] through sending the SEQSTART[0] or SEQSTART[1] task. The complex playback always ends with delay 1.

The two sequences 0 and 1 are defined by the addresses of value tables in RAM (pointed to by SEQ[n].PTR) and the buffer size (SEQ[n].CNT). The rate at which a new value is loaded is defined individually for each sequence by SEQ[n].REFRESH. The chaining of sequence 1 following the sequence 0 is implicit, the LOOP.CNT register allows the chaining of sequence 1 to sequence 0 for a determined number of times. In other words, it allows to repeat a complex sequence a number of times in a fully automated way.

In the following code example, sequence 0 is defined with SEQ[0].REFRESH set to 1, meaning that a new PWM duty cycle is pushed every second PWM period. This complex sequence is started with the SEQSTART[0] task, so SEQ[0] is played first. Since SEQ[0].ENDDELAY=1 there will be one PWM period delay between last period on sequence 0 and the first period on sequence 1. Since SEQ[1].ENDDELAY=0 there is no delay 1, so SEQ[0] would be started immediately after the end of SEQ[1]. However, as LOOP.CNT is

1, the playback stops after having played SEQ[1] only once, and both SEQEND[1] and LOOPSDONE are generated (their order is not guaranteed in this case).

```
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
NRF_PWM0->LOOP        = (1 << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER   = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                      (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
NRF_PWM0->SEQ[0].PTR  = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[0].CNT  = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[0].REFRESH  = 1;
NRF_PWM0->SEQ[0].ENDDELAY = 1;
NRF_PWM0->SEQ[1].PTR  = ((uint32_t)(seq1_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[1].CNT  = ((sizeof(seq1_ram) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[1].REFRESH  = 0;
NRF_PWM0->SEQ[1].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[0] = 1;
```

The decoder can also be configured to asynchronously load new PWM duty cycle. If the DECODER.MODE register is set to NextStep, then the NEXTSTEP task will cause an update of internal compare registers on the next PWM period.

The following figures provide an overview of each part of an arbitrary sequence, in various modes (LOOP.CNT=0 and LOOP.CNT>0). In particular, the following are represented:

- Initial and final duty cycle on the PWM output(s)
- Chaining of SEQ[0] and SEQ[1] if LOOP.CNT>0
- Influence of registers on the sequence
- Events generated during a sequence
- DMA activity (loading of next value and applying it to the output(s))

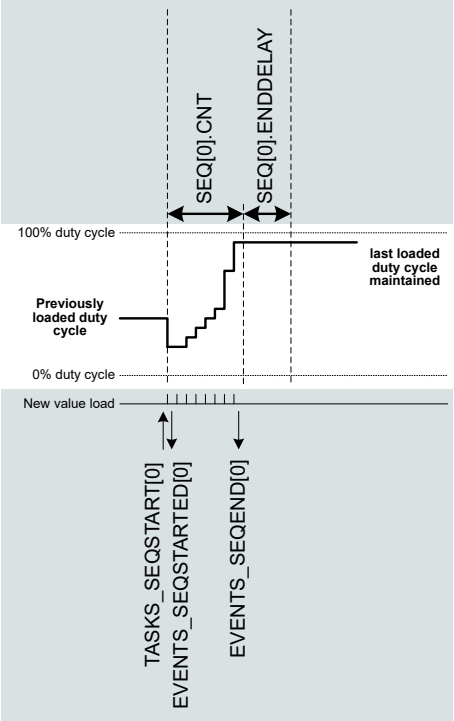

Figure 49: Single shot (LOOP.CNT=0)

Note: The single-shot example also applies to SEQ[1]. Only SEQ[0] is represented for simplicity.

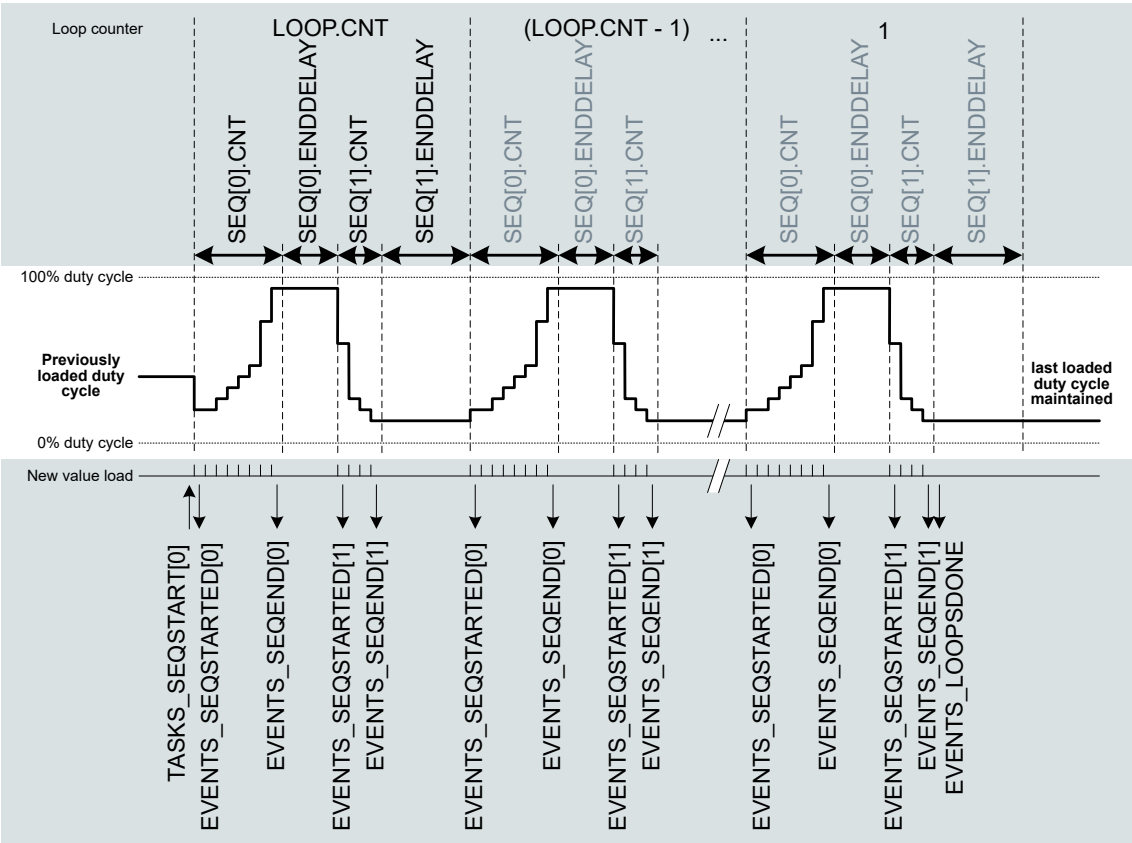

Figure 50: Complex sequence (LOOP.CNT>0) starting with SEQ[0]

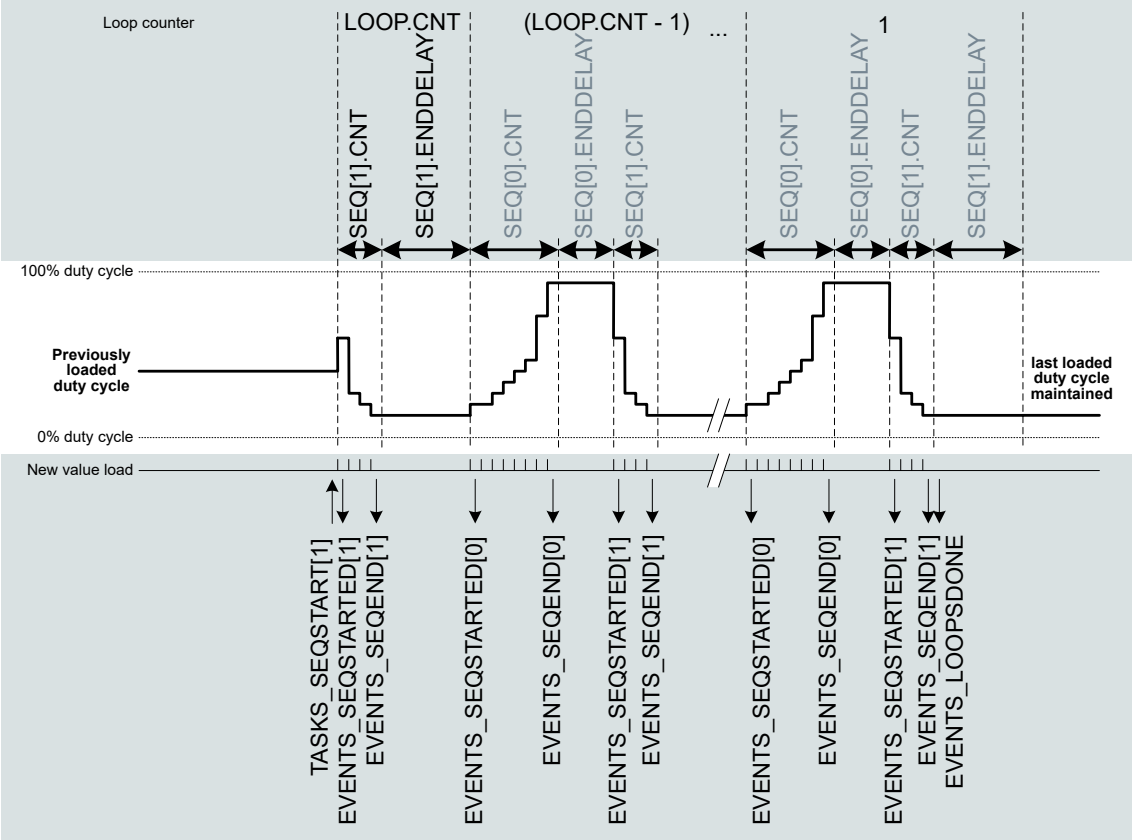

Figure 51: Complex sequence (LOOP.CNT>0) starting with SEQ[1]

Note: If a sequence is in use in a simple or complex sequence, it must have a length of SEQ[n].CNT > 0.

This example shows how the PWM module can be configured to repeat a single sequence until stopped.

```
NRF_PWM0->PSEL.OUT[0] = (first_pin << PWM_PSEL_OUT_PIN_Pos) |
                        (PWM_PSEL_OUT_CONNECT_Connected <<
                                                PWM_PSEL_OUT_CONNECT_Pos);
NRF_PWM0->ENABLE      = (PWM_ENABLE_ENABLE_Enabled << PWM_ENABLE_ENABLE_Pos);
NRF_PWM0->MODE        = (PWM_MODE_UPDOWN_Up << PWM_MODE_UPDOWN_Pos);
NRF_PWM0->PRESCALER   = (PWM_PRESCALER_PRESCALER_DIV_1 <<
                                                PWM_PRESCALER_PRESCALER_Pos);
NRF_PWM0->COUNTERTOP  = (16000 << PWM_COUNTERTOP_COUNTERTOP_Pos); //1 msec
// Enable the shortcut from LOOPSDONE event to SEQSTART1 task for infinite loop
NRF_PWM0->SHORTS      = (PWM_SHORTS_LOOPSDONE_SEQSTART1_Enabled <<
                                          PWM_SHORTS_LOOPSDONE_SEQSTART1_Pos);
// LOOP_CNT must be greater than 0 for the LOOPSDONE event to trigger and enable looping
NRF_PWM0->LOOP        = (1 << PWM_LOOP_CNT_Pos);
NRF_PWM0->DECODER     = (PWM_DECODER_LOAD_Common << PWM_DECODER_LOAD_Pos) |
                       (PWM_DECODER_MODE_RefreshCount << PWM_DECODER_MODE_Pos);
// To repeat a single sequence until stopped, it must be configured in SEQ[1]
NRF_PWM0->SEQ[1].PTR  = ((uint32_t)(seq0_ram) << PWM_SEQ_PTR_PTR_Pos);
NRF_PWM0->SEQ[1].CNT  = ((sizeof(seq0_ram) / sizeof(uint16_t)) <<
                                                PWM_SEQ_CNT_CNT_Pos);
NRF_PWM0->SEQ[1].REFRESH  = 0;
NRF_PWM0->SEQ[1].ENDDELAY = 0;
NRF_PWM0->TASKS_SEQSTART[1] = 1;
```

6.10.3 Limitations

The previous compare value is repeated if the PWM period is shorter than the time it takes for the EasyDMA to retrieve from RAM and update the internal compare registers. This is to ensure a glitch-free operation even for very short PWM periods.

Only SEQ[1] can trigger the LOOPSDONE event upon completion, not SEQ[0]. This requires looping to be enabled (LOOP > 0) and SEQ[1].CNT > 0 when sequence playback starts.

6.10.4 Pin configuration

The OUT[n] (n=0..3) signals associated with each PWM channel are mapped to physical pins according to the configuration of PSEL.OUT[n] registers. If PSEL.OUT[n].CONNECT is set to Disconnected, the associated PWM module signal will not be connected to any physical pins.

The PSEL.OUT[n] registers and their configurations are used as long as the PWM module is enabled and the PWM generation active (wave counter started). They are retained only as long as the device is in System ON mode (see the POWER section for more information about power modes).

To ensure correct behavior in the PWM module, the pins that are used must be configured in the GPIO peripheral in the following way before the PWM module is enabled:

PWM signal	PWM pin	Direction	Output value	Comment
OUT[n]	As specified in PSEL.OUT[n] (n=0..3)	Output	0	Idle state defined in GPIO OUT register

Table 26: Recommended GPIO configuration before starting PWM generation

The idle state of a pin is defined by the OUT register in the GPIO module, to ensure that the pins used by the PWM module are driven correctly. If PWM generation is stopped by triggering a STOP task, the PWM module itself is temporarily disabled or the device temporarily enters System OFF. This configuration must be retained in the GPIO for the selected pins (I/Os) for as long as the PWM module is supposed to be connected to an external PWM circuit.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

6.10.5 Registers

Instances

Instance	Base address	TrustZone			Split access	Description
		Map	Att	DMA		
PWM0 : S PWM0 : NS	0x50021000 0x40021000	US	NS	SA	No	Pulse width modulation unit 0
PWM1 : S PWM1 : NS	0x50022000 0x40022000	US	NS	SA	No	Pulse width modulation unit 1
PWM2 : S PWM2 : NS	0x50023000 0x40023000	US	NS	SA	No	Pulse width modulation unit 2
PWM3 : S PWM3 : NS	0x50024000 0x40024000	US	NS	SA	No	Pulse width modulation unit 3

Register overview

Register	Offset	TZ	Description
TASKS_STOP	0x004		Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback
TASKS_SEQSTART[n]	0x008		Loads the first PWM value on all enabled channels from sequence n, and starts playing that sequence at the rate defined in SEQ[n]REFRESH and/or DECODER.MODE. Causes PWM generation to start if not running.
TASKS_NEXTSTEP	0x010		Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running.
SUBSCRIBE_STOP	0x084		Subscribe configuration for task STOP
SUBSCRIBE_SEQSTART[n]	0x088		Subscribe configuration for task SEQSTART[n]
SUBSCRIBE_NEXTSTEP	0x090		Subscribe configuration for task NEXTSTEP
EVENTS_STOPPED	0x104		Response to STOP task, emitted when PWM pulses are no longer generated
EVENTS_SEQSTARTED[n]	0x108		First PWM period started on sequence n
EVENTS_SEQEND[n]	0x110		Emitted at end of every sequence n, when last value from RAM has been applied to wave counter
EVENTS_PWMPERIODEND	0x118		Emitted at the end of each PWM period
EVENTS_LOOPSDONE	0x11C		Concatenated sequences have been played the amount of times defined in LOOP.CNT
PUBLISH_STOPPED	0x184		Publish configuration for event STOPPED
PUBLISH_SEQSTARTED[n]	0x188		Publish configuration for event SEQSTARTED[n]
PUBLISH_SEQEND[n]	0x190		Publish configuration for event SEQEND[n]
PUBLISH_PWMPERIODEND	0x198		Publish configuration for event PWMPERIODEND
PUBLISH_LOOPSDONE	0x19C		Publish configuration for event LOOPSDONE
SHORTS	0x200		Shortcuts between local events and tasks
INTEN	0x300		Enable or disable interrupt
INTENSET	0x304		Enable interrupt
INTENCLR	0x308		Disable interrupt
ENABLE	0x500		PWM module enable register
MODE	0x504		Selects operating mode of the wave counter
COUNTERTOP	0x508		Value up to which the pulse generator counter counts
PRESCALER	0x50C		Configuration for PWM_CLK
DECODER	0x510		Configuration of the decoder
LOOP	0x514		Number of playbacks of a loop
SEQ[n].PTR	0x520		Beginning address in RAM of this sequence
SEQ[n].CNT	0x524		Number of values (duty cycles) in this sequence
SEQ[n].REFRESH	0x528		Number of additional PWM periods between samples loaded into compare register
SEQ[n].ENDDELAY	0x52C		Time added after the sequence
PSEL.OUT[n]	0x560		Output pin select for PWM channel n

6.10.5.1 TASKS_STOP

Address offset: 0x004

Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_STOP			Stops PWM pulse generation on all channels at the end of current PWM period, and stops sequence playback
			Trigger	1	Trigger task

6.10.5.2 TASKS_SEQSTART[n] (n=0..1)

Address offset: 0x008 + (n × 0x4)

Loads the first PWM value on all enabled channels from sequence n, and starts playing that sequence at the rate defined in SEQ[n]REFRESH and/or DECODER.MODE. Causes PWM generation to start if not running.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_SEQSTART			Loads the first PWM value on all enabled channels from sequence n, and starts playing that sequence at the rate defined in SEQ[n]REFRESH and/or DECODER.MODE. Causes PWM generation to start if not running.
			Trigger	1	Trigger task

6.10.5.3 TASKS_NEXTSTEP

Address offset: 0x010

Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																																A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	W	TASKS_NEXTSTEP			Steps by one value in the current sequence on all enabled channels if DECODER.MODE=NextStep. Does not cause PWM generation to start if not running.
			Trigger	1	Trigger task

6.10.5.4 SUBSCRIBE_STOP

Address offset: 0x084

Subscribe configuration for task STOP

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID									B																A	A	A	A	A	A	A	A
Reset 0x00000000	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

ID	R/W	Field	Value ID	Value	Description
A	RW	CHIDX		[0..255]	DPPI channel that task STOP will subscribe to
B	RW	EN			
			Disabled	0	Disable subscription
			Enabled	1	Enable subscription

6.10.5.5 SUBSCRIBE_SEQSTART[n] (n=0..1)

Address offset: 0x088 + (n × 0x4)

Subscribe configuration for task SEQSTART[n]