

Lierda DB35

Module hardware design manual

Version: Rev03

Date: 25/9/4

Status: controlled version

legal notice

By receiving this document from Lierda Technology Group Co., LTD. (hereinafter referred to as "Lierda"), you agree to the following terms and conditions. If you do not agree to the following terms and conditions, please stop using this document.

The copyright of this document belongs to Lierda Technology Group Co., Ltd. All rights reserved, including those not expressly granted herein. This document contains proprietary information related to Lierda. Without prior written consent from Lierda, no entity or individual may reproduce, transmit, distribute, use, or disclose this document, including any images, tables, data, or other information contained within it.

This product complies with the design requirements of environmental protection and personal safety. The storage, use and disposal of the product shall comply with the requirements of the product manual, relevant contracts or relevant laws and regulations.

The Company reserves the right to modify and improve the products described in this manual without prior notice; and reserves the right to revise or withdraw this manual at any time.

History of document revisions

Document version	Date of change	Revisers	auditor	changed content
Rev01	25-07-28	CF	LXY	Initial version
Rev02	25-09-04	CF	LXY	Modulation system modification
Rev03	25-09-19	CF	LXY	Update ESD protection

Lierda
利 尔 达

safety instruction

Users are responsible for complying with national regulations governing wireless communication modules and equipment, as well as specific environmental requirements. By following these security principles, we can safeguard personal safety and protect products and work environments from potential harm. Our company will not be responsible for any losses incurred due to customers' non-compliance with these regulations.



Road safety first! When you are driving, do not use a handheld mobile terminal device unless it has a hands-free function. Please stop and make a phone call!



Please turn off your mobile device before boarding. The wireless function of your mobile device is prohibited on the plane to prevent interference with the aircraft's communication system. Ignoring this warning may lead to flight safety and even legal violations.



When in a hospital or health care facility, be aware of restrictions on the use of mobile devices. RF interference can cause medical equipment to malfunction, so mobile devices may need to be turned off.



Mobile devices cannot guarantee a stable connection under all circumstances, such as when your SIM card is invalid or your phone has no credit. In emergency situations where these issues occur, remember to use the emergency call feature while keeping your device powered on and in an area with sufficient signal strength.



Your mobile terminal device receives and transmits radio frequency signals when it is turned on. Radio frequency interference occurs when it is near a TV, radio, computer or other electronic devices.



Keep your mobile device away from flammable gas. When you are near a gas station, oil depot, chemical plant or explosion site, turn off your mobile device. There are safety risks when operating electronic devices in any potentially explosive places.

Applicable module

- 1、product name: DB35 Wi-Fi &BLE Module
- 2、Model name: DB35
- 3、Serial model name: L-NLEDB35-G5NN4-E1、 L-NLEDB35-G5NN4-E4
- 4、operating temperature: -40~85° C
- 5、reference:

Radio Waves specs		
Radio	Frequency/MHz	Max. Output Power/dBm
Bluetooth	2402-2480	8.6
2.4G WiFi	2400-2483.5	17.5

- 6、Declaration of Conformity:

Hereby, Lierda declares that the radio equipment type DB35 is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following internet address:

- 7、RF exposure statement:

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of d=20 cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

8、FCC MODULAR APPROVAL INFORMATION EXAMPLES for Manual:

1.This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

2.This device may not cause harmful interference.

3.This device must accept any interference received, including interference that may cause undesired operation.

4.CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

5.NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- ①Reorient or relocate the receiving antenna.
- ②Increase the separation between the equipment and receiver.
- ③Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- ④Consult the dealer or an experienced radio/TV technician for help.

Requirement per KDB996369 D03**1.1 List of applicable FCC rules**

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.³

Explanation: This module meets the requirements of FCC part 15C(15.247). part 15E(15.407)

1.2 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users, then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

Explanation: The EUT has a Chip Antenna, and the antenna use a permanently attached antenna which is not replaceable.

1.3 Limited module procedures

If a modular transmitter is approved as a "limited module," then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval. This limited module procedure is also applicable for RF exposure evaluation when it is necessary to demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

Explanation: The module is not a limited module.

1.4 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects:

layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

- a) Information that includes permitted variances (e.g., trace boundary limits, thickness, length, width, shape(s), dielectric constant, and impedance as applicable for each type of antenna);
- b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency, the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered);
- c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;
- d) Appropriate parts by manufacturer and specifications;
- e) Test procedures for design verification; and
- f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

Explanation: Yes, The module with trace antenna designs, and This manual has been shown the layout of trace design, antenna, connectors, and isolation requirements.

1.5 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information: (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person's body); and (2) additional text needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

Explanation: This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is:2AOFDL-DB35.

OEM Integrators - End Product Labeling Considerations: This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following:

“Contains, FCC ID: 2AOFDL-DB35” . The grantee's FCC ID can be used only when all FCC

compliance requirements are met.

OEM Integrators - End Product Manual Provided to the End User: The OEM integrator shall not provide information to the end user regarding how to install or remove this RF module in end product user manual. The end user manual must include all required regulatory information and warnings as outlined in this document.



catalogue

legal notice	1
History of document revisions	2
safety instruction	3
Applicable module	4
catalogue	9
1 foreword	12
2 Product overview	13
2.1 Key features	13
2.2 product superiority	13
2.3 Application Scenarios	14
2.4 Functional Block Diagram	14
2.5 Pin description	15
2.6 Key hardware words for power supply	18
2.7 Pin multiplexing instructions	19
3 Performance Characteristics	21
3.1 Power Supply Design	21
3.1.1 VDDIO design	21
3.1.2 VBAT_IN design	21
3.2 Reset design	22
3.2.1 Transistor reset reference circuit	22
3.2.2 Key reset reference circuit	23
3.3 Power sequencing	23
4 Application interface	26
4.1 SDIO joggle	26
4.1.1 Single-line SDIO mode	26

4.1.2 Single-line SDIO circuit reference design	27
4.1.3 Four-line SDIO mode	29
4.1.4 Fourth-line SDIO circuit reference design	30
4.2 UART joggle	32
4.3 PWM interface reference design	33
4.4 I2S interface reference design	34
4.5 I2C interface reference design	34
4.6 ADC reference design	35
4.7 SPI interface reference design	36
4.8 PATA interface reference design	37
4.9 Ultra-low power interface reference design	39
4.10 Antenna selection interface	40
5 Radio frequency characteristics	41
5.1 radio frequency interface	41
5.2 Wi-Fi function	41
5.3 BLE function	42
5.4 Reference design of RF link	43
5.5 Antenna selection reference	45
5.6 Plate layout notes	46
6 Electrical performance and reliability	48
6.1 Rated power supply	48
6.2 DC electrical characteristics	48
6.3 power dissipation	50
6.4 electrostatic protection	50
6.5 Working and storage temperature	51
7 Mechanical dimensions	52
7.1 Mechanical dimensions	52

7.2 Recommended packaging	52
8 Production and packaging information	53
8.1 packing specifications	53
8.1.1 manner of packing	53
8.1.2 Strap size and product direction	53
8.2 storage condition	54
8.3 Production welding	55
8.3.1 Furnace type	55
8.3.2 Module position requirements on the base plate	55
8.3.3 Steel mesh opening design	55
8.3.4 Production Notes	56
8.3.5 Reflow soldering operation instructions	56
8.3.6 keep in repair	57
9 Related documents and abbreviations of terms	58

Lierda
利 尔 达

1 foreword

The DB35 is a triple-mode wireless communication module integrating Wi-Fi, Bluetooth LE, It supports IEEE 802.11b/g/ n/ax(2.4G frequency bands and BLE5.3 standard protocols through an SDIO 2.0 interface. With dual-band support (802.11n 20MHz/40MHz and 802.11ax 20MHz) and extended coverage, this module delivers maximum physical layer speeds of 150Mbps while maintaining long-range connectivity. Its versatile applications span Industrial Network Communication (IPC), surveillance pan-tilt units, smart home systems, security devices, dashcams, and intelligent access control solutions.

remarks

(1) DB35 module:

The DB35 supports four-wire SDIO mode and has no built-in RTC crystal. The module is usually pre-programmed with Lirda factory firmware at the time of delivery. When users reprogram other firmware, be careful not to erase the entire FLASH.

2 Product overview

2.1 Key features

Table 2-1 Key module features

joggle	Postage stamp hole
Wireless standards	IEEE 802.11b/g/n/ax+BLE5.3
Module size	12mm × 12mm × 2.5mm
working voltage	3.16V~3.465V, typical value 3.3V
Working frequency band	2400~2483.5MHz (2.4GHz ISM Band)
Working temperature (2)	-40 ~ +85°C
Storage temperature	-40 ~ +105°C
communication interface	SDIO 2.0 UART0: Debug/AT port UART1: User-defined serial port can be used as AT serial port UART2: User Customized Serial Port
tape width	Support IEEE 802.11n:20MHz/40MHz bandwidth Support IEEE 802.11ax: 20MHz bandwidth
MAC	IEEE 802.11d/e/i/k/v/w

remarks

(2) To ensure compliance with the operational temperature specifications, heat dissipation enhancements such as active or passive heat sinks and equalizing plates are essential. Within this operational temperature range, the module's performance metrics align with the established standards of IEEE 802.11, including the latest advancements in data rates and interoperability, as well as the BLE5.3 standard.

2.2 product superiority

- 1) Support IEEE 802.11b/g/n/ax @ 20M/40M 2.4GHz
- 2) Supports BLE 5.3 @ 1M/2M Supports BLE 5.3 @ 1M/2M

- 3) Supports STA, AP, and Wi-Fi Direct modes
- 4) Supports WEP/WPA/WPA2/WPA3-SAE Personal, MFP frequency band
- 5) Support Wi-Fi and BLE time-division multiplexing
- 6) Support SDIO 2.0 interface
- 7) Supports OFDMA

2.3 Application Scenarios

- Low power IPC, monitoring PTZ
- Smart home, security equipment
- tachograph
- Smart access control

2.4 Functional Block Diagram

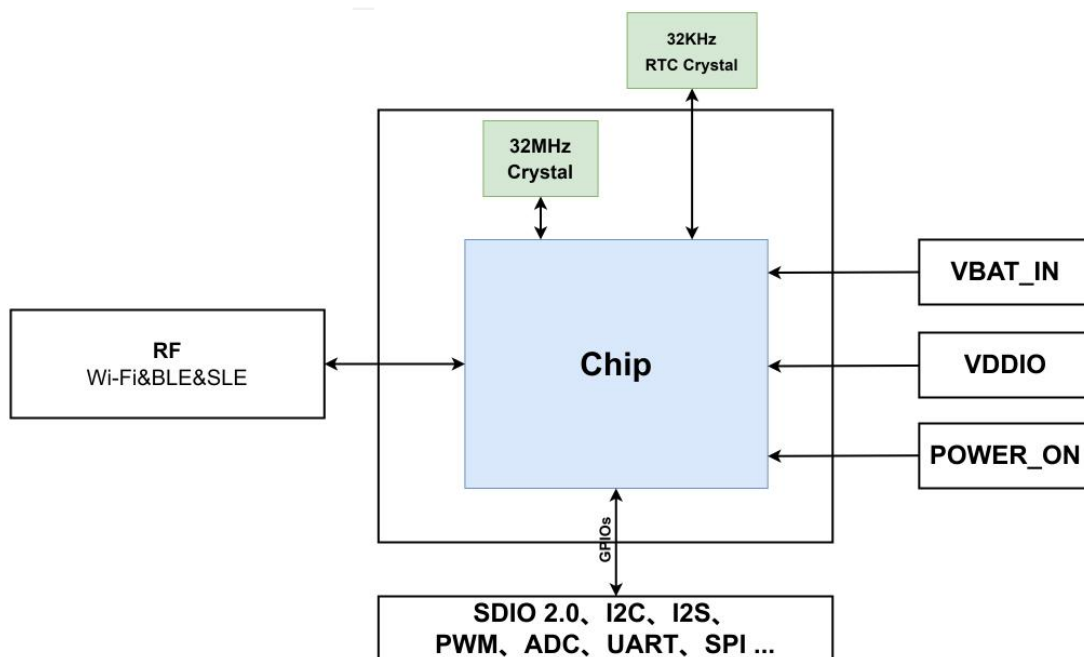


Figure 2.1DB35 module functional block diagram

2.5 Pin description

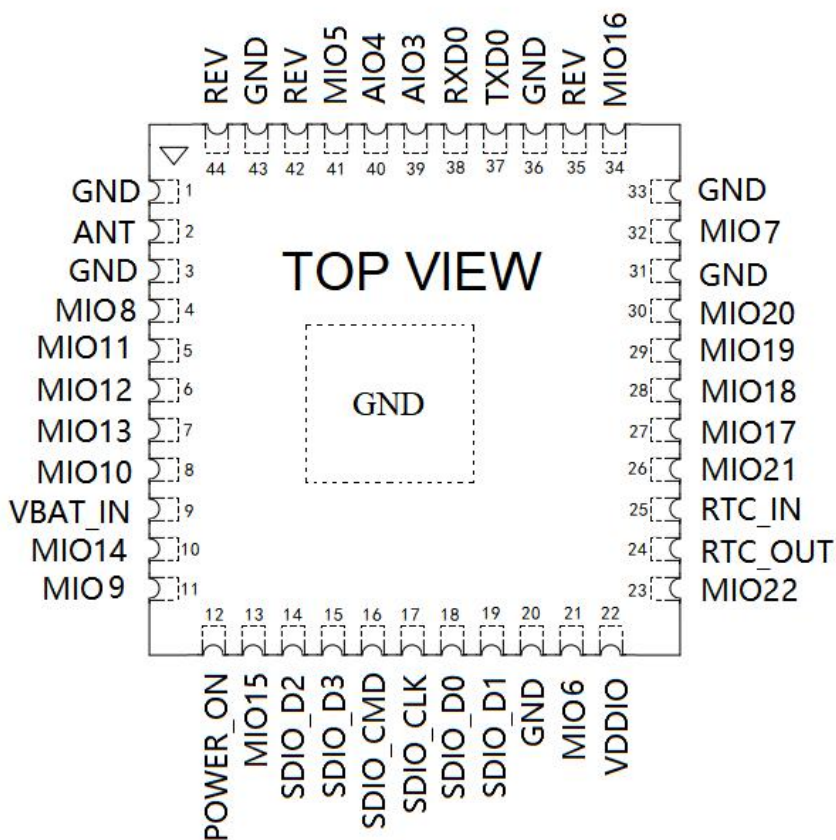


Figure 2.2DB35 module pin distribution diagram

Table 2-2 DB35 module pin function description

pin	Pin definitions	I/O type	Typical voltage values	functional description
1	GND	G	–	the earth
2	ANT	RF	–	2.4G Wi-Fi & BT RF interface
3	GND	G	–	the earth
4	MIO8	I/O	VIO	General IO corresponds to the MGPIO8 of IC
5	MIO11	I/O	VIO	General IO corresponds to the MGPIO11 of IC
6	MIO12	I/O	VIO	General IO corresponds to the MGPIO12 of IC
7	MIO13	I/O	VIO	General IO corresponds to the MGPIO13 of IC
8	MIO10	I/O	VIO	General IO corresponds to the MGPIO10 of IC
9	VBAT_IN	P	3.3V	main power source
10	MIO14	I/O	VIO	General IO corresponds to the MGPIO14 of IC
11	MIO9	I/O	VIO	General IO corresponds to the MGPIO9 of IC
12	POWER_ON	I	VIO	Enable pin, high level enable, low level shutdown (already pulled up to VDDIO internally)
13	MIO15	I/O	VIO	General IO corresponds to the MGPIO15 of IC
14	SDIO_D2	I/O	VIO	SDIO data line D0, corresponding to IC's MGPIO0
15	SDIO_D3	I/O	VIO	SDIO data line D1, corresponding to IC's MGPIO1
16	SDIO_CMD	I/O	IO	SDIO command/response corresponds to the MGPIO2 of the IC
17	SDIO_CLK	I/O	VIO	SDIO clock signal, corresponding to IC's MGPIO3
18	SDIO_D0	I/O	VIO	SDIO data line D0 corresponds to the MGPIO4 of the IC
19	SDIO_D1	I/O	VIO	SDIO data line D1, corresponding to IC's AGPIO5
20	GND	G	–	the earth

pin	Pin definitions	I/O type	Typical voltage values	functional description
21	MIO6	I/O	VIO	General IO corresponds to the MGPIO6 of the IC
22	VDDIO	P	1.8/3.3V	IO source
23	MIO22	I/O	VIO	General IO, corresponding to IC's MGPIO22
24	RTC_OUT	I/O	VIO	RTC reserved, suspended treatment
25	RTC_IN	I/O	VIO	RTC reserved, suspended treatment
26	MIO21	I/O	VIO	General IO, corresponding to IC's MGPIO21
27	MIO17	I/O	VIO	General IO corresponds to the MGPIO17 of IC
28	MIO18	I/O	VIO	General IO corresponds to the MGPIO18 of IC
29	MIO19	I/O	VIO	General IO corresponds to MGPIO19 of IC
30	MIO20	I/O	VIO	General IO corresponds to the MGPIO20 of IC
31	GND	G	–	the earth
32	MIO7	I/O	VIO	General IO corresponds to the MGPIO7 of IC
33	GND	G	–	the earth
34	MIO16	I/O	VIO	General IO corresponds to the MGPIO16 of IC
35	REV	REV	–	Undefined reserved pins, left floating
36	GND	G	–	the earth
37	TXD0	O	VIO	UART0 serial port, TXD data transmission, corresponding to the IC's AGPIO1
38	RXD0	I	VIO	UART0 serial port, RXD data reception, corresponding to IC AGPIO2
39	AIO3	I/O	VIO	General IO, corresponding to IC's AGPIO3
40	AIO4	I/O	VIO	General IO, corresponding to IC's AGPIO4
41	MIO5	I/O	VIO	General IO corresponds to the MGPIO5 of IC

pin	Pin definitions	I/O type	Typical voltage values	functional description
42	REV	REV	–	Undefined reserved pins, left floating
43	GND	G	–	the earth
44	REV	REV	–	Undefined reserved pins, left floating

remarks

"P": POWER "I": INPUT "O": OUTPUT "G": GND "REV": RESERVE

2.6 Key hardware words for power supply

The normal startup of the module must have the correct hardware configuration word when powered on, which is strongly related to the chip hardware startup. Its level state must be shown in Table 2-3.

Table 2-3 DB35 module pin hardware configuration word description

pin	Pin name	low level	high level
10	MIO14	Normal startup	forbidden
13	MIO15	Normal startup	forbidden

2.7 Pin multiplexing instructions

Table 2-4 DB35 module (four-wire SDIO mode) pin multiplexing description

Pin numbers	GPIO	SDIO	UART_H0 (UART2)	UART_H1 (UART1)	UART_L0 (UART0)	SPI0	QSPI	I2C1	I2C0	ADC	PWM	I2S	PTA Bundling of traffic arbitration	ANT_SE Smart antenna selection	low power consumption Input wake-up	low power consumption output
4	MIO8		UART_H0_TXD			SPI0_CLK		I2C1_SCL		ADC_CH5						
5	MIO11			UART_H1_RTS		SPI0_CLK					PWM0_N	I2S_BCLK			support	
6	MIO12			UART_H1_TXD		SPI0_DI						I2S_DI		ANT_SEL4		
7	MIO13			UART_H1_RXD		SPI0_DO			I2C0_SCL			I2S_DO				
8	MIO10			UART_H1_CTS		SPI0_CS0					PWM0_P	I2S_WS		ANT_SEL3		
10	MIO14		UART_H0_CTS						I2C0_SDA		SPWM1_N		BT_ACTIVE			
11	MIO9		UART_H0_RXD			SPI0_DO		I2C1_SDA		ADC_CH6						
13	MIO15			UART_H1_RTS							SPWM1_P		BT_STATUS			
14	MIO0	SDIO_D2														
15	MIO1	SDIO_D3														
16	MIO2	SDIO_CMD				SPI0_DI										
17	MIO3	SDIO_CLK				SPI0_CLK										
18	MIO4	SDIO_D0				SPI0_DO										
19	AIO5	SDIO_D1				SPI0_CS0									support	support
21	MIO6		UART_H0_RTS			SPI0_DI				ADC_CH7					support	
23	MIO22			UART_H1_CTS					I2C0_SDA	ADC_CH4	PWM3_P		WLAN_ACTIVE	ANT_SEL5		
26	MIO21		UART_H0_RTS						I2C0_SCL		PWM0_P		BT_STATUS			
27	MIO17		UART_H0_TXD				QSPI1_CLK					I2S_BCLK	BT_ACTIVE			
28	MIO18		UART_H0_RXD				QSPI1_D0					I2S_DO	BT_STATUS			
29	MIO19						QSPI1_D1				PWM2_P	I2S_DI	BT_FREQ			
30	MIO20						QSPI1_CS				PWM2_N	I2S_WS	WLAN_ACTIVE			
32	MIO7		UART_H0_CTS			SPI0_CS0	QSPI1_D2							ANT_SEL2	support	
34	MIO16						QSPI1_D3				PWM3_N				support	
37	TXD0				UART_L0_TXD					ADC_CH0					support	support

Pin numbers	GPIO	SDIO	UART_H0 (UART2)	UART_H1 (UART1)	UART_L0 (UART0)	SPI0	QSPI	I2C1	I2C0	ADC	PWM	I2S	PTA Bundling of traffic arbitration	ANT_SE Smart antenna selection	low power consumption Input wake-up	low power consumption output
	(AGPIO1)															
38	RXD0 (AGPIO2)				UART_L0_RXD						PWM0_P				support	support
39	AIO3							I2C1_SCL		ADC_CH1	PWM0_N				support	support
40	AIO4			UART_H1_RXD				I2C1_SDA		ADC_CH2					support	support
41	MIO5			UART_H1_TXD												

remarks

- (1) The DB35 module supports the four-wire SDIO mode. If the user intends to reuse the single-wire SDIO mode, it is essential to keep SDIO_D2 (at pin 14) and SDIO_D3 (at pin 15) of the module suspended, i.e., disable these two IOs.

(2) When utilizing MIO16 as the input wake-up function, it is recommended to maintain the default state as high and use a low level or falling edge for wake-up.

3 Performance Characteristics

3.1 Power Supply Design

The DB35 module has two power supply pins VBAT_IN and VDDIO, whose pin definitions are as follows:

Table 3-1 Power pin definitions

Pin number	Pin definitions	description	least value V	representative value V	crest value V
9	VBAT_IN	Module power	3.16	3.3	3.465
22	VDDIO	IO electrical level	1.71	1.8/3.3	3.465

3.1.1 VDDIO design

VDDIO is the power supply pin for the module GPIO. For the convenience of design, VDDIO can be directly connected with the main power supply VBAT_IN to realize the synchronization of power on and off between the main power supply and VDDIO.

The VDDIO can be powered by external DCDC or LDO (VBAT_IN and VDDIO have no power-up sequence requirements). The required supply current capacity should exceed 300mA. A 1 μ F decoupling capacitor should be placed adjacent to the pin on the trace line. It should be noted that when the DB35 module communicates with other host devices via SDIO (or other interface types such as UART), both modules must maintain identical VDDIO levels. If there is a difference in VDDIO levels, a voltage conversion circuit must be incorporated during device communication to prevent module or host burn-in.

3.1.2 VBAT_IN design

VBAT_IN serves as the power supply input for the entire module. The quality of this power supply directly impacts the module's performance. When designing, if the VDDIO is directly connected to the main power supply VBAT_IN, the external power must provide at least 1000mA

current capacity. This ensures the VBAT_IN voltage for the DB35 module remains above the minimum operating voltage, preventing voltage drop-induced malfunctions in the module.

When the voltage difference between the input and module supply is minimal, an LDO should be selected as the power source. For significant voltage differentials between input and output, a DC-DC converter is recommended, while also considering the EMI issues associated with DC-DC conversion. To ensure optimal power performance, the VBAT_IN input reference circuit is designed as follows:

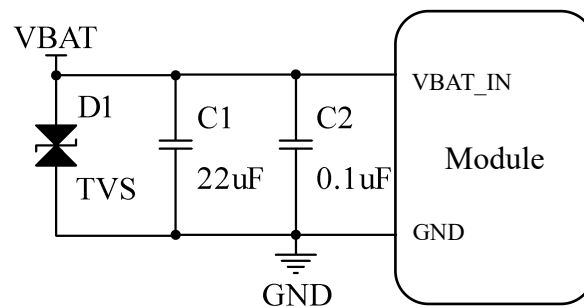


Figure 3.1 Recommended power supply design

In PCB design, the width of power line should not be less than 0.7mm. The GND plane of power part should be as complete as possible and more ground holes should be drilled. Meanwhile, the capacitor should be placed as close as possible to the VBAT_IN pin of the module.

- D1 is a TVS tube, which can improve the electrostatic protection capability of the module
- C1 is a 22uF ceramic capacitor that improves the module's ability to suppress surges, and C2 is a 0.1uF decoupling capacitor

3.2 Reset design

The POWER_ON pin of the module is the reset pin of the module (the internal pull-up to VDDIO). Users can directly connect it to the host for power on and off control. Under normal circumstances, the startup time of the host can meet the reset timing requirements of the module. For details, refer to 3.3 Power and Reset Timing.

3.2.1 Transistor reset reference circuit

The transistor reset circuit is illustrated in Figure 3.2. During layout design, ensure reset traces

are kept short and properly shielded from RF interference, power supply lines, and strong electromagnetic sources. Place transistors as close as possible to the module's POWER_ON pin to minimize external signal interference. It is recommended to reserve a 100nF-1 μ F capacitor near the module's PWOER_ON pin, which should remain unmounted by default.

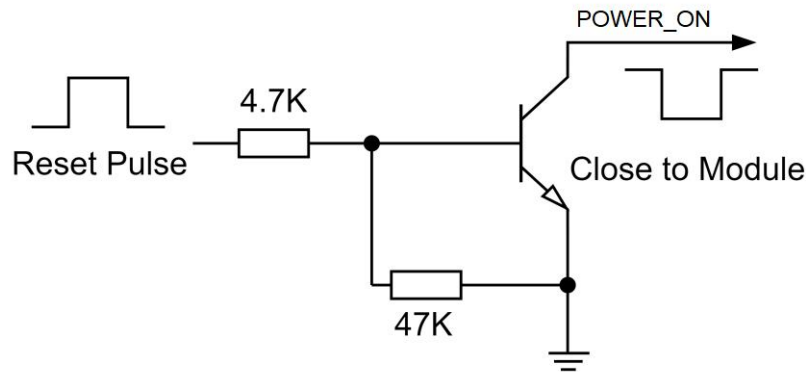


Figure 3.2 Transistor reset reference circuit

3.2.2 Key reset reference circuit

The button reset reference circuit is shown in Figure 3.3. In order to prevent the key from being affected by ESD, it is usually recommended to place a TVS near the key. A capacitor of 100nF~1 μ F can also be reserved near the POWER_ON pin of the module. It is not installed by default.

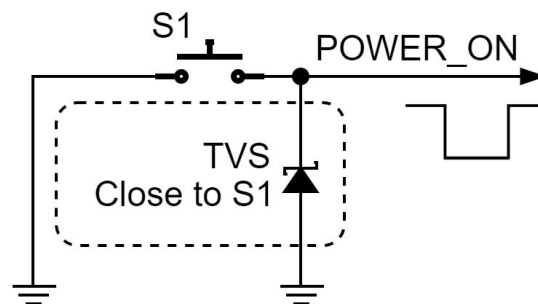


Figure 3.3 Key reset reference circuit

3.3 Power sequencing

The following figure shows the power-on timing diagram of DB35 module *.

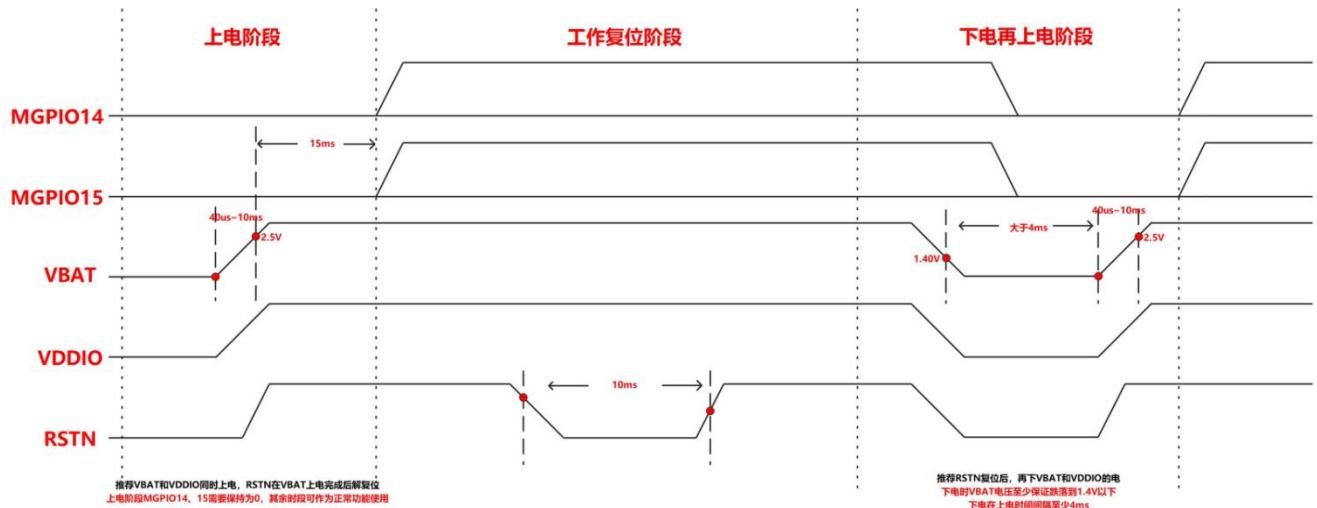


Figure 3.4 Power on/off and reset timing diagram

The sequence of power up is as follows:

- (1) The external power supply VBAT and IO power supply VDDIO are in the power-off state, and the module is in the power-off state.
- (2) External power supplies VBAT and VDDIO should be powered on simultaneously, as recommended. In this scenario, VBAT may experience a slow power-on sequence, and it is crucial to ensure that VBAT stabilizes for a minimum of 2.6 ms to avoid potential device malfunction or damage, as per the LPC55S1x specifications.
- (3) After VBAT and VDDIO are powered on for about 20ms, CLDO is powered on and stabilized, and CRG reset begins.
- (4) There is no POWER_ON signal on the power supply system of the main chip. The POR module mainly performs detection on VBAT and internal power supply. When both are in place, the chip will issue the internal reset signal.
- (5) VBAT power threshold: 2.5V;
- (6) VBAT power down threshold: 1.4V.
- (7) There is no POWER_ON signal on the power supply system of the main chip, and there is POWER_ON outside the module to reset the whole chip. Its status is maintained by the board circuit.

(8) Upon detection of an under-voltage condition or removal of VBAT, the Power On Reset (POR) circuitry initiates a system-wide reset to ensure a safe shutdown of the chip.

remarks

- 1) When the chip loses power, ensure that VDDIO and VBAT levels are below 200mV.
- 2) The board reset is achieved by pulling the POWER_ON (RSTN) pin of module 12 low initially, followed by a high state. To ensure a proper reset, the POWER_ON (RSTN) pin must be held low for a duration exceeding 10 milliseconds.

Lierda
利 尔 达

4 Application interface

4.1 SDIO joggle

The SDIO interface facilitates command and data transfer between the host controller (HOST) and peripheral devices. The DB35 module supports both single-line and four-line SDIO configurations. SDIO operates at 1.8V or 3.3V voltage levels, requiring the host to maintain either 1.8V or 3.3V output. When not meeting this requirement, a voltage converter must be integrated between them. The selected converter chip must comply with the SDIO's 50MHz transmission rate specifications.

4.1.1 Single-line SDIO mode

The DB35 module's SDIO single-line mode is categorized into two types based on the interrupt mode: GPIO interrupt mode and SDIO interrupt mode, as follows:

- (1) Mode 1 (GPIO interrupt mode): This mode requires four module pins: SDIO_CLK, SDIO_CMD, SDIO_D0, and MIO13 (used as the interrupt pin).
- (2) Mode 2: The SDIO interrupt mode requires four module PIN pins, namely SDIO_CLK, SDIO_CMD, SDIO_D0 and SDIO_D1, among which SDIO_D1 is used as the interrupt.

Other control signals and low power applications are shown in the figure and Table 4-1 below.

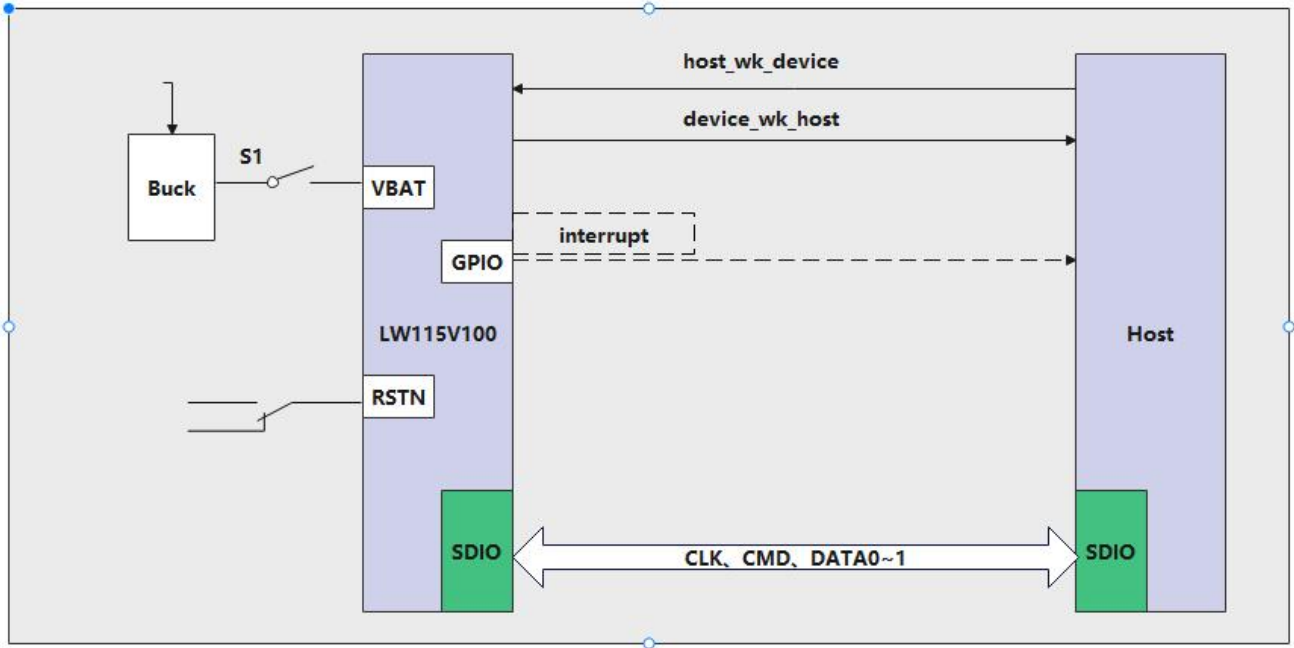


Figure 4.1 Reference block diagram of low power application system connection in single-line SDIO mode

Table 4-1 Control signal and low power application reference design suggestions

name	Design recommendations
VBAT_IN	The main power supply of the module is usually powered by a board-level BUCK or LDO
POWER_ON	The module reset pin is pulled up to VDDIO by default and controlled by the board circuit
HOST_WK_DEVICE	Directly connected to the HOST chip, used for HOST to wake up the DB35 module. Must be connected to the module's GPIO that supports low-power wake up
DEVICE_WK_HOST	Directly connected to the HOST chip for DB35 module wake up of the HOST
SDIO INTERRUPT	SDIO interrupt signal. SDIO_D1 can be used as the interrupt signal, or other GPIOs (e.g., MIO13) can be used instead.

4.1.2 Single-line SDIO circuit reference design

The reference design for a single-line SDIO interface (using MIO13 as an example of an SDIO interrupt) is as follows:

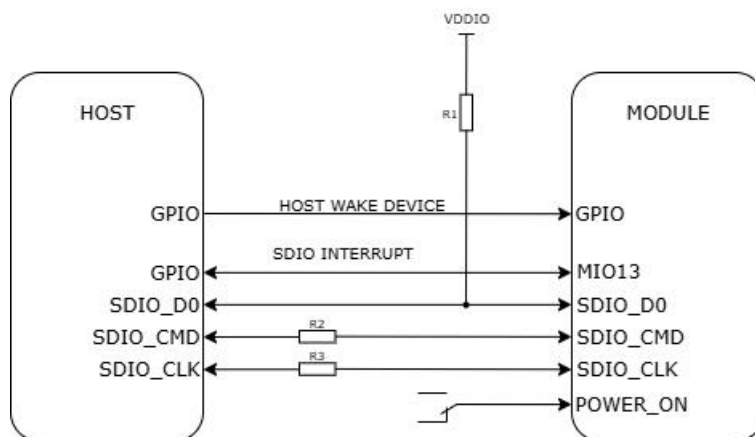


Figure 4.2 Reference design for low power applications in single-line SDIO mode

Lierda
利 尔 达

Table 4-2 Single-line SDIO mode pin definition

Pin number	Pin definitions	description	remarks
16	SDIO_CMD	SDIO command/response	(1) The typical value of the pin support level is 3.3/1.8V (2) PCB design if using two layers, it is recommended to connect 50 Ω resistor; if using four layers, it is recommended to connect 33 Ω resistor
17	SDIO_CLK	SDIO clock signal	
18	SDIO_D0	SDIO data line 0	
7	MIO13	SDIO suspend	(3) The series resistors for clock signals are placed near the source; the series resistors for command/response and data signals are placed near the terminal (4) SDIO wiring length ≤ 5 inch (5) When designing a data line pin, it is recommended to reserve a pull-up resistor. One end of the resistor is directly connected to the signal line and the other end is connected to VDDIO

remarks

(1) The DB35 module only supports four-wire SDIO mode. If the user wants to reuse it as a single-wire SDIO mode, the SDIO_D2 and SDIO_D3 pins of the module must be left empty, that is, these two IOs are disabled.

4.1.3 Four-line SDIO mode

The SDIO four-line mode of DB35 module is divided into two types according to the interrupt mode: one is the GPIO interrupt mode, and the other is the SDIO interrupt mode.

(1) Method 1: The GPIO interrupt mode requires 7 module PIN pins, which are SDIO_CLK, SDIO_CMD, SDIO_D0, SDIO_D1, SDIO_D2, SDIO_D3 and MIO13, among which, MIO13 is used as the interrupt.

(2) Method 2: SDIO interrupt mode requires 6 module PIN pins, which are SDIO_CLK, SDIO_CMD, SDIO_D0, SDIO_D1, SDIO_D2, SDIO_D3, among which SDIO_D1 is used as the interrupt.

Other control signals and low power applications are shown in the figure and Table 4-3 below.

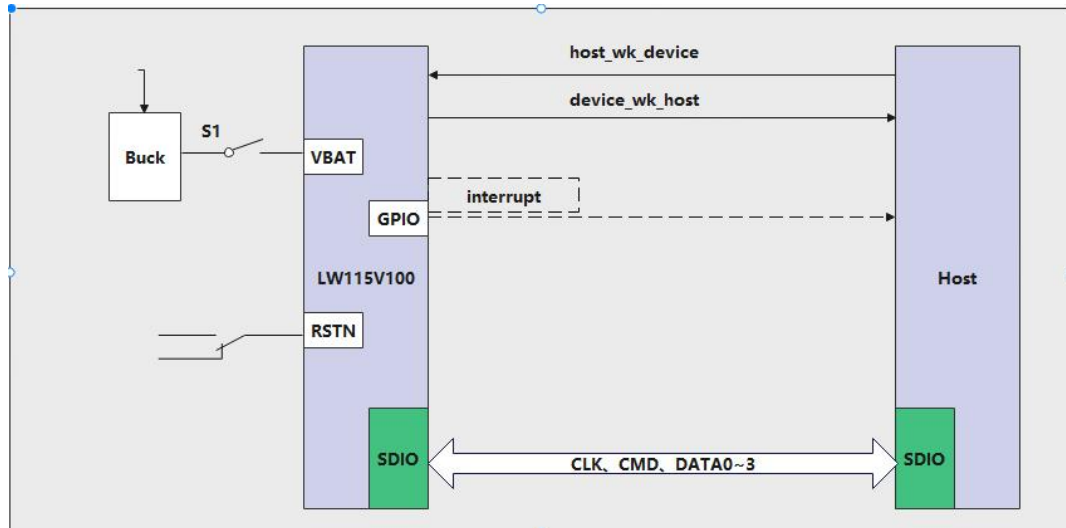


Figure 4.3 Four-line SDIO mode low-power application system connection reference block diagram

Table 4-3 Control signals and low power application reference design suggestions

name	Design recommendations
VBAT_IN	The main power supply of the module is usually powered by a board-level BUCK or LDO
POWER_ON	The module reset pin is internally pulled up to VDDIO and controlled by the board circuit
HOST_WK_DEVICE	Directly connected to the HOST chip, used for HOST to wake up the DB35 module. Must be connected to the module's GPIO that supports low-power wake up
DEVICE_WK_HOST	Directly connected to the HOST chip for DB35 module wake up of the HOST
SDIO INTERRUPT	SDIO interrupt signal. SDIO_D1 can be used as the interrupt signal, or other GPIOs (e.g., MIO13) can be used instead.

4.1.4 Fourth-line SDIO circuit reference design

The reference design for a single-line SDIO interface (using MIO13 as an example of an SDIO interrupt) is as follows:

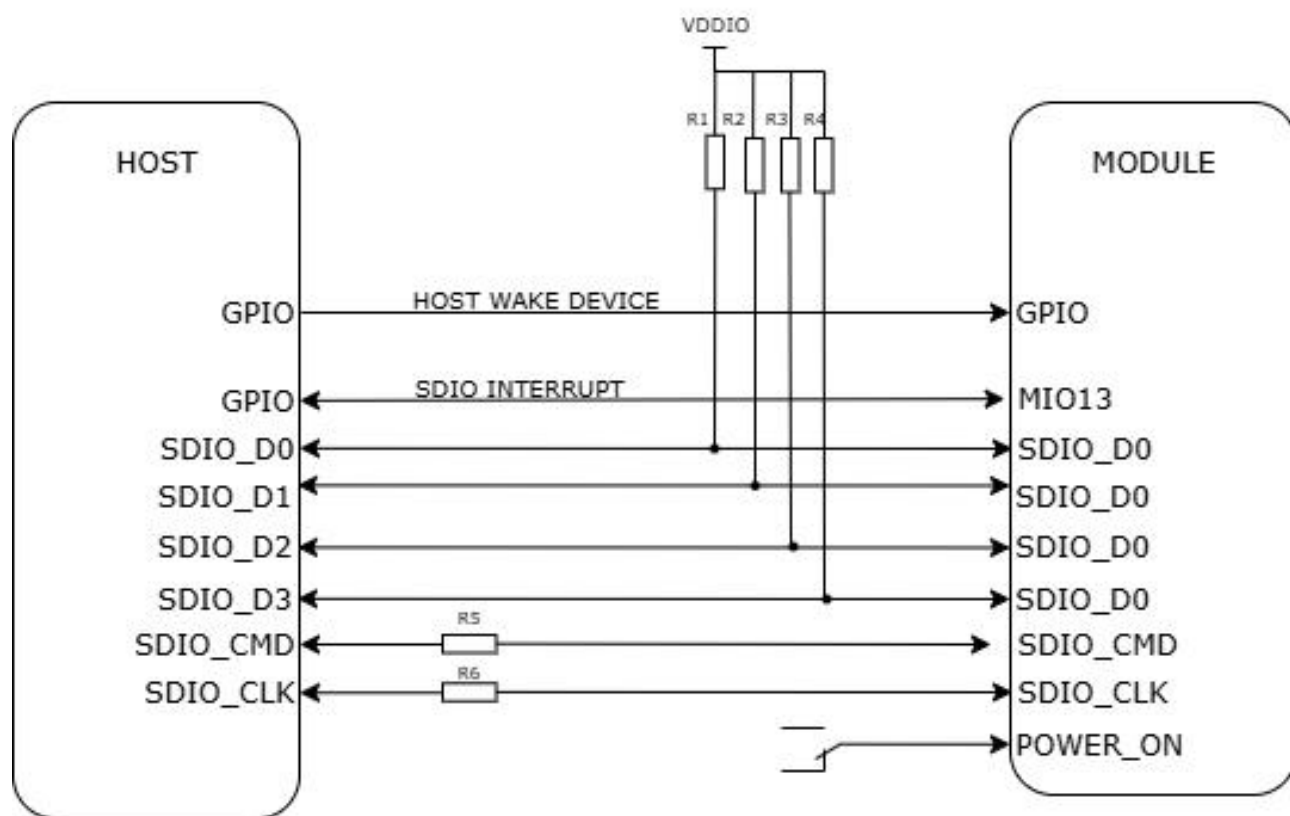


Figure 4.4 SDIO 4.0 low power application reference design for four-line mode

Table 4-4 Four-line SDIO mode pin definition

Pin number	Pin definitions	description	remarks
16	SDIO_CMD	SDIO command/response	(1) The typical value of the pin support level is 3.3/1.8V (2) PCB design if using two layers, it is recommended to connect 50 Ω resistor; if using four layers, it is recommended to connect 33 Ω resistor (3) The series resistors for clock signals are placed near the source; the series resistors for command/response and data signals are placed near the terminal (4) SDIO wiring length ≤ 5 inch (5) When designing a data line pin, it is recommended to reserve a pull-up resistor. One end of the resistor is directly connected to the signal line and the other end is connected to VDDIO
17	SDIO_CLK	SDIO clock signal	
18	SDIO_D0	SDIO data line 0	
19	SDIO_D1	SDIO data line 1	
14	SDIO_D2	SDIO data line 2	
15	SDIO_D3	SDIO data line 3	
7	MIO13	SDIO suspend	

4.2 UART joggle

The module contains three UART interfaces, namely UART0 (UART_L0), UART1 (UART_H1) and UART2 (UART_H0) for debugging/AT port, and user custom/AT port.

UART0 is the debugging serial port, which is used for module firmware burning, maintenance and testing printing, AT debugging, etc. The default baud rate is 115200. The interface description is as follows:

Table 4-5 UART0 interface pin definition

Pin number	Pin definitions	description	remarks
37	TXD0	UART0 serial port send pin, that is UART_L0_TXD	The pin is directly connected, so the pull-up resistor can be reserved. Note the external level of VDDIO to ensure that it is consistent with the main control IO level
38	RXD0	UART0 serial receiver pin, i.e. UART_L0_RXD	

UART1 is a user-defined serial port, which can be used to connect with other devices and can

be used as an AT serial port for AT command transmission. The default baud rate is 115200. The interface description is as follows:

Table 4-6 Default pin definitions for UART1 interface

Pin number	Pin definitions	description	remarks
6/41	TXD1	UART1 serial port send pin, that is, UART_H1_TXD	The pin is directly connected, so the pull-up resistor can be reserved. Note that the VDDIO external level is consistent with the main control IO level
7/40	RXD1	UART1 serial port receive pin, that is, UART_H1_RXD	

UART2 is a user-defined serial port that can be used to connect with other devices. It supports modules configured as UART_H0_TXD and UART_H0_RXD functions. Please refer to the pin multiplexing table in Section 2.7 of the previous article. When utilizing the device, it is crucial to ensure that the VDDIO external level matches the main control IO level to prevent potential damage or malfunction.

4.3 PWM interface reference design

The DB35 module supports 8 PWM interface signal outputs, including 3 complementary PWM channels (PWM0 to PWM2) and 2 safety PWM channels (SPWM). The output levels are synchronized with the VDDIO voltage level, with a duty cycle output range of 0-100% (excluding 0% duty cycle), achieving up to 30kHz frequency and 100Hz step resolution. Note that PWM does not support multi-channel complementary outputs.

Table 4-7 PWM interface design suggestions

Module pin number	GPIO name	Interface name	Design recommendations
8/26/38	MIO10/AIO21/AIO2	PWM0_P	Direct connection, wiring $\leq 5\text{inch}$
5/39	AIO11/AIO3	PWM0_N	Direct connection, wiring $\leq 5\text{inch}$
29	MIO19	PWM2_P	Direct connection, wiring $\leq 5\text{inch}$

Module pin number	GPIO name	Interface name	Design recommendations
30	MIO20	PWM2_N	Direct connection, wiring $\leq 5\text{inch}$
23	MIO22	PWM3_P	Direct connection, wiring $\leq 5\text{inch}$
34	MIO16	PWM3_N	Direct connection, wiring $\leq 5\text{inch}$
10	MIO14	SPWM1_N	Direct connection, wiring $\leq 5\text{inch}$
13	MIO15	SPWM1_P	Direct connection, wiring $\leq 5\text{inch}$

PWM interface specifications are as follows:

- (1) Support 8 PWM outputs, registers can be configured separately.
- (2) The width of 0 and 1 levels can be adjusted.
- (3) Support fixed periodic sending mode.
- (4) Support for sending completion interrupt, support for interrupt clear and interrupt query.

4.4 I2S interface reference design

The DB35 module supports one I2S interface, and the input/output level is consistent with the VDDIO level.

Table 4-8 I2S interface design suggestions

Module pin number	GPIO name	Interface name	Design recommendations
6/29	MIO12/MIO19	I2S_DI	Direct link
7/28	MIO13/MIO18	I2S_DO	Direct link
8/30	MIO10/MIO20	I2S_WS	Direct link, land package treatment
5/27	MIO11/MIO17	I2S_BCLK	Connect the 33R resistor in series with the module and wrap the ground

4.5 I2C interface reference design

The DB35 module supports two sets of hardware I2C interfaces, and the input/output levels are

consistent with the VDDIO levels.

Table 4-9DB35 module I2C interface design suggestions

Module pin number	GPIO name	Interface name	Design recommendations
7/26	MIO13/MIO21	I2C0_SCL	Direct connection, wiring $\leq 5\text{inch}$, pull up $1\text{K}\Omega$ resistor to VDDIO
10/23	MIO14/MIO22	I2C0_SDA	Direct connection, wiring $\leq 5\text{inch}$, pull up $1\text{K}\Omega$ resistor to VDDIO
11/40	MIO9/AIO4	I2C1_SDA	Direct connection, wiring $\leq 5\text{inch}$, pull up $1\text{K}\Omega$ resistor to VDDIO
4/39	MIO8/AIO3	I2C1_SCL	Direct connection, wiring $\leq 5\text{inch}$, pull up $1\text{K}\Omega$ resistor to VDDIO

The I2C interface specifications are as follows:

(1) It supports two working modes: standard speed and fast speed. In the serial 8-bit two-way data transmission scenario, the standard mode can reach 100kbit/s and the fast mode can reach 400kbit/s.

(2) Support FIFO with 32bit $\times$ 8 bit width.

(3) Support 7bit/10bit addressing mode.

4.6 ADC reference design

The DB35 module supports 5 ADC interfaces with an ADC voltage input range 0 ~ 1.715V.

ADC input signals can be read through the UART0 serial port to determine the signal level.

Table 4-10DB35 module ADC interface design suggestions

Module pin number	GPIO name	Interface name	Design recommendations
37 (3)	AIO1	ADC_CH0	Direct connection, wiring $\leq 5\text{inch}$
39	AIO3	ADC_CH1	Direct connection, wiring $\leq 5\text{inch}$

40	AIO4	ADC_CH2	Direct connection, wiring $\leq 5\text{inch}$
23	MIO22	ADC_CH4	
4	MIO8	ADC_CH5	
11	MIO9	ADC_CH6	Direct connection, wiring $\leq 5\text{inch}$
21	MIO6	ADC_CH7	Direct connection, wiring $\leq 5\text{inch}$

remarks

(3) Module pin 37 is used as TXD0 function by default, and it is not recommended to reuse it for other GPIO functions.

4.7 SPI interface reference design

The DB35 module supports two SPI interfaces. The first is a full-duplex standard SPI interface designed to connect devices supporting the SPI protocol, where the SPI unit can operate as either a master or slave device. The second is a QSPI interface specifically configured for devices compliant with the QSPI protocol. Note that the input/output voltage levels must be synchronized with the VDDIO voltage levels.

Table 4-11DB35 module SPI interface design suggestions

Module pin number	GPIO name	Interface name	Design recommendations
6/21/16	MIO12/MIO6/MIO2	SPI0_DI	Direct connection, wiring $\leq 5\text{inch}$
7/11/18	MIO13/MIO9/MIO4	SPI0_DO	Direct connection, wiring $\leq 5\text{inch}$
8/19/32	MIO10/AIO5/MIO7	SPI0_CS0	Direct connection, wiring $\leq 5\text{inch}$
4/5/17	MIO8/MIO11/MIO3	SPI0_CLK	Connect the 33R resistor in series with the module, wrap the ground, and run the wiring $\leq 5\text{inch}$
30	MIO20	QSPI1_CS	Direct connection, wiring $\leq 5\text{inch}$
27	MIO17	QSPI1_CLK	Connect the 33R resistor in series with

Module pin number	GPIO name	Interface name	Design recommendations
			the module, wrap the ground, and run the wiring $\leq 5\text{inch}$
28	MIO18	QSPI1_D0	Direct connection, wiring $\leq 5\text{inch}$
29	MIO19	QSPI1_D1	Direct connection, wiring $\leq 5\text{inch}$
32	MIO7	QSPI1_D2	Direct connection, wiring $\leq 5\text{inch}$
34	MIO16	QSPI1_D3	Direct connection, wiring $\leq 5\text{inch}$

The SPI interface specifications are as follows:

(1) Supports SPI frame formats, which are divided into the following three types:

- Motorola frame format
- TI (Teaxs Instruments) frame format
- National Microwire frame format

(2) Each SPI has a FIFO with a 32-bit $\times$ 8 bit width that is separated from the transmission.

(3) Supports a maximum transfer bit width of 32 bits.

4.8 PATA interface reference design

Both Bluetooth and Wi-Fi operate on the 2.4GHz frequency band, which may cause mutual interference. Time-division multiplexing is a common solution to address noise and blocking interference issues. The 802.15.2 standard specifies arbitration methods and the Packet Traffic Arbitration (PTA) framework. When either Bluetooth or Wi-Fi transmits data, applications are submitted to the PTA controller (integrated into the Wi-Fi system), which then processes and grants permissions.

The DB35 module supports one PTA interface and supports both STA mode and Soft AP mode. The coexistence management of Bluetooth and Wi-Fi is shown in Figure 3.3. Note that the input/output level should be consistent with the VDDIO level.

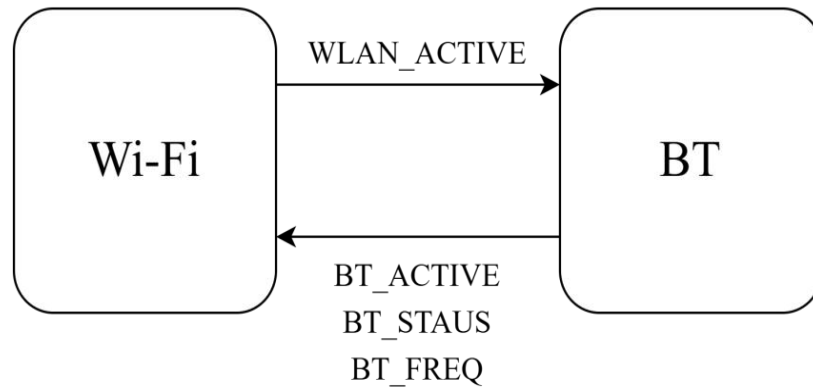


Figure 4.5 PTA interface design principle block diagram

Table 4-12 PTA interface design suggestions for DB35 module

Module pin number	GPIO name	Interface name	Design recommendations
29	MIO19	BT_FREQ	Direct connection, wiring ≤5inch
13/26/28	MIO15/MIO21/MIO18	BT_STAUS	Direct connection, wiring ≤5inch
10/27	MIO14/MIO17	BT_ACTIVE	Direct connection, wiring ≤5inch
23/30	MIO22/MIO20	WLAN_ACTIVE	Direct connection, wiring ≤5inch

The PTA sits between Wi-Fi MAC and Bluetooth, receiving TX/RX requests and status inputs from both Wi-Fi MAC and Bluetooth, and outputting arbitration results to Wi-Fi and Bluetooth. The handshake signal between Bluetooth and Wi-Fi is defined as follows:

- Wi-Fi signal PTA wl_tx_status: There is a packet transmission service on Wi-Fi.
- Wi-Fi signal PTA wl_rx_status: Wi-Fi has packet service.
- Wi-Fi signal priority: Wi-Fi service status, Wi-Fi high priority.
- Wi-Fi signal wl_occupied: Wi-Fi service status, Wi-Fi highest priority.
- Bluetooth sends PTA signal bt_status: Bluetooth has a service.

- Bluetooth signal PTA bt priority: Bluetooth service status, indicating the priority of Bluetooth.

4.9 Ultra-low power interface reference design

The DB35 module supports 9 ultra-low power consumption interfaces. Note that the input/output level should be consistent with the VDDIO level.

Table 4-13DB35 module ultra-low power interface design suggestions

Module pin number	GPIO name	Design recommendations	remarks
15	MIO6	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, only input wake-up is supported, not output
19	AIO5	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, input wake up or output is supported
37	AIO1	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, input wake up or output is supported
38	AIO2	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, input wake up or output is supported
39	AIO3	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, input wake up or output is supported
40	AIO4	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, input wake up or output is supported
5	MIO11	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, only input wake-up is supported and output is not supported
32	MIO7	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, only input wake-up is supported, not output
34	MIO16	Direct connection, wiring $\leq 5\text{inch}$	In deep sleep mode, only input wake-up is supported, not output

4.10 Antenna selection interface

The DB35 module supports four antenna selection interfaces. Note that the input/output levels are consistent with the VDDIO levels.

Table 4-14DB35 module ultra-low power interface design suggestions

Module pin number	GPIO name	Interface name	Design recommendations
6	MIO12	ANT_SEL4	Direct connection, wiring $\leq$ 5inch
8	MIO10	ANT_SEL3	Direct connection, wiring $\leq$ 5inch
23	MIO22	ANT_SEL5	Direct connection, wiring $\leq$ 5inch
32	MIO7	ANT_SEL2	Direct connection, wiring $\leq$ 5inch

5 Radio frequency characteristics

5.1 radio frequency interface

Table 5-1 Antenna interface definitions

Pin number	Pin definitions	I/O type	description	remarks
2	RF	ANT	2.4G Wi-Fi&BT radio frequency interface	50Ω characteristic impedance

5.2 Wi-Fi function

Table 5-2 Wi-Fi performance parameters

function	description	
Wireless standards	IEEE 802.11b/g/n/ax(@2.4GHz), Wi-Fi compliant	
service frequency	2400~2483.5MHz (2.4GHz ISM Band)	
channel	2.4GHz: Ch1 ~ Ch13	
modulation mode	802.11b	DQPSK,DBPSK,CCK
	802.11g/n: OFDM	64-QAM,16-QAM,QPSK,BPSK
	802.11ax: OFDMA	256-QAM,64-QAM,16-QAM, QPSK,BPSK
frequency tolerance	±20ppm	
Receive Sensitivity (11b,20MHz) @ 8% PER	1Mbps	-97dBm, Typical
	11Mbps	-89dBm, Typical
Receive Sensitivity (11g,20MHz) @ 10% PER	6Mbps	-94dBm, Typical
	54Mbps	-76dBm, Typical
Receive Sensitivity (11n,20MHz) @ 10% PER	MCS=0	-93dBm, Typical
	MCS=7	-74dBm, Typical

function	description	
Receive Sensitivity (11n,40MHz) @ 10% PER	MCS=0	-91dBm, Typical
	MCS=7	-71dBm, Typical
Receive Sensitivity (11ax,20MHz) @ 10% PER	MCS=0	-94dBm, Typical
	MCS=9	-69dBm, Typical

5.3 BLE function

Table 5-3 BLE performance parameters

function	description
Bluetooth standard	BLE5.3
service frequency	2402~2480MHz (2.4GHz ISM Band)
channel	LE: Ch0 ~ Ch39
modulation mode	GFSK
Sensitivity @ PER=30.8%, for LE(1Mbps)	-97dBm, Typical
Sensitivity @ PER=30.8%, for LE(2Mbps)	-93dBm, Typical
Sensitivity @ PER=30.8%, for LE(S2)	-98dBm, Typical
Sensitivity @ PER=30.8%, for LE(S8)	-101dBm, Typical
maximum input level	0dBm

5.4 Reference design of RF link

When the DB35 module is applied, it is recommended to reserve π matching circuit on the wiring of the RF interface of the module on the user's base plate, and strict 50Ω characteristic impedance control should be done, as shown in the figure below:

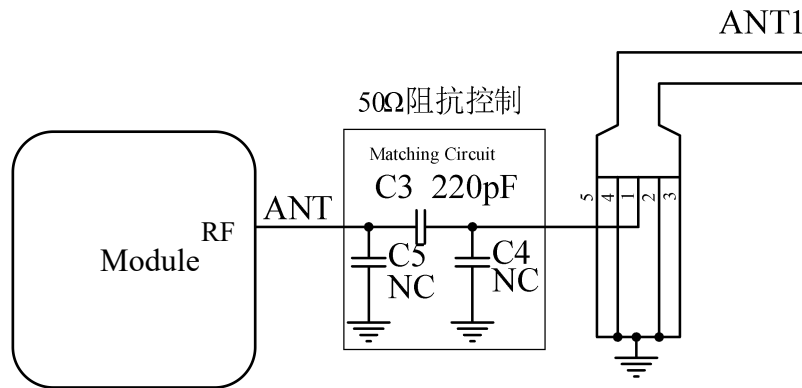


Figure 5.1 Antenna reference design circuit

Before the initial debugging of the user, C3 uses 220pF capacitor or 0R resistor by default, and C4 and C5 are not installed as matching reserve. The final value of this π type matching parameter should be determined according to the actual debugging results.

The RF interface of the module must be connected to the antenna on the base plate with wiring that strictly maintains a 50Ω characteristic impedance, as this is the internationally recognized standard for RF circuits to ensure optimal energy transfer and minimize reflections. The wiring should be as short as possible, without vias or sharp angles. It is recommended to make more GND vias around the RF wiring to reduce signal crosstalk, as shown in Figure 5.2:

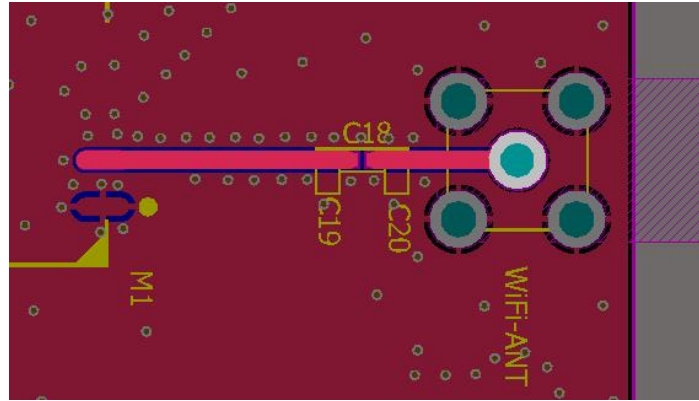


Figure 5.2 Impedance lines of the base plate

The relationship between plate thickness and line width and line spacing can be referenced as follows:

FR4 double panel recommended value (H= plate thickness, W= line width, D= spacing between wiring and copper)

- H=1.0mm, W=0.8mm, D=0.2mm
- H=1.0mm, W=1.0mm, D=0.254mm (Recommended)
- H=1.2mm, W=1.0mm, D=0.2mm (Recommended)
- H=1.6mm, W=1.0mm, D=0.2mm (Recommended)

For the π -type matching circuit, in order to avoid introducing additional parasitic parameters, it is recommended to place it as shown in the following figure:

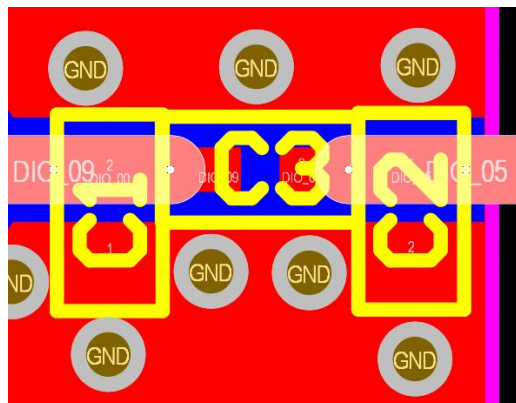


Figure 5.3 CLC placement method for π -type matching circuit

5.5 Antenna selection reference

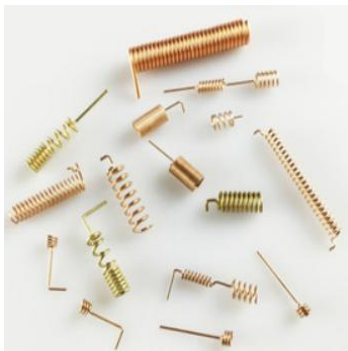
The DB35 module requires an external antenna connection, with available types including PCB-mounted antennas, electronic wires, spring antennas, FPC antennas, rod antennas, and ceramic antennas. Adequate clearance space must be ensured around the antenna. Users should select appropriate antenna configurations based on product dimensions and available space, as illustrated in Figure 5.4 which displays several common antenna configurations.



(a) PCB antenna



(b) Wireless antenna



(c) spring antenna



(d) FPC antenna-with IPEX connector



(e) bar antenna



(f) But SMT ceramic antenna

Figure 5.4 Several common 2.4GHz antennas,

Table 5-5 lists the specifications and parameters of a 2.4GHz antenna for users to select and

reference.

Recommended antenna specifications

frequency range	2400~2500MHz
input impedance	50Ω
Return Loss (RL)	S11≤-10dB
Standing wave ratio (VSWR)	≤2.0
Gain (4)	≥2.0dBi
Direction of radiation (5)	omnidirectional

remarks

(4) The gain should be selected in compliance with the local radio regulations, ensuring that the equivalent isotropically radiated power (EIRP) does not exceed the specified limits, such as $\leq 100\text{mW}$ or $\leq 20\text{dBm}$ for antennas with a gain less than 10dBi, and $\leq 500\text{mW}$ or $\leq 27\text{dBm}$ for antennas with a gain of 10dBi or more.

(5) Common wireless intelligent products should use omnidirectional antenna as far as possible.

5.6 Plate layout notes

Users are advised to route signals on the TOP layer of the base board to avoid modules. Critical interference-prone traces should maintain sufficient clearance to prevent unintended disturbances. For example, RF traces should be kept as far away as possible from strong interference sources such as clock lines, power lines, SDIO traces, DDR, and CPU. The reference ground for RF traces must remain intact, with strict prohibition of crossing or layer changes.

The base plate design does not require special hollowing treatment, enabling full copper plating across the entire surface. To enhance heat dissipation, users are advised to implement windowed copper exposure in the TOP layer corresponding to the module's BOTTOM layer's

exposed copper area. Slight soldering on this exposed zone can optimize thermal conductivity, though excessive solder paste may cause module soldering issues like floating and poor contact during assembly, as well as via solder leakage. As shown in Figure 5.5, the DB35 module's BOTTOM layer windowed copper exposure area dimensions and positions should follow the recommended packaging specifications outlined in Section 7.2.

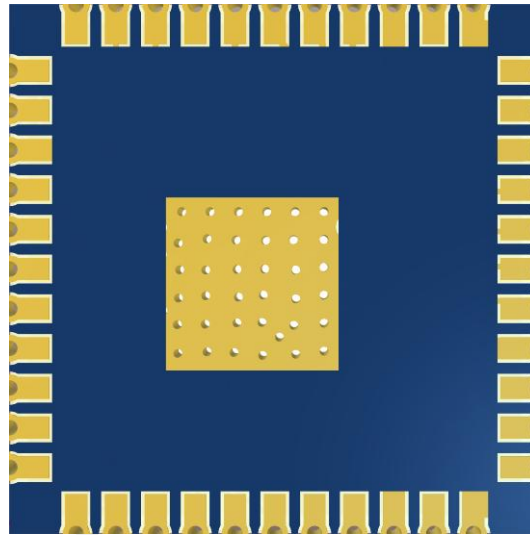


Figure 5.5 Module BOTTOM layer exposed copper window area

6 Electrical performance and reliability

6.1 Rated power supply

Table 6-1 Rated power supply values

parameter	description	least value	representative value	crest value	unit
VBAT_IN(6)	Power supply voltage at the power pin	3.16	3.3(7)	3.465	V
VDDIO	IO power supply voltage	1.71	1.8/3.3	3.465	V

remarks

(6) The limit value of VBAT_IN power supply is 3.0~3.6V, exceeding the range may cause permanent damage to the device;

(7) To guarantee the module's stable operation, the external power supply's total capacity should exceed the module's power consumption, which is typically greater than 1000mA.

6.2 DC electrical characteristics

Table 6-2 DC electrical characteristics of modules (VDDIO=1.8V)

symbol	description	least value		crest value	
VDDPST	interface voltage	1.62	1.8	1.98	V
VIL	low level input voltage	-0.3	-	0.35*VDDPST	V
VIH	high level input voltage	0.65*VDDPST	-	VDDPST+0.3	V
IL	Input leakage current	0.06	-	61.18	nA
VOL	low level input voltage	-	-	0.45	V
VOH	high level output voltage	VDDPST-0.45	-	-	V
RPU	Internal pull-up resistor	49.3	61.56	85.07	KΩ

RPD	Internal pull-down resistor	54.54	70.3	102.3	KΩ
-----	-----------------------------	-------	------	-------	----

Lierda
利 尔 达

Table 6-3 DC electrical characteristics of modules (VDDIO=3.3V)

symbol	description	least value		crest value	
VDDPST	interface voltage	2.97	3.3	3.63	V
VIL	low level input voltage	-0.3	-	0.8	V
VIH	high level input voltage	2.0	-	VDDPST+0.3	V
IL	Input leakage current	0.12	-	68.29	nA
VOL	low level input voltage	-	-	0.4	V
VOH	high level output voltage	2.4	-	-	V
RPU	Internal pull-up resistor	50.36	60.72	74.71	KΩ
RPD	Internal pull-down resistor	47.84	57.42	70.73	KΩ

6.3 power dissipation

Table 6-4 Module power consumption data

description	test condition	representative value (mA)		
		IAve@TX	IPeak@TX1	IAve@RX
Wi-Fi data transmission	802.11b,11Mbps@20dBm	320	370	50
	802.11g,54Mbps@18dBm	220	300	50
	802.11n,HT20,MCS7@17dBm	200	300	50
	802.11n,HT40,MCS7@17dBm	190	300	50
	802.11ax,HE20,MCS9@14dBm	180	250	50
BLE data transmission	BLE @1M @14dBm	85	105	30
	BLE @2M @14dBm	65	105	30

6.4 electrostatic protection

In module applications, static electricity generated by human body discharge and microelectronic interfacial friction can be released to modules through various pathways, potentially

causing damage. Prioritizing ESD protection is crucial to ensure product quality and reliability, as emphasized in the manufacturing of PCBs and PCBA, where ESD 防护 is integrated from the design phase to the production process. In the design, development, and testing phases, especially during the product design stage, it is imperative to incorporate robust ESD protection measures to safeguard electronic components from the detrimental effects of electrostatic discharge. For instance, anti-static shielding should be added at circuit interface points and vulnerable areas. Susceptible to electrostatic discharge damage. Testing equipment must maintain proper grounding, while production personnel should wear anti-static gloves during manufacturing processes.

6.5 Working and storage temperature

Table 6-6 Operating temperature and storage temperature

parameter	description	least value	representative value	crest value	unit
TA	Working temperature (8)	-40	/	+85	°C
TStorage	Storage temperature	-40	/	+105	°C

remarks

(8) In order to meet the requirements of normal working temperature range, it is necessary to add heat dissipation measures, such as using active or passive radiator, equalizing plate, etc. The module meets the requirements of IEEE 802.11 and BLE within its operational temperature range, which is suitable for industrial applications.

7 Mechanical dimensions

7.1 Mechanical dimensions

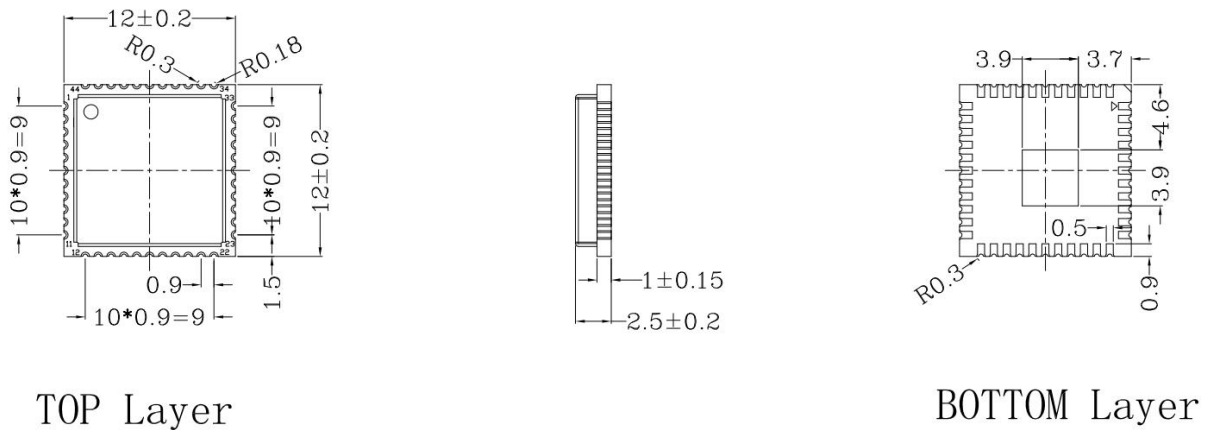


Figure 7.1 Module external dimensions (unit: mm)

7.2 Recommended packaging

The outermost Mechanical 1 layer in module packaging defines the safety distance for 0402 and smaller components. Any 0402 or smaller package components on the base board must be positioned outside this peripheral layer. Critical bottom areas of the base board must remain free of any traces to prevent soldering interference that could cause product malfunctions. The TOP layer of the package is equipped with reserved thermal window pads. Users are advised to retain these pads and adjust soldering quantities based on actual board mounting conditions to optimize heat dissipation.

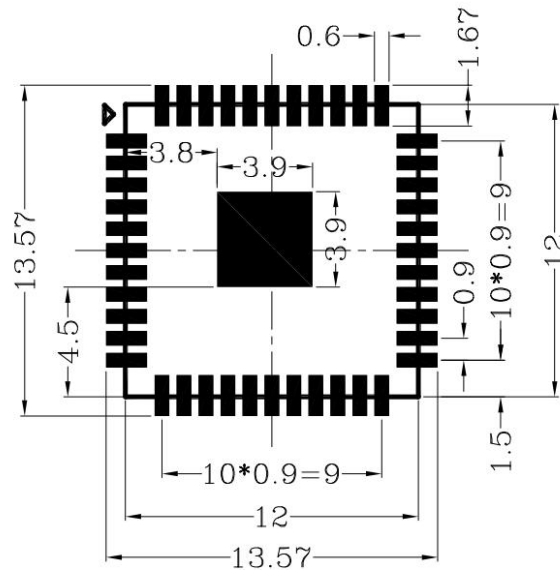


Figure 7.2 Module recommended package (unit: mm)

8 Production and packaging information

This chapter describes the packaging, storage, production, maintenance and other guidance information of the module, which is applicable to the assembly process guidance of the module.

8.1 packing specifications

8.1.1 manner of packing

Table 8-1 Module roll packaging information

model	manner of packing	Box (PCS)	Minimum package quantity (PCS)	Number of coils per box
DB35	winding	6500	1300	5

8.1.2 Strap size and product direction

Schematic diagram of packaging module placement direction: (Refer to the figure, the label content is subject to the actual, pay attention to the position of module PIN1)

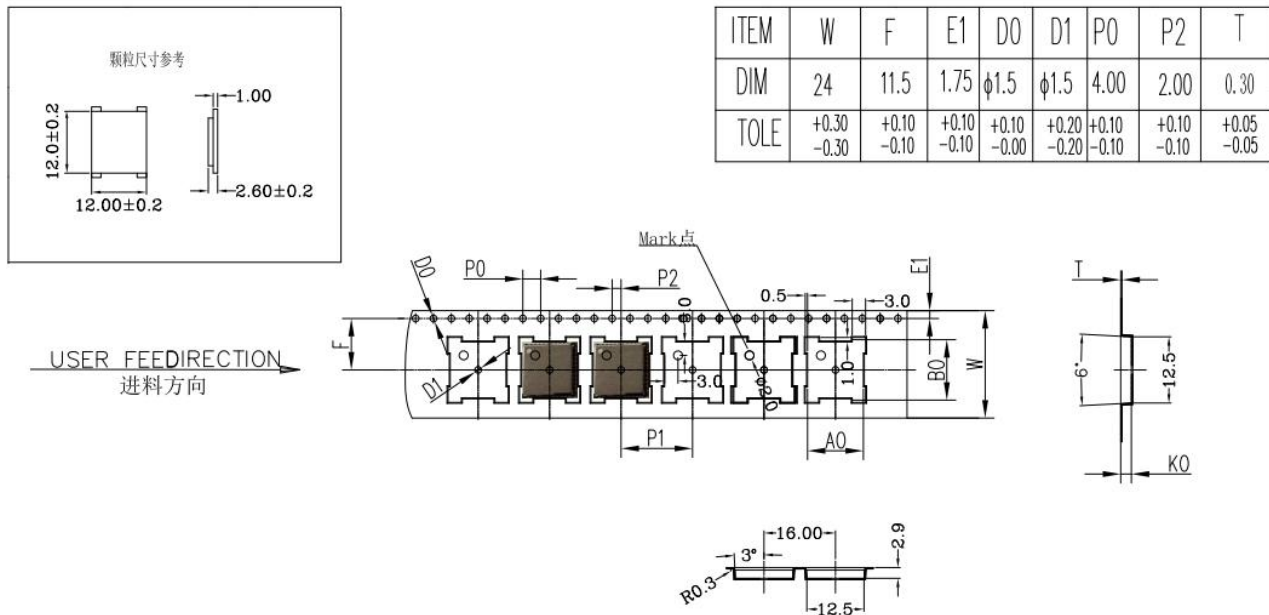


Figure 8.1 Packing specifications and dimensions

8.2 storage condition

The modules are shipped in the form of vacuum reel sealing bags with a humidity sensitive grade of MSL 3.

condition of storage :

- (1) Temperature below 40°C and humidity below 90% (RH) can ensure 12 months of weldability in a well-sealed package.
- (2) After unpacking, ensure that the patch assembly is performed within 168 hours under ambient temperature less than 30°C and relative humidity less than 60% (RH).

If the above conditions are not met, baking is required:

- (1) Carton packaging, baked at $60^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 24 to 48 hours,
- (2) If you need to accelerate the baking, you need to take the module out of the roll and place it on a high temperature resistant container (e.g., tray) for baking (note ESD protection during

removal), and bake it for 8 hours at $125^{\circ}\text{C} \pm 5^{\circ}\text{C}$.

(3) The cumulative baking time should not exceed 96 hours.

For more details, please refer to the IPC/JEDECJ-STD-033 specification.

8.3 Production welding

8.3.1 Furnace type

If the customer's module substrate is a double-sided board, it is recommended to place the module in the second placement process. During the first placement, the customer's substrate should ideally be baked on a wire mesh. For the second placement, it's advisable to maintain this practice. If special circumstances prevent wire mesh baking, consider using fixtures to bake the PCB via track alignment or placing a flat, heat-resistant straight template to support the PCBA during baking. This prevents PCB deformation that could cause module soldering failures.

8.3.2 Module position requirements on the base plate

It is recommended that the thickness of green oil at the bottom plate module position should be less than 0.02mm to avoid excessive thickness, which may prevent the raised module from effectively contacting the solder paste and affect the welding quality. In addition, other components should not be arranged within 2mm around the interface board module position to ensure the maintenance of the module.

8.3.3 Steel mesh opening design

The selection principle of steel mesh thickness on the base plate is selected according to the packaging type of the internal components of the plate. The following requirements should be paid attention to:

The position of the module pad can be thickened locally to 0.15~0.20mm to avoid empty welding.

8.3.4 Production Notes

- In the production process, all operators must wear static gloves;
- Do not exceed the specified baking time when baking;
- Do not add explosive, combustible and corrosive substances during baking;
- When baking, the module should be placed in a high temperature tray to maintain air circulation between the modules;
- When baking, the oven door should be closed to ensure that the oven is closed to prevent temperature leakage;
- Try not to open the door when the oven is running. If it must be opened, shorten the time to open the door as far as possible;
- After baking, wait for the module to cool down to below 36°C before wearing static gloves to take it out to avoid burns;
- When operating, strictly prevent water or dirt on the bottom surface of the module.

8.3.5 Reflow soldering operation instructions

The temperature curve of the PCBA reflow soldering furnace is related to the use of solder paste and should be adjusted according to the actual solder paste. The data is only suitable for lead-free operation, refer to Figure 8.2 lead-free reflow soldering operation instruction.

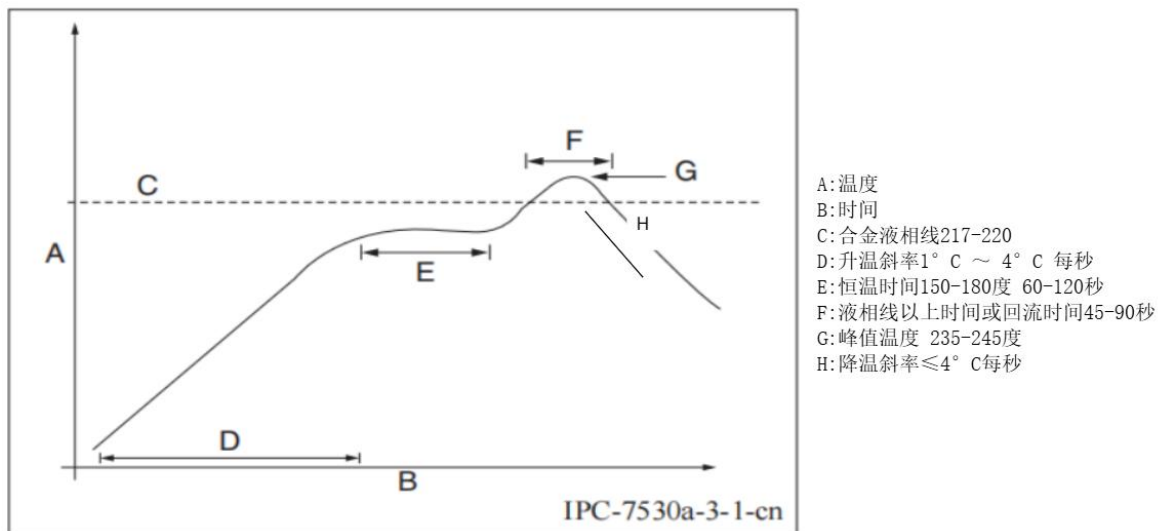


Figure 8.2 Reflow soldering instruction manual

remarks

- (1) In the process of welding or other possible direct contact with the module, do not use any organic solvents (such as alcohol, isopropanol, acetone, trichloroethylene, etc.) to wipe the module shield; otherwise, the shield may be rusted.
- (2) The module silver-white copper laser-engraved shielding cover can meet the requirements that after 12 hours of neutral salt spray test, the laser-engraved information is clear and recognizable, and the QR code can be scanned (there may be white rust).
- (3) If you need to spray the module, make sure that the spraying material does not react with the module shield or PCB, and ensure that the spraying material does not flow into the module.
- (4) Do not ultrasonically clean the module, otherwise the crystal inside the module may be damaged.
- (5) Due to the complexity of SMT process, if there are uncertain conditions or processes not mentioned in the document (such as selective wave soldering, ultrasonic welding), please confirm with Lierda technical support before the start of SMT process.

8.3.6 keep in repair

If the module is faulty such as false soldering or short circuit and needs to be repaired, please follow the following parameters:

Lead-free process: soldering iron temperature $380\pm 10^{\circ}\text{C}$, soldering iron contact time $\leq 5\text{S}$;

Lead process: soldering iron temperature $350\pm 10^{\circ}\text{C}$, soldering iron contact time $\leq 5\text{S}$;

The module is not recommended to be blown with a hot air gun to avoid affecting the performance of the module.

9 Related documents and abbreviations of terms

The following documents provide the name of the document. Please use the latest release as the version.

Table 9-1 Relevant documents

order number	Document name	explanatory note
[1]	IEC 61000-4-2 standard	
[2]	IPC/JEDECJ-STD-033 specification	

Table 9-2 Abbreviations

abbreviation	English full name	Chinese full name
IEEE	Institute of Electrical and Electronics Engineers	Institute of Electrical and Electronics Engineers
BLE	Bluetooth Low Energy	Bluetooth Low Power
SDIO	Secure Digital Input and Output	Secure Digital Input/Output (Interface)
IPC	IP Camera	web camera
ISM band	Industrial Scientific Medical Band	Industrial, scientific and medical frequencies
MAC	Media Access Control	medium access control
WEP	Wired Equivalent Privacy	Wired equivalent security (protocol)
WPA	Wi-Fi Protected Access	Wi-Fi protected access
UART	Universal Asynchronous Receiver/Transmitter	General asynchronous receiver transmitter
TXD	Transmit external Data	transmit by radio
RXD	Receive external Data	receive
bps	Bits Per Second	Rate unit
PTA	Packet Traffic Arbitration	Subcontracting flow arbitration
RF	Radio Frequency	radio frequency

abbreviation	English full name	Chinese full name
ANT	Antenna	antenna
OFDM	Orthogonal Frequency Division Multiplexing	orthogonal frequency division multiplexing
DQPSK	Differential Quadrature (Reference) Phase Shift Keying	Differential orthogonal phase shift keying
DBPSK	Differential Binary (Coherent) Phase Shift Keying	Differentiated binary phase shift keying
CCK	Complementary Code Keying	Complementary code keystrokes
QAM	Quadrature Amplitude Modulation	Orthogonal amplitude modulation
QPSK	Quadrature Phase Shift Keying	Orthogonal phase shift keying
BPSK	Binary Phase Shift Keying	Binary phase shift keying
PER	Packets Error Rates	Error rate
GFSK	Gauss frequency Shift Keying	Gaussian frequency shift keying
PCB	Printed Circuit Board	printed-circuit board
VSWR	Voltage Standing Wave Ratio	voltage standing-wave ratio
DDR	Double Data Rate	Double speed
CPU	Central Processing Unit	central processing unit
VIL	Input Low Level Voltage Value	low level input voltage
VIH	Input High Level Voltage Value	high level input voltage
VOL	Output Low Level Voltage Value	low level input voltage
VOH	Output High Level Voltage Value	high level input voltage
RPU	Pull-up resistor value	Pull-up resistance value
RPD	Pull-down resistor value	Pull-down resistance value
ESD	Electro-Static discharge	static electricity discharge
MSL	Moisture Sensitivity levels	Moisture sensitivity level