

# Lierda WB81 Series Hardware Design Manual

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State: Controlled Version

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## Revision History

| Version | Date       | Draft | Approved | Revision Content |
|---------|------------|-------|----------|------------------|
| Rev 1.0 | 2023-01-13 | TTY   | YB       | Initial Version  |



# Safety Instructions

It is the user's responsibility to follow the relevant regulations of other countries on wireless communication modules and equipment, as well as their specific operating environment regulations. By following the safety principles below, you can ensure personal safety and help protect the product and work environment from potential damage. Our company is not responsible for related losses caused by customers' failure to follow these regulations.



Road safety first! Do not use a handheld mobile terminal while driving unless it has a hands-free function. Please stop and call again!



Please turn off the mobile terminal device before boarding the plane. The wireless function of the mobile terminal is prohibited on the aircraft to prevent interference with the aircraft communication system. Ignoring this prompt may affect flight safety or even violate the law.



When in a hospital or health care facility, pay attention to whether there are restrictions on the use of mobile terminal equipment. RF interference can cause medical equipment to malfunction and it may be necessary to switch off the mobile terminal equipment.



The mobile terminal device does not guarantee a valid connection in all cases, eg no call charges or SIM invalidation on the mobile terminal device. When you encounter the above situations in an emergency, please remember to use the emergency call, and at the same time make sure that your device is powered on and in an area with sufficient signal strength.



Your mobile terminal equipment will receive and transmit radio frequency signals when it is turned on, and radio frequency interference will be generated when it is close to a TV, radio, computer or other electronic equipment.



Please keep the mobile terminal away from flammable gas. When you are close to gas stations, oil depots, chemical plants or explosive workplaces, please turn off the mobile terminal device. Operating electronic equipment in any potentially explosive atmosphere is a safety hazard.

## Applicable Module Selection

| No. | Model Name      | Support<br>Frequency Band | Dimension(mm) | Description      |
|-----|-----------------|---------------------------|---------------|------------------|
| 1   | L-WFIWB81-G5PP4 | 2.4GHz ISM Band           | 31.4×18×3.35  | IoT Wi-Fi Module |

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# Contents

|                                                                  |    |
|------------------------------------------------------------------|----|
| Legal Notices .....                                              | 1  |
| Revision History .....                                           | 2  |
| Safety Instructions .....                                        | 3  |
| Applicable Module Selection .....                                | 4  |
| Contents .....                                                   | 5  |
| 1 Introduction .....                                             | 7  |
| 2 Overview .....                                                 | 8  |
| 2.1 Product Information .....                                    | 8  |
| 2.2 General Specification .....                                  | 8  |
| 2.3 Features .....                                               | 9  |
| 2.4 Applications .....                                           | 10 |
| 2.5 Block Diagram .....                                          | 10 |
| 2.6 Pin Assignments .....                                        | 11 |
| 2.7 Pin Definition .....                                         | 11 |
| 2.8 Strapping pin .....                                          | 13 |
| 2.9 Physical Dimensions .....                                    | 16 |
| 2.10 Recommended schematic symbol and PCB package graphics ..... | 16 |
| 3 RF Characteristics .....                                       | 18 |
| 3.1 Wi-Fi RF Characteristics .....                               | 18 |
| 3.2 BT RF Characteristics .....                                  | 19 |
| 3.2.1 BR+EDR Mode .....                                          | 19 |
| 3.2.2 Bluetooth LE Mode .....                                    | 20 |
| 3.3 Antenna area clearance design .....                          | 21 |

|                                                           |    |
|-----------------------------------------------------------|----|
| 4 Reference Design .....                                  | 23 |
| 4.1 Peripheral schematic design reference .....           | 23 |
| 4.2 Peripheral Pinout .....                               | 24 |
| 4.3 Backplane Layout Considerations .....                 | 28 |
| 5 Electrical Performance and Reliability .....            | 30 |
| 5.1 Electrical Characteristics .....                      | 30 |
| 5.2 Power Consumption .....                               | 30 |
| 6 Production and Packaging Information .....              | 33 |
| 6.1 Production Welding .....                              | 33 |
| 6.1.1 Production Instructions .....                       | 33 |
| 6.1.2 Module location requirements on the backplane ..... | 34 |
| 6.1.3 Stencil Opening Design .....                        | 34 |
| 6.1.4 Production Notes .....                              | 34 |
| 6.1.5 Recommended Reflow Profile .....                    | 35 |
| 6.2 Package Information .....                             | 36 |
| 6.2.1 Packaging Method .....                              | 36 |
| 6.2.2 Carrier Size Detail .....                           | 36 |

# 1 Introduction

WB81 series is a high-performance universal IoT Wi-Fi4 module that supports 802.11b/g/n @ 2.4 GHz and Bluetooth 4.2 (BR/EDR/BLE) functions (currently only the onboard antenna version is optional). The module is scalable and self-adaptive, powerful and versatile. The built-in chip contains an Xtensa® 32-bit LX6 single/dual-core CPU that can be individually controlled, and the main clock frequency supports adjustment within the range of 80 MHz to 240 MHz; the module has rich internal development resources and provides optional PSRAM and FLASH with different capacities (default 2 MB PSRAM and 8 MB FLASH); supports TCP/IP protocol, fully complies with 802.11 Wi-Fi MAC protocol stack, data transmission rate up to 150 Mbps, antenna output power up to 20 dBm, can achieve a wide range of wireless communication. At the same time, WB81 supports optimizing the effective working time and realizing power consumption management by minimizing host interaction; it also integrates a wealth of peripherals, including Hall sensors, SD card interface, Ethernet interface, high-speed SPI, UART, I2S and I2C, etc., can be widely used in mobile devices, low-power IoT sensor hubs, photovoltaic communication sticks/collectors, smart homes and other fields.



Figure 1.1 WB81 Series Module

## 2 Overview

### 2.1 Product Information

Table 2-1 Product Information

| Module          | Description                                                                       |
|-----------------|-----------------------------------------------------------------------------------|
| L-WFIWB81-G5PP4 | ESP32, b/g/n Wi-Fi, 1T1R, 31.4mm*18mm*3.35mm, with shield, TVS and 40MHz Crystal. |

### 2.2 General Specification

Table 2-2 General Specification

| Feature                 | Description                                                                                                                          |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| Interface               | Stamp hole                                                                                                                           |
| Wireless Standard       | IEEE 802.11 b/g/n + BT 4.2 (BR/EDR+BLE)                                                                                              |
| Dimension               | 18.0 mm × 31.4 mm × 3.35 (Max) mm                                                                                                    |
| Operating Voltage       | 3.0 V ~ 3.6 V , Typ 3.3 V                                                                                                            |
| Frequency Range         | 2400 ~ 2483.5 MHz (2.4 GHz ISM Band)                                                                                                 |
| Operating Temperature   | -40 ~ +85 °C                                                                                                                         |
| Storage Temperature     | -40 ~ +105 °C                                                                                                                        |
| Communication Interface | SD card, UART, SPI, SDIO, I2C, LED PWM, I2S, IR, Capacitive TOUCH, pulse counter, GPIO, ADC, DAC, TWAI® and Ethernet interface, etc. |
| Bandwidth               | Support 20/40MHz bandwidth                                                                                                           |
| Storage Characteristics | Initial model supports 2 MB PSRAM (QSPI) and 8 MB FLASH (QSPI)                                                                       |

## 2.3 Features

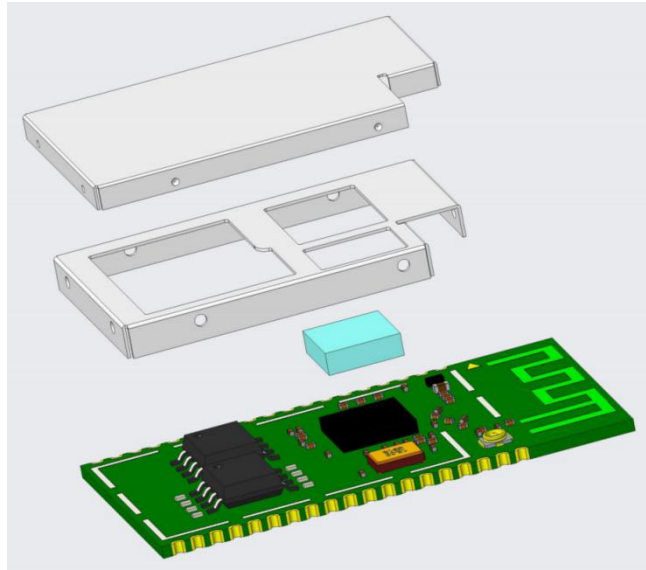


Figure 2.1 Schematic diagram of module structure

- Shielding frame + shielding cover combination structure is adopted, the shielding cover is flexible to install and disassemble, and it is convenient for visual inspection and maintenance. The module structure is shown in Figure 2.1; and heat-dissipating silica gel is added to the chip, and the heat dissipation performance can be optimized up to 5°C in a 25°C working environment. °C, optimized up to 10°C under 85°C working environment.

- Support IEEE 802.11b/g/n @ 2.4G (802.11n, transmission speed up to 150 Mbps).
- Support Bluetooth 4.2, including traditional Bluetooth (BR/EDR) and low-power Bluetooth (Bluetooth LE).
- Support infrastructure network (Infrastructure BSS) Station/Soft AP/hybrid mode.
- Supports CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4) and CRC.
- Standard HCI based on SDIO/SPI/UART interface.
- High-speed UART HCI, up to 4 Mbps.
- Support CVSD and SBC audio codec algorithms.
- Ethernet MAC interface with dedicated DMA supporting IEEE 1588.

- Supports the two-wire automotive interface TWAI®, compliant with ISO 11898-1 (CAN specification 2.0).
- Cryptographic hardware accelerators such as AES, Hash (SHA-2), RSA, ECC, and Random Number Generator (RNG) are supported.

## 2.4 Applications

- Photovoltaic communication stick/collector
- Smart Gateway Device
- Smart Home Appliances
- Health/Medical/Nursing Equipment

## 2.5 Block Diagram

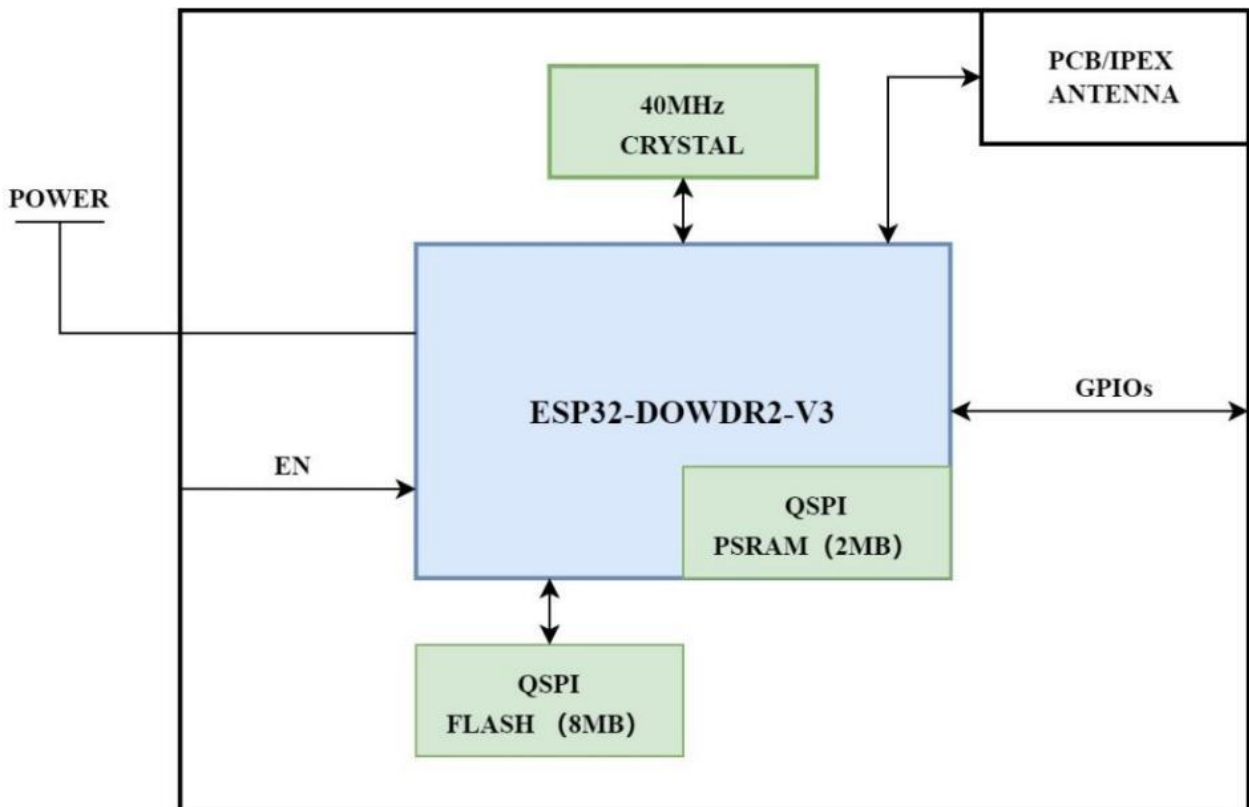


Figure 2.2 WB81 Block Diagram

## 2.6 Pin Assignments

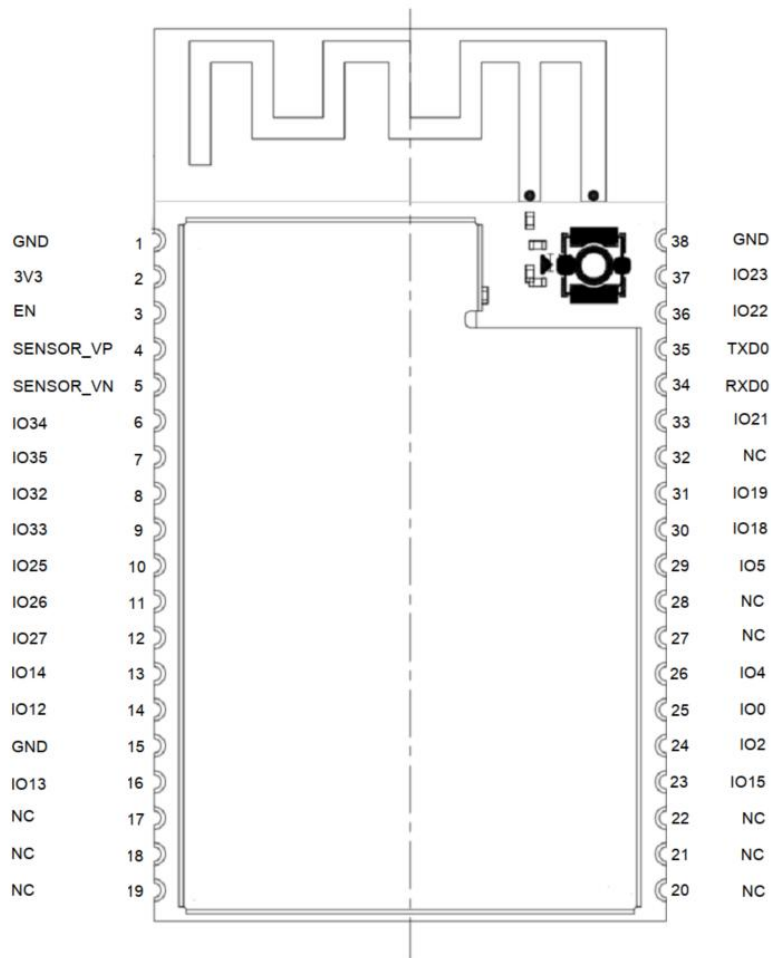


Figure 2.2 Pin Outline

## 2.7 Pin Definition

Table 2-3 Pin Definition

| No. | Name      | Type | Description                                                                    |
|-----|-----------|------|--------------------------------------------------------------------------------|
| 1   | GND       | P    | Ground                                                                         |
| 2   | 3V3       | P    | Power supply                                                                   |
| 3   | EN        | I    | Module-enable signal, Active high, which is connected to pin CHIP_PU on the IC |
| 4   | SENSOR_VP | I    | GPIO36, ADC1_CH0, RTC_GPIO0                                                    |

|    |           |     |                                                                                        |
|----|-----------|-----|----------------------------------------------------------------------------------------|
| 5  | SENSOR_VN | I   | GPIO39, ADC1_CH3, RTC_GPIO3                                                            |
| 6  | IO34      | I   | GPIO34, ADC1_CH6, RTC_GPIO4                                                            |
| 7  | IO35      | I   | GPIO35, ADC1_CH7, RTC_GPIO5                                                            |
| 8  | IO32      | I/O | GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9  |
| 9  | IO33      | I/O | GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8 |
| 10 | IO25      | I/O | GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0                                          |
| 11 | IO26      | I/O | GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1                                          |
| 12 | IO27      | I/O | GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV                                       |
| 13 | IO14      | I/O | GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2        |
| 14 | IO12      | I/O | GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3      |
| 15 | GND       | P   | Ground                                                                                 |
| 16 | IO13      | I/O | GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER     |
| 17 | NC        | -   | Pulled up and not connected                                                            |
| 18 | NC        | -   | Pulled up and not connected                                                            |
| 19 | NC        | -   | Pulled up and not connected                                                            |
| 20 | NC        | -   | Pulled up and not connected                                                            |
| 21 | NC        | -   | Pulled up and not connected                                                            |
| 22 | NC        | -   | Pulled up and not connected                                                            |
| 23 | IO15      | I/O | GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3        |
| 24 | IO2       | I/O | GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPiWP, HS2_DATA0, SD_DATA0                       |
| 25 | IO0       | I/O | GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK                             |
| 26 | IO4       | I/O | GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPiHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER           |
| 27 | NC        | -   | Pulled up and not connected                                                            |

|    |      |     |                                        |
|----|------|-----|----------------------------------------|
| 28 | NC   | -   | Pulled up and not connected            |
| 29 | IO5  | I/O | GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK |
| 30 | IO18 | I/O | GPIO18, VSPICLK, HS1_DATA7             |
| 31 | IO19 | I/O | GPIO19, VSPIQ, U0CTS, EMAC_TXD0        |
| 32 | NC   | -   | Pulled up and not connected            |
| 33 | IO21 | I/O | GPIO21, VSPIHD, EMAC_TX_EN             |
| 34 | RXD0 | I/O | GPIO3, U0RXD, CLK_OUT2                 |
| 35 | TXD0 | I/O | GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2      |
| 36 | IO22 | I/O | GPIO22, VSPIWP, U0RTS, EMAC_TXD1       |
| 37 | IO23 | I/O | GPIO23, VSPID, HS1_STROBE              |
| 38 | GND  | -   | Ground                                 |

## NOTE

Note:P indicates a power supply pin and I/O indicates an input/output pin.

## 2.8 Strapping pin

The WB81 module has 5 strapping pins: MTDI (GPIO12), GPIO0, GPIO2, MTDO (GPIO15) and GPIO5. Software can read the strapping values of these 5 pins in the register "GPIO\_STRAPPING".

In the process of releasing the system reset (power-on reset, RTC watchdog reset, brown-out reset) of the module chip, the Strapping pin will sample the level and store it in the latch, and the latch is "0". or "1" and remain until the chip is powered down or turned off. And each Strapping pin will be connected to internal pull-up/pull-down. If a Strapping pin has no external connection or the connected external line is in a high-impedance state, the internal weak pull-up/pull-down will determine the default value of the Strapping pin input level. To change the value of Strapping, users can use an external pull-down/pull-up resistor, or use the GPIO of the host MCU to control the Strapping pin level when the

module is powered on and released. After the reset is released, the Strapping pin has the same function as the normal pin.

Please refer to Table 2-4 for the detailed startup mode of configuring the Strapping pin:

Table 2-4 Strapping Pin Description

| Voltage of Internal LDO (VDD_SDIO)                               |           |                          |                          |                          |                          |
|------------------------------------------------------------------|-----------|--------------------------|--------------------------|--------------------------|--------------------------|
| PIN                                                              | Default   | 3.3V                     | 1.8V                     |                          |                          |
| MTDI                                                             | Pull-down | 0                        | 1                        |                          |                          |
| Bootting Mode                                                    |           |                          |                          |                          |                          |
| PIN                                                              | Default   | SPI Boot                 | Download Boot            |                          |                          |
| GPIO0                                                            | Pull-up   | 1                        | 0                        |                          |                          |
| GPIO2                                                            | Pull-down | Do not care              | 0                        |                          |                          |
| Enabling/Disabling Debugging Log Print over U0TXD During Booting |           |                          |                          |                          |                          |
| PIN                                                              | Default   | U0TXD Active             | U0TXD Silent             |                          |                          |
| MTDO                                                             | Pull-up   | 1                        | 0                        |                          |                          |
| Timing of SDIO Slave                                             |           |                          |                          |                          |                          |
| PIN                                                              | Default   | FE Sampling<br>FE Output | FE Sampling<br>RE Output | RE Sampling<br>FE Output | RE Sampling<br>RE Output |
| MTDO                                                             | Pull-up   | 0                        | 0                        | 1                        | 1                        |
| GPIO5                                                            | Pull-up   | 0                        | 1                        | 0                        | 1                        |

## NOTE

(1)FE: falling-edge, RE: rising-edge.

(2)Firmware can configure register bits to change the settings of “Voltage of Internal LDO (VDD\_SDIO)” and “Timing of SDIO Slave” after booting.

(3)Internal pull-up resistor (R9) for MTDI is not populated in the module, as the flash and SRAM in the module only support a power voltage of 3.3 V (output by VDD\_SDIO).

Figure 2.4 shows the setup time and hold time of the Strapping pin of the module EN (corresponding to the CHIP\_PU pin of the IC) before and after power-on. The description of each parameter is shown in Table 2-5.

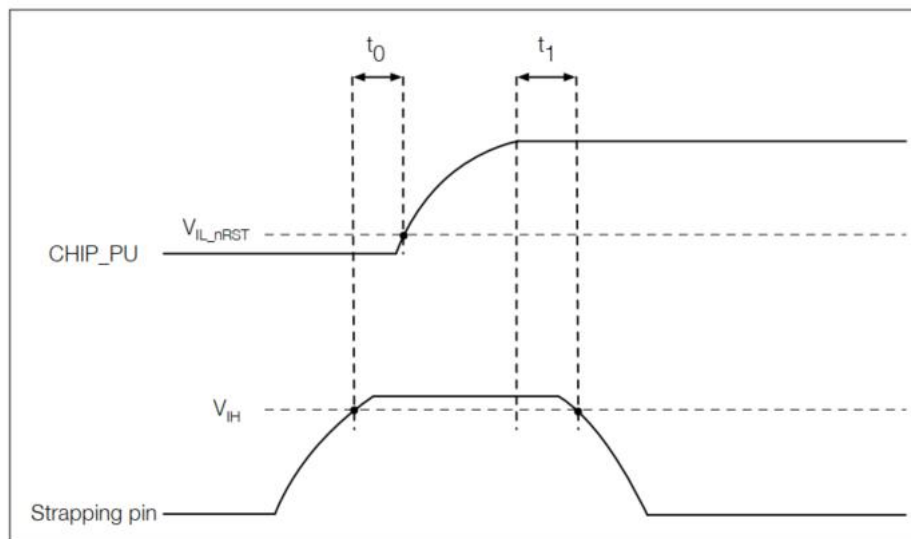


Figure 2.4 The setup time and hold time of the strapping pin

Table 2-5 Parameter description of the setup time and hold time of the Strapping pin

| Parameter | Description                                     | Min | Unit |
|-----------|-------------------------------------------------|-----|------|
| $t_0$     | Setup time before CHIP_PU goes from low to high | 0   | ms   |
| $t_1$     | Pull-down                                       | 1   | ms   |

## 2.9 Physical Dimensions

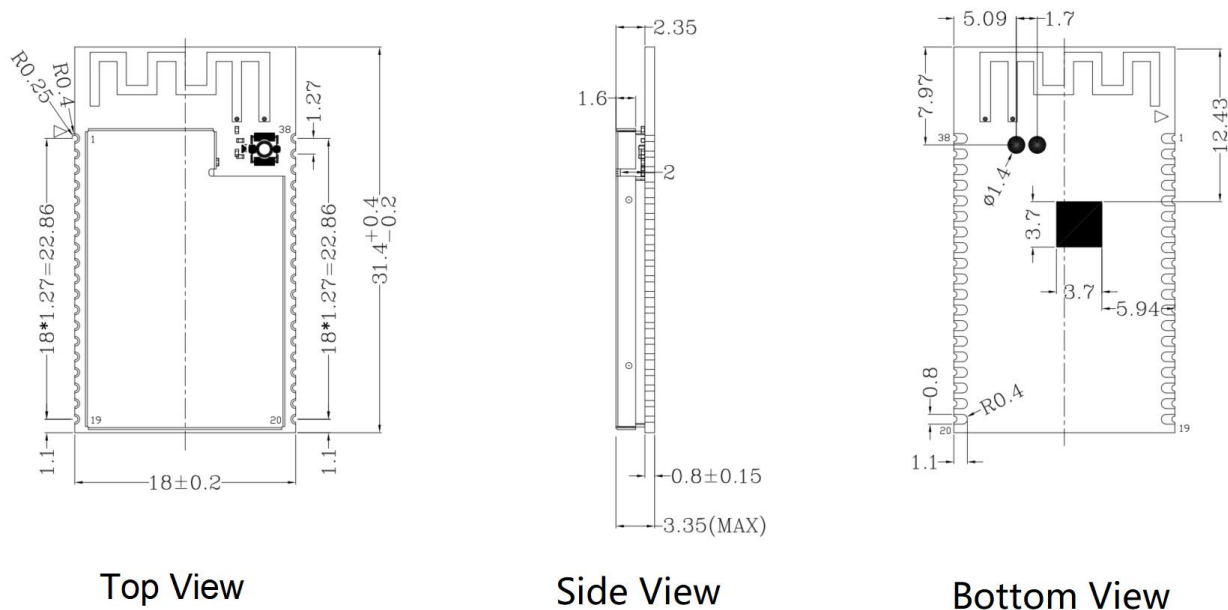


Figure 2.5 Dimensions of the module

## 2.10 Recommended schematic symbol and PCB package graphics

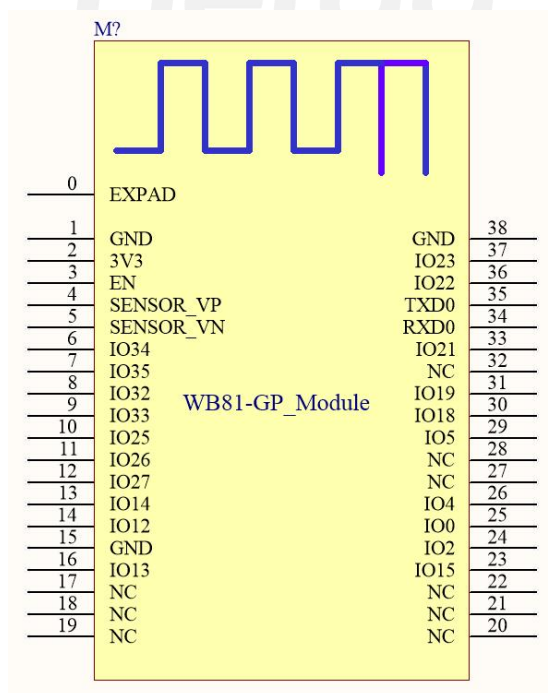
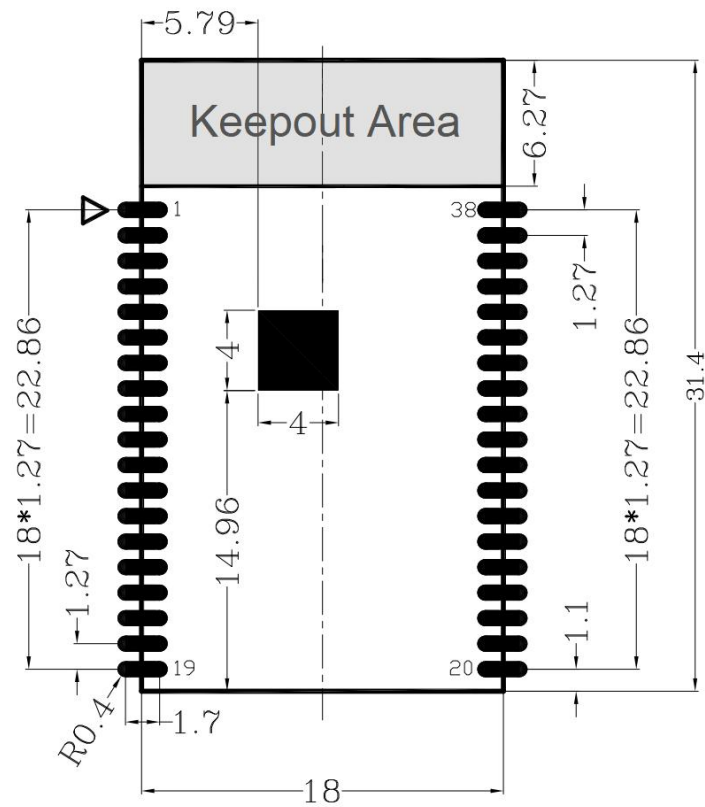


Figure 2.6 Schematic Symbol



### Figure 2.7 PCB Package Graphics

## 3 RF Characteristics

### 3.1 Wi-Fi RF Characteristics

Table 3-1 Module Wi-Fi RF Performance

| Parameter                                        | Content                                  |                                           |
|--------------------------------------------------|------------------------------------------|-------------------------------------------|
| Frequency Range                                  | 2400 MHz ~ 2483.5 MHz (2.4 GHz ISM Band) |                                           |
| Number of Channels                               | 2.4 GHz: Ch1 ~ Ch13                      |                                           |
| Modulation                                       | 802.11b                                  | DQPSK, DBPSK, CCK                         |
|                                                  | 802.11g/n (OFDM)                         | 64-QAM, 16-QAM, QPSK, BPSK                |
| Output Power                                     | 802.11b @ 1 Mbps                         | 19.5 dBm $\pm$ 2 dB @ EVM $\leq$ -10.5 dB |
|                                                  | 802.11b @11 Mbps                         | 19.5 dBm $\pm$ 2 dB @ EVM $\leq$ -15.5 dB |
|                                                  | 802.11g @ 6 Mbps                         | 17 dBm $\pm$ 2 dB @ EVM $\leq$ -5 dB      |
|                                                  | 802.11g @ 54 Mbps                        | 13 dBm $\pm$ 2 dB @ EVM $\leq$ -25dB      |
|                                                  | 802.11n @ MCS0 (20/40 M)                 | 17 dBm $\pm$ 2 dB @ EVM $\leq$ -5dB       |
|                                                  | 802.11n @ MCS7 (20/40 M)                 | 13 dBm $\pm$ 2 dB @ EVM $\leq$ -27dB      |
| Freq. Tolerance                                  | $\pm$ 20 ppm                             |                                           |
| Receive Sensitivity<br>(11b, 20 MHz)<br>@8% PER  | 1 Mbps                                   | PER @ -97 dBm, typical                    |
|                                                  | 11 Mbps                                  | PER @ -88 dBm, typical                    |
| Receive Sensitivity<br>(11g, 20 MHz)<br>@10% PER | 6 Mbps                                   | PER @ -92 dBm, typical                    |
|                                                  | 54 Mbps                                  | PER @ -75 dBm, typical                    |
| Receive Sensitivity<br>(11n, 20 MHz)<br>@10% PER | MCS0                                     | PER @ -92 dBm, typical                    |
|                                                  | MCS7                                     | PER @ -72 dBm, typical                    |
| Receive Sensitivity<br>(11n, 40 MHz)<br>@10% PER | MCS0                                     | PER @ -89 dBm, typical                    |
|                                                  | MCS7                                     | PER @ -69 dBm, typical                    |
| Adjacent channel rejection                       | 802.11g @ 6 Mbps                         | 27 dB, typical                            |
|                                                  | 802.11g @ 54 Mbps                        | 13 dB, typical                            |
|                                                  | 802.11n @ HT20, MCS0                     | 27 dB, typical                            |
|                                                  | 802.11n @ HT20, MCS7                     | 12 dB, typical                            |

Note: The module is powered by 3.3V and tested at 25°C.

## 3.2 BT RF Characteristics

### 3.2.1 BR+EDR Mode

Table 3-2 Module BR/EDR RF Performance

| Parameter                                            | Content                 |                  |
|------------------------------------------------------|-------------------------|------------------|
| Bluetooth Standard                                   | BR+EDR                  |                  |
| Frequency Range                                      | 2402 MHz ~ 2480 MHz     |                  |
| Channels                                             | BR/EDR: Ch0 ~ Ch78      |                  |
| Modulation                                           | BR (1M)                 | GFSK             |
|                                                      | EDR (2M)                | $\pi/4$ -DQPSK   |
|                                                      | EDR (3M)                | 8DPSK            |
| RF transmit power                                    | 0 dBm, typical          |                  |
| Gain control step                                    | 3 dB, typical           |                  |
| RF power control range                               | -12 ~ +9 dBm            |                  |
| Sensitivity @ BER=0.1% for GFSK (1 Mbps)             | -90 dBm, typical        |                  |
| Sensitivity @ BER=0.01% f or $\pi/4$ -DQPSK (2 Mbps) | -89 dBm, typical        |                  |
| Sensitivity @ BER=0.01% f or 8DPSK (3 Mbps)          | -82 dBm, typical        |                  |
| Maximum received signal @ 0.1%/0.01% BER             | GFSK (1 Mbps)           | 0 dBm, typical   |
|                                                      | $\pi/4$ -DQPSK (2 Mbps) | 0 dBm, typical   |
|                                                      | 8DPSK (3 Mbps)          | -15 dBm, typical |

## NOTE

The module is powered by 3.3V and tested at 25°C.

### 3.2.2 Bluetooth LE Mode

| Parameter                               | Content             |
|-----------------------------------------|---------------------|
| Bluetooth Standard                      | BT4.2               |
| Frequency Range                         | 2402 MHz ~ 2480 MHz |
| Channels                                | LE: Ch0 ~ Ch39      |
| Modulation                              | GFSK                |
| RF transmit power                       | 0 dBm, typical      |
| Gain control step                       | 3 dB, typical       |
| RF power control range                  | -12 ~ +9 dBm        |
| Sensitivity @ PER = 30.8% for LE(1Mbps) | -96 dBm, typical    |
| Maximum received signal@ 30.8% PER      | 0 dBm               |

#### NOTE

The module is powered by 3.3V and tested at 25°C.

### 3.3 Antenna area clearance design

When designing the upper board of the module, attention must be paid to the layout of the module on the bottom board, and the influence of the bottom board on the performance of the module PCB antenna should be minimized as much as possible. It is strongly recommended to place the module as close to the edge of the bottom board as possible. If conditions permit, the PCB antenna area should preferably extend out of the bottom board frame, and make the antenna feed point the closest to the half side. If there is a bottom plate under the antenna area, be sure to cut it off to minimize the impact of the bottom plate; ensure that interfering signals (such as USB, LCD, camera, power inductors, crystals, etc.) traces and vias are at least 10 mm away; If there are components with metal shells and high device heights near the module antenna area, a distance of more than 10 mm should be kept from the antenna area; when it comes to the design of the whole machine, the equipment shell (especially the material around the antenna) should be made of non-metallic materials Made, and keep at least 3 mm distance between the antenna and the housing, and please pay attention to the influence of the housing on the antenna. In Figure 3.1, positions (3) and (4) of the WB81-GP module on the backplane are strongly recommended, positions (1), (2), (5) and (6) are not recommended, especially position (5), the bottom plate will greatly attenuate the radiation capability of the antenna if the area of the module antenna is not cleared.

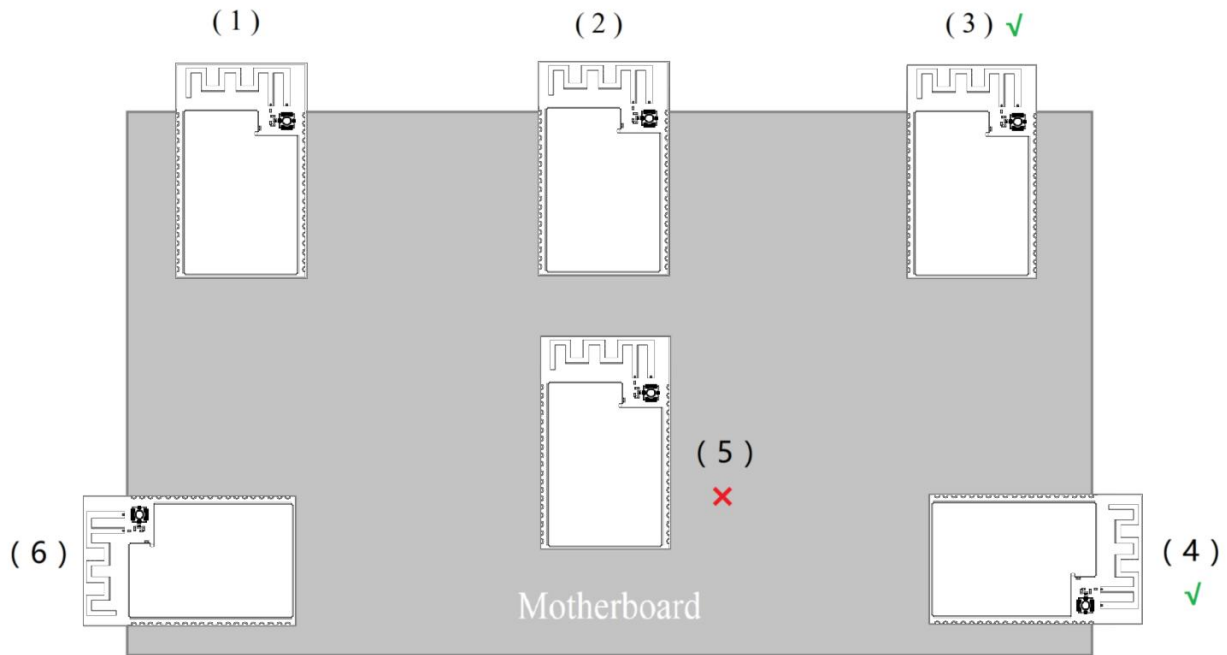


Figure 3.1 Schematic diagram of the position of the WB81-GP module on the bottom plate

If the above method is limited and cannot be implemented in an ideal situation, please ensure that the module is not wrapped by any metal casing, and the PCB antenna area of the module and the 15 mm extended area must be strictly clear, as shown in Figure 3.2:

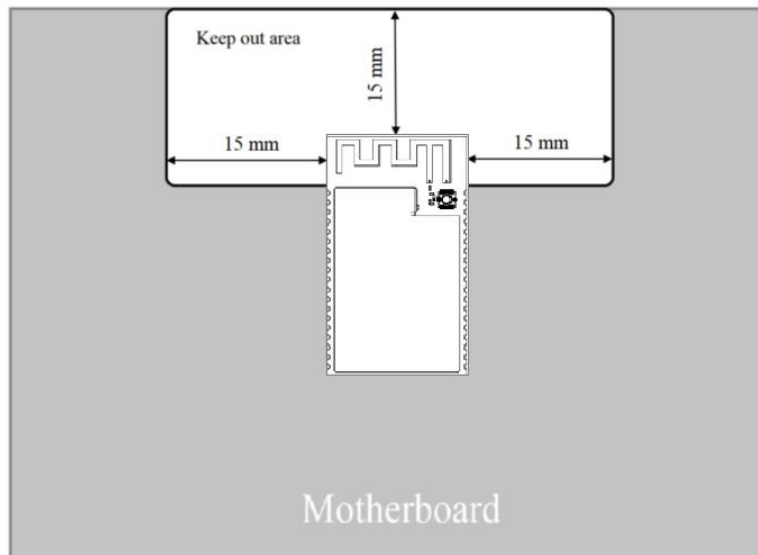


Figure 3.2 Schematic diagram of the clearance of the antenna area



## 4.2 Peripheral Pinout

Table 4-1 Module Peripheral Pinout Recommendations

| Interface    | Signal   | Pin    | Description                 |
|--------------|----------|--------|-----------------------------|
| ADC          | ADC2_CH0 | GPIO4  | 12-bit SAR ADC              |
|              | ADC2_CH1 | GPIO0  |                             |
|              | ADC2_CH2 | GPIO2  |                             |
|              | ADC2_CH3 | MTDO   |                             |
|              | ADC2_CH4 | MTCK   |                             |
|              | ADC2_CH5 | MTDI   |                             |
|              | ADC2_CH6 | MTMS   |                             |
|              | ADC2_CH7 | GPIO27 |                             |
|              | ADC2_CH8 | GPIO25 |                             |
|              | ADC2_CH9 | GPIO26 |                             |
| DAC          | DAC_1    | GPIO25 | Two 8-bit DACs              |
|              | DAC_2    | GPIO26 |                             |
| TOUCH Sensor | TOUCH0   | GPIO4  | Capacitive touch sensors    |
|              | TOUCH1   | GPIO0  |                             |
|              | TOUCH2   | GPIO2  |                             |
|              | TOUCH3   | MTDO   |                             |
|              | TOUCH4   | MTCK   |                             |
|              | TOUCH5   | MTDI   |                             |
|              | TOUCH6   | MTMS   |                             |
|              | TOUCH7   | GPIO27 |                             |
|              | TOUCH8   | 32K_XN |                             |
|              | TOUCH9   | 32K_XP |                             |
| JTAG         | MTDI     | MTDI   | JTAG for software debugging |
|              | MTCK     | MTCK   |                             |

|                                |           |               |                                                                                          |
|--------------------------------|-----------|---------------|------------------------------------------------------------------------------------------|
|                                | MTMS      | MTMS          |                                                                                          |
|                                | MTDO      | MTDO          |                                                                                          |
| SD/SDIO/MMC<br>Host Controller | HS2_CLK   | MTMS          | Supports SD memory card<br>V3.01 standard                                                |
|                                | HS2_CMD   | MTDO          |                                                                                          |
|                                | HS2_DATA0 | GPIO2         |                                                                                          |
|                                | HS2_DATA1 | GPIO4         |                                                                                          |
|                                | HS2_DATA2 | MTDI          |                                                                                          |
|                                | HS2_DATA3 | MTCK          |                                                                                          |
| SDIO/SPI Slave<br>Controller   | SD_CLK    | MTMS          | SDIO interface that conforms<br>to the industry standard SD<br>IO 2.0 card specification |
|                                | SD_CMD    | MTDO          |                                                                                          |
|                                | SD_DATA0  | GPIO2         |                                                                                          |
|                                | SD_DATA1  | GPIO4         |                                                                                          |
|                                | SD_DATA2  | MTDI          |                                                                                          |
|                                | SD_DATA3  | MTCK          |                                                                                          |
| UART                           | U0RXD_in  | Any GPIO Pins | Three UART devices with ha<br>rdware flow-control and DMA                                |
|                                | U0CTS_in  |               |                                                                                          |
|                                | U0SDR_in  |               |                                                                                          |
|                                | U0TXD_out |               |                                                                                          |
|                                | U0RTS_out |               |                                                                                          |
|                                | U0DTR_out |               |                                                                                          |
|                                | U1RXD_in  |               |                                                                                          |
|                                | U1CTS_in  |               |                                                                                          |
|                                | U1TXD_out |               |                                                                                          |
|                                | U1RTS_out |               |                                                                                          |
|                                | U2RXD_in  |               |                                                                                          |
|                                | U2CTS_in  |               |                                                                                          |
|                                | U2TXD_out |               |                                                                                          |
|                                | U2RTS_out |               |                                                                                          |

|                     |                    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------|--------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I2C                 | I2CEXT0_SCL_in     | Any GPIO Pins | Two I2C devices in slave or master mode                                                                                                                                                                                                                                                                                                                                                         |
|                     | I2CEXT0_SDA_in     |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | I2CEXT1_SCL_in     |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | I2CEXT1_SDA_in     |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | I2CEXT0_SCL_out    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | I2CEXT0_SDA_out    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | I2CEXT1_SCL_out    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | I2CEXT1_SDA_out    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
| LED PWM             | Ledc_hs_sig_out0~7 | Any GPIO Pins | 16 independent channels @ 80 MHz clock/RTC CLK. Duty accuracy: 16 bits                                                                                                                                                                                                                                                                                                                          |
|                     | Ledc_ls_sig_out0~7 |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
| General Purpose SPI | HSPIQ_in/_out      | Any GPIO Pins | <p>Standard SPI consists of clock, chip-select, MOSI and MISO. These SPIs can be connected to LCD and other external devices. They support the following features:</p> <ul style="list-style-type: none"> <li>● Both master and slave modes;</li> <li>● Four sub-modes of the SPI transfer format;</li> <li>● Configurable SPI frequency;</li> <li>● Up to 64 bytes of FIFO and DMA.</li> </ul> |
|                     | HSPID_in/_out      |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPICLK_in/_out    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPI_CS0_in/_out   |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPI_CS1_out       |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPI_CS2_out       |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | VSPIQ_in/_out      |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | VSPID_in/_out      |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | VSPICLK_in/_out    |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | VSPI_CS0_in/_out   |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | VSPI_CS1_out       |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | VSPI_CS2_out       |               |                                                                                                                                                                                                                                                                                                                                                                                                 |
| Parallel QSPI       | HSPICLK            | MTMS          | Supports Standard SPI, Dual SPI, and Quad SPI that can be connected to the external flash and SRAM                                                                                                                                                                                                                                                                                              |
|                     | HSPICS0            | MTDO          |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPIQ              | MTDI          |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPID              | MTCK          |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPIHD             | GPIO4         |                                                                                                                                                                                                                                                                                                                                                                                                 |
|                     | HSPIWP             | GPIO2         |                                                                                                                                                                                                                                                                                                                                                                                                 |

|      |                 |               |                                                              |
|------|-----------------|---------------|--------------------------------------------------------------|
|      | VSPICLK         | GPIO18        |                                                              |
|      | VSPICS0         | GPIO5         |                                                              |
|      | VSPIQ           | GPIO19        |                                                              |
|      | VSPID           | GPIO23        |                                                              |
|      | VSPIHD          | GPIO21        |                                                              |
|      | VSPIWP          | GPIO22        |                                                              |
| EMAC | EMAC_TX_EN      | GPIO21        | Ethernet MAC with RMI Interface                              |
|      | EMAC_TXD0       | GPIO19        |                                                              |
|      | EMAC_TXD1       | GPIO22        |                                                              |
|      | EMAC_RXD0       | GPIO25        |                                                              |
|      | EMAC_RXD1       | GPIO26        |                                                              |
|      | CRS_DV          | GPIO27        |                                                              |
|      | REF_CLK         | GPIO0         |                                                              |
|      | EMAC_MDC        | GPIO23        |                                                              |
|      | EMAC_MDIO       | GPIO18        |                                                              |
|      | EMAC_RST        | GPIO5         |                                                              |
| TWAI | Twai_rx         | Any GPIO Pins | Compatible with ISO 11898-1 protocol (CAN Specification 2.0) |
|      | Twai_tx         |               |                                                              |
|      | Twai_bus_off_on |               |                                                              |
|      | Twai_clkout     |               |                                                              |

### 4.3 Backplane Layout Considerations

There is no high-speed signal or sensitive signal routing on the BOTTOM layer of the WB81-GP module, but it is recommended to design the routing on the TOP layer of the bottom board to avoid the module to avoid unexpected factors.

There are not too many hollowing-out processing requirements in the design of the bottom board. In addition to the clearance requirements for the antenna area mentioned above, the bottom board can be used for almost the entire board copper laying, but it must be noted that the test point pads of the module BOTTOM layer need to be exposed due to the window opening. For avoidance treatment, no via holes or exposed copper should be placed in the corresponding position of the bottom plate, and it should be covered with solder resist oil to prevent short-circuiting. WB81-GP module BOTTOM layer window exposed copper area is shown in Figure 4.2:

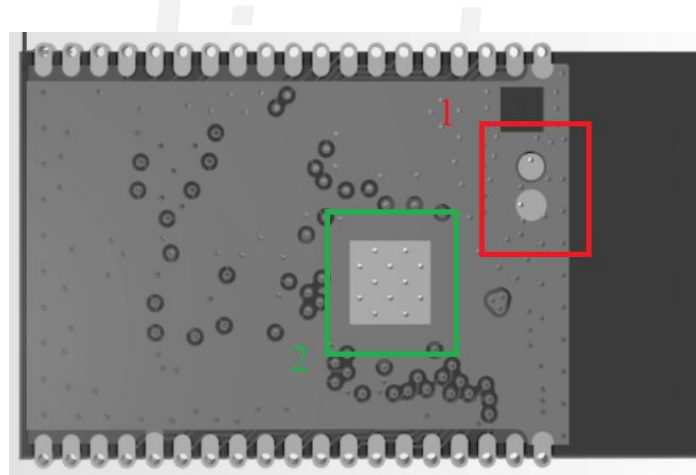


Figure 4.2 WB81-GP module BOTTOM layer open window schematic diagram of exposed copper area

The exposed copper points in the area 1 marked by the red box are RF test points, and the positions mapped to the backplane area must not have any traces or exposed copper.

Area 2 marked by the green box is the heat dissipation pad EXPAD (connected to GND) under the chip on the back of the module. The area is fully connected to the ground plane of other layers to improve thermal conductivity; when connecting to the ground plane of the

same layer, the cross connection method (Direct Connect should be selected) cannot be selected for copper plating. The effect of the cross connection is shown in Figure 4.3, and the heat will pass through Conduction accumulates on the copper-clad block in the middle, resulting in excessive local temperature; in addition, it should be noted that the exposed copper area is generally not tinned, but an appropriate amount of tin can optimize the heat conduction effect of the bottom plate (excessive tin may lead to mold Floating height and false soldering when soldering and pasting, and tin leakage through holes, etc.): If EXPAD is a whole piece of rectangular window opening method, the via holes must be half-plugged to avoid tin leakage; a more recommended optimization method is Make the EXPAD on the bottom plate into a nine-square pattern, as shown in Figure 4.4, cover the gap with ink, and drill the ground hole in the gap, which can effectively improve the problem of tin leakage.。



Figure 4.3 Copper connection not recommended



Figure 4.4 The nine-square grid method of the floor EXPAD

## 5 Electrical Performance and Reliability

### 5.1 Electrical Characteristics

Table 5-1 Module Electrical Characteristics

| SYMBOL               | DESCRIPTION                                                   | MIN      | TYP. | Max      | Unit |
|----------------------|---------------------------------------------------------------|----------|------|----------|------|
| V <sub>DD</sub>      | Absolute Maximum power supply voltage                         | -0.3     | -    | 3.6      | V    |
|                      | Recommended Power Supply                                      | 3.0      | 3.3  | 3.6      | V    |
| I <sub>VDD</sub>     | Current delivered by external power supply                    | 0.5      | -    | -        | A    |
| I <sub>output</sub>  | Cumulative IO output current                                  | -        | -    | 1100     | mA   |
| V <sub>IL</sub>      | Low Level Input Voltage                                       | -0.3     | -    | 0.25×VDD | V    |
| V <sub>IH</sub>      | High Level Input Voltage                                      | 0.75×VDD | -    | VDD+0.3  | V    |
| I <sub>IL</sub>      | Low-level input current                                       | -        | -    | 50       | nA   |
| I <sub>IH</sub>      | High-level input current                                      | -        | -    | 50       | nA   |
| V <sub>OL</sub>      | Low-level output voltage                                      | 0.8×VDD  | -    | -        | V    |
| V <sub>OH</sub>      | High-level output voltage                                     | -        | -    | 0.1×VDD  | V    |
| R <sub>PU</sub>      | Resistance of internal pull-up resistor                       | -        | 45   | -        | KΩ   |
| R <sub>PD</sub>      | Resistance of internal pull-down resistor                     | -        | 45   | -        | KΩ   |
| V <sub>IL_nRST</sub> | Low-level input voltage of EN (Chip_PU) to power off the chip | -        | -    | 0.6      | V    |
| T <sub>A</sub>       | Operating temperature                                         | -40      | -    | +85      | ℃    |
| T <sub>Store</sub>   | Storage temperature                                           | -40      | -    | +105     | ℃    |
| V <sub>ESD</sub>     | VDD & ANT PIN ESD performance                                 | -        | 4    | -        | KV   |

### 5.2 Power Consumption

Table 5-2 Module RF Power Consumption Description

| Description |                                             | Max Current @ TX | Max Current @ RX |
|-------------|---------------------------------------------|------------------|------------------|
| WIFI        | 802.11b, 11 Mbps @ 19.5 dBm, 50% duty cycle | 250 mA           | 120 mA           |
|             | 802.11b, 11 Mbps @ 19.5 dBm, 10% duty cycle | 145 mA           |                  |

|    |                                              |        |        |
|----|----------------------------------------------|--------|--------|
|    | 802.11g, 54 Mbps @ 14 dBm, 50% duty cycle    | 195 mA |        |
|    | 802.11g, 54Mbps @ 14 dBm, 10% duty cycle     | 135 mA |        |
|    | 802.11n, HT20, MCS0 @ 17 dBm, 50% duty cycle | 225 mA |        |
|    | 802.11n, HT20, MCS0 @ 17 dBm, 10% duty cycle | 145 mA |        |
|    | 802.11n, HT20, MCS7 @ 14 dBm, 50% duty cycle | 190 mA |        |
|    | 802.11n, HT20, MCS7 @ 14 dBm, 10% duty cycle | 135 mA |        |
|    | 802.11n, HT40, MCS0 @ 16 dBm, 10% duty cycle | 145 mA |        |
|    | 802.11n, HT40, MCS7 @ 14 dBm, 10% duty cycle | 140 mA |        |
| BT | BR @ DH5, default power (0 dBm)              | 145 mA | 120 mA |
|    | BR @ DH5, max power (9 dBm)                  | 190 mA |        |
|    | EDR @ 2-DH5, default power (0 dBm)           | 145 mA |        |
|    | EDR @ 2-DH, max power (9 dBm)                | 190 mA |        |
|    | EDR @ 3-DH5 default power (0 dBm)            | 145 mA |        |
|    | EDR @ 3-DH5 max power (9 dBm)                | 190 mA |        |
|    | BLE @ 1M, default power (0 dBm)              | 150 mA |        |
|    | BLE @ 1M, max power (9 dBm)                  | 195 mA |        |

## NOTE

(1) Test conditions: VDD: 3.3V, Temp: 25° C, Product: L-WFIWB81-G5PP4.

(2) The power consumption data may vary under different firmware versions, and the actual test shall prevail.

Table 5-3 Module low power consumption performance

| Mode         |        | Typ. | Unit | Test instruction                                                     |
|--------------|--------|------|------|----------------------------------------------------------------------|
| Deep sleep   |        | 5.47 | μA   | AT+GSLP=10000                                                        |
| System sleep | Dtim 1 | 8.02 | mA   | AT+CWMODE=1<br>AT+CWJAP="wifi_ax_test","12345678",,,,1<br>AT+SLEEP=2 |
|              | Dtim 3 | 4.48 |      | AT+CWMODE=1<br>AT+CWJAP="wifi_ax_test","12345678",,,,3               |

|  |         |      |                                                                       |
|--|---------|------|-----------------------------------------------------------------------|
|  |         |      | AT+SLEEP=2                                                            |
|  | Dtim 5  | 3.87 | AT+CWMODE=1<br>AT+CWJAP="wifi_ax_test","12345678",,,,5<br>AT+SLEEP=2  |
|  | Dtim 10 | 3.31 | AT+CWMODE=1<br>AT+CWJAP="wifi_ax_test","12345678",,,,10<br>AT+SLEEP=2 |
|  | Dtim 30 | 2.90 | AT+CWMODE=1<br>AT+CWJAP="wifi_ax_test","12345678",,,,30<br>AT+SLEEP=2 |

## NOTE

(1)Test conditions: VDD: 3.3V, Temp: 25° C, product: L-WFIWB81-G5PP4.

(2)The power consumption data may vary under different firmware versions, and the actual test shall prevail.

**Lierda**  
利 尔 达

## 6 Production and Packaging Information

### 6.1 Production Welding

#### 6.1.1 Production Instructions

It is recommended to use SMT machine to mount the stamp mouth packaging module, and the mounting should be completed within 24 hours after unpacking, otherwise, it should be vacuum-packed again to avoid moisture and poor mounting.

If the package contains a humidity indicator card, it is recommended to judge whether the module needs to be baked according to the humidity card. The conditions for baking are as follows:

Baking temperature:  $125^{\circ}\text{C}\pm 5^{\circ}\text{C}$ ;

The alarm temperature is set to  $130^{\circ}\text{C}$ ;

After cooling  $<36^{\circ}\text{C}$  under natural conditions, SMT patching can be carried out;

If the unpacking time exceeds 3 months, you need to pay special attention to whether the product is damp. Because of the PCB immersion gold process, more than 3 months may cause oxidation of the pads, which may cause problems such as virtual soldering and missing soldering during placement.

In order to ensure the qualified rate of reflow soldering, it is recommended to select 10% of the products for visual inspection and AOI inspection for the first placement, so as to ensure the rationality of furnace temperature control, device adsorption method and placement method.

Operators at each station must wear electrostatic gloves during the whole production process.

### 6.1.2 Module location requirements on the backplane

It is recommended that the thickness of the green oil at the position of the module on the bottom plate be less than 0.02mm to avoid excessive thickness, and the raised module cannot effectively contact the solder paste and affect the soldering quality. In addition, it is necessary to consider that other devices cannot be placed within 2mm around the interface board module to ensure the maintenance of the module.

### 6.1.3 Stencil Opening Design

In principle, the thickness of the stencil on the bottom plate is selected based on the comprehensive consideration of the package type of the device on the board. The following requirements need to be focused on:

The pad position of the module can be partially thickened to 0.15~0.20mm to avoid empty soldering.

### 6.1.4 Production Notes

- During the production process, each operator must wear electrostatic gloves;
- Do not exceed the specified baking time when baking;
- It is strictly forbidden to add explosive, flammable and corrosive substances during baking;
- When baking, the modules should be placed in a high-temperature tray to keep the air circulation between the modules;
- When baking, the oven door must be closed to ensure that the oven is closed to prevent temperature leakage;
- Try not to open the door when the oven is running. If it must be opened, try to shorten the time for opening the door;
- After baking, wait for the module to cool naturally below 36° C before taking it out with electrostatic gloves to avoid burns;

- During operation, strictly prevent the bottom surface of the module from getting water or dirt;

### 6.1.5 Recommended Reflow Profile

Note: This work guide is only suitable for lead-free work and is for reference only.

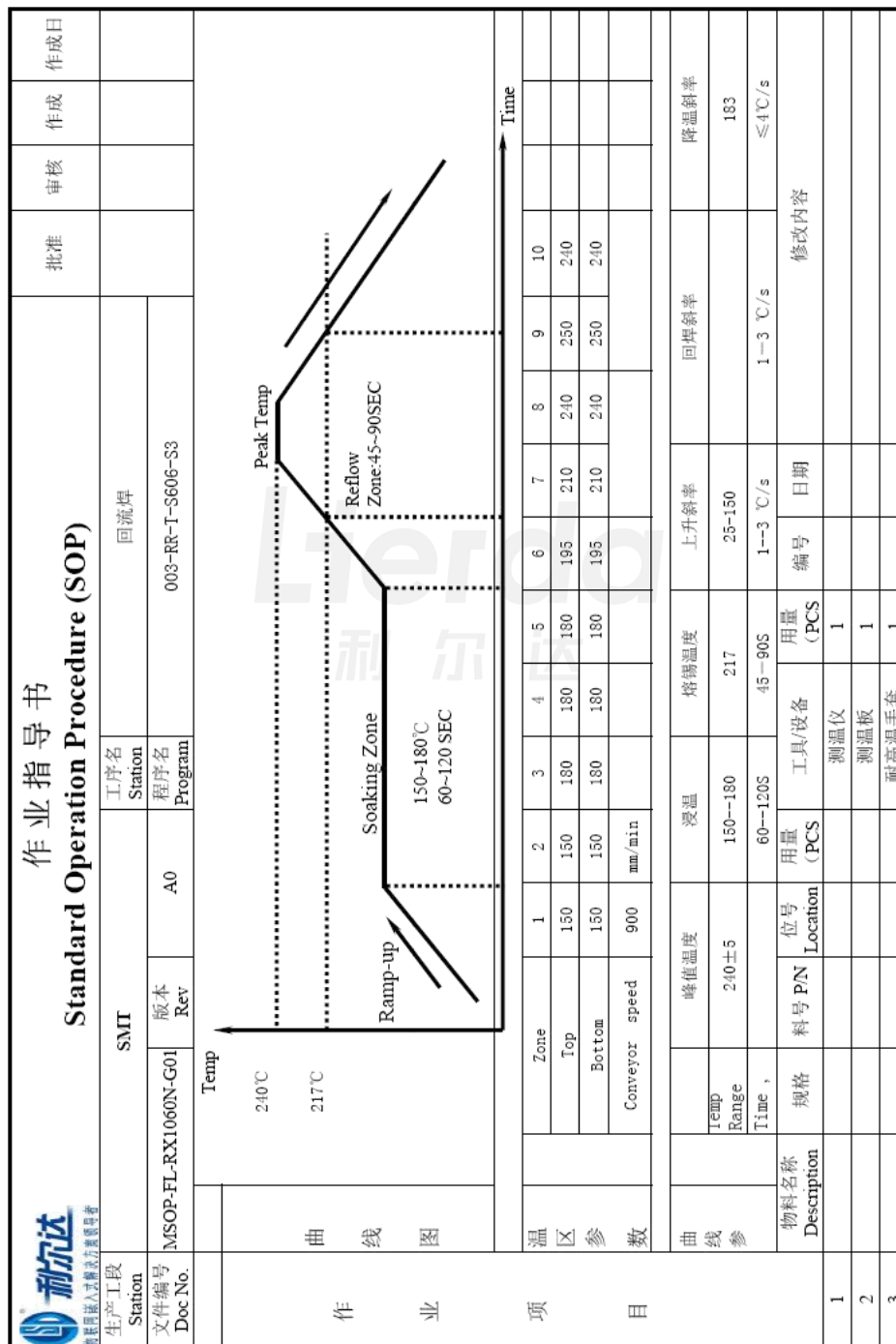


Figure 6-1 Reflow Soldering Operation Instructions

Company Address: Lierda Internet of Things Technology Park, No. 1326 Wenyi West Road, Hangzhou

Tel: 0571-88800000

## 6.2 Package Information

### 6.2.1 Packaging Method

| Model Name      | Packing Method | Packing Case (pcs) | MPQ(pcs) | Reels per Case |
|-----------------|----------------|--------------------|----------|----------------|
| L-WFIWB81-G5PP4 | Tape and Reel  | 4000               | 800      | 5              |

### 6.2.2 Carrier Size Detail

Schematic diagram of the placement direction of the tape and reel packaging module:

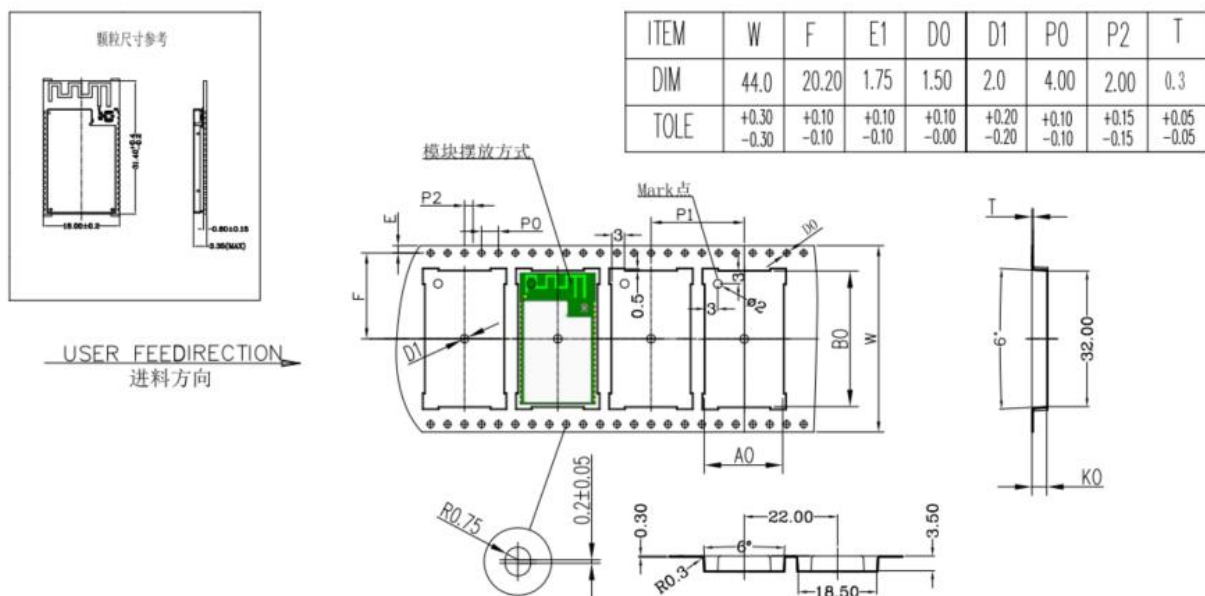


Figure 6.2 Carrier size and product orientation

## Conformity

### **FCC regulatory conformance :**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two

conditions:

- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

NOTE: The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications to this equipment. Such modifications could void the user's authority to operate the equipment.

### **FCC Radiation Exposure Statement:**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

---

## ORIGINAL EQUIPMENT MANUFACTURER (OEM) NOTES

The OEM must certify the final end product to comply with unintentional radiators (FCC Sections 15.107 and 15.109) before declaring compliance of the final product to Part 15 of the FCC rules and regulations. Integration into devices that are directly or indirectly connected to AC lines must add with Class II Permissive Change.

The OEM must comply with the FCC labeling requirements. If the module's label is not visible when installed, then an additional permanent label must be applied on the outside of the finished product which states: "Contains transmitter module FCC ID: **2AOFDL-WFIWB81**". Additionally, the following statement should be included on the label and in the final product's user manual: "This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interferences, and
- (2) this device must accept any interference received, including interference that may cause undesired operation."

The module is limited to installation in mobile or fixed applications. Separate approval is required for all other operating configurations, including portable configuration with respect to Part 2.1093 and different antenna configurations.

A module or modules can only be used without additional authorizations if they have been tested and granted under the same intended end - use operational conditions, including simultaneous transmission operations. When they have not been tested and granted in this manner, additional testing and/or FCC application filing may be required. The most straightforward approach to address additional testing conditions is to have the grantee responsible for the certification of at least one of the modules submit a permissive change application. When having a module grantee file a permissive change is not practical or feasible, the following guidance provides some additional options for host manufacturers. Integrations using modules where additional testing and/or FCC application filing(s) may be required are: (A) a module used in devices requiring additional RF exposure compliance information (e.g., MPE evaluation or SAR testing); (B) limited and/or split modules not meeting all of the module requirements; and (C) simultaneous transmissions for independent collocated transmitters not previously granted together.

This Module is full modular approval, it is limited to OEM installation ONLY.

Integration into devices that are directly or indirectly connected to AC lines must add with Class II Permissive Change. (OEM) Integrator has to assure compliance of the entire end product include the integrated Module. Additional measurements (15B) and/or equipment authorizations (e.g. Verification) may need to be addressed depending on co-location or simultaneous transmission issues if applicable. (OEM) Integrator is reminded to assure that these installation instructions will not be made available to the end user

---

## Requirement per KDB996369 D03

### 2.2 List of applicable FCC rules

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.<sup>3</sup>

**Explanation:** This module meets the requirements of FCC part 15C(15.247).

### 2.3 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users, then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

**Explanation:** The EUT has a PCB Antenna, and the antenna use a permanently attached antenna which is not replaceable.

### 2.4 Limited module procedures

If a modular transmitter is approved as a "limited module," then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval.

This limited module procedure is also applicable for RF exposure evaluation when it is necessary to demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

**Explanation:** The module is not a limited module.

---

## 2.5 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects:

layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

- a) Information that includes permitted variances (e.g., trace boundary limits, thickness, length, width, shape(s), dielectric constant, and impedance as applicable for each type of antenna);
- b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency, the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered);
- c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;
- d) Appropriate parts by manufacturer and specifications;
- e) Test procedures for design verification; and
- f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

**Explanation:** Yes, The module with trace antenna designs, and This manual has been shown the layout of trace design, antenna, connectors, and isolation requirements.

## 2.6 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information: (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person's body); and (2) additional text needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

**Explanation:** This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the FCC statement, FCC ID is: 2AOFDL-WFIWB81.

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## 2.7 Antennas

A list of antennas included in the application for certification must be provided in the instructions. For modular transmitters approved as limited modules, all applicable professional installer instructions must be included as part of the information to the host product manufacturer. The antenna list shall also identify the antenna types (monopole, PIFA, dipole, etc. (note that for example an “omni-directional antenna” is not considered to be a specific “antenna type”)).

For situations where the host product manufacturer is responsible for an external connector, for example with an RF pin and antenna trace design, the integration instructions shall inform the installer that unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturers shall provide a list of acceptable unique connectors.

**Explanation:** The EUT has a PCB Antenna, and the antenna use a permanently attached antenna which is unique.

## 2.8 Label and compliance information

Grantees are responsible for the continued compliance of their modules to the FCC rules. This includes advising host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID” with their finished product. See Guidelines for Labeling and User Information for RF Devices – KDB Publication 784748.

**Explanation:** The host system using this module, should have label in a visible area indicated the following texts: “Contains FCC ID:2AOFDL-WFIWB81”

## 2.9 Information on test modes and additional testing requirements<sup>5</sup>

Additional guidance for testing host products is given in KDB Publication 996369 D04 Module Integration Guide. Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

The grantee should provide information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or other transmitters in a host.

Grantees can increase the utility of their modular transmitters by providing special means, modes, or instructions that simulates or characterizes a connection by enabling a transmitter. This can greatly simplify a host manufacturer’s determination that a module as installed in a host complies with FCC requirements.

**Explanation:** Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.

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## 2.10 Additional testing, Part 15 Subpart B disclaimer

The grantee should include a statement that the modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

**Explanation:** The module without unintentional-radiator digital circuitry, so the module does not require an evaluation by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.