1 Introduction

SH-BLEM01 is a Bluetooth low energy module designed by Sino Wealth. This module is based on SH87F8801 BLE single chip solution, which intergrates a ultra low power Bluetooth transceiver and a high performance low power 32 bit microprocessor. It also contains a Bluetooth low energy protocol stack, supports all of the BLE applications.

1.1 Features

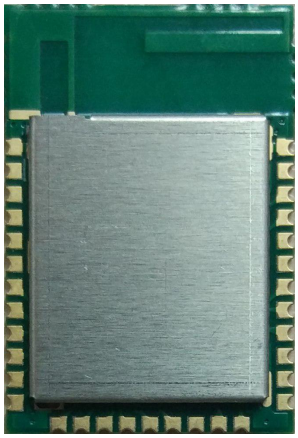
BLE:

- Frequency range: 2.400~2.4835GHz
- Bluetooth 4.2 specification certification
- Receive Sensitivity = -87 dBm @ 1.0 Mbps
- Output power range: -20 ~ +2 dBm
- Ultra low power consumption:
- 16.5 mA @ Receive
- 13.4 mA @ +2 dBm Transmit
- 12.1 mA @ 0 dBm Transmit
- 10.1 mA @ -6 dBm Transmit
- Data Rate = 1 Mbps

- Andes 32-bit CPU core
- 26 MHz maximum frequency
- Flash ROM: 128KB
- SRAM: 17KB
- 30 GPIO, with interrupt function
- 1 SPI, 1 I2C, 2 EUARTs
- 4 Times, 3 PWMs, 1 RTC
- 12bit x 10ch ADC
- Segment LCD driver:
  4COM×20SEG (1/4Duty,1/3 Bias)
  5COM×19SEG (1/5Duty,1/3 Bias)
  6COM×18SEG (1/6Duty,1/3 Bias)
- Serial two wire debug interface
- Deep Sleep Mode（3uA）
- Power Down Mode（0.3uA）

MCU:
Module:

- Single power supply: 1.9V~3.6V
- Small size: 16×23.5 mm, Height: 1.8 mm
- high performance 2.4GHz inverted F antenna
- 33 pins, stamp half hole package



1.2 Applications

- Wireless keyboard, mouse
- Fitness
- Wearable products
- Smart home

Revison history

Version	Date	Content
1.0	2015.11.11	Initial
1.1	2016.03.18	Modify features ,DC/AC parameters and dimension of module
1.2	2016.04.18	Add Module internal BOM
1.3	2017.12.20	Add metal shieding&FCC warning

FCC warning

Compliance Information:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: 1. This device may not cause harmful interference, 2. This device must accept any interference received, including interference that may cause undesired operation. Any changes or modifications to this device not expressly approved by SINO WEALTH ELECTRONIC LTD. For compliance could void the user's authority to operate the equipment.

Note:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced technician for help.

If the module's FCC ID is not visible when installed in the host, or if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: “Contains Transmitter Module FCC ID: 2AOT2SH-BLEM01” or “Contains FCC ID: 2AOT2SH-BLEM01” must be used.

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2 Description

2.1 block diagram

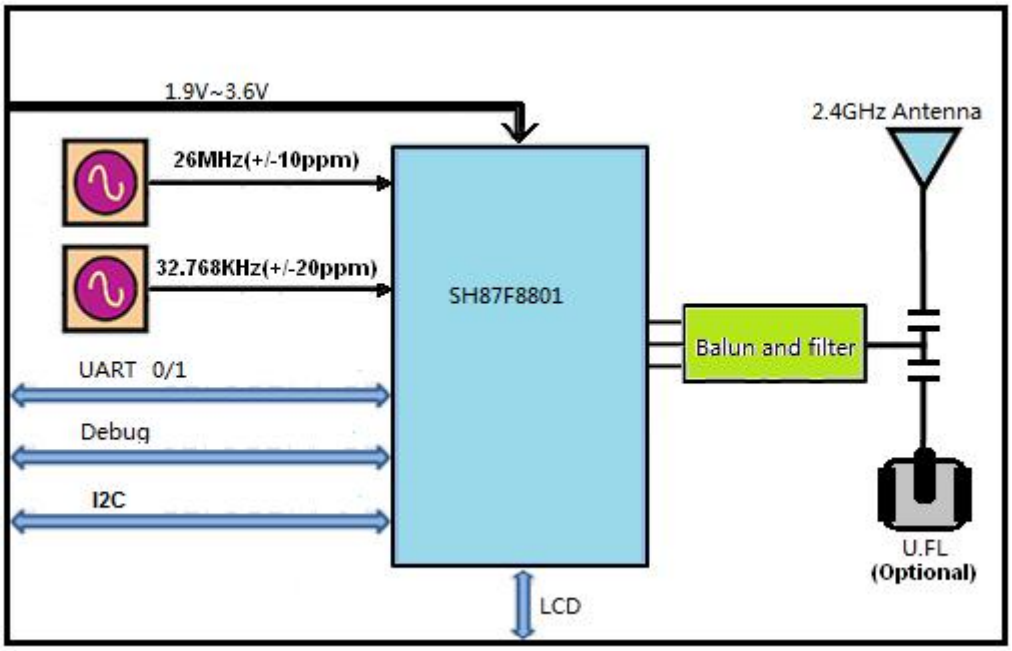

Figure 1. SH-BLEM01 module diagram

2.2 Pin assignment

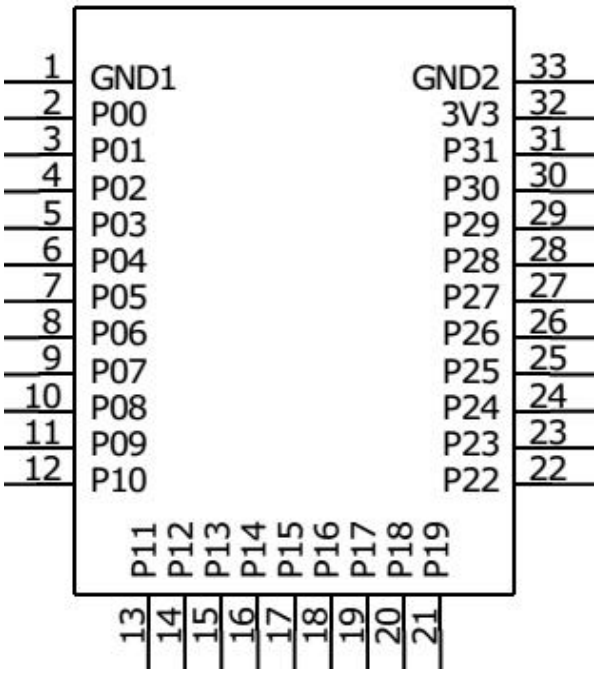

Figure 2. Module pin assignment

Pin #	Name	Type	Description

1,33	GND	POWER	Ground
2	P00	I/O	P00/SEG0/SCK
3	P01	I/O	P01/SEG1/MOSI
4	P02	I/O	P02/SEG2/MISO
5	P03	I/O	P03/SEG3/SS
6	P04	I/O	P04/SEG4/RXD0/SDA
7	P05	I/O	P05/SEG5/TXD0/SCL
8	P06	I/O	P06/SEG6/RXD1
9	P07	I/O	P07/SEG7/TXD1
10	P08	I/O	P08/ SEG8/PWM0
11	P09	I/O	P09/SEG9/PWM1
12	P10	I/O	P10/SEG10/PWM2
13	P11	I/O	P11/SEG11
14	P12	I/O	P12/SEG12
15	P13	I/O	P13/SEG13/RSTN
16	P14	I/O	P14/SEG14/TCK
17	P15	I/O	P15/SEG15/TDA
18,	P16	I/O	P16/SEG16/T2EX
19	P17	I/O	P17/SEG17/T2
20	P18	I/O	P18/SEG18/COM5
21	P19	I/O	P19/SEG19/COM4
22	P22	I/O	P22/COM3/AIN9
23	P23	I/O	P23/COM2/AIN8
24	P24	I/O	P24/COM1/AIN7
25	P25	I/O	P25/COM0/AIN6
26	P26	I/O	P26/AIN5
27	P27	I/O	P27/AIN4
28	P28	I/O	P28/AIN3
29	P29	I/O	P29/AIN2
30	P30	I/O	P30/AIN1
31	P31	I/O	P31/AIN0/VREF
32	3V3	POWER	Power supply

Table 1. Module pin definition

3 Funciton overview

3.1 GPIO

- Built in pull up and pull down resistor.
- If GPIO used as an input, it supports external interrupt and its trigger mode can be configured.
- P13/P14/P15/P26 can wake up chip from sleep mode.

3.2 PWM

- 3 PWMs，cycle and duty can be configured independently
- Each PWM supports an independent cycle overflow interrupt
- Output plarity can be configured

3.3 EUART

Two enhanced universal asynchronous receiver transmitter(EUART)，can be used for standard two wire UART communication.

- Baud rate generator
- Supports automatic address recognition and address broadcast
- Support frame error detection
- Support four kinds work modes

3.4 RTC

- Registers for sub second(1/256 second), second, minute, day, week, month and year
- Day register for automatic cross month and leap year adjustment
- Alarm function
- Can wake up chip from DSM mode

3.5 SPI

- Support master/slave mode
- Polarity and phase can be configured for synchronous clocks, support, support four modes: 0~3
- Frequency of synchronous clock can be configure
- MSB or LSB priority

3.6 LCDC(Segment LCD interface)

- Support contrast adjustment
- Support duty adjustment：
  - 1/4 Duty，1/3Bias，20 segment
  - 1/5 Duty，1/3Bias，19 segment

- 1/6Duty，1/3Bias，18 segment

3.7 TWI

- Two wire，comatible with I^2C protocol
- Support master/slave mode
- Arbitration for multi host communication
- Low level bus timeout detection
- Wake up system in idle mode
- Address programmable
- Built in pull up resistor

3.8 ADC

- One 12 bit ADC
- Optional internal or external reference voltage
- 10 analog input channel, An internal 1.2V reference voltage

3.9 BLE

- Frequency range: 2.400~2.4835 GHz
- Receive Sensitivity = -87 dBm @ 1.0 Mbps
- Output power range: -20 ~ +3 dBm
- Ultra low power consumption:

  -16.5 mA @ Receive

  -13.4 mA @ +2 dBm Transmit

  -12.1 mA @ 0 dBm Transmit

  -10.1 mA @ -6 dBm Transmit
- Data Rate = 1 Mbps

4 Electical characters

4.1 Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage			3.6	V
VIN (Input Voltage)	1.9		3.6	V
Operating Temperature	-40		85	℃
Storage Temperature	-40		125	℃

Table 2. Absolute Maximum Ratings

4.2 DC Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{DD}	Supply voltage	1.9	3.0	3.6	V
Current Consumption	$I_{POWERDOWN}$	Power down current	-	0.2	0.3	μA
	I_{deep_sleep}	RC32K active	-	3	6	μA
		RC32K off	-	2	4	μA
	I_{sleep}	X26MHz active, Sysclk=1MHz core/buffers are active	-	0.8	-	mA

Table 1. DC Electrical Specifications

4.3 Synthesizer Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency Range	F_{SYN}		2400	-	2483.5	MHz
Frequency Resolution	F_{RES}		-	400	-	Hz
Reference Frequency	F_{REF}		-	26	-	MHz
Reference Frequency tolerance	F_{TOL}		-	-	±40	ppm
Synthesizer Settling Time	t_{LOCK}		-	-	30	μs
Synthesizer Wake up Time	$T_{WAKE-UP}$	Including references, calibrations and synthesizer lock	-	-	80	μs
Phase Noise at offset	$L_{\Phi}(f_M)$	ΔF = 1 MHz	-	-106	-	dBc/Hz
	$L_{\Phi}(f_M)$	ΔF = 2 MHz	-	-111	-	dBc/Hz
	$L_{\Phi}(f_M)$	ΔF = 3 MHz	-	-114	-	dBc/Hz

RMS Phase Error	Φ_{RMS}	Integrated from 1kHz to 13MHz	-	2.0	-	Deg

Table 2. Synthesizer Electrical Specifications

4.4 Transmitter Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
TX Frequency Range	F_{TX}	World Wide	2400	-	2483.5	MHz
FSK Data Rate	DR_{FSK}		-	1.0	-	Mbps
Modulation Deviation	Δf			250		kHz
20dB signal bandwidth (1Mbps)	BW_{20dB}			0.95	1.2	MHz
Output Power Range	P_{TX}		-20	-	+2	dBm
Current Consumption	I_{TX2}	Supply current @ +2dBm	-	13.4	-	mA
	I_{TX0}	Supply current @ 0dBm	-	12.1	-	mA
	I_{TX-6}	Supply current @ -6dBm	-	10.1	-	mA
TX RF Output Steps	ΔP_{TX-OUT}	Controlled by 3bits	-	2	-	Db
TX Power Variation vs. Temperature	$\Delta P_{TX-TEMP}$	-40 to +85 ºC	-	±0.5	-	Db
TX Power Variation vs. VDD	ΔP_{TX-VDD}	From 1.9 to 3.6V	-	±1	-	Db
TX Power Variation vs. Frequency	$\Delta P_{TX-FREQ}$	Measured across any frequency band (2400–2483.5 MHz)	-	±1	-	Db
Transmit Modulation Filtering	BT	Gaussian filter bandwidth time product	-	0.5	-	
In band Spurious		Frequency offset ≦2MHZ		-20		dBm
		Frequency offset ≧3MHZ		-30		dBm
Out of band Spurious Emissions		POUT = 0 dBm, Frequencies <2.4 GHz	-	-	-52	dBm
		2.4~12 GHz, excluding harmonics	-	-	-50	dBm
Harmonics	2HARM	POUT = 0 dBm, using of-chip Harmonic filter	-	-	-40	dBc
	3HARM	POUT = 0 dBm, using of-chip Harmonic filter	-	-	-42	dBc

Table 3. Transmitter Electrical Specifications

4.5 Receiver Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RX Frequency Range	F_{TX}	World Wide (Not Supported)	2400	-	2483.5	MHz
Intermediate frequency	F_{LIF}	1Mbps data rate,RX BW 1MHz		1		MHz
RX Sensitivity (BER < 0.1%)	$P_{RX\text{-}1MHz}$	Sensitivity at 1.0 Mbps, GFSK Δf = ±250 kHz, channel-spacing = 2 MHz	-	-87		dBm
Maximum Receiving Power	$P_{RX\text{-}MAX}$		-	-10	-	dBm
Current Consumption	I_{RX}	Synthesizer & Receiver enabled	-	16.5	-	mA
RX Channel Bandwidth	BW	Depends on the input data rate	-	1.0	-	MHz
RSSI Resolution	RES_{RSSI}	Analog RSSI		2		dB
Selectivity (For Desired signal at -67dBm)	$C/I_{co\text{-}channel}$	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer and desired modulated with the desired data rate and channel spacing accordingly, GFSK with BT = 0.5	-	21	-	dB
	C/I_{1MHz}		-	15	-	dB
	C/I_{2MHz}		-	-17	-	dB
	$C/I_{\geqq 3MHz}$			-27		dB
Blockers (For Desired signal at -67dBm)	P_{BLOCK1}	Blockers from 30 to 2000 MHz	-	-30	-	dBm
	P_{BLOCK2}	Blockers from 2003 to 2399 GHz	-	-35	-	dBm
	P_{BLOCK3}	Blockers from 2.484 to 2.997 GHz	-	-35	-	dBm
	P_{BLOCK4}	Blockers from 3.0 to 12.75 GHz	-	-30	-	dBm

Table 4. Receiver Electrical Specifications

5 Hardware Description

5.1 Module size

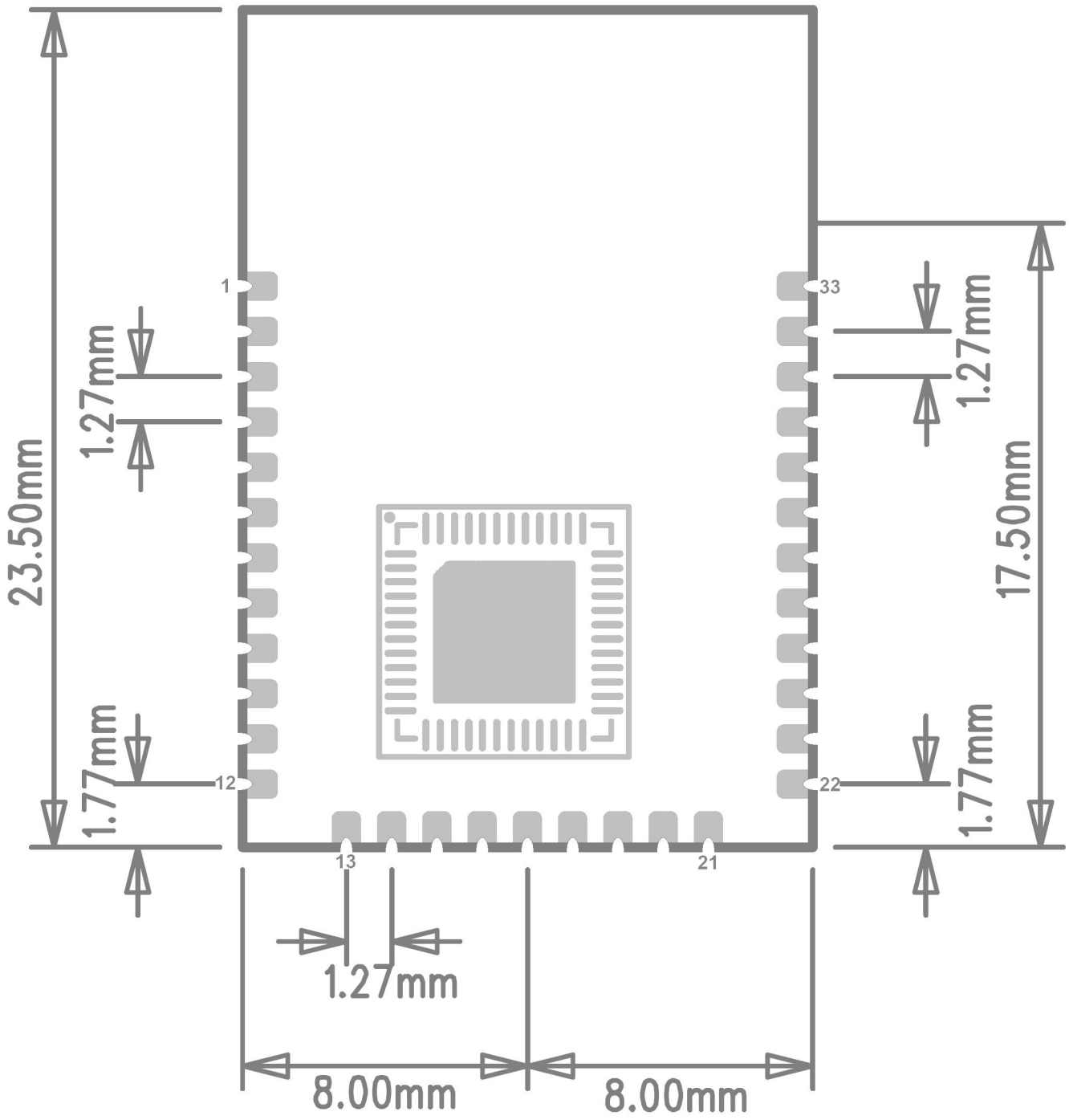

Figure 3. Module size(Top view)

5.2 Module internal BOM

Item	Quant	Reference	Value	Description	MPN	VENDOR
1	2	C21, C23	0.5pF	CAP CER,0.4PF,50V,±0.1pF,NP0,0402	CC0402BRNP09BN0R5	Yageo
2	1	C24	1.8pF	CAP CER,1.8PF,50V,±0.25pF,NP0,0402	CC0402CRNP09BN1R8	Yageo
3	5	C2,C3,C13, C15,C16	10pF	CAP CER, 10PF, 50V, ±5%, NP0,0402	CC0402JRNP09BN100	Yageo
4	5	C4,C6,C9,C18,C19	0.1uF	CAP CER, 0.1UF,10V,±10%,X5R,0402	CC0402KRX7R7BB104	Yageo
5	1	C1	10uF	CAP CER,10UF,6.3V,±20%,X5R,0603	CC0603MRX5R5BB106	Yageo
6	2	L1,C22	0	RES FILM,0ohm;±5%;1/16W;0402	RC0402JR-070RL	Yageo
7	1	L2	1.5nH	IND CER,1.5nH,±0.3nH,300mA,0402	SDCL1005C1N5STDF	Sunlord
8	1	L4	3.9nH	IND CER,3.9nH,±0.3nH,300mA,0402	SDCL1005C3N9STDF	Sunlord
9	1	L5	4.3nH	IND CER,4.3nH,±0.3nH,300mA,0402	SDCL1005C4N3STDF	Sunlord
10	1	L3	22nH	IND CER,22nH,±5%,300mA,0402	SDCL1005C22NJTDF	Sunlord
11	1	Y2	26MHz	Crystal,26MHz,10pF,±10ppm,3.2*2.5mm	S3225A 26MHZ	Yoketant
12	1	Y3	32768Hz	Crystal,32768Hz,12.5pF,± 20ppm,3.2*1.5	S3215C 32.768KHZ	Yoketant
13	1	U0	SH87F8801	IC,BLE chip,QFN48,6*6mm	SH87F8801	Sinowealth

5.3 Reference schematic

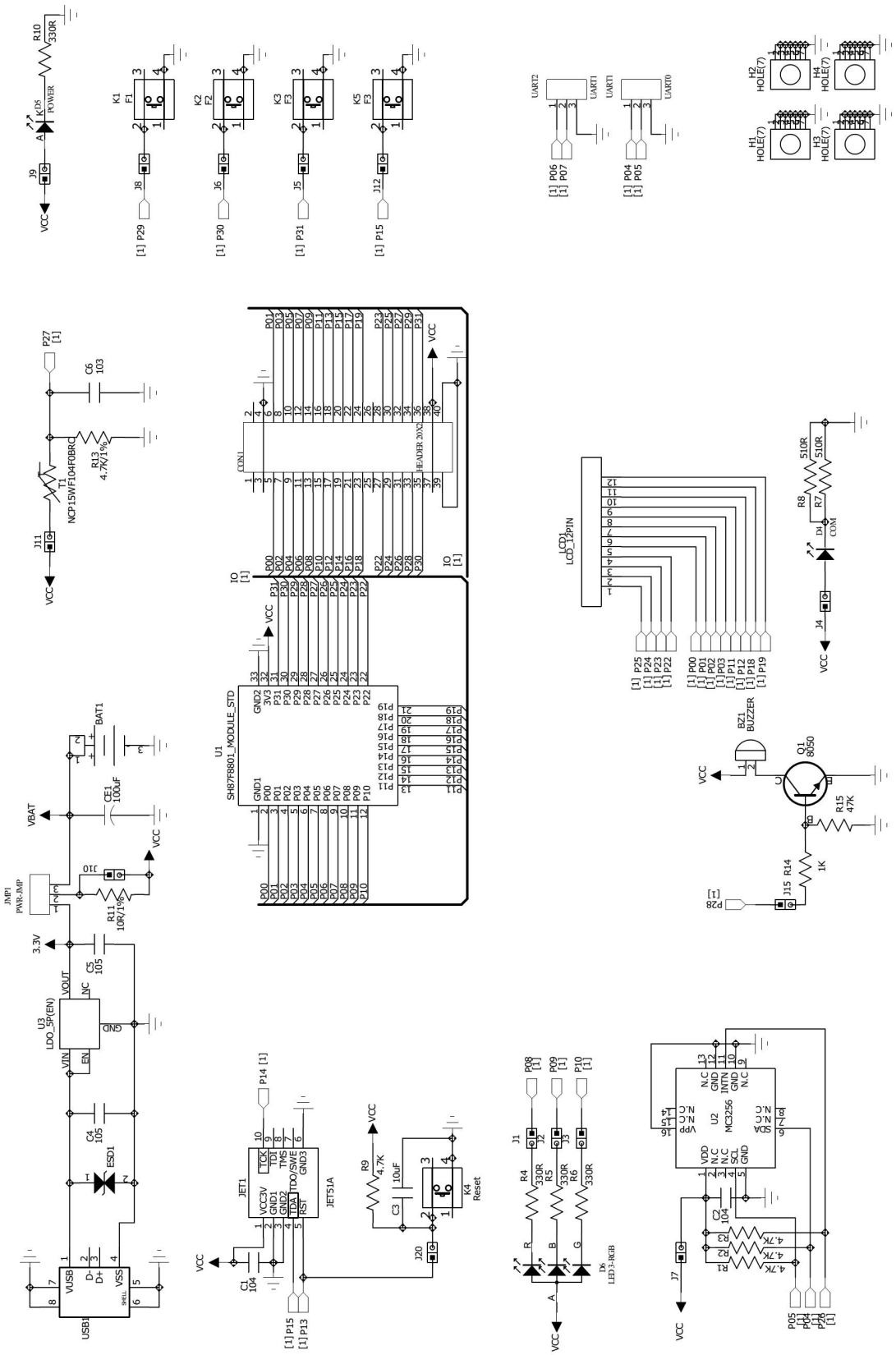

Figure 4. reference schematic for BLE module

5.4 Layout guide

BLE works in 2.4GHz ISM band, PCB and Mechanical design should be very careful to avoid various bad effects on the RF performance. Please note the following points:

1. Product housing surrounding BLE module should be avoided using metal materials. If the housing is metal, it is recommended to use an external 2.4GHz antenna.
2. Metal screws should be far away from RF part of module.
3. Module should be placed on the edge of motherboard, ensure the antenna towards outside. Please make sure that all layers have no trace or copper under the Antenna region.

6 Software introduction

For detail, please refer to SH-BLEM01 BLE module SW application documents.