SLM500S Hardware Design Manual

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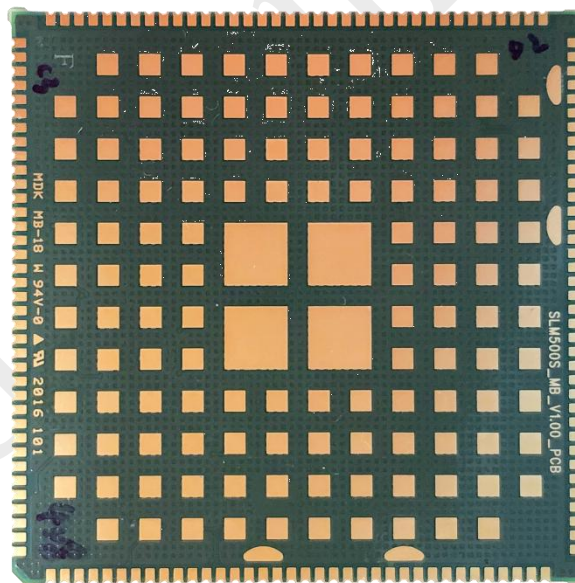
Foreword

Thank you for using the SLM500S module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

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Contents

Version History

Time	Revision	Change Description	Author
2020-3-14	1.00	Initial establishment	Hardware Department
2020-5-19	1.01	Update the content	Hardware Department
2020-6-22	1.02	Add MIC and earphone design instructions	Hardware Department
2020-10-26	1.03	Update module 3D dimension diagram and recommended PCB package dimension diagram, increase pin interval size. Added 7.5 Packaging Information	Hardware Department
2021-1-18	1.04	NTC resistance changed from 47K to 10K; Update ADC Description	Hardware Department
2021-8-5	1.05	Changing PIN Definitions	Hardware Department
2022-08-26	1.06	Overall content modification	Hardware Department

1. Introduction

This document describes the hardware application interfaces of the module, including circuit connections and radio frequency interfaces. This helps users quickly learn about the interface definition, electrical performance, and structural dimensions of the module. Combining this document with other application documents, customers can quickly design various mobile communication solutions and provide more perfect solutions for end users.

2. Module Overview

The SLM500S module uses a quad-core base band processor based on ARM Cotex-A53. The main frequency is up to 1.4GHz, and the memory supports single-channel 32-bit LPDDR3/667MHz. The chip can support TD-LTE/FDD-LTE/WCDMA/GSM and other systems.

The SLM500S module supports the following operating frequency bands：
- TDD-LTE: B34/38/39/40/41
- FDD-LTE: B1/3/5/7/8/20
- WCDMA: B1/B5/B8
- GSM: B2/3/5/8

Note: The TDD-LTE B41 band bandwidth of SLM500S is 100MHz (2535 ~ 2655 MHz), and the channel is 40040 ~ 41240

The physical interface of the module is a 274-pin pad, and the hardware interface is as follows：

- Three 1.8V UART serial ports, including one four-wire port and two two-wire port
- One LCD (MIPI interface)
- Double Camera Interface (MIPI interface)
- A high-speed USB interface
- Three-channel audio input interface
- Two audio output interfaces
- Two UIM card ports
- GPIO interfaces
- Four sets of I2C interfaces (one set of CAM-specific I2C)
- Two SPI interfaces
- One SD card port
- Support GNSS, 2.4G WiFi, Bluetooth 4.2 functions

2.1.Summary of Features

Table 2.1:Main features of the module

Product Feature	Description
CPU	Quad-core A53 (64bit) 1.4GHz
GPU	Mail T820 MP1@680MHz
System memory	8GB eMMC + 1GB LPDDR3 Compatible with 16GB+2GB
Operating System	Android10
Size	40.5x40.5x2.8mm，LCC 146pin+LGA 128pin
Network band SLM500S	TDD-LTE: B34/38/39/40/41 FDD-LTE: B1/3/5/8 WCDMA: B1/B5/B8 GSM: B2/3/5/8
Wi-Fi	IEEE 802.11b/g/n 2.4G

Bluetooth	BT 4.2	
FM	NO Support	
GNSS	GPS/Beidou/Glonass	
Data access	TD-LTE	Cat4 TD-LTE 117/30Mbps
	FDD-LTE	Cat4 FDD-LTE 150/50Mbps
	DC-HSPA+	42/11.2Mbps
	EDGE	Class12, 236.8kbps/236.8kbps
	GPRS	Class12, 85.6kbps/85.6kbps
SIM	DSDS 3.0/1.8V Support SIM detection L/W/G+G with CSFB to W/G	
Display	Matrix: HD+：1440*720	
	Support HD up to 60fps	
	LCD Size: User defined	
	Interface: MIPI DSI 4-lane;	
Camera	Interface: Main: MIPI CSI 2-lanes; front: MIPI CSI 1-lanes	
	Camera Pixel: Max. Front 2Mp/Rear 5Mp	
	Video decode	1080p@30 fps:H.264/MPEG-4
	Video encode	1080p@30 fps: H.264/MPEG-4
Input devices	Keypads（Power on/off、Reset、volume+、volume-）	
	TP	
Reset	Support hard reset	
Application interface	The name of the interface	Main Function Description
	VBAT	4pin，Module power input，3.5V～4.2V，Nominal value3.8V
	SDIO *1	SD Card，support up to 256GB
	USB	Support OTG USB_BOOT（For forced download）
	UART*3	One four-wire port and two two-wire port
	I2C*4	Support
	SPI*2(master only)	Support
	ADC*1	Support
	PWM*1	Support
	Charger	Linear Charger 1A
	Vibration	Support
	GPIO	37 GPIOs
	VRTC	Real-time clock backup battery
	RF Interface	Multi-mode LTE main antenna Multi-mode LTE diversity antenna GPS antenna 2.4G WiFi/BT antenna
	Audio	Three groups of analog MICs

One Hands free speaker.

One earpiece

One stereo headphone.

2.2.Block Diagram

The following figure lists the main functional parts of the module：

- Base band chips
- Power management chip
- The RF Transceiver chip
- WIFI/BT 2-in-1 chip
- The antenna interface
- LCD/CAM - MIPI interface
- EMCP memory chip
- AUDIO interface
- Serial port, SD card interface, SIM card interface, I2C interface and so on
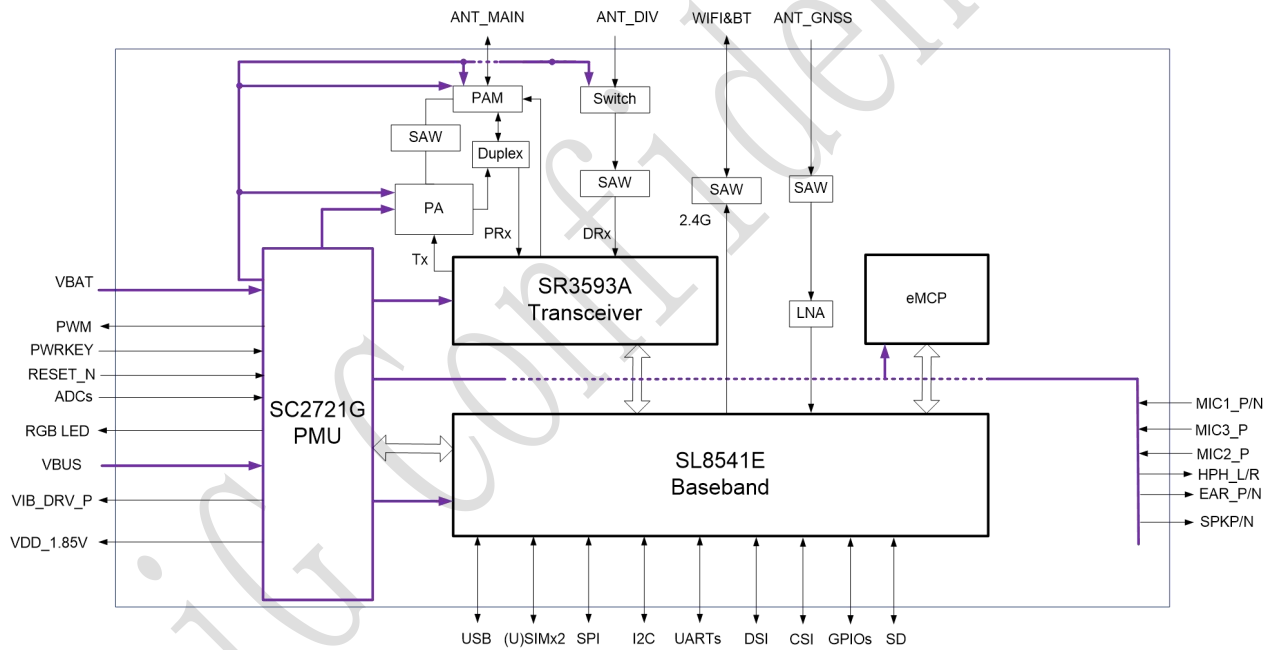
Fig2.1：Module function block diagram

3.Module Package

3.1.Pin Distribution Diagram
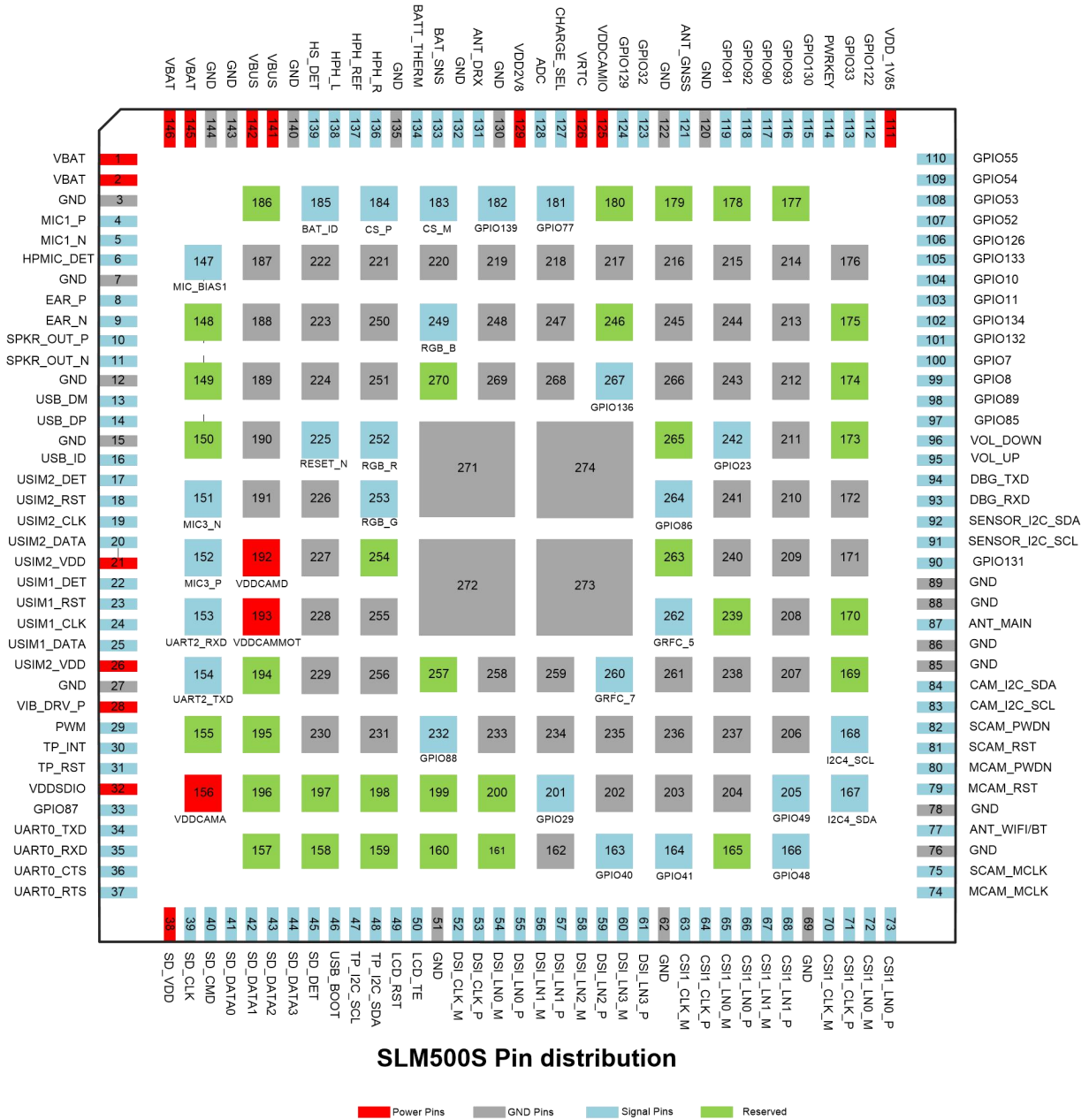
Fig3.1：Module pin diagram (top view)

3.2.Module Pin Description

Table 3.1:Pin description

#	Pin Name	GPIO Interrupt	Pad Characteristics	Functional Description
1	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
2	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
3	GND		GND	GND
4	MIC1_P		AI	Microphone 1 input plus
5	MIC1_N		AI	Microphone 1 input minus
6	MIC2_P		AI	Microphone 2 input
7	GND		GND	GND
8	EAR_P		AO	Earpiece output, plus
9	EAR_M		AO	Earpiece output, minus
10	SPKR_OUT_P		AO	Class-D speaker driver output, plus
11	SPKR_OUT_M		AO	Class-D speaker driver output, minus
12	GND		GND	GND
13	USB_DM		I/O	USB data minus
14	USB_DP		I/O	USB data plus
15	GND		GND	GND
16	USB_ID		DI	USB ID
17	UIM2_DET	GPIO9	DI	Configurable I/O,UIM2 removal detection
18	UIM2_RESET		DO	UIM2 reset
19	UIM2_CLK		DO	UIM2 clock
20	UIM2_DATA		I/O	UIM2 data
21	UIM2_VDD		PO	PMIC output for UIM2
22	UIM1_DET	GPIO31	DI	Configurable I/O,UIM1 removal detection
23	UIM1_RESET		DO	UIM1 reset
24	UIM1_CLK		DO	UIM1 clock
25	UIM1_DATA		I/O	UIM1 data

26	UIM1_VDD		PO	PMIC output for UIM1
27	GND		GND	GND
28	VIB_DRV_P		PO	Haptics driver output positive
29	PWM	GPIO123	I/O	Configurable PWM
30	TP_INT	GPIO144	DI	Configurable I/O,TP INT
31	TP_RST	GPIO145	DO	Configurable I/O,TP RESET
32	VDDSDIO		PO	PMIC output 1.8V for SD-card IO
33	GPIO87	GPIO87	I/O	Configurable I/O
34	UART0_TXD	GPIO60	I/O	Configurable I/O,UART0 TX
35	UART0_RXD	GPIO61	I/O	Configurable I/O,UART0 RX
36	UART0_CTS	GPIO62	I/O	Configurable I/O,UART0 CTS
37	UART0_RTS	GPIO63	I/O	Configurable I/O,UART0 RTS
38	SD_VDD		PO	PMIC output 2.95V for SD-card power
39	SD_CLK		DO	Secure digital controller clock
40	SD_CMD		I/O	Secure digital controller command
41	SD_D0		I/O	Secure digital controller data bit 0
42	SD_D1		I/O	Secure digital controller data bit 1
43	SD_D2		I/O	Secure digital controller data bit 2
44	SD_D3		I/O	Secure digital controller data bit 3
45	SD_DET	GPIO78	DI	Configurable I/O,SD card detection
46	USB_BOOT		DI	Pullup to forced USB boot
47	TP_I2C_SCL	GPIO146	DO	Configurable I/O,TP I2C SCL
48	TP_I2C_SDA	GPIO147	I/O	Configurable I/O,TP I2C SDA
49	LCD_RESET	GPIO50	DO	Configurable I/O, LCD RESET
50	LCD_TE	GPIO51	DO	Configurable I/O, LCD TE
51	GND		GND	GND
52	DSI_CLK_M		AO	MIPI display serial interface 0 clock-
53	DSI_CLK_P		AO	MIPI display serial interface 0 clock+
54	DSI_LAN		AIO	MIPI display serial interface 0 lane0-

	E0_M		
55	DSI_LANE0_P	AIO	MIPI display serial interface 0 lane0+
56	DSI_LANE1_M	AIO	MIPI display serial interface 0 lane1-
57	DSI_LANE1_P	AIO	MIPI display serial interface 0 lane1+
58	DSI_LANE2_M	AIO	MIPI display serial interface 0 lane2-
59	DSI_LANE2_P	AIO	MIPI display serial interface 0 lane2+
60	DSI_LANE3_M	AIO	MIPI display serial interface 0 lane3-
61	DSI_LANE3_P	AIO	MIPI display serial interface 0 lane3+
62	GND	GND	GND
63	CSI1_CLK_M	AO	MIPI camera serial interface 1 clock-
64	CSI1_CLK_P	AO	MIPI camera serial interface 1 clock+
65	CSI1_LANE0_M	AIO	MIPI camera serial interface 1 lane0-
66	CSI1_LANE0_P	AIO	MIPI camera serial interface 1 lane0+
67	CSI1_LANE1_M	AIO	MIPI camera serial interface 1 lane1-
68	CSI1_LANE1_P	AIO	MIPI camera serial interface 1 lane1+
69	GND	GND	GND
70	CSI0M_CLK_M	AO	MIPI camera serial interface 0 clock-
71	CSI0M_CLK_P	AO	MIPI camera serial interface 0 clock+
72	CSI0M_LANE0_M	AIO	MIPI camera serial interface 0 lane0-
73	CSI0M_LANE0_P	AIO	MIPI camera serial interface 0 lane0+

74	MCAM_MCLK	GPIO42	DO	Configurable I/O,main CAM MCLK
75	SCAM_MCLK	GPIO43	DO	Configurable I/O,front CAM MCLK

76	GND	GND	GND
77	ANT_WIFI/BT	AIO	RF signal for WIFI/BT

78	GND		GND	GND
79	MCAM_RST	GPIO44	DO	Configurable I/O,main CAM RESET
80	MCAM_PWDN	GPIO46	DO	Configurable I/O,main CAM PWDN
81	SCAM_RST	GPIO45	DO	Configurable I/O,front CAM RESET
82	SCAM_PWDN	GPIO47	DO	Configurable I/O,front CAM PWDN
83	CAM_I2C_SCL	GPIO74	DO	Dedicated camera I2C SCL
84	CAM_I2C_SDA	GPIO75	I/O	Dedicated camera I2C SDA
85	GND		GND	GND
86	GND		GND	GND
87	ANT_MAIN		AIO	RF signal for main ANT
88	GND		GND	GND
89	GND		GND	GND
90	GPIO131	GPIO131	I/O	Configurable I/O
91	SENSOR_I2C_SCL	GPIO127	DO	SENSOR I2C SCL
92	SENSOR_I2C_SDA	GPIO128	I/O	SENSOR I2C SDA
93	DBG_UART_RX		DI	UART RX
94	DBG_UART_TX		DO	UART TX
95	VOL_UP		DI	KEY VOL+
96	VOL_DOWN		DI	KEY VOL-
97	GPIO85	GPIO85	I/O	Configurable I/O
98	GPIO89	GPIO89	I/O	Configurable I/O
99	GPIO8	GPIO8	I/O	Configurable I/O
100	GPIO7	GPIO7	I/O	Configurable I/O
101	GPIO132	GPIO132	I/O	Configurable I/O
102	GPIO134	GPIO134	I/O	Configurable I/O
103	GPIO11	GPIO11	I/O	Configurable I/O
104	GPIO10	GPIO10	I/O	Configurable I/O
105	GPIO133	GPIO133	I/O	Configurable I/O,
106	GPIO121	GPIO121	I/O	Configurable I/O

107	GPIO52	GPIO52	I/O	Configurable I/O
108	GPIO53	GPIO53	I/O	Configurable I/O
109	GPIO54	GPIO54	I/O	Configurable I/O
110	GPIO55	GPIO55	I/O	Configurable I/O
111	VDD_1V85		PO	PMIC output 1.85V for digital I/Os
112	GPIO122	GPIO122	I/O	Configurable I/O
113	GPIO33	GPIO33	I/O	Configurable I/O
114	PWRKEY		DI	KEY POWER ON/OFF
115	GPIO130	GPIO130	I/O	Configurable I/O
116	GPIO93	GPIO93	I/O	Configurable I/O,SPI CLK
117	GPIO90	GPIO90	I/O	Configurable I/O,SPI CS
118	GPIO92	GPIO92	I/O	Configurable I/O,SPI DI
119	GPIO91	GPIO91	I/O	Configurable I/O,SPI DO
120	GND		GND	GND
121	ANT_GNSS		AI	RF signal for GPS ANT
122	GND		GND	GND
123	GPIO32	GPIO32	I/O	Configurable I/O
124	GPIO129	GPIO129	I/O	Configurable I/O
125	VDDCAMIO		PO	PMIC output 1.8V for Camera IO
126	VRTC		AI,AO	Coin-cell battery or backup battery
127	CHARGE_SEL		DI	Charge path selection
128	ADC		AI	Configurable ADC
129	VDD_2V8		PO	PMIC output 2.8V for TP and sensor
130	GND		GND	GND
131	ANT_DRX		AI	RF signal for diversity ANT
132	GND		GND	GND
133	BAT_SNS		AI	battery voltage input to ADC
134	BATT_THERM		AI	Battery temperature input to ADC
135	GND		GND	GND
136	HPH_R		AO	Headphone output, right channel
137	HPH_REF		AI	Headphone ground reference
138	HPH_L		AO	Headphone output, left channel
139	HS_DET		AI	MBHC mechanical insertion/removal-detection

140	GND		GND	GND
141	VBUS		PI	USB Voltage
142	VBUS		PI	USB Voltage
143	GND		GND	GND
144	GND		GND	GND
145	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
146	VBAT		PI,PO	Battery,3.5V-4.2V,default 3.8V
147	MIC_BIAS 1		AO	Microphone bias #1
148	RESERVED			Reserved
149	RESERVED			Reserved
150	RESERVED			Reserved
151	MIC3_N		AI	Microphone 3 input minus
152	MIC3_P		AI	Microphone 3 input plus
153	UART2_RXD	GPIO73	I/O	Configurable I/O,UART2 RXD
154	UART2_TXD	GPIO72	I/O	Configurable I/O,UART2 TXD
155	RESERVED			Reserved
156	VDDCAMA		PO	PMIC output 2.8V for Camera AVDD
157	RESERVED			Reserved
158	RESERVED			Reserved
159	RESERVED			Reserved
160	RESERVED			Reserved
161	RESERVED			Reserved
162	GND		GND	GND
163	GPIO40	GPIO40	I/O	Configurable I/O
164	GPIO41	GPIO41	I/O	Configurable I/O
165	RESERVED			Reserved
166	GPIO48	GPIO48	I/O	Configurable I/O

167	I2C4_SDA	GPIO155	I/O	Configurable I/O, I2C4 SDA for switching Charging and Flash LED Driver and Source Driver(if need)
168	I2C4_SCL	GPIO154	DO	Configurable I/O, I2C4 SCL for switching Charging and Flash LED Driver and Source Driver(if need)
169	RESERVED			Reserved
170	RESERVED			Reserved
171	GND		GND	GND
172	GND		GND	GND
173	RESERVED			Reserved
174	RESERVED			Reserved
175	RESERVED			Reserved
176	GND		GND	GND
177	RESERVED			Reserved
178	RESERVED			Reserved
179	RESERVED			Reserved
180	RESERVED			Reserved
181	GPIO77	GPIO77	I/O	Configurable I/O
182	GPIO139	GPIO139	I/O	Configurable I/O
183	CS_M		DI	Fuel gauge input,minus
184	CS_P		DI	Fuel gauge input,plus
185	BAT_ID		DI	Battery ID
186	RESERVED			Reserved
187	GND		GND	GND
188	GND		GND	GND
189	GND		GND	GND
190	GND		GND	GND
191	GND		GND	GND
192	VDDCAMD		PO	PMIC output 1.2V for Camera DVDD
193	VDDCAMMOT		PO	PMIC output 2.8V

194	RESERVED			Reserved
195	RESERVED			Reserved
196	RESERVED			Reserved
197	RESERVED			Reserved
198	RESERVED			Reserved
199	RESERVED			Reserved
200	RESERVED			Reserved
201	GPIO29	GPIO29	I/O	Configurable I/O
202	GND		GND	GND
203	GND		GND	GND
204	GND		GND	GND
205	GPIO49	GPIO49	I/O	Configurable I/O
206	GND		GND	GND
207	GND		GND	GND
208	GND		GND	GND
209	GND		GND	GND
210	GND		GND	GND
211	GND		GND	GND
212	GND		GND	GND
213	GND		GND	GND
214	GND		GND	GND
215	GND		GND	GND
216	GND		GND	GND
217	GND		GND	GND
218	GND		GND	GND
219	GND		GND	GND
220	GND		GND	GND
221	GND		GND	GND
222	GND		GND	GND
223	GND		GND	GND
224	GND		GND	GND
225	RESET_N		DI	PMIC RESET

226	GND		GND	GND
227	GND		GND	GND
228	GND		GND	GND
229	GND		GND	GND
230	GND		GND	GND
231	GND		GND	GND
232	GPIO88	GPIO88	I/O	Configurable I/O
233	GND		GND	GND
234	GND		GND	GND
235	GND		GND	GND
236	GND		GND	GND
237	GND		GND	GND
238	GND		GND	GND
239	RESERVED			Reserved
240	GND		GND	GND
241	GND		GND	GND
242	GPIO23	GPIO23	I/O	Configurable I/O
243	GND		GND	GND
244	GND		GND	GND
245	GND		GND	GND
246	RESERVED			Reserved
247	GND		GND	GND
248	GND		GND	GND
249	RGB_B		SINK IN	Blue LED Driver
250	GND		GND	GND
251	GND		GND	GND
252	RGB_R		SINK IN	Red LED Driver
253	RGB_G		SINK IN	Green LED Driver
254	RESERVED			Reserved
255	GND		GND	GND
256	GND		GND	GND
257	RESERVED			Reserved
258	GND		GND	GND

259	GND		GND	GND
260	GRFC_7		DO	RFFE3 CLK
261	GND		GND	GND
262	GRFC_5		DI,DO	RFFE3 DATA
263	RESERVED			Reserved
264	GPIO86	GPIO86	I/O	Configurable I/O
265	RESERVED			Reserved
266	GND		GND	GND
267	GPIO136	GPIO136	I/O	Configurable I/O
268	GND		GND	GND
269	GND		GND	GND
270	RESERVED			Reserved
271	GND		GND	GND
272	GND		GND	GND
273	GND		GND	GND
274	GND		GND	GND

All the GPIO could be programmed to be either input or output, when in input mode,they could be programmed to trigger interrupt to CPU

WPU：Weak pull up
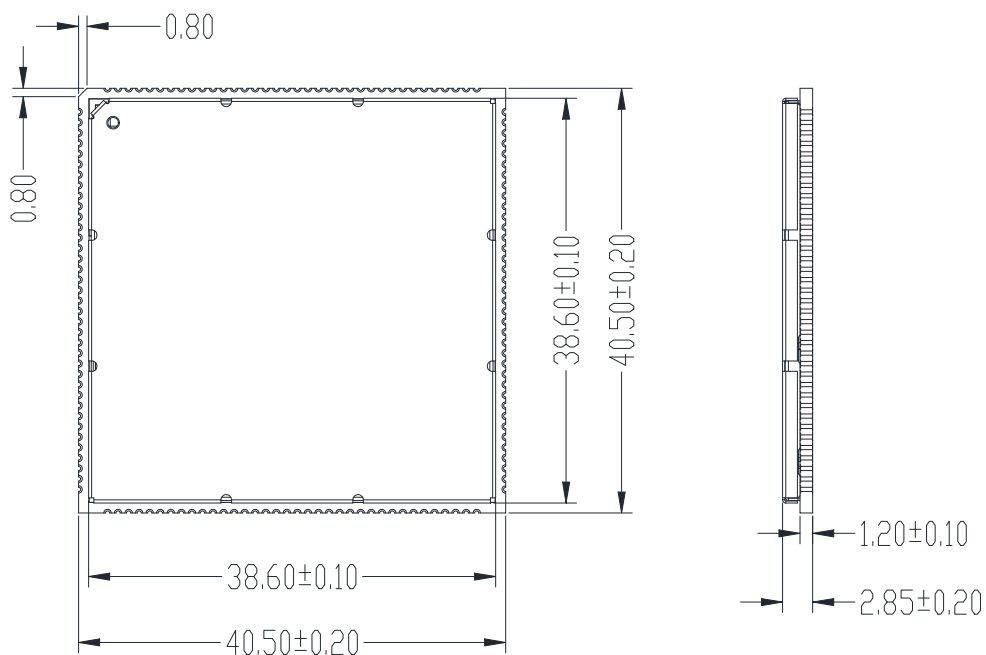
WPD：Weak pull down

3.3.Mechanical Dimensions
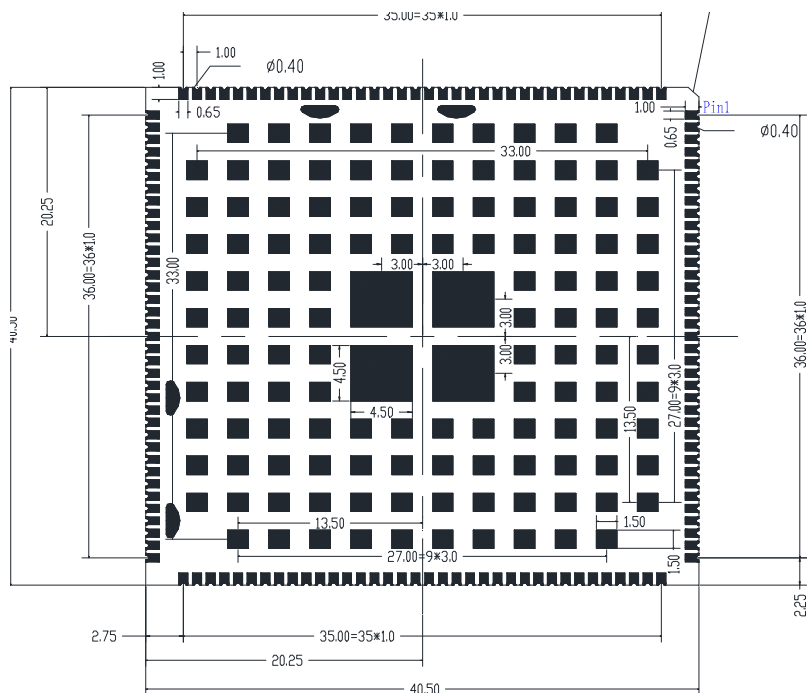
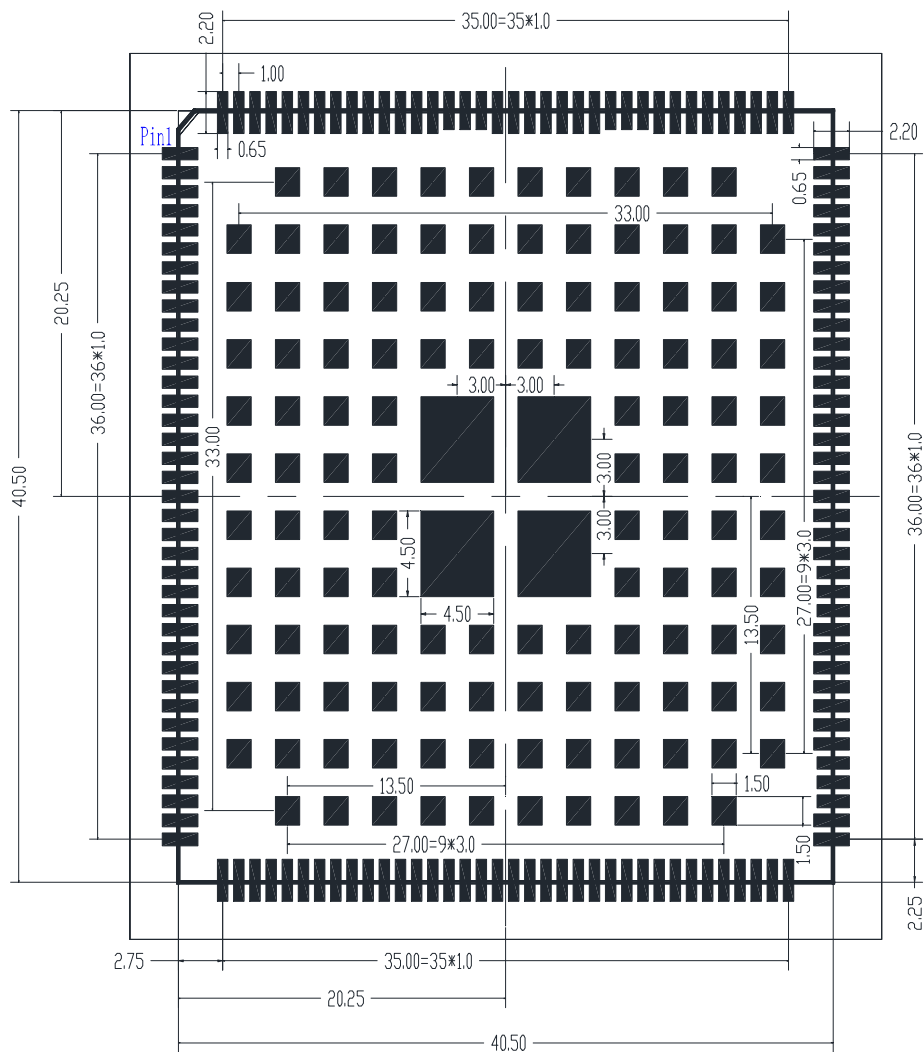**Fig3.2：Module 3D dimension（mm）**

Fig3.3：Recommended PCB package size（mm）

# 4.Interface Application

4.1.Power Supply

For battery-powered devices, the VBAT module has a voltage input range of 3.5V to 4.2V and a recommended voltage of 3.8V. In GSM band, when the module is transmitted at maximum power, the current peak can reach up to 3A instantly, resulting in a large voltage drop on VBAT. It is recommended to use a large capacitor to stabilize voltage close to VBAT. It is recommended to use a 22uF ceramic capacitor, and a 100nF capacitor in parallel can effectively remove high-frequency interference. At the same time, in order to prevent ESD and surge damage to the chip, it is recommended to use appropriate TVS tube and 4.5V voltage regulator tube at module VBAT pin. When PCB layout, capacitor and TVS tube should be as close as possible to module VBAT pin. The user can directly power the module with a 3.8v lithium ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.
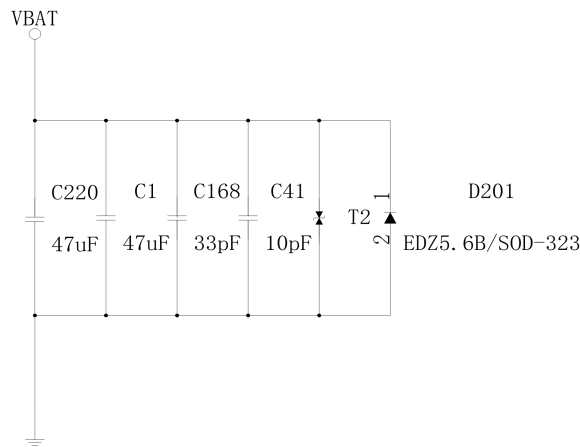
Fig4.1：VBAT input reference circuit

The DC input voltage is +5V. The following figure shows the recommended circuit for using dc-dc power supply：
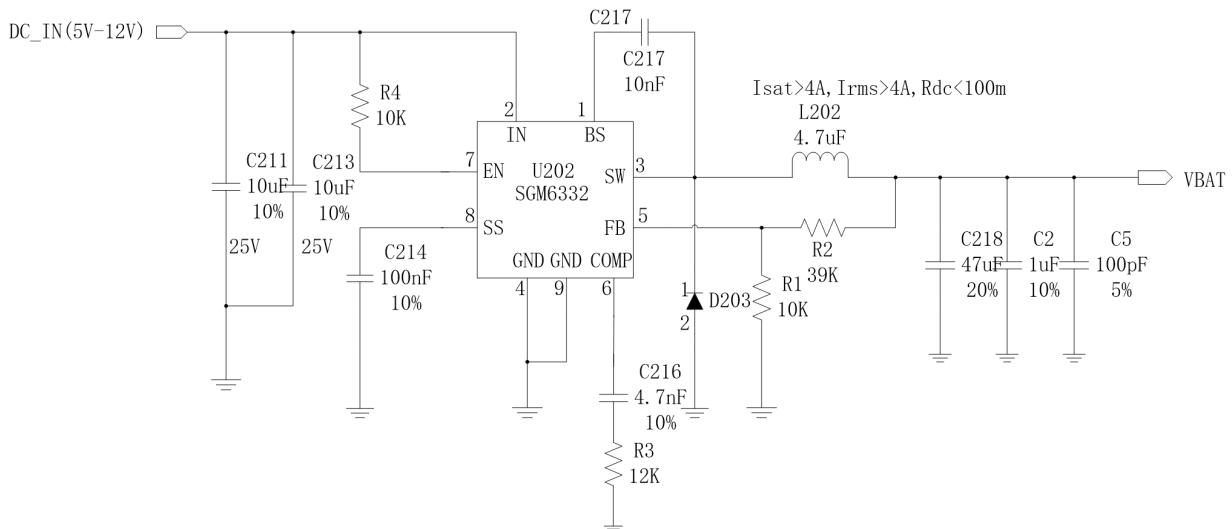
Fig4.2：DC-DC power supply circuit

Note:If the user does not use battery power supply, please note that a 10K resistor is connected to pin 134 (BATT_THERM) of the module and pulled down to GND, so as to prevent the software from judging abnormal battery temperature after the module is powered on and leading to shutdown.

The connection diagram is as follows:
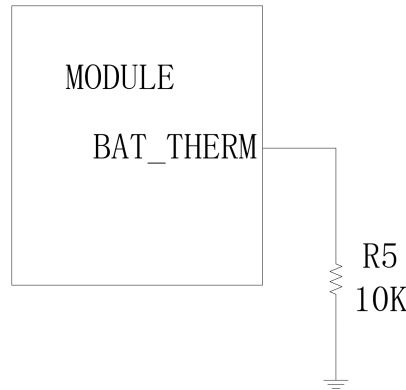
Fig4.3：Diagram of connection when not powered by battery

Users can directly use the 3.8V lithium ion battery to power the module, or use the Nickel-cadmium or nickel-manganese battery to power the module. However, the maximum voltage of the nickel-cadmium or nickel-manganese battery cannot exceed the maximum allowed voltage of the module. Otherwise, the module may be damaged. When using a battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

4.1.1.Power Pin

The VBAT pins (1, 2, 145, 146) are used for power input. In the user's design, please pay special attention to the design of the power supply part to ensure that the drop of VBAT is not less than 3.5V even when the module consumption reaches 3A. If the voltage drop is less than 3.5V, the module may shut down. PCB wiring from VBAT pins to the power supply should be wide enough to reduce voltage sags in transmission burst mode.
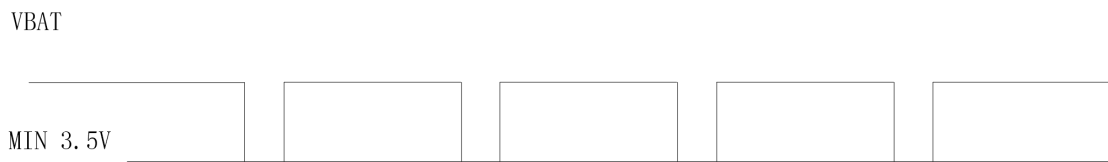

Fig4.4：VBAT lowest voltage sag

4.2.Power On/Off

Do not turn on the module when the temperature and voltage upper limits of the module are exceeded. In extreme cases such operations can cause permanent damage to the module.
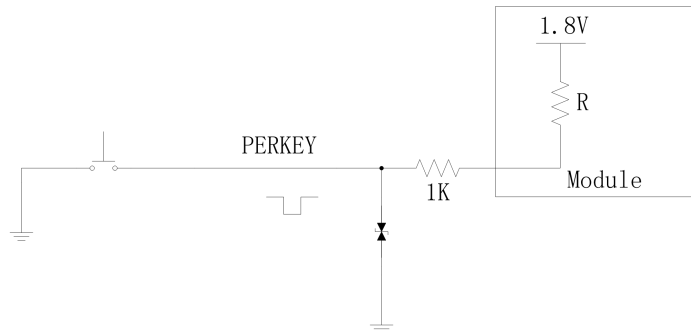
4.2.1.Power On

The user can start the module by pulling down the PWRKEY pin (114) for at least 3 seconds. The pin

has been pulled up to the 1.8V power supply in the module. The recommended circuit is as follows.
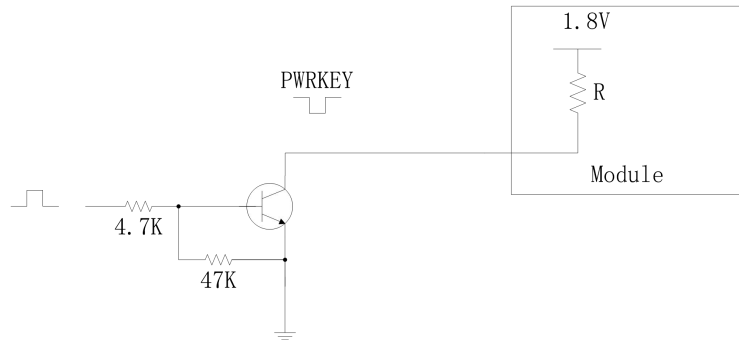
Fig4.5：Power on using external signal driver module
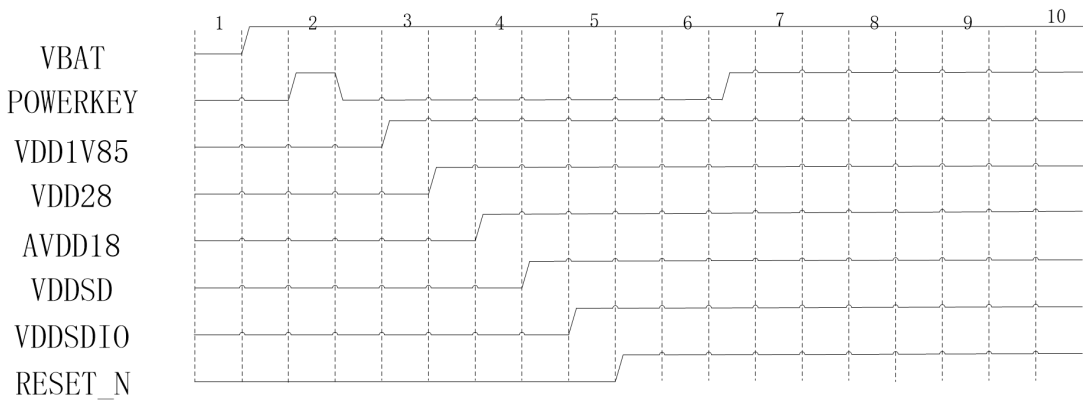

Fig4.6：Use the button circuit to boot

The following figure shows the boot sequence description:

Fig4.7：PWRKEY startup sequence table

*This is a reference timing diagram. Because there may be slight differences with the actual measurement, the actual measurement shall prevail.

4.2.2.Module Shutdown

The user can shut down the machine using the PWRKEY pin.

4.2.2.1PWRKEY Shutdown

The user can power off the device by lowering the PWRKEY signal for at least 3 seconds. Power off circuit can refer to the design of power on circuit. After the module detects the shutdown action, a prompt window will pop up on the screen to confirm whether to execute the shutdown action.

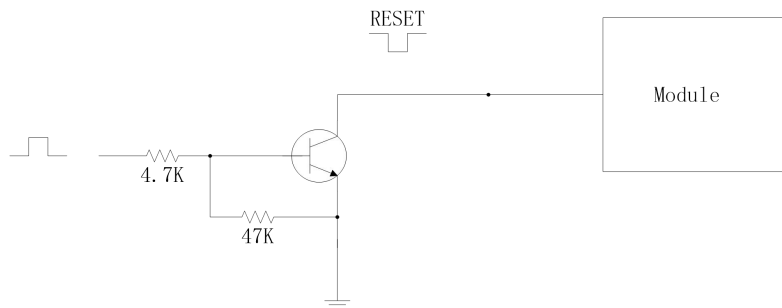You can forcibly shut down the PWRKEY by holding it down for at least 15 seconds.

4.2.3.Module Reset

The SLM500S module supports the reset function. Users can quickly restart the module by pulling down the RESET_N pin of the module.

Recommended circuits are as follows:
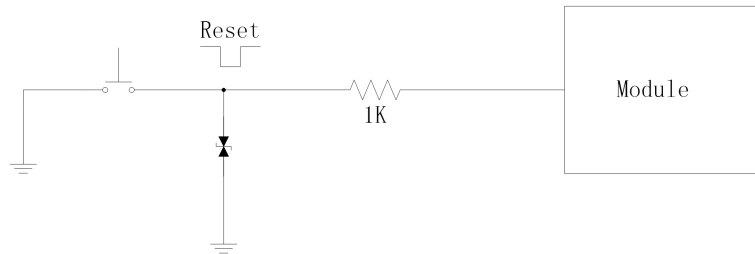
Fig4.8：Use the button circuit to reset

Fig4.9：Reset module using external signal

The typical voltage of the pin is 1.8V at high current level, so the user with 3V or 3.3V level can not directly use GPIO of MCU to drive the pin, and an isolation circuit is required, as shown in Figure 4.9.

4.3.VCOIN

When the VBAT is disconnected and the user needs to save the real-time clock, the VCOIN pin should not be suspended and should be connected to a large external capacitor or battery. When the external capacitor is connected, the recommended value is 100uF, which can keep the real-time clock for 30 seconds. The RTC power module uses an external capacitor or battery to supply power to the RTC inside

the module.
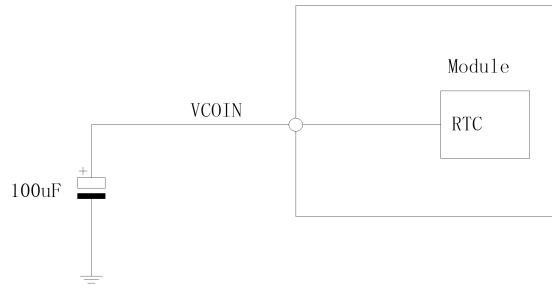
Fig4.10：The external capacitor supplies power to the RTC

Chargeable battery power:

Fig4.11：Chargeable batteries power the RTC

Notes：This VCOIN power supply is 2.5-3.1V, typical typically 3.0V.

4.4.Power Output

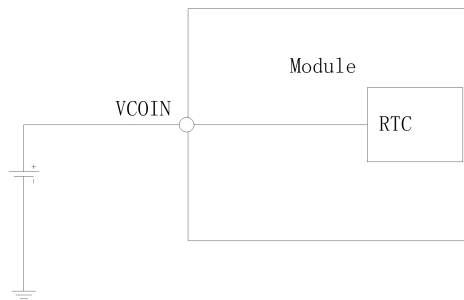The SLM500S has multiple power outputs. Used for LCD, Camera, touch panel and so on. In application, it is recommended to add parallel 33PF and 10PF capacitors in each power supply to effectively remove high-frequency interference.

Table 4.1:The power to describe

Signal	Voltage	Drive current
UIM1_VDD	1.8V/3V	50mA
UIM2_VDD	1.8V/3V	50mA
SD_VDD	3.0V	400mA
VDD_1V85	1.85V	200mA
VDD_2V8	2.8V	150mA
VRTC	3.0V	
VDDCAMIO	1.8V	200mA
VDDCAMD	1.2V	400mA
VDDCAMMOT	2.8V	100mA
VDDCAMA	2.8V	150mA
VDDSDIO	1.8V/3V	100mA

4.5.Serial Port

The SLM500S provides three sets of UART serial ports

Table 4.2:UART Pin description

Name	Pin	Direction	Function
UART0_TXD	34	DI	UART0 Data sending
UART0_RXD	35	DO	UART0 Data receiving
UART0_CTS	36	DI	UART0 Clear to send（CTS）
UART0_RTS	37	DO	UART0 Request to send（RTS）
DBG_UART_RX	93	DI	UART1 Data receiving
DBG_UART_TX	94	DO	UART1 Data sending
UART2_RXD	153	DI	UART2 Data receiving
UART2_TXD	154	DO	UART2 Data sending

You can refer to the following connection mode:
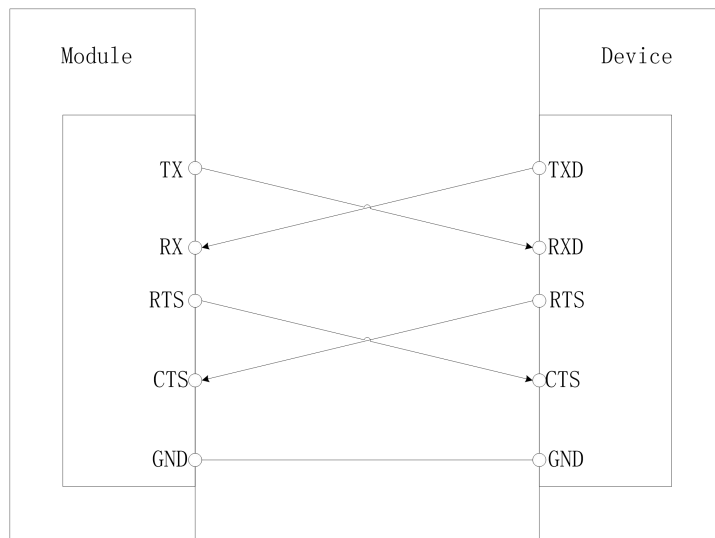
Fig4.12：Serial port connection diagram

When the serial port level used by the user does not match the module, in addition to increasing the level conversion IC, the figure below can also be used to achieve level matching. Here, only TX and RX matching circuits are listed, and other low-speed signals can refer to these two circuits.
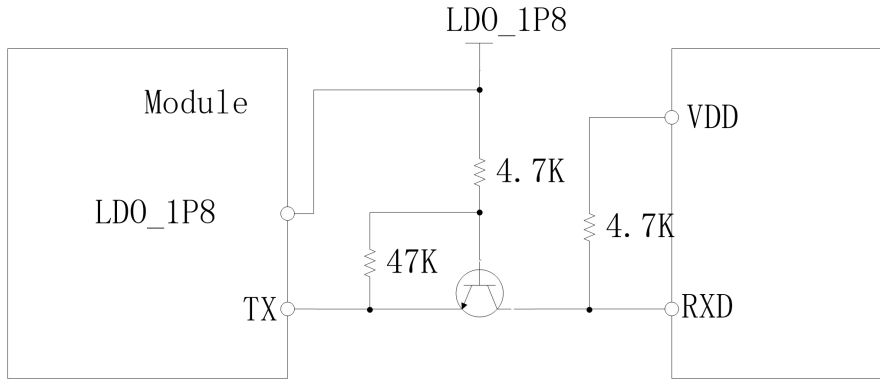
Fig4.13：TX connection diagram
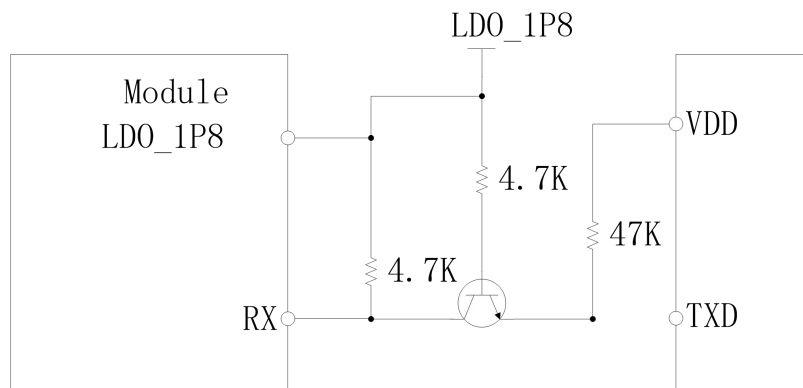
Fig4.14：RX connection diagram

Note: When using Figure 14 and 15 for level isolation, it is necessary to pay attention to the output timing of VDD1V85. The serial port can communicate normally only after VDD1V85 is output normally.

Table 4.3:Serial Port Hardware Parameters

Description	MIN	MAX	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Output low level	-	0.45	V
Output high level	1.35	-	V

Note:

1. The serial port of the module is CMOS interface, which cannot be directly connected to RS232 signal. Use an RS232 converter chip if necessary.

2. If the 1.8V output of the module cannot meet the high level range of the client, please add a level conversion circuit.

4.6.MIPI Interface

The SLM500S supports the Module Industry Processor Interface(MIPI) Interface for Camera and LCD. The module supports a maximum HD+(1440*720) display, in which the Main Camera supports a maximum of 2 lane MIPI and the Front Camera supports 1 lane MIPI.

MIPI is a high-speed signal cable. During the Layout phase, Layout the cables according to the impedance and length requirements:

1. MIPI differential wiring, 100ohm impedance control, priority is given to each pair of separate wrapping. In the case of insufficient space, CLK needs to wrap the ground, while the others need to wrap the ground together, but it should be noted that when the ground cannot be wrapped, the space between the pair and the pair should be extended.

2. Equal length control: 0.5mm between P and N, ±2mm between groups based on CLK.

3. The length of the MIPI cable should not exceed 75mm(3000mil), and the number of through-holes on the path should not exceed four.

4.6.1.LCD Interface

The SLM500S module supports one set of MIPI LCD screens with a maximum resolution of 1440 x 720. The signal interfaces are shown in the following table

Table 4.4:PIN Interface

Main Screen Interface		
Name	**Pin**	**Description**
DSI0_CLK_M	52	MIPI_LCD clock line
DSI0_CLK_P	53	
DSI0_LANE0_M	54	MIPI_LCD data line
DSI0_LANE0_P	55	
DSI0_LANE1_M	56	
DSI0_LANE1_P	57	
DSI0_LANE2_M	58	
DSI0_LANE2_P	59	
DSI0_LANE3_M	60	
DSI0_LANE3_P	61	
LCD_RESET	49	LCD reset pin
LCD_TE	50	LCD frame sync signal
VDD_2V8	129	2.8V power supply
VDDCAMIO	125	1.8V power supply

The GPIO of the module can be used as the LCD_ID. If the GPIO is used as the LCD_ID, please confirm the internal circuit of the LCD. If the resistor divider mode is used in the LCD, please note that the

voltage must meet the voltage range of GPIO.

MIPI is a high-speed signal cable. To avoid EMI interference, you are advised to place a common-mode inductor near the LCD.
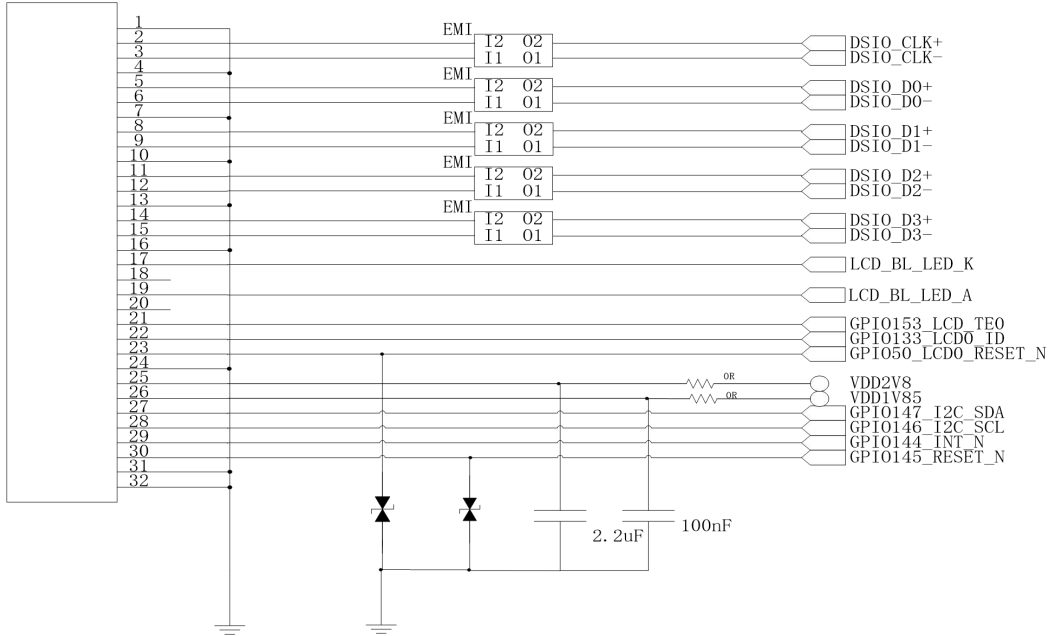

Fig4.15：LCD Interface

SLM500S does not support internal backlight drive. The backlight drive circuit of LCD needs to be added by customers themselves. For details, please refer to the following figure:
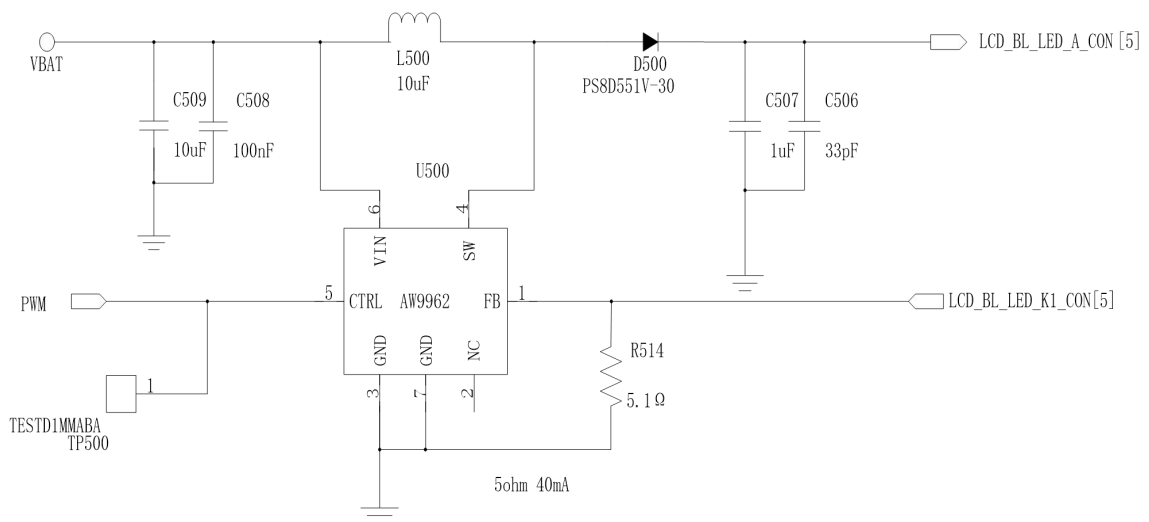

Fig4.16：LCD backlight drive circuit

4.6.2.MIPI Camera Interface

SLM500S module supports MIPI Camera interface and provides Camera dedicated power supply. The

rear Camera is CSI1 interface, supporting two sets of data lines and supporting 5M pixels. The front Camera is CSI0 interface and supports a set of data lines, which can support 2M pixels. The module provides power for the Camera, including VDDCAMA (2.8V), VDDCAMIO (1.8V), VDDCAMMOT (2.8V) (focusing motor power) and VDDCAMD (1.2V).

Table 4.5:MIPI Camera Interface

Rear Camera Interface		
Name	**Pin**	**Description**
CSI1_CLK_M	63	Camera MIPI CLK
CSI1_CLK_P	64	
CSI1_LANE0_M	65	Camera MIPI DATA
CSI1_LANE0_P	66	
CSI1_LANE1_M	67	
CSI1_LANE1_P	68	
MCAM_MCLK	74	Camera CLK
MCAM_RST	79	Camera Reset
MCAM_PWDN	80	Camera Sleep
CAM_I2C_SCL	83	I2C Clock
CAM_I2C_SDA	84	I2C Data
VDDCAMIO	125	Output 1.8V,Camera IOVDD
VDDCAMD	192	Output 1.2V,Camera DVDD
VDDCAMMOT	193	Output 2.8V,Camera AFVDD
VDDCAMA	156	Output 2.8V,Camera AVDD

Front Camera Interface		
Name	**Pin**	**Description**
CSI0M_CLK_M	70	Camera MIPI CLK
CSI0M_CLK_P	71	
CSI0M_LANE0_M	72	Camera MIPI DATA
CSI0M_LANE0_P	73	
SCAM_MCLK	75	Camera CLK
SCAM_RST	81	Camera Reset
SCAM_PWDN	82	Camera Sleep
CAM_I2C_SCL	83	I2C Clock
CAM_I2C_SDA	84	I2C Data
VDDCAMIO	125	Output 1.8V,Camera IOVDD
VDDCAMD	192	Output 1.2V,Camera DVDD
VDDCAMMOT	193	Output 2.8V,Camera AFVDD
VDDCAMA	156	Output 2.8V,Camera AVDD

If the user designs a CAMERA module with auto-focus function, please note that the I2C of the module cannot be directly connected to the AF device, and the I2C of the AF device should be connected to the driver chip of the CAMERA.

The rate of the MIPI interface is high. During cabling, use 100 ohm impedance to control the cable, and pay attention to the cable length. Do not add a small capacitor to the MIPI signal cable, because the rising edge time of MIPI data may be affected and MIPI data may be invalid
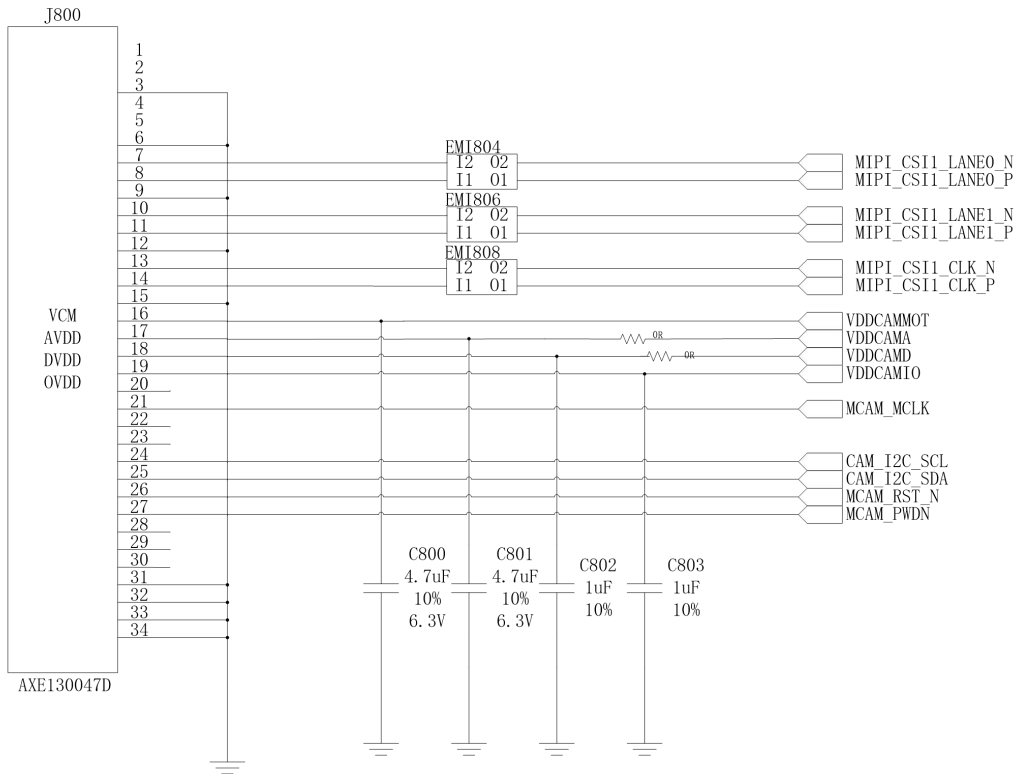
Fig4.17：MIPI Camera1 reference circuit
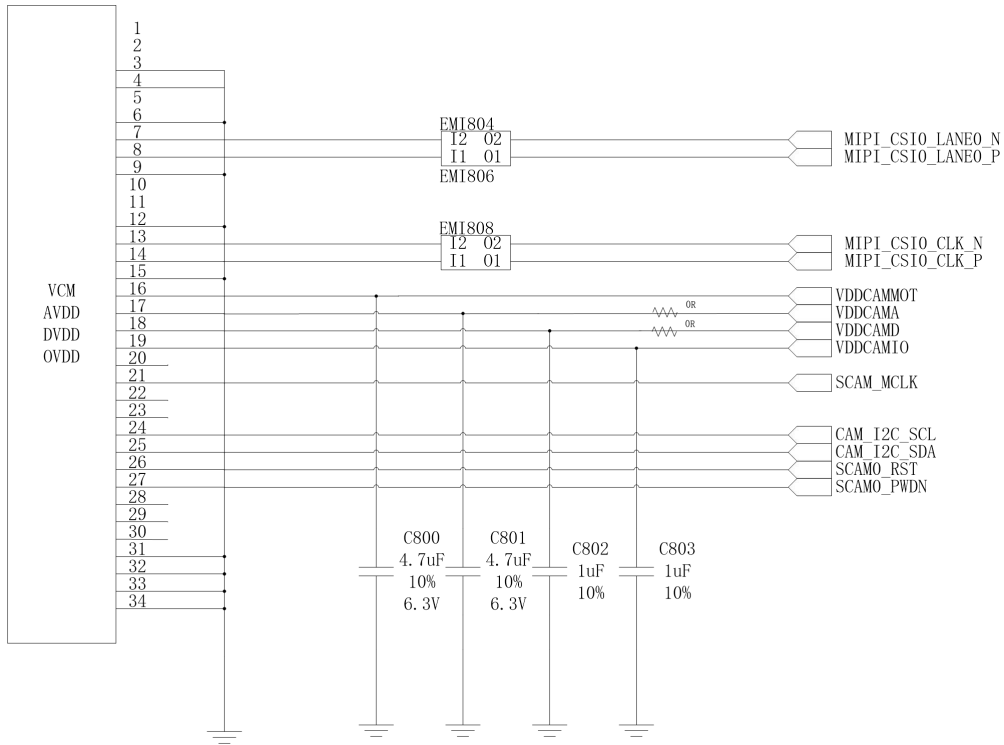
Fig4.18：MIPI Camera0 reference circuit

The power supply required by the Camera, including AVDD-2.8V, AFVDD-2.8V (focus motor power supply) and DVDD-1.2V (CAM core voltage), can be designed with reference to the following LDO circuit.
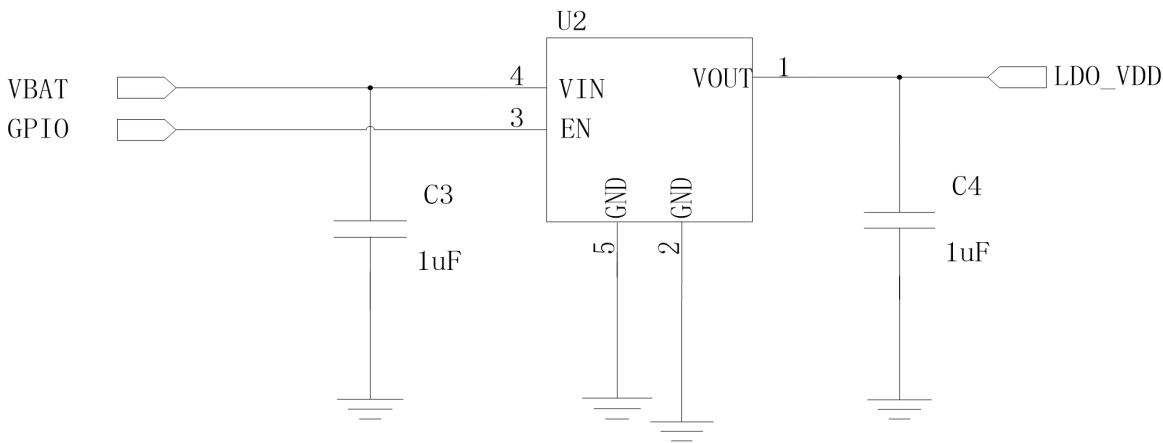
Fig4.19：Camera imaging diagram

4.7.Capacitive Touch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touch, as well as the required power supply and interrupt pins. The default interface pins of capacitive touch software are defined as follows:

Table 4.6:Capacitive touch interface definition

Name	Pin	IN/OUT	Description
TP_I2C_SCL	47	DO	The I2C interface with capacitive touch needs to be pulled up to VDD_1V85
TP_I2C_SDA	48	I/O	
TP_INT	30	DI	INT
TP_RST	31	DO	Reset
VDD_2V8	129	PO	2.8V

Note: The interface definition for capacitive touch can be adjusted by software, and users can change GPIO and I2C according to design needs.

4.8.Audio Interface

The module provides three analog audio inputs. MIC1_P/N is used to connect the main mic; MIC2_P/N can be used to connect the headset mic, and MIC3_P/N can be used to connect the noise-canceling mic. The module also provides three channels of analog audio output (HPH_L/R, REC_P/N, SPK_P/N). The definition of audio PIN is as follows:

Table 4.7:Audio pin

Name	Pin	IN/OUT	Description
MIC1_P	4	AI	MIC1 differential input +
MIC1_N	5	AI	MIC1 differential input -
MIC2_P	6	AI	MIC2 single input
MIC3_P	152	AI	MIC2 differential input +
MIC3_N	151	AI	MIC3 differential input -
MIC_BIAS1	147	AO	MIC1 bias voltage
HPH_REF	137	GND	Earphone reference Gnd
HPH_L	138	AO	Earphone left channel
HPH_R	136	AO	Earphone right channel
HS_DET	139	AI	Earphone plug detection
EAR_M	9	AO	Receiver differential output +
EAR_P	8	AO	Receiver differential output -
SPKR_OUT_M	11	AO	Speaker differential output +
SPKR_OUT_P	10	AO	Speaker differential output -

It is recommended that users choose the following circuit according to the actual application situation to get better sound effect.

4.8.1.Receiver Interface Circuit

EAR_P

B302 0

C313
100pF
5%

EAR_N

B303 0

C319
33pF
5%

C320
33pF
5%

1
2

REC
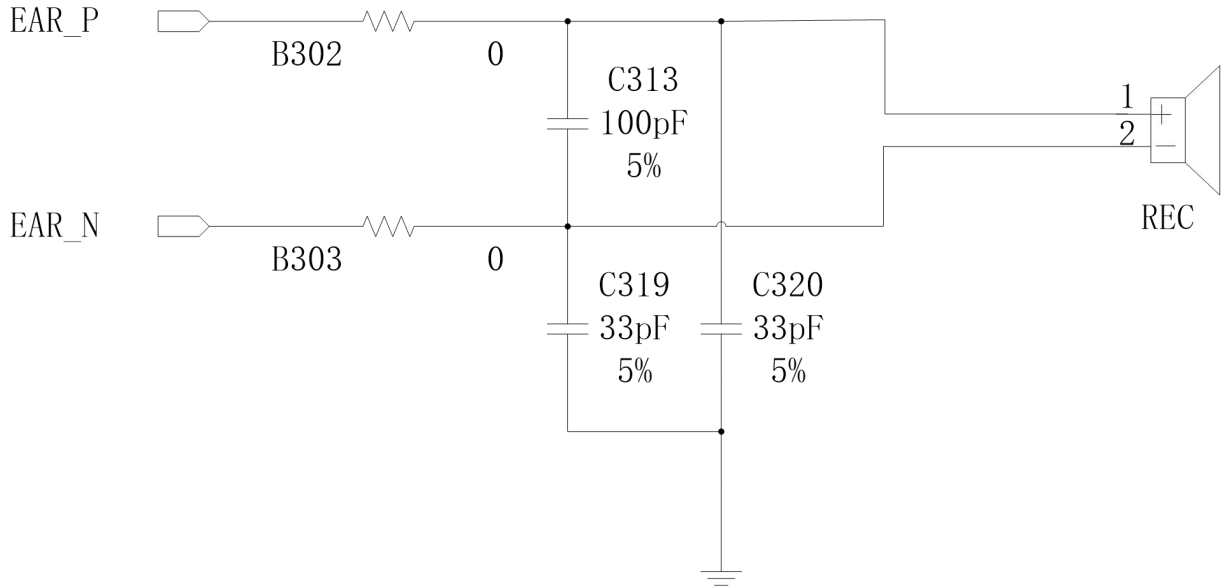
Fig4.20：Receiver interface circuit

4.8.2.Microphone Receiving Circuit

MIC_BIAS1

If use ECM mic,OR
If use MEMS mic, 100nF

MIC_IN1_P

100nF B300

100pF

MIC
1
2

POWER

4 OUTPUT MIC301
NSM0402AT

100nF
10%

GND GND

MIC_IN1_M 100nF B301

33pF 33pF

OR

If use ECM mic
Removed this circuit
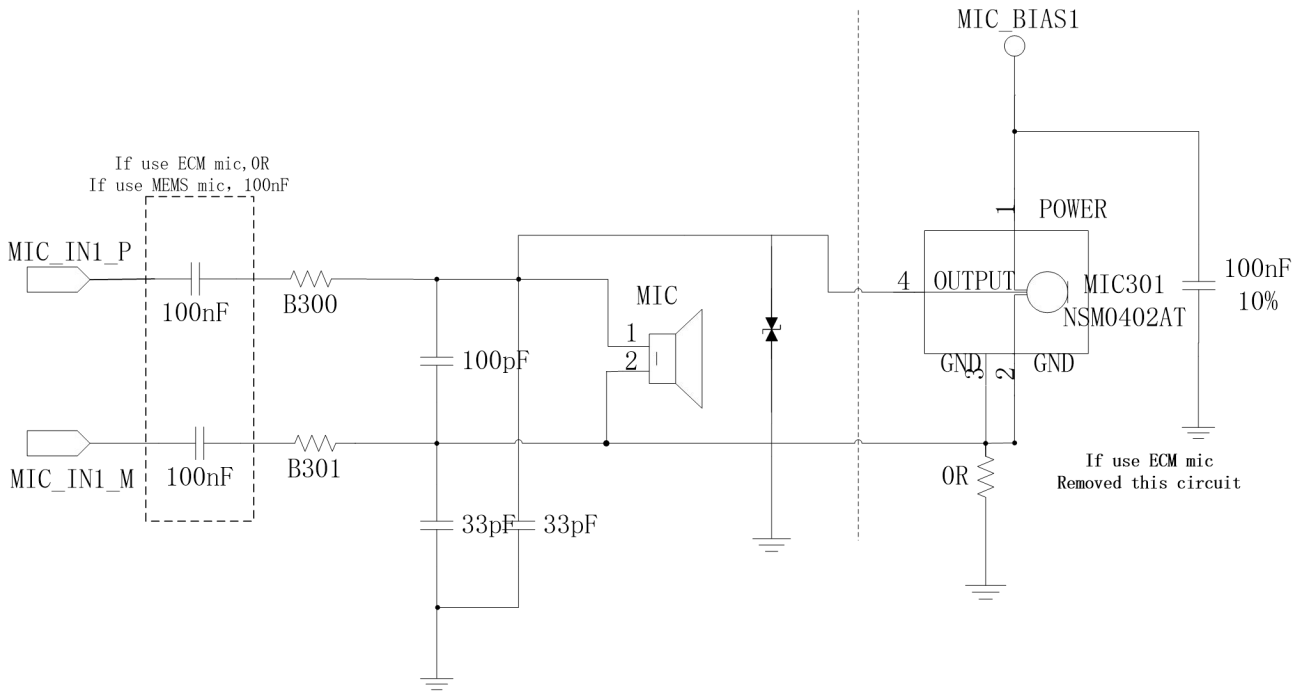
Fig4.21：Microphone interface circuit

4.8.3.Headphone Interface Circuit

The module integrates a stereo headphone jack. You are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as interrupt. By default, this pin is headset interrupt in the software. Users can use this pin to detect the plug and unplug of the headset.

Note: HP_L must increase the pull-down resistance of 100K.
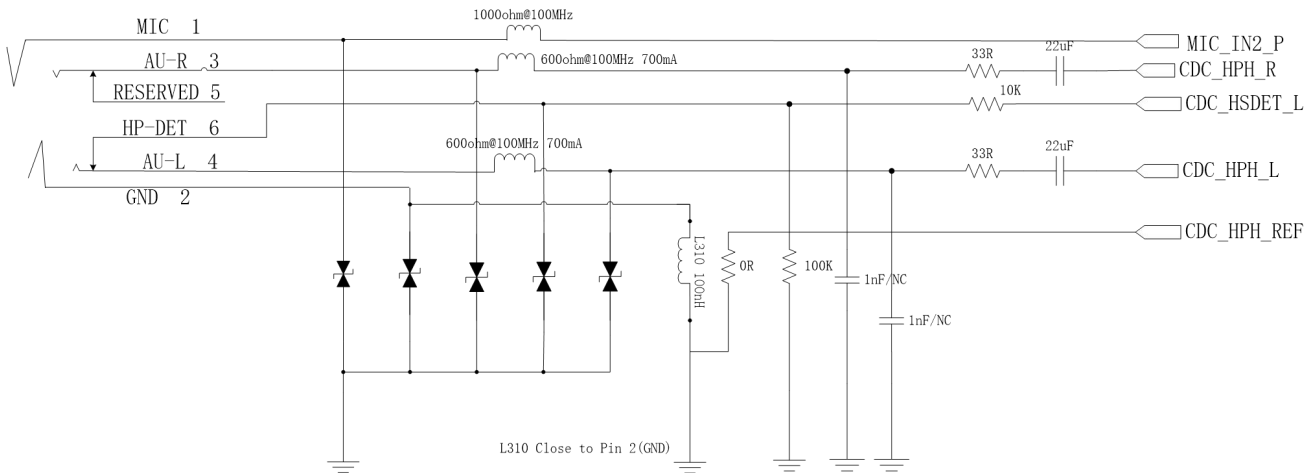
Fig4.22：Headphone interface circuit

Note:1. The headphone holder in Figure 4.24 is type NO. If NC headphone is used, 10K is reserved on HP_DET and pulled up to VDD_2V8.

4.8.4.Speaker Interface Circuit

The speaker interface adopts differential output, with built-in class D power amplifier driver. Under 4.2V VBAT power supply, the typical output power is 800mW when the load is 8 ω, and the output signal is SPKR_OUT_P/SPKR_OUT_M.
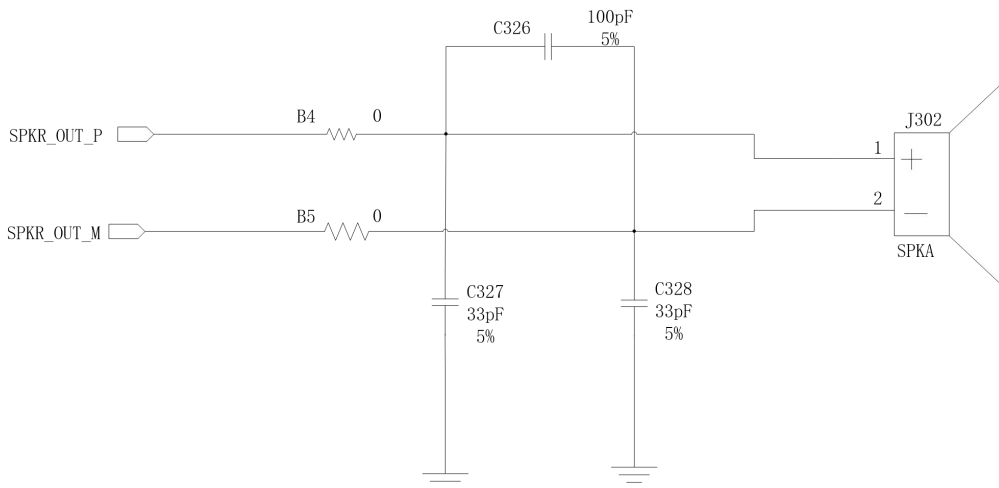
Fig4.23：Internal audio amplifier circuit

You can also add an audio power amplifier externally and use HPH_R as a single-ended input signal. The reference circuit is shown in the figure below.
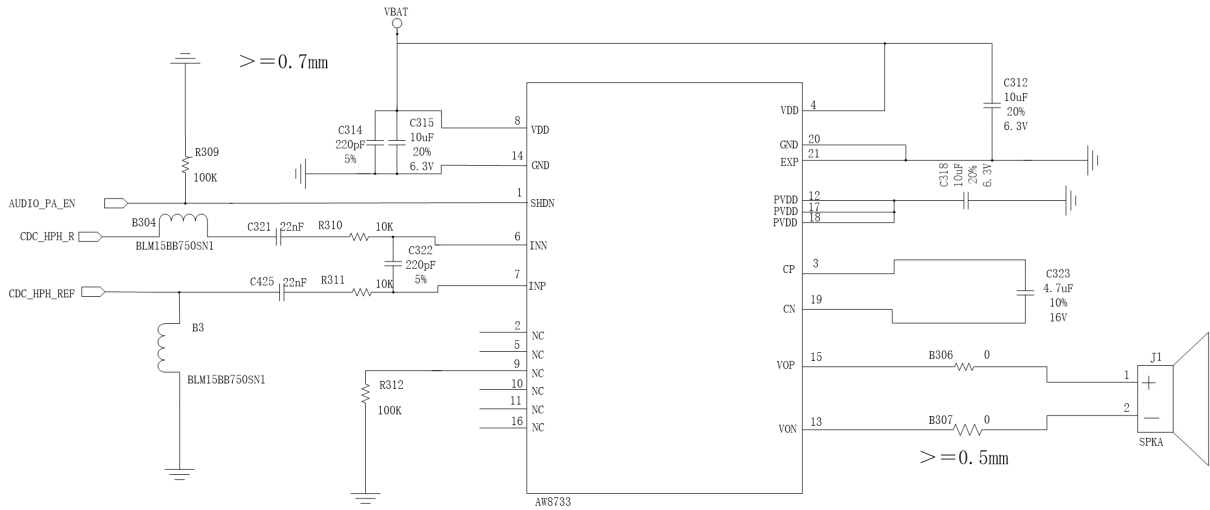
4.24：Recommended circuit with external audio amplifier

4.8.5 SPI Interface

There are two sets of GPIO compatible I2S interfaces inside the module. The pins used for this function are listed below:

Name	Pin	IN/OUT	Description
GPIO90	117	DO	SPI0_CS
GPIO91	119	DO	SPI0_DO
GPIO92	118	DI	SPI0_DI
GPIO93	116	DO	SPI0_ CLK
GPIO52	107	DO	SPI2_CS
GPIO53	108	DO	SPI2_DO
GPIO54	109	DI	SPI2_DI
GPIO55	110	DO	SPI2_ CLK

4.9.USB Interface

The SLM500S supports a USB 2.0 High Speed interface. The 90 ohm differential impedance must be controlled during Layout and the external cable length must be controlled according to the cable length inside the module. The module also supports OTG function. OTG power supply needs external IC power supply.

The voltage input range during charging is as follows:

Table 4.8:Voltage input range during charging

PIN	Min	Typical	Max	Unit

VBUS	4.5	-	9.7	V

The USB insertion detection of the module is realized by VBUS and DP/DM data cable. When the USB cable is inserted, the VBUS voltage is detected first, and then the USB cable or charger is determined by detecting the pull up and down state of DM/DP. Therefore, if the user needs to use USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is in high-speed mode. You are advised to connect a serial common-mode inductor close to the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. It is recommended to add TVS to prevent electrostatic damage caused by plugging and unplugging data cables. Users should notice that the load capacitance of TVS should be less than 1PF when selecting TVS. The connection diagram is as follows:

Fig4.25：USB Connection diagram
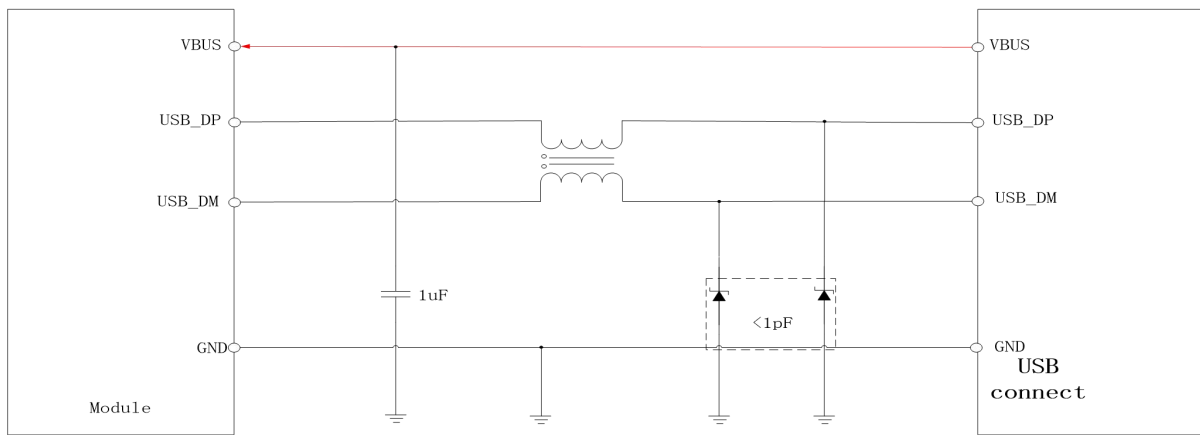
4.9.1.USB OTG

The SLM500S module provides the USB OTG function, which uses the following pins:

Table 4.19:USB OTG

Name	Pin	Description
VBUS	141、142	OTG power supply requires external IC power supply
USB_DM	13	USB DATA-
USB_DP	14	USB DATA+
USB_ID	16	USB ID

The recommended circuit diagram of USB_OTG is shown below:
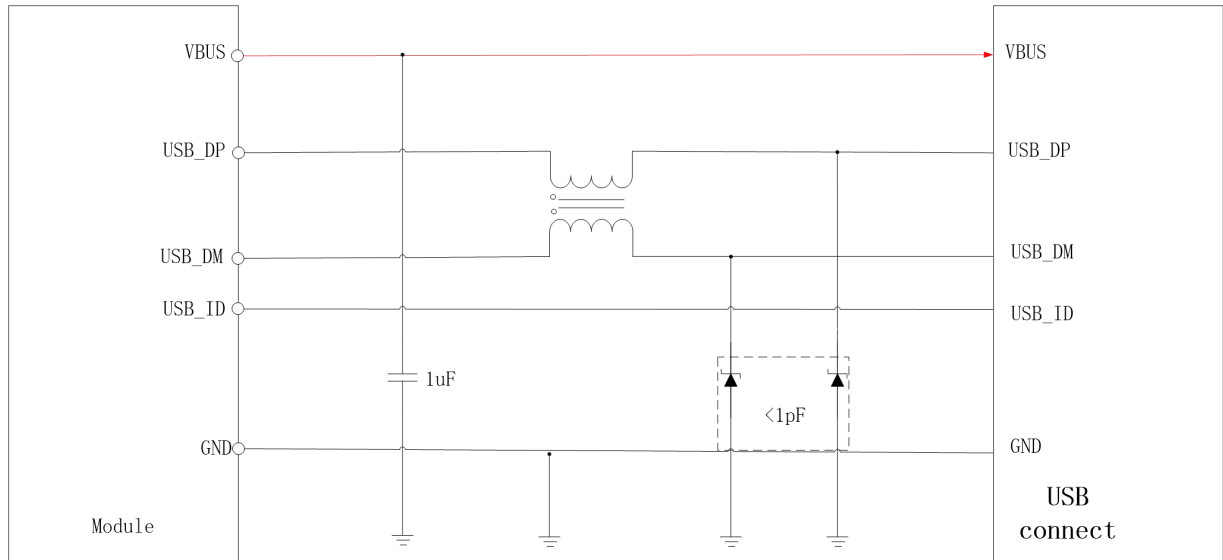
Fig4.26：Schematic of USB-OTG connection

4.10.Charging Interface

The SLM500S module is integrated with 1A linear charging scheme. The charging contents in this manual are explained only by the internal charging scheme. The SLM500S module can charge over discharged batteries, including trickling charge, constant current charge, and constant voltage charge.

Trickle charging: it is divided into two parts, trickle charging -A: when the battery voltage is lower than 2.05V, the charging current is 70mA; Trickle charging -B: the charging current is 450mA when the battery voltage is between 2.05V and 3.05V;

Constant current charging: when the battery voltage between 3.05V and 4.18V constant current charging, adapter charging charging current 1.0A, USB charging current 450mA;

Constant voltage charging: when the battery voltage reaches 4.18V, it enters the constant voltage charging, the charging current gradually decreases, the charging current decreases to about 100mA, and the charging ends.
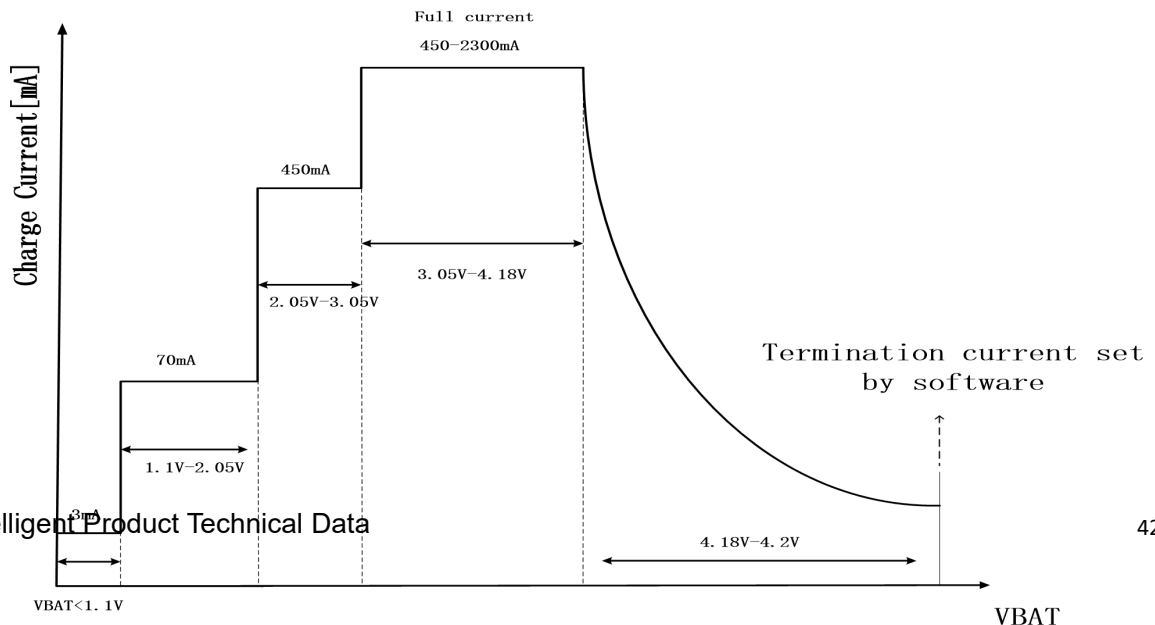
Fig4.27：Charging diagram

4.10.1.Charging Detection

When the VBUS PIN voltage is higher than 4.0V, a hardware interrupt will occur inside the module, and the software will judge USB_HS_DP/USB_HS_DM status to identify whether the charger or USB data cable is inserted.

4.10.2.Charge Control

The SLM500S module can charge over discharged batteries, including trickle charge, pre-charge, constant current charge, and constant voltage charge. When the VBAT voltage is lower than 3.05V, the module is pre-charged. When VBAT is between 3.05V and 4.2V, the optimal constant current and constant voltage charging method for lithium battery is adopted. The current charging cut-off voltage of the software is 4.2V, and the back flush voltage is 4.05V.

4.10.3.BAT_THERM

The SLM500S module comes with battery temperature detection, which you can implement with BATT_THERM (134PIN). This requires the battery to integrate an NTC resistor (negative temperature coefficient) at room temperature of 10K ω and connect the NTC resistor pin to the BATT_THERM pin. During the charging process, the software reads the voltage of the BATT_THERM pin to determine whether the battery temperature is too high. If it is found to be too high or too low, it will immediately stop charging to prevent battery damage. The schematic diagram of battery charging connection is shown below.
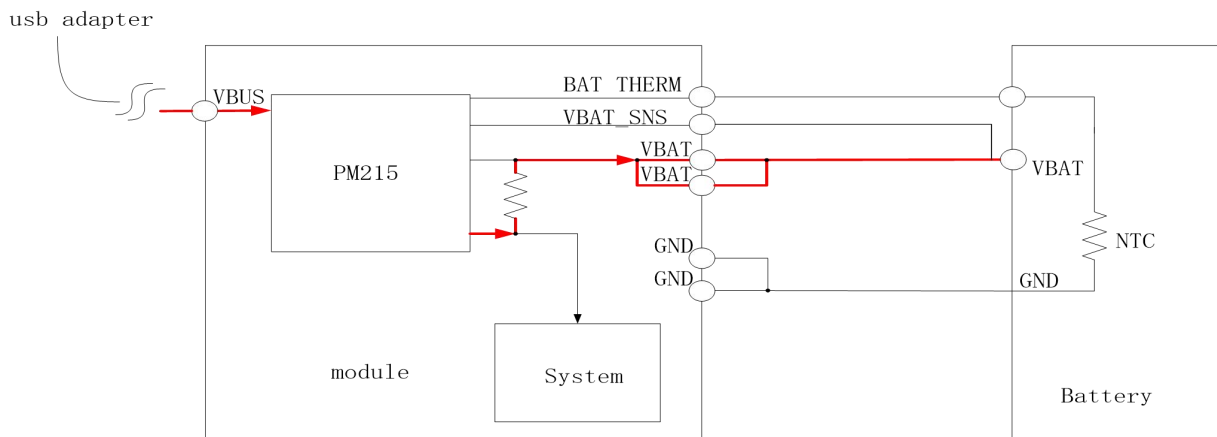
Fig4.28：Charging circuit connection diagram

4.11.UIM Interface

The SLM500S supports two SIM card interfaces to achieve dual-card dual-standby. It supports hot swap of SIM cards and automatically identifies 1.8V and 3.0V cards. Below is the recommended SIM interface circuit. To protect SIM cards, TVS devices are recommended for static protection. The peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:
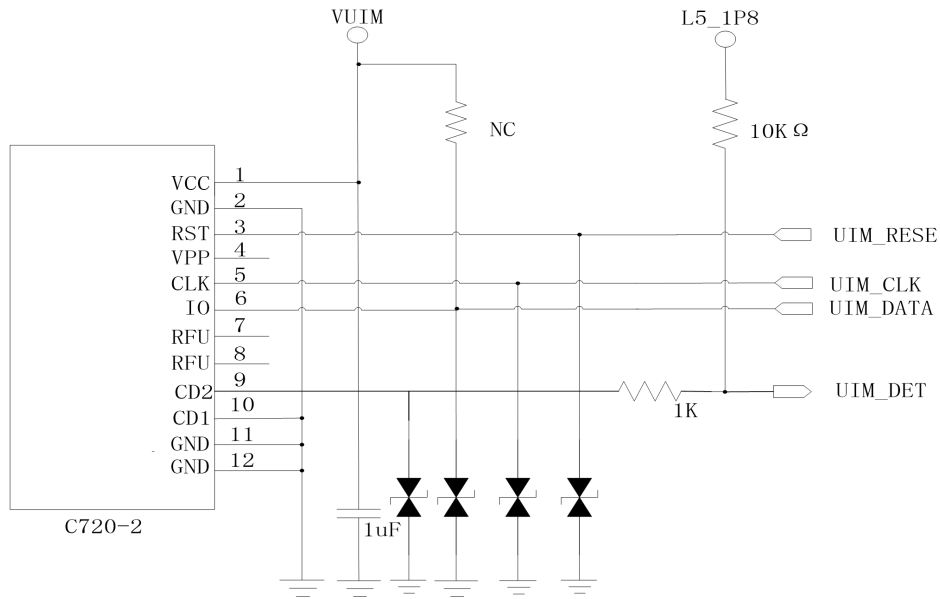
Fig4.29：UIM card interface circuit

4.12.SD Interface

The SLM500S supports SD card interfaces with a maximum of 256GB.

The reference circuit is as follows:
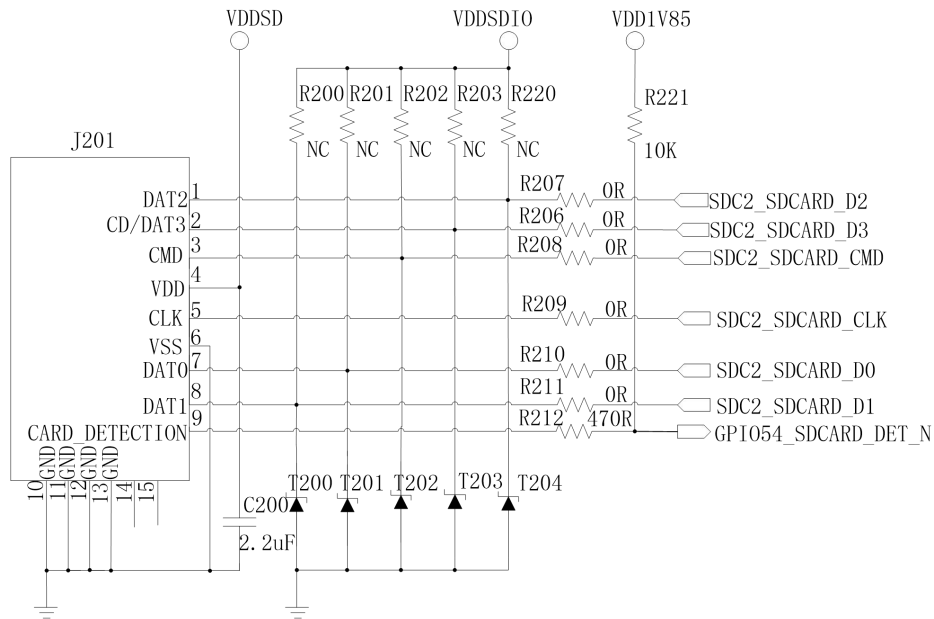
Fig4.30： SD interface circuit

4.13.I2C Bus Interface

SLM500S module supports four hardware I2C bus interfaces, including one Camera dedicated CCI interface. Pin definitions and default functions are as follows:

Table 4.10:I2C interface

Name	Pin	Description
CAM_I2C_SCL	83	Camera I2C
CAM_I2C_SDA	84	
TP_I2C_SCL	47	Universal I2C, default for TP
TP_I2C_SDA	48	
SENSOR_I2C_SCL	91	General I2C
SENSOR_I2C_SDA	92	
I2C4_SDA	167	General I2C
I2C4_SCL	168	

4.14.ADC

The SLM500S module uses a power management chip to provide two ADC functional signals: ADC (128PIN) and BAT_ID (185PIN).

ADC signal has a resolution of 12bit, and its performance parameters are as follows:

Table 4.11:ADC performance parameters

Describe	Minimum	Typical	Maximum	Unit
Input Voltage Range	-	1.2	-	V
ADC Resolution	-	-	12	bits
Sampling Frequency	-	49	-	kHz

4.15.PWM

PWM pin can be used to do LCD backlight adjustment, by adjusting the duty ratio to adjust the backlight brightness.

4.16.MOTOR

The SLM500S supports motor function, which can be achieved by VIB_DRV_P (28PIN). The reference schematic diagram is as follows:
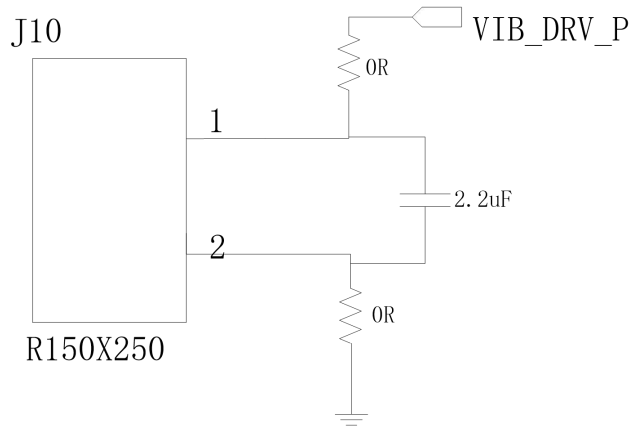
Fig4.31：motor Interface circuit

4.17. Antenna Interface

The module provides four antenna interfaces: MAIN antenna, DRX antenna, GPS antenna and WiFi/BT antenna. To ensure good wireless performance of the user's product, the user should select an antenna whose input impedance is 50 ohm and standing wave coefficient is less than 2 in the working frequency band.

4.17.1.Main Antenna

The module provides the MAIN antenna interface pin RF_MAIN. The antenna on the user's MAIN board shall be connected to the antenna pin of the module with a characteristic impedance of 50 ohm micros trip line or ribbon line.

To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:
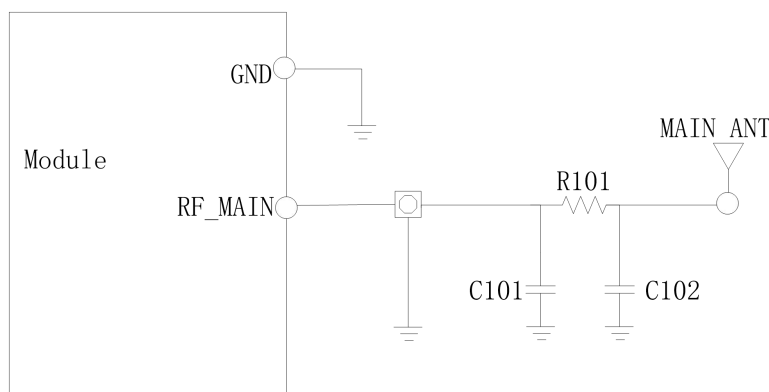
Fig4.32：MAIN Antenna interface connects the circuit

In the figure, R101, C101 and C102 are antenna matching devices. The specific component values can be determined after the antenna is debugging in the antenna factory. 0R is displayed by default for R101, and not for C101 and C102.

If there are fewer components that can be placed between the antenna and the output end of the module, or RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the figure below:

Fig4.33：MAIN antenna interface simplifies the connection circuit

Note: In the figure above, R101 is pasted by default, C101 and C102 are not pasted by default.

4.17.2.DRX Antenna

The module provides the DRX antenna interface pin RF_DIV. The antenna on the user's motherboard shall be connected to the antenna pin of the module using a micro strip line or ribbon line with a characteristic impedance of 50 ohm.

To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:
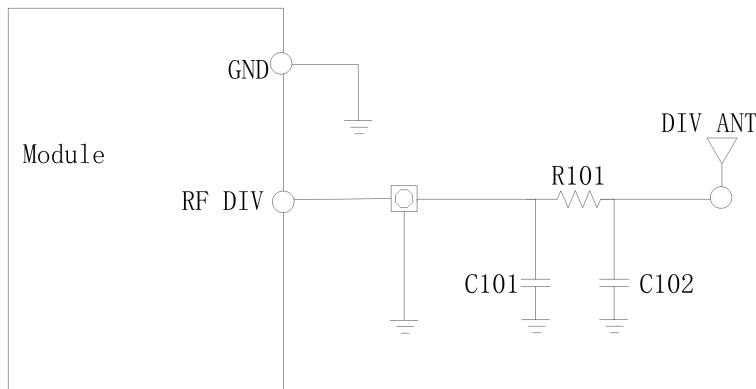
Fig4.34：The DRX antenna port connects to the circuit

Note: R102, C103, C104 are antenna matching devices, the specific component value can be determined after the antenna is debugging in the antenna factory. 0R is attached by default to R102, C103 and C104 are not attached by default.

If there are fewer components that can be placed between the antenna and the output end of the module, or RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the figure below:
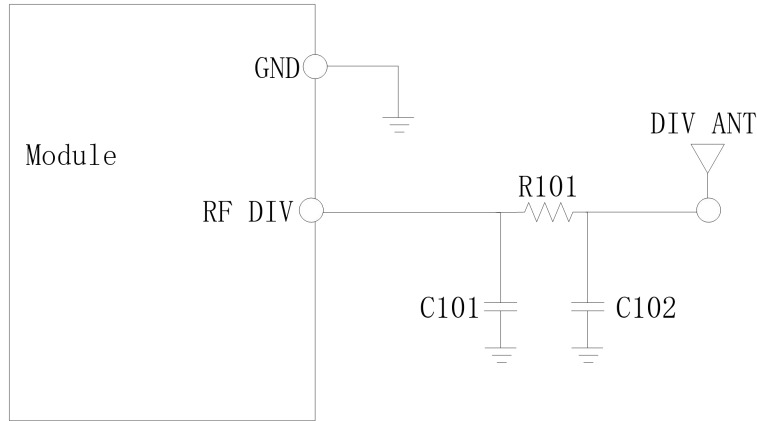
Fig4.35：The DRX antenna port simplifies the connection circuit

Note: R102 default paste 0R, C103 and C104 default do not paste.

4.17.3.GPS Antenna

GNSS antenna pin RF_GPS is provided by the module. The antenna on the user's motherboard shall be connected to the antenna pin of the module using a micros trip line or ribbon line with a characteristic impedance of 50 ohm.

LNA is integrated in the module.

To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connection is shown in the figure below:
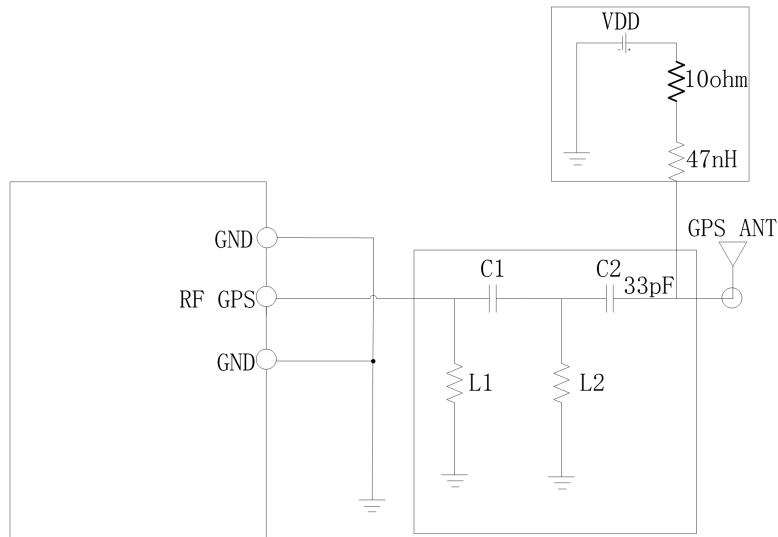
Fig4.36：Connect active antenna

4.17.4.WiFi/BT Antenna

The module provides WiFi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard shall be connected to the antenna pin of the module using a microstrip line or ribbon line with a characteristic impedance of 50 ohm.
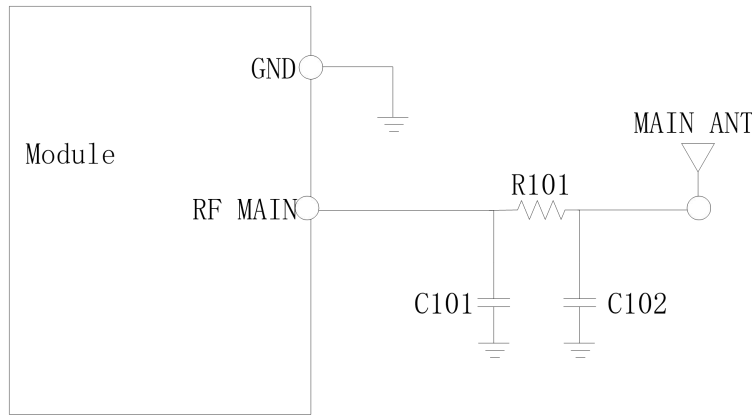
To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:
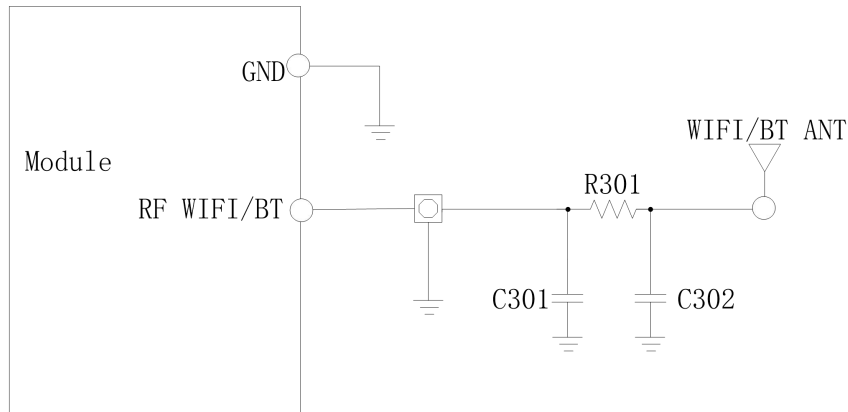
Fig4.37：WiFi_BT antenna interface connection circuit

Note: R301, C301, C302 are antenna matching devices. The specific component values can be determined after the antenna is debugging in the antenna factory. 0R is displayed by default for R301, C301 and C302 are not displayed by default.

If there are fewer components that can be placed between the antenna and the output end of the module, or RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the figure below:
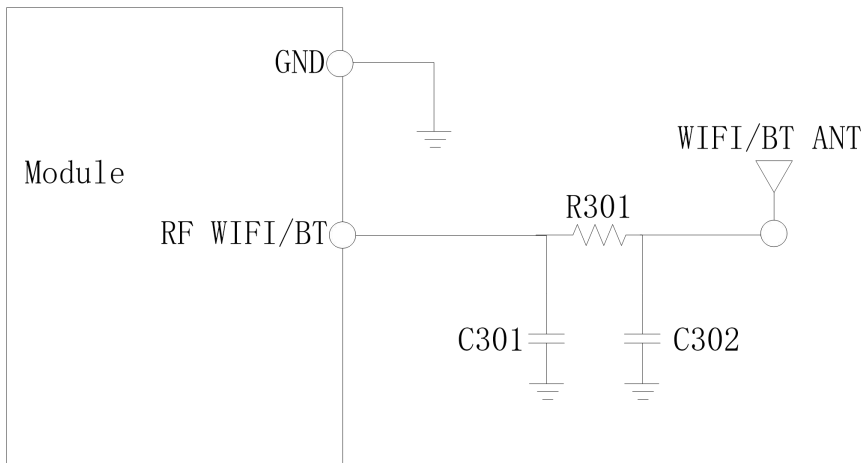

Fig4.38：WIFI_BT antenna interface simplifies connection circuit

Note: R301 is pasted by default, C301 and C302 are not pasted by default.

5.Electrical, Reliability

5.1.Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits may cause permanent damage to the module.

Table 5.1:Absolute maximum

Parameter	Min	Typical	Max	Unit
VBAT	-	-	6	V
VBUS	-	-	12	V
Peak current	-	-	3	A

5.2.Working Temperature

The following table shows the operating temperature range of the module:

Table 5.2:Module operating temperature

Parameter	Min	Typical	Max	Unit
Working temperature	-25	-	75	℃
Storage temperature	-40	-	90	℃

5.3.Working Voltage

Table 5.3:Module operating voltage

Parameter	Min	Typical	Max	Unit
VBAT	3.5	3.8	4.2	V
VBUS	4.5	5	9.2	V
Hardware shutdown voltage	3.4	-	-	V

5.4. Digital Interface Features

Table 5.4: Digital Interface Features (1.8V)

Parameter	Description	Min	Typical	Max	Unit
VIH	Input high level voltage	1.26	-	-	V
VIL	Input low level voltage	-	-	0.54	V
VOH	Output high level voltage	1.6	-	-	V
VOL	Output low level voltage	-	-	0.2	V

5.5. SIM_VDD Features

Table 5.5: SIM_VDD Features

Parameter	Description	Min	Typical	Max	Unit
VO	Output voltage	-	3	-	V
		-	1.8	-	
IO	Output current	-	-	50	mA

5.6. PWRKEY Features

Table 5.6: PWRKEY features

Parameter	Description	Min	Typical	Max	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Valid time	3000			ms

5.7. VCOIN Features

Table 5.7: VCOIN features

Parameter	Description	Min	Typical	Max	Unit
VCOIN-IN	VCOIN Input voltage	2.5	3.0	3.1	V
VCOIN-OUT	VCOIN Output voltage	-	3.0	3.35	V

5.8.Consumption（VBAT=3.8V）

Table 5.8:Consumption

Parameter	Description	Conditions	Min	Typical	Max	Unit
VBAT	Power supply voltage	The voltage must be between the maximum and minimum	3.5	3.8	4.2	V
Ivbat	Average current	Shutdown mode	-	-	67	uA
		GSM Standby consumption	-	2.36	-	mA
		WCDMA Standby consumption	-	2.99	-	mA
		FDD Standby consumption	-	3.47	-	mA
		TDD Standby consumption	-	2.98	-	mA
	Call flow consumption	GSM900 CH62 32dBm	-	-	278.11	mA
		WCDMA2100 CH10700 22.5 dBm	-	-	490.18	mA
	Digital transmission	GPRS GSM900 CH62 PCL5 1DL 4UL	-	-	547.6	mA
		EGPRS GSM900 CH62 PCL8 1DL 4UL	-	-	535.5	mA
Imax	Peak current	Power is controlled at maximum output power	-	-	3	A

5.9.Electrostatic Protection

The module is not protected against electrostatic discharge. Therefore, you must pay attention to ESD protection when producing, assembling, and operating modules.

5.10.Module Operating Frequency Band

The following table lists the operating bands of the modules in accordance with 3GPP TS 05.05 technical specification.

Table 5.9:Module operating frequency band

Band	Receiving	Transmitting	Physical Channel
GSM850	869～894MHz	824～849MHz	128~251
EGSM900	925～960MHz	880～915MHz	0~124，975~1023
DCS1800	1805 ～1880MHz	1710 ～1785MHz	512~885
PCS1900	1930 ～1890MHz	1850 ～1910MHz	512~661
WCDMA B1	2110 ～2170 MHz	1920～1980 MHz	TX: 9612~9888

			RX: 10562~10838
WCDMA B5	869~894MHz	824~849MHz	TX: 4132~4233
			RX: 4357~4458
WCDMA B8	880~915MHz	925~960MHz	TX: 2712~2863
			RX: 2937~3088
LTE B1	2110~2170 MHz	1920~1980 MHz	TX: 18000~18599
			RX: 0~599
LTE B3	1805~1880 MHz	1710~1785 MHz	TX: 19200~19949
			RX: 1200~1949
LTE B5	869~894MHz	824~849MHz	TX: 20400~20649
			RX: 2400~2649
LTE B7	2620~2690MHz	2500~2570MHz	TX: 20750~21449
			RX: 2750~3449
LTE B8	925~960MHz	880~915MHz	TX: 21450~21799
			RX: 3450~3799
LTE B20	791~821MHz	832~862MHz	TX: 24150~24449
			RX: 6150~6449
LTE B34	2010~2025 MHz	2010~2025 MHz	36200~36349
LTE B38	2570~2620 MHz	2570~2620 MHz	37750~38249
LTE B39	1880~1920 MHz	1880~1920 MHz	38250~38649
LTE B40	2300~2400 MHz	2300~2400 MHz	38650~39649
LTE B41	2496~2690 MHz	2496~2690 MHz	39650~41589

Note: THE LTE TDD B41 band bandwidth of SLM500S is 100MHz (2555 ~ 2655 MHz), and the channel is 40240 ~ 41240.

5.11.RF Characteristics

The table below lists the conducted RF output power of the module in accordance with 3GPP TS 05.05 technical specification, 3GPP TS 134121-1 standard.

Table 5.10:Conducted output power

Band	Standard Output(dBm)	Output Tolerance(dBm)
GSM850、EGSM900	33dBm	±2
DCS1800	30dBm	±2
WCDMA	24 dBm	+1/-3
LTE	23 dBm	±2.7

5.12.Module Conduction Receiving Sensitivity

The following table lists the conductive reception sensitivity of the module, which is tested under static conditions.

Table 5.11:Conduction reception sensitivity

Band	Reception Sensitivity（TYP）	Reception Sensitivity（MAX）
GSM850、EGSM900	<-108dBm	3GPP
DCS1800、PCS1900	<-108dBm	3GPP
WCDMAB1	<-109 dBm	3GPP
WCDMAB5	<-109 dBm	3GPP
WCDMAB8	<-109 dBm	3GPP
LTEFDD/TDD	Shown in Table 6.12	3GPP

Table 5.12:LTE reference sensitivity 3GPP Dual Antenna Requirements (QPSK)

E-UTRA Band Number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD
6	-	-	-100	-97			FDD
7	-	-	-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
9	-	-	-99	-96	-94.2	-93	FDD
10	-	-	-100	-97	-95.2	-94	FDD
11	-	-	-100	-97			FDD
12	-101.7	-98.7	-97	-94			FDD
13			-97	-94			FDD
14		-	-97	-94			FDD
...							
17	-	-	-97	-94			FDD
18	-	-	-1007	-977	-95.27	-	FDD
19	-	-	-100	-97	-95.2	-	FDD
20			-97	-94	-91.2	-90	FDD
21			-100	-97	-95.2		FDD
22			-97	-94	-92.2	-91	FDD
23	-104.7	-101.7	-100	-97	-95.2	-94	FDD
24			-100	-97			FDD

25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
26	-102.7	-99.7	-97.56	-94.56	-92.76		FDD
27	-103.2	-100.2	-98	-95			FDD
28		-100.2	-98.5	-95.5	-93.7	-91	FDD
31	-99.0	-95.7	-93.5				FDD
...							
33	-	-	-100	-97	-95.2	-94	TDD
34	-	-	-100	-97	-95.2	-	TDD
35	-106.2	-102.2	-100	-97	-95.2	-94	TDD
36	-106.2	-102.2	-100	-97	-95.2	-94	TDD
37	-	-	-100	-97	-95.2	-94	TDD
38	-	-	-100	-97	-95.2	-94	TDD
39	-	-	-100	-97	-95.2	-94	TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-98	-95	-93.2	-92	TDD

5.13.WIFI Main RF Performance

The following table lists the main RF performance under WIFI conduction.

Table 5.13:WIFI Main RF performance parameters under conduction

Launch Performance 2.4G				
	802.11B	802.11G	802.11N	
Transmitted power (minimum rate)	19	17	16	dBm
Transmitted power (maximum rate)	18	15	13	dBm
EVM (Maximum rate)	20%	-27	-30	dB
Receiving Performance 2.4G				
Reception sensitivity	802.11B	802.11G	802.11N	
Minimum speed	-89	-88	-87	dBm
Maximum speed	-86	-71.5	-69.5	dBm

5.14.BT Main RF Performance

The following table lists the main rf properties under BT conduction.

Table 5.14:Main RF performance parameters under BT conduction

Launch Performance			
Transmission power	DH5	2DH5	3DH5	
	10	6	6	dBm
Receiving Performance			
Reception sensitivity	DH5	2DH5	3DH5	
	-91.5	-91.5	-83	dBm

5.15.Main RF Performance of GNSS

The main RF performance under GNSS conduction is listed in the following table.

Table 5.15:Main RF performance parameters under GNSS conduction

GNSS Working Band:1575.42MHZ			
GNSSC Carrier to noise ratioN0：40dB/Hz			
GNSS Sensitivity：	Capture (cold start)	Capture (hot start)	tracking	
	-148	-156	-160	dBm
GNSS Startup time	hot start	start	cold start	
	5	10	38	S

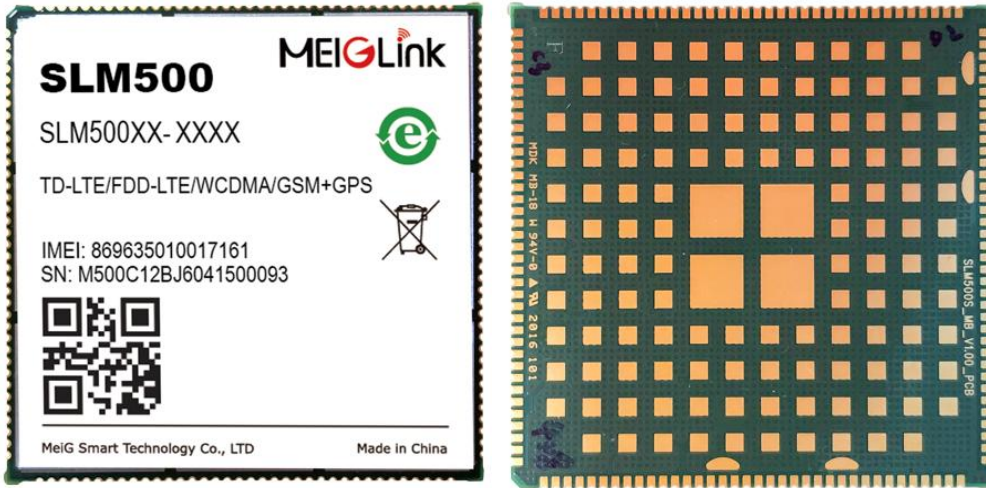# 6.Production

6.1.Top and Bottom Views of Modules

Fig6.1：Top and bottom views of modules

6.2.Recommended Welding Furnace Temperature Curve

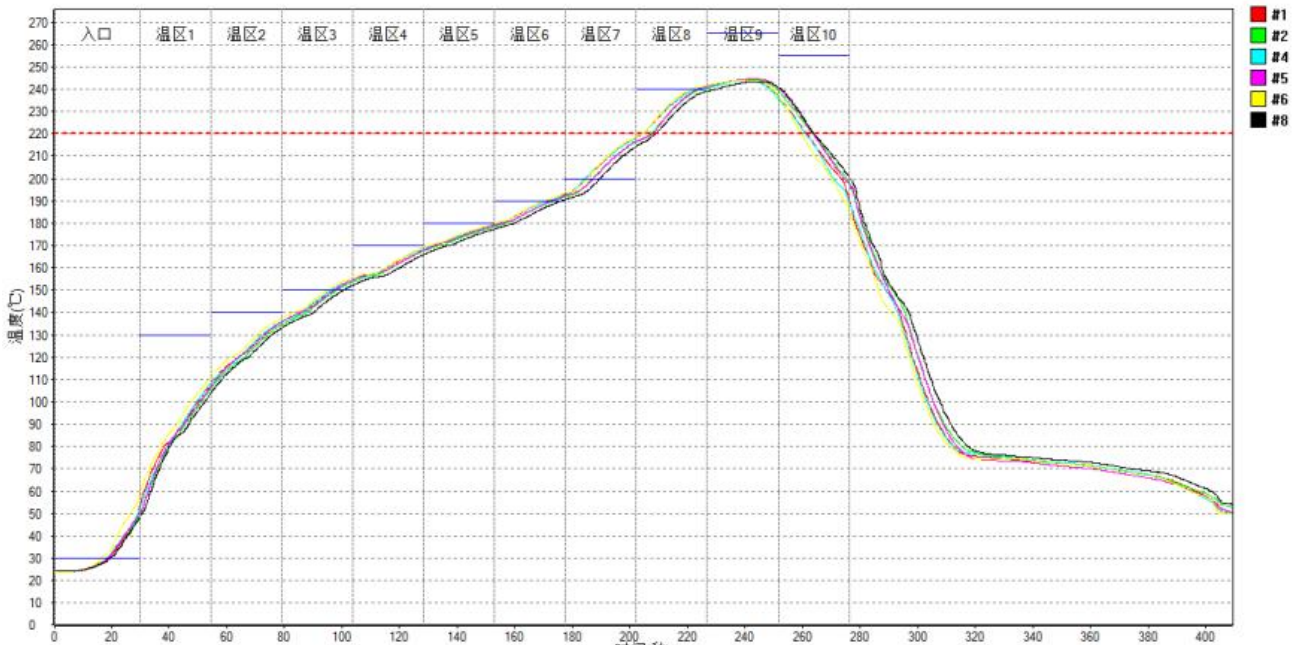**Fig6.2：Recommended welding furnace temperature curve**

6.3.Humidity Sensitive Characteristic (MSL)

The SLM500S meets humidity sensitivity level 3. The temperature & lt; 30 degrees and relative humidity < 60% of the environmental conditions, dry packaging according to IPC/JEDEC standard J-STD-020C specification. The temperature & lt; 40 degrees and relative humidity < Shelf life is at least 6

months when unopened in 90% of environmental conditions. After unpacking, table 22 lists the shelf life of modules corresponding to different moisture sensitivity levels.

Table 6.1:Humidity sensitivity level differentiation

Level	Factory environment ≦ 30℃/60%RH
1	Indefinite quality at ambient ≦ 30℃/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Force bake before use. After baking, the module must be fitted within the time limit specified on the label.

After unpacking, at temperature < 30 degrees and relative humidity < SMT within 168 hours in 60% of environmental conditions. Bake if the above conditions are not met. Note: Oxidation risk: Baking SMD packaging can cause metal oxidation and, if excessive, can lead to solder ability problems during circuit board assembly. Baking SMD packages for temperature and time, thus limiting solder ability considerations. The accumulated baking time at temperatures greater than 90°C and up to 125°C should not exceed 96 hours.

6.4.Baking Requirements

Due to the moisture sensitive nature of the modules, the SLM500S should be fully baked before reflow soldering, otherwise the modules may be permanently damaged during reflow soldering. The SLM500S should be baked for 192 hours at 40°C +5°C /-0°C with relative humidity less than 5%, or the module should be baked for 72 hours at 80°C +5°C. The user should be aware that the tray is not resistant to high temperatures and should remove the module from the tray for baking, otherwise the tray may be damaged by high temperatures.

Table 6.2:Baking needs:

Baking Temperature	Humidity	Baking Time
40°C±5°C	<5%	192 hours
120°C±5°C	<5%	4 hours

7.Appendix

7.1.The related documents

Table 7.1:The related documents

#	File Name	Comment
[1]	GSM 07.07：	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10：	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05：	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14：	Digital cellular telecommunications system (Phase 2+);Specification of the UIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (UIM–ME) interface
[5]	GSM 11.11：	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (UIM–ME) interface
[6]	GSM 03.38：	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)；Mobile Station (MS) conformance specification；Part 1：Conformance specification
[8]	AN_Serial Port	AN_Serial Port

7.2.Terminology and Interpretation

Table 7.2:Terminology and Interpretation

Term	Explanation
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM

ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
UIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Telephone book abbreviation	explain
FD	UIM fix dialing phonebook
LD	UIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	UIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	UIM phonebook

NC	Not connect

MeiG Intelligent Technology Co., LTD

Address: 5th floor, Building G, Vijing Center, 2337 Gudai Road, Minhang District, Shanghai

Zip code：200233

Tel：+86-21-54278676

Fax：+86-21-54278679

Web： http://www.meigsmart.com

Doc：

Products with CE Marking comply with the radio Equipment Directive（2014/53/EU）and

UK Radio Equipment Regulations (SI 2017/1206) The full text of the EU declaration of conformity

is available at the following internet address: http://www.meigsmart.com

RF exposure statement：

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of d=20 cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

Temperature: -40°C ~ +75°C

Bands:

The Radio equipment operation with following frequecy bands Maximum tune-up power(dBm)

BT3.0: 5dBm(eirp)

Ble: 5dBm(eirp)

2.4GWIFI:17.83dBm(eirp)

GSM 900:32dBm

GSM 1800:31dBm

WCDMA band8:23dbm

LTE Band7:24dbm

LTE Band8:24dbm

LTE Band28:24dbm

LTE Band34:24dbm

LTE Band38:24dbm

LTE Band40:24dbm

15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

15.21 Changes or modification warning.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help

RF warning for Mobile device:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 15

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not application

2.5 Trace antenna designs

Not application

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

Antenna Type(Dipole)	BT/2.4Gwifi 1.77 dBi;
Antenna connector	R-SMA

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2APJ4-SL500SA". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment