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SLM756 Hardware Design Guide

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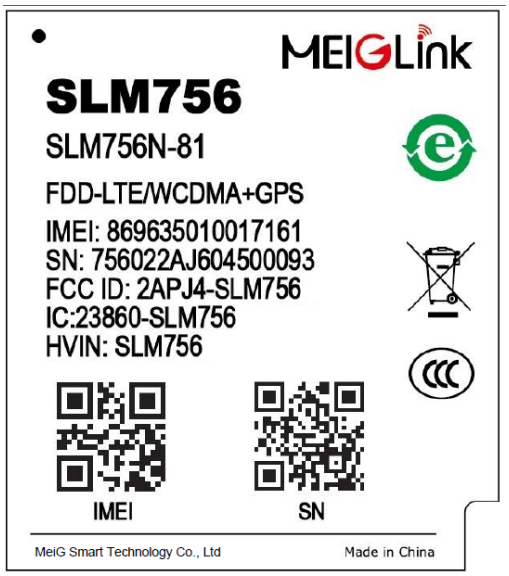

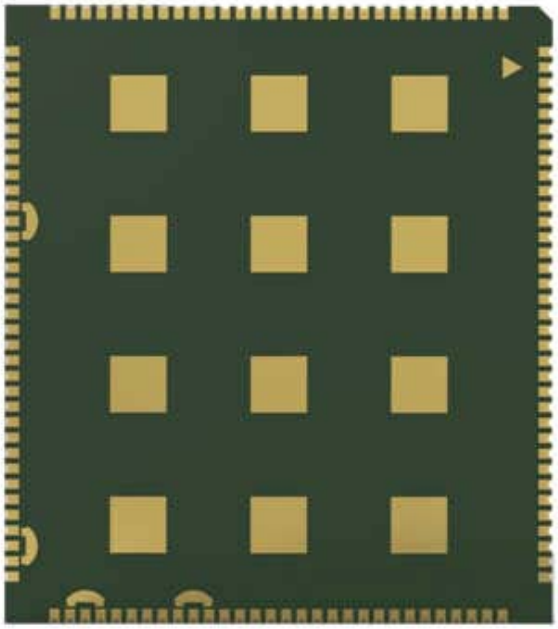

Foreword

Thank you for using the SLM756 module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

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Version History

Date	Version	Change description	Author
2017-10	1.00	First edition	Zheng Lei
2018-2	1.01	Modify the description of the 4.18.3 GPS antenna section	Zheng Lei
2018-8	1.02	Increase I2S information	Zheng Lei
2018-9	1.03	Update image information	Zheng Lei
2018-11	1.04	Update reset, GPS and baking information	Zheng Lei

1.Introduction

This document describes the hardware application interface of the module, including the circuit connections and RF interfaces of the relevant applications. It can help users quickly understand the module's interface definition, electrical performance and structural size details. Combined with this and other application documents, users can quickly use modules to design mobile communication applications.

2.Module Overview

The SLM756 module uses the Qualcomm MSM8909 platform solution, the MSM8909 processor is manufactured in a 28nm LP CMOS process, the quad core clocked at 1.1GHz, and the memory supports 8GB+1GB (compatible with 16GB+2GB) LPDDR3. The chip can support WCDMA, FDD-LTE and other standards, and is a highly integrated product.

For FCC
The working frequency bands that the SLM756 module can support are:

- FDD-LTE: B2/4/5/7/12/13/17
- WCDMA: B2/B4/5

The physical interface of the module is a 210-pin pad that provides the following hardware interfaces:

- Two serial ports, including one four-wire serial port and one two-wire serial port.
- LCM (MIPI interface).
- Two-way Camera interface (MIPI data).
- A high-speed USB interface.
- Three audio input interfaces.
- Three-channel audio output interface.
- Two-way UIM card interface.
- GPIO interface.
- Four sets of I2C interfaces.
- A set of SPI interfaces.
- A TF card interface.
- Support GNSS, WiFi, Bluetooth4.1, FM function.

2.1 Summary of features

Table 2.1：SLM756 features

Product characteristics		Description
Plateform		Qualcomm MSM8909
CPU		Quad-core A7 (32bit) 1.1GHz
GPU		A304 409.6MHz
System memory		8GB eMMC + 1GB LPDDR3
OS		Android 5.1
Size		44.0x39.0x3.0mmA LCC+LGA130pin
SLM756 Network band	-NA (North America)	FDD-LTE: B2/4/5/7/12/13/17 WCDMA: B2/4/5
	-CH (China)	FDD-LTE:B1/3 TDD-LTE:B38/39/40/41 TDSCDMA:B34/39 WCDMA:B1/8 CDMA 1X/EVDO:BC0 GSM:B3/5/8
	-EU (Eurasian, Middle East)	FDD-LTE:B1/3/5/7/8/20 TDD-LTE:B38/40/41 WCDMA:B1/5/8 GSM:B3/5/8
	-LA (Latin America, Australia, Taiwan)	FDD-LTE:B1/3/5/7/8/28 TDD-LTE:B40 WCDMA:B1/2/5/8 GSM:B2/3/5/8
Wi-Fi		IEEE 802.11b/g/n 2.4G
Bluetooth		BT4.1
FM		Support
GNSS		GPS/Beidou/Glonass
DATA	TDD-LTE	Cat4 TDD-LTE 117/30Mbps
	FDD-LTE	Cat4 FDD-LTE 150/50Mbps
	DC-HSPA+	42/11.2Mbps
	TD-HSPA	2.8/2.3Mbps
	EVDO Rev.A	3.1/1.8Mbps
	EDGE	Class12, 236.8kbps/236.8kbps
	GPRS	Class12, 85.6kbps/85.6kbps
SIM		DSDS (Dual Sim-card Dual Stanby) 3.0/1.8V Support SIM hot plug L/W/G+G with CSFB to W/G L/TDS/G+G with CSFB to G

	L/EVDO/CDMA1x+G Don't support dual CDMA sim-card	
Display	Matrix: HD(720p)B 1280*720@60fps	
	LCM Size: User defined	
	Interface: MIPI DSI 4-lane	
Camera C Front and rearD	Interface: main: MIPI CSI0 2-lanes; front: MIPI CSI1 1-lanes	
	Camera Pixel: Max: FRONT5M/REAR8M	
	Video decode	1080p 30 fps: HEVC/H264/ MP4/DivX/VP8 WVGA 30 fps:H.263
	Video encode	720p 30 fps:H264 WVGA 30 fps:VP8/MP4
Input Device	KeyC Power on/off, Volume+, Volume-D	
	Capacitive TP	
Reset	Support HW reset	
Application interface	Interface	Main function description
	VBAT	Module power input, 3.3V ~ 4.2V, nominal value 3.8V
	SDIO *1	TF CardA Support32GB max
	USB	SupportOTG FORCE_USB_BOOTC Pull-up forced USB boot for emergency downloadD
	UART*2	A set of 4-wire uart, a set of 2-wire uart
	I2C*4	For sensors/TP/others
	SPI*1	Master only
	ADC*2	Support
	Charging function	Built-in 5V/1.44A, support external charging chip
	Motor	Support
	GPIO	17
	VCOIN	Real-time clock backup battery
	RF PIN	Multimode LTE main antenna Multimode LTE diversity antenna The GPS antenna 2.4 G WiFi/BT antenna
	Audio	2-way single-ended MICC ECM&MEMSD ,1 way headphone MIC 1 way speakerphone (with amplifier) 1 way earpiece 1 channel stereo headset

2.2 Block diagram

The following figure lists the main functional parts of the module.

- MSM8909 Baseband
- PM8909 Power management
- Antenna interface
- MIPI interface
- Storage EMCP
- AUDIO interface
- Serial port, SD card interface, SIM card interface, I2C interface, etc.

3.Module Encapsulation

3.1 Pin distribution diagram

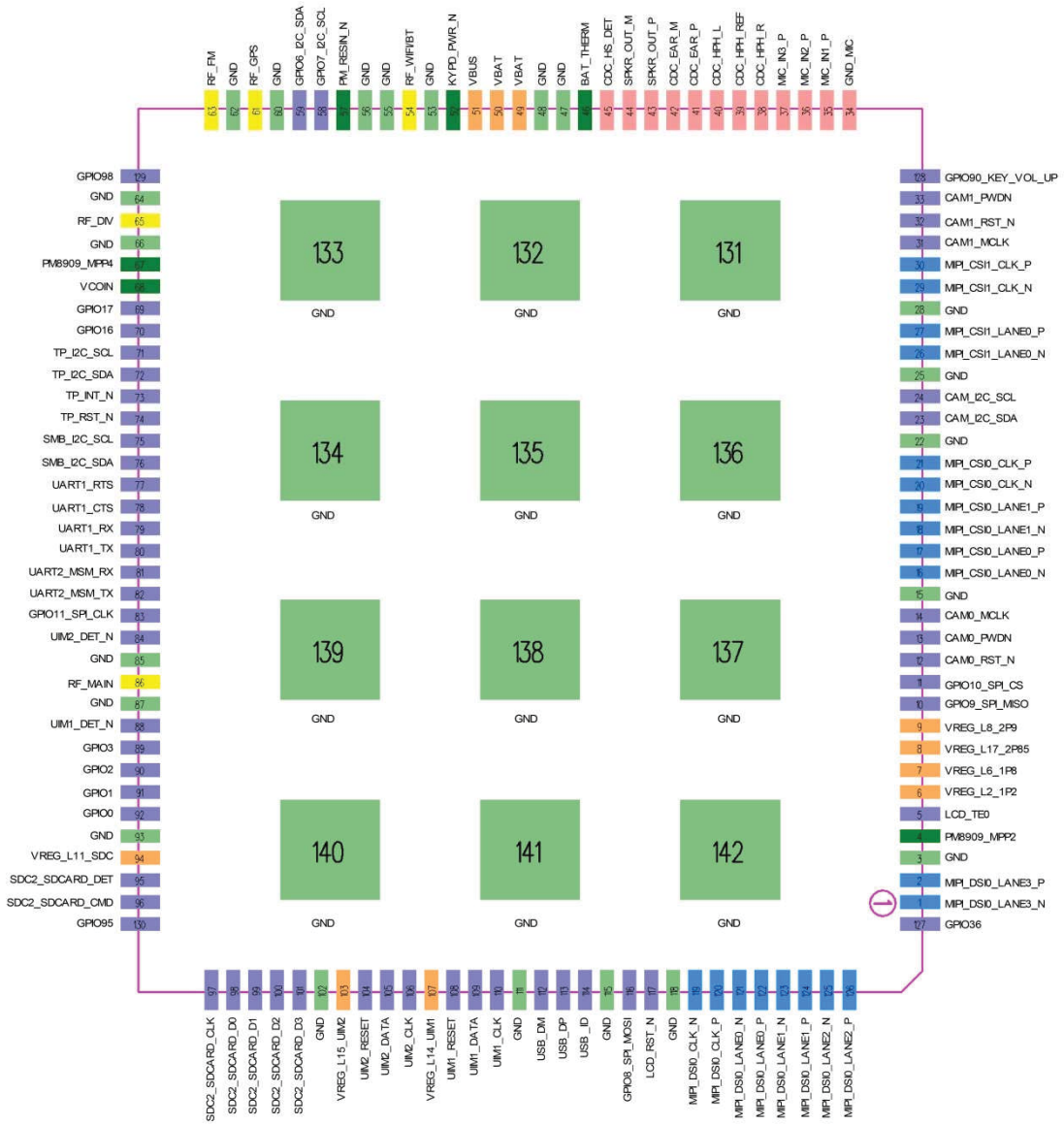


Figure 3.1B module pin diagram (top view)

3.2 Pin definitions

Table 3.1：Pin description

Pin Name	Pin number	I/O	Description	Comment
The power supply				

VBAT	49、50	I	The module provides four VBAT power pin pins. The SLM756 operates from a single supply with a voltage range from 3.3V to 4.2V for VBAT.	Externally, the capacitor and Zener diode need to be increased for surge protection.
VBUS	51	I	Charging input power.	
VCOIN	68	I/O	The external backup battery provides power to the system real-time clock when the system power supply VBAT is not in place. The backup battery is charged when VBAT is in place.	Connect the 3V button battery or large capacitor to the VCOIN pin.
VREG_L2_1P2	6	O	1.2V power output for CAM DVDD power supply	200mA
VREG_L6_1P8	7	O	1.8V power output for LCM, Camera and other low current supplies.	200mA
VREG_L17_2P85	8	O	2.85V power output for Camera power supply.	420mA
VREG_L11_SDC	94	O	TF card power supply pin	600mA
VREG_L8_2P9	9	O	2.9V power output for Camera power supply.	300mA
VREG_L14_UIM1	107	O	UIM1 power supply pin	55mA
VREG_L15_UIM2	103	O	UIM2 power supply pin	55mA
GND	3、15、22、25、28、47、48、53、55、56、60、62、64、66、85、87、93、102、111、115、118		Ground	
Display interface (MIPI)				
MIPI_DSI0_CLK_N	119	I/O	MIPI_LCD clock	
MIPI_DSI0_CLK_P	120	I/O		
MIPI_DSI0_LANE0_N	121	I/O	MIPI_LCD data	
MIPI_DSI0_LANE0_P	122	I/O		
MIPI_DSI0_LANE1_N	123	I/O		
MIPI_DSI0_LANE1_P	124	I/O		
MIPI_DSI0_LANE2_N	125	I/O		
MIPI_DSI0_LANE2_P	126	I/O		
MIPI_DSI0_LANE3_N	1	I/O		
MIPI_DSI0_LANE3_P	2	I/O		
LCD_RST_N	117	O	LCD reset	
LCD_TE0	5	I	LCD frame sync signal	

UART				
UART_TX	80	O	UART1 Data sent	
UART_RX	79	I	UART1 Data reception	
UART_CTS	78	I	UART1 Clear to send	
UART_RTS	77	O	UART1 Request to send	
UART_MSM_TX	82	O	UART2 Data sent	debug
UART_MSM_RX	81	I	UART2 Data reception	debug
UIM Card Interface				
UIM1_DET	88	I	UIM1 detect	
UIM1_RESET	108	O	UIM1 reset	
UIM1_CLK	110	O	UIM1 clock	
UIM1_DATA	109	I/O	UIM1 data	
UIM2_DET	84	I	UIM2 detect	
UIM2_RESET	104	O	UIM2 reset	
UIM2_CLK	106	O	UIM2 clock	
UIM2_DATA	105	I/O	UIM2 data	
Front Camera				
MIPI_CSI1_LANE0_N	26	I/O	Front Camera MIPI data	
MIPI_CSI1_LANE0_P	27	I/O	Front Camera MIPI data	
MIPI_CSI1_CLK_N	29	I/O	Front Camera MIPI clock	
MIPI_CSI1_CLK_P	30	I/O		
CAM1_MCLK	31	I/O	Front Camera main clock	
CAM1_RST_N	32	I/O	Front Camera reset	
CAM1_PWDN	33	I/O	Front Camera dormancy	
Rear Camera				
MIPI_CSI0_LANE0_N	16	I/O	Rear Camera MIP Idata	
MIPI_CSI0_LANE0_P	17	I/O	Rear Camera MIPI data	
MIPI_CSI0_LANE1_N	18	I/O	Rear Camera MIPI data	
MIPI_CSI0_LANE1_P	19	I/O	Rear Camera MIPI data	
MIPI_CSI0_CLK_N	20	I/O	Rear Camera MIPI clock	
MIPI_CSI0_CLK_P	21	I/O	Rear Camera MIPI clock	
CAM0_MCLK	14	I/O	Rear Camera main clock	
CAM0_RST_N	12	I/O	Rear Camera reset	
CAM0_PWDN	13	I/O	Rear Camera dormancy	
Audio Interface				
GND_MIC	34		MIC reference ground	
MIC_IN1_P	35	I	Main MIC	
MIC_IN2_P	36	I	Headphone MIC	
MIC_IN3_P	37	I	Noise MIC	
CDC_HPH_R	38	O	Headphone right channel	
CDC_HPH_L	40	O	Headphone left channel	
CDC_HS_DET	45	I	Headphone plug detection	
CDC_HPH_REF	39	I	Headphone reference ground	
CDC_EAR_P	41	O	Earpiece output positive	
CDC_EAR_M	42	O	Earpiece output negative	
SPKR_DRV_P	43	O	Amplifier (0.85W) output positive	Class_D
SPKR_DRV_M	44	O	Amplifier (0.85W) output	Class_D

			negative	
SD Card Interface				
SDC2_SDCARD_DET	95	I/O	SD card insertion detection	
SDC2_SDCARD_CMD	96	I/O	SD CMD signal	
SDC2_SDCARD_CLK	97	I/O	SD clock signal	
SDC2_SDCARD_D0	98	I/O	SD data signal	
SDC2_SDCARD_D1	99	I/O		
SDC2_SDCARD_D2	100	I/O		
SDC2_SDCARD_D3	101	I/O		
I2C				
CAM_I2C_SDA	23	I/O	I2C signal, dedicated to CAM	Up to the L6
CAM_I2C_SCL	24	I/O	I2C signal, dedicated to CAM	
SENSOR_I2C_SDA	59	I/O	I2C signal, default SENSOR	
SENSOR_I2C_SCL	58	I/O	I2C signal, default SENSOR	
TP_I2C_SDA	72	I/O	I2C signal, default TP	
TP_I2C_SCL	71	I/O	I2C signal, default TP	
TP				
TP_INT_N	73	I	TP interrupt signal	
TP_RST_N	74	O	TP reset signal	
USB				
USB_DM	112	I/O	USB DM	
USB_DP	113	I/O	USB DP	
USB_ID	114	I	USB ID	
Antenna interface				
RF_MAIN	86	I/O	The main antenna	
RF_WIFI/BT	54	I/O	WIFI/BT antenna	
RF_DIV	65	I	Diversity antenna	
RF_GPS	61	I	GPS antenna	
GPIO and default function				
GPIO0	92	I/O	Generic GPIO, without default configuration	
GPIO1	91	I/O	Generic GPIO, without default configuration	
GPIO2	90	I/O	Generic GPIO, without default configuration	
GPIO3	89	I/O	Generic GPIO, without default configuration	
GPIO8_SPI1_MOSI	116	O	SPI interface	
GPIO9_SPI1_MISO	10	I	SPI interface	
GPIO10_SPI1_CS	11	O	SPI interface	
GPIO11_SPI1_CLK	83	O	SPI interface	
GPIO14	76	I/O	Generic GPIO, without default configuration	
GPIO15	75	I/O	Generic GPIO, without default	

			configuration	
GPIO16	70	I/O	Generic GPIO, without default configuration	
GPIO17	69	I/O	Generic GPIO, without default configuration	
GPIO36	127	I/O	Generic GPIO, without default configuration	
GPIO90	128	I/O	Generic GPIO, without default configuration	
GPIO95	130	I/O	Generic GPIO, without default configuration	
GPIO98	129	I/O	Generic GPIO, without default configuration	
Other functional pin				
KYPD_PWR_N	52	I	Powerkey	
PM_RESIN_N	57	I	Pull down to achieve reset	
BAT_THERM	46	I	Battery temperature detection (default battery terminal NTC resistance is 10K)	
PM8909_MPP4	67	I	Analog voltage input for use as an ADC input	
PM8909_MPP2	4	O	Analog voltage output for use as a PWM output	
RF_FM	63	I	FM antenna signal	

Table 3.2B Pin Characteristics

pin#	pin name	GPIO Interrupt	Pad characteristics	Functional description
1	MIPI_DSI0_LANE3_N		AI, AO	MIPI display serial interface 0 lane 3 E negative
2	MIPI_DSI0_LANE3_P		AI, AO	MIPI display serial interface 0 lane 3 E positive
3	GND		GND	GND
4	PM8909_MPP2	MPP2**	AO-Z; DO	Configurable MPP; used for PWM
5	LCD_TE0	GPIO24	B-PD:nppukp	Configurable I/O,CCI_TIMER0, GP_CLK0
6	VREG_L2_1P2		OUPUT	PMU Supply 1.2V
7	VREG_L6_1P8		OUPUT	PMU Supply 1.8V
8	VREG_L17_2P85		OUPUT	PMU Supply 2.85V
9	VREG_L8_2P9		OUPUT	PMU Supply 2.9V
10	GPIO9_SPI_MISO	GPIO9	B-PD:nppukp	Configurable I/O SPI
11	GPIO10_SPI_CS	GPIO10	B-PD:nppukp	Configurable I/O SPI or I2C
12	CAM0_RST_N	GPIO35*	DO;B-PD:nppukp	Rear camera reset; Configurable I/O
13	CAM0_PWDN	GPIO34*	DO;B-PD:nppukp	Rear camera pwdn;Configurable I/O
14	CAM0_MCLK	GPIO26	DO;B-PD:nppukp	Rear camera clock; Configurable I/O
15	GND		GND	GND
16	MIPI_CSI0_LANE0_N		AI, AO	MIPI camera serial interface 0 lane 0 E negative
17	MIPI_CSI0_LANE0_P		AI, AO	MIPI camera serial interface 0 lane 0 E positive

18	MIPI_CSI0_LANE1_N		AI, AO	MIPI camera serial interface 0 lane 1 E negative
19	MIPI_CSI0_LANE1_P		AI, AO	MIPI camera serial interface 0 lane 1 E positive
20	MIPI_CSI0_CLK_N		AI	MIPI camera serial interface 0 CLK E negative
21	MIPI_CSI0_CLK_P		AI	MIPI camera serial interface 0 CLK E positive
22	GND		GND	GND
23	CAM_I2C_SDA	GPIO29	B-PD:nppukp	Camera I2C_SDA,canF t be used for other
24	CAM_I2C_SCL	GPIO30	B-PD:nppukp	Camera I2C_SCL,canF t be used for other
25	GND		GND	GND
26	MIPI_CSI1_LANE0_N		AI, AO	MIPI camera serial interface 1 lane 0E negative
27	MIPI_CSI1_LANE0_P		AI, AO	MIPI camera serial interface 1 lane 0 E positive
28	GND		GND	GND
29	MIPI_CSI1_CLK_N		AI	MIPI camera serial interface 1 clock E negative
30	MIPI_CSI1_CLK_P		AI	MIPI camera serial interface 1 clock E positive
31	CAM1_MCLK	GPIO27	DO;B-PD:nppukp	Camera master clock 1 Configurable I/O
32	CAM1_RST_N	GPIO28*	DO;B-PD:nppukp	Front camera reset Configurable I/O
33	CAM1_PWDN	GPIO33	DI;B-PD:nppukp	Front camera pwdn Configurable I/O
34	GND_MIC		GND	MIC GND
35	MIC_IN1_P		AI	Microphone 1 input, single-ended
36	MIC_IN2_P		AI	Earphone Microphone input, single-ended
37	MIC_IN3_P		AI	Microphone 3 input, single-ended
38	CDC_HPH_R		AO	Earphone right output
39	CDC_HPH_REF		AI	Earphone driver amplifier ground reference
40	CDC_HPH_L		AO	Earphone left output
41	CDC_EAR_P		AO	Earpiece amplifier output, differential plus
42	CDC_EAR_M		AO	Earpiece amplifier output, differential minus
43	SPKR_OUT_P		AO	SpeakerC 0.85w / 4.2VD driver output, plus
44	SPKR_OUT_M		AO	SpeakerC 0.85w / 4.2VD driver output, minus
45	CDC_HS_DET		DI	Headset detection
46	BAT_THERM		DI	Battery therm monitor
47	GND		GND	GND
48	GND		GND	GND
49	VBAT		PI,PO	Battery
50	VBAT		PI,PO	Battery
51	VBUS		PI	USB VBUS Voltage
52	KYPD_PWR_N		DI	Power on key
53	GND		GND	GND
54	RF_WIFI/BT		AI,AO	RF signal

55	GND		GND	GND
56	GND		GND	GND
57	PM_RESIN_N		DI	PMIC reset
58	GPIO7_I2C_SCL	GPIO7	DO;B-PD:nppukp	Configurable I/O I2C or GPIO
59	GPIO6_I2C_SDA	GPIO6	DO;B-PD:nppukp	Configurable I/O I2C or GPIO
60	GND		GND	GND
61	RF_GPS		AI	RF signal-GPS ANT
62	GND		GND	GND
63	RF_FM		AI	RF signal-FM ANT
64	GND		GND	GND
65	RF_DIV		AI	RF signal-DIV ANT
66	GND		GND	GND
67	PM8909_MPP4	MPP4**	AO-Z;DI	Configurable MPP; used for ADC IN
68	VCOIN		PI	VCOIN
69	GPIO17	GPIO17	B-PD:nppukp	Configurable I/O,
70	GPIO16	GPIO16	B-PD:nppukp	Configurable I/O,
71	TP_I2C_SCL	GPIO19	B;B-PD:nppukp	Configurable I/O CTP I2C
72	TP_I2C_SDA	GPIO18	B;B-PD:nppukp	Configurable I/O CTP I2C
73	TP_INT_N	GPIO13*	DI;B-PD:nppukp	Configurable I/O Touchscreen interrupt
74	TP_RST_N	GPIO12*	DI;B-PD:nppukp	Configurable I/O Touchscreen reset
75	SMB_I2C_SCL	GPIO15	B;B-PD:nppukp	Configurable I/O SMB I2C
76	SMB_I2C_SDA	GPIO14	B;B-PD:nppukp	Configurable I/O SMB I2C
77	UART1_RTS	GPIO112*	B;B-PD:nppukp	Configurable I/O UARTor I2C SCL
78	UART1_CTS	GPIO111*	B-PD:nppukp	Configurable I/O UARTor I2C SDA
79	UART1_RX	GPIO21*	B-PD:nppukp	Configurable I/O UART
80	UART1_TX	GPIO20*	B-PD:nppukp	Configurable I/O UART
81	UART2_MSM_RX	GPIO5*	B;B-PD:nppukp	Configurable I/O UART for debug
82	UART2_MSM_TX	GPIO4	BD;B-PD:nppukp	Configurable I/O UART for debug
83	GPIO11_SPI_CLK	GPIO11*	B-PD:nppukp	Configurable I/O SPI or I2C
84	UIM2_DET_N	GPIO52	DI,B-PD:nppukp	Configurable I/O UIM2 removal detection
85	GND		GND	GND
86	RF_MAIN		AI,AO	RF signal-Main ANT
87	GND		GND	GND
88	UIM1_DET_N	GPIO56	DI,B-PD:nppukp	Configurable I/O UIM1 removal detection
89	GPIO3	GPIO3	B-PD:nppukp	Configurable I/O, MI2S_2_D1
90	GPIO2	GPIO2	B-PD:nppukp	Configurable I/O,MI2S_2_D0
91	GPIO1	GPIO1	B-PD:nppukp	Configurable I/O,MI2S_2_SCK
92	GPIO0	GPIO0	B-PD:nppukp	Configurable I/O,MI2S_2_WS

93	GND		GND	GND
94	VREG_L11_SDC		PO	PMIC output 2.95V
95	SDC2_SDCARD_DET	GPIO38*	B-PD:nppukp	Configurable I/O ,SD_DET_N
96	SDC2_SDCARD_CMD		BH-PD:nppukp	Secure digital controller 2 command
97	SDC2_SDCARD_CLK		BH-NP:pdpukp	Secure digital controller 2 clock
98	SDC2_SDCARD_D0		BH-PD:nppukp	Secure digital controller 2 data bit 0
99	SDC2_SDCARD_D1		BH-PD:nppukp	Secure digital controller 2 data bit 1
100	SDC2_SDCARD_D2		BH-PD:nppukp	Secure digital controller 2 data bit 2
101	SDC2_SDCARD_D3		BH-PD:nppukp	Secure digital controller 2 data bit 3
102	GND		GND	GND
103	VREG_L15_UIM2		PO	PMIC supply for UIM2
104	UIM2_RESET		DO,B-PD:nppukp	Configurable I/O UIM2 reset
105	UIM2_DATA		B,B-PD:nppukp	Configurable I/O UIM2 data
106	UIM2_CLK		DO,B-PD:nppukp	Configurable I/O UIM2 clock
107	VREG_L14_UIM1		PO	PMIC supply for UIM1
108	UIM1_RESET		DO,B-PD:nppukp	Configurable I/O UIM1 reset
109	UIM1_DATA		B,B-PD:nppukp	Configurable I/O UIM1 data
110	UIM1_CLK		DO,B-PD:nppukp	Configurable I/O UIM1 clock
111	GND		GND	GND
112	USB_DM		AI, AO	USB data minus
113	USB_DP		AI, AO	USB data plus
114	USB _ID		AI	USB ID
115	GND		GND	GND
116	GPIO8_SPI_MOSI	GPIO8	B-PD:nppukp	Configurable I/O SPI
117	LCD_RST_N	GPIO25*	B-PD:nppukp	Configurable I/O, #DSI_RST# ,MDP_VSYNC_S
118	GND		GND	GND
119	MIPI_DSI0_CLK_N		AO	MIPI display serial interface 0 clock – negative
120	MIPI_DSI0_CLK_P		AO	MIPI display serial interface 0 clock –positive
121	MIPI_DSI0_LANE0_N		AI, AO	MIPI display serial interface 0 lane 0 – negative
122	MIPI_DSI0_LANE0_P		AI, AO	MIPI display serial interface 0 lane 0 –positive
123	MIPI_DSI0_LANE1_N		AI, AO	MIPI display serial interface 0 lane 1 – negative
124	MIPI_DSI0_LANE1_P		AI, AO	MIPI display serial interface 0 lane 1 –positive
125	MIPI_DSI0_LANE2_N		AI, AO	MIPI display serial interface 0 lane 2 –negative
126	MIPI_DSI0_LANE2_P		AI, AO	MIPI display serial interface 0 lane 2 –positive
127	GPIO36	GPIO36*	B-PD:nppukp	Configurable I/O
128	GPIO90_KEY_VOL_UP	GPIO90*	DI;B-PD:nppukp	Configurable I/O Keypad sense bit 0
129	GPIO98	GPIO98*	B-PD:nppukp	Configurable I/O

130	GPIO95	GPIO95*	B-PD:nppukp	Configurable I/O

*：Wake-up system interrupt pin

**：Power chip（PM8909）pin

B：Bidirectionaldigital with CMOS input

H：High-voltage tolerant

NP：pdpukp=defaultno-pull with programmable options following the colon (:)

PD：nppukp=defaultpulldownwith programmable options following the colon (:)

PU：nppdkp=defaultpullupwith programmable options following the colon (:)

KP：nppdpu=defaultkeeperwith programmable options following the colon (:)

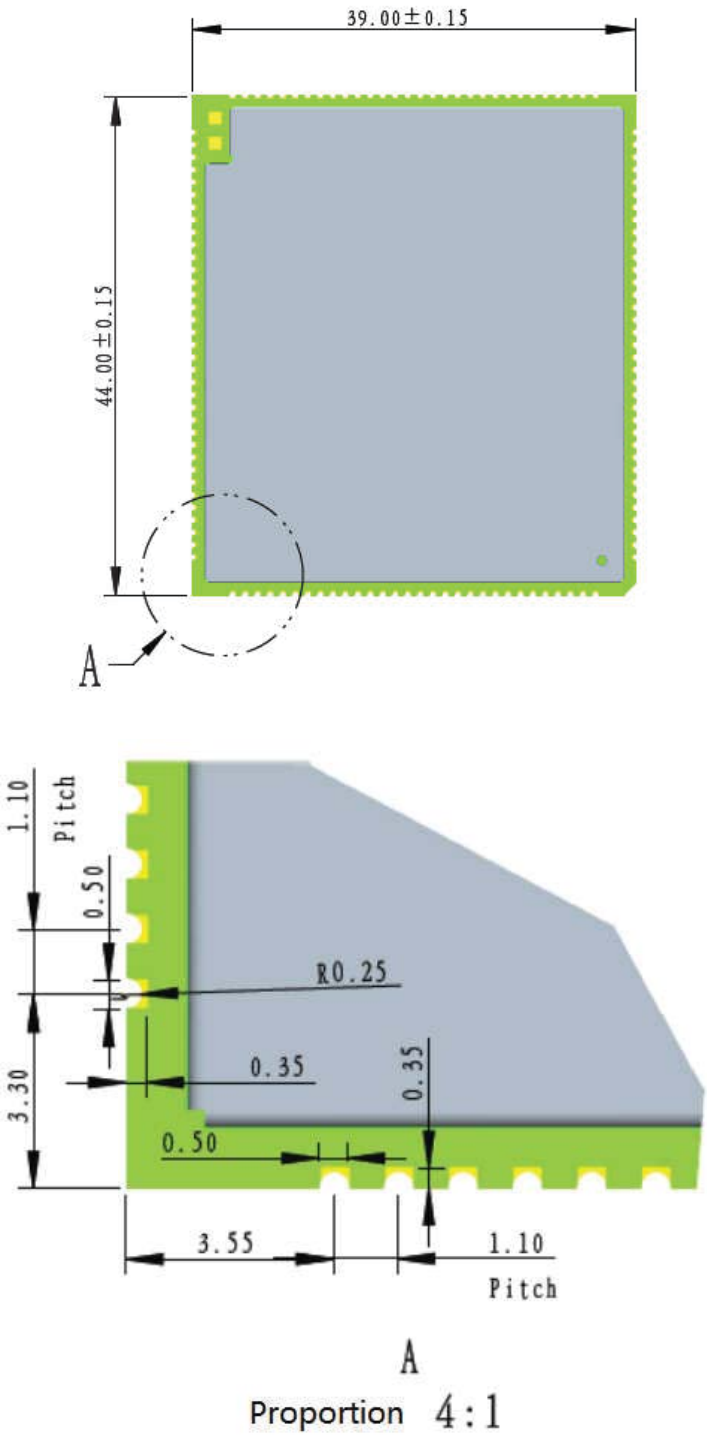
Table 3.3B Multiplexing function

GPIO	Module pin	BLSP Multiplexing function（default is blue）			Outside BLSP Other functions
		SPI	UART	I2C	
GPIO0	92	MOSI			I2S/GPIO
GPIO1	91	MISO			I2S/GPIO
GPIO2	90	CS_N			I2S/GPIO
GPIO3	89	CLK			I2S/GPIO
GPIO4	82	MOSI	TX		GPIO
GPIO5	81	MISO	RX		GPIO
GPIO6	59	CS_N	CTS	SDA	GPIO
GPIO7	58	CLK	RTS	SCL	GPIO
GPIO8	116	MOSI			GPIO
GPIO9	10	MISO			GPIO
GPIO10	11	CS_N		SDA	GPIO
GPIO11	83	CLK		SCL	GPIO
GPIO12	74	MOSI			GPIO
GPIO13	73	MISO			GPIO
GPIO14	76	CS_N		SDA	GPIO
GPIO15	75	CLK		SCL	GPIO
GPIO16	70	MOSI			GPIO
GPIO17	69	MISO			GPIO
GPIO18	72	CS_N		SDA	GPIO
GPIO19	71	CLK		SCL	GPIO
GPIO20	80	MOSI	TX		GPIO
GPIO21	79	MISO	RX		GPIO

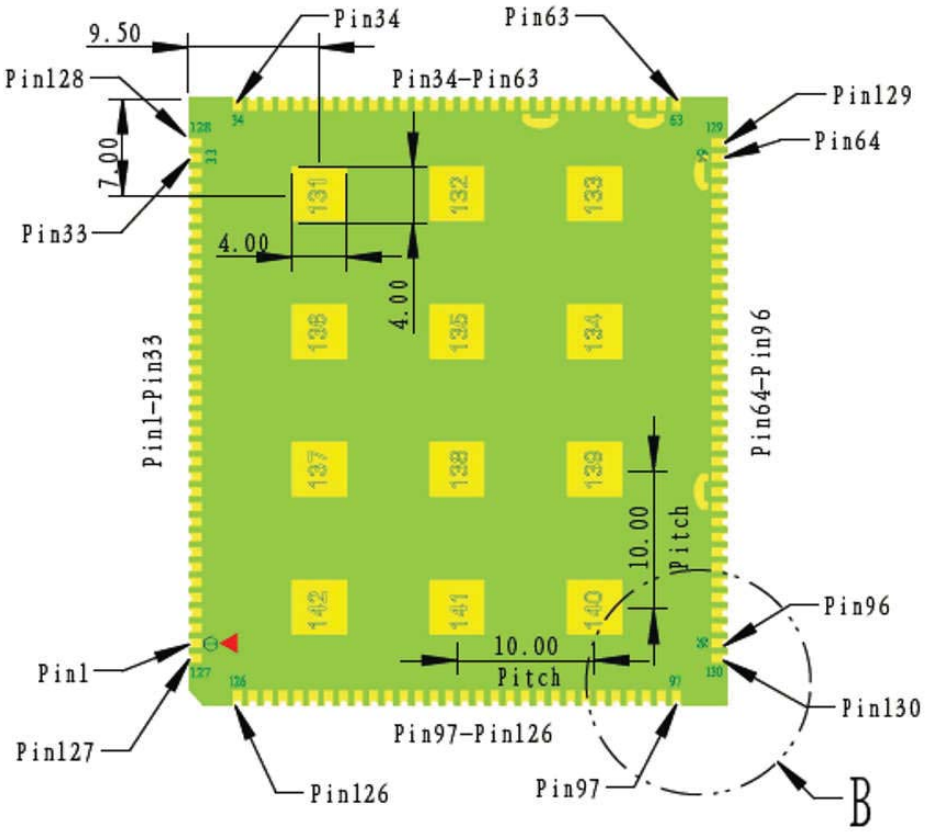
GPIO111	78	CS_N	CTS	SDA	GPIO
GPIO112	77	CLK	RTS	SCL	GPIO

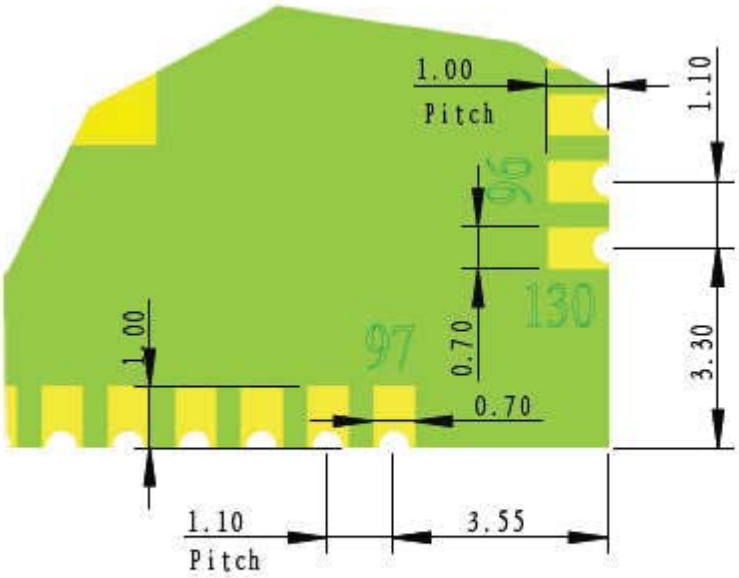
3.3 Mechanical Dimensions

TOP:



BOTTOM:





B

Proportion 4:1

SideB

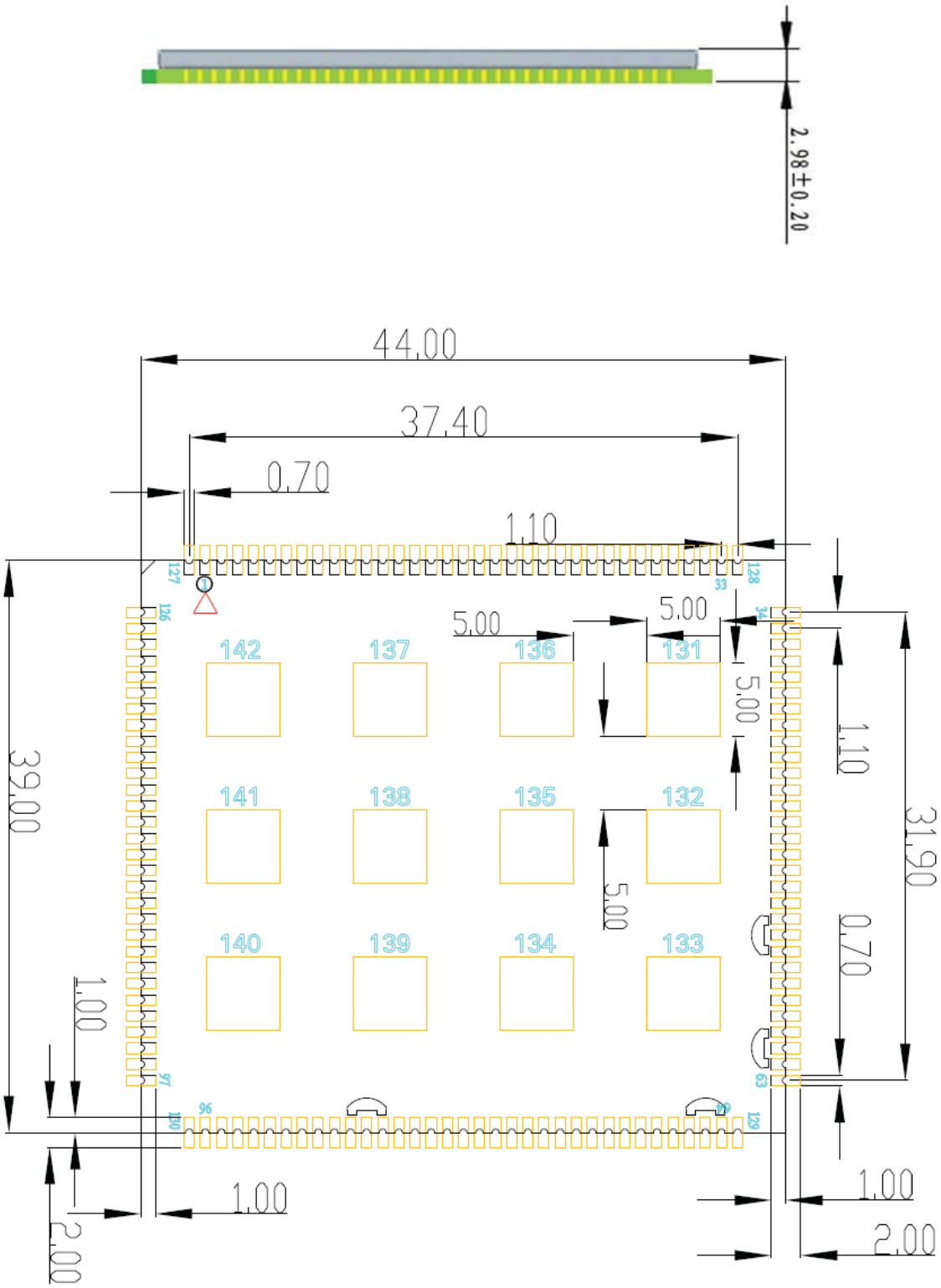


Figure 3.3B Recommended PCB package size (unit: mm)

4.Interface Application

4.1 Power Supply

In the case of a battery device, the voltage input range of the module VBAT is 3.4V to 4.2V, and the recommended voltage is 3.8V. In the GSM band, when the module is transmitting at maximum power, the peak current can reach up to 3A, resulting in a large voltage drop on VBAT.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to use a suitable TVS tube and a 5.6V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.7V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

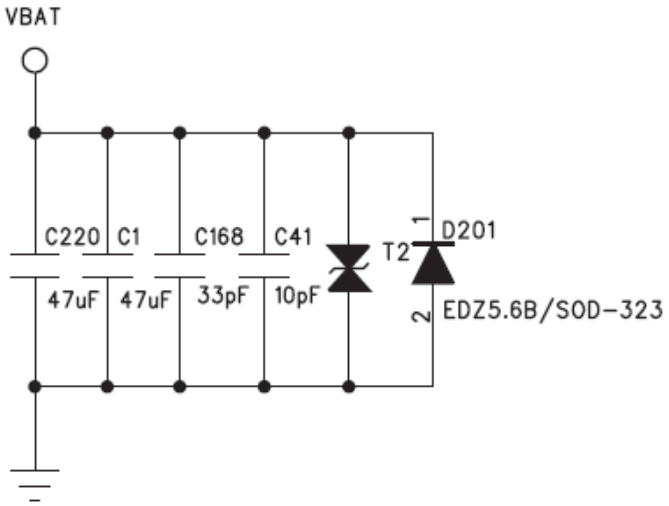


Figure 4.1B VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 5V-12V, and the recommended circuit that can be powered by DC-DC is shown below.

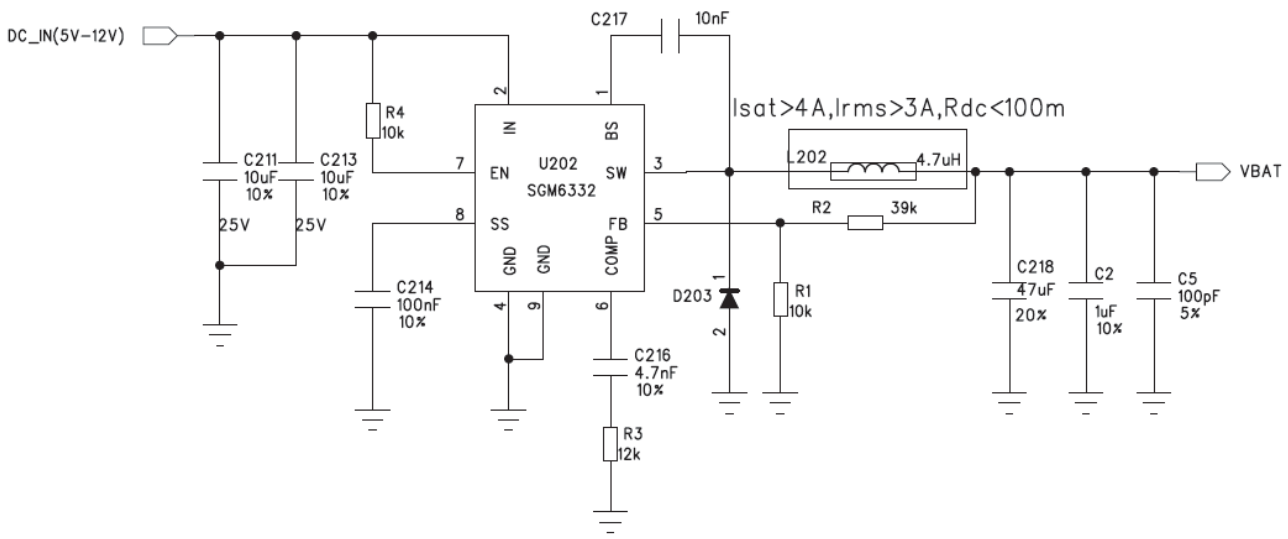


Figure 4.2B DC-DC power supply circuit

Note：

If the user does not use battery power, please note that a 10K resistor is connected to the 134 pin (BAT_THERM) of the module and pulled down to GND to prevent the software from judging the abnormal battery temperature after the module is turned on, resulting in shutdown. The connection diagram is as follows:

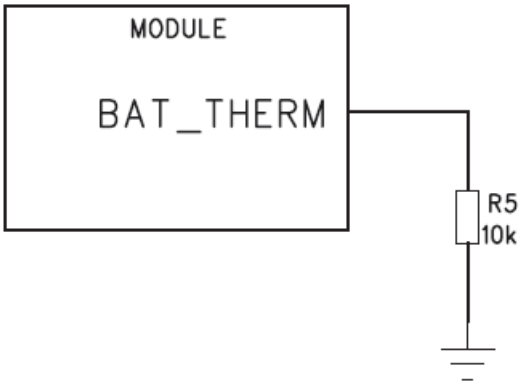


Figure 4.3B Connection diagram when not powered by battery

4.1.1 Power Pin

The VBAT pin (49, 50) is used for power supply input. In the user's design, please pay special attention to the design of the power supply part to ensure that the VBAT drop should not be lower than 3.4V even when the module consumes 2A. If the voltage drops below 3.4V, the module may shut down. The PCB layout from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

Figure 4.4：VBAT lowest voltage drop

4.2. Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In extreme cases, such operations can cause permanent damage to the module.

4.2.1 Module Boot

The user can power up the module by pulling the PWRKEY pin (52) low. Pull down for at least 5 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows:

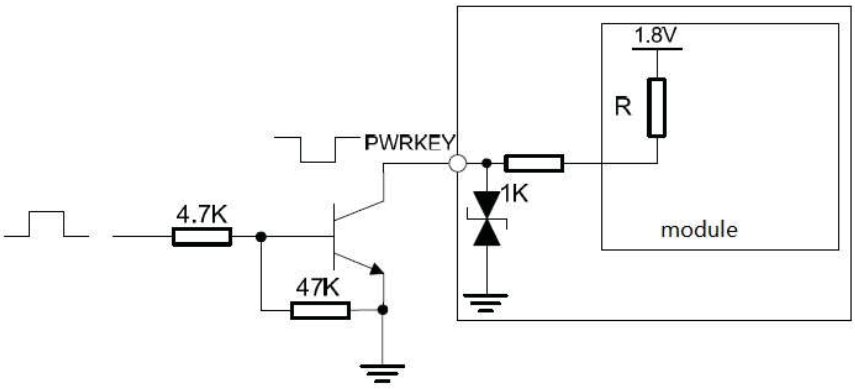


Figure 4.5：Using an external signal to drive the module to boot

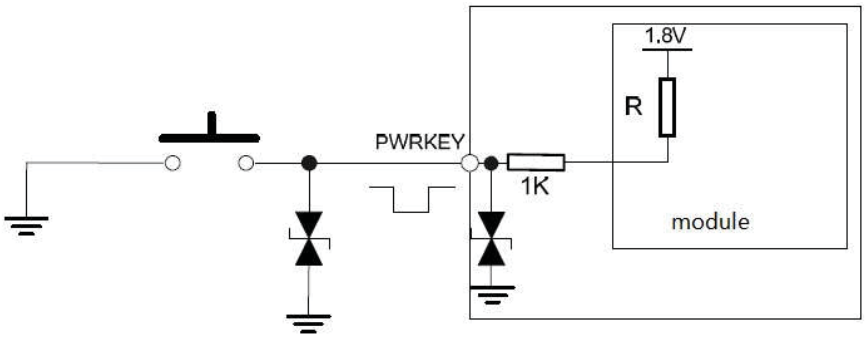


Figure 4.6：Use the PWRKEY button circuit to boot

The following figure is the boot timing description：

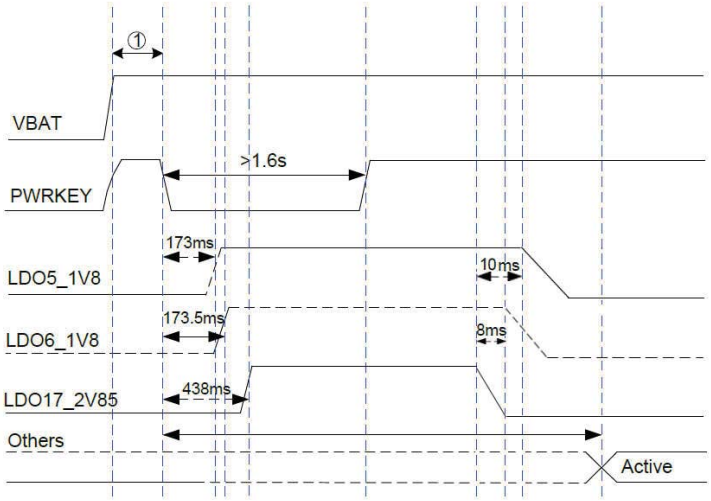


Figure 4.7： Using PWRKEY boot timing diagram

4.2.2 Module Shutdown

Users can use the PWRKEY pin to shut down.

4.2.2.1 PWRKEY Shutdown

The user can turn off the PWRKEY signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the boot circuit. After the module detects the shutdown action, a prompt window pops up on the screen to confirm whether to perform the shutdown action.

The user can achieve a forced shutdown by pulling PWRKEY down for a long time, pulling down for at least 15 seconds

4.2.3 Module Reset

The SLM756 module supports a reset function that allows the user to quickly restart the module by pulling the module's PM_RESIN_N1 (PIN57) pin low. The RESET signal is used as the volume-key by default in Android. If you need to use the RESET signal, you need to modify the software. The recommended circuit is as follows:

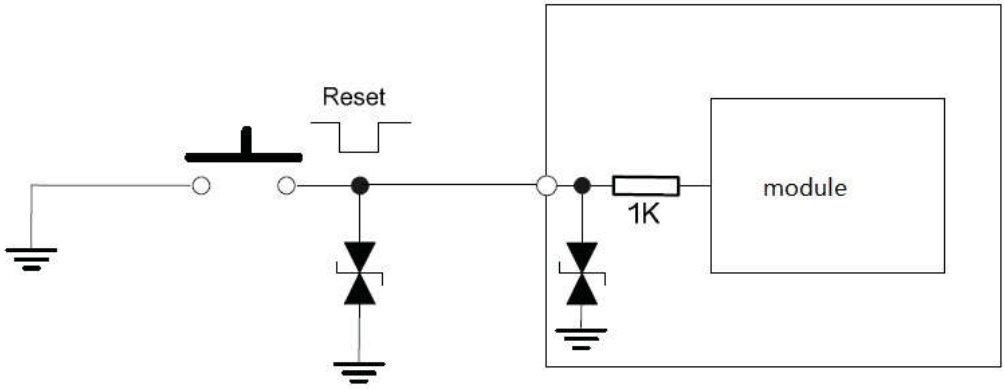


Figure 4.8： Reset using the key circuit

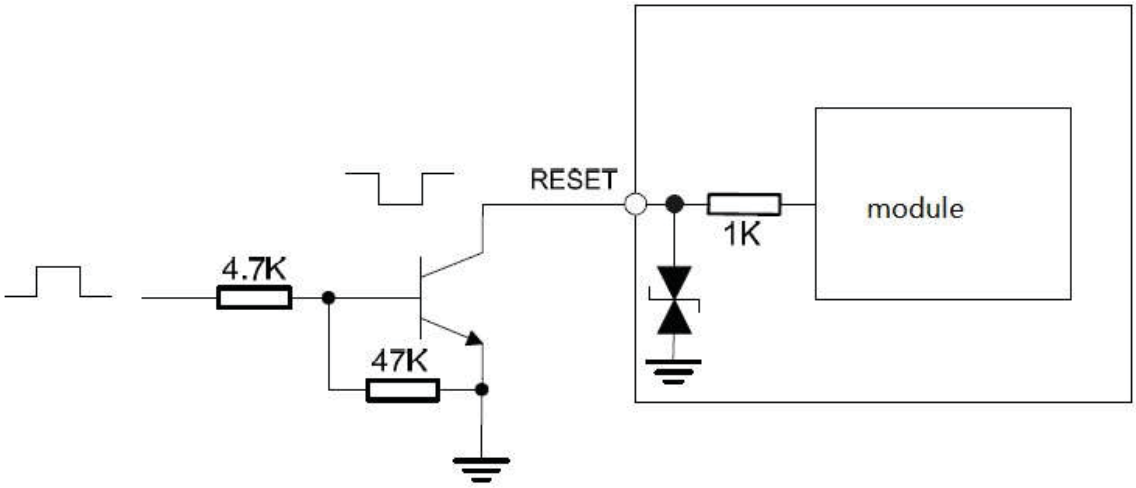


Figure 4.9：Reset Module Using External Signa

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or 3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET can refer to the following table:

Table 4.1: RESET Hardware Parameters

Pin	Description	Minimum	Typical	Maximum	Unit
RESET	Input high level	1	-	-	V
	Input low level	-	-	0.65	V
	Pull down effective time	500		-	ms

4.3 VCOIN Power

When VBAT is disconnected, the user needs to save the real-time clock. The VCOIN pin cannot be suspended. It should be connected to a large capacitor or battery. When external capacitor is connected, the recommended value is 100uF, and the real-time clock can be kept for 1 minute. The reference design circuit is used when the RTC power supply uses an external large capacitor or battery to power the RTC inside the module:

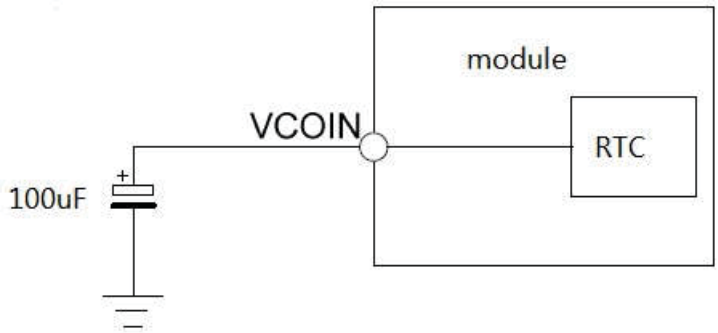


Figure 4.10: External Capacitor Powering the RTC

Non-rechargeable battery powered:

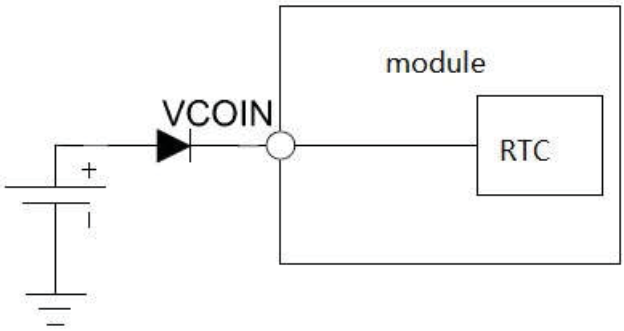


Figure 4.11: Non-rechargeable battery to power the RTC

Rechargeable battery powered:

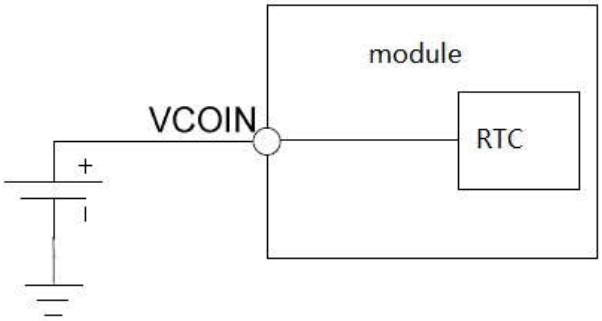


Figure 4.12: Rechargeable Battery Powers RTC

This VCOIN power supply is typically 3.0V and consumes approximately 8uA when VBAT is disconnected.

4.4 Power Output

The SLM756 has multiple power outputs. For LCD, Camera, touch panel, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively

remove high frequency interference.

Table 4.2: Power Description

Signal	Programmable Range (V)	Default Voltage(V)	Drive Current(mA)
VREG_L2_1P2		1.8	200
VREG_L6_1P8	-	1.8	200
VREG_L17_2P85	-	2.85	420
VREG_L11_SDC	1.75~3.337	2.95	600
VREG_L8_2P9	-	2.9	300
VREG_L14_UIM1	1.75~3.337	1.8/3.3	55
VREG_L15_UIM2	1.75~3.337	1.8/3.3	55

4.5 Serial Port

The SLM756 provides two serial ports for communication. UART1 with hardware flow control, UART2 default for debugging.

Table 4.3: UART Pin Description

Name	Pin	Direction	Function
UART_TX	80	O	UART1 Data Transmission
UART_RX	79	I	UART1 Data Reception
UART_CTS	78	I	UART1Clear To Send
UART_RTS	77	O	UART1Request To Send
UART_MSM_TX	82	O	UART2 Data Transmission
UART_MSM_RX	81	I	UART2 DataReception

Please refer to the following connection method:

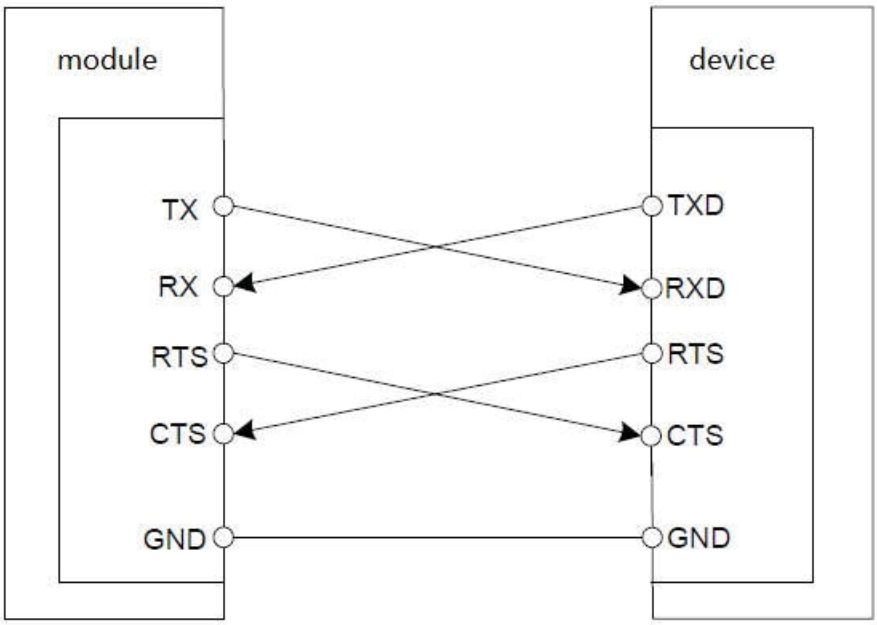


Figure 4.13: Serial Port Connection Diagram

When the serial level used by the user does not match the module, in addition to adding the level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to this two circuits.

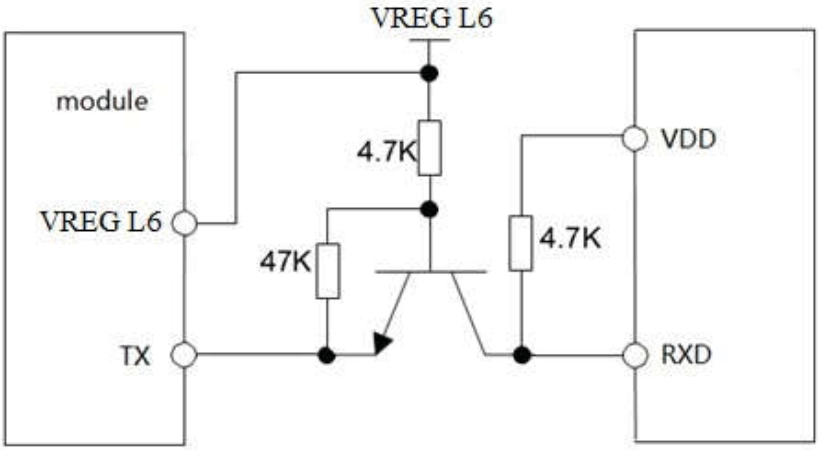


Figure 4.14: TX Connection Diagram

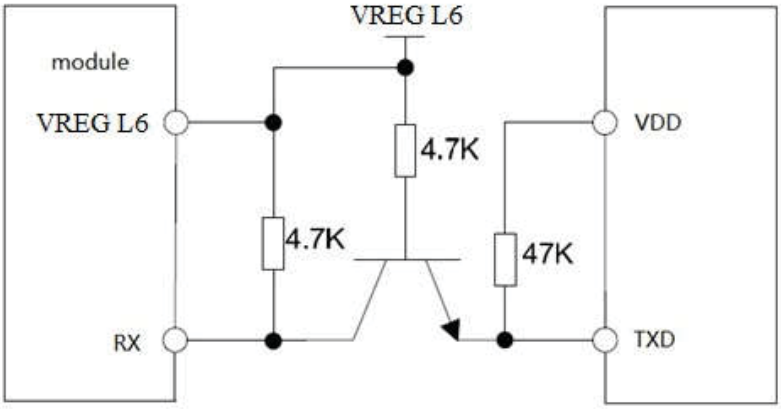


Figure 4.15: RX Connection Diagram

Note: When using Levels 14 and 15 for level isolation, you need to pay attention to the output timing of VREG_L6_1P8. Only after VREG_L6_1P8 is output normally, the serial port can communicate normally. VREG_L6_1P8 will enter low power mode when sleeping. If the serial port needs to be in sleep mode. When communicating, please use the commonly used 1.8V as the pull-up power supply.

Table 4.4: Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Input low level	-	0.45	V
Input high level	1.35	-	V

Note: 1. The serial port of the module is a CMOS interface, and the RS232 signal cannot be directly connected. If necessary, please use the RS232 conversion chip.

2. If the 1.8V output of the module cannot meet the high level range of the user

terminal, please add a level shifting circuit.

4.6 MIPI Interface

The SLM756 supports the Moble Industry Processor Interface (MIPI) interface for Camera andLCM. The module supports up to HD (720P) display, of which MIPI interface Main Camera supports up to 8MP and Front Camera supports 5MP.
MIPI is a high-speed signal line. In the Layout stage, please strictly follow the impedance and length requirements to control the length of the differential pair within the group and the group length. The total length should be as short as possible.

4.6.1 LCD Interface

The SLM756 module supports the LCD display of the MIPI interface with an identification signal for the compatible screen. The resolution of the screen can be up to 1280*720. The signal interface is shown in the following table. In the Layout, the MIPI signal line should strictly control the differential 100 ohm impedance and the equal length between the signal line group and the group.
The module's MIPI interface is a 1.2V power domain. When the user needs a compatible screen design, the module's GPIO or ADC pin can be used. At the same time, the module can provide 2.8V power to the LCD. The LCD interface is as follows:

Table 4.5: Interface Definitions

Name	Pin	Input/Output	Description
LCD_RST	117	O	LCM Reset Pin
MIPI_DSI0_CLK_N	119	O	MIPI Clock Line
MIPI_DSI0_CLK_P	120	O	
MIPI_DSI0_LANE0_N	121	I/O	MIPI Data Line
MIPI_DSI0_LANE0_P	122	I/O	
MIPI_DSI0_LANE1_N	123	I/O	
MIPI_DSI0_LANE1_P	124	I/O	
MIPI_DSI0_LANE2_N	125	I/O	

MIPI_DSI0_LANE2_P	126	I/O	
MIPI_DSI0_LANE3_N	1	I/O	
MIPI_DSI0_LANE3_P	2	I/O	
PM8909_MPP2	4	O	Backlight PWM ontrol signal
LCD_TE	5	I/O	Frame synchronization signal
LDO6_1P8	7	O	1.8V power supply
LDO17_2P85	8	O	2.85V power supply

The LCD_ID of the module can use GPIO (only recognize high and low level) or ADC (PM8909_MPP4). Please confirm the internal circuit of LCM. If the internal divider of LCM uses resistor divider, please note that the voltage domain is 1.8V.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor on the side close to the LCM.

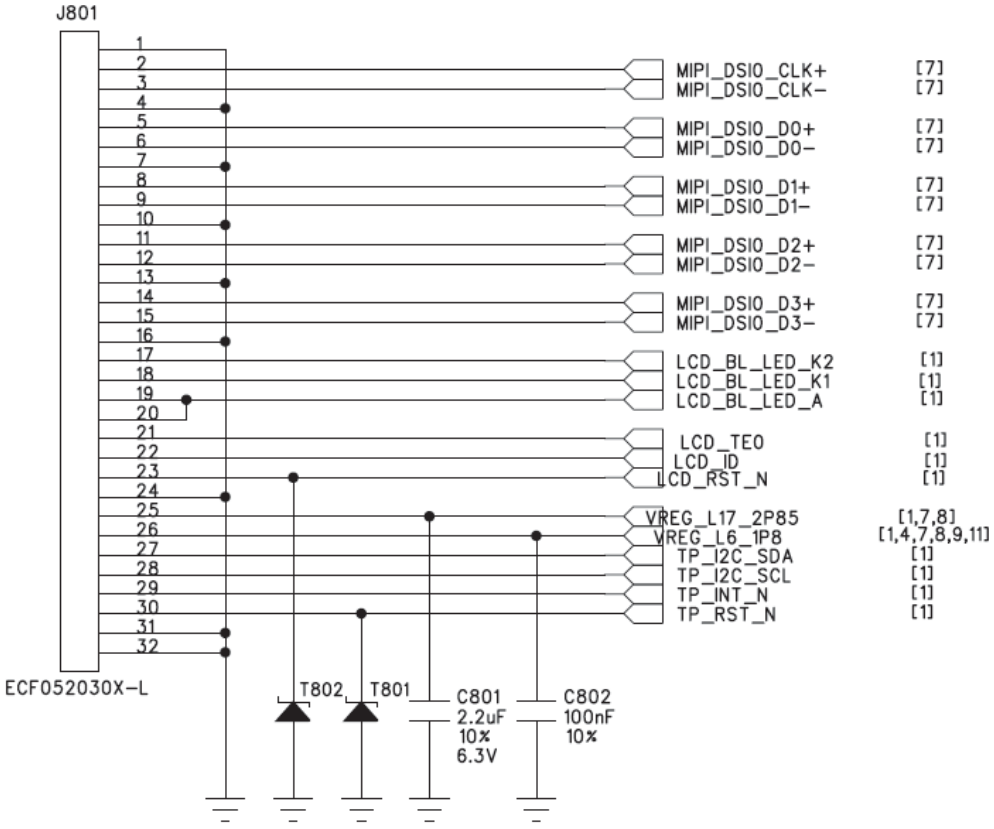


Figure 4.16: Main LCD Interface Circuit

LCD needs a backlight circuit. The backlight driver circuit can refer to Figure 4.17. Adjusting the backlight brightness can be realized by the module's PM8909_MPP2 (112PIN). The modulation mode is PWM mode.

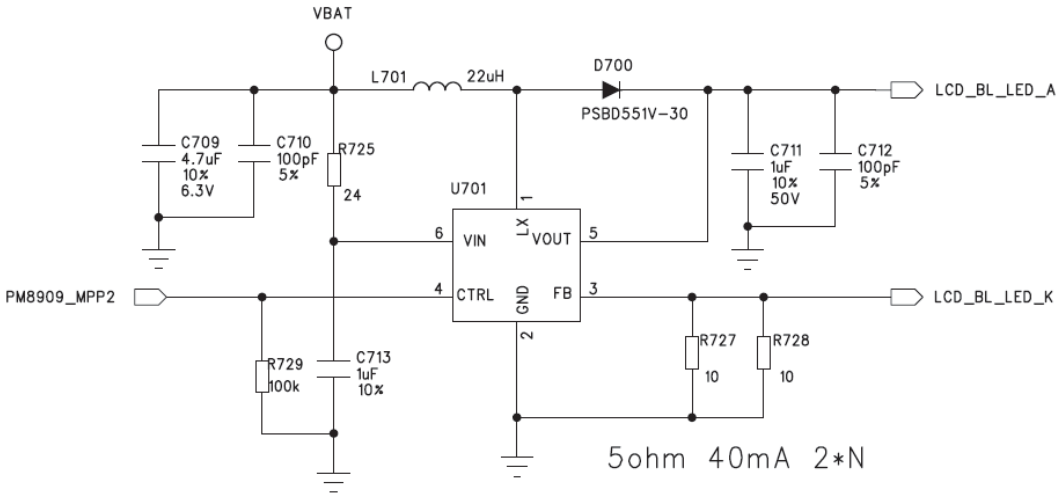


Figure 4.17: Backlight Drive Circuit

Note: 1. The backlight circuit should select the chip according to the backlight circuit of LCD. Users should carefully read the LCD document and select the correct driver chip. The reference circuit provided in this document is a series-type PWM dimming backlight driver circuit; if a series-type one-line dimming backlight driver circuit (such as KTD2801) is used due to design requirements, GPIO is required for control.

4.6.2 MIFI camera Interface

The SLM756 module supports the MIPI interface Camera and provides a dedicated camera power supply. The main camera is a CSI0 interface that supports two sets of data lines and can support 8M pixels. The front camera is a CSI1 interface that supports a set of data lines and can support 5M pixels. The module provides the power required by the Camera, including AVDD-2.85V, IOVDD-1.8V, DVDD-1.2V and AFVDD-2.8V (powering the focus motor).

Table 4.6: MIPI Camera Interface Definition

Main camera interface			
Name	Pin	Input/Output	Description
MIPI_CSI0_LANE0_N	16	I/O	Rear Camera MIPI data signal
MIPI_CSI0_LANE0_P	17	I/O	
MIPI_CSI0_LANE1_N	18	I/O	
MIPI_CSI0_LANE1_P	19	I/O	
MIPI_CSI0_CLK_N	20	I/O	Rear Camera MIPIclock signal
MIPI_CSI0_CLK_P	21	I/O	Rear Camera MIPIclock signal
CAM0_MCLK	14	I/O	Rear Camera main clock
CAM0_RST_N	12	I/O	Rear Camera reset signal
CAM0_PWDN	13	I/O	Rear Camera sleep signal
CAM_I2C_SDA	23	I/O	I2Csignal,CAMdedicated
CAM_I2C_SCL	24	I/O	I2Csignal,CAMdedicated
VREG_L6_1P8	7	O	1.8V IOVDD
VREG_L17_2P85	8	O	2.8V AVDD
VREG_L8_2P9	9	O	2.9V AFVDDC powering the focus motorD
VREG_L2_1P2	6	O	1.2V DVDD

Front camera interface			
Name	Pin	Input/Output	Description
MIPI_CSI1_LANE0_N	26	I/O	Front Camera MIPIdata signal
MIPI_CSI1_LANE0_P	27	I/O	
MIPI_CSI1_CLK_N	29	I/O	Front Camera MIPIclock signal
MIPI_CSI1_CLK_P	30	I/O	Front Camera MIPIclock signal
CAM1_MCLK	31	I/O	Front Camera main clock
CAM1_RST_N	32	I/O	Front Camera reset signal
CAM1_PWDN	33	I/O	Front Camera sleep signal
CAM_I2C_SDA	23	I/O	I2Csignal,CAMdedicated
CAM_I2C_SCL	24	I/O	I2Csignal,CAMdedicated
VREG_L6_1P8	7	O	1.8V IOVDD
VREG_L17_2P85	8	O	2.8V AVDD
VREG_L8_2P9	9	O	2.9V AFVDDC powering the focus motorD
VREG_L2_1P2	6	O	1.2V DVDD

If the user designs to use the CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the driver chip of CAMERA, and the correct connection is as follows:

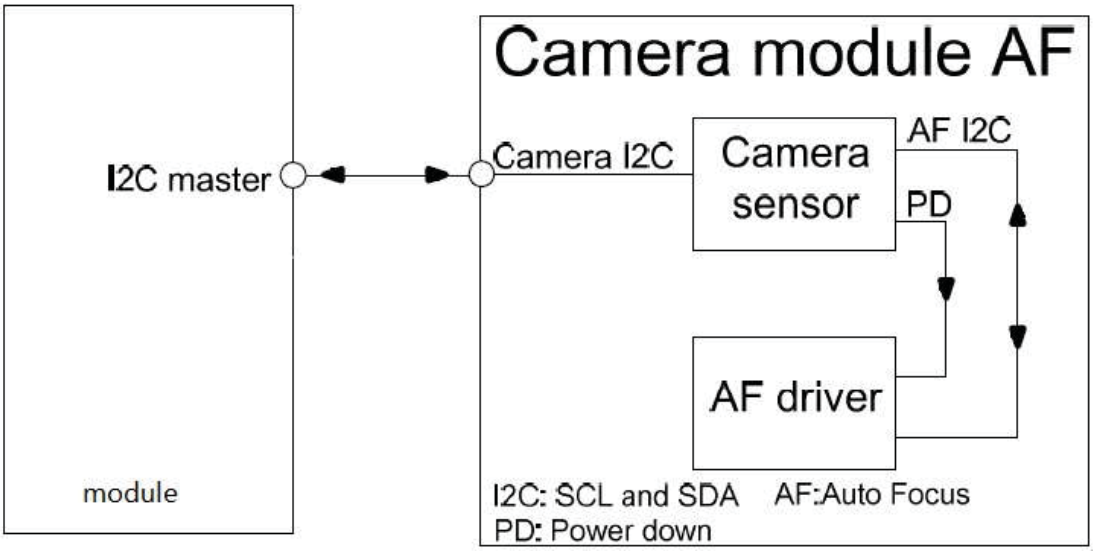


Figure 4.18: Correct CAMERA connection diagram

The MIPI interface has a high rate. The user should control the impedance by 100 ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.

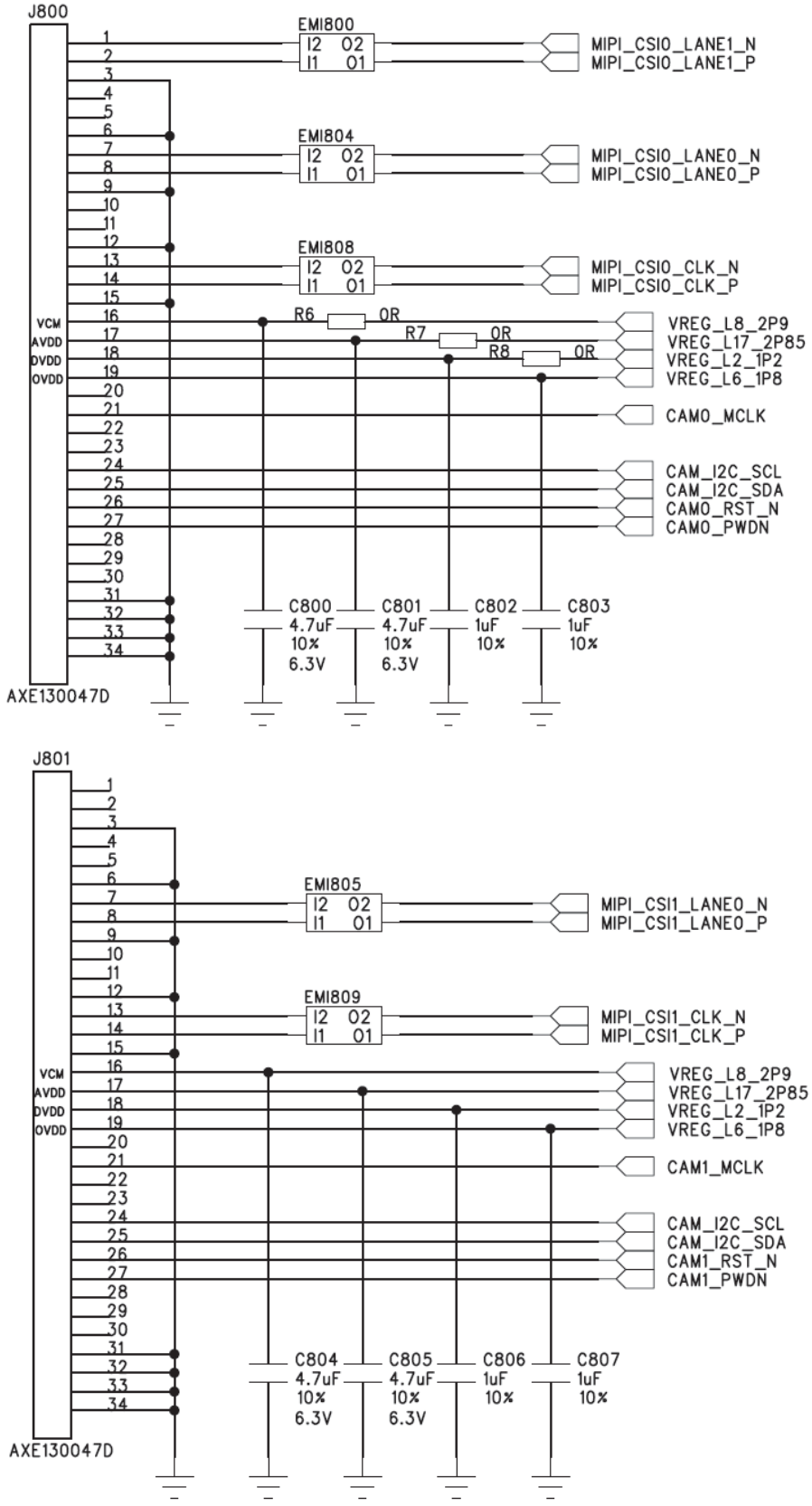


Figure 4.19: MIPI Camera Reference Circuit

When designing the camera function, you need to pay attention to the position of the connector. There will be a small person in the specification of the camera to indicate the imaging direction. You need to ensure that the villain stands on the long side of the LCD. As shown in the two figures below.

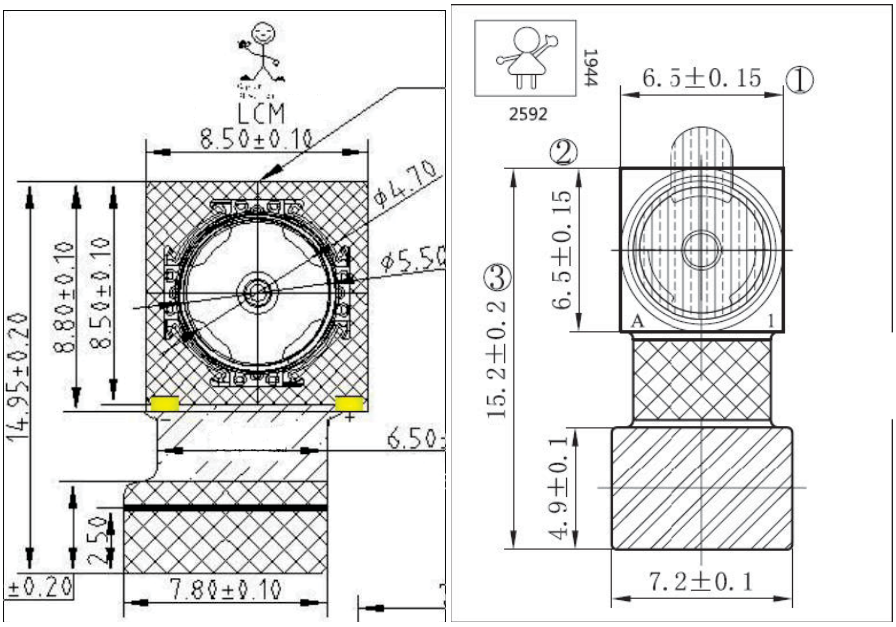


Figure 4.20: Camera imaging diagram

4.7 Resistive Touch Interface

The module does not provide a resistive touch screen interface. If the user needs to use a resistive touch, an external dedicated chip is required. The module can provide an I2C interface.The reference circuit is as follows:

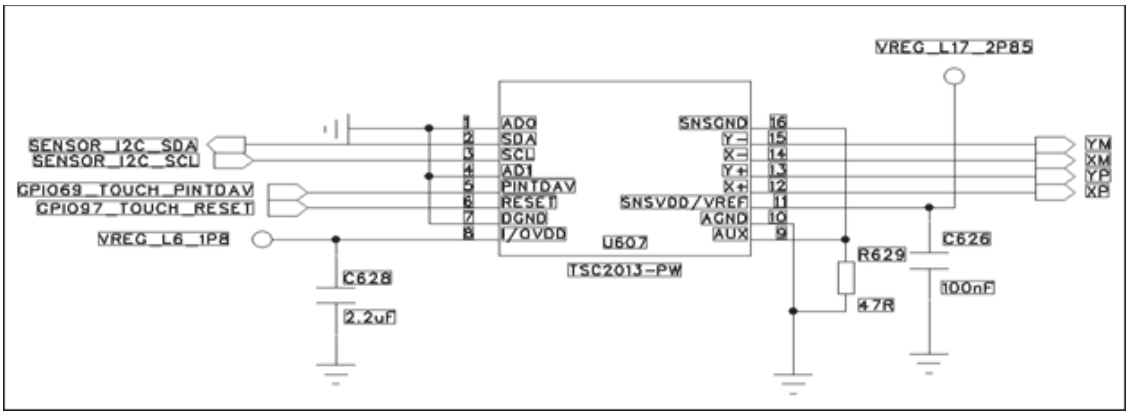


Figure 4.21: RTP Reference Circuit

4.8 CapacitiveTouch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touches while providing the required power and interrupt pins. The default interface pins for capacitive touch software are defined as follows:

Table 4.7: Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO10_TP_I2C3_SDA	82	I/O	The capacitive touch I2C interface needs to be pulled up toVREG_L5_1P8
GPIO11_TP_I2C3_SCL	81	I/O	
GPIO65_TP_INT_N	79	I	Interrupt

GPIO64_TP_RST_N	80	O	Reset
VREG_L17_2P85	112	O	2.8V Power

Note: The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.9 Audio Interface

The module provides three analog audio inputs, MIC_IN1_P/M for the main microphone, MIC_IN2_P for the microphone, and MIC_IN3_P for the noise reduction microphone. The module also provides three analog audio outputs (HPH_L/R, REC_P/N, SPK_P/N). The audio pin is defined as follows:

Table 4.8: Audio Pin Foot Definitions

Name	Pin	Input/Output	Description
MIC_IN1_P	35	I	Main MIC positive
MIC_IN2_P	36	I	Headphone MIC positive
GND_MIC	34	I	Headphone MIC, noise reduction MIC negative
MIC_IN3_P	37	I	Noise reduction MIC positive
CDC_HPH_R	38	O	Headphone right channel
CDC_HPH_L	40	O	Headphone left channel
CDC_HS_DET	45	I	Headphone plug detection
CDC_HPH_REF	39	I	Headphone reference ground
CDC_EAR_M	42	O	Earpiece output negative
CDC_EAR_P	41	O	Earpiece output positive
SPKR_DRV_M	44	O	Amplifier (0.85W) output negative
SPKR_DRV_P	43	O	Amplifier (0.85W) output positive

Users are advised to use the following circuit according to the actual application to get better sound effects.

4.9.1 Receiver Interface Circuit

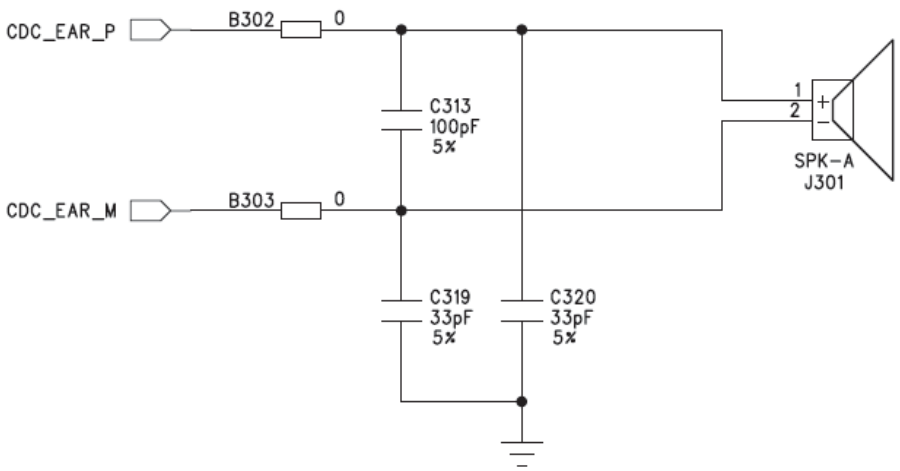


Figure 4.21: Receiver Interface Circuit

4.9.2 Microphone receiving Circuit

Below is the MEMS microphone interface circuit, which has more BIAS power supply than the electret MIC.

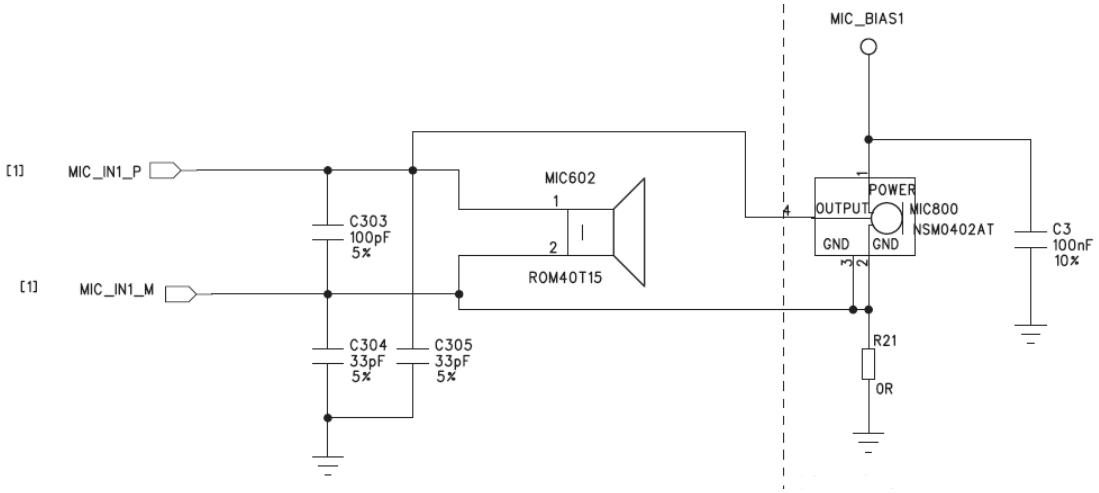


Figure 4.22: Microphone Differential Interface Circuit

4.9.3 Headphone Interface Circuit

The module integrates a stereo headphone jack. Users are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as an interrupt. In software, this pin is the earphone interrupt by default. The user can use this pin to detect the plugging and unplugging of the earphone.

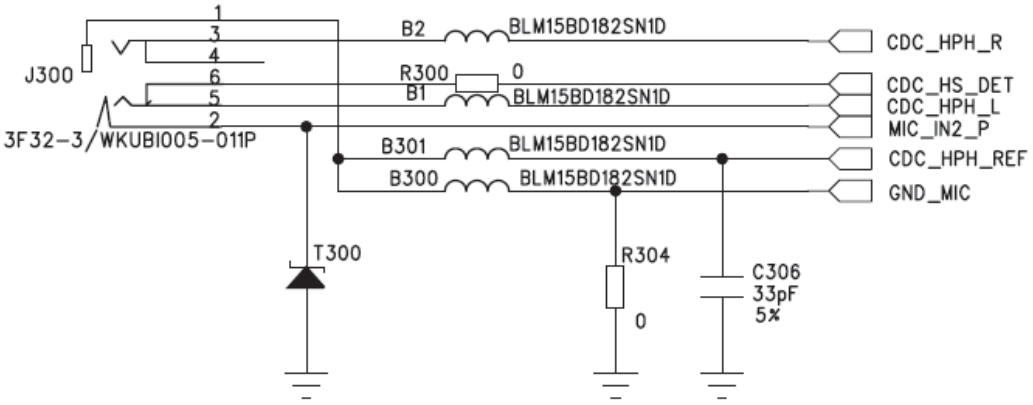


Figure 4.23: Headphone Interface Circuit

note:

1. The earphone holder in Figure 4.23 is normally closed. If the user is using the normally open mode earphone holder, please modify the detection circuit according to the actual pin and modify the software accordingly.
2. We recommend that the headphone detection pin HS_DET and HPH_L form a detection circuit (the connection method in the above figure), because the HPH_L has a pull-down resistor inside the chip, which can ensure that HS_DET is low when connected with HPH_L, if the user will HS_DET and HPH_R Connect, please reserve the position of 1K pull-down resistor on HPH_R.

3 The standard of the headphone interface is the European standard OMPT. If you need to design the American standard CTIA interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headset standards, you need an external dedicated chip, such as the TI-TS3A226AE.

4.9.4 Speaker Interface Circuit

The module integrates a Class-D audio amplifier with an output power of 0.85W and an output signal of SPKR_OUT_P / SPKR_OUT_M

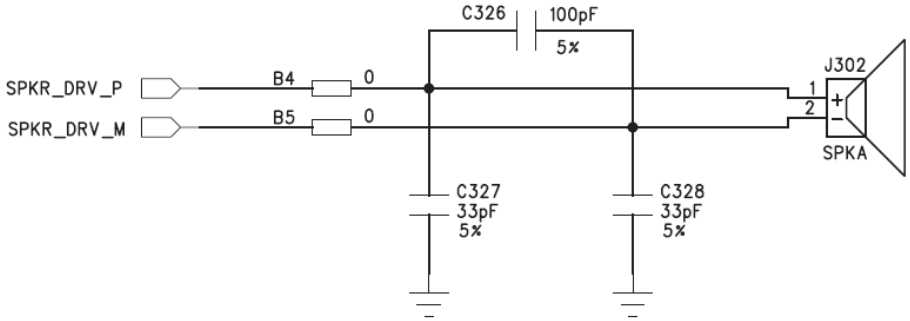


Figure 4.24: Recommended Circuit with Internal Audio Power Amplifier

It is also possible to add an audio amplifier externally, using CDC_HPH_R as a single-ended input signal, and the reference circuit is shown below.

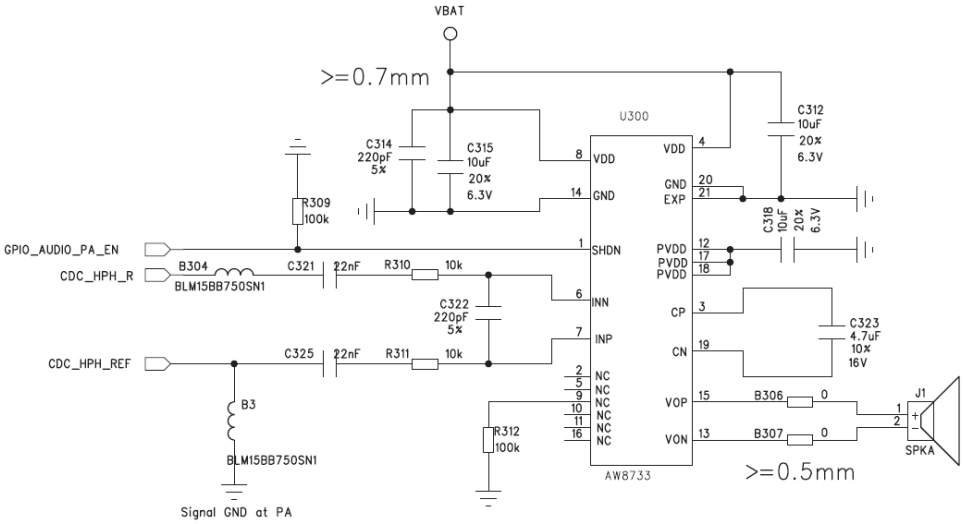


Figure 4.25: Recommended Circuit with External Audio Power Amplifier

4.9.5 I2S Interface

There is a set of GPIO-compatible I2S interfaces inside the module. The pins used by this function are as follows:

Name	Pin	Input/Output	Description
GPIO3	89	I	I2S1 input DATA
GPIO2	90	O	I2S1 output DATA
GPIO1	91	O	I2S1_ SCK
GPIO0	92	O	I2S1_ WS

4.10 USBInterface

The SLM756 supports a USB 2.0 High speed interface. It must control the 90 ohm differential impedance during Layout and control the external trace length according to the internal trace length of the module.
The module supports OTG function at the same time (requires external circuit to provide external 5V power supply)
The voltage input range during charging is as follows:

Table 4.9: Voltage input range during charging

Name	Description	Minimum	Typical	Maximum	Unit
VBUS	Input range	4	-	6.3	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.
USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. It is recommended to add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting TVS, please pay attention to the load capacitance should be less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand, it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

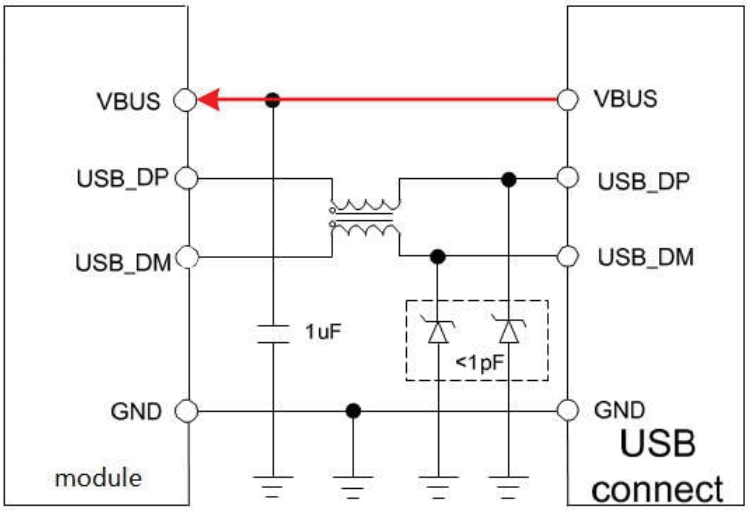


Figure 4.26: USB Connection Diagram

4.10.1 USB OTG

The SLM756 module provides USB OTG functionality and requires an external charging chip or power chip to output 5V power to external devices. The work
The pins that can be used are as follows:

Table 4.10: USB OTG Pin Description

Name	Pin	Decription
USB_DM	112	USB data-
USB_DP	113	USB data+
USB_ID	114	USB ID

The recommended circuit diagram of USBOTG is as follows:

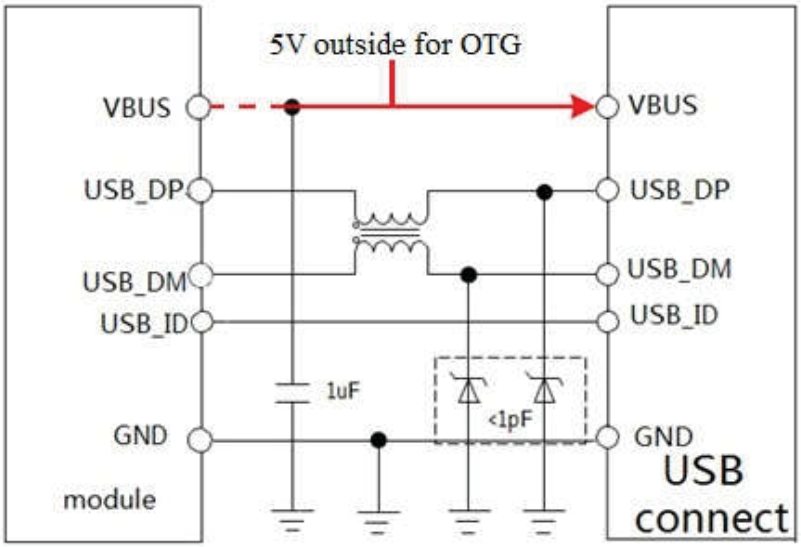


Figure 4.27: USB-OTG Connection Diagram

4.11 Charging Interface

4.11.1 Charging Detection

The USB_VBUS power supply is a USB power supply or an adapter power supply. It can be used as a USB plug-in detection and charge the battery through the internal PMU of the module. The power input voltage range is 4.35~6.3V, and the recommended value is 5V. The module supports single-cell lithium battery charge management, and different capacity models need to set different charging parameters. The module's built-in linear charging circuit supports up to 1.44A of charging current.

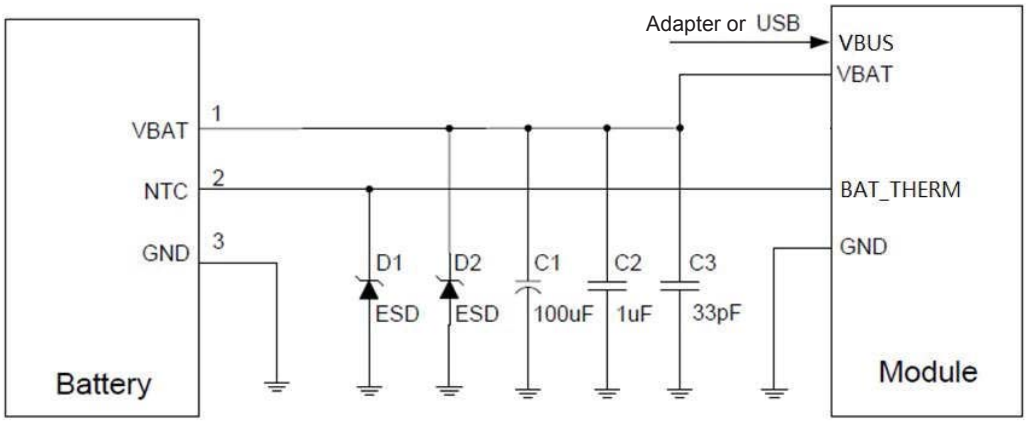


Figure 4.28: Battery connection diagram

4.11.2 Charge Control

The SLM756 module can charge the over-discharged battery. The charging process includes trickle charge, constant current, and constant voltage charging.

Trickle charge: it is divided into 2 parts, trickle charge-A: charge current 90mA when the battery voltage is lower than 2.8V; trickle charge-B: charge current 450mA when the battery voltage is between 2.8V~3.2V;

Constant current charging: When the battery voltage is between 3.2V and 4.2V, the constant current is charged, the charging current is 1.44A when the adapter is charging, and the charging current is 450mA when charging the USB;

Constant voltage charging: When the battery voltage reaches 4.2V, the constant voltage is charged, the charging current is gradually decreased, the charging current is reduced to about 100mA, and the charging is cut off.

4.11.3 BAT _THERM

The SLM756 module has battery temperature detection and can be implemented by BAT_THERM (46PIN). This requires the internal integration of a 10KΩ thermistor (negative temperature coefficient) inside the battery to connect the thermistor to the BAT_THERM pin. During the charging process, the software reads the voltage of the BAT_THERM pin to determine if the battery temperature is too high. If the temperature is too high or too low, the battery will stop charging immediately to prevent battery damage.

4.12 UIM Card Interface

The SLM756 can support two SIM cards at the same time to achieve dual card dual standby. Support SIM card hot swap, can automatically recognize 1.8V and 3.0V cards. The figure below shows the recommended interface circuit for the SIM card. In order to protect the SIM card, it is recommended to use TVS devices for electrostatic protection. The DATA signal requires a 15K resistor to pull up to the SIM power supply. The device of the peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

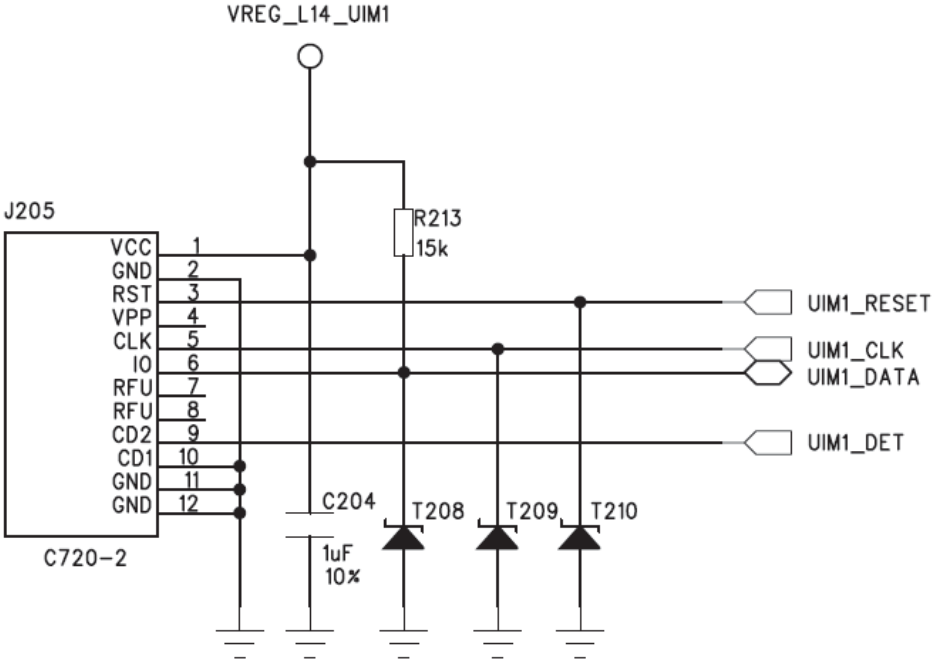


Figure 4.29: UIM card interface circuit

4.13 SD Card Interface

SLM756 supports SD card interface and supports up to 64GB
The reference circuit is as follows:

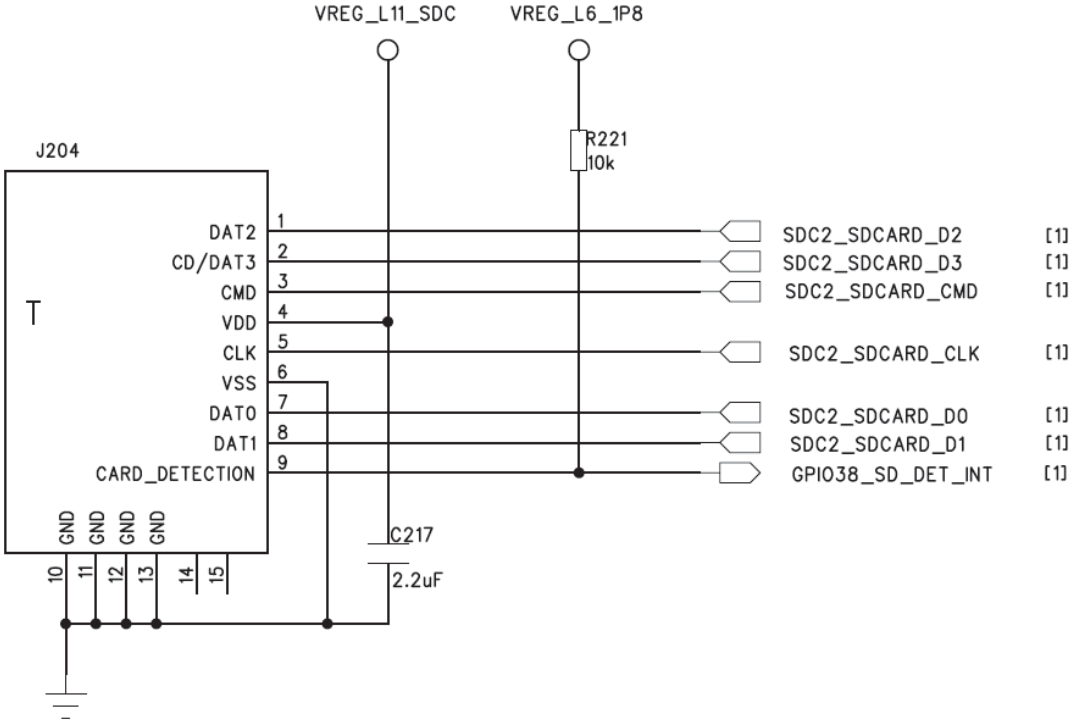


Figure 4.30: SD card interface circuit

4.14 I2C Bus Interface

The SLM756 module supports multiple hardware I2C bus interfaces. The default I2C pin definition functions are as follows:

Table 4.11: Default I2C Interface Pin Description

Name	Pin	Default function
CAM_I2C_SDA	23	Camera dedicated I2C
CAM_I2C_SCL	24	
SENSOR_I2C_SDA	59	General purpose I2C, default for sensor
SENSOR_I2C_SCL	58	
TP_I2C_SDA	72	General purpose I2C, default for TP
TP_I2C_SCL	71	

Note: 1 These 3 groups of I2C have been internally pulled up to VERG_L6_1P8 by default 2.2K, so they cannot be used as normal GPIOs.

2 For other I2C signals, please refer to the table (3.3 Multiplexing Function). If necessary, add an external pull-up resistor.

4.15 Analog to Digital Converter (ADC)

The SLM756 module provides two MPP function signals from the power management chip. MPP4 is the ADC input signal and MPP2 is the PWM signal. The ADC signal is 16-bit resolution, and its performance parameters are as follows:

Table 4.12: ADC Performance Parameters

	Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	Measurement range can be selected by software programming	0.1	-	1.7	V
		0.3	-	4.5	
ADC Resolution		-	16	-	Bits
Analog Input Bandwidth		-	100	-	kHz
Sampling Frequency		-	2.4M	-	MHz
INL		-	-	±8	LSB
DNL		-	-	±4	LSB
Error	Offset error	-	-	±1	%
	Gain error	-	-	±1	%

4.16 PWM

The PWM pin can be used as a backlight adjustment for the LCD to adjust the backlight brightness by adjusting the duty cycle.

4.17 Motor

The SLM756 supports motor functions that can be implemented by the user with GPIO control power. The reference schematic is as follows:

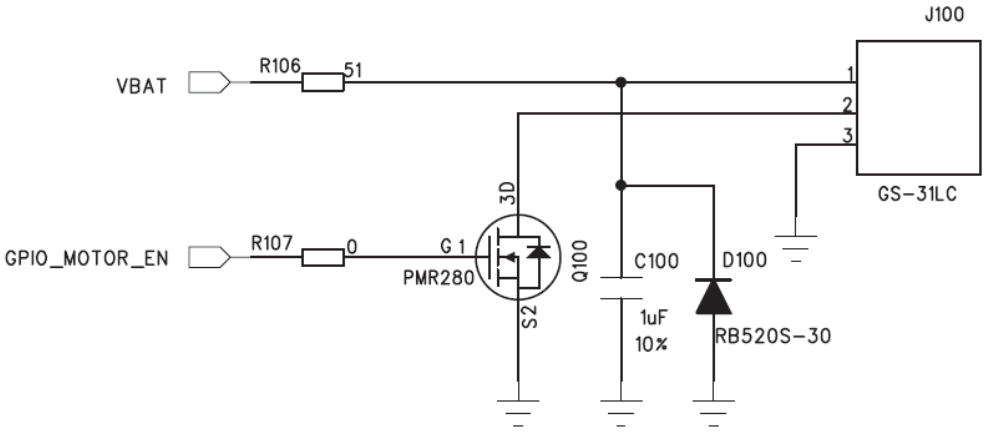


Figure 4.32: Motor interface circuit

4.18 Antenna Interface

The module provides four antenna interfaces: MAIN antenna, DRX antenna, GPS antenna and WiFi/BT antenna. In order to ensure that the user's products have good wireless performance, the antenna selected by the user should meet the requirement that the input impedance is 50 ohms in the working frequency band and the VSWR is less than 2.

4.18.1 Main Antenna

The module provides the MAIN antenna interface pin Pin1 RF_MAIN. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.
In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

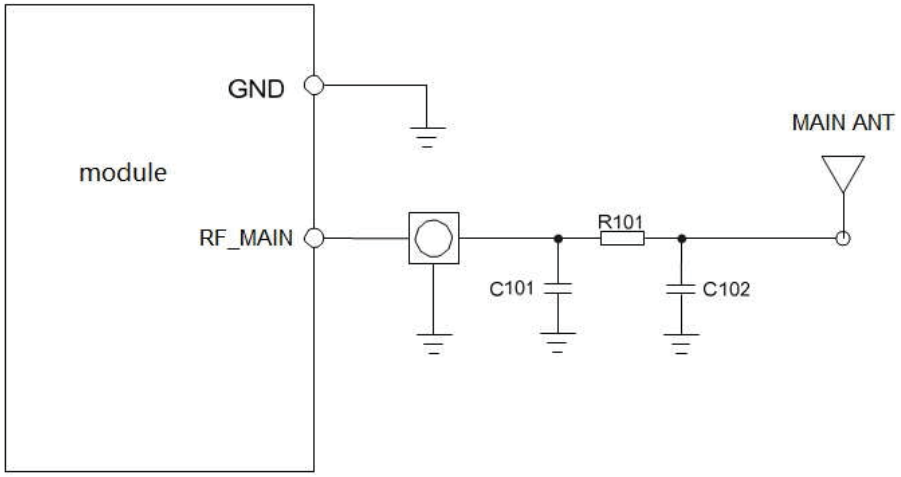


Figure 4.33: MAIN Antenna Interface Connection Circuit

In the figure, R101, C101, and C102 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R101 defaults to 0R, C101 and C102 do not paste by default.
If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

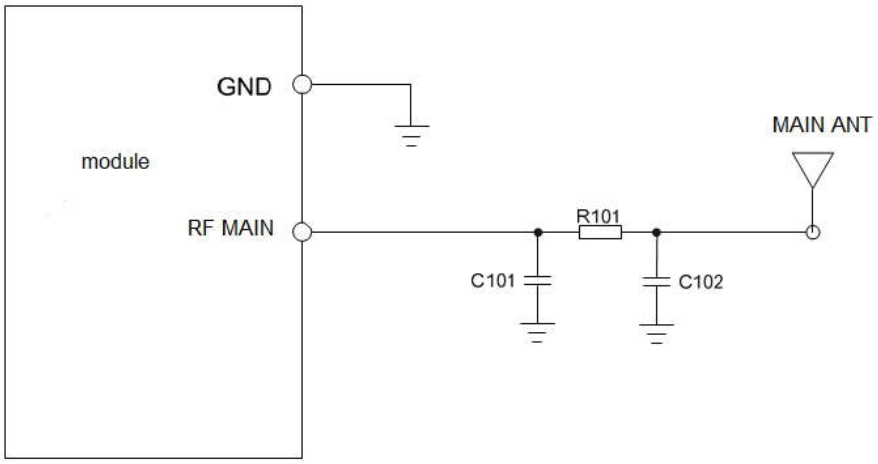


Figure 4.34: MAIN Antenna Interface Simplified Connection Circuit

In the above figure, R101 defaults to 0R, and C101 and C102 do not paste by default.

4.18.2 DRX Antenna

The module provides the DRX antenna interface pin RF_DIV, and the antenna on the user's motherboard should be connected to the module's antenna pins using a 50-ohm characteristic microstrip or stripline.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

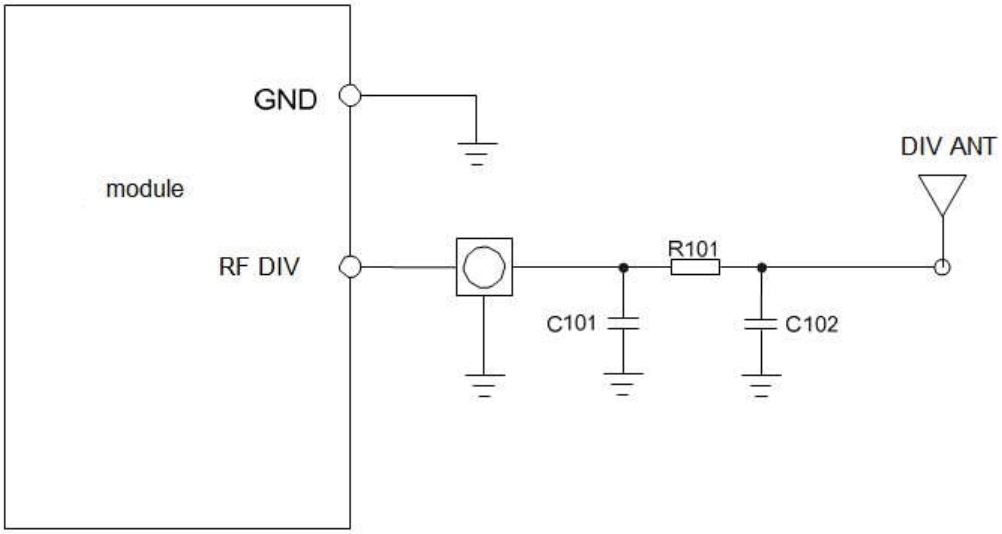


Figure 4.35: DRX Antenna Interface Connection Circuit

In the figure, R102, C103, and C104 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R102 defaults to 0R, C103 and C104 are not posted by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

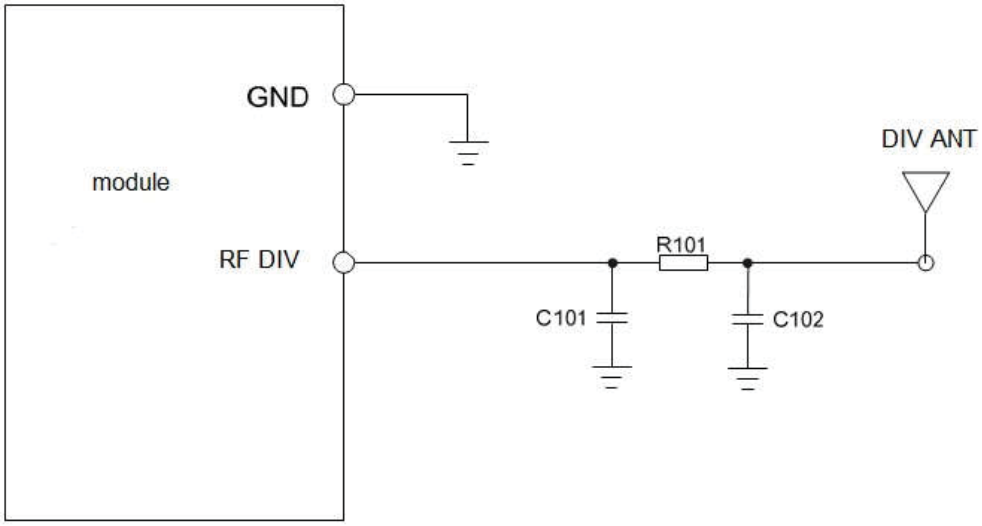


Figure 4.36: DRX Antenna Interface Simplified Connection Circuit

In the above figure, R102 defaults to 0R, C103 and C104 are not attached by default.

4.18.3 GPS Antenna

The module provides the GNSS antenna pin RF_GPS. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line. The LNA is integrated inside the module.
To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connections are as follows:

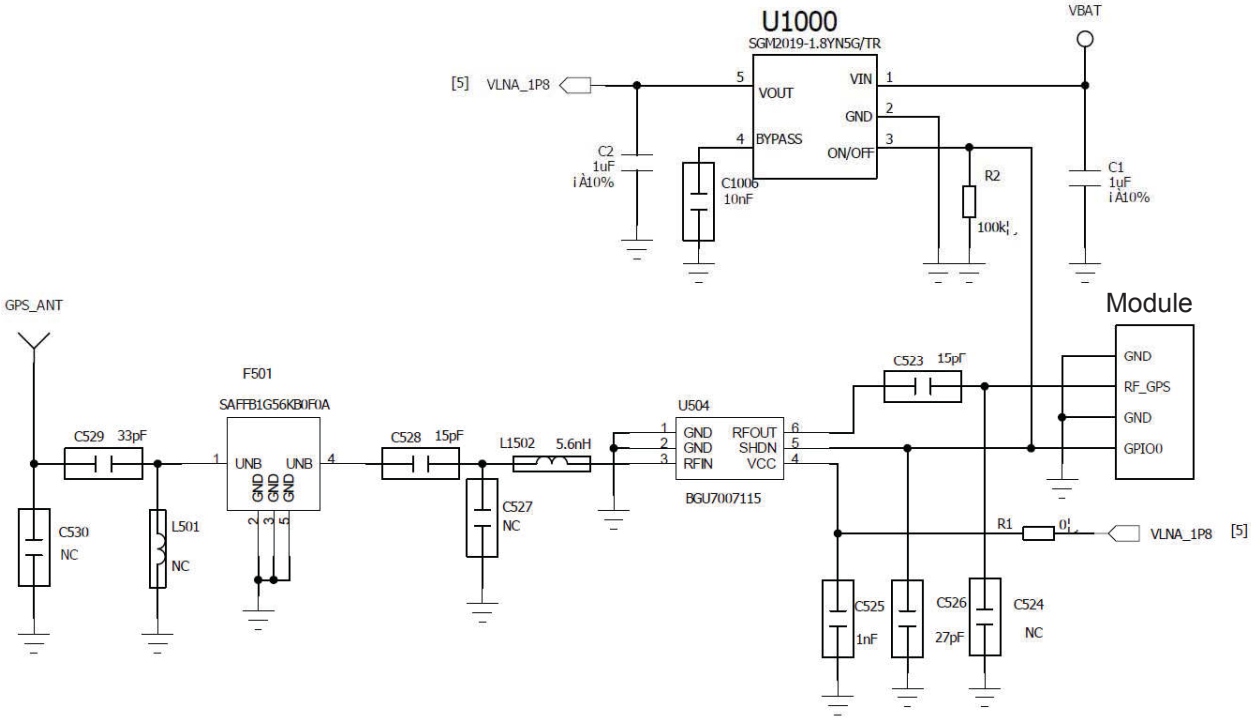


Figure 4.37: Connecting Active Antennas

To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connections are as follows:

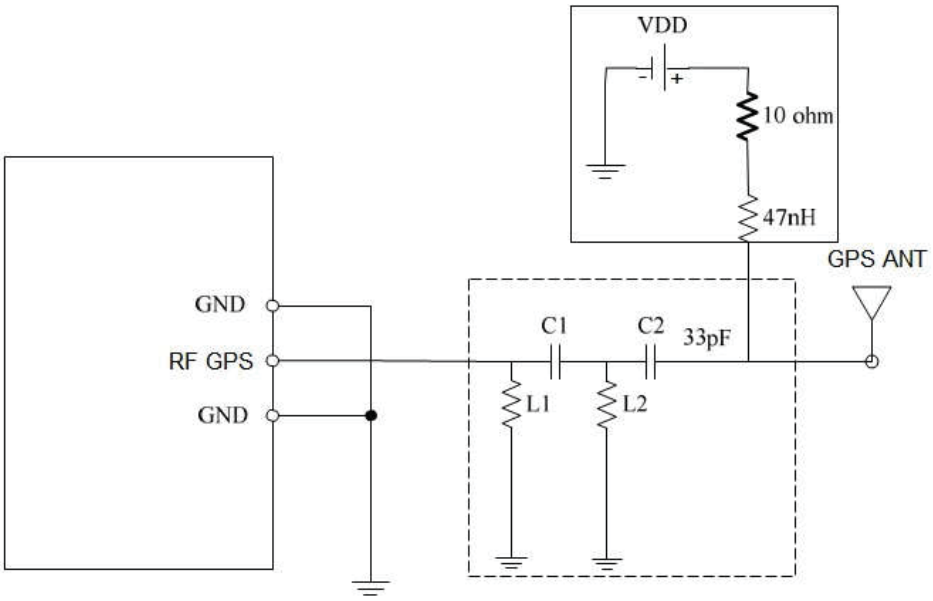


Figure 4.38: Connecting Active Antennas

4.18.4 WiFi/BT antenna

The module provides the WiFi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50 ohm microstrip line or strip line. In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

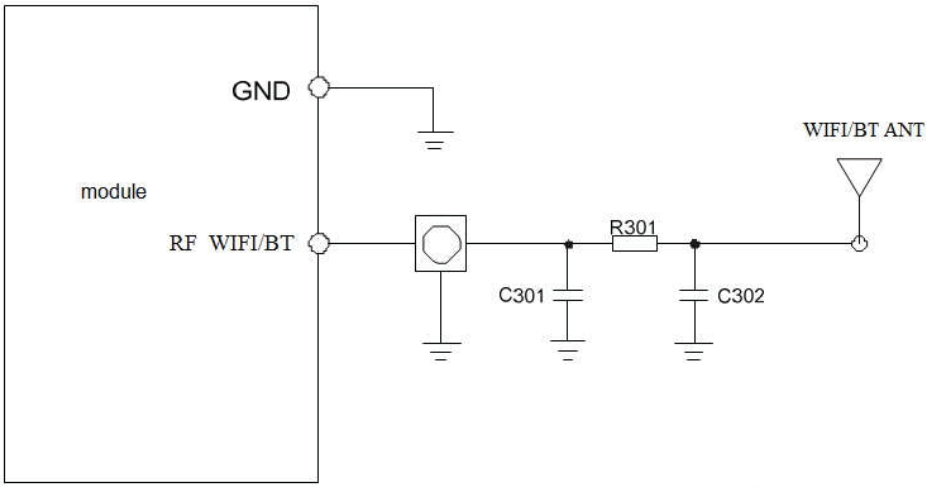


Figure 4.39: WiFI_BT antenna interface connection circuit

In the figure, R301, C301, and C302 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C301 and C302 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

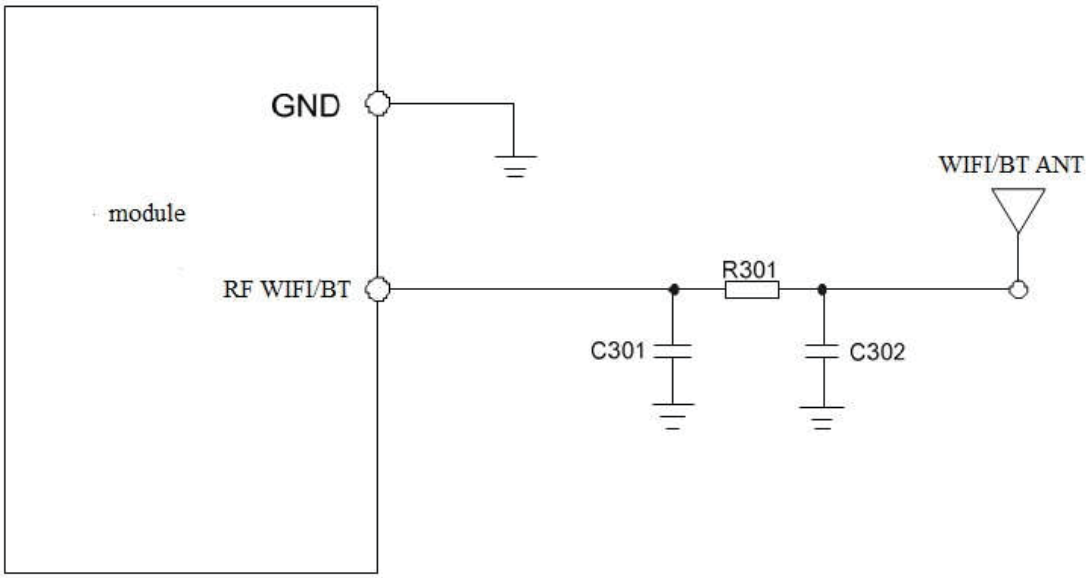


Figure 4.40: WIFI_BT antenna interface simplified connection circuit

In the above figure, R301 defaults to 0R, and C301 and C302 do not paste by default.

5.PCB Layout

The performance of a product depends largely on the PCB trace. As mentioned above, if the PCB layout is unreasonable, it may cause interference problems such as card loss. The way to solve these interferences is often to redesign the PCB. If you can plan a good PCB layout in the early stage, the PCB traces smoothly, saving a lot of time. Of course, it can also save a lot of costs. This chapter mainly introduces some things that users should pay attention to during the PCB layout stage, minimizing interference problems and shortening the user's development cycle.
The SLM756 module is an intelligent module with its own Android operating system. It includes sensitive data lines such as high-speed USB and MIPI. It also has strict requirements on the length and impedance of the signal line. If the high-speed signal processing is not good, it will cause serious EMI. The problem, more serious will also affect the USB identification, LCM display, so the PCB design requirements when using the SLM756 module is much higher than the previous 2G module, please read this chapter carefully, reduce the subsequent hardware debugging cycle.
When using the SLM756 module, the user is required to use at least 4 layers of via design for the impedance control and signal line shielding.

5.1. Module PIN distribution

Before the PCB layout, first understand the pin distribution of the module, and rationally layout the relevant devices and interfaces according to the distribution defined by the pin. Please refer to Figure 2 to determine the distribution of the function feet of the module.

5.2. PCB layout principles

Several aspects of the main attention during the PCB layout phase:

5.2.1. Antenna

Antenna part design, SLM756 module has a total of 5 antenna interfaces, they are: RF_MAIN, RF_DRX, RF_GPS, RF_WIFI, RF_FM. Pay attention to component placement and RF routing:
The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pins of the module;

The antenna matching circuit needs to be placed close to the antenna end;

The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;

The devices and connections between the antenna pins of the module and the antenna connector must be away from high-speed signal lines and strong interference sources to avoid crossing or parallel with any signal lines in adjacent layers.

The length of the RF cable between the antenna pin of the module and the antenna connector should be as short as possible. The situation across the entire PCB should be absolutely avoided.

If the antenna is connected by a coaxial RF line, care should be taken to avoid coaxial RF lines across the SIM card, power circuit, and high-speed digital circuits to minimize the effects of each other.

5.2.2 Power supply

Power traces must consider not only VBAT, but also the return GND of the power supply. The trace of the positive electrode of VBAT must be short. To be thick, the trace must first pass through the large capacitor, Zener diode and then the power PIN of the module. There are multiple PAD exposed copper at the bottom of the module. It is necessary to ensure that the GND path of these exposed copper areas to the power supply is the shortest and most smooth. This ensures that the current path of the entire power supply is the shortest and the interference is minimal.

5.2.3. SIM card

The size of the SIM card is large, and there is no anti-EMI interference device itself, which is relatively susceptible to interference. Therefore, in the layout, first ensure that the SIM card is away from the antenna and the antenna extension cable inside the product, as close as possible to the module. When the PCB is routed, pay attention to The SIM_CLK signal is protected, and the SIM_DATA, SIM_RST, and SIM_VDD signals of the SIM card are away from the power source and away from the high-speed signal line. If the processing is not easy, it may cause problems such as not knowing the card or dropping the card. Therefore, please follow the following principles when designing:

- Keep the SIM card holder away from the antenna during the PCB layout phase;
- Keep the SIM card away from the RF line, VBAT, and high-speed signal lines, and do not leave the SIM card too long.
- The GND of the SIM card holder should be in good communication with the GND of the module to make the GND equipotential between the two.
- To prevent SIM_CLK from interfering with other signals, it is recommended to protect SIM_CLK.
- It is recommended to place a 100nF capacitor on the SIM_VDD signal line near the SIM card holder.
- Place TVS near the SIM card holder. The parasitic capacitance of the TVS should not exceed 50pF. The 51Ω resistor in series with the module can enhance ESD protection.
- The SIM card signal line increases the capacitance of 22pf to ground to prevent radio frequency interference.
- The VBAT's return path has a large current, so the SIM card trace should avoid the VBAT return path.

5.2.4. MIPI

MIPI is a high-speed signal line. Users must pay attention to protection during the layout phase, so that they are away from the signal lines that are easily interfered. The GND processing must be performed on the upper and lower sides, and the traces are differential pairs. 100 ohm differential impedance matching is performed. Ensure impedance consistency and do not bridge different GND planes as much as possible.
The MIPI interface selects a small-capacity TVS when selecting an ESD device. It is recommended that the parasitic capacitance be less than 1pF.
The MIPI routing requirements are as follows:

- The total length of the cable does not exceed 305mm
- It is required to control 100 ohm differential impedance with an error of ±10%.
- The error of the differential line length within the group is controlled within 0.7mm.
- The length error between groups is controlled within 1.4mm.

5.2.5. USB

The module supports high-speed USB interface at a rate of 480Mbps. The user recommends adding a common-mode inductor during the schematic design phase to effectively suppress EMI interference. If you need to increase the static protection, please select a TVS tube with a parasitic capacitance of less than 1pF. Please refer to the following notes when planning:

- The common mode inductor should be close to the USB connector side.
- It is required to control the 90 ohm differential impedance with an error of ±10%.
- The differential line length error is controlled within 6mm.
- If the USB has a charging function, please note that the VBUS cable is as wide as possible.
- If there is a test point, try to avoid the split line and put the test point on the path of the trace.

Table 5.1:

Pin	Signal	Length(mm)	Length Error（P-N）
14	USB_DP	26.2	0.2mm
13	USB_DM	26.5	

5.2.6.Audio

The module supports 3 analog audio signals. Analog signals are susceptible to interference from high speed digital signals. So stay away from high-speed digital signal lines. The module supports the WCDMA/LTE system, and the WCDMA/LTE signal can interfere with the audio by coupling and conduction.

The users should pay attention to keeping the audio trace away from the WCDMA/LTE antenna and VBAT during PCB layout and routing. The filter capacitor of the audio is preferably placed close to the module end and placed next to the interface end. The audio output should be routed according to the differential signal rules.
The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the fzizig sound at the SPK output. Therefore, it is better to connect in parallel with the input of the Audio PA in the schematic design. Some large capacitance capacitors and series magnetic beads.
FDD and GND also have a great relationship. If GND is not handled well, many high-frequency interference signals will interfere with MIC and Speaker through devices such as bypass capacitors, so users should ensure good performance of GND during PCB design.

5.2.7. Other

The serial port interface of the module should also be kept as short as possible. It is best to walk in a group when routing, and do not distract the wires.

6. Electrical, Reliability

6.1 Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 6.2: Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	-	-	6	V
VBUS	-	-	10.5	V
Peak current	-	-	3	A

6.2 Working Temperature

The table below shows the operating temperature range of the module:

Table 6.2: Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	h
Storage temperature	-40	-	90	h

6.3 Working Voltage

Table 6.3: Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.4	-	4.2	V
VBUS	4	5	6	V
Hardware shutdown voltage	2.5	2.8	-	V

6.4 Digital Interface Features

Table 6.4: Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	1.17	-	-	V
V_{IL}	Input low level voltage	-	-	0.63	V
V_{OH}	Output high level voltage	1.35	-	-	V
V_{OL}	Output low level voltage	-	-	0.45	V

6.5 SIM_VDD Characteristics

Table 6.5: SIM_VDD Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
V_O	Output voltage	-	3	-	V
		-	1.8	-	
I_O	Output current	-	-	55	mA

6.6 PWRKEY Feature

Table 6.6: PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	low level	-	-	0.6	V
	Effective time	2000			ms

6.7 VCOIN Feature

Table 6.6: VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
$VCOIN_{-IN}$	VCOIN input voltage	2	3	3.25	V
I_{RTC-IN}	VCOINCurrent consumption	-	-	8	uA
$VCOIN_{-OUT}$	VCOIN Output voltage	-	3	-	V
$I_{RTC-OUT}$	VCOIN Output current	-	-	2	mA

6.8 Current Consumption (VBAT = 3.8V)

Table 6.8: Current consumption

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
VBAT	voltage	Voltage must be between the maximum and minimum values	3.4	3.8	4.2	V
Ivbat	Average current	Shutdown mode	-	-	TBD	uA
		WCDMA Standby power consumption	-	-	TBD	mA
		FDD Standby power consumption			TBD	mA

6.9 Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling, and operating modules.

6.10 Module Operating Frequency Band

The table below lists the operating frequency bands of the module and complies with the 3GPP TS 05.05 technical specification.
Table 6.9: Module Operating Band

Frequency	Receive	Transmission	
WCDMA B2	1930~1990MHZ	1850~1910MHZ	
WCDMA B4	2110~2155MHz	1710~1755MHz	
WCDMA B5	869 ~ 894MHz	824 ~ 849MHz	
LTE B2	1930 ~ 1990 MHz	1850 ~ 1910 MHz	
LTE B4	2110 ~ 2155 MHz	1710 ~ 1755 MHz	
LTE B5	869~894MHz	824~849MHz	
LTE B7	2620~2690MHz	2500 ~ 2570MHz	
LTE B12	729~746MHz	699 ~ 716MHz	
LTE B13	746~756MHz	777 ~ 787MHz	
LTE B17	734~746MHz	704~716MHz	

6.11 RF Characteristics

The following table lists the conducted RF output power of the module, in accordance with 3GPP TS 05.05 technical specification, 3GPP TS 134121-1 standard.
Table 6.10: Conducted Output Power

Frequency band	tune-up output power (dBm)
WCDMA band II	23
WCDMA band IV	23
WCDMA band V	24
LTE Band 2	22
LTE Band 4	23
LTE Band 5	23
LTE Band 7	23
LTE Band 12	25
LTE Band 13	23
LTE Band 17	25

6.12 Module Conduction Receiving Sensitivity

The table below lists the conducted receive sensitivity of the module and is tested under static conditions.
Table 6.11: Conducted Receive Sensitivity

Frequency band	Receive sensitivity (typical)	Receive sensitivity (maximum)
WCDMAB5	<-109 dBm	3GPP Claim
LTEFDD	See table 6.12	3GPP Claim

Table 6.12: LTE Reference Sensitivity 3GPP Dual Antenna Requirements (QPSK)

E-UTRA Frequency band number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex mode
3#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	FDD#
;#	T3L;2J#	T``2J#	T`4#	T`K#	T`52;#	T`;#	FDD#
5#	T3L32J#	T`42J#	T`J#	T`1#	T`;2;#	T`3#	FDD#
1#	T3L12J#	T3L32J#	T3LL#	T`J#	T`K2;#	T`1#	FDD#
K#	T3L52;#	T3LL2;#	T`4#	T`K#			FDD#
a#	T#	T#	T3LL#	T`J#			FDD#
J#	T#	T#	T`4#	T`K#	T`52;#	T`;#	FDD#
4#	T3L;2;#	T``2;#	T`J#	T`1#			FDD#
`#	T#	T#	T``#	T`a#	T`12;#	T`5#	FDD#
3L#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	FDD#
33#	T#	T#	T3LL#	T`J#			FDD#
3;#	T3L32J#	T`42J#	T`J#	T`1#			FDD#
35#			T`J#	T`1#			FDD#
31#		T#	T`J#	T`1#			FDD#
222#							
3J#	T#	T#	T`J#	T`1#			FDD#
34#	T#	T#	T3LL^{J}#	T`J^{J}#	T`K2;^{J}#	T#	FDD#
3`#	T#	T#	T3LL#	T`J#	T`K2;#	T#	FDD#
;L#			T`J#	T`1#	T`32;#	T`L#	FDD#
;3#			T3LL#	T`J#	T`K2;#		FDD#
;;#			T`J#	T`1#	T`;2;#	T`3#	FDD#
;5#	T3L12J#	T3L32J#	T3LL#	T`J#	T`K2;#	T`1#	FDD#
;1#			T3LL#	T`J#			FDD#
;K#	T3L32;#	T`42;#	T`a2K#	T`52K#	T`32J#	T`L2K#	FDD#
;a#	T3L;2J#	T``2J#	T`J2K^{a}#	T`12K^{a}#	T`;2J^{a}#		FDD#
;J#	T3L52;#	T3LL2;#	T`4#	T`K#			FDD#
;4#		T3LL2;#	T`42K#	T`K2K#	T`52J#	T`3#	FDD#
53#	T``2L#	T`K2J#	T`52K#				FDD#
222#							
55#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
51#	T#	T#	T3LL#	T`J#	T`K2;#	T#	X^^#
5K#	T3La2;#	T3L;2;#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
5a#	T3La2;#	T3L;2;#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
5J#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
54#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
5`#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
1L#	T#	T#	T3LL#	T`J#	T`K2;#	T`1#	X^^#
13#	T#	T#	T`4#	T`K#	T`52;#	T`;#	X^^#

6.13 WIFI Main RF Performance

The table below lists the main RF performance under WIFI conduction.
Table 6.13: Main RF performance parameters under WIFI conduction

Transmission performance				
	802.11B	802.11G	802.11N	
Transmit power (minimum rate)	18	17	17	dBm
Transmit power (maximum rate)	17	15	13	dBm
EVM (maximum rate)	20%	-27	-30	dB
Receiving performance				
Receiving sensitivity	802.11B	802.11G	802.11N	
Minimum rate	-92	-91	-90	dBm
Maximum rate	-89	-74.5	-72.5	dBm

6.14 BT Main RF Prformance

The table below lists the main RF performance under BT conduction.
Table 6.14: Main RF performance parameters under BT conduction

Transmission performance				
Transmit power	GFSK	π/4-DQPSK	8DPSK	
	10.34	11.32	11.45	dBm
Receiving performance				
Receiving sensitivity	DH5	2DH5	3DH5	
	-94.5	-94.5	-86	dBm

6.15 GNSS Main RF Performance

The table below lists the main RF performance under GNSS conduction.

Table 6.15: Main RF performance parameters under GNSS conduction

GNSS working frequency band: 1575.42MHZ				
GNSS carrier-to-noise ratio CN0: 39dB/Hz				
GNSS sensitivity:	Capture (cold start)	Capture (hot start)	Track	
	-148	-156	-160	dBm
GNSS startup time	Hot start	Warm start	Cold start	
	TBD	TBD	TBD	

7. Production

7.1. Top And Bottom Views Of The Module

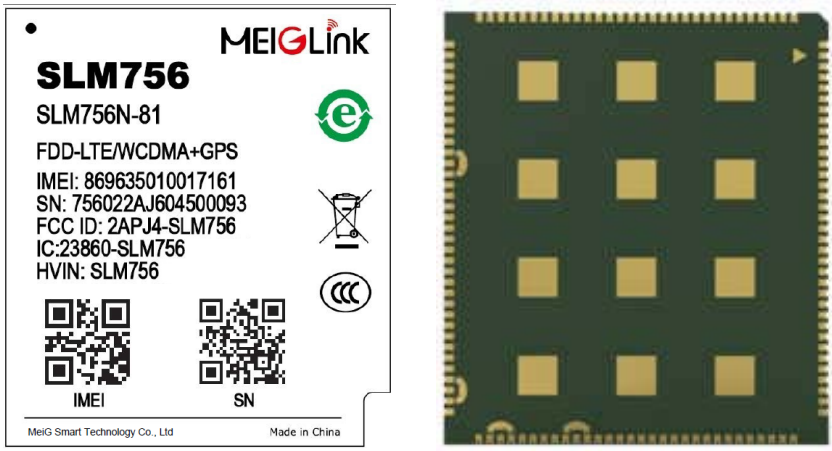


Figure 48: Module top and bottom views

7.2. Recommended Soldering Furnace Temperature Curve

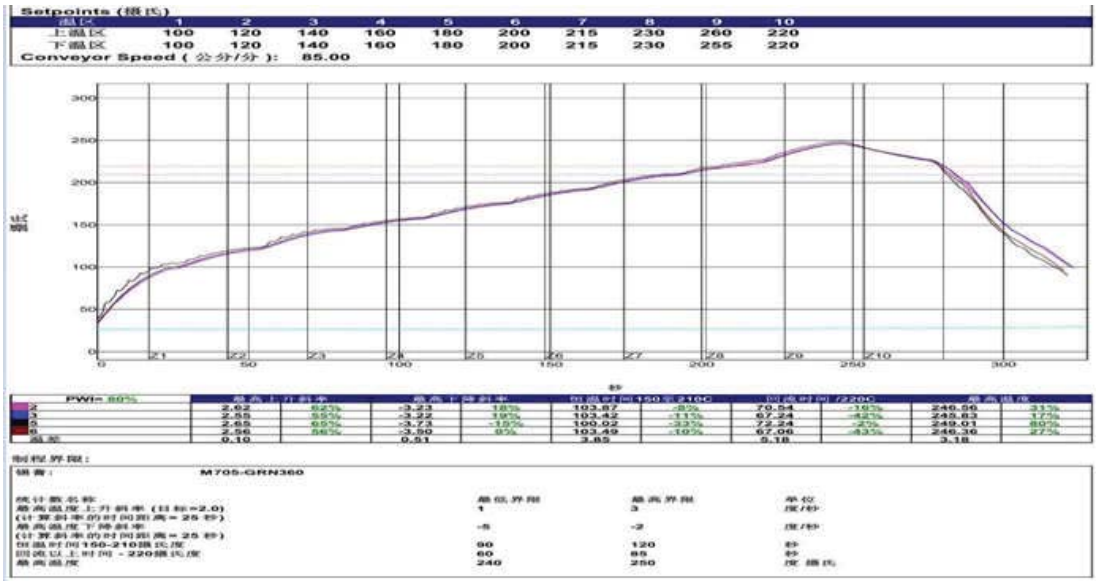


Figure 49: Module recommended soldering furnace temperature curve

7.3. Humidity Sensitivity (MSL)

The SLM756 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of <30 degrees of temperature and <60% of relative humidity. Under ambient conditions of temperature <40 degrees and relative humidity <90%, the shelf life is

at least 6 months without unpacking. After unpacking, Table 22 lists the shelf life of the modules for different moisture sensitivity levels.

Table 7.1: Humidity sensitivity level distinction

Grade	Factory environmenti +30h /60%RH
1	Indefinite quality in the environmenti +30h /85% RH Under conditions
2	1 Year
2a	4 Weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the time limit specified on the label.

After unpacking, the SMT patch should be performed within 168 hours under ambient conditions of <30 degrees and relative humidity <60%. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solderability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solderability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90 ° C and as high as 125 ° C.

7.4. Baking Requirements

The MEIG Smart Module has a moisture rating of three. The SLM756 should be fully baked before reflow soldering, otherwise the module may cause permanent damage during reflow. The SLM756 can use the following three baking conditions. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 7.2: Baking requirements:

Baking condition	40°/5%RH	60°/5%RH	90°/5%RH
Baking time	30 Days	72 Hours	48Hours
Description	Original tray can be used	Original tray can be used	Original tray cannot be used

8. Support Peripheral Device List

Table 8.1: List of supported display models

Vendor	Drive IC
DJN/Dijing	ILI9881C
HOLITECH/Helitai	ILI9881C

Table 8.2: List of supported camera models

Vendor	Drive IC
GXKJ/High image technology	SP5506
GXKJ/High image technology	SP2509

Table 8.3: List of supported touch screen models

Vendor	Drive IC
DJN/Dijing	GT5688
HOLITECH/Helitai	GT5688
DIXIAN/Emperor Xian	GT970

Table8.4：List of supported G sensor models

Vendor	Model	Specification
Bosch/Bosch	BMA223	3-Axis,8-bit

Table8.5：List of supported Ecompass models

Vendor	Model	Specification
AKM/Asahi Kasei	AK09911	3-Axis,14-bit

Table8.6：List of supported PS/ALS Sensor models

Vendor	Model	Specification
Elan/Yilong	EPL2182KQWJ0	ALS+PS

Table8.7：List of supported Gyro Sensor models

Vendor	Model	Specification
Bosch/Bosch	BMI120	9-axis,16bit/16bit

Table8.8： List of supported Flash LED Driver models

Vendor	Model	Specification
SGMICRO/Saint Bonwe	SGM3785YTDP14G/TR	FLASH LED Driver,1.5A

Table 8.8: Peripheral Support List

Peripheral	Vendor	Model
Fingerprint recognition	ZHIANG/Ang	
Fingerprint recognition	FingerCrystal/Finger core	
Identification	CHINA-VISION/Huashi	
Sweeping the pier	Zeba	

9. Appendix

9.1. Terms And Explanations

Table 9.2: Terms and explanations

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send

DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Phone book abbreviation	Explanations
FD	SIM fix dialing phonebook

LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

9.3. Multiplexing function

Table 9.3: Multiplexing Functions

GPIO	Module pin	BLSP multiplexing function (default is blue)			Other functions besides BLSP
		SPI	UART	I2C	
GPIO0	92	MOSI			I2S/GPIO
GPIO1	91	MISO			I2S/GPIO
GPIO2	90	CS_N			I2S/GPIO
GPIO3	89	CLK			I2S/GPIO
GPIO4	82	MOSI	TX		GPIO
GPIO5	81	MISO	RX		GPIO
GPIO6	59	CS_N	CTS	SDA	GPIO
GPIO7	58	CLK	RTS	SCL	GPIO
GPIO8	116	MOSI			GPIO
GPIO9	10	MISO			GPIO
GPIO10	11	CS_N		SDA	GPIO
GPIO11	83	CLK		SCL	GPIO
GPIO12	74	MOSI			GPIO
GPIO13	73	MISO			GPIO
GPIO14	76	CS_N		SDA	GPIO
GPIO15	75	CLK		SCL	GPIO
GPIO16	70	MOSI			GPIO
GPIO17	69	MISO			GPIO
GPIO18	72	CS_N		SDA	GPIO
GPIO19	71	CLK		SCL	GPIO
GPIO20	80	MOSI	TX		GPIO
GPIO21	79	MISO	RX		GPIO
GPIO111	78	CS_N	CTS	SDA	GPIO
GPIO112	77	CLK	RTS	SCL	GPIO

9.4. Safety Warning

Pay attention to the following safety precautions when using or repairing any terminal or mobile phone that contains modules. The user should be informed of the following safety information on the terminal device. Otherwise, MeiG will not be responsible for any consequences caused by the user not following these warning actions.

Table 9.4: Security Warnings

Identification	Claim
	When you are at a hospital or medical facility, observe the restrictions on using your phone. If necessary, please turn off the terminal or mobile phone, otherwise the medical device may malfunction due to radio frequency interference.
	Turn off the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the aircraft. Ignoring the above will violate local laws and may result in a flight accident.
	Do not use mobile terminals or mobile phones in front of flammable gases. Turn off the mobile terminal when you are near an explosion, chemical factory, fuel depot, or gas station. It is dangerous to operate a mobile terminal next to any potentially explosive electrical equipment.
	The mobile terminal receives or transmits radio frequency energy when it is turned on. It can interfere with TV, radio, computer or other electrical equipment.
	Road safety first! Do not use a handheld terminal or mobile phone while driving, please use a hands-free device. Stop before using your handheld terminal or mobile phone.
SOS	mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

FCC Certification Requirements.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.
FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Regulatory Module Integration Instructions
This device complies with part 22H/24E/27 and Part 15.247 of the FCC Rules RSS130/132/133/139/199 and RSS-247 of the ISED Rules .
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

This module has been granted modular approval for mobile applications. OEM integrators for host products may use the module in their final products without additional FCC certification if they meet the following conditions. Otherwise, additional FCC approvals must be obtained.

The host product with the module installed must be evaluated for simultaneous transmission requirements.

The user's manual for the host product must clearly indicate the operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, use this module only with the included onboard antenna.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

Single Module Approval,Output power is conducted,This device is to be used or fixed applications only,Antenna gain including cables loss must not exceed 10dBi@WCDMA Band II/LTE Band 2 , 7dBi@ WCDMABand IV/ LTE Band 4 , 10.35dBi@ WCDMABand V/LTE Band 5 , 10.00dBi @LTE Band 7, 8.67dBi @ LTE Band 12/LTE Band 17,11.11dBi @ LTE Band 13.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF

The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre

For IC , to meet RF exposure & ERP/ERIP, the maximum net gain of antennas allowed are 10dBi@WCDMA Band II/LTE Band 2 , 7dBi@ WCDMABand IV/ LTE Band 4 , 10.35dBi@ WCDMABand V/LTE Band 5 ,10.00dBi @LTE Band 7, 8.67dBi @ LTE Band 12/LTE Band 17,11.11dBi @ LTE Band 13.

End Product Labeling:

The outside of final products that contains this module device must display a label referring to the enclosed module. This exterior label can use wording such as: "Contains Transmitter Module FCC ID: 2APJ4-SLM756 / IC:23860-SLM756 or “Contains FCC ID:2APJ4-SLM756 / IC:23860-SLM756 , Any similar wording that expresses the same meaning may be used.

Étiquetage du produit final: L'extérieur des produits finis contenant ce module doit afficher une étiquette faisant référence au module inclus. Cette étiquette extérieure peut utiliser des libellés tels que: "Contient le module émetteur ID FCC: 2APJ4-SLM756 / IC: 23860-SLM756 ou" Contient l'ID FCC: 2APJ4-SLM756 / IC: 23860-SLM756, Tout libellé similaire exprimant le même sens peut être utilisé.