SNM900 Hardware Design Guide

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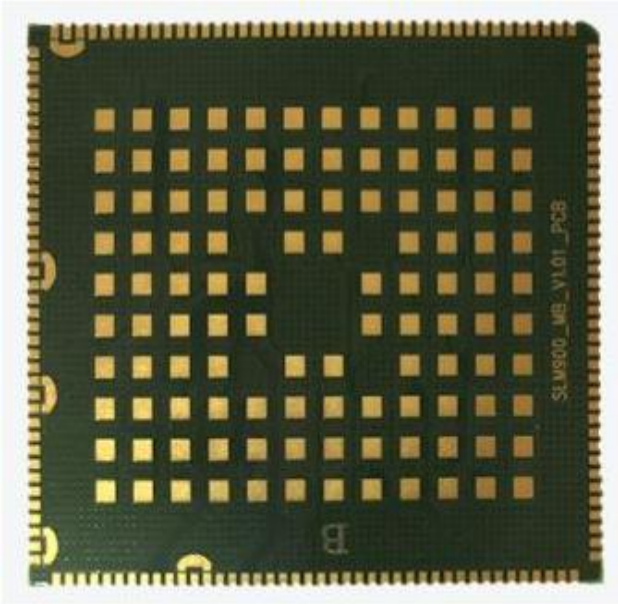

Foreword

Thank you for using the SNM900 module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

Before the announcement, the company has the right to modify the contents of this manual according to the needs of technological development.

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Version History

Date	Version	Change description	Author
2019-10-21	1.00	First edition	Hardware Department
2020-2-17	1.01	Modify 3.1 pin distribution	Hardware Department
2020-11	1.02	Modify some pin descriptions	Hardware Department

1. Introduction

This document describes the hardware application interface of the module, including the connection of the circuit and the RF interface.It can help users quickly understand the interface definition, electrical performance, and structural dimensions of the module.Combining this document with other application documents, users can quickly use modules to design mobile communication applications.

2. Module overview

The core board of SNM900 series adopts sdm660 of Qualcomm snapdragon 600 series. The CPU is made of 14nm FinFET, with 64bit arm and 8-core kryo 260 CPU (kryo Gold: Quad high-performance cores targeting 2.2 GHz, kryo silver: Quad low-power cores targeting 1.843 GHz). Main frequency 2.2g processor, support lpddr4 / 4x SDRAM memory.
This module is suitable for the broadband intelligent wireless

SNM900 not only provides high-speed broadband data access, but also provides voice, SMS, address book, WiFi, BT functions; the product supports dual 1600W 3D camera or depth of field photography, and can be widely used in police law enforcement instruments, intelligent POS cash registers, logistics terminals, VR Camera, intelligent robot, video monitoring, security monitoring, vehicle mounted equipment, intelligent information acquisition equipment, intelligent handheld terminal, UAV and other products.

The physical interface of the module is a 272-pin pad that provides the following hardware interfaces:

- Three 1.8V UART serial ports, supporting four or two wires.
- Main LCD（MIPI interface）+Secondary LCD（MIPI interface）.
- LCD backlight interface.
- Three-way Camera interface（MIPI data ）.
- Flashlight interface
- Two high-speed USB interface.
- Three channel analog audio input interface
- Two channel digital mic interface
- Three channel audio output interface
- Two-way UIM card interface
- GPIO interface.
- Five groups of I2C interface
- Two sets of SPI interfaces
- One TF card interface
- Support GNSS,WiFi, Bluetooth 5.0.

2.1 Summary of features

Table 2.1：SNM900 features

Product	Description
Plateform	Qualcomm SDM660
CPU	Octa-core Kryo 260 CPU
GPU	Adreno512;650MHz
System memory	32GB eMMC + 3GB LPDDR4X 1866Mhz compatible with 64GB+4GB,128GB+6GB
OS	Android 9.0
Size	45.5x41.0x3.0mm，Stamp hole package 160pin + 112pin LCC + LGA
Wi-Fi	WCN3980:IEEE 802.11b/g/n/ac 2.4G&5G
Bluetooth	BT 5.0
FM	I won't support it
SIM	DSDS(Dual Sim-card Dual Stanby) 3.0/1.8V Support SIM hot plug L/W/G/T+G L/W/G/T+W L/W/G/T+1X L/EVDO/CDMA1X+G，

	Don't support dual CDMA SIM card	
Display (screen/subscreen)	Matrix: FULL HD: 2560*1600 60fps;	
	LCD Size: User defined	
	Interface: 1st LCM：MIPI DSI 4-lane; 2nd LCM：MIPI DSI 4-lane	
Camera (Front and Rear)	Interface: Support three sets of CSI, each group is 4-Lane	
	Camera Pixel:Rear 16-16Mp/Front up to 16Mp ， Dual ISP can support dual 24MP Camera at the same time	
	Video decode	4K30 8-bit: H.264/VP8/VP9 4K30 10-bit: HEVC
	Video encode	4K30 HEVC/H264/VP8/MPEG4
Input Device	Key（Power on/off,Home,RESET,VOL+,VOL-)	
	Capacitive TP	
Reset	Support HW reset	
Application interface	Interface name	Main function description
	VBAT	3pin，Power input，3.5V～4.35V，Nominal value3.8V
	SDIO *1	TF Card，Support 128GB max
	USB2.0(3.0)	Support OTG USB_BOOT（Force USB boot for emergency downloads)
	BLSP ports	8 ports(BLSP1-8), 4-bits each, multiplexed serial interface functions
	UART*5	BLSP1-2,BLSP7-8&BLSP5 support UART，up to 4 Mbps
	I2C*9	BLSP1-8&LPI_GPIO2-3 support I2C, These BLSPs use bits [1:0] for I2C
	SPI(master only)	SPI is only support via BLSP
	ADC*2	Support
	Charge	Support Quick Charge 3.0/4.0
	Vibrator	Support
	GPIO	19 gpios, excluding blsp multiplexing GPIO and LCM TP camera related GPIO
	VCOIN	Real time clock backup battery
	RF Interface	Multimode LTE main antenna Multimode LTE diversity antenna The GPS antenna 2.4G WiFi/BT antenna 5G WIFI- antenna
	Audio	One main MIC One noise reduction MIC One Handsfree speaker（Built in 0.8W Class D

		amplifier) One earpiece One stereo headphone(With headphone MIC) 2-channel digital mic signal (can support 4 digital MICs at the same time)Two I2S signal

2.2 Block diagram

The following figure lists the main functional parts of the module:

- SDM660 baseband chip
- PM660，PM660L power management chip
- WCN3980-WIFI/BT/FM three in one chip
- Antenna interface
- LCD/CAM-MIPI interface
- EMCP memory chip
- AUDIO interface
- UART, SD card interface, SIM card interface,I2C interface,etc.

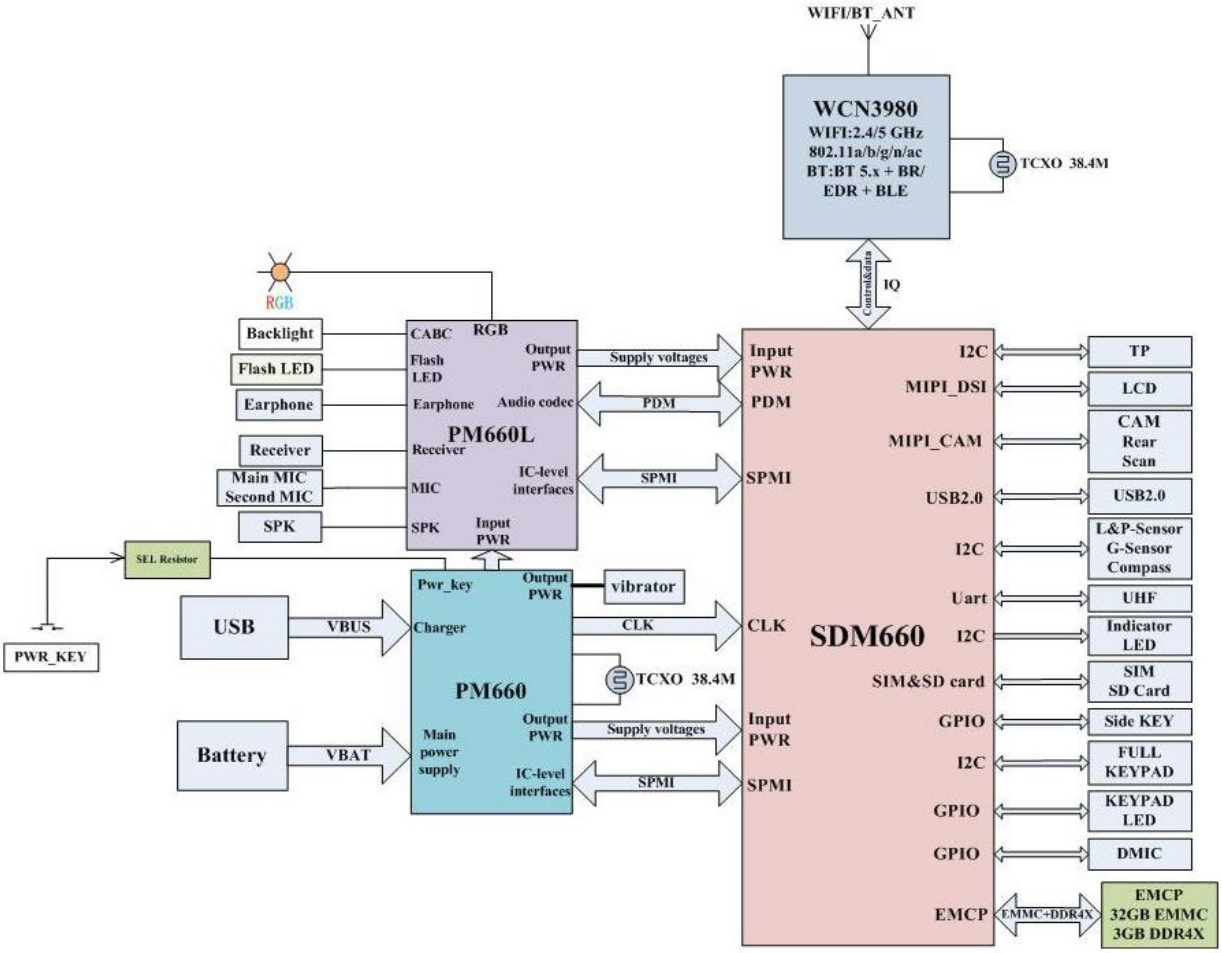


Figure 2.1: module function block diagram

3. Module Package

3.1.Pin distribution diagram

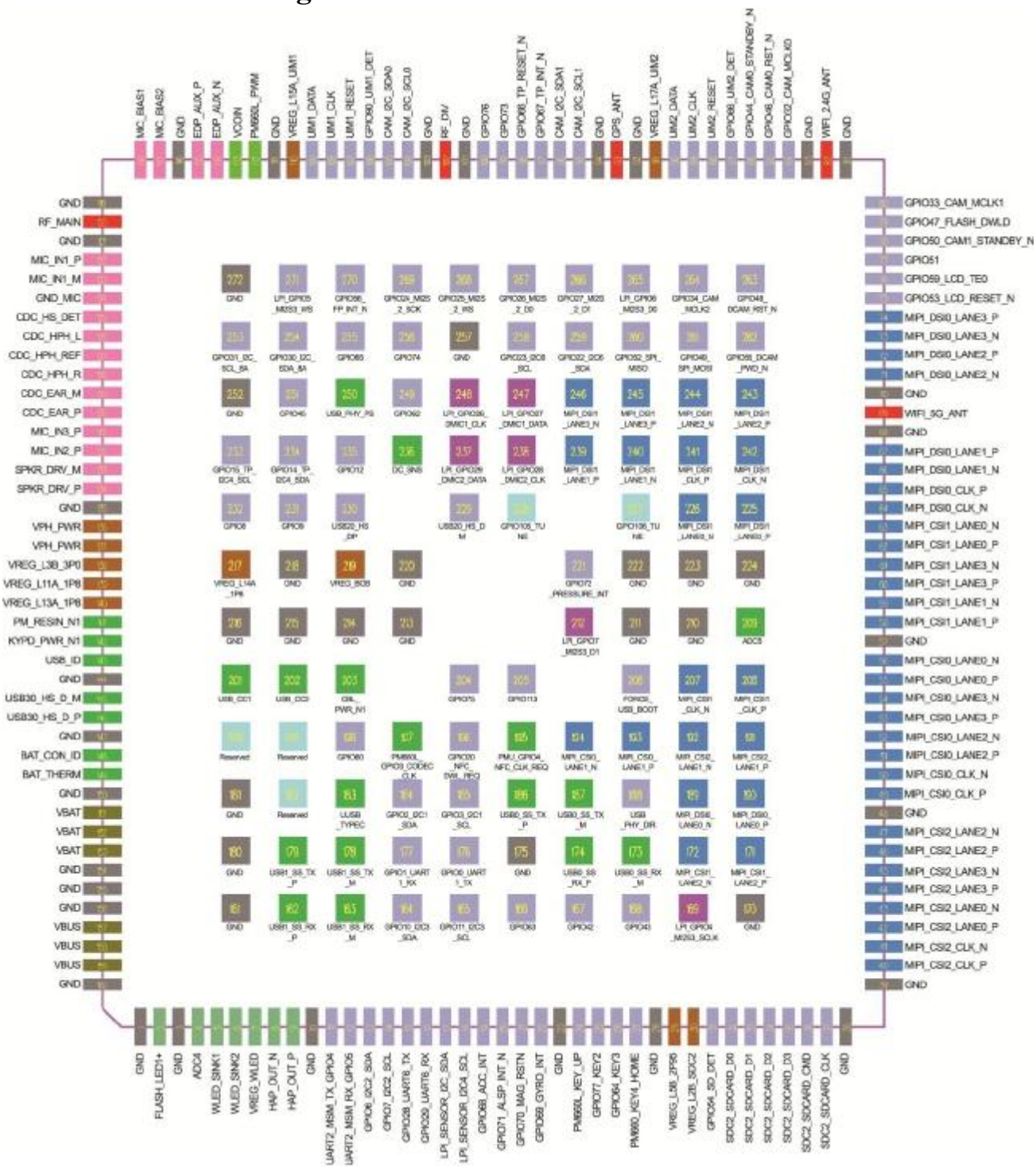


Figure 3.1： module pin diagram (top view)

3.2. Pin definitions

table 3.1： Pin description

Pin name	Pin number	I/O	Description	Comment
The power supply				
VBAT	151、152、153	I/O	The module provides three VBAT power pin pins. The SNM900 operates from a single supply with a voltage range from 3.5V to 4.35V for VBAT.	External capacitance and zener diode should be increased for surge protection
VBUS	157、158、159	I/O	5V charging input power.	
VCOIN	113	I/O	When the VBAT of the system power is absent, the external backup battery provides power to the system real-time clock.When VBAT is present, the backup battery is charged.	Connect 3V button battery or large capacitance to vcoin pin.
VREG_L13A_1P8	140	O	1.8V power output, always available for CPU, Memory, IO and other power supply.	100mA
VREG_L11A_1P8	139	O	1.8 V power output, standby will be closed, used for Camera, LCD and other small current power supply.	100mA
VREG_L3B_3P0	138	O	2.8V power output, will be turned off during standby, used for Sensor, TP power supply.	300mA
VPH_PWR	136、137	I/O	System power input / output, typical value 3.8V	External capacitance and zener diode should be increased for surge protection.
VREG_L5B_2P95	29	O	TF card power supply pin	600mA
VREG_L2B_SDC2	30	O	TF card signal pull-up power supply pin	50mA
VREG_L14A_1P8	217	O	1.8V power output, which will be turned off when standby, used as sensor I2C pull-up source	150mA
VREG_BOB	219	O	3.3V power output for external LDO power input	300mA
VREG_L15A_UIM1	110	O	UIM1 power supply pins	50mA
VREG_L17A_UIM2	91	O	UIM2 power supply pins	50mA
GND	1、3、10、23、28、38、39、48、57、68、70、81、83、		GND	

	92、94、101、103、111、116、119、121、135、144、147、150、154、155、156、160、161、170、175、180、181、210、211、213、214、215、216、218、220、222、223、224、252、257、272			
Main display interface(MIPI)				
MIPI_DSI0_CLK_N	64	O	MIPI_LCD clock	
MIPI_DSI0_CLK_P	65	O		
MIPI_DSI0_LANE0_N	189	O	MIPI_LCD data	
MIPI_DSI0_LANE0_P	190	O		
MIPI_DSI0_LANE1_N	66	O		
MIPI_DSI0_LANE1_P	67	O		
MIPI_DSI0_LANE3_N	73	O		
MIPI_DSI0_LANE3_P	74	O		
MIPI_DSI0_LANE2_N	71	O		
MIPI_DSI0_LANE2_P	72	O		
GPIO53_LCD_RESET_N	75	I/O	LCD reset	
GPIO59_LCD_TE0	76	I/O	LCD frame sync signal	
The main display backlight interface				
WLED_SINK1	5	I	LCD Series backlight negative	Each normal20mA ，max 30m
WLED_SINK2	6	I	LCD Series backlight negative	
VREG_WLED	7	O	LCD Series backlight positive	Maximum output 28V
Sub display interface (MIPI)				
MIPI_DSI1_CLK_N	242	O	MIPI_LCD2 clock	
MIPI_DSI1_CLK_P	241	O		
MIPI_DSI1_LANE0_N	226	O	MIPI_LCD2 data	
MIPI_DSI1_LANE0_P	225	O		
MIPI_DSI1_LANE1_N	240	O		

MIPI_DSI1_LANE1_P	239	O		
MIPI_DSI1_LANE2_N	244	O		
MIPI_DSI1_LANE2_P	243	O		
MIPI_DSI1_LANE3_N	246	O		
MIPI_DSI1_LANE3_P	245	O		
GPIO73	99	I/O	LCD2 reset	
GPIO51	77	I/O	LCD2 frame sync signal	
UART(1.8V)				
GPIO4_UART2_MSM_TX	11	O	UART data transmit	System debugging UART
GPIO5_UART2_MSM_RX	12	I	UART data receive	
GPIO29_UART_RX	16	I	UART data receive	
GPIO28_UART_TX	15	O	UART data transmit	
GPIO1_UART1_RX	177	I	UART data receive	
GPIO0_UART1_TX	176	O	UART data transmit	
UIM card Interface				
GPIO90_UIM1_DET	106	I	UIM1 insert detect	
UIM1_RESET	107	O	UIM1 reset	
UIM1_CLK	108	O	UIM1 clock	
UIM1_DATA	109	I/O	UIM1 data	
GPIO86_UIM2_DET	87	I	UIM2 insert detect	
UIM2_RESET	88	O	UIM2 reset	
UIM2_CLK	89	O	UIM2 clock	
UIM2_DATA	90	I/O	UIM2 data	
Front Camera				
MIPI_CSI2_CLK_P	40	O	Front Camera MIPI clock	
MIPI_CSI2_CLK_N	41	O		
MIPI_CSI2_LANE0_P	42	I	Front Camera MIPI data	
MIPI_CSI2_LANE0_N	43	I		
MIPI_CSI2_LANE1_P	191	I		
MIPI_CSI2_LANE1_N	192	I		
MIPI_CSI2_LANE2_P	46	I		
MIPI_CSI2_LANE2_N	47	I		
MIPI_CSI2_LANE3_P	44	I		
MIPI_CSI2_LANE3_N	45	I		
GPIO33_CAM_MCLK1	80	I/O	Front Camera main clock	

GPIO47_SCAM_RST_N	79	I/O	Front Camera reset	
GPIO50_SCAM_PWD_N	78	I/O	Front Camera dormancy	
Rear Camera				
MIPI_CSI0_CLK_N	50	O	Rear Camera MIPI clock	
MIPI_CSI0_CLK_P	49	O		
MIPI_CSI0_LANE0_N	56	I	Rear Camera MIPI data	
MIPI_CSI0_LANE0_P	55	I		
MIPI_CSI0_LANE1_N	194	I		
MIPI_CSI0_LANE1_P	193	I		
MIPI_CSI0_LANE2_N	52	I		
MIPI_CSI0_LANE2_P	51	I		
MIPI_CSI0_LANE3_N	54	I		
MIPI_CSI0_LANE3_P	53	I		
GPIO32_CAM_MCLK0	84	I/O	Rear Camera main clock	
GPIO46_CAM0_RST_N	85	I/O	Rear Camera reset	
GPIO44_CAM0_STANDBY_N	86	I/O	Rear Camera dormancy	
Depth Camera				
MIPI_CSI1_CLK_N	207	O	Depth Camera clock	
MIPI_CSI1_CLK_P	208	O		
MIPI_CSI1_LANE0_N	63	I	Depth Camera MIPI data	
MIPI_CSI1_LANE0_P	62	I		
MIPI_CSI1_LANE1_N	59	I		
MIPI_CSI1_LANE1_P	58	I		
MIPI_CSI1_LANE2_N	172	I		
MIPI_CSI1_LANE2_P	171	I		
MIPI_CSI1_LANE3_N	61	I		
MIPI_CSI1_LANE3_P	60	I		
GPIO55_DCAM_PWD_N	262	I/O	Depth Camera dormancy	
GPIO48_DCAM_RST_N	263	I/O	Depth Camera reset	
GPIO34_CAM_MCLK2	264	I/O	Depth Camera main clock	
Audio Interface				
MIC_IN1_M	123	I	The main MIC negative	
MIC_IN1_P	122	I	The main MIC positive	
MIC_IN2_P	132	I	Headphone MIC positive	
GND_MIC	124	I	Headphone Mic、Noise	

			reduction MIC negative	
MIC_IN3_P	131	I	Noise reduction MIC positive	
MIC_BIAS1	118	O	The BIAS voltage of main MIC is used in the design of silicon wheat	
MIC_BIAS2	117	O	The BIAS voltage of the earphone MIC is used in the design of silicon wheat	
CDC_HPH_R	128	O	Right channel of earphone	
CDC_HPH_L	126	O	Left channel of earphone	
CDC_HS_DET	125	I	Headphone plug and unplug detection	
CDC_HPH_REF	127	I	Earphone reference GND	
CDC_EAR_M	129	O	Earpiece output negative	
CDC_EAR_P	130	O	Earpiece output positive	
SPKR_DRV_M	133	O	Power amplifier (0.8 W) output negative	Class_D
SPKR_DRV_P	134	O	Power amplifier(0.85W) output positive	
LPI_GPIO29_DMIC2_DATA	237	I	Digital mic clock signal	Cannot be used as a normal GPIO
LPI_GPIO28_DMIC2_CLK	238	O	Digital mic clock signal	
LPI_GPIO27_DMIC1_DATA	247	I	Digital mic clock signal	
LPI_GPIO26_DMIC1_CLK	248	O	Digital mic clock signal	
SD car d Interface				
GPIO54_SDCARD_DET_N	31	I/O	SD card insertion detection	
SDC2_SDCARD_CMD	36	I/O	SD CMD	
SDC2_SDCARD_CLK	37	I/O	SD clock	
SDC2_SDCARD_D0	32	I/O	SD data	
SDC2_SDCARD_D1	33	I/O		
SDC2_SDCARD_D2	34	I/O		
SDC2_SDCARD_D3	35	I/O		
I2C				
CAM_I2C_SDA0	105	I/O	Special I2C signal can only be used for CAM	Pullup to VREG_L11A_1P
CAM_I2C_SCL0	104	I/O		
CAM_I2C_SDA1	96	I/O	Special I2C signal can only be used 8 for CAM	
CAM_I2C_SCL1	95	I/O		
LPI_SENSOR_I2C_SDA	17	I/O	Special I2C signal can only be used for SENSOR	Pullup to VREG_L14A_1P 8
LPI_SENSOR_I2C_SCL	18	I/O		
GPIO10_I2C3_SDA	164	I/O	Universal I2C signal	Pullup to VREG_L13A_1P 8
GPIO11_I2C3_SCL	165	I/O		

GPIO6_I2C2_SDA	13	I/O	Universal I2C signal	
GPIO7_I2C2_SCL	14	I/O		
GPIO2_I2C1_SDA	184	I/O	Universal I2C signal	
GPIO3_I2C1_SCL	185	I/O		
GPIO30_I2C_SDA_8A	254	I/O	Universal I2C signal	
GPIO31_I2C_SCL_8A	253	I/O		
TP				
GPIO14_TP_I2C4_SDA	234	I/O	I2C data	Pullup to VREG_L11A_1P8
GPIO15_TP_I2C4_SCL	233	I/O	I2C clock	
GPIO67_TP_INT_N	97	I/O	TP interrupt	
GPIO66_TP_RST_N	98	I/O	TP reset	
USB				
USB30_HS_DM	145	I/O	USB 3.0 DM	
USB30_HS_DP	146	I/O	USB 3.0 DP	
USB0_SS_TX_P	186	O	USB super-speed 0 transmit – plus	
USB0_SS_TX_M	187	O	USB super-speed 0 transmit – minus	
USB1_SS_TX_M	178	O	USB super-speed 1 transmit – minus	
USB1_SS_TX_P	179	O	USB super-speed 1 transmit – plus	
USB0_SS_RX_M	173	I	USB super-speed 0 receive – minus	
USB0_SS_RX_P	174	I	USB super-speed 0 receive – plus	
USB1_SS_RX_P	162	I	USB super-speed 1 receive – plus	
USB1_SS_RX_M	163	I	USB super-speed 1 receive – minus	
USB_CC1	201	I/O	USB type C connector configuration channel2	
USB_CC2	202	I/O	USB type C connector configuration channel2	
USB_ID	143	I	USB ID	
USB20_HS_DM	229	I/O	USB 2.0 DM	
USB20_HS_DP	230	I/O	USB 2.0 DP	
Antenna interface				
RF_MAIN	120	I/O	The main antenna	
WIFI_2.4G_ANT	82	I/O	WIFI/BT antenna	
RF_DIV	102	I	Diversity antenna	
GPS_ANT	93	I	GPS antenna	
WIFI_5G_ANT	69	I/O	5GWIFI antenna	
GPIO and default function				

GPIO49_SPI_MOSI	261	I/O	The default configuration is the SPI interface	
GPIO52_SPI_MISO	260	I/O		
GPIO22_I2C6_SDA	259	I/O		
GPIO23_I2C6_SCL	258	I/O		
GPIO8	232	I/O	Generic GPIO, without default configuration	
GPIO65	255	I/O	Generic GPIO, without default configuration	
GPIO74	256	I/O	Generic GPIO, without default configuration	
GPIO9	231	I/O	Generic GPIO, without default configuration	
GPIO63	166	I/O	Generic GPIO, without default configuration	
GPIO42	167	I/O	Generic GPIO, without default configuration	
GPIO43	168	I/O	Generic GPIO, without default configuration	
GPIO45	251	I/O	Generic GPIO, without default configuration	
GPIO68_ACCL_INT1	19	I/O	The default configuration is G-sensor interrupt	
GPIO71_ALSP_INT_N	20	I/O	The default configuration is Ps-sensor interrupt signal	
GPIO70_MAG_INT	21	I/O	The default configuration is the compass interrupt signal.	
GPIO69_GYRO_INT	22	I/O	The default configuration is the gyroscope interrupt signal.	
GPIO72_PRESSURE_INT	221	I/O	The default configuration is the pressure sensor interrupt signal	
GPIO12	235	I/O	Generic GPIO, without default configuration	
GPIO56_FP_INT_N	270	I/O	The default configuration is the interrupt signal for fingerprint recognition.	
GPIO76	100	I/O	General purpose GPIO, no default configuration	
GPIO73	99	I/O	General purpose GPIO, no default configuration	
LPI_GPIO6_MI2S3_D0	265	I/O	Output signal configured as IIS	Cannot be used as a normal GPIO
LPI_GPIO7_MI2S3_D1	212	I/O	Input signal configured as IIS	
LPI_GPIO4_MI2S3_SCLK	169	I/O	Clock signal configured as IIS	
LPI_GPIO5_MI2S3_WS	271	I/O	Channel selection signal configured as IIS	
GPIO77_KEY2	25	I/O	The default configuration is volume-	
GPIO64_KEY3	26	I/O	The default configuration is key	
GPIO60	198	I/O	Generic GPIO, without default configuration	

GPIO75	204	I/O	Generic GPIO, without default configuration	
GPIO20_NFC_DWL_REQ	196	I/O	Generic GPIO, without default configuration	
GPIO106_TUNE	227	I/O	Configure as RF tune enable	
GPIO105_TUNE	228/	I/O	Configure as RF tune enable	
GPIO113	205	I/O	Generic GPIO, without default configuration	
PMU_GPIO4_NFC_CLK_REQ	195	I/O	PMU can be configured with GPIO without default configuration	
PM660L_GPIO3_CODEC_CLK	197	I/O	PMU can be configured with GPIO without default configuration	
GPIO62	249	I/O	Generic GPIO, without default configuration	
GPIO27_MI2S_2_D1	266	I	The default configuration is I2S interface	
GPIO26_MI2S_2_D0	267	O		
GPIO25_MI2S_2_WS	268	O		
GPIO24_MI2S_2_SCK	269	O		
Other functional pin				
FORCE_USB_BOOT	206	I	Pull up to 1.8 V (VREG_L5_1P8) into the emergency download mode	
FLASH_LED1+	2	O	Flash light positive,1.5A output	
RESERVED	182、199、200		NC pin	
HAP_OUT_N	8	O	motor output negative	
HAP_OUT_P	9	O	motor output positive	
BAT_THERM	149	I	Battery temperature detection, the battery NTC terminal (battery terminal NTC resistance is 10K), such as no battery temperature detection requirement, need to increase 10K resistance to GND.	
ADC4	4	I	Analog voltage input, can be used as ADC input	
PM660L_PWM	112	O	It can be used as PWM output	
ADC5	209	I	Analog voltage input, can be used as ADC input	
KYPD_PWR_N1	142	I	Power key	
PM_RESIN_N1	141	I	Reset key, android device for volume reduction	
USB_PHY_PS	250	O	Type-c or Micro USB switch	
USB_PHY_DIR	188	I	Type-c or Micro USB switch	

UUSB_TYPEC	183	I	Type-c or Micro USB switch	
EDP_AUX_N	114	O	DP interface auxiliary channel-	
EDP_AUX_P	115	O	DP interface auxiliary channel+	
CBL_PWR_N1	203	I	Power on control pin	
DC_SNS	236	I	DC power insertion detection	
PM660_KEY4_HOME	27	I	Home key	
PM660L_KEY_UP	24	I	Control volume+	
BAT_CON_ID	148	I	Battery ID detection	

Table 3.2：Pin Characteristics

PIN #	SNM900 Pin name	GPIO Interrupt	Pad characteristics	Functional description
1	GND		GND	GND
2	FLASH_LED1+		AO	FLASH LED anode(1.5A)
3	GND		GND	GND
4	ADC4		AI	Configurable ADC
5	WLED_SINK1		AI	LCD Backlight cathode1(20mA)
6	WLED_SINK2		AI	LCD Backlight cathode2(20mA)
7	VREG_WLED		AO	LCD Backlight anode
8	HAP_OUT_N		AO	Haptics driver output negative
9	HAP_OUT_P		AO	Haptics driver output positive
10	GND		GND	GND
11	UART2_MSM_TX_GPIO4	GPIO4	B-PD:nppukp	Configurable I/O,UART2 TX
12	UART2_MSM_RX_GPIO5	GPIO5*	B-PD:nppukp	Configurable I/O,UART2 RX
13	GPIO6_I2C2_SDA	GPIO6*	B-PD:nppukp	Configurable I/O, I2C SDA
14	GPIO7_I2C2_SCL	GPIO7	B-PD:nppukp	Configurable I/O, I2C SCL
15	GPIO28_UART6_TX	GPIO28*	B-PD:nppukp	Configurable I/O,UART6 TX
16	GPIO29_UART6_RX	GPIO29*	B-PD:nppukp	Configurable I/O,UART6 RX
17	LPI_SENSOR_I2C_SDA	LPI_GPIO2	B-PD:nppukp	Configurable SENSOR I2C SDA
18	LPI_SENSOR_I2C4_SCL	LPI_GPIO3	B-PD:nppukp	Configurable SENSOR I2C SCL
19	GPIO68_ACC_INT	GPIO68*	B-PD:nppukp	Configurable I/O,ACC INT
20	GPIO71_ALSP_INT_N	GPIO71*	B-PD:nppukp	Configurable I/O,ALSP INT
21	GPIO70_MAG_RSTN	GPIO70*	B-PD:nppukp	Configurable I/O,MAG INT
22	GPIO69_GYRO_INT	GPIO69*	B-PD:nppukp	Configurable I/O,GYRO INT
23	GND		GND	GND

24	PM660L_KEY_UP		B-PD:nppukp	Configurable KEY VOL+
25	GPIO77_KEY2	GPIO77*	B-PD:nppukp	Configurable I/O,KEY VOL-
26	GPIO64_KEY3	GPIO64*	B-PD:nppukp	Configurable I/O,KEY
27	PM660_KEY4_HOME		B-PD:nppukp	Configurable I/O,KEY HOME
28	GND		GND	GND
29	VREG_L5B_2P95		PO	PMIC output 2.95V for SD-card power
30	VREG_L2B_SDC2		PO	PMIC output 2.95V for SDC2 signal
31	GPIO54_SD_DET	GPIO54*	B-PD:nppukp	Configurable I/O,SD card detection
32	SDC2_SDCARD_D0		BH-NP:pdpukp	Secure digital controller 2 data bit 0
33	SDC2_SDCARD_D1		BH-NP:pdpukp	Secure digital controller 2 data bit 1
34	SDC2_SDCARD_D2		BH-NP:pdpukp	Secure digital controller 2 data bit 2
35	SDC2_SDCARD_D3		BH-NP:pdpukp	Secure digital controller 2 data bit 3
36	SDC2_SDCARD_CMD		BH-NP:pdpukp	Secure digital controller 2 command
37	SDC2_SDCARD_CLK		BH-NP:pdpukp	Secure digital controller 2 clock
38	GND		GND	GND
39	GND		GND	GND
40	MIPI_CSI2_CLK_P		AI	MIPI camera serial interface 2 clock+
41	MIPI_CSI2_CLK_N		AI	MIPI camera serial interface 2 clock-
42	MIPI_CSI2_LANE0_P		AI	MIPI camera serial interface 2 lane0+
43	MIPI_CSI2_LANE0_N		AI	MIPI camera serial interface 2 lane0-
44	MIPI_CSI2_LANE3_P		AI	MIPI camera serial interface 2 lane3+
45	MIPI_CSI2_LANE3_N		AI	MIPI camera serial interface 2 lane3-
46	MIPI_CSI2_LANE2_P		AI	MIPI camera serial interface 2 lane2+
47	MIPI_CSI2_LANE2_N		AI	MIPI camera serial interface 2 lane2-
48	GND		GND	GND
49	MIPI_CSI0_CLK_P		AI	MIPI camera serial interface 0 clock+
50	MIPI_CSI0_CLK_N		AI	MIPI camera serial interface 0 clock-
51	MIPI_CSI0_LANE2_P		AI	MIPI camera serial interface 0 lane2+
52	MIPI_CSI0_LANE2_N		AI	MIPI camera serial interface 0 lane2-
53	MIPI_CSI0_LANE3_P		AI	MIPI camera serial interface 0 lane3+
54	MIPI_CSI0_LANE3_N		AI	MIPI camera serial interface 0 lane3-
55	MIPI_CSI0_LANE0_P		AI	MIPI camera serial interface 0 lane0+
56	MIPI_CSI0_LANE0_N		AI	MIPI camera serial interface 0 lane0-

57	GND		GND	GND
58	MIPI_CSI1_LANE1_P		AI	MIPI camera serial interface 1 lane1+
59	MIPI_CSI1_LANE1_N		AI	MIPI camera serial interface 1 lane1-
60	MIPI_CSI1_LANE3_P		AI	MIPI camera serial interface 1 lane3+
61	MIPI_CSI1_LANE3_N		AI	MIPI camera serial interface 1 lane3-
62	MIPI_CSI1_LANE0_P		AI	MIPI camera serial interface 1 lane0+
63	MIPI_CSI1_LANE0_N		AI	MIPI camera serial interface 1 lane0-
64	MIPI_DSI0_CLK_N		AO	MIPI display serial interface 0 clock-
65	MIPI_DSI0_CLK_P		AO	MIPI display serial interface 0 clock+
66	MIPI_DSI0_LANE1_N		AO	MIPI display serial interface 0 lane1-
67	MIPI_DSI0_LANE1_P		AO	MIPI display serial interface 0 lane1+
68	GND		GND	GND
69	WIFI_5G_ANT		AI	RF signal for 5G WIFI
70	GND		GND	GND
71	MIPI_DSI0_LANE2_N		AO	MIPI display serial interface 0 lane2-
72	MIPI_DSI0_LANE2_P		AO	MIPI display serial interface 0 lane2+
73	MIPI_DSI0_LANE3_N		AO	MIPI display serial interface 0 lane3-
74	MIPI_DSI0_LANE3_P		AO	MIPI display serial interface 0 lane3+
75	GPIO53_LCD_RESET_N	GPIO53	B-PD:nppukp	Configurable I/O, primary LCD RESET
76	GPIO59_LCD_TE0	GPIO59	B-PD:nppukp	Configurable I/O, primary LCD TE
77	GPIO51	GPIO51	B-PD:nppukp	Configurable I/O, secondary LCD TE
78	GPIO50_CAM1_STANDBY_N	GPIO50*	B-PD:nppukp	Configurable I/O, front CAM PWDN
79	GPIO47_FLASH_DWLD	GPIO47*	B-PD:nppukp	Configurable I/O, front CAM RESET
80	GPIO33_CAM_MCLK1	GPIO33	B-PD:nppukp	Configurable I/O, front CAM MCLK
81	GND		GND	GND
82	WIFI_2.4G_ANT		AI	RF signal for 2.4G WIFI&BT
83	GND		GND	GND
84	GPIO32_CAM_MCLK0	GPIO32	B-PD:nppukp	Configurable I/O, main CAM MCLK
85	GPIO46_CAM0_RST_N	GPIO46*	B-PD:nppukp	Configurable I/O, main CAM RESET
86	GPIO44_CAM0_STANDBY_N	GPIO44*	B-PD:nppukp	Configurable I/O, main CAM PWDN
87	GPIO86_UIM2_DET	GPIO86*	B-PD:nppukp	Configurable I/O,UIM2 removal detection
88	UIM2_RESET	GPIO85*	B-PD:nppukp	Configurable I/O,UIM2 reset
89	UIM2_CLK	GPIO84*	B-PD:nppukp	Configurable I/O,UIM2 clock
90	UIM2_DATA	GPIO83*	B-PD:nppukp	Configurable I/O,UIM2 data

91	VREG_L17A_UIM2		PO	PMIC output for UIM2
92	GND		GND	GND
93	GPS_ANT		AI	RF signal for GPS ANT
94	GND		GND	GND
95	CAM_I2C_SCL1	GPIO39	B-PD:nppukp	Configurable I/O, Dedicated camera I2C1 SCL
96	CAM_I2C_SDA1	GPIO38	B-PD:nppukp	Configurable I/O, Dedicated camera I2C1 SDA
97	GPIO67_TP_INT_N	GPIO67*	B-PD:nppukp	Configurable I/O,TP INT
98	GPIO66_TP_RESET_N	GPIO66*	B-PD:nppukp	Configurable I/O,TP RESET
99	GPIO73	GPIO73*	B-PD:nppukp	Configurable I/O,
100	GPIO76	GPIO76*	B-PD:nppukp	Configurable I/O,
101	GND		GND	GND
102	RF_DIV		AI	RF signal for diversity ANT
103	GND		GND	GND
104	CAM_I2C_SCL0	GPIO37	B-PD:nppukp	Configurable I/O, Dedicated camera I2C0 SCL
105	CAM_I2C_SDA0	GPIO36	B-PD:nppukp	Configurable I/O, Dedicated camera I2C0 SDA
106	GPIO90_UIM1_DET	GPIO90*	B-PD:nppukp	Configurable I/O,UIM1 removal detection
107	UIM1_RESET	GPIO89	B-PD:nppukp	Configurable I/O,UIM1 reset
108	UIM1_CLK	GPIO88	B-PD:nppukp	Configurable I/O,UIM1 clock
109	UIM1_DATA	GPIO87*	B-PD:nppukp	Configurable I/O,UIM1 data
110	VREG_L15A_UIM1		PO	PMIC output for UIM1
111	GND		GND	GND
112	PM660L_PWM		AO-Z,DI,DO	Configurable PWM
113	VCOIN		AI,AO	Coin-cell battery or backup battery
114	EDP_AUX_N		AO	DisplayPort auxiliary channel – negative
115	EDP_AUX_P		AO	DisplayPort auxiliary channel – positive
116	GND		GND	GND
117	MIC_BIAS2		AO	Microphone bias #2
118	MIC_BIAS1		AO	Microphone bias #1
119	GND		GND	GND
120	RF_MAIN		AI	RF signal for main ANT
121	GND		GND	GND
122	MIC_IN1_P		AI	Microphone 1 input plus
123	MIC_IN1_M		AI	Microphone 1 input minus

124	GND_MIC		GND	Microphone bias filter ground
125	CDC_HS_DET		AI	MBHC mechanical insertion/removal-detection
126	CDC_HPH_L		AO	Headphone output, left channel
127	CDC_HPH_REF		AI	Headphone ground reference
128	CDC_HPH_R		AO	Headphone output, right channel
129	CDC_EAR_M		AO	Earpiece output, minus
130	CDC_EAR_P		AO	Earpiece output, plus
131	MIC_IN3_P		AI	Microphone input 3
132	MIC_IN2_P		AI	Microphone input 2
133	SPKR_DRV_M		AO	Class-D speaker driver output, minus
134	SPKR_DRV_P		AO	Class-D speaker driver output, plus
135	GND		GND	GND
136	VPH_PWR		PO	System Power input/output
137				
138	VREG_L3B_3P0		PO	PMIC output 2.8V for sensor
139	VREG_L11A_1P8		PO	PMIC output 1.8V for LCD,CAM,TP, sensor
140	VREG_L13A_1P8		PO	PMIC output 1.8V for digital I/Os
141	PM_RESIN_N1		DI	KEY RESET or VOL-
142	KYPD_PWR_N1		DI	KEY POWER ON/OFF
143	USB_ID		AI	USB ID
144	GND		GND	GND
145	USB30_HS_D_M		AI,AO	USB3.0 data minus
146	USB30_HS_D_P		AI,AO	USB3.0 data plus
147	GND		GND	GND
148	BAT_CON_ID		AI	Battery ID input to ADC
149	BAT_THERM		AI	Battery temperature input to ADC
150	GND		GND	GND
151	VBAT		PI,PO	Battery,3.5V-4.35V,default 3.8V
152				
153				
154	GND		GND	GND
155	GND		GND	GND
156	GND		GND	GND
157	VBUS		PI,PO	USB Voltage

158				
159				
160	GND		GND	GND
161	GND		GND	GND
162	USB1_SS_RX_P		AI	USB super-speed 1 receive – plus
163	USB1_SS_RX_M		AI	USB super-speed 1 receive – minus
164	GPIO10_I2C3_SDA	GPIO10*	B-PD:nppukp	Configurable I/O, I2C SDA
165	GPIO11_I2C3_SCL	GPIO11	B-PD:nppukp	Configurable I/O, I2C SCL
166	GPIO63	GPIO63	B-PD:nppukp	Configurable I/O
167	GPIO42	GPIO42*	B-PD:nppukp	Configurable I/O
168	GPIO43	GPIO43*	B-PD:nppukp	Configurable I/O
169	LPI_GPIO4_MI2S3_SCLK	LPI_GPIO4	B-PD:nppukp	Configurable I/O,MI2S1_SCK
170	GND		GND	GND
171	MIPI_CSI1_LANE2_P		AI	MIPI camera serial interface 1 lane2+
172	MIPI_CSI1_LANE2_N		AI	MIPI camera serial interface 1 lane2-
173	USB0_SS_RX_M		AI	USB super-speed 0 receive – minus
174	USB0_SS_RX_P		AI	USB super-speed 0 receive – plus
175	GND		GND	GND
176	GPIO0_UART1_TX	GPIO0*	B-PD:nppukp	Configurable I/O,UART1 TX
177	GPIO1_UART1_RX	GPIO1*	B-PD:nppukp	Configurable I/O,UART1 RX
178	USB1_SS_TX_M		AO	USB super-speed 1 transmit – minus
179	USB1_SS_TX_P		AO	USB super-speed 1 transmit – plus
180	GND		GND	GND
181	GND		GND	GND
182	Reserved			Reserved
183	UUSB_TYPEC		B-PD:nppukp	Type-c or Micro select
184	GPIO2_I2C1_SDA	GPIO2	B-PD:nppukp	Configurable I/O, I2C SDA
185	GPIO3_I2C1_SCL	GPIO3	B-PD:nppukp	Configurable I/O, I2C SCL
186	USB0_SS_TX_P		AO	USB super-speed 0 transmit – plus
187	USB0_SS_TX_M		AO	USB super-speed 0 transmit – minus
188	USB_PHY_DIR	GPIO58*	B-PD:nppukp	Configurable I/O,Type-c or Micro select
189	MIPI_DSI0_LANE0_N		AO	MIPI display serial interface 0 lane0-
190	MIPI_DSI0_LANE0_P		AO	MIPI display serial interface 0 lane0+
191	MIPI_CSI2_LANE1_P		AI	MIPI camera serial interface 2 lane1+
192	MIPI_CSI2_LANE1_N		AI	MIPI camera serial interface 2 lane1-

193	MIPI_CSI0_LANE1_P		AI	MIPI camera serial interface 0 lane1+
194	MIPI_CSI0_LANE1_N		AI	MIPI camera serial interface 0 lane1-
195	PMU_GPIO4_NFC_CLK_REQ		B-PD:nppukp	PMU Configurable I/O
196	GPIO20_NFC_DWL_REQ	GPIO20	B-PD:nppukp	Configurable I/O
197	PM660L_GPIO3_CODEC_CLK		B-PD:nppukp	PMU Configurable I/O
198	GPIO60	GPIO60*	B-PD:nppukp	Configurable I/O
199	Reserved			Reserved
200	Reserved			Reserved
201	USB_CC1		AI;AO	USB type C connector configuration channel1
202	USB_CC2		AI;AO	USB type C connector configuration channel2
203	CBL_PWR_N1		DI	Cable power-on
204	GPIO75	GPIO75*	B-PD:nppukp	Configurable I/O
205	GPIO113	GPIO113*	B-PD:nppukp	Configurable I/O
206	FORCE_USB_BOOT	GPIO57	DI	pullup with VREG_L5 to forced USB boot
207	MIPI_CSI1_CLK_N		AI	MIPI camera serial interface 1 clock-
208	MIPI_CSI1_CLK_P		AI	MIPI camera serial interface 1 clock-
209	ADC5		AI	Configurable ADC
210	GND		GND	GND
211	GND		GND	GND
212	LPI_GPIO7_MI2S3_D1	LPI_GPIO7	B-PD:nppukp	Configurable I/O,MI2S3_D1
213	GND		GND	GND
214	GND		GND	GND
215	GND		GND	GND
216	GND		GND	GND
217	VREG_L14A_1P8		PO	PMIC output 1.8V
218	GND		GND	GND
219	VREG_BOB		PO	PMIC output 3.3V
220	GND		GND	GND
221	GPIO72_PRESSURE_INT	GPIO72*	B-PD:nppukp	Configurable I/O, Pressure INT
222	GND		GND	GND
223	GND		GND	GND
224	GND		GND	GND
225	MIPI_DSI1_LANE0_P		AO	MIPI display serial interface 1 lane0+
226	MIPI_DSI1_LANE0_N		AO	MIPI display serial interface 1 lane0-

227	GPIO106_TUNE	GPIO106	B-PD:nppukp	Configurable I/O for RF tune EN
228	GPIO105_TUNE	GPIO105	B-PD:nppukp	Configurable I/O for RF tune EN
229	USB20_HS_DM		B-PD:nppukp	USB2.0 data minus
230	USB20_HS_DP		B-PD:nppukp	USB2.0 data plus
231	GPIO9	GPIO9*	B-PD:nppukp	Configurable I/O,
232	GPIO8	GPIO8	B-PD:nppukp	Configurable I/O,
233	GPIO15_TP_I2C4_SCL	GPIO15	B-PD:nppukp	Configurable I/O, CTP I2C SCL
234	GPIO14_TP_I2C4_SDA	GPIO14	B-PD:nppukp	Configurable I/O, CTP I2C SDA
235	GPIO12	GPIO12	B-PD:nppukp	Configurable I/O,
236	DC_SNS		AI	DC IN SENSE
237	LPI_GPIO29_DMIC2_DATA	LPI_GPIO29	B-PD:nppukp	Configurable LPI I/O, Digital MIC2 data
238	LPI_GPIO28_DMIC2_CLK	LPI_GPIO28	B-PD:nppukp	Configurable LPI I/O, Digital MIC2 clk
239	MIPI_DSI1_LANE1_P		AO	MIPI display serial interface 1 lane1+
240	MIPI_DSI1_LANE1_N		AO	MIPI display serial interface 1 lane1-
241	MIPI_DSI1_CLK_P		AO	MIPI display serial interface 1 clock+
242	MIPI_DSI1_CLK_N		AO	MIPI display serial interface 1 clock-
243	MIPI_DSI1_LANE2_P		AO	MIPI display serial interface 1 lane2+
244	MIPI_DSI1_LANE2_N		AO	MIPI display serial interface 1 lane2-
245	MIPI_DSI1_LANE3_P		AO	MIPI display serial interface 1 lane3+
246	MIPI_DSI1_LANE3_N		AO	MIPI display serial interface 1 lane3-
247	LPI_GPIO27_DMIC1_DATA	LPI_GPIO27	B-PD:nppukp	Configurable LPI I/O, Digital MIC1 data
248	LPI_GPIO26_DMIC1_CLK	LPI_GPIO26	B-PD:nppukp	Configurable LPI I/O, Digital MIC1 clk
249	GPIO62	GPIO62	B-PD:nppukp	Configurable I/O,
250	USB_PHY_PS		AO	Type-c or Micro select
251	GPIO45	GPIO45*	B-PD:nppukp	Configurable I/O,
252	GND		GND	GND
253	GPIO31_I2C_SCL_8A	GPIO31*	B-PD:nppukp	Configurable I/O,NFC I2C SCL
254	GPIO30_I2C_SDA_8A	GPIO30*	B-PD:nppukp	Configurable I/O, NFC I2C SDA
255	GPIO65	GPIO65*	B-PD:nppukp	Configurable I/O
256	GPIO74	GPIO74*	B-PD:nppukp	Configurable I/O
257	GND		GND	GND
258	GPIO23_I2C6_SCL	GPIO23	B-PD:nppukp	Configurable I/O, I2C,SPI CLK
259	GPIO22_I2C6_SDA	GPIO22*	B-PD:nppukp	Configurable I/O, I2C,SPI CS
260	GPIO52_SPI_MISO	GPIO52*	B-PD:nppukp	Configurable I/O, SPI MISO

261	GPIO49_SPI_MOSI	GPIO49*	B-PD:nppukp	Configurable I/O, SPI MOSI
262	GPIO55_DCAM_PWD_N	GPIO55*	B-PD:nppukp	Configurable I/O, Depth camera pwdn
263	GPIO48_DCAM_RST_N	GPIO48*	B-PD:nppukp	Configurable I/O, Depth camera reset
264	GPIO34_CAM_MCLK2	GPIO34	B-PD:nppukp	Configurable I/O, Depth camera MCLK
265	LPI_GPIO6_MI2S3_D0	LPI_GPIO6	B-PD:nppukp	Configurable LPI I/O, MI2S3_D0
266	GPIO27_MI2S_2_D1	GPIO27	B-PD:nppukp	Configurable I/O, fingerprint SPI MISO,MI2S2_D1
267	GPIO26_MI2S_2_D0	GPIO26	B-PD:nppukp	Configurable I/O, fingerprint SPI CLK,MI2S2_D0
268	GPIO25_MI2S_2_WS	GPIO25*	B-PD:nppukp	Configurable I/O, fingerprint SPI MISO,MI2S2_CS
269	GPIO24_MI2S_2_SCK	GPIO24	B-PD:nppukp	Configurable I/O, fingerprint SPI MOSI,MI2S2_CK
270	GPIO56_FP_INT_N	GPIO56*	B-PD:nppukp	Configurable I/O, fingerprint INT
271	LPI_GPIO5_MI2S3_WS	LPI_GPIO5	B-PD:nppukp	Configurable LPI I/O, MI2S3_WS
272	GND		GND	GND

*: Wake-up system interrupt pin

B: Bidirectionaldigital with CMOS input

H: High-voltage tolerant

NP: pdpukp=defaultno-pull with programmable options following the colon (:)

PD: nppukp=defaultpulldown with programmable options following the colon (:)

PU: nppdkp=defaultpullup with programmable options following the colon (:)

KP: nppdpu=defaultkeeper with programmable options following the colon (:)

3.3. Mechanical Dimensions

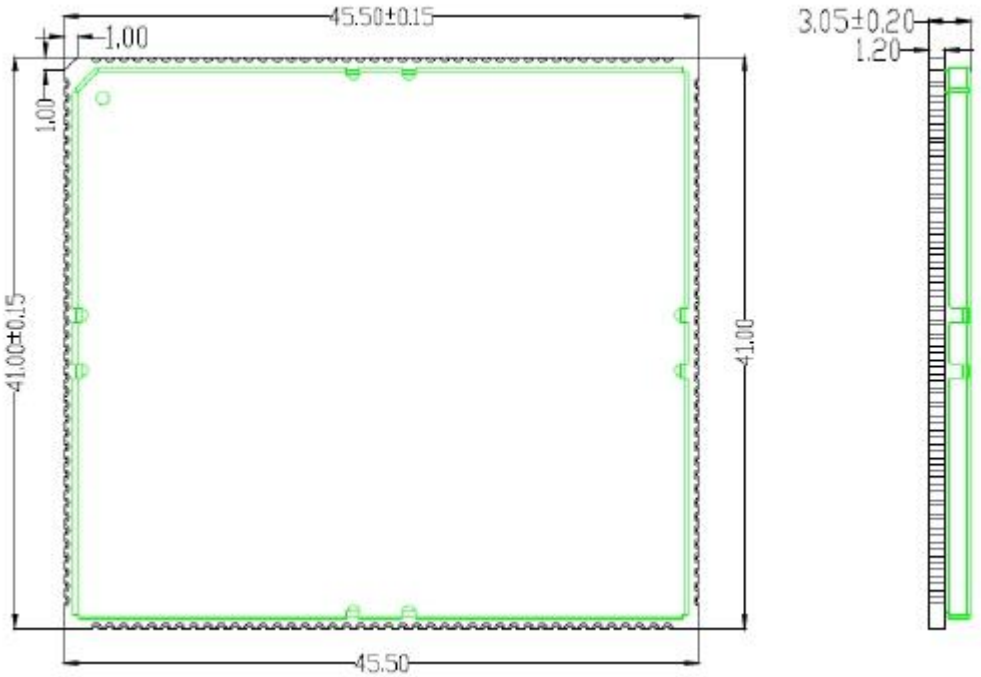


Figure 3.2：TOP View & Side View

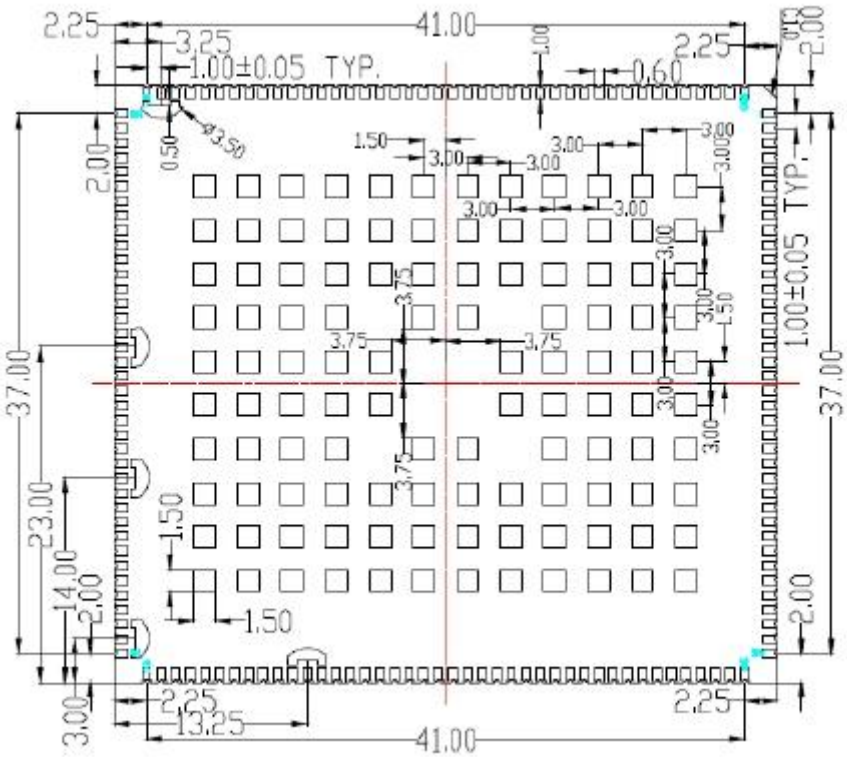


Figure 3.3：BOTTOM View

z

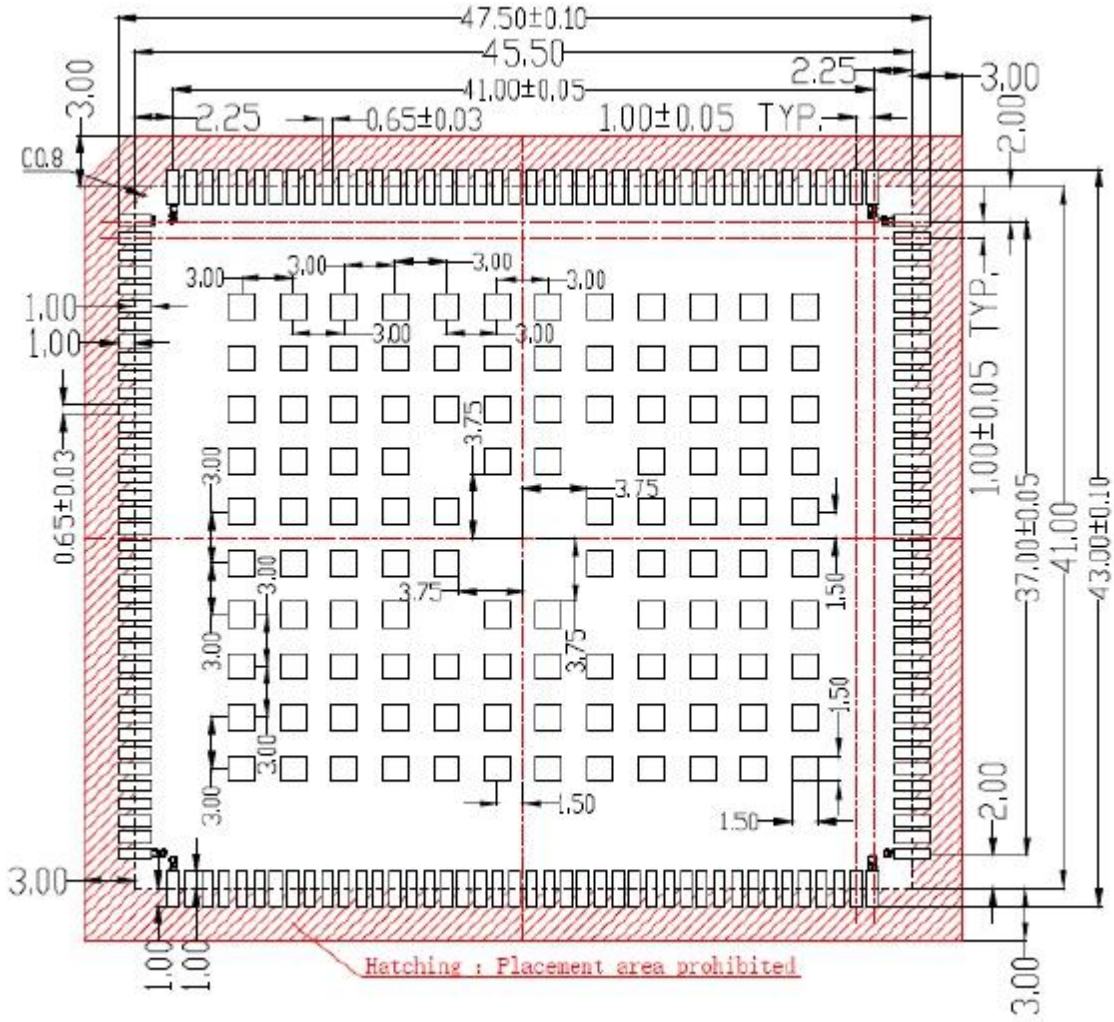


Figure 3.4: recommended encapsulation

4. Interface application

4.1. Power Supply

In the case of a battery device, the voltage input range of the module VBAT is 3.5V to 4.35V, and the recommended voltage is 3.8V.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to use a suitable TVS tube and a 5.6V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.8V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

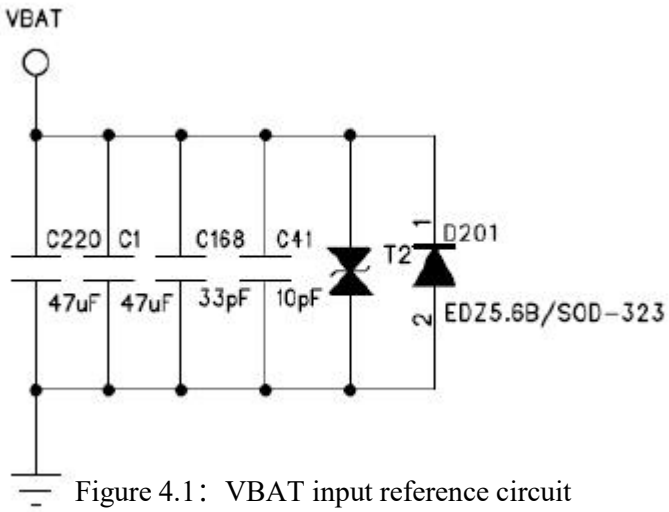


Figure 4.1： VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 5V-12V. The recommended circuit that can be powered by DC-DC is shown below:

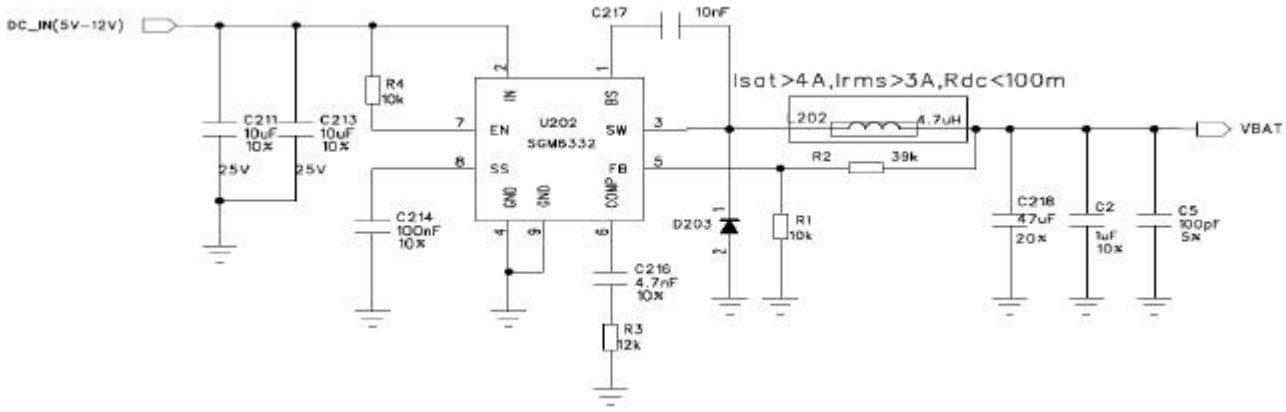


Figure 4.2：DC-DC power supply circuit

NOTE：If the user does not use battery power,please note that a 10K resistor is connected to the 149 pin(BAT_THERM) of the module and pulled down to GND to prevent the software from judging the abnormal batter temperature after the module is turned on,resulting in shutdown.the connection diagram is as follows:

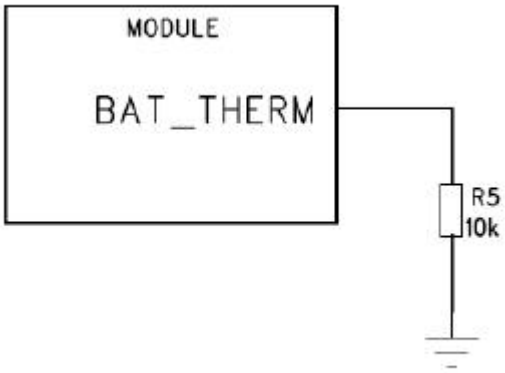


Figure 4.3：Connection diagram when not powered by battery

4.1.1. Power Pin

The VBAT pin (151, 152, 153) is used for power input. In the user's design, pay special attention to the design of the power supply section to ensure that the VBAT does not fall below 3.4V even when the module consumes 2A. If the voltage drops below 3.4V, the module may shut down. The PCB layout from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

Figure 4.4: minimum voltage for Vbat drop

4.2. Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In extreme cases, such operations can cause permanent damage to the module.

4.2.1. Module Boot

The user can power on the module by pulling the KYPD_PWR_N1 pin (142) low. The pull-down time is at least 5 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows; or the CBL_PWR_N pin (203) is pulled low. CBL_PWR_N can be powered on by 10K pull-down resistor to GND. It does not need to release this signal after booting

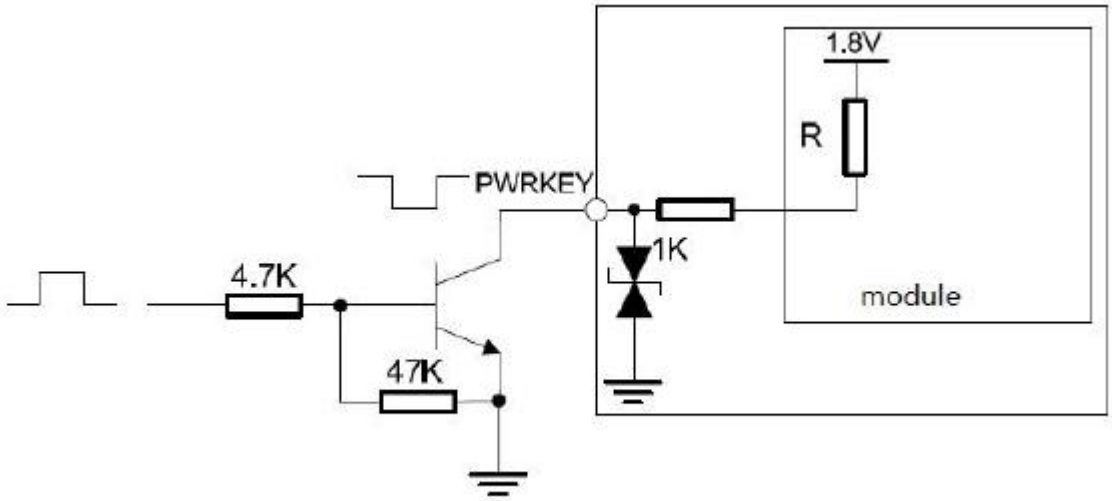


Figure 4.5：Using an external signal to drive the module to boot

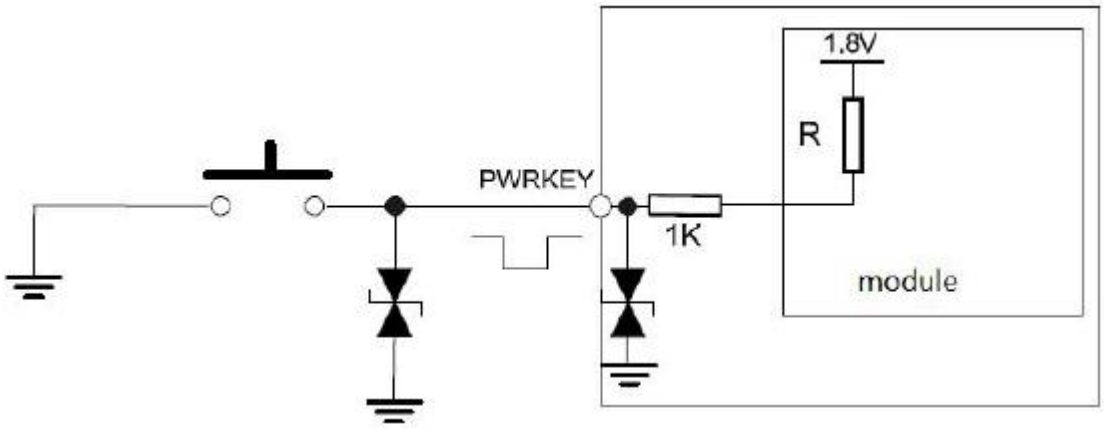


Figure 4.6：Booting with the button circuit

The following figure is the boot timing description:

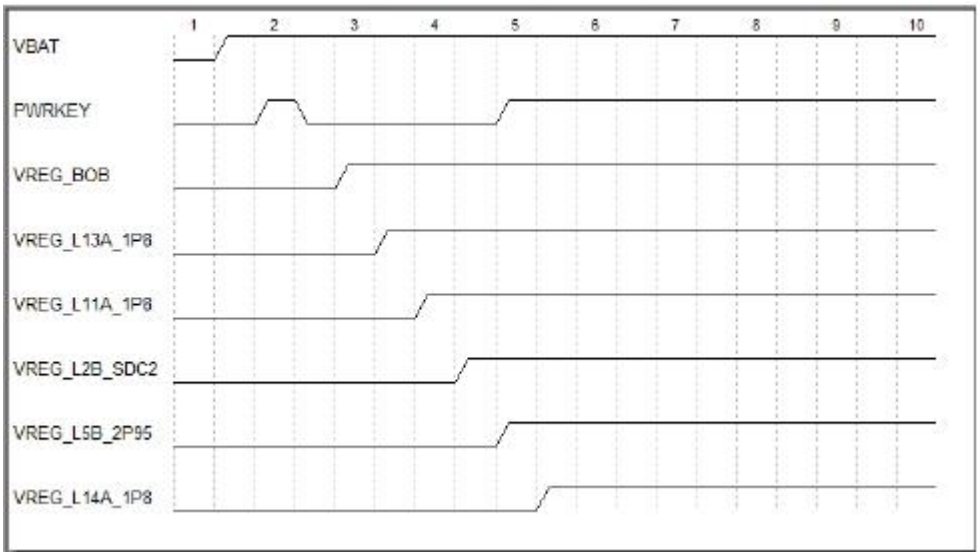


Figure 4.7: Using PWRKEY boot timing diagram

4.2.2. Module Shutdown

Users can use the PWRKEY pin to shutdown.

4.2.2.1 PWRKEY Shutdown

The user can turn off the PWRKEY signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the boot circuit. After the module detects the shutdown action, a prompt window pops up on the screen to confirm whether to perform the shutdown action.

The user can achieve a forced shutdown by pulling PWRKEY down for a long time, pulling down for at least 15 seconds.

4.2.3.Module Reset

The SNM900module supports a reset function that allows the user to quickly restart the module by pulling the RESET pin of the module low. The recommended circuit is as follows:

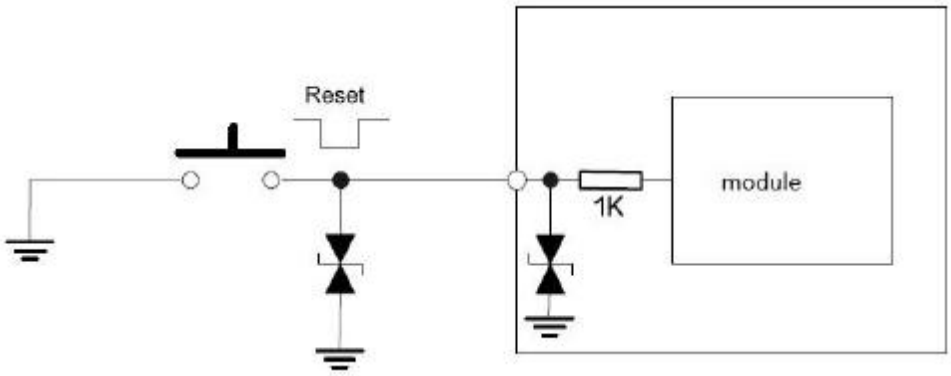


Figure 4.8: Reset using the key circuit

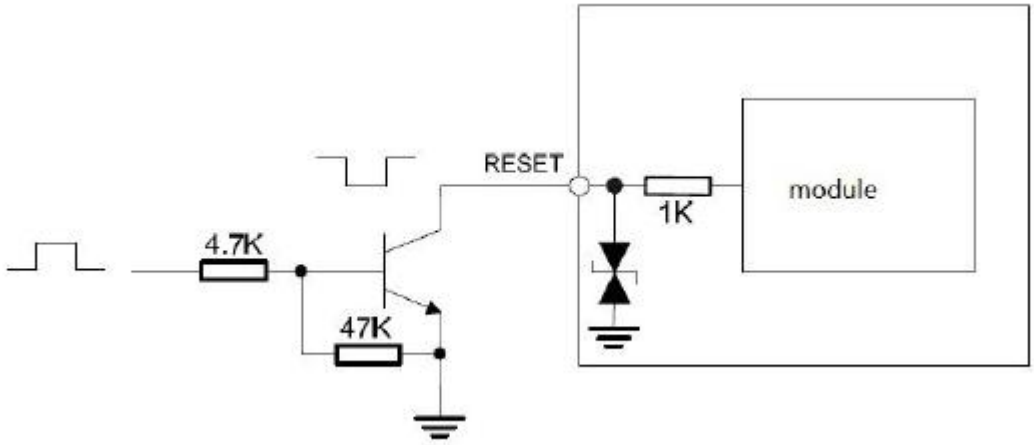


Figure 4.9： Reset Module Using External Signal

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or 3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET can refer to the following table:

Table 4.1：RESET Hardware Parameters

Pin	Description	Minimum	Typical	Maximum	Unit
RESET	Input high level	1	-	-	V
	Input low level	-	-	0.65	V
	Pull down effective time	500		-	ms

4.3. VCOIN Power

When VBAT is disconnected, the user needs to save the real-time clock. The VCOIN pin cannot be left floating. It should be connected to a large capacitor or battery. When external capacitor is connected, the recommended value is 100uF, and the real-time clock can be kept for 1 minute. The reference design circuit is used when the RTC power supply uses an external large capacitor or battery to power the RTC inside the module:

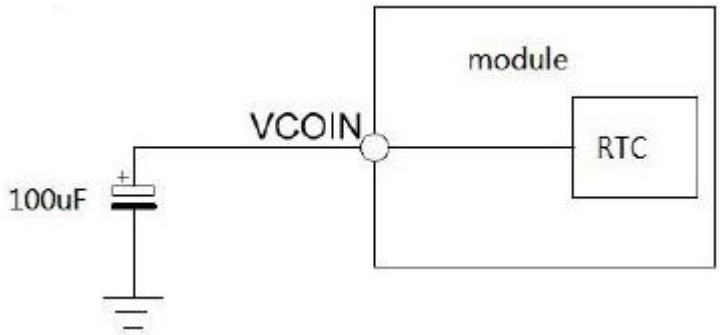


Figure 4.10：External Capacitor Powering the RTC

Non-rechargeable battery powered:

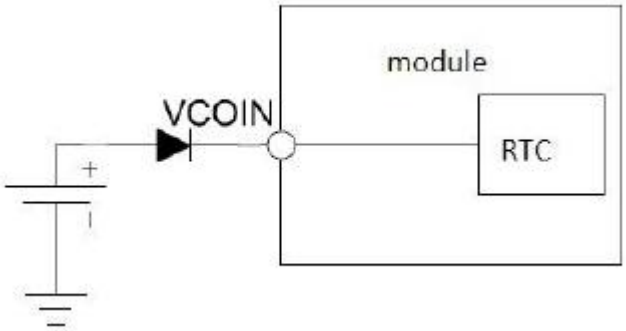


Figure 4.11：Non-rechargeable battery to power the RTC

Rechargeable battery powered:

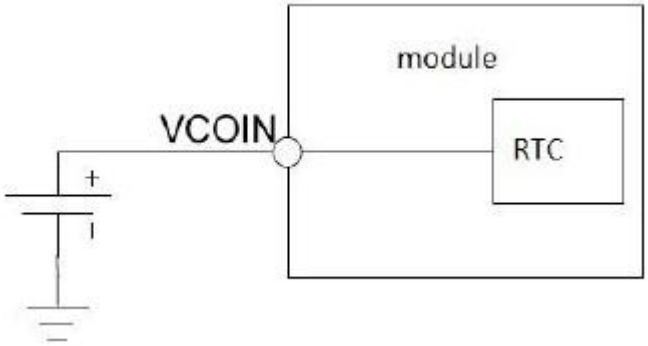


Figure 4.12： Rechargeable Battery Powers RTC

This VCOIN power supply is typically 3.0V.

4.4. Power Output

The SNM900 has multiple power outputs. For SD card,SIM ,sensor,touch panel, LDO , etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high frequency interference.

Table 4.2：Power Description

Signal	Default Voltage(V)	Drive Current(mA)
VREG_L13A_1P8	1.8	100
VREG_L11A_1P8	1.8	100
VREG_L3B_3P0	3.0	300
VPH_PWR	3.8	
VREG_L5B_2P95	2.95	600
VREG_L2B_SDC2	2.95	50
VREG_L15A_UIM1	1.8/2.95	50
VREG_L17A_UIM2	1.8/2.95	50
VREG_L14A_1P8	1.8	150
VREG_BOB	3.3	300

4.5. Serial Port

The SNM900 provides three serial ports for communication. And corresponding to three groups of I2C interfaces can be multiplexed into hardware flow control, note that the I2C interface can not be added to the UART_RTS/CTS when the pull resistor can be added.

Table 4.3：UART Pin Description

Name	Pin	Direction	Function
GPIO4_UART2_MSM_TX	11	O	UART Data Transmission
GPIO5_UART2_MSM_RX	12	I	UART Data Reception
GPIO6_I2C2_SDA	13	I	UART Clear To Send（CTS）
GPIO7_I2C2_SCL	14	O	UART Request To Send(RTS)
GPIO29_UART_RX	16	I	UART Data Reception
GPIO28_UART_TX	15	O	UART Data Transmission
GPIO30_I2C_SDA_8A	254	I	UART Clear To Send（CTS）
GPIO31_I2C_SCL_8A	253	O	UART Request To Send（RTS）
GPIO1_UART1_RX	177	I	UART Data Reception
GPIO0_UART1_TX	176	O	UART Data Transmission
GPIO2_I2C1_SDA	184	I	UART Clear To Send（CTS）
GPIO3_I2C1_SCL	185	O	UART Request To Send（RTS）

Please refer to the following connection method:

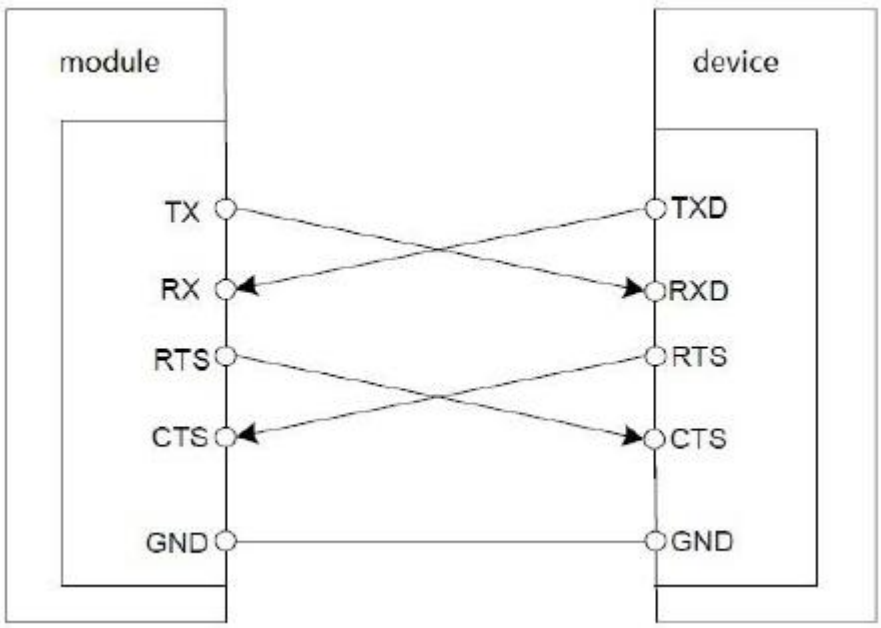


Figure 4.13：Serial Port Connection Diagram

When the serial level used by the user does not match the module, in addition to adding the level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to this two circuits.

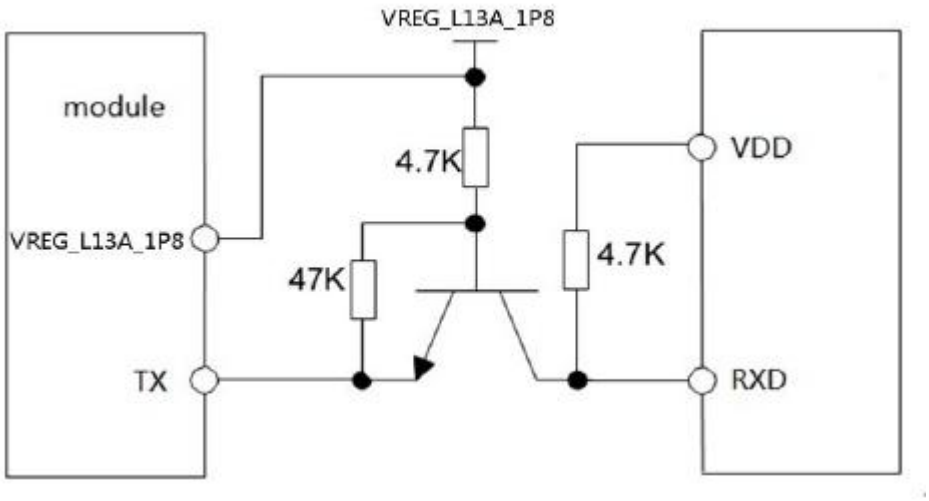


Figure 4.14：TX Connection Diagram

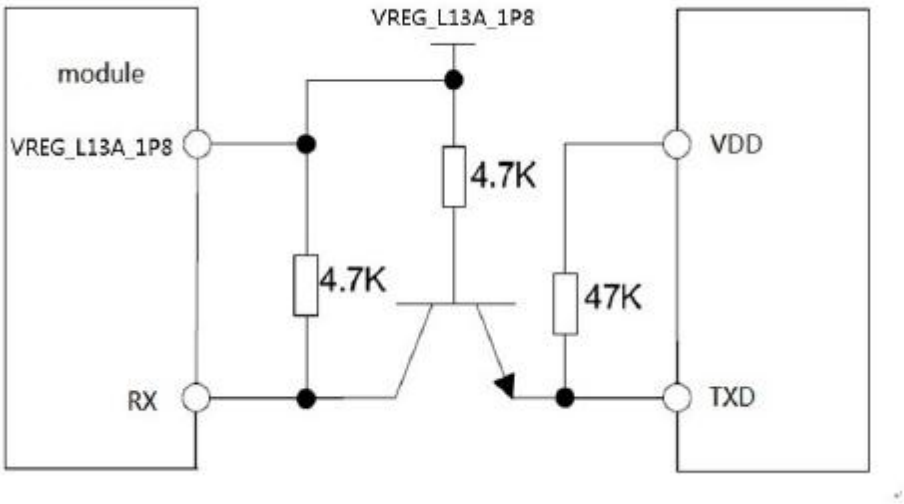


Figure 4.15：RX Connection Diagram

Note ： When using Levels Isolation in Figures 4.14 and 4.15, it is necessary to use VREG_L13A_1P8 as the pull-up power supply. VREG_L11A_1P8 will enter the low power mode during sleep. It is not recommended.

Table 4.4：Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Input low level	-	0.45	V
Input high level	1.35	-	V

Note：1. The serial port of the module is a CMOS interface, If necessary, please use the RS232 conversion chip.

2. If the 1.8V output of the module cannot meet the high level range of the user terminal, please add a level shifting circuit.

4.6. MIPI Interface

The SNM900 supports the Moble Industry Processor Interface (MIPI) interface for Camera and LCD. The module supports FULL HD (2560*1600) display. The MIPI interface Main Camera supports up to 24MP, and the Front Camera supports16MP.

MIPI is a high-speed signal line. In the Layout stage, please follow the impedance and length requirements strictly, and control the length of the differential pair within the group and the group length. The total length should be as short as possible.

Metrics			Information/design guidance	Comments
General information	CLK frequency		750 MHz	
	Data rate		1.5 Gbit/s per lane	
Impedance	Differential	Main route	100Ω ± 3%	Inspected by TDR simulation @ 150 ps (20-80%). No manufacturing variation considered.
		Break-out	100Ω ± 10%	
		Connector	100Ω ± 20%	
	Single-ended	Main route	50Ω ± 20%	
		Break-out	50Ω ± 30%	
		Connector	50Ω ± 30%	
Length match	Intra-lane length match		0.7 mm (5 ps)	It is important to maintain differential lines; single line meandering should not be used other than at Tx breakout.
	Data to clock slew		1.4 mm (10 ps)	This target is for compliance mode. For mission mode while data rate is 1 Gbps or less, inter-pair skew may be relaxed to 100 ps; consider 100 ps for extra-cable inter-pair time skew. At 1.0-1.5 Gbps, this value is 50 ps. (Refer to the MIPI Alliance Specfication for D-PHY 9.2.1 for mission-mode target).
	Max trace length		30 cm	This max length guidance is practical level of definition. (Refer to the MIPI Alliance Specfication for D-PHY 7.6.1).
Spacing	Spacing to all other signal	Main route	4x line width	If not practical, may be relaxed to x3 line width by accepting potential risk. (Refer to the MIPI Alliance Specfication for D-PHY 7.6.5).
	Spacing data lane to lane		3x line width	If not practical, may be relaxed to x2 line width by accepting potential risk. (Refer to the MIPI Alliance Specfication for D-PHY 7.6.5).

4.6.1. LCD Interface

The SNM900 module supports the MIPI interface of two LCD displays, supports dual-screen display, and has a compatible screen identification signal. The resolution of the screen can be up to 2560*1600. The signal interface is shown in the following table. In the Layout, the MIPI signal line should strictly control the differential 100 ohm impedance and the equal

length between the signal line group and the group.

The module's MIPI interface is a 1.2V power domain. When the user needs a compatible screen design, the module's LCD_ID pin or ADC pin can be used.LCD 2.8V power supply needs external LDO generation, LDO input power can use vreg_ BOB。

Table 4.5：Primary and secondary screen interface definition

Main screen interface			
MIPI_DSI0_CLK_N	64	O	MIPI_LCD clock line
MIPI_DSI0_CLK_P	65	O	
MIPI_DSI0_LANE0_N	189	O	MIPI_LCD data line
MIPI_DSI0_LANE0_P	190	O	
MIPI_DSI0_LANE1_N	66	O	
MIPI_DSI0_LANE1_P	67	O	
MIPI_DSI0_LANE3_N	73	O	
MIPI_DSI0_LANE3_P	74	O	
MIPI_DSI0_LANE2_N	71	O	
MIPI_DSI0_LANE2_P	72	O	
GPIO53_LCD_RESET_N	75	I/O	LCD reset pin
GPIO59_LCD_TE0	76	I/O	LCD frame sync signa
WLED_SINK1	5	AI	LCD series backlight negative 1
WLED_SINK2	6	AI	LCD series backlight negative2
VREG_WLED	7	PO	LCD series backlight positive
VREG_L11A_1P8	139	PO	1.8V power supply

Secondary screen interface			
MIPI_DSI1_CLK_N	242	O	MIPI_LCD2 clock line
MIPI_DSI1_CLK_P	241	O	
MIPI_DSI1_LANE0_N	226	O	MIPI_LCD2 data line
MIPI_DSI1_LANE0_P	225	O	
MIPI_DSI1_LANE1_N	240	O	
MIPI_DSI1_LANE1_P	239	O	
MIPI_DSI1_LANE2_N	244	O	
MIPI_DSI1_LANE2_P	243	O	
MIPI_DSI1_LANE3_N	246	O	
MIPI_DSI1_LANE3_P	245	O	
GPIO73	99	I/O	LCD2 reset pin

GPIO51	77	I/O	LCD2 frame sync signal
PM660L_PWM	112	O	Screen backlight PWM control
VREG_L11A_1P8	139	PO	1.8V power supply

LCD_ID of the module, this pin is internally GPIO. When used as LCD_ID, please confirm the internal circuit of LCD. If the internal divider of the LCD uses resistor divider, please pay attention to the voltage to meet the high or low range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor near the LCD side.

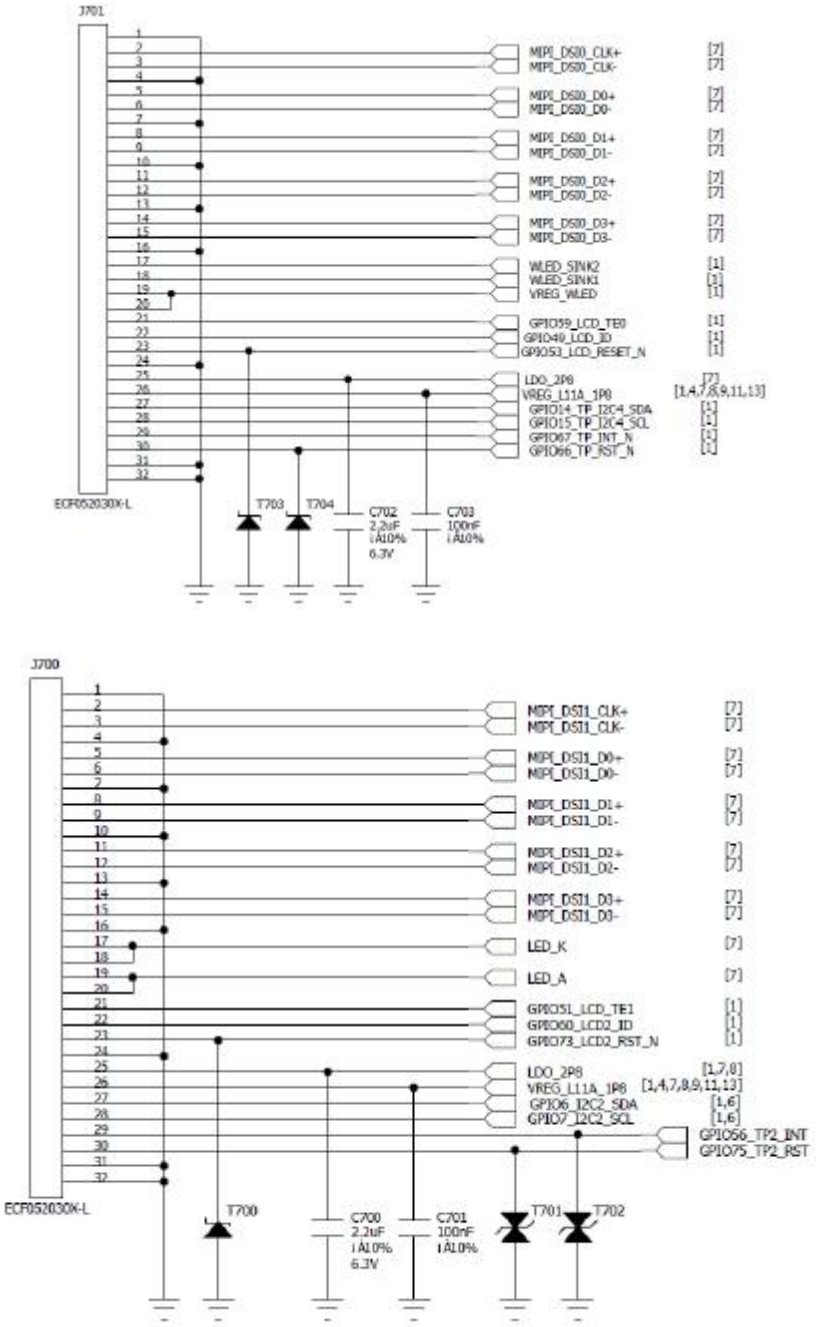


Figure 4.16：Main LCD and sub LCD interface circuit

Among them, LDO_ 2p8 needs to be generated by external 2.8V LDO. Refer to Fig. 4.17 for LDO circuit. It is suggested to use two 2.8V LDOS to supply power to the main and auxiliary panels respectively in the design of main and auxiliary screens.

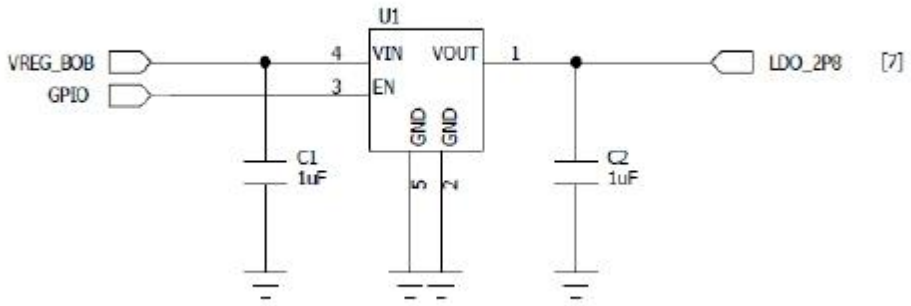


Figure 4.17: LCD 2.8V LDO reference circuit

SNM900 module has its own backlight drive output. Customers can directly use this function to drive LCM backlight. The backlight driving features of SNM900 are as follows:

- Common anode driving mode, vreg_ WLED is a common anode output, and the output voltage can be configured up to 28V:
- WLED_ Sink has two channels, each of which can support 30mA current at most. The two-way series connection can light up 16 LEDs
- The software can be configured with WLED_ Sink current to adjust the backlight brightness.

In the design of the main and secondary screens, the main screen can directly use the SNM900 internal backlight circuit vreg_ WLED，WLED_ SINK1，WLED_ Sink2 can support up to two strings of 8, with a total of 16 lights; the backlight driving circuit of the sub screen can refer to figure 4.18, and the backlight brightness can be adjusted through the pm660l of the module_ PWM to achieve, the modulation mode is PWM mode.

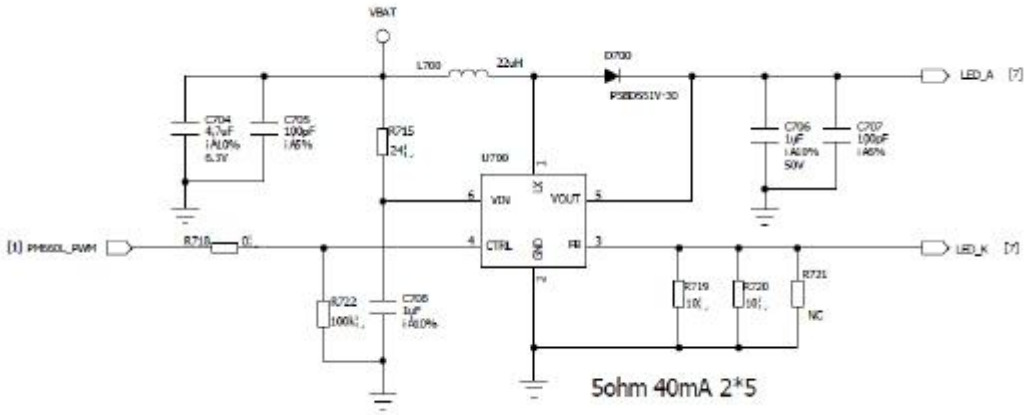


Figure 4.18：Backlight drive schematic

Note: 1. The backlight circuit should select the chip according to the backlight circuit of the LCD. Users should carefully read the LCD document and select the correct driver chip. The

reference circuit provided in this document is a series-type PWM dimming backlight driver circuit; if it is a series-type one-line dimming backlight driver circuit, it needs to be controlled by GPIO.

4.6.2.MIPI Camera Interface

The SNM900 module supports the MIPI interface Camera and provides a dedicated camera power supply. The main camera is a CSI0 interface that supports four sets of data lines and can support up to24M pixels. The front camera is a CSI2 interface that supports four sets of data lines and can support16M pixels. There is also a set of CSI1 interface, which can do dual 16M dual camera design with the main camera, or as a dual camera design for the depth of field camera; it can also be used as the MIPI interface scan head design.

The module does not provide the power required by camera, including avdd-2.8v, afvdd-2.8v (focusing motor power supply) and dvdd-1.2v (CAM core voltage), which need external LDO generation.

Table 4.6: MIPI Camera Interface Definition

Main camera interface			
Name	Pin	Input/output	Description
MIPI_CSI0_CLK_N	50	O	Main camera MIPI clock signal
MIPI_CSI0_CLK_P	49	O	
MIPI_CSI0_LANE0_N	56	I	Main camera MIPI data signal
MIPI_CSI0_LANE0_P	55	I	
MIPI_CSI0_LANE1_N	194	I	
MIPI_CSI0_LANE1_P	193	I	
MIPI_CSI0_LANE2_N	52	I	
MIPI_CSI0_LANE2_P	51	I	
MIPI_CSI0_LANE3_N	54	I	
MIPI_CSI0_LANE3_P	53	I	
GPIO32_CAM_MCLK0	84	I/O	Main camera clock signal
GPIO46_CAM0_RST_N	85	I/O	Main camera reset signal
GPIO44_CAM0_STANDBY_N	86	I/O	Main camera sleep signal
CAM_I2C_SDA0	105	I/O	I2C data
CAM_I2C_SCL0	104	I/O	I2C clock
VREG_L11A_1P8	139	PO	1.8V IOVDD

Front camera interface			
Name	Pin	Input/output	Description
MIPI_CSI2_CLK_P	40	O	Front camera MIPI clock signal
MIPI_CSI2_CLK_N	41	O	
MIPI_CSI2_LANE0_P	42	I	Front camera MIPI data signal
MIPI_CSI2_LANE0_N	43	I	

MIPI_CSI2_LANE1_P	191	I	
MIPI_CSI2_LANE1_N	192	I	
MIPI_CSI2_LANE2_P	46	I	
MIPI_CSI2_LANE2_N	47	I	
MIPI_CSI2_LANE3_P	44	I	
MIPI_CSI2_LANE3_N	45	I	
GPIO33_CAM_MCLK1	80	I/O	Front camera clock signal
GPIO47_SCAM_RST_N	79	I/O	Front camera reset signal
GPIO50_SCAM_PWD_N	78	I/O	Front camera sleep signal
CAM_I2C_SDA1	96	I/O	I2C data
CAM_I2C_SCL1	95	I/O	I2C clock
VREG_L11A_1P8	139	PO	1.8V IOVDD

Depth camera interface			
Name	Pin	Input / output	Description
MIPI_CSI1_CLK_N	207	O	Depth camera MIPI clock signal
MIPI_CSI1_CLK_P	208	O	
MIPI_CSI1_LANE0_N	63	I	Depth camera MIPI data signal
MIPI_CSI1_LANE0_P	62	I	
MIPI_CSI1_LANE1_N	59	I	
MIPI_CSI1_LANE1_P	58	I	
MIPI_CSI1_LANE2_N	172	I	
MIPI_CSI1_LANE2_P	171	I	
MIPI_CSI1_LANE3_N	61	I	
MIPI_CSI1_LANE3_P	60	I	
GPIO34_CAM_MCLK2	264	I/O	Depth camera clock signal
GPIO48_DCAM_RST_N	263	I/O	Depth camera reset signal
GPIO55_DCAM_PWD_N	262	I/O	Depth camera sleep signal
CAM_I2C_SDA1	96	I/O	I2C date
CAM_I2C_SCL1	95	I/O	I2C clock
VREG_L11A_1P8	139	PO	1.8V IOVDD

If the user designs to use the CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the driver chip of CAMERA, and the correct connection is as follows:

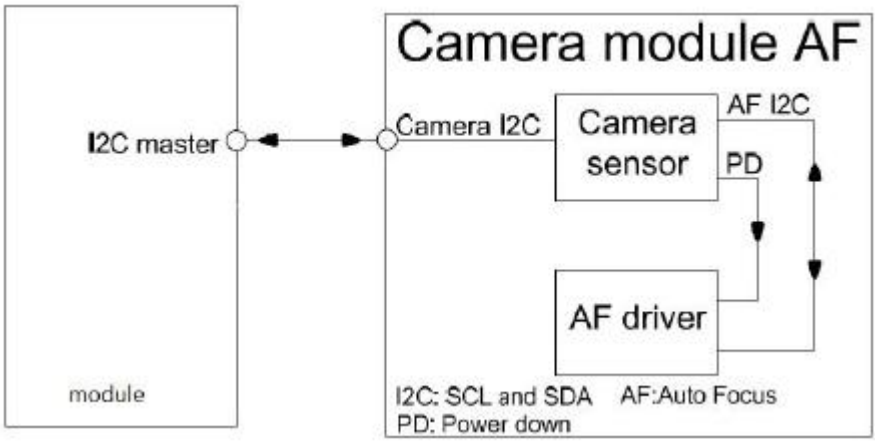
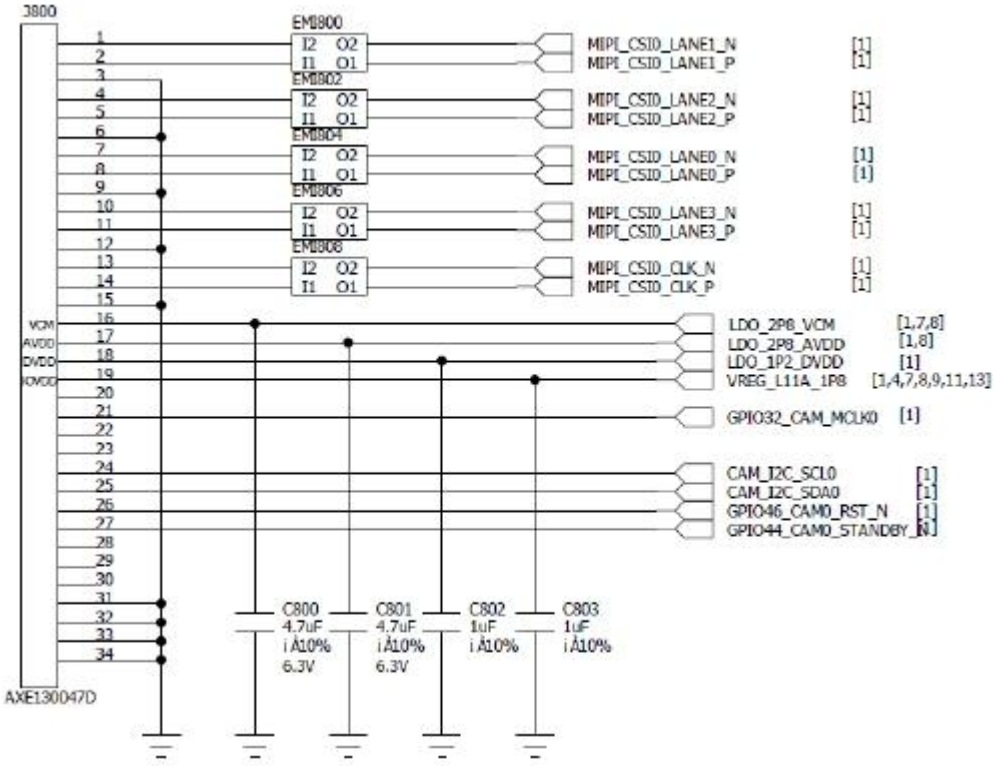


Figure 4.19：Correct CAMERA connection diagram

The MIPI interface has a high rate. The user should control the impedance by 100 ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.



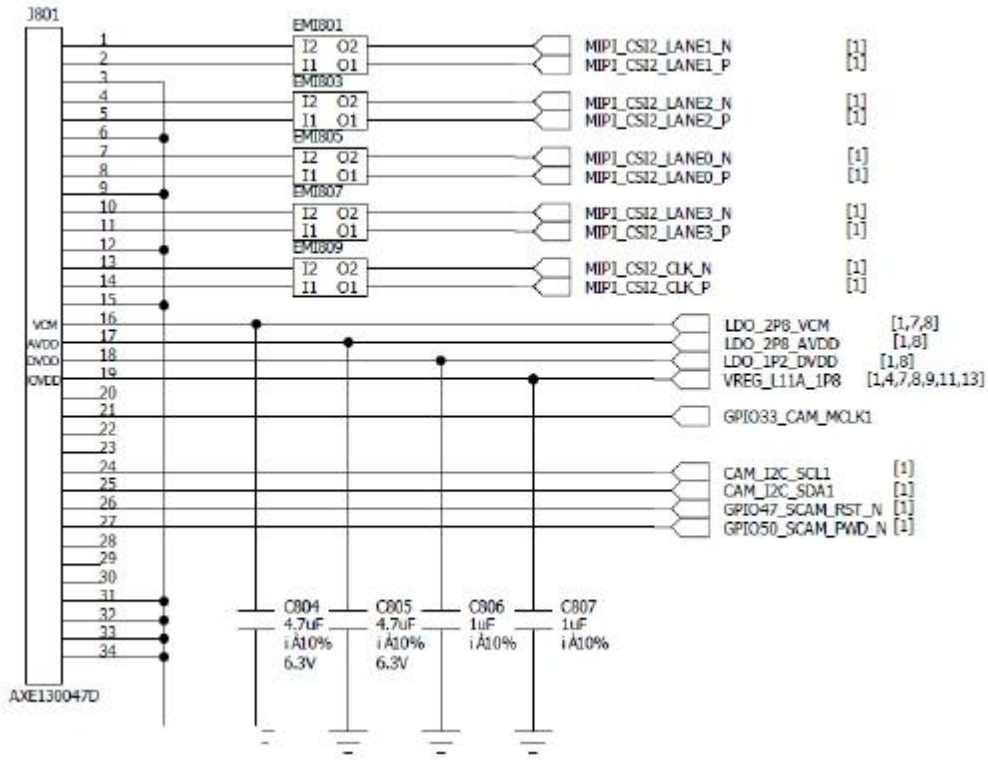


Figure 4.20：MIPI Camera Reference Circuit

The power supply required by camera, including avdd-2.8v, afvdd-2.8v (focusing motor power supply) and dvdd-1.2v (CAM core voltage), can be designed with reference to the following LDO circuit

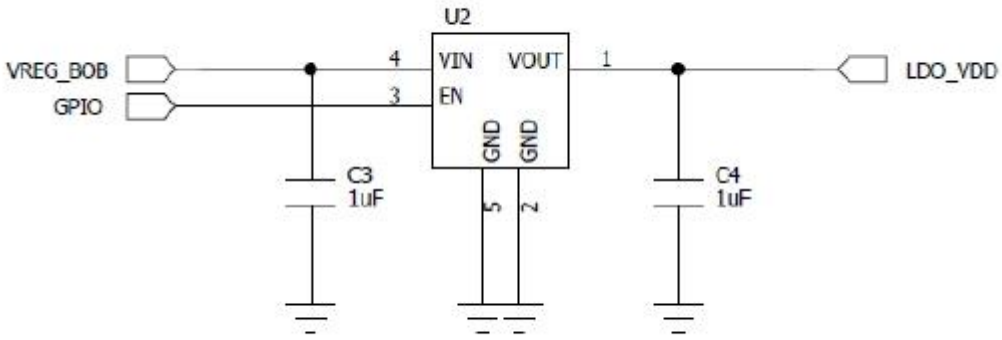


Figure 4.21 camera power reference circuit

Important note: When designing the camera function, you need to pay attention to the position of the connector. There will be a small person in the specification of the camera to indicate the imaging direction. You need to ensure that the villain is standing on the long side of the LCD, otherwise the camera will be flipped. The software cannot be adjusted at 90°. As shown in the two figures below.

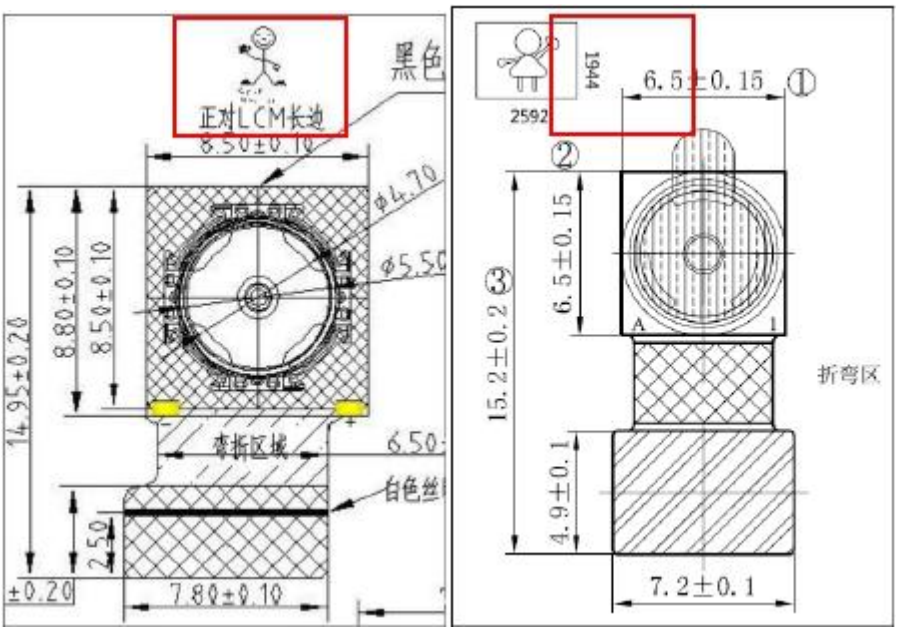


Figure 4.22：Camera imaging diagram

4.7.Resistive Touch Interface

The module does not provide a resistive touch screen interface. If the user needs to use a resistive touch, an external dedicated chip is required. The module can provide an I2C interface.

4.8.CapacitiveTouch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touches The default interface pins for capacitive touch software are defined as followsThe 2.8V power supply required by capacitor panel needs external LDO generation.

Table 4.7：Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO14_TP_I2C4_SDA	234	I/O	The capacitive touch I2C interface needs to be pulled up to VREG_L11A_1P8
GPIO15_TP_I2C4_SCL	233	I/O	
GPIO67_TP_INT_N	97	I	Interrupt
GPIO66_TP_RST_N	98	O	Reset
VREG_L11A_1P8	139	PO	1.8V Power supply

Note: The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.9.Audio Interface

The module provides three analog audio inputs, MIC_IN1_P/M for the main microphone, MIC_IN2_P for the microphone, and MIC_IN3_P for the noise reduction microphone. The module also provides three analog audio outputs (HPH_L/R, REC_P/N, SPK_P/N). The

audio pin is defined as follows:

Table 4.8：Audio Pin Definitions

Name	Pin	Input/Output	Description
MIC_IN1_M	123	I	Main MIC negative, grounded at MIC
MIC_IN1_P	122	I	Main MIC positive
MIC_IN2_P	132	I	Headphone MIC positive
GND_MIC	124	I	Headphone MIC, noise reduction MIC
MIC_IN3_P	131	I	Noise reduction MIC positive
MIC_BIAS1	118	O	BIAS voltage of the main MIC for silicon wheat
MIC_BIAS2	117	O	BIAS voltage of the headphone MIC for silicon wheat design
CDC_HPH_R	128	O	Headphone right channel
CDC_HPH_L	126	O	Headphone left channel
CDC_HS_DET	125	I	Headphone plug detection
CDC_HPH_REF	127	I	Headphone reference ground
CDC_EAR_M	129	O	Earpiece output negative
CDC_EAR_P	130	O	Earpiece output positive
SPKR_DRV_M	133	O	Amplifier (0.8W) output negative
SPKR_DRV_P	134	O	Amplifier (0.8W) output positive

Users are advised to use the following circuit according to the actual application to get better sound effects.

4.9.1 Receiver Interface Circuit

The receiver interface circuit places the following devices near the REC end, and B302 and B303 can be changed to magnetic beads according to actual effects.

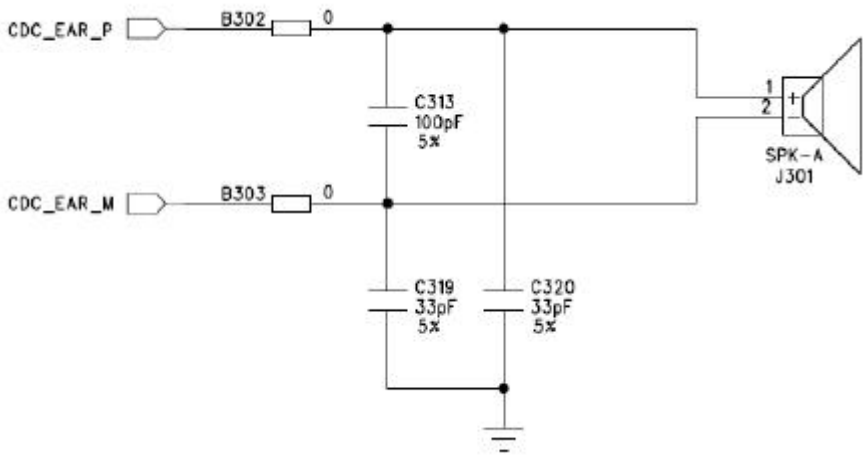


Figure 4.23：Receiver Interface Circuit

4.9.2 Microphone receiving Circuit

On the right side is the MEMS microphone interface circuit, which has more bias power supply than electret mic. The negative signal of main mic must be designed with 0r to ground resistance close to MIC. As shown in Figure 4.24.

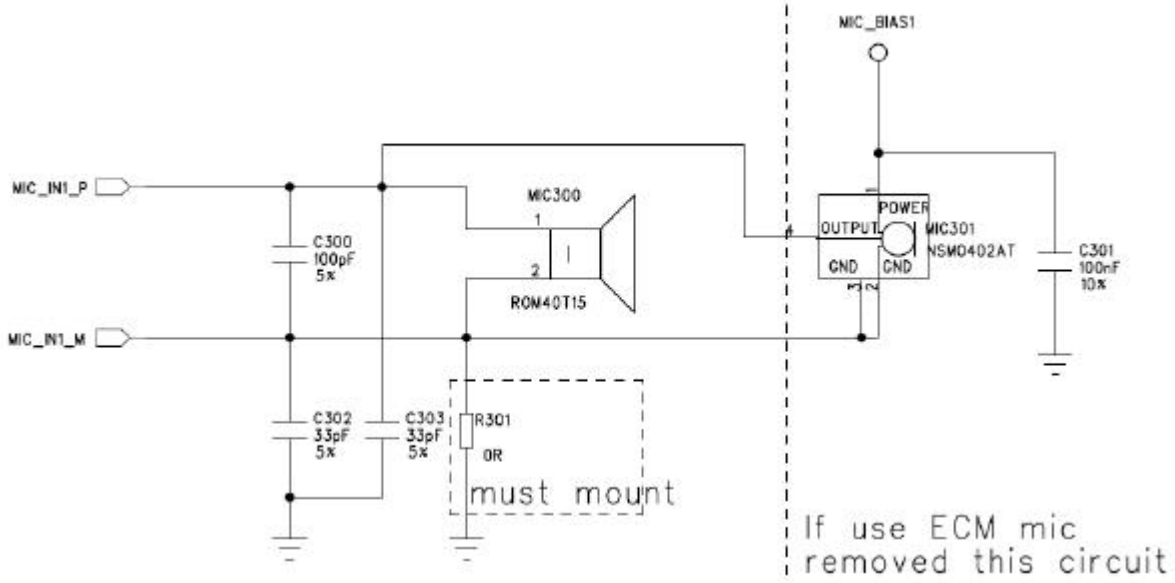


Figure 4.24： Microphone Differential Interface Circuit

4.9.3.Headphone Interface Circuit

The module integrates a stereo headphone jack. Users are advised to reserve ESD devices during the design phase to prevent ESD damage. The HS_DET pin of the module can be set as an interrupt. In software, this pin is the earphone interrupt by default. The user can use this pin to detect the plugging and unplugging of the earphone.

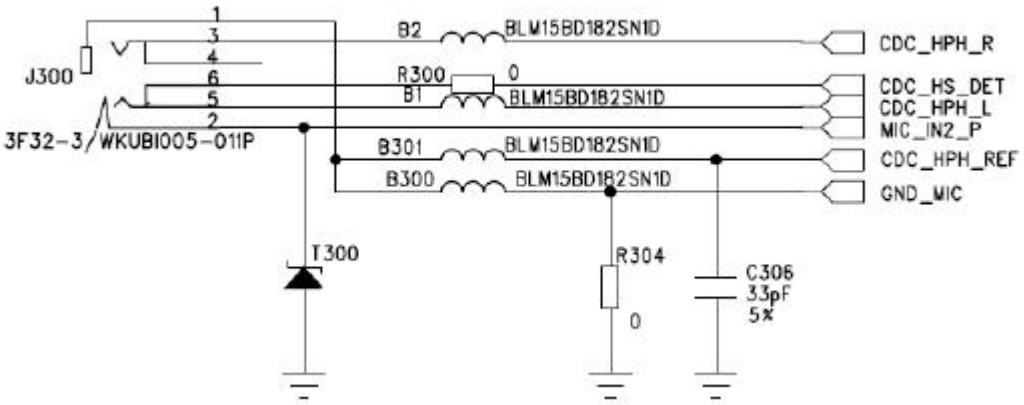


Figure 4.25：Headphone Interface Circuit

Note:

1. The earphone holder in Figure 4.24 is normally closed. If the user is using the normally open mode earphone holder, please modify the detection circuit according to the actual pin and modify the software accordingly.

2. We recommend that the headphone detection pin HS_DET and HPH_L form a detection circuit (the connection method in the above figure), because HPH_L has a pull-down resistor inside the chip, which can ensure that HS_DET is low when connected with HPH_L, if the user will HS_DET and HPH_R To connect, please reserve a 1K pull-down resistor on HPH_R.
3. The standard of the headphone interface is the European standard OMPT. If you need to design the American standard CTIA interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headset standards, you need an external dedicated chip, such as the TI-TS3A226AE.

4.9.4.Speaker Interface Circuit

The module integrates a Class-D audio amplifier with an output power of 0.8W and an output signal of SPKR_DRV_P / SPKR_DRV_M。

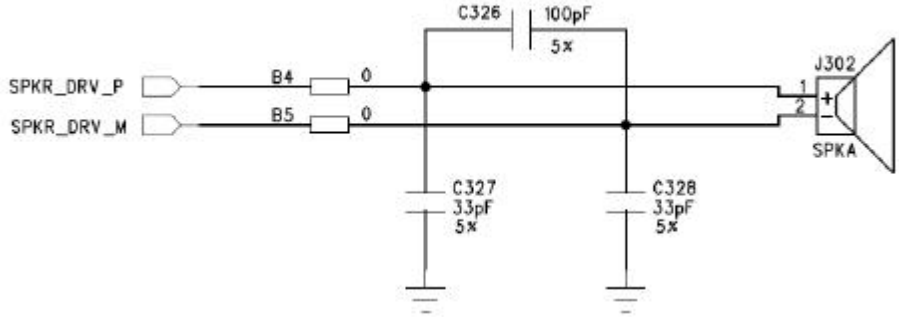


Figure 4.26: recommended circuit with internal audio amplifier

It is also possible to add an audio amplifier externally, using CDC_HPH_R as a single-ended input signal, and the reference circuit is shown below.

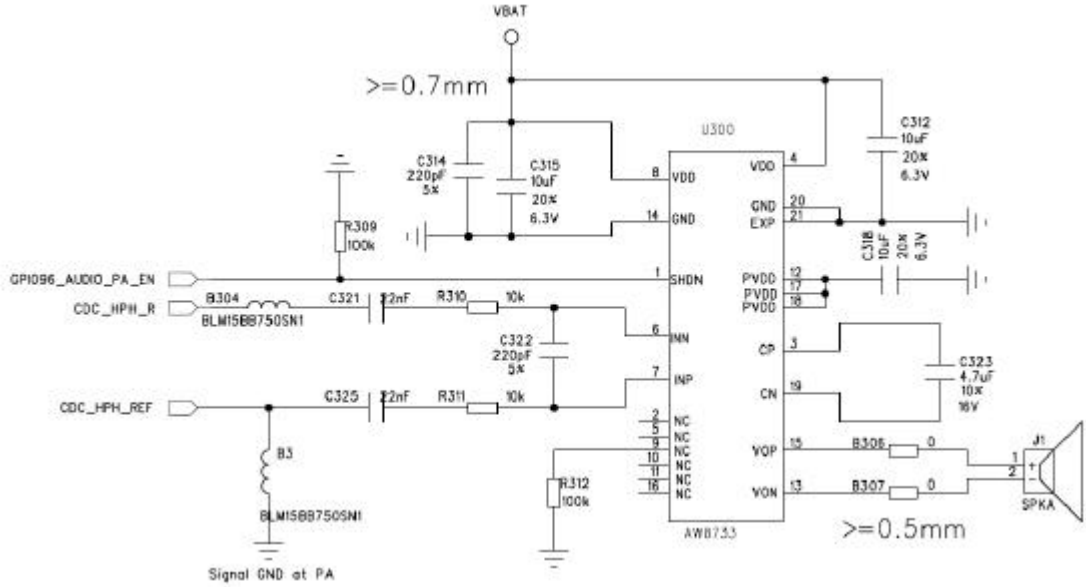


Figure 4.27：Recommended circuit with external audio amplifier

4.9.5.I2S Interface

There are two sets of GPIO-compatible I2S interfaces inside the module. The pins used by this function are as follows:

Table 4.9: pin definition of I2S interface

Name	Pin	Intput/Output	Description
LPI_GPIO7_MI2S3_D1	212	I	I2S3 input DATA
LPI_GPIO6_MI2S3_D0	265	O	I2S3output DATA
LPI_GPIO5_MI2S3_WS	271	O	I2S3_ WS
LPI_GPIO4_MI2S3_SCLK	169	O	I2S3_ SLK
GPIO27_MI2S_2_D1	266	I	I2S2 input DATA
GPIO26_MI2S_2_D0	267	O	I2S2 output DATA
GPIO25_MI2S_2_WS	268	O	I2S2_WS
GPIO24_MI2S_2_SCK	269	O	I2S2_SCK

4.10. USB Interface

The SNM900 supports a USB 2.0 /3.0High/Super speed interface. It must control the 90 ohm differential impedance during Layout and control the external trace length.It should be noted that SNM900 module must be controlled by hardware to switch the USB interface of type-C and mirco. The pins required for switching circuit are shown in the following table:

Table 4.10: USB interface switch pin definition

Name	Pin	Intput/Output	Description
USB_PHY_PS	250	O	Type-c or Micro USB switch
USB_PHY_DIR	188	I	Type-c or Micro USB switch
UUSB_TYPEC	183	I	Type-c or Micro USB switch
VPH_PWR	136、137	I/O	System power input and output, typical value 3.8V

The switching circuit can refer to the following design, when the switch 1,2 is turned on, USB_ PHY_ Dir and USB_ PHY_ PS direct connection, uusb_ Typec is pulled up to VPH through 10K resistor_ When PWR is switched to the type-C interface, switches 3 and 4 are turned on, that is, USB_ PHY_ DIR，UUSB_ TYPEC When typec is grounded through 10K resistance, it switches to mirco USB interface

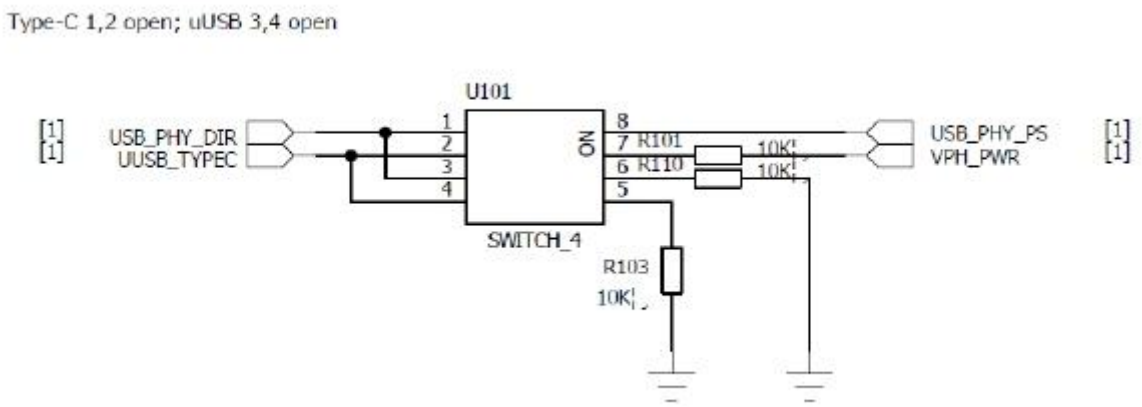


Figure 4.28: USB interface type switching reference circuit

The module also supports OTG function and can output 5V / 1.5A current
The voltage input range during charging is as follows:

Table 4.11： Voltage input range during charging

Name	Description	Minimum	Typical	Maximum	Unit
VBUS	Input range	4	-	6	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. The DM/DP must add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting the TVS, the user should pay attention to the load capacitance of less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand, it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

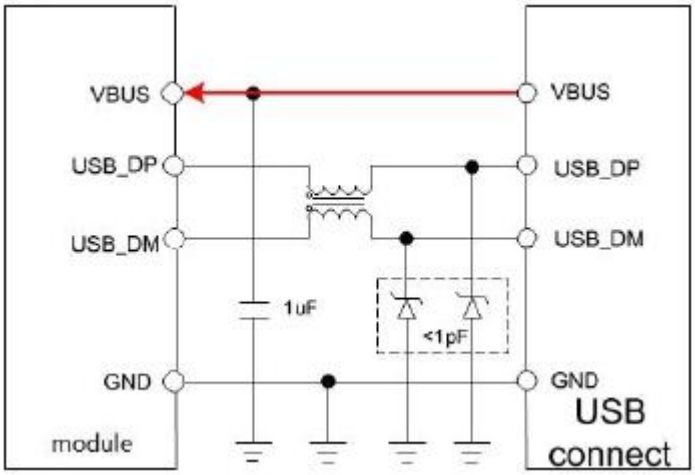


Figure 4.29: USB connection diagram

4.10.1. USB OTG

The SNM900 module can provide USB OTG function. The pins used in this function are as follows:

Table 4.12： USB OTG Pin Description

Pin name	Pin	Description
VBUS	157、158、159	5V charging input / OTG output power.
USB30_HS_DM	145	USB Date-

USB30_HS_DP	146	USB Date-
USB_ID	143	USB ID

The recommended circuit diagram of USB OTG is as follows:

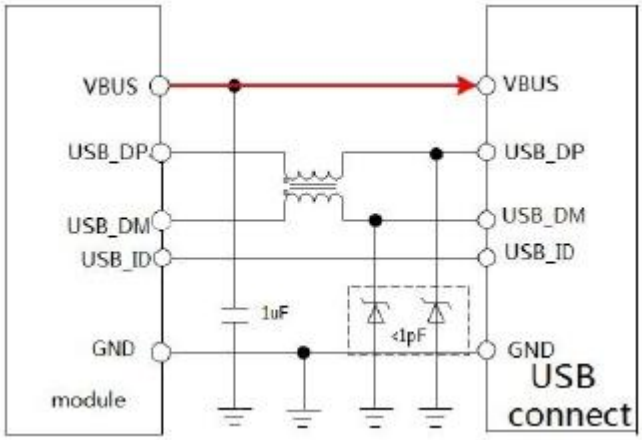


Figure 4.30： USB-OTG Connection Diagram

4.11. Charging Interface

SNM900 module is internally integrated with 3A charging scheme. The charging related contents in this manual are only described by internal charging scheme. The sdm660 platform uses the internal integrated charging chip of Qualcomm pm660 by default, and supports the charging protocol of qc3.0 & 4.0. The chip is in switching mode and has high efficiency. It integrates 15bit battery voltage detection ADC and 15bit current detection ADC, and the maximum charging current can reach 3A.

4.11.1. Charging Detection

When the voltage of VBUS pin is higher than 4.0V, a hardware interrupt will be generated in the module_ HS_ DP、USB_ HS_ DM、USB_ CC1、USB_ CC2 status to identify whether the charger is plugged in or the USB cable is plugged in.。

4.11.2. Charge Control

The SNM900 module can charge the over-discharged battery. The charging process includes trickle charge, pre-charge, constant current, and constant-voltage charge. When the VBAT voltage is lower than 3.4V, the module is pre-charged; when VBAT is between 3.4V and 4.2V, it is charged by the constant current plus constant voltage method optimized for the lithium battery. At present, the software's charge cut-off voltage is 4.2V, and the back-off voltage is 4.05V.

4.11.3. BAT_CON_TEM

The SNM900 module has battery temperature detection and can be implemented by BAT_THERM (149PIN). This requires the internal integration of a 10KΩ thermistor (negative

temperature coefficient) inside the battery to connect the thermistor to the BAT_THERM pin. During the charging process, the software reads the voltage of the BAT_THERM pin to determine if the battery temperature is too high. If the temperature is too high or too low, the battery will stop charging immediately to prevent battery damage. The battery charging connection diagram is shown below:

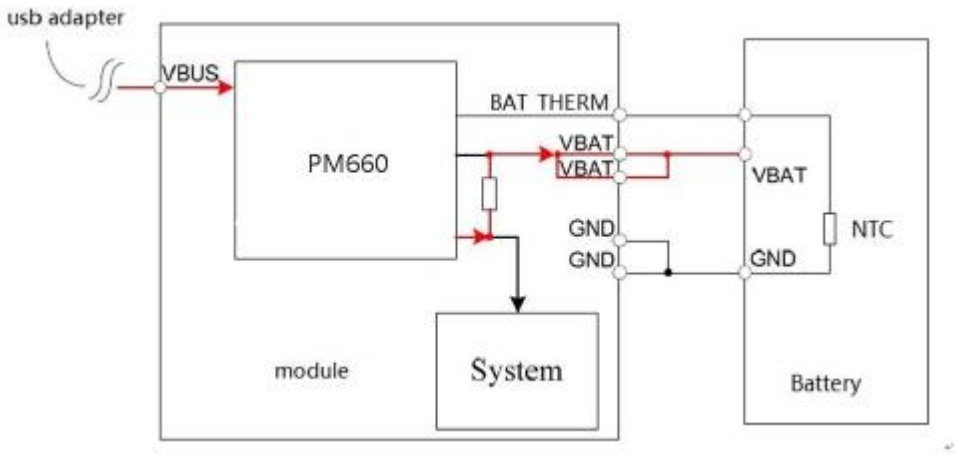


Figure 4.31： Charging circuit connection diagram

4.12 UIM Card Interface

The SNM900 can support two SIM cards at the same time to achieve dual card dual standby. Support SIM card hot swap, can automatically recognize 1.8V and 3.0V cards. The figure below is the SIM recommended interface circuit. In order to protect the SIM card, it is recommended to use TVS devices for electrostatic protection. The device of the peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

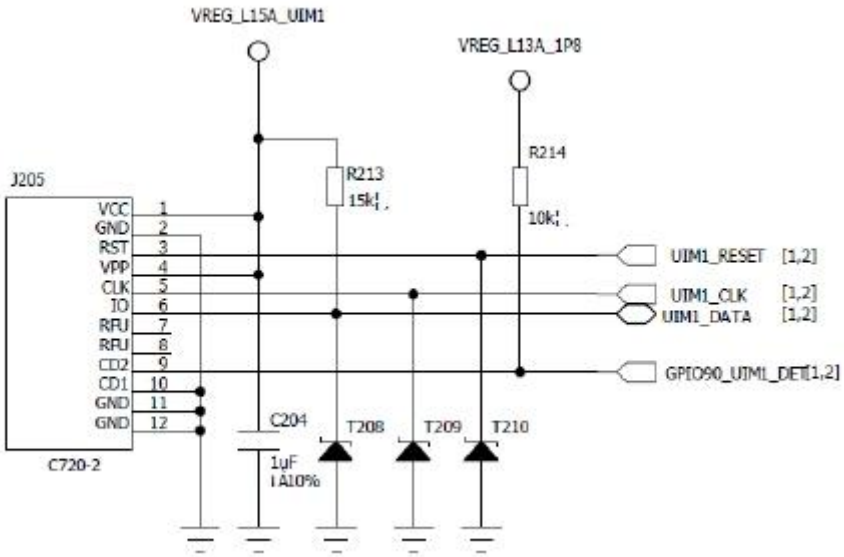


Figure 4.32： UIM card interface circuit

4.13. SD Card Interface

SNM900 supports SD card interface and supports up to 128GB.

The reference circuit is as follows:

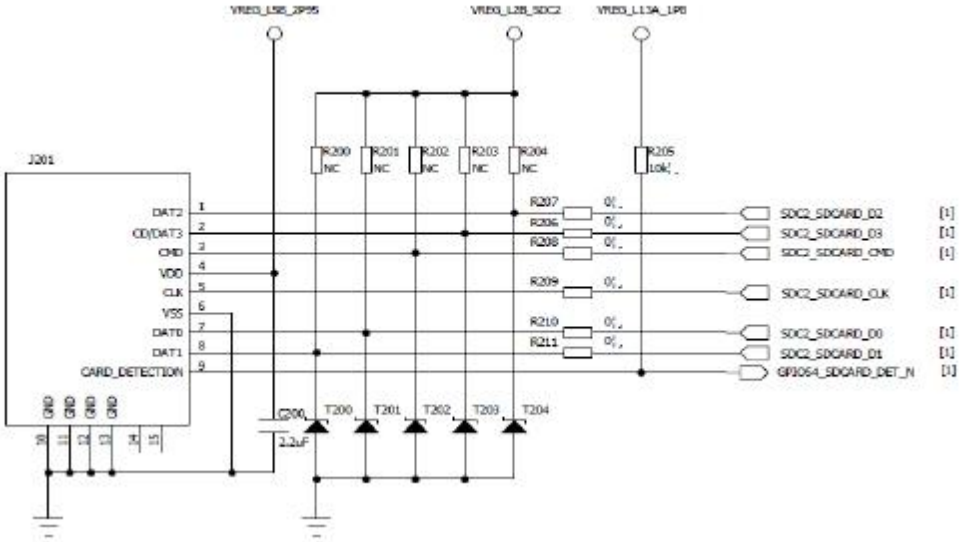


Figure 4.33： SD Card Interface Circuit

4.14 I2C Bus Interface

The SNM900 module supports seven hardware I2C bus interfaces and Two camera-specific CCI interface. The pin definitions and default functions are as follows:

Table 4.13: I2C Interface Pin Description

Name	Pin	Default function
CAM_I2C_SDA0	105	Camera dedicated
CAM_I2C_SCL0	104	
LPI_SENSOR_I2C_SDA	17	Sensor only
LPI_SENSOR_I2C_SCL	18	
GPIO6_I2C2_SDA	13	General purpose I2C
GPIO7_I2C2_SCL	14	
GPIO10_I2C3_SDA	164	General purpose I2C
GPIO11_I2C3_SCL	165	
GPIO2_I2C1_SDA	184	General purpose I2C
GPIO3_I2C1_SCL	185	
CAM_I2C_SDA1	96	Camera dedicated
CAM_I2C_SCL1	95	
GPIO14_TP_I2C4_SDA	234	General purpose I2C, default for TP
GPIO15_TP_I2C4_SCL	233	
GPIO30_I2C_SDA_8A	254	General purpose I2C
GPIO31_I2C_SCL_8A	253	
GPIO22_I2C6_SDA	259	General purpose I2C
GPIO23_I2C6_SCL	258	

Note: To use the 2.2KΩ pull-up resistor to 1.8V when used as an I2C bus interface, refer to Table 3.1 - I2C Interface.

4.15 Analog to Digital Converter (ADC)

SNM900 module is provided by power management chip with two ADC: adc4 (4Pin) and adc5 (209pin)

The ADC signal is 16 bit resolution, and its performance parameters are as follows:

Table 4.14: ADC Performance Parameters

Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	-	1.8	-	V
ADC Resolution	-	-	15	bits
Analog Input Bandwidth	-	500	-	kHz
Sampling Frequency	-	4.8	-	MHz

4.16. PWM

The PM660L_PWM(112 PIN) pin can be used as a backlight adjustment for the LCD to adjust the backlight brightness by adjusting the duty cycle.

4.17. Motor

The SNM900 supports motor functions and can be implemented by the user via PMI_HAP_OUT_N (8PIN) and PMI_HAP_OUT_P (9PIN). The reference schematic diagram is as follows. Note that the uF-level capacitor cannot be placed on the signal line.

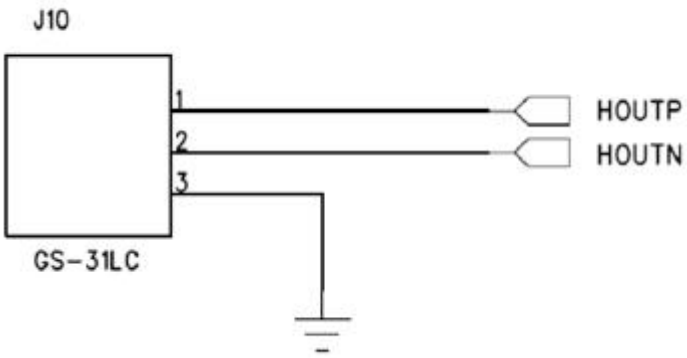


Figure 4.34: Motor interface circuit

4.18 Antenna Interface

The module provides main antenna, DRX antenna, GPS antenna and WiFi / BT_ 5G, WiFi/BT_ 2.4G antenna five antenna interfaces。 In order to ensure that the user's products have good wireless performance, the antenna selected by the user should meet the requirement that the input impedance is 50 ohms in the working frequency band and the VSWR is less than 2.

4.18.1 Main Antenna

The module provides the MAIN antenna interface pin Pin1 RF_MAIN. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

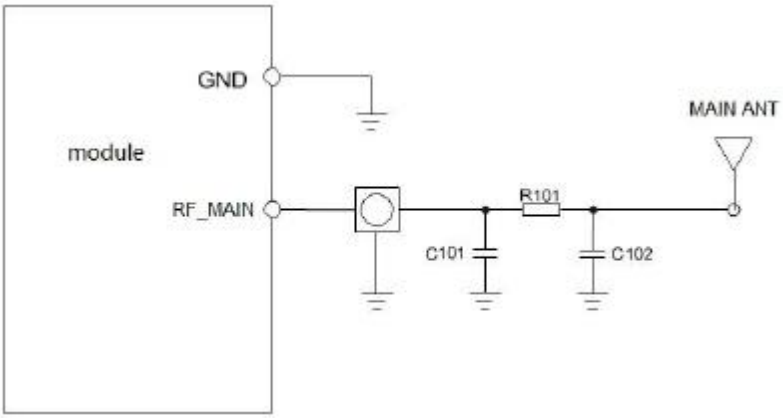


Figure 4.35：MAIN Antenna Interface Connection Circuit

In the figure, R101, C101, and C102 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R101 defaults to 0R, C101 and C102 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

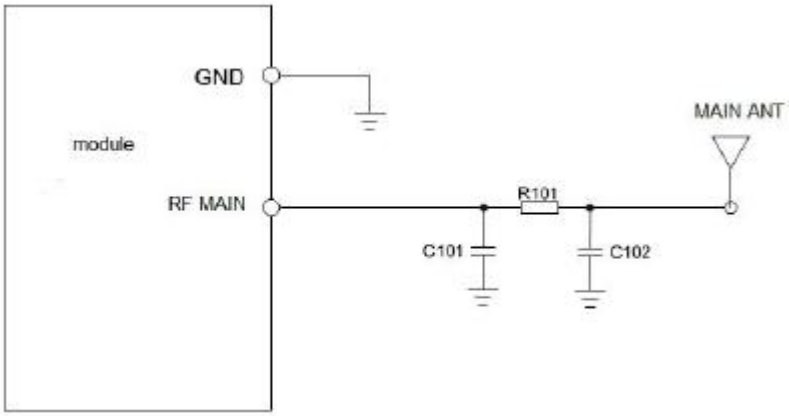


Figure 4.36：MAIN Antenna Interface Simplified Connection Circuit

In the above figure, R101 defaults to 0R, and C101 and C102 do not paste by default.

4.18.2 DRX Antenna

The module provides the DRX antenna interface pin RF_DIV, and the antenna on the user's motherboard should be connected to the module's antenna pins using a 50-ohm characteristic microstrip or stripline.

In order to facilitate antenna debugging and certification testing, an RF connector and

antenna matching network should be added. The recommended circuit diagram is as follows:

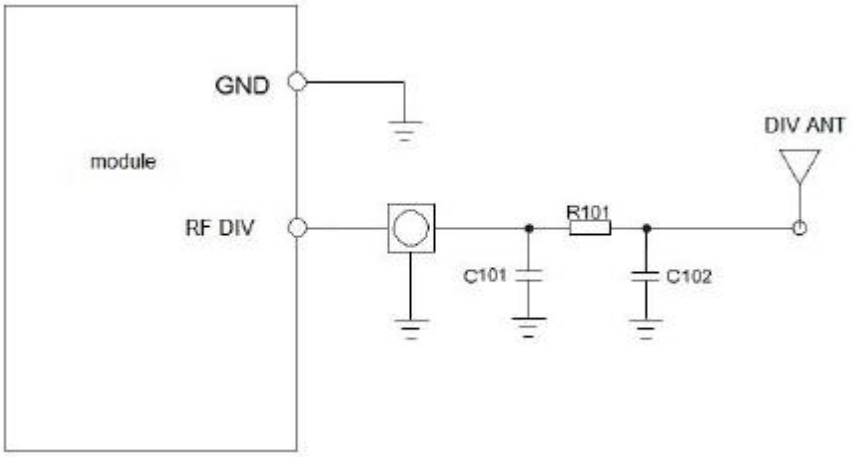


Figure 4.37: DRX antenna interface connection circuit

In the figure, R102, C103, and C104 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R102 defaults to 0R, C103 and C104 are not posted by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

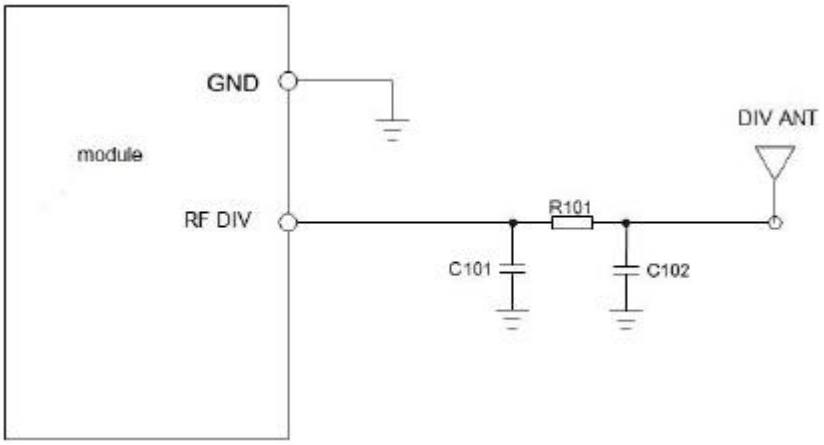


Figure 4.38: DRX Antenna Interface Simplified Connection Circuit

In the above figure, R102 defaults to 0R, C103 and C104 are not attached by default.

4.18.3 GPS Antenna

The module provides the GNSS antenna pin RF_GPS. The antenna on the user's main board should be connected to the antenna pin of the module using a 50-ohm characteristic microstrip line or strip line. The LNA is integrated inside the module.

To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connections are as follows:

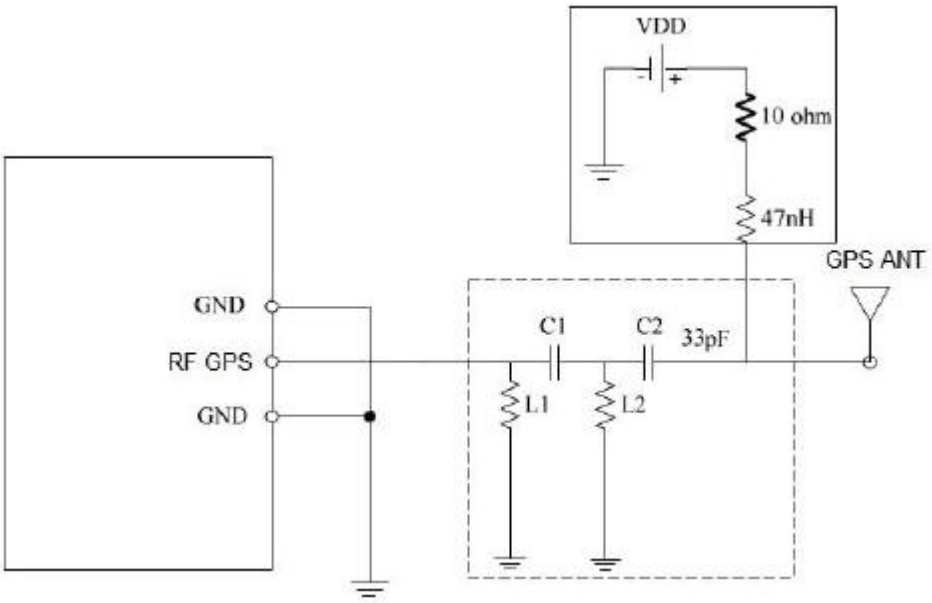


Figure 4.39：Connecting Active Antennas

4.18.4 WiFi/BT antenna

The module provides the WiFi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50 ohm microstrip line or strip line.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

:

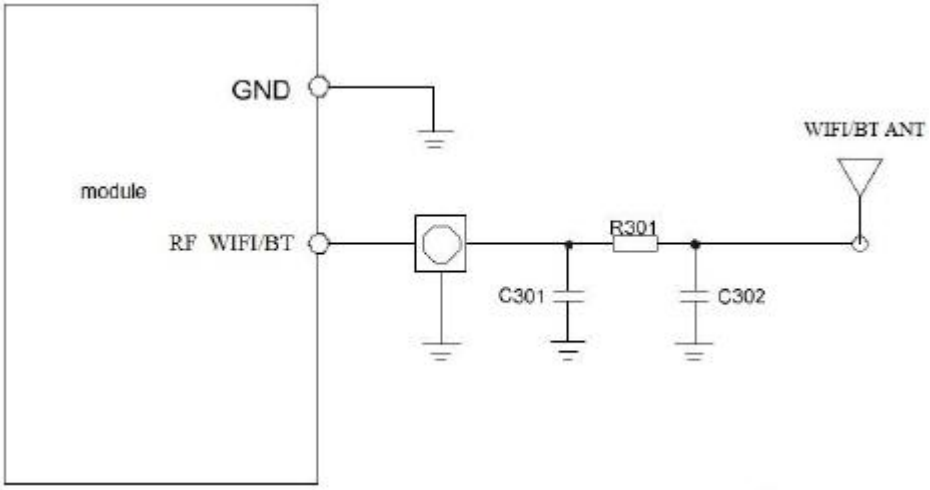


Figure 4.40：WiFI_BT antenna interface connection circuit

In the figure, R301, C301, and C302 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C301 and C302 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

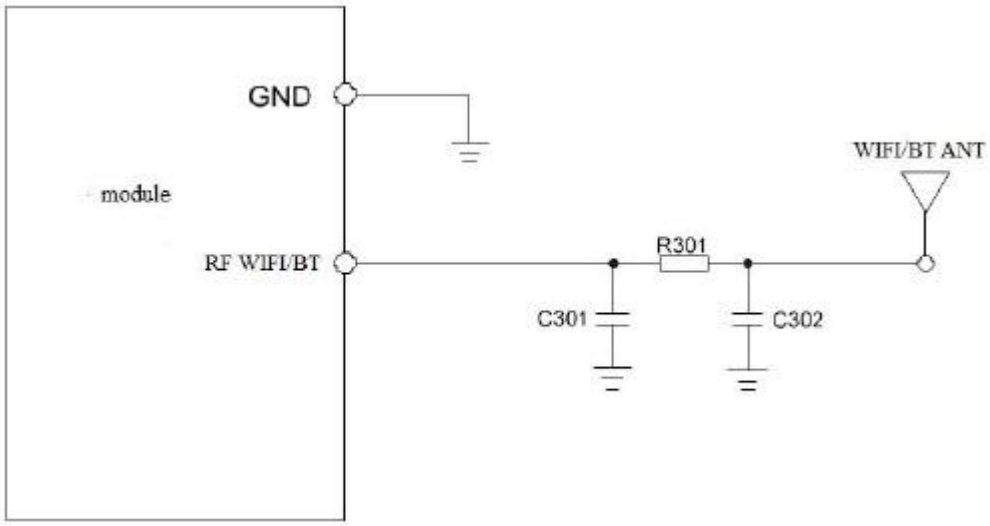


Figure 4.41: WIFI_BT antenna interface simplified connection circuit

In the above figure, R301 defaults to 0R, and C301 and C302 do not paste by default.

5.PCB Layout

The performance of a product depends largely on the PCB trace. As mentioned above, if the PCB layout is unreasonable, it may cause interference problems such as card loss. The way to solve these interferences is often to redesign the PCB. If you can plan a good PCB layout in the early stage, the PCB traces smoothly, saving a lot of time. Of course, it can also save a lot of costs. This chapter mainly introduces some things that users should pay attention to during the PCB layout stage, minimizing interference problems and shortening the user's development cycle.

The SNM900 module is an intelligent module with its own Android operating system. It includes sensitive data lines such as high-speed USB and MIPI. It also has strict requirements on the length and impedance of the signal line. If the high-speed signal processing is not good, it will cause serious EMI. The problem, more serious will also affect the USB identification, LCD display, so the PCB design requirements when using the SNM900 module is much higher than the previous 2G module, please read this chapter carefully, reduce the subsequent hardware debugging cycle.

When using the SNM900 module, the user is required to use at least 4 layers of via holes for the PCB to facilitate impedance control and signal line shielding.

5.1. Module PIN distribution

Before the PCB layout, first understand the pin distribution of the module, and rationally layout the related devices and interfaces according to the distribution defined by the pin. Please refer to Figure 3.1 to determine the distribution of the function feet of the module.

5.2. PCB Layout Principles

Several aspects of the main attention during the PCB layout phase:

5.2.1. Antenna

Antenna part design, SNM900 module has a total of 5 antenna interfaces, they are: RF_MAIN，RF_DIV，GPS_ANT，WIFI_5G_ANT,WIFI_2.4G_ANT.Pay attention to component placement and RF roting :

- The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pins of the module.
- The antenna matching circuit needs to be placed close to the antenna end;
- The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;
- The device and wiring between the antenna pin and the antenna connector of the module must be away from high-speed signal lines and strong interference sources to avoid crossing or parallel with any signal lines in adjacent layers.

- The length of the RF cable between the antenna pin of the module and the antenna connector should be as short as possible. The situation of crossing the entire PCB should be absolutely avoided.
- If the antenna is connected by a coaxial RF line, care should be taken to avoid the coaxial RF line spanning the SIM card, power supply circuit, and high-speed digital circuits to minimize the effects of each other.

5.2.2 Power Supply

Power traces must consider not only VBAT, but also the return GND of the power supply. The trace of the VBAT positive must be short and thick, the trace must first pass through the large capacitor, Zener diode and then the power PIN of the module. There are multiple PAD exposed copper at the bottom of the module. Make sure that the GND path of these exposed copper areas to the power supply is the shortest and smoothest. This ensures that the current path of the entire power supply is the shortest and the interference is minimal.

5.2.3. SIM Card

The SIM card has a large area and does not have an anti-EMI interference device. It is relatively susceptible to interference. Therefore, in the layout, first ensure that the SIM card is away from the antenna and the antenna extension cable inside the product. Place it as close as possible to the module. When the PCB is routed, pay attention to it. The SIM_CLK signal is protected, and the SIM_DATA, SIM_RST, and SIM_VDD signals of the SIM card are away from the power source and away from the high-speed signal line. If the processing is not easy, it may cause problems such as not knowing the card or dropping the card. Therefore, please follow the following principles when designing:

- Keep the SIM card holder away from the GSM antenna during the PCB layout phase;
- SIM card routing should be as far away as possible from RF line, VBAT and high-speed signal lines, and the SIM card should not be too long;
- The GND of the SIM card holder should be in good communication with the GND of the module to make the GND equipotential between the two.
- To prevent SIM_CLK from interfering with other signals, it is recommended to protect SIM_CLK.
- It is recommended to place a 100nF capacitor on the SIM_VDD signal line near the SIM card holder;
- The SIM card signal line increases the capacitance of 22pF to ground to prevent radio frequency interference.
- Place TVS near the SIM card holder. The parasitic capacitance of the TVS should not exceed 50pF, and the 51Ω resistor in series with the module can enhance ESD protection.
- The return path of VBAT has a large current, so the SIM card trace should avoid the return path of VBAT as much as possible.

5.2.4. MIPI

MIPI is a high-speed signal line. Users must pay attention to protection during the layout stage, so that they are away from the signal lines that are easily interfered. The GND processing must be performed on the upper and lower sides, and the traces are differential

pairs. 100 ohm differential impedance matching is performed. Ensure impedance consistency and do not bridge different GND planes as much as possible.

The MIPI interface selects a small-capacity TVS when selecting an ESD device. It is recommended that the parasitic capacitance be less than 1pF.

The MIPI routing requirements are as follows:

- The total length of the cable does not exceed 300mm
- It is required to control 100 ohm differential impedance with an error of ±10%.
- The error of the differential line length within the group is controlled within 0.7mm.
- The length error between groups is controlled within 1.4mm.

5.2.5. USB

The module supports high-speed USB interface at a rate of 480Mbps. The user recommends adding a common-mode inductor during the schematic design phase to effectively suppress EMI interference. If you need to increase the static protection, please select a TVS tube with a parasitic capacitance of less than 1pF. Please refer to the following notes when planning Layout:

- The common mode inductor should be close to the side of the USB connector.
- Requires control of 90 ohm differential impedance with an error of ±10%.
- The differential line length error is controlled within 6mm.
- If the USB has a charging function, please note that the VBUS cable is as wide as possible.
- If there is a test point, try to avoid the split line and put the test point on the path of the trace.

Table 5.1: Internal USB cable length of the module

Pin	Signal	Length (mm)	Length Error（P-N）
146	USB30_HS_DP	40.75	0.66mm
145	USB30_HS_DM	40.09	
230	USB20_HS_DP	19.48	3.56mm
229	USB20_HS_DM	15.92	

5.2.6.Audio

The module supports 3 analog audio signals. Analog signals are susceptible to interference from high speed digital signals. So stay away from high-speed digital signal lines.

The conducted interference is mainly caused by the voltage drop of VBAT. If the Audio PA is directly powered by VBAT, it is easier to hear the “zizi” sound at the SPK output. Therefore, it is better to connect in parallel with the input of the Audio PA in the schematic design. Some large capacitance capacitors and series magnetic beads.

5.2.7. Other

The serial port interface of the module should also be kept as short as possible. It is best to walk in a group when routing, and do not distract the wires.

6. Electrical, Reliability

6.1 Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 6.1: Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	--0.5	-	6	V
VBUS	--0.3	-	16	V
Peak current	-	-	3	A

6.2 Working Temperature

The table below shows the operating temperature range of the module:

Table 6.2: Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	℃
Storage temperature	-40	-	90	℃

6.3 Working Voltage

Table 6.3: Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.5	3.8	4.35	V
VBUS	4	5	9	V

6.4 Digital Interface Features

Table 6.4: Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	1.17	1.8	2.1	V
V_{IL}	Input low level voltage	-0.3	0	0.63	V
V_{OH}	Input high level voltage	1.35	-	1.8	V
V_{OL}	Output low level voltage	0	-	0.45	V

6.5 SIM_VDD Characteristics

Table 6.5: SIM_VDD Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit

V_O	Output voltage	1.65	1.8	1.95	V
		-	2.95	-	
I_O	Output current	-	-	55	mA

6.6 PWRKEY Feature

Table 6.6: PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	2000			ms

6.7 VCOIN Feature

Table 6.7: VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
$VCOIN_{-IN}$	VCOIN input voltage	2.1	3.0	3.25	V
$VCOIN_{-OUT}$	VCOIN Output voltage	-	3.0	-	V

6.8 Current Consumption (VBAT = 3.8V)

Table 6.8: Current consumption

Parameter	Description	Condition	Minimum	Typical	Maximum	Unit
VBAT	voltage	Voltage must be between the maximum and minimum values	3.5	3.8	4.35	V
Ivbat	Average current	Shutdown mode	-	-	100	uA
		GSM Standby power consumption	-	-	4.9	mA
		WCDMA Standby power consumption	-	-	5	mA
		TD-S Standby power consumption	-	-	5	mA
		CDMA Standby power consumption	-	-	4.8	mA
		FDD Standby power consumption			5.8	mA
		TDD Standby power consumption			4.9	mA
	Call Current consumption	GSM900 CH62 32dBm	-	-	290	mA
		WCDMA2100 CH10700 22.5 dBm	-	-	600	mA
	Digital transmission	GPRS GSM900 CH62 PCL5 1DL 4UL	-	-	485	mA
		EGPRS GSM900 CH62 PCL8 1DL 4UL	-	-	440	mA

Imax	Peak current	Power control at maximum output power	-	-	3	A

6.9 Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling, and operating module

6.10 WIFI Main RF Performance

The table below lists the WIFI conduction

Transmission performance(2.4G)				
	802.11B	802.11G	802.11N	
Transmit power (minimum rate)	19	18	17	dBm
Transmit power (maximum rate)	18	16	15	dBm

7. Production

7.1. Top And Bottom Views Of The Module

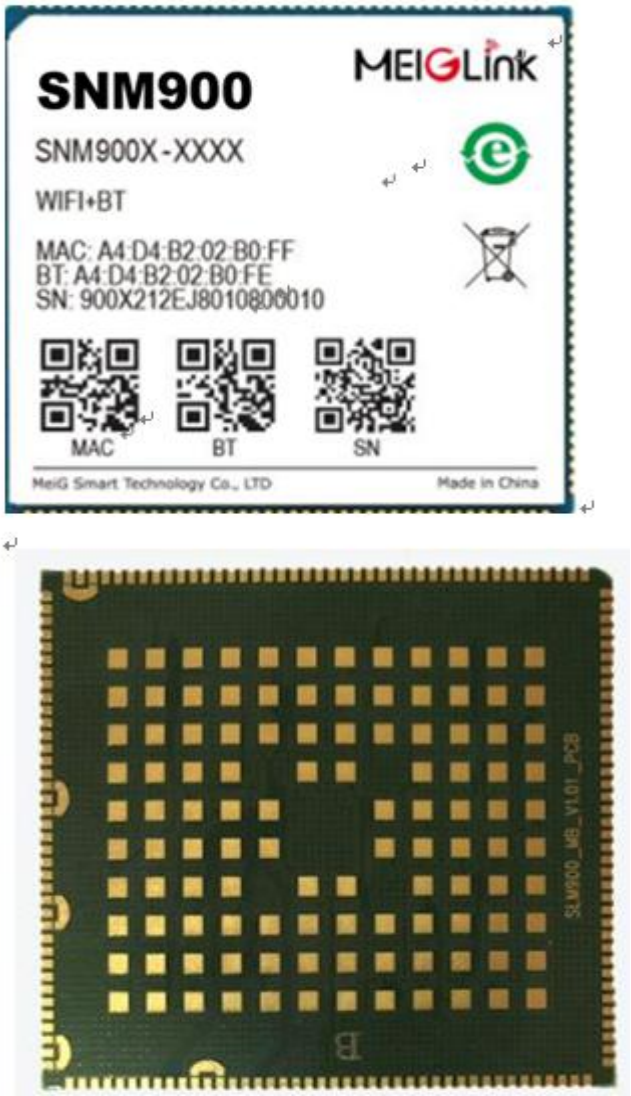


Figure7.1: Module top and bottom views

7.2. Recommended Soldering Furnace Temperature Curve

Figure7.2: Module recommended soldering furnace temperature curve

7.3. Humidity Sensitivity (MSL)

The SNM900 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of temperature <30 degrees and relative humidity <60%. Under ambient conditions of temperature <40 degrees and relative humidity <90%, the shelf life is at least 6 months without unpacking. After unpacking, Table 7.1 lists the shelf life of the modules for different moisture sensitivity levels.

Table 7.1: Humidity sensitivity level distinction

Grade	Factory environment≦+30℃/60%RH
1	Indefinite quality in the environment≦+30℃/85% RH Under conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the time limit specified on the label.

After unpacking, the SMT patch should be taken within 168 hours under ambient conditions of <30 degrees and relative humidity <60%. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solderability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solderability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90°C and as high as 125°C

7.4. Baking Requirements

Due to the humidity sensitivity of the module, the SNM900 should be thoroughly baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SNM900 should be baked for 192 hours in a cryogenic vessel at 40°C +5°C/-0°C and a relative humidity of less than 5%, or in a high temperature vessel at 80°C±5°C.Bake for 72 hours. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 7.2: Baking requirements:

Baking temperature	Humidity	Baking time
40°C±5°C	<5%	192 h
120°C±5°C	<5%	4 h

8. Support Peripheral Device List

SNM900 peripheral devices can support the devices included in the platform QVL. The following are the default software adapter devices.

Table 8.1: List of supported display models

Vendor	Drive IC	Specification
Zoneway	ILI9881P	1280x720

Table 8.2: Support for Camera Model List

Vendor	Drive IC	Specification
Ambitious	s5k3m2xx	13M
Ambitious	s5k4h7	8M
Shun Yu	S5K5E8	5M

Table 8.3: Support for touch screen model list

Vendor	Drive IC	Specification
Zoneway	GT5688	5"

Table 8.4: Support for G Sensor Model List

Vendor	Model	Specification
Bosch	BMI120	9-Axis,16-bit

Table 8.5: Support for Ecompass Model List

Vendor	Model	Specification
AKM	GM303	3-Axis,14-bit

Table 8.6: Support PS/ALS Sensor Model List

Vendor	Model	Specification
LITEON	LTR-553ALS-01	ALS+PS

Table 8.7 Support Gyro Sensor Model List

Vendor	Model	Specification
Bosch	BMI120	9-axis,16bit/16bit

9. Appendix

9.1. Related Documents

Table 9.1: Related documents

Serial number	File name	Comment
[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10:	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05:	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2)；Mobile Station (MS) conformance specification；Part 1：Conformance specification
[8]	AN_Serial Port	AN_Serial Port

9.2. Terms And Explanations

Table 9.2: Terms and explanations

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate

GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

9.3. Multiplexing function

Table 9.3: Multiplexing Functions

GPIO	Module pin	Reuse function		
		SPI	UART	I2C
0	176	MOSI	TXD	
1	177	MISO	RXD	
2	184	CS_N	CTS_N	SDA
3	185	CLK	RFR_N	SCL
4	11	MOSI	TXD	
5	12	MISO	RXD	
6	13	CS_N	CTS_N	SDA
7	14	CLK	RFR_N	SCL
8	232	MOSI		
9	231	MISO		
10	164	CS_N		SDA
11	165	CLK		SCL
12	235	MOSI	TX	
13	/	MISO	RX	
14	234	CS_N	CTS	SDA
15	233	CLK	RTS	SCL
49	261	MOSI		
52	260	MISO		
22	259	CS_N		SDA
23	258	CLK		SCL
24	269	MOSI		
25	268	MISO		
26	267	CS_N		SDA
27	266	CLK		SCL
28	15	MOSI	TXD	
29	16	MISO	RXD	
30	254	CS_N	CTS_N	SDA
31	253	CLK	RFR_N	SCL

Note: Blue is the default function

9.4. Safety Warning

Pay attention to the following safety precautions when using or repairing any terminal or mobile phone that contains modules. The user should be informed of the following safety information on the terminal device. Otherwise, Meig will not be responsible for any consequences caused by the user not following these warning actions.

Table 9.4: Security Warnings

FCC Caution.

§ 15.19 Labelling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§ 15.21 Information to user.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

§ 15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

RF Exposure statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated withmini mum distance 20cm between the radiator & your body

C.Appendix A

A1.Requirement of FCC KDB 996369 D03 for module certification:

1.1List of applicable FCC rules:

The module complies with FCC Part 2, 15B,15C,15E.

1.2Summarize the specific operational use conditions:

SLM320 use the independent GPS chip，includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BeiDou. It supports standard NMEA-0183 protocol.

1.3Limited module procedures:

The module is a Single Modular .

Resolve: Supply example as follows:

Installation Notes:

1) SNM900 Module Power supply range is DC 3.5V~4.2V, when you use SNM900 Module design product, the power supply cannot exceed this range.

2) When connect SNM900 Module to the host device, the host device must be power off.

3) Make sure the module pins correctly installed.

4) Make sure that the module does not allow users to replace or demolition.

5)All types of antennas that can be used with a transmitter：External antenna with maximum gain not Exceeding6.49dBi.

1.4Trace antenna designs: Not applicable.

1.5RF exposure considerations:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated withmini mum distance 20cm between the radiator & your body.

1.6Antennas:

The module does not have a standard antenna.

1.7Label and compliance information

This device complies with part 15 of the FCC Rules. Operation is subject to the condition that this device does not cause harmful interference.Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

Body-worn Operation

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated withmini mum distance 20cm between the radiator & your body The host product Labeling Requirements:

NOTICE: The host product must make sure that FCC labeling requirements are met. This includes clearly visible exterior label on the outside of the final product housing that displays the contents shown in below:

Contains FCC ID:2APJ4-SNM900

1.8Information on test modes and additional testing requirements:

When setting up the configuration, if the pairing and call box options for testing do not work, the tester needs to coordinate with the module manufacturer to access the test mode software.

1.9Additional testing, Part 15 Subpart B disclaimer:

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 2, 15B,15C,15E.) list on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

1.10Information on test modes and additional testing requirements:

When testing, testers need to refer to the user manual, and the sample power supply needs to use a special adapter power supply

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