

SNM970 Hardware Design Manual

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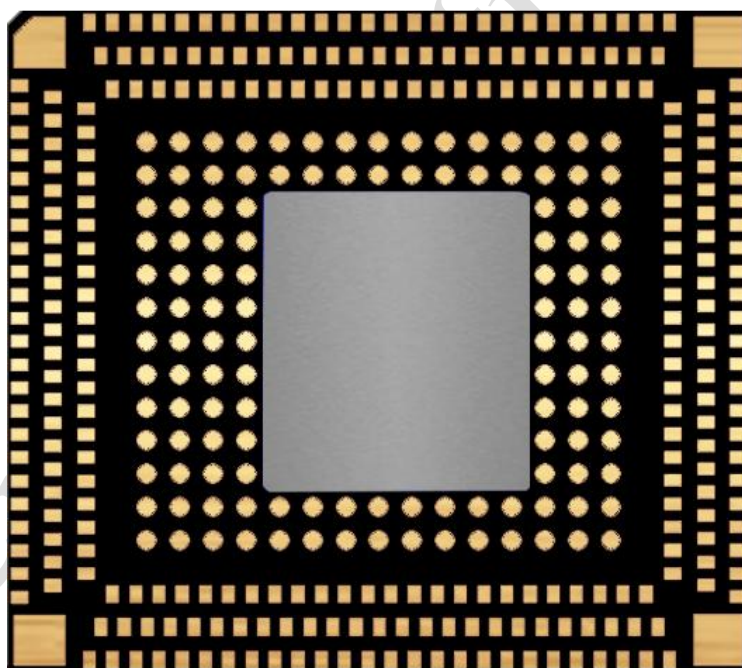
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Identification	Claim
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	GSM mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

SNM970 Hardware Design Guide_V1.00



Foreword

Thank you for using the SNM970 module from Meg Smart. This product can provide data communication services. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

The company does not assume responsibility for property damage or personal injury caused by improper operation of the user. Users are requested to develop the corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety issues that mobile products should focus on.

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Revision History

Date	Revision	Description
2023-04	1.00	First edition
2023-05	1.01	Add BAT_THERM and BAT_ID description
2023-05	1.02	Add PDM functions description
2024-01	1.03	Add BATT_ISNS pins description Update PWM pins description
2024-01	1.04	Add CPU and UFS selection GPIO_155 for BOOT_CONFIG Add GPIO_206 STANDBY description
2024-3	1.05	Update module pin distribution diagram
2024-3	1.06	Add flatness description
2024-6	1.07	Update Volume key mark Add 1.2VGPIO mark

1 Introduction

This document describes the hardware application interface of the module, including the connection of the circuit and the RF interface. It can help users quickly understand the interface definition, electrical performance, and structural dimensions of the module. Combining this document with other application documents, users can quickly use modules to design mobile communication applications.

2 Module overview

SNM970 module uses QCS8550 for main chip based on 4nm FinFET, with 4 × 16 bit ARM and 8-core CPU (1- Kryo Prime: 3.2GHz, 4- Kryo Gold: 2.8GHz, 3- Kryo Silver: 2.0 GHz)*, and supports LPDDR5X SDRAM for memory.

SNM970 (WIFI Only) supports WiFi and BT functions, which can be widely used in VR Camera, Intelligent Robot, Video Surveillance, Security, Vehicle Mounted Devices, Intelligent Platform Handheld Terminals, etc.

The physical interface of the module is a 491- pin pad that provides the following hardware interfaces:

- Six 1.8V UART serial ports, supporting four or two wires (including Debug UART).
- 2 sets of LCD interface (MIPI interface)
- 8 sets of Camera interface (MIPI, one for AON Camera)
- 4 sets of Flashlight interface
- 1 set of USB interface (supports USB2.0 and USB3.1)
- 2 sets of digital MIC interface
- GPIO interface
- 15 sets of I2C interface (3 for sensor, 4 for Camera)
- 4 sets of SPI interface
- 1 set of TF card interface
- 1 set of PCIE 4.0 interface
- Supports WiFi 2.4/5/6/7, Bluetooth 5.3 functions
- 3 sets of RGB interface
- 4 sets of I2S interface (supports 6 wires in 1 set)
- 4 sets of ADC interface

Note: 1. The number of functional interfaces is based on the default function of the pins

2. The “*” sign means that this information is to be confirmed.

2.1 Summary of features

Table 2.1: SNM970 features

Product characteristics		Description
Platform		Qualcomm QCS8550
CPU		Octa-core CPU(optional) AC : no modem; AB : no camera,no modem
GPU		Adreno740
System memory		256GB UFS + 16GB LPDDR5 (Default, compatible with other capacities) 128GB UFS + 12GB LPDDR5(optional)
OS		Android 13
Size		45.0x40.0x3.95mm, LGA 491pin
network band		No support
Wi-Fi		WCN7851-IEEE 802.11a/n/ac/ax/be 2.4G&5G&6G&7G
Bluetooth		BT 5.3
GNSS		No support
Data Access	TD-LTE	No support
	FDD-LTE	No support
	DC-HSPA+	No support
	TD-HSPA	No support
	EVDO Rev.A	No support
	EDGE	No support
	GPRS	No support
SIM		No support
Display		Matrix: HD+: 3480 × 2160 at 120 Hz, 3360 × 1600 at 144 Hz
		LCD Size: User defined
		Interface: 2st LCM: MIPI DSI 4-lane;
Camera (Front and Rear)		Interface:8 sets of 4-Lane CSI (CSI4 for AON Camera)
		(36 M + 36 M + 36 M) @ 30 fps - triple camera
		(64 M + 36 M) @ 30 fps - dual camera
		108 M @ 30 fps - single cameras
Video	Video decode	4K@240fps or 8K@60fps H.264/H.265/VP9
	Video encode	4K@120fps or 8K@30fps H.264/H.265
	Decode + Encode	4K60 Decode + 4K60 Encode
Input Device		Key (Power on/off, Reset, Home, Volume+, Volume-)
		Capacitive TP
Reset		Support HW reset
Application interface	Interface name	Main function description
	VBAT	6pin, Power input, 3.5V ~ 4.2V, Nominal value 3.8V
	SDIO *1	SD3.0
	USB2.0(3.1)	Support OTG

		USB_BOOT (Force USB boot for emergency downloads)
	BLSP ports	8 QUP ports+4 SSC_QUP ports, multiplexed serial interface functions
	ADC*4	Support
	Charge	Support (QC5.0)
	Vibrator	No support
	GPIO	55 GPIOs, Excluding QUP multiplexed GPIOs and GPIOs involved in LCM, TP, CAMERA
	VCOIN	Real time clock backup battery
	RF Interface	2.4G WiFi/BT antenna 5G/6G/7G WIFI-antenna
	Audio	2 sets of digital MIC 4 sets of I2S interface

2.2 Block diagram

The following figure lists the main functional parts of the module:

- QCS8550 -- Baseband chip
- PM8550, PM8550VS*4, PM8550VE*1, PM8550BH, PMK8550 -- Power management chip
- WCN7851 -- WCN chip
- Antenna interface
- LCD/CAM-MIPI interface
- PCIe interface
- UFS memory chip
- Serial ports, SD card interface, USB interface, AUDIO interface, etc.

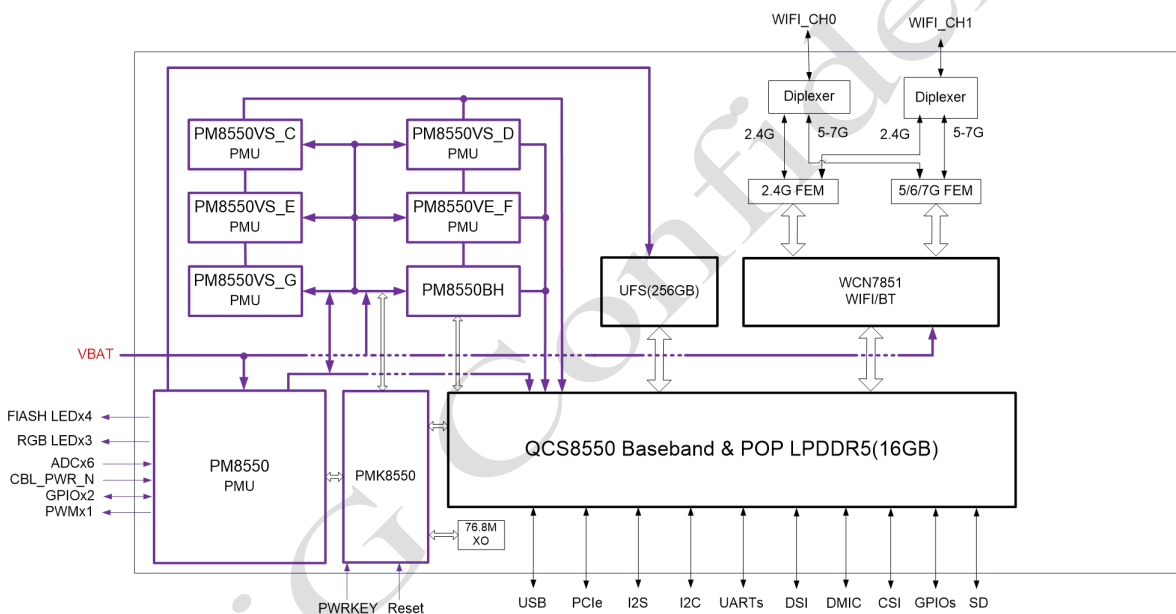


Figure 2.1: Module function block diagram

3 Module Package

3.1 Pin distribution diagram

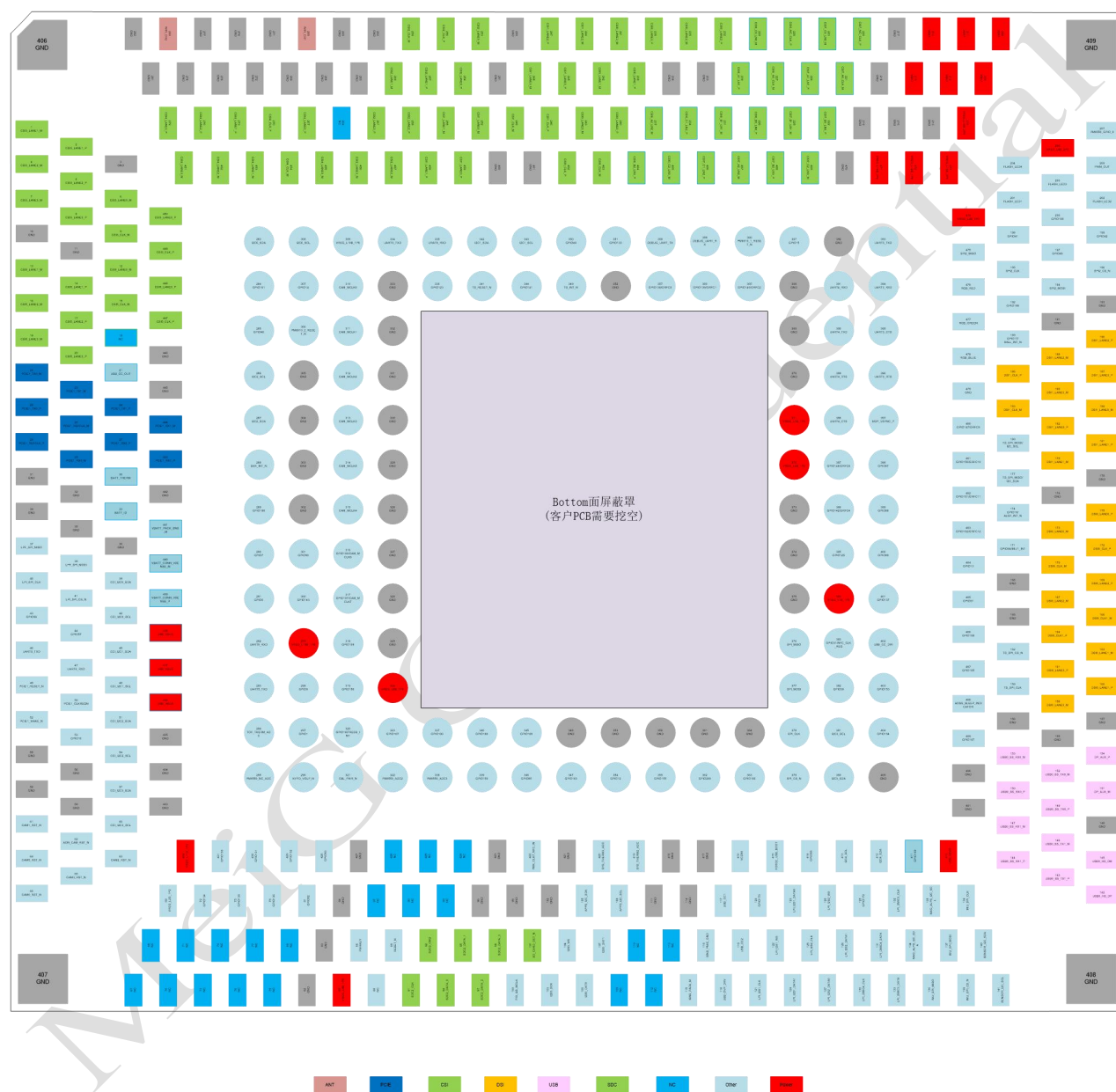


Figure 3.1: Module pin diagram (top view)

3.2 Pin definitions

Table 3.1: Pin description (GPIOs with ‘*’ support INT)

引脚名称	引脚序号	I/O	描述	备注
Power supply				
VBAT	208, 209 211, 212 214, 215	PI	The module provides six VBAT power pin pins. The SNM970 operates from a single supply with a voltage range from 3.5V to 4.2V for VBAT.	Externally, large capacitors and Zener diodes must be added for surge protection.
USB_VBUS	410, 436, 437, 438	PI, PO	USB_VBUS supports QC5.0 fast charge function with a voltage range from 3.7V to 21.5V.	
VCOIN	416	AI/AO	When the VBAT of the system power is absent, the external backup battery provides power to the system real-time clock. When VBAT is present, the backup battery is charged.	VCOIN pins connect 3V button batteries or large capacitors.
VREG_L9B_2P9	206	PO	1.8/2.95V power output, used for SD card power supply	600mA
VREG_L8B_1P8	85	PO	1.8/2.95V power output, used for SD card signal pull-up power supply	50mA
VREG_L6B_1P8	324	PO	Reserved	250mA
VREG_L16B_2P8	210	PO	Reserved	100mA
VREG_L2G_1P2	69	PO	1.2V power output, used for CAM DVDD power supply	300mA
VREG_L11B_1P2	432	PO	1.2V power output, used for CAM DVDD power supply	300mA
VREG_L10B_1P8	309	PO	Reserved	250mA
VREG_L7B_1P8	371	PO	Reserved	250mA
VREG_L4B_1P8	372	PO	Reserved	250mA
VREG_L15B_1P8	299	PO	1.8V power output, power-on supply, used for signal pull-up and level shifting circuit	100mA

VREG_L1B_1P8	384	PO	1.8V power output, power-on supply, used for Sensor I/O power supply	200mA
VREG_L12B_1P8	472	PO	1.8V power output, power-on supply, used for LCD power supply	100mA
VREG_L14B_3P2	471	PO	3.0V power output, used for TP power supply	100mA
VREG_L13B_3P0	473	PO	3.0V power output, used for LCD power supply	100 mA
VREG_L2B_3P0	474	PO	3.0V power output, used for Sensor power supply	250 mA
NC	18, 67, 68, 70, 71, 73, 74, 76, 77, 79, 80, 87, 88, 90, 93, 109, 110, 112, 113, 264, 424-426		Floating	
GND	3, 10-11, 31-32, 34-36, 55-56, 58-59, 82-84, 96, 99, 102, 111, 114, 148, 155-157, 165, 168, 176, 178, 191, 193, 213, 216-219, 233, 236, 250-251, 262-263, 265-266, 269, 271-272, 274-275, 277-278, 281-282, 302-305, 325-333, 348, 352-353, 356, 361, 364, 368-369, 370, 373-375, 392, 405-409, 417, 418, 421, 423, 427, 433-435, 442, 445-446, 460-461, 470, 479, 490-491		GND	
Main display interface (MIPI)				
MIPI_DSI0_CLK_N	170	AO	MIPI_LCD clock	
MIPI_DSI0_CLK_P	172	AO		

MIPI_DSI0_LANE0_N	173	AO	MIPI_LCD data	
MIPI_DSI0_LANE0_P	175	AO		
MIPI_DSI0_LANE1_N	163	AO		
MIPI_DSI0_LANE1_P	160	AO		
MIPI_DSI0_LANE3_N	158	AO		
MIPI_DSI0_LANE3_P	161	AO		
MIPI_DSI0_LANE2_N	167	AO		
MIPI_DSI0_LANE2_P	169	AO		
MIPI_DSI0_CLK1_N	166	AO	DSI split link	
MIPI_DSI0_CLK1_P	164	AO		
GPIO133/DISP0_RESET_N	351	I/O	LCD reset	
GPIO86*_MDP_VSYNC_P	397	I/O	LCD frame sync signal	
Sub display interface (MIPI)				
MIPI_DSI1_CLK_N	183	AO	MIPI_LCD clock	
MIPI_DSI1_CLK_P	186	AO		
MIPI_DSI1_LANE0_N	184	AO	MIPI_LCD data	
MIPI_DSI1_LANE0_P	182	AO		
MIPI_DSI1_LANE1_N	179	AO		
MIPI_DSI1_LANE1_P	181	AO		
MIPI_DSI1_LANE3_N	185	AO		
MIPI_DSI1_LANE3_P	187	AO		
MIPI_DSI1_LANE2_N	188	AO		
MIPI_DSI1_LANE2_P	190	AO		
GPIO87*_MDP1_VSYNC_S	398	I/O	LCD frame sync signal	
Main display backlight interface				
PM8550_PWM_OUT_GPIO9	205	I/O	Backlight chip PWM	
UART (1.8V)				
DEBUG_RX	359	DI	UART data receive	DEBUG UART
DEBUG_TX	358	DO	UART data transmit	
GPIO51*_UART0_RXD	335	DI	UART data receive	
GPIO50_UART0_TXD	334	DO	UART data transmit	

GPIO75*_UART5_RXD	292	DI	UART data receive	BOOTCONFIG, do not pull-up before power-on
GPIO74_UART5_TXD	293	DO	UART data transmit	
GPIO59*_UART6_RX	47	DI	UART data receive	
GPIO58_UART6_TX	46	DO	UART data transmit	
GPIO71*_UART4_RXD	391	DI	UART data receive	
GPIO70_UART4_TXD	390	DO	UART data transmit	
GPIO68_UART4_CTS	388	DI	UART data transmit	
GPIO69_UART4_RTS	389	DO	UART data transmit	
GPIO63*_UART3_RXD	394	DI	UART data receive	
GPIO62*_UART3_TXD	393	DO	UART data transmit	
GPIO60_UART3_CTS	395	DI	UART data transmit	
GPIO61_UART3_RTS	396	DO	UART data transmit	
Camera0				
MIPI_CSI0_CLK_N	463	AO	Camera0 MIPI clock	
MIPI_CSI0_CLK_P	462	AO		
MIPI_CSI0_LANE0_N	243	AI/AO	Camera0 MIPI data	
MIPI_CSI0_LANE0_P	240	AI/AO		
MIPI_CSI0_LANE1_N	242	AI/AO		
MIPI_CSI0_LANE1_P	239	AI/AO		
MIPI_CSI0_LANE2_N	235	AI/AO		
MIPI_CSI0_LANE2_P	232	AI/AO		
MIPI_CSI0_LANE3_N	241	AI/AO		
MIPI_CSI0_LANE3_P	238	AI/AO		
CAM_MCLK0	310	DO	Camera0 main clock	
CAM0_RST_N	66	DO	Camera0 reset	
GPIO143_CAM0_PWD_N	300	DO	Camera0 dormancy	
Camera1				
MIPI_CSI1_CLK_N	249	AO	Camera1 MIPI clock	
MIPI_CSI1_CLK_P	246	AO		
MIPI_CSI1_LANE0_N	252	AI/AO	Camera1 MIPI data	

MIPI_CSI1_LANE0_P	459	AI/AO		
MIPI_CSI1_LANE1_N	255	AI/AO		
MIPI_CSI1_LANE1_P	458	AI/AO		
MIPI_CSI1_LANE2_N	244	AI/AO		
MIPI_CSI1_LANE2_P	247	AI/AO		
MIPI_CSI1_LANE3_N	248	AI/AO		
MIPI_CSI1_LANE3_P	245	AI/AO		
CAM_MCLK1	311	DO	Camera1 main clock	
CAM1_RST_N	61	DO	Camera1 reset	
GPIO90_CAM1_PWD_N	301	DO	Camera1 dormancy	
Camera2				
MIPI_CSI2_CLK_N	259	AO	Camera2 clock	
MIPI_CSI2_CLK_P	256	AO		
MIPI_CSI2_LANE0_N	253	AI/AO	Camera2 data	
MIPI_CSI2_LANE0_P	254	AI/AO		
MIPI_CSI2_LANE1_N	260	AI/AO		
MIPI_CSI2_LANE1_P	257	AI/AO		
MIPI_CSI2_LANE2_N	457	AI/AO		
MIPI_CSI2_LANE2_P	258	AI/AO		
MIPI_CSI2_LANE3_N	456	AI/AO		
MIPI_CSI2_LANE3_P	261	AI/AO		
CAM_MCLK2	312	DO	Camera2 main clock	
GPIO118_CAM2_RST_N	63	DO	Camera2 reset	
GPIO125	385	DO	Camera2 dormancy	
Camera3				
MIPI_CSI3_CLK_N	9	AO	Camera3 clock	
MIPI_CSI3_CLK_P	449	AO		
MIPI_CSI3_LANE0_N	6	AI/AO	Camera3 MIPI data	
MIPI_CSI3_LANE0_P	450	AI/AO		
MIPI_CSI3_LANE1_N	1	AI/AO		
MIPI_CSI3_LANE1_P	2	AI/AO		

MIPI_CSI3_LANE2_N	4	AI/AO		
MIPI_CSI3_LANE2_P	5	AI/AO		
MIPI_CSI3_LANE3_N	7	AI/AO		
MIPI_CSI3_LANE3_P	8	AI/AO		
CAM_MCLK3	313	DO	Camera3 main clock	
CAM3_RST_N	65	DO	Camera3 reset	
GPIO159*_CAM3_PWD_N	339	DO	Camera3 dormancy	
Camera4 (AON_CAM)				
MIPI_CSI4_CLK_N	454	AO	Camera4 clock	
MIPI_CSI4_CLK_P	270	AO		
MIPI_CSI4_LANE0_N	455	AI/AO	Camera4 MIPI clock	
MIPI_CSI4_LANE0_P	267	AI/AO		
MIPI_CSI4_LANE1_N	453	AI/AO		
MIPI_CSI4_LANE1_P	273	AI/AO		
MIPI_CSI4_LANE2_N	452	AI/AO		
MIPI_CSI4_LANE2_P	276	AI/AO		
MIPI_CSI4_LANE3_N	451	AI/AO		
MIPI_CSI4_LANE3_P	279	AI/AO		
CAM_MCLK4	315	DO	Camera4 main clock	
AON_CAM_RESET_N	62	DO	Camera4 reset, under development	
GPIO40*_CAM4_PWD_N	197	DO	Camera4 dormancy	Use GPIO_206 for AON function
Camera5				
MIPI_CSI5_CLK_N	15	AO	Camera5 clock	
MIPI_CSI5_CLK_P	447	AO		
MIPI_CSI5_LANE0_N	12	AI/AO	Camera5 data	
MIPI_CSI5_LANE0_P	448	AI/AO		
MIPI_CSI5_LANE1_N	13	AI/AO		
MIPI_CSI5_LANE1_P	14	AI/AO		
MIPI_CSI5_LANE2_N	16	AI/AO		
MIPI_CSI5_LANE2_P	17	AI/AO		

MIPI_CSI5_LANE3_N	19	AI/AO		
MIPI_CSI5_LANE3_P	20	AI/AO		
CAM_MCLK5	314	DO	Camera5 main clock	
GPIO144_CAM5_RST_N	64	DO	Camera5 reset	
GPIO125	385	DO	Camera5 dormancy	
Camera6				
MIPI_CSI6_CLK_N	227	AO	Camera6 clock	
MIPI_CSI6_CLK_P	226	AO		
MIPI_CSI6_LANE0_N	229	AI/AO	Camera6 data	
MIPI_CSI6_LANE0_P	228	AI/AO		
MIPI_CSI6_LANE1_N	231	AI/AO		
MIPI_CSI6_LANE1_P	230	AI/AO		
MIPI_CSI6_LANE2_N	237	AI/AO		
MIPI_CSI6_LANE2_P	234	AI/AO		
MIPI_CSI6_LANE3_N	465	AI/AO		
MIPI_CSI6_LANE3_P	464	AI/AO		
CAM_MCLK6	316	DO	Camera6 main clock	
GPIO42	199	I/O	Camera6 reset	
GPIO108	200	I/O	Camera6 dormancy	
Camera7				
MIPI_CSI7_CLK_N	221	AO	Camera7 clock	
MIPI_CSI7_CLK_P	220	AO		
MIPI_CSI7_LANE0_N	223	AI/AO	Camera7 data	
MIPI_CSI7_LANE0_P	222	AI/AO		
MIPI_CSI7_LANE1_N	225	AI/AO		
MIPI_CSI7_LANE1_P	224	AI/AO		
MIPI_CSI7_LANE2_N	467	AI/AO		
MIPI_CSI7_LANE2_P	466	AI/AO		
MIPI_CSI7_LANE3_N	469	AI/AO		
MIPI_CSI7_LANE3_P	468	AI/AO		
CAM_MCLK7	317	DO	Camera7 main clock	

GPIO56	43	I/O	Camera7 reset	
GPIO57	44	I/O	Camera7 dormancy	
PCIE				
PCIE1_TX0_M	22	AO	PCIE1 differential data	
PCIE1_TX0_P	25	AO		
PCIE1_RX0_M	29	AI		
PCIE1_RX0_P	27	AI		
PCIE1_TX1_M	23	AO		
PCIE1_TX1_P	24	AO		
PCIE1_RX1_M	444	AI		
PCIE1_RX1_P	443	AI		
PCIE1_REFCLK_M	26	AO	PCIE differential clock	
PCIE1_REFCLK_P	28	AO		
GPIO97/PCIE1_RESET_N	49	DO	PCIE1 reset	
GPIO98*/PCIE1_CLKREQN	50	DO	PCIE1 clock require	
GPIO99*/PCIE1_WAKE_N	52	AO	PCIE1 wake-up	
SD card interface				
SD_CARD_DET_N	101	DI	SD card insertion detection, can't be used for GPIO	
SDC2_SDCARD_CMD	92	DO	SD CMD	
SDC2_SDCARD_CLK	91	DO	SD clock	
SDC2_SDCARD_D0	94	I/O	SD data	
SDC2_SDCARD_D1	95	I/O		
SDC2_SDCARD_D2	97	I/O		
SDC2_SDCARD_D3	98	I/O		
I2C				
CCI_I2C0_SDA	39	OD	CAM-specific I2C signals	For CSI0/1
CCI_I2C0_SCL	42	OD		
CCI_I2C1_SDA	45	OD	CAM-specific I2C signals	For CSI2
CCI_I2C1_SCL	48	OD		
CCI_I2C2_SDA	51	OD	CAM-specific I2C signals	For CSI3

CCI_I2C2_SCL	54	OD		
GPIO208/CCI_I2C3_SDA	57	OD	CAM-specific I2C signals	Only for CSI4(AON CAM (Always on Camera))
GPIO209/CCI_I2C3_SCL	60	OD		
APPS_I2C_SDA	105	OD	Generic I2C	
APPS_I2C_SCL	108	OD		
MAG_ALPS_I2C_SDA	134	OD	I2C for Sensor	For MAG/ALPS
MAG_ALPS_I2C_SCL	135	OD		
SENSOR_I2C_SDA	140	OD	I2C for Sensor	For SAR/Pressure
SENSOR_I2C_SCL	141	OD		
GPIO188*/I2C_SDA	340	OD	I2C for Sensor	For ACCEL/GYRO
GPIO189/I2C_SDL	345	OD		
GPIO4/I2C1_SDA	342	OD	Generic I2C	
GPIO5/I2C1_SCL	343	OD		
GPIO8*/I2C2_SDA	283	OD	Generic I2C	
GPIO9*/I2C2_SCL	308	OD		
GPIO28*/I2C3_SDA	380	OD	Generic I2C	
GPIO29/I2C3_SCL	381	OD		
GPIO206*/I2C4_SDA	412	OD	Generic I2C	AON CAM: Standby
GPIO207*/I2C4_SCL	413	OD		
GPIO6/I2C5_SDA	291	OD	Generic I2C	
GPIO7/I2C5_SCL	290	OD		
GPIO22/I2C6_SDA	287	OD	Generic I2C	
GPIO23/I2C6_SCL	286	OD		
SPI				
GPIO32*/SPI1_MISO	376	DI	Generic SPI	
GPIO33/SPI1_MOSI	377	DO		
GPIO34/SPI1_CLK	378	DO		
GPIO35*/SPI1_CS_N	379	DO		
GPIO36/SPI2_MISO	475	DI	Generic SPI	
GPIO37/SPI2_MOSI	194	DO		

GPIO38/SPI2_CLK	195	DO	Generic SPI	
GPIO39*/SPI2_CS_N	196	DO		
GPIO64/LPF_SPI_MISO	37	DI		
GPIO65/LPF_SPI_MOSI	38	DO		
GPIO66/LPF_SPI_CLK	40	DO		
GPIO67*/LPF_SPI_CS_N	41	DO		
IMU_SPI_MISO	136	DI	Specific SPI	For ACCEL/GYRO
IMU_SPI_MOSI	137	DO		
IMU_SPI_CLK	138	DO		
IMU_SPI_CS_N	139	DO		
I2S				
I2S0_SCK	103	DO	Generic I2S	
I2S0_WS	104	DO		
I2S0_DATA0	106	I/O		
I2S0_DATA1	107	I/O		
LPI_I2S1_CLK	121	DO	Generic I2S	Multiplexing PDM, CLK
LPI_I2S1_WS	122	DO		Multiplexing PDM, DAT
LPI_I2S1_DATA0	123	I/O		Multiplexing PDM, CLK
LPI_I2S1_DATA1	124	I/O		Multiplexing PDM, DAT
LPI_I2S2_CLK	125	DO	Generic I2S	
LPI_I2S2_WS	126	DO		
LPI_I2S2_DATA0	127	I/O		
LPI_I2S2_DATA1	128	I/O		
GPIO170_LPI_I2S0_DATA3	120	I/O	Generic I2S	
GPIO166*_LPI_I2S0_WS	363	DO		
GPIO169_LPI_I2S0_DATA2	411	I/O		
GPIO168_LPI_I2S0_DATA1	486	I/O		
GPIO165_LPI_I2S0_SCK	487	DO		
GPIO167_LPI_I2S0_DATA0	489	I/O		
PRI_I2S_MCLK	100	DO	Primary I2S main clock	

TP				
GPIO44/TS_SPI_MISO_I2C_SDA	177	I/O	TP_SPI clock, Multiplexing TP_I2C data	
GPIO45/TS_SPI_MOSI_I2C_SCL	180	I/O	TP_SPI chip-select, Multiplexing TP_I2C clock	
GPIO46/TS_SPI_CLK	159	DO	TP_SPI clock	
GPIO47*/TS_SPI_CS_N	162	DO	TP_SPI chip-select	
GPIO25*/TS_INT_N	349	DI	TP interrupt	
GPIO24/TS_RESET_N	341	DO	TP reset	
USB				
USB0_HS_DM	145	AI/AO	USB 2.0 D-	
USB0_HS_DP	142	AI/AO	USB 2.0 D+	
USB0_SS_TX0_P	149	AI/AO	USB super-speed 0 transmit – plus	
USB0_SS_TX0_M	152	AI/AO	USB super-speed 0 transmit – minus	
USB0_SS_TX1_M	146	AI/AO	USB super-speed 1 transmit – minus	
USB0_SS_TX1_P	143	AI/AO	USB super-speed 1 transmit – plus	
USB0_SS_RX0_M	153	AI/AO	USB super-speed 0 receive – minus	
USB0_SS_RX0_P	150	AI/AO	USB super-speed 0 receive – plus	
USB0_SS_RX1_P	144	AI/AO	USB super-speed 1 receive – plus	
USB0_SS_RX1_M	147	AI/AO	USB super-speed 1 receive – minus	
DP_AUX_M	151	AI/AO	DP auxiliary differential signal	
DP_AUX_P	154	AI/AO	DP auxiliary differential signal	
Antenna interface				
WIFI_CH0	268	AI/AO	WIFI/BT antenna	
WIFI_CH1	280	AI/AO	WIFI/BT antenna	
GPIO default function				
GPIO41*	198	I/O	Generic GPIO	
GPIO10	53	I/O	Generic GPIO	

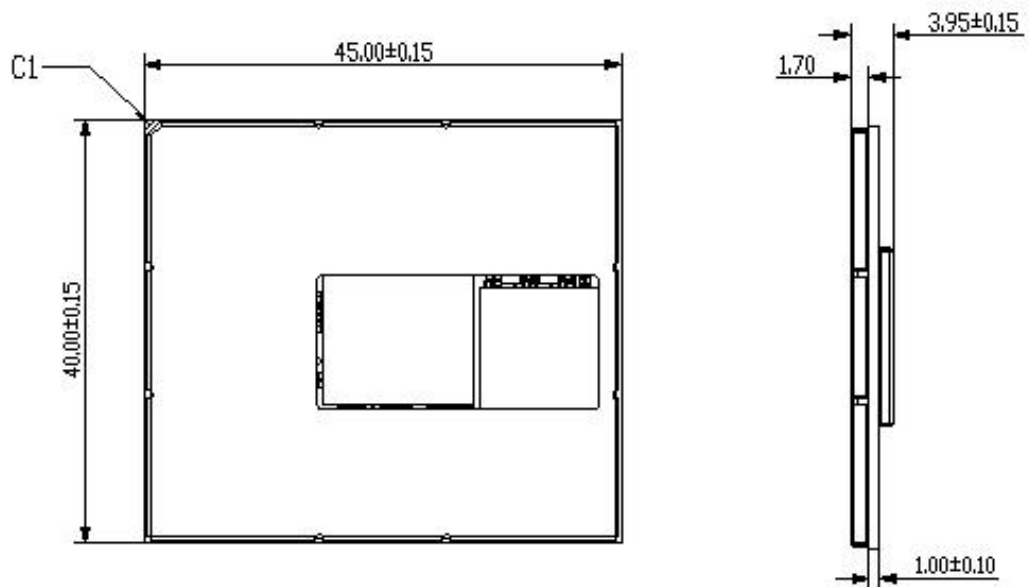
GPIO134	72	I/O	Generic GPIO, with 1.2V voltage range.	
GPIO135	75	I/O	Generic GPIO, with 1.2V voltage range.	
GPIO136	78	I/O	Generic GPIO, with 1.2V voltage range.	
GPIO52	81	I/O	Generic GPIO	
GPIO199*	192	I/O	Generic GPIO	
GPIO161	284	I/O	Generic GPIO	BOOTCONFIG, do not pull-up before power-on
GPIO48	285	I/O	Generic GPIO	
GPIO198*	289	I/O	Generic GPIO	
GPIO14*	307	I/O	Generic GPIO	
GPIO109	318	I/O	Generic GPIO	
GPIO156*	319	I/O	Generic GPIO	
GPIO187*	323	I/O	Generic GPIO	
GPIO123	336	I/O	Generic GPIO	
GPIO186	337	I/O	Generic GPIO	
GPIO141	344	I/O	Generic GPIO	
GPIO85*	346	I/O	Generic GPIO	
GPIO163	347	I/O	Generic GPIO	
GPIO12	354	I/O	Generic GPIO	
GPIO155	355	I/O	Generic GPIO	BOOTCONFIG, do not pull-up before power-on
GPIO200	362	I/O	Generic GPIO	
GPIO15*	367	I/O	Generic GPIO	
GPIO30	382	I/O	Generic GPIO	
GPIO88*	399	I/O	Generic GPIO	
GPIO137*	401	I/O	Generic GPIO	
GPIO153*	403	I/O	Generic GPIO	BOOTCONFIG, do not pull-up before power-on
GPIO154*	404	I/O	Generic GPIO	BOOTCONFIG, do not pull-up before power-on
GPIO55*	414	I/O	Generic GPIO	

GPIO93	428	I/O	Generic GPIO	
GPIO132	429	I/O	Generic GPIO (1.2V)	(1.2V) GPIO
GPIO131	430	I/O	Generic GPIO (1.2V)	(1.2V) GPIO
GPIO130	431	I/O	Generic GPIO (1.2V)	(1.2V) GPIO
PM8550_GPIO_11	207	I/O	PM8550 Generic GPIO	
GPIO1	297	I/O	Generic GPIO	
GPIO0	298	I/O	Generic GPIO	
GPIO170/EXT_MCLK1_C	120	I/O	Generic GPIO, Multiplexed as external clock signal 1C	Multiplexed as 6-lane LPI_I2S0
GPIO179/EXT_MCLK1_D	129	I/O	Generic GPIO, Multiplexed as external clock signal 1D	
GPIO84*/IMU1_INT	171	I/O	Generic GPIO, used for IMU1 interrupt by default	
GPIO16*/ALSP_INT_N	174	I/O	Generic GPIO, used for ALSP interrupt by default	
GPIO17*/HALL_INT_N	189	I/O	Generic GPIO, used for HALL interrupt by default	
GPIO19*/SAR_INT_N	288	I/O	Generic GPIO, used for SAR interrupt by default	
GPIO18*/PRESS_INT	320	I/O	PRESS interrupt	
GPIO49/WSA0_EN	350	I/O	Generic GPIO, used for WSA0 enable by default	
GPIO138/GRFC0	357	I/O	RF GPIO	
GPIO139/GRFC1	360	I/O	RF GPIO	
GPIO140/GRFC2	365	I/O	RF GPIO	
GPIO31*/NFC_CLK_REQ	383	I/O	Generic GPIO, used for NFC clock require by default	
GPIO142/GRFC4	386	I/O	RF GPIO	
GPIO146/GRFC8	387	I/O	RF GPIO	
GPIO89*/WSA1_EN	400	I/O	Generic GPIO, used for WSA1 enable by default	
GPIO147/GRFC9	480	I/O	RF GPIO	
GPIO150*/GRFC10	481	I/O	RF GPIO	BOOTCONFIG, do not pull-up before power-on
GPIO151/GRFC11	482	I/O	RF GPIO	BOOTCONFIG, do not pull-up before power-on

GPIO152/GRFC12	483	I/O	RF GPIO	BOOTCONFIG, do not pull-up before power-on
GPIO13	484	I/O	Generic GPIO	
GPIO91	485	I/O	Generic GPIO	
Other functional pins				
USB_CC_DIR	402	I/O	Connect the two pins using 0R resistors	
USB_CC_OUT	21	DO		
PWRKEY	86	DI	Module power on/off key	
BATT_THERM	30		BATT_THERM	
BATT_ID	33		BATT_ID	
RESET_N	89	DI	Module reset key	
ISNS_PACK_M	115		BATT_ISNS_PACK_M	
ISNS_PMIC_GND	116		BATT_ISNS_PMIC_GND	
USB_CC1	117	AI	USB_CC1	
USB_OVP_DRV	118	DO	External OVP chip control signal	
USB_CC2	119	AI	USB_CC2	
LPI_DMIC4_CLK	130	I/O	LPI_DMIC4 clock	Multiplexing PDM, CLK
LPI_DMIC4_DATA	131	I/O	LPI_DMIC4 data	Multiplexing PDM, DAT
LPI_DMIC3_CLK	132	I/O	LPI_DMIC3 clock	Multiplexing PDM, CLK
LPI_DMIC3_DATA	133	I/O	LPI_DMIC3 data	Multiplexing PDM, DAT
FLASH_LED1	201	DO	Flash 1 output+	
FLASH_LED2	202	DO	Flash 2 output+	
FLASH_LED3	203	DO	Flash 3 output+	
FLASH_LED4	204	DO	Flash 4 output+	
TOF_THERM_ADC	294	AI	ADC input	
PM8550_NC_ADC	295	AI	ADC input	
KYPD_VOLP_N	296	I/O	Volume+ key	
PM8010_2_RESET_N	306	I/O	Volume- key	
PM8550_CBL_PWR_N	321	DI	Automatic power-on signal, low effective	

PM8550_ADC2	322	I/O	PM8550 ADC input 2	
PM8550_ADC3	338	I/O	PM8550_ADC input 3	
PM8010_1_RESET_N	366	I/O	PM8850VS_G_GPIO_05	
FORCE_USB_BOOT	415	I/O	Forced download, highly effective	
SYS_THERM2_ADC	419	AI	Can be reused as ADC	
SYS_THERM3_ADC	420	AI	Can be reused as ADC	
PMK_CLK7_NFC_IN	422	I/O	PMK_CLK7_NFC_IN	
VBATT_CONN_VSENSE_P	439	AI	VBATT_CONN_VSENSE_P	
VBATT_CONN_VSENSE_M	440	AI	VBATT_CONN_VSENSE_M	
VBATT_PACK_SNS_M	441	AI	VBATT_PACK_SNS_M	
RGB_RED	476	DO	RGB red indicator output positive	
RGB_GREEN	477	DO	RGB green indicator output positive	
RGB_BLUE	478	DO	RGB blue indicator output positive	
AOSS_SLEEP_INDICATOR	488	DO	AOSS sleep indication	

3.3 Mechanical Dimensions



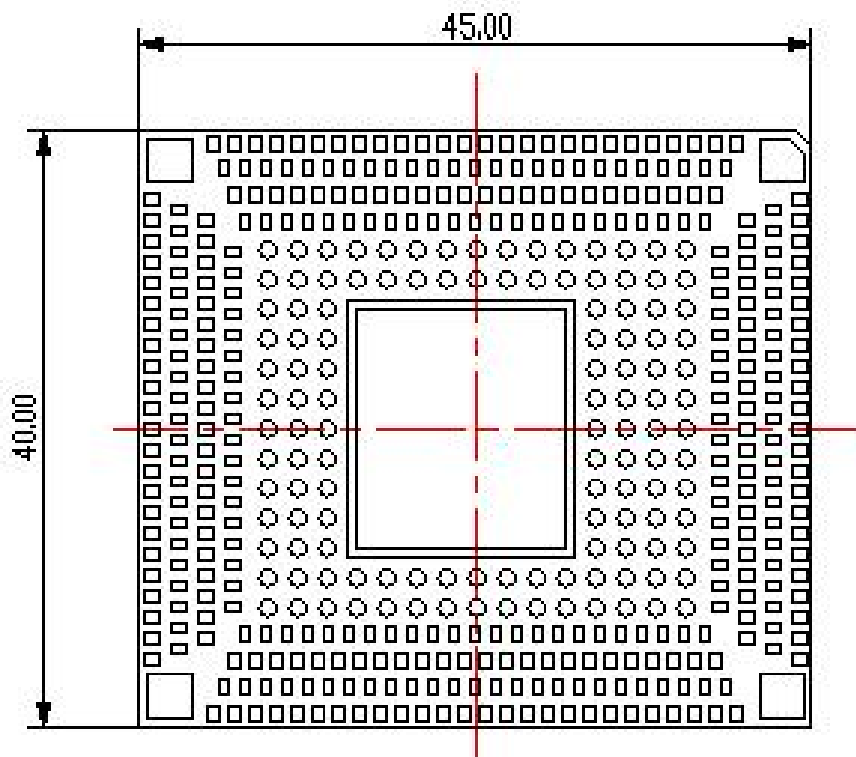


Figure 3.2: Module 3D size (unit: mm)

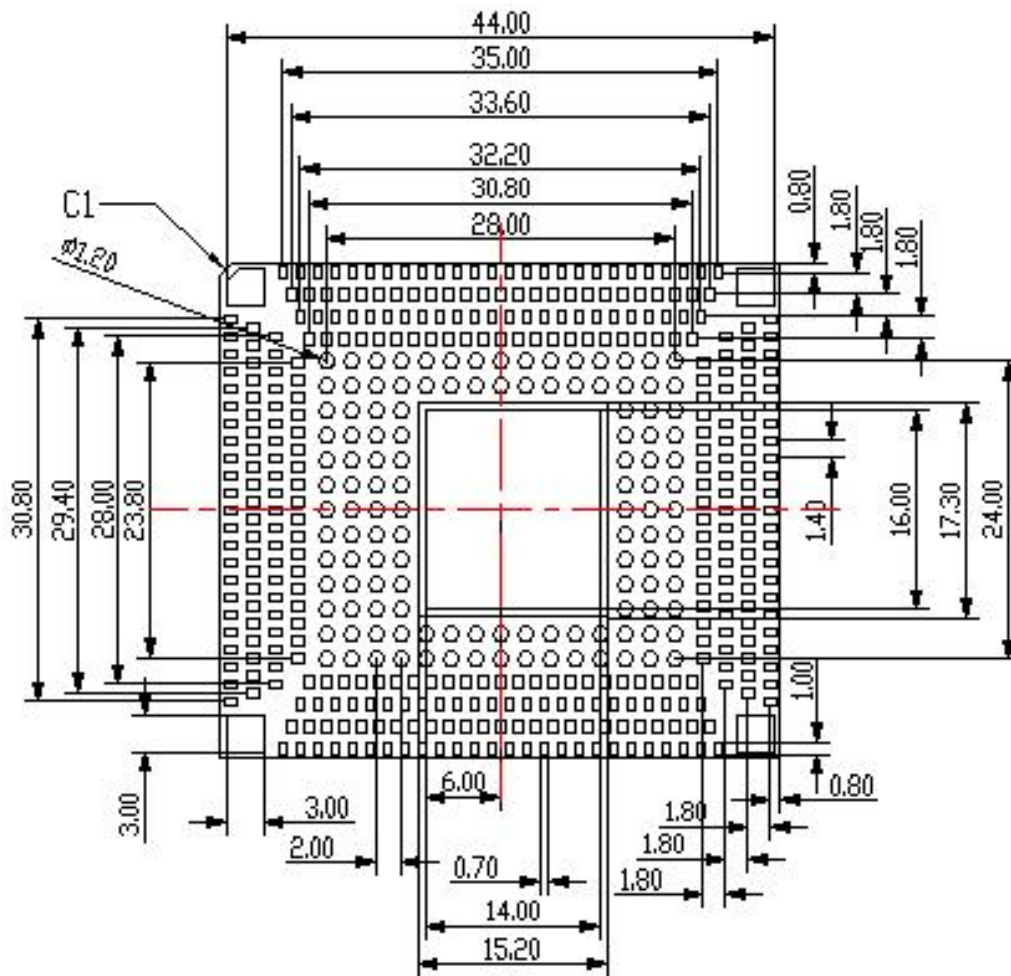


Figure 3.3: Recommended PCB package size (unit: mm)

4 Interface application

4.1 Power Supply

In the case of a battery device, the voltage input range of the module VBAT is 3.5V to 4.2V, and the recommended voltage is 3.8V. In the GSM band, when the module is transmitting at maximum power, the peak current can reach up to 4A, resulting in a large voltage drop on VBAT.

It is recommended to use a large capacitor regulator close to VBAT. It is recommended to use two 47uF ceramic capacitors. Parallel 33PF and 10PF capacitors can effectively remove high frequency interference. To prevent damage to the chip due to ESD and surge, it is recommended to

use a suitable TVS tube and a 5.1V/500mW Zener diode at the VBAT pin of the module. For PCB layout, the capacitors and diodes should be as close as possible to the VBAT pin of the module. The user can directly power the module with a 3.8V lithium-ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150m Ω .

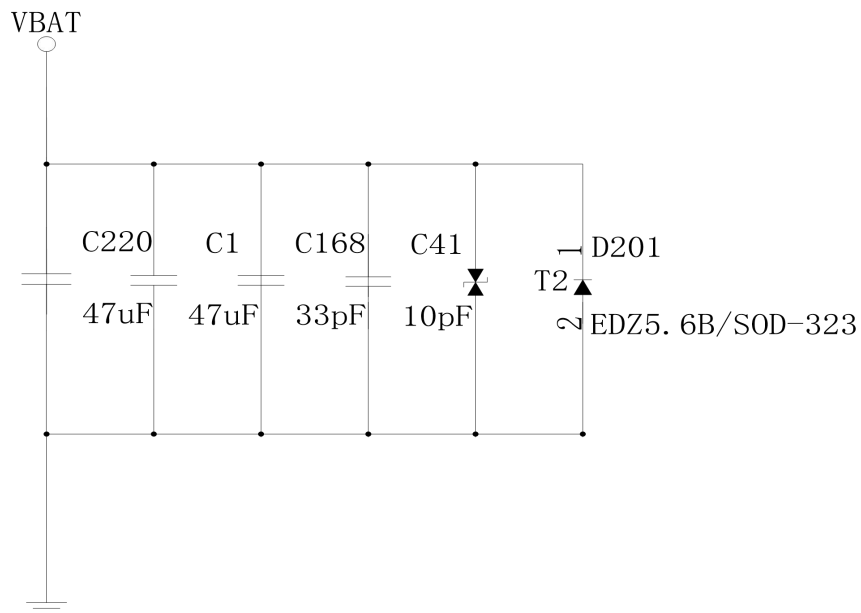


Figure 4.1: VBAT input reference circuit

If it is a DC power supply device, the DC input voltage is 4.5V-17V. The recommended circuit that can be powered by DC-DC is shown below:

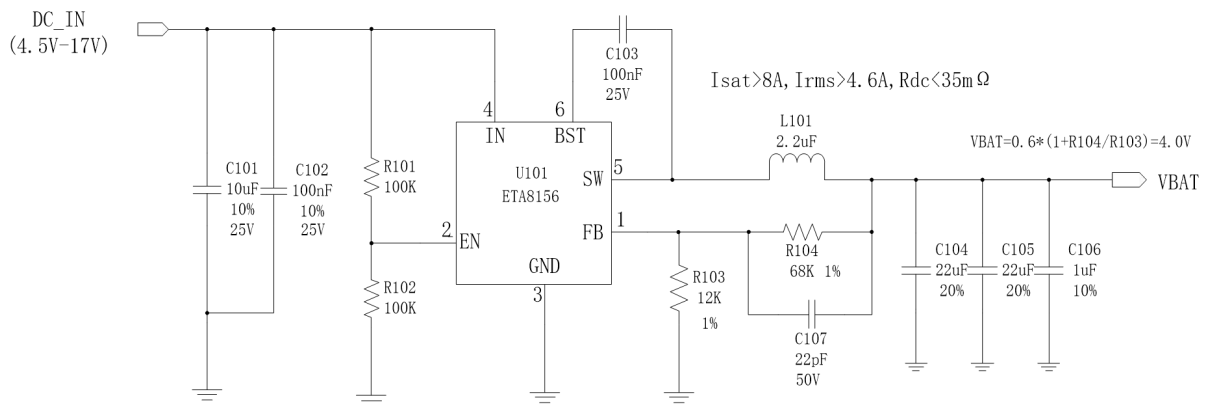


Figure 4.2: DC-DC power supply circuit

4.1.1 Power Pin

The VBAT pin (1, 2, 145, 146) is used for power input. In the user's design, pay special attention to the design of the power supply section to ensure that the VBAT does not fall below 3.5V even when the module consumes 4A. If the voltage drops below 3.5V, the module may shut down. The PCB layout from the VBAT pin to the power supply should be wide enough to reduce the voltage drop in the transmit burst mode.

VBAT



Figure 4.3: VBAT lowest voltage drop

4.2 Power on and off

Do not turn on the module when the module's temperature and voltage limits are exceeded. In

extreme cases, such operations can cause permanent damage to the module.

4.2.1 Module Boot

The user can power on the module by pulling the PWRKEY pin (86) low. The pull-down time is at least 3 seconds. This pin has been pulled up to 1.8V in the module. The recommended circuit is as follows; or the PM8550_CBL_PWR_N pin (321) is pulled low. PM8550_CBL_PWR_N can be powered on by 1K pull-down resistor to GND. It does not need to release this signal after booting.

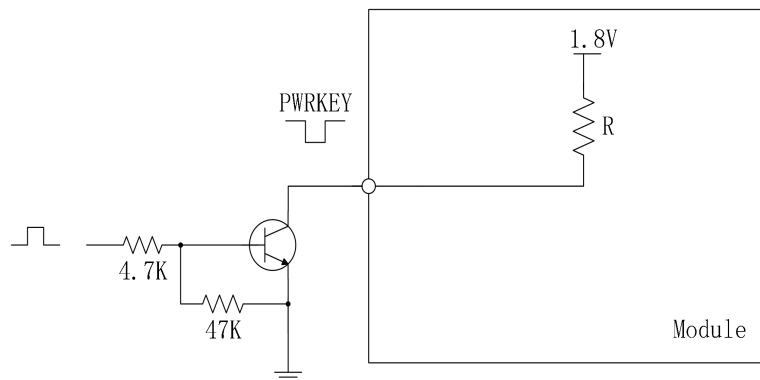


Figure 4.4: Using an external signal to drive the module to boot

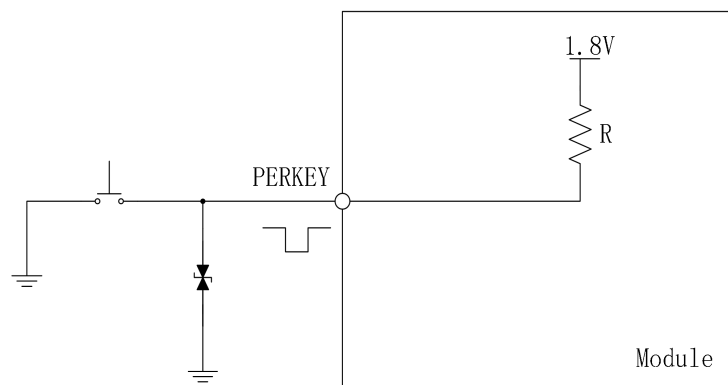


Figure 4.5: Booting with the button circuit

The following figure is the boot timing description:

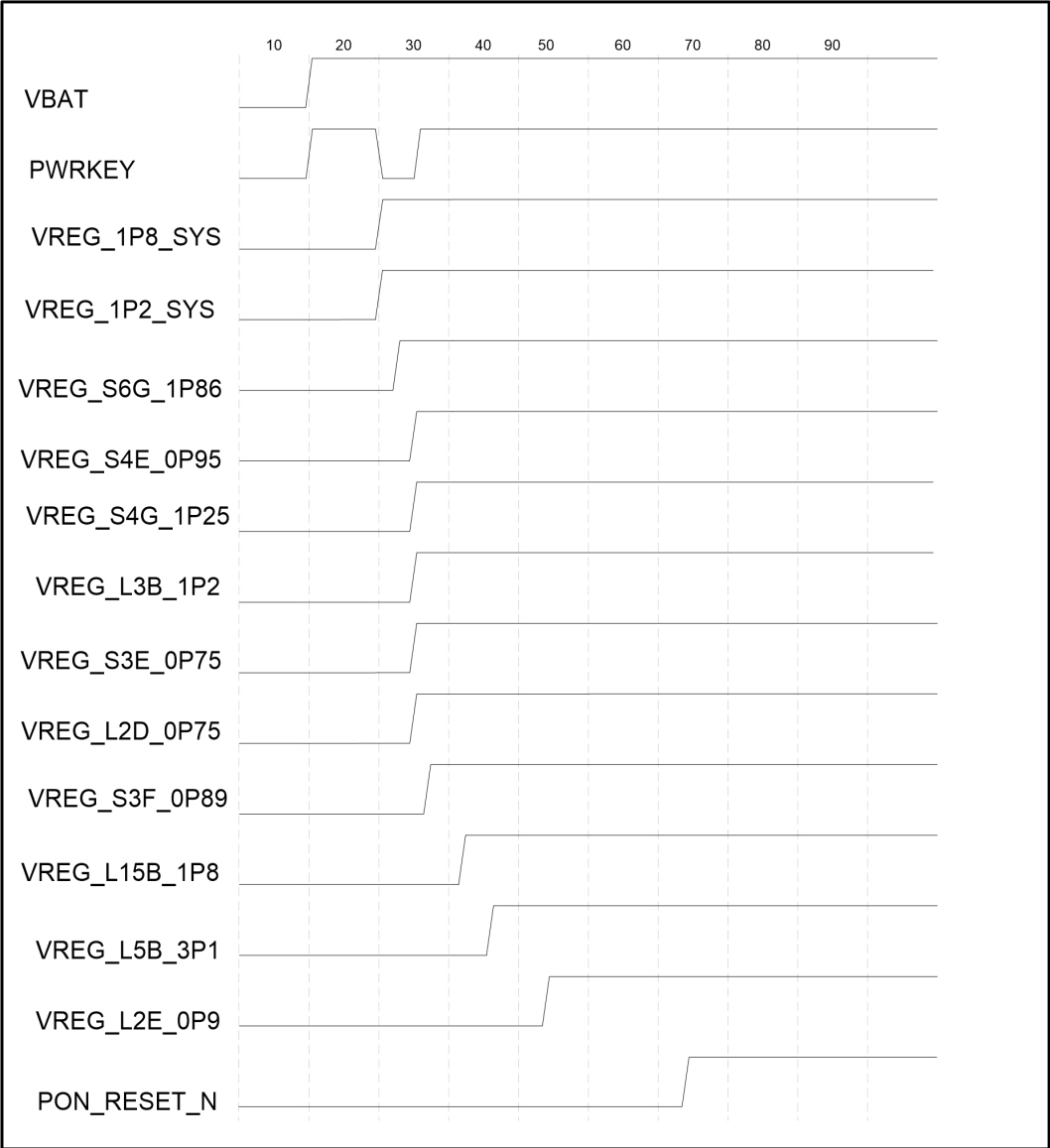


Figure 4.6: Using PWRKEY boot timing diagram

4.2.2 Module Shutdown

Users can use the PWRKEY pin to shut down.

4.2.2.1 PWRKEY Shutdown

The user can turn off the PWRKEY signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the boot circuit. After the module detects the shutdown action, a prompt window pops up on the screen to confirm whether to perform the shutdown action.

The user can achieve a forced shutdown by pulling PWRKEY down for a long time, pulling down for at least 15 seconds.

4.2.3 Module Reset

The SNM970 module supports a reset function that allows the user to quickly restart the module by pulling the RESET_N pin (PIN89) of the module low. The recommended circuit is as follows:

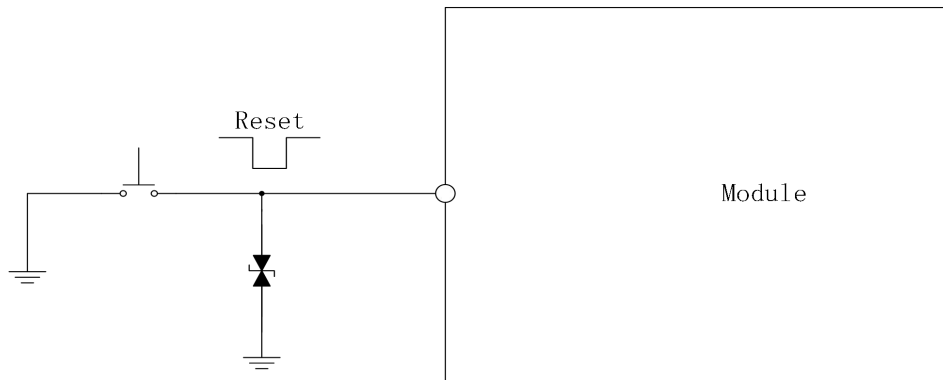


Figure 4.7: Reset using the key circuit

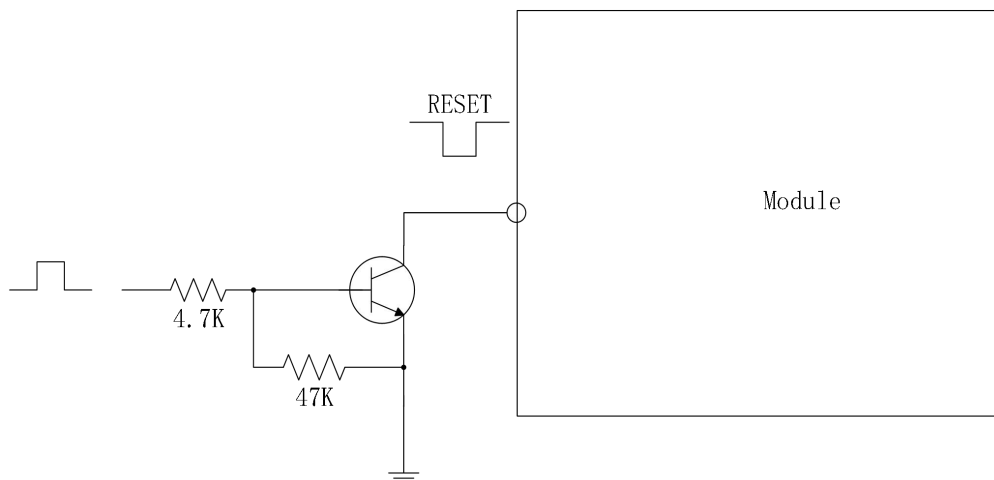


Figure 4.8: Reset Module Using External Signal

When the pin is high, the voltage is typically 1.8V. Therefore, for users with a level of 3V or 3.3V, it is not possible to directly use the GPIO of the MCU to drive the pin. An isolation circuit is required. The hardware parameters of the RESET can refer to the following table:

Table4.1: RESET Hardware Parameters

Pin	Description	Minimum	Typical	Maximum	Unit
RESET_N	Input high level	1.4	1.8	-	V

	Input low level	-	0	0.6	V
	Pull down effective time	500		-	ms

4.3 VCOIN Power

When VBAT is disconnected, the user needs to save the real-time clock. The VCOIN pin cannot be left floating. It should be connected to a large capacitor or battery. When external capacitor is connected, the recommended value is 10uF. The reference design circuit is used when the RTC power supply uses an external large capacitor or battery to power the RTC inside the module:

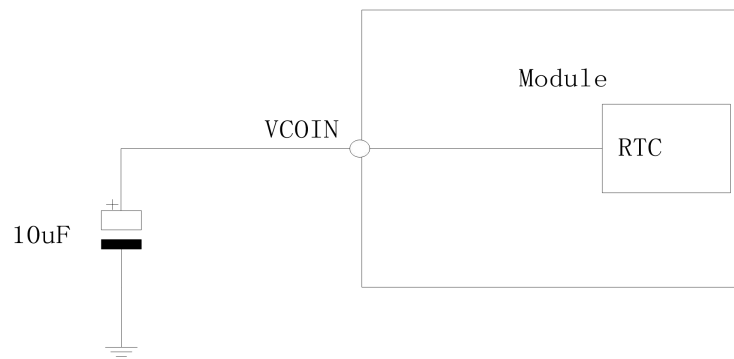


Figure 4.9: External Capacitor Powering the RTC

Rechargeable battery powered:

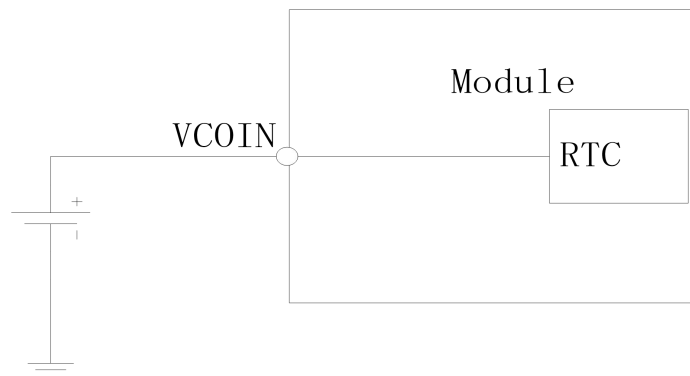


Figure 4.10: Rechargeable battery to power the RTC

Note:

This VCOIN supply has a typical value of 3.0V and consumes about 10uA of current when VBAT is disconnected.

4.4 Power Output

The SNM970 has multiple power outputs. For SD card, sensor, touch panel, USB 3.0, external LDO power supply, etc. In application, it is recommended to add parallel 33PF and 10PF capacitors to each power supply to effectively remove high frequency interference.

Table 4.2: Power Description

Signal	Range(V)	Default Voltage(V)	Drive Current(mA)
VREG_L9B_2P9	1.65–3.3	2.96	600
VREG_L8B_1P8	1.65–3.54	1.8	50
VREG_L2G_1P2	1.1–1.3	1.2	300
VREG_L11B_1P2	1.1–1.3	1.2	300
VREG_L15B_1P8		1.8	100
VREG_L1B_1P8	1.71–1.95	1.8	200
VREG_L12B_1P8	1.71–1.95	1.8	100
VREG_L14B_3P2	2.7–3.54	3.2	100
VREG_L13B_3P0	2.7–3.3	3.0	100
VREG_L2B_3P0	2.9–3.54	3.0	250

4.5 Serial Port

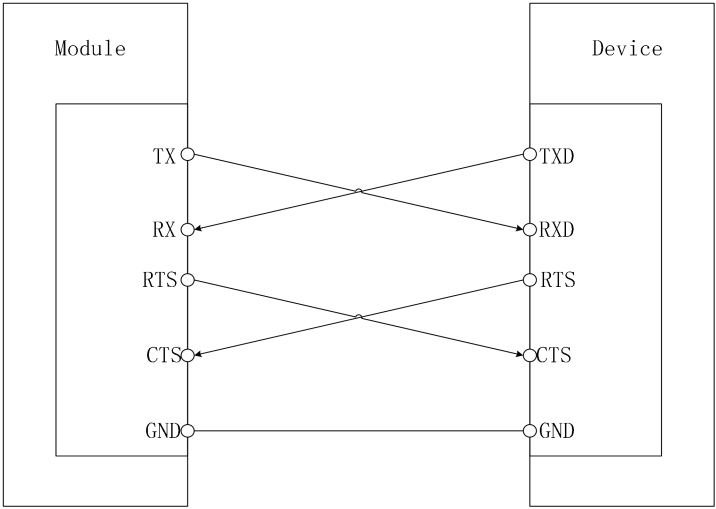
The SNM970 provides six serial ports for communication.

Table 4.3: UART Pin Description

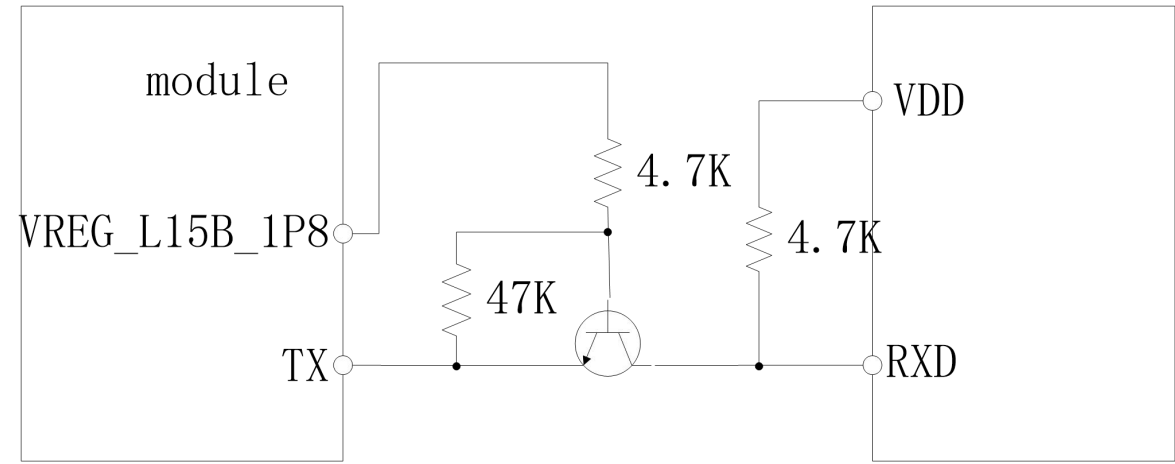
Name	Pin	Direction	Function
DEBUG_RX	359	DI	UART Data Reception (DEBUG UART)
DEBUG_TX	358	DO	UART Data Transmission (DEBUG UART)
GPIO51*_UART0_RXD	335	DI	UART Data Reception
GPIO50*_UART0_TXD	334	DO	UART Data Transmission
GPIO75*_UART5_RXD	292	DI	UART Data Reception
GPIO74*_UART5_TXD	293	DO	UART Data Transmission
GPIO59*_UART6_RXD	47	DI	UART Data Reception
GPIO58*_UART6_TXD	46	DO	UART Data Transmission

GPIO71*_UART4_RXD	391	DI	UART Data Reception
GPIO70_UART4_TXD	390	DO	UART Data Transmission
GPIO68/UART4_CTS	388	DI	UART Data Transmission
GPIO69/UART4_RTS	389	D0	UART Data Transmission
GPIO63*_UART3_RXD	394	DI	UART Data Reception
GPIO62*_UART3_TXD	393	D0	UART Data Transmission
GPIO60/UART3_CTS	395	DI	UART Data Transmission
GPIO61/UART3_RTS	396	D0	UART Data Transmission

If you need to use a four-wire serial port, you can refer to Table 9.3 for multiplexing.
The serial port connection can be referred to the following connection:



When the serial level used by the user does not match the module, in addition to adding the level shifting IC, the following figure can also be used to achieve level matching. Only the matching circuits on TX and RX are listed here. Other low speed signals can refer to these two circuits.



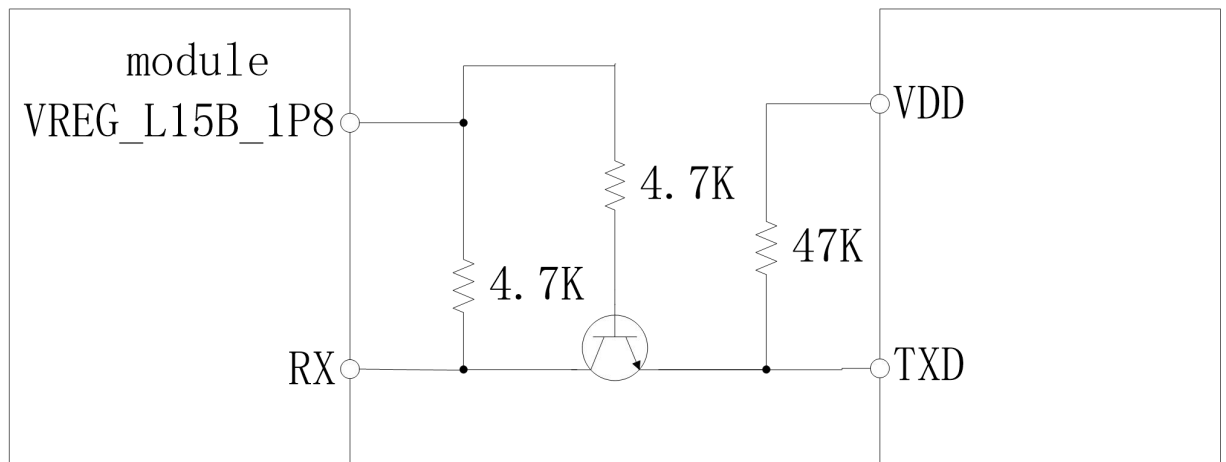


Figure 4.13: RX Connection Diagram

Note: When using Figures 12, 13 for level isolation, it is recommended that VREG_L15B_1P8 be used as the pull-up supply.

Table 4.4: Serial Port Hardware Parameters

Description	Minimum	Maximum	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Output low level	-	0.45	V
Output high level	1.35	-	V

Note:

1. The serial port of the module is a CMOS interface, and the RS232 signal cannot be directly connected. If necessary, please use the RS232 conversion chip.
2. If the 1.8V output of the module cannot meet the high-level range of the user terminal, please add a level shifting circuit.

4.6 MIPI Interface

SNM970 supports Mobile Industry Processor Interface(MIPI) interface used for Camera and LCD.

MIPI is a high-speed signal line. In the Layout stage, please follow the impedance and length

requirements strictly, and control the length of the differential pair within the group and the group length. The total length should be as short as possible.

4.6.1 LCD Interface

SNM970 module supports 2 groups of LCD display MIPI interface, the screen resolution can support up to $3480 \times 2160 @ 120\text{Hz}$ or $3360 \times 1600 @ 144\text{Hz}$. signal interface as shown in the table below, in the Layout, MIPI signal line please strictly control the differential $85 \pm 10\%$ ohm impedance and signal line within and between the groups of the same length.

When users need compatible screen design, they can use the LCD_ID pin or ADC pin of the module, and the LCD interface is as follows:

Table 4.5: Screen interface definition

Main display interface			
MIPI_DSI0_CLK_N	170	AO	MIPI_LCD clock
MIPI_DSI0_CLK_P	172	AO	
MIPI_DSI0_LANE0_N	173	AO	MIPI_LCD data
MIPI_DSI0_LANE0_P	175	AO	
MIPI_DSI0_LANE1_N	163	AO	
MIPI_DSI0_LANE1_P	160	AO	
MIPI_DSI0_LANE3_N	158	AO	
MIPI_DSI0_LANE3_P	161	AO	
MIPI_DSI0_LANE2_N	167	AO	
MIPI_DSI0_LANE2_P	169	AO	
MIPI_DSI0_CLK1_N	166	AO	DSI split link
MIPI_DSI0_CLK1_P	164	AO	
GPIO133/DISP0_RESET_N	351	I/O	LCD reset
GPIO86*_MDP_VSYNC_P	397	I/O	LCD frame sync signal

Sub display interface			
MIPI_DSI1_CLK_N	183	AO	MIPI_LCD clock
MIPI_DSI1_CLK_P	186	AO	
MIPI_DSI1_LANE0_N	184	AO	MIPI_LCD data
MIPI_DSI1_LANE0_P	182	AO	

MIPI_DSI1_LANE1_N	179	AO	
MIPI_DSI1_LANE1_P	181	AO	
MIPI_DSI1_LANE3_N	185	AO	
MIPI_DSI1_LANE3_P	187	AO	
MIPI_DSI1_LANE2_N	188	AO	
MIPI_DSI1_LANE2_P	190	AO	
GPIO87*_MDP1_VSYNC_S	398	I/O	LCD frame sync signal

LCD_ID of the module, this pin is internally GPIO. When used as LCD_ID, please confirm the internal circuit of LCD. If the internal divider of the LCD uses resistor divider, please pay attention to the voltage to meet the high or low range of GPIO.

MIPI is a high-speed signal line. To avoid EMI interference, it is recommended to place a common-mode inductor near the LCD side.

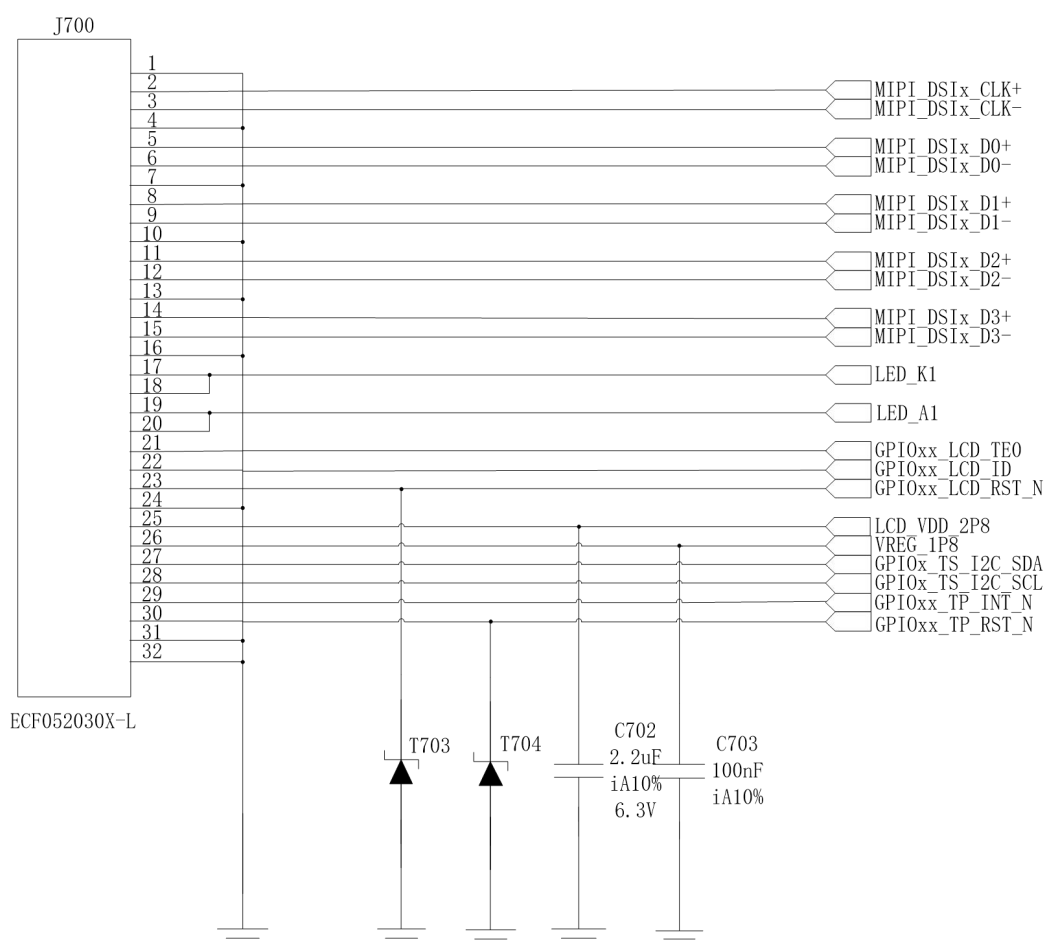


Figure 4.14: LCD interface circuit

SNM970 does not support backlight drive. LCD backlight driver circuit needs to be added by customers. Please refer to figure 4.16 for specific circuit. Adjusting the backlight brightness can be achieved by the module's PM8550_PWM_OUT_GPIO9 (PIN205), modulated in PWM mode.

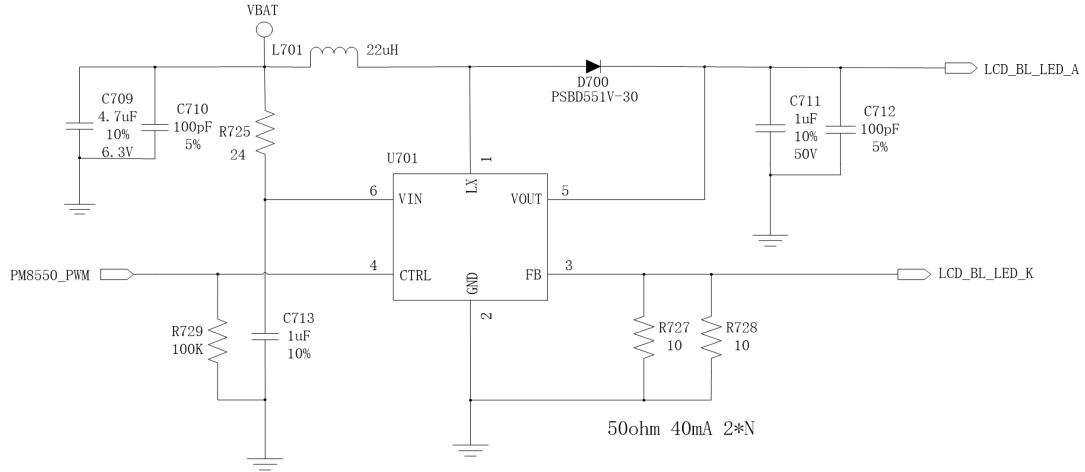


Figure 4.15: Backlight drive schematic

Note: The backlight circuit should be based on the LCD backlight circuit to select the chip, the user should carefully read the LCD document to select the correct driver chip. The reference circuit provided in this document is a series-type PWM dimming backlight driver circuit; if it is a series-type one-line dimming backlight driver circuit, it needs to be controlled by GPIO.

4.6.2 MIPI Camera Interface

SNM970 module supports 6 sets of MIPI camera interface. Single camera can support up to 108 M @ 30 fps; additionally supports Triple Camera (36 M + 36 M + 36 M) @ 30 fps, Dual Camera (64 M + 36 M) @ 30 fps. The module provides the power required by the Camera, including AVDD-2.8V, AFVDD-2.8V (powered by the focus motor) and D-VDD1.2V (CAM core voltage). D-VDD1.2V (CAM core Voltage) needs the customer to add an external LDO circuit.

Table 4.6: MIPI Camera Interface Definition

CSI0 interface			
Name	Pin	Input/output	Description
MIPI_CSI0_CLK_N	463	AO	Camera0 MIPI clock
MIPI_CSI0_CLK_P	462	AO	

MIPI_CSI0_LANE0_N	243	AI/AO	Camera0 MIPI data
MIPI_CSI0_LANE0_P	240	AI/AO	
MIPI_CSI0_LANE1_N	242	AI/AO	
MIPI_CSI0_LANE1_P	239	AI/AO	
MIPI_CSI0_LANE2_N	235	AI/AO	
MIPI_CSI0_LANE2_P	232	AI/AO	
MIPI_CSI0_LANE3_N	241	AI/AO	
MIPI_CSI0_LANE3_P	238	AI/AO	
CAM_MCLK0	310	DO	Camera0 main clock
CAM0_RST_N	66	DO	Camera0 reset
GPIO143_CAM0_PWD_N	300	DO	Camera0 dormancy

CSI1 interface			
Name	Pin	Input/output	Description
MIPI_CSI1_CLK_N	249	AO	Camera1 MIPI clock
MIPI_CSI1_CLK_P	246	AO	
MIPI_CSI1_LANE0_N	252	AI/AO	Camera1 MIPI data
MIPI_CSI1_LANE0_P	459	AI/AO	
MIPI_CSI1_LANE1_N	255	AI/AO	
MIPI_CSI1_LANE1_P	458	AI/AO	
MIPI_CSI1_LANE2_N	244	AI/AO	
MIPI_CSI1_LANE2_P	247	AI/AO	
MIPI_CSI1_LANE3_N	248	AI/AO	
MIPI_CSI1_LANE3_P	245	AI/AO	
CAM_MCLK1	311	DO	Camera1 main clock
CAM1_RST_N	61	DO	Camera1 reset
GPIO90_CAM1_PWD_N	301	DO	Camera1 dormancy

CSI2 interface			
Name	Pin	Input/output	Description
MIPI_CSI2_CLK_N	259	AO	Camera2 clock
MIPI_CSI2_CLK_P	256	AO	
MIPI_CSI2_LANE0_N	253	AI/AO	Camera2 data
MIPI_CSI2_LANE0_P	254	AI/AO	
MIPI_CSI2_LANE1_N	260	AI/AO	
MIPI_CSI2_LANE1_P	257	AI/AO	

MIPI_CSI2_LANE2_N	457	AI/AO	
MIPI_CSI2_LANE2_P	258	AI/AO	
MIPI_CSI2_LANE3_N	456	AI/AO	
MIPI_CSI2_LANE3_P	261	AI/AO	
CAM_MCLK2	312	DO	Camera2 main clock
GPIO18_CAM2_RST_N	63	DO	Camera2 reset
GPIO125	385	DO	Camera2 dormancy

CSI3 interface			
Name	Pin	Input/output	Description
MIPI_CSI3_CLK_N	9	AO	Camera3 时钟信号
MIPI_CSI3_CLK_P	449	AO	
MIPI_CSI3_LANE0_N	6	AI/AO	Camera3 MIPI 数据线
MIPI_CSI3_LANE0_P	450	AI/AO	
MIPI_CSI3_LANE1_N	1	AI/AO	
MIPI_CSI3_LANE1_P	2	AI/AO	
MIPI_CSI3_LANE2_N	4	AI/AO	
MIPI_CSI3_LANE2_P	5	AI/AO	
MIPI_CSI3_LANE3_N	7	AI/AO	
MIPI_CSI3_LANE3_P	8	AI/AO	
CAM_MCLK3	313	DO	Camera3 主时钟
CAM3_RST_N	65	DO	Camera3 复位信号线
GPIO159*_CAM3_PWD_N	339	DO	Camera3 休眠信号线

CSI4 interface			
Name	Pin	Input/output	Description
MIPI_CSI4_CLK_N	454	AO	Camera4 clock
MIPI_CSI4_CLK_P	270	AO	
MIPI_CSI4_LANE0_N	455	AI/AO	Camera4 MIPI data
MIPI_CSI4_LANE0_P	267	AI/AO	
MIPI_CSI4_LANE1_N	453	AI/AO	
MIPI_CSI4_LANE1_P	273	AI/AO	
MIPI_CSI4_LANE2_N	452	AI/AO	
MIPI_CSI4_LANE2_P	276	AI/AO	
MIPI_CSI4_LANE3_N	451	AI/AO	
MIPI_CSI4_LANE3_P	279	AI/AO	

CAM_MCLK4	315	DO	Camera4 main clock
AON_CAM_RESET_N	62	DO	Camera4 reset
GPIO40*_CAM4_PWD_N	197	DO	Camera4 dormancy

CSI5 interface			
Name	Pin	Input/output	Description
MIPI_CSI5_CLK_N	15	AO	Camera5 clock
MIPI_CSI5_CLK_P	447	AO	
MIPI_CSI5_LANE0_N	12	AI/AO	Camera5 MIPI data
MIPI_CSI5_LANE0_P	448	AI/AO	
MIPI_CSI5_LANE1_N	13	AI/AO	
MIPI_CSI5_LANE1_P	14	AI/AO	
MIPI_CSI5_LANE2_N	16	AI/AO	
MIPI_CSI5_LANE2_P	17	AI/AO	
MIPI_CSI5_LANE3_N	19	AI/AO	
MIPI_CSI5_LANE3_P	20	AI/AO	
CAM_MCLK5	314	DO	Camera5 main clock
GPIO144_CAM5_RST_N	64	DO	Camera5 reset
GPIO125	385	DO	Camera5 dormancy

CSI6 interface			
Name	Pin	Input/output	Description
MIPI_CSI6_CLK_N	227	AO	Camera6 clock
MIPI_CSI6_CLK_P	226	AO	
MIPI_CSI6_LANE0_N	229	AI/AO	Camera6 MIPI data
MIPI_CSI6_LANE0_P	228	AI/AO	
MIPI_CSI6_LANE1_N	231	AI/AO	
MIPI_CSI6_LANE1_P	230	AI/AO	
MIPI_CSI6_LANE2_N	237	AI/AO	
MIPI_CSI6_LANE2_P	234	AI/AO	
MIPI_CSI6_LANE3_N	465	AI/AO	
MIPI_CSI6_LANE3_P	464	AI/AO	
CAM_MCLK6	316	DO	Camera6 main clock
GPIO42	199	I/O	Camera6 reset
GPIO108	200	I/O	Camera6 dormancy

CSI7 interface			
Name	Pin	Input/output	Description
MIPI_CSI7_CLK_N	221	AO	Camera7 clock
MIPI_CSI7_CLK_P	220	AO	
MIPI_CSI7_LANE0_N	223	AI/AO	Camera7 data
MIPI_CSI7_LANE0_P	222	AI/AO	
MIPI_CSI7_LANE1_N	225	AI/AO	
MIPI_CSI7_LANE1_P	224	AI/AO	
MIPI_CSI7_LANE2_N	467	AI/AO	
MIPI_CSI7_LANE2_P	466	AI/AO	
MIPI_CSI7_LANE3_N	469	AI/AO	
MIPI_CSI7_LANE3_P	468	AI/AO	
CAM_MCLK7	317	DO	Camera7 main clock
GPIO56	43	I/O	Camera7 reset
GPIO57	44	I/O	Camera7 dormancy

If the user designs to use the CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device. The I2C of the AF device should be connected to the driver chip of CAMERA, and the correct connection is as follows:

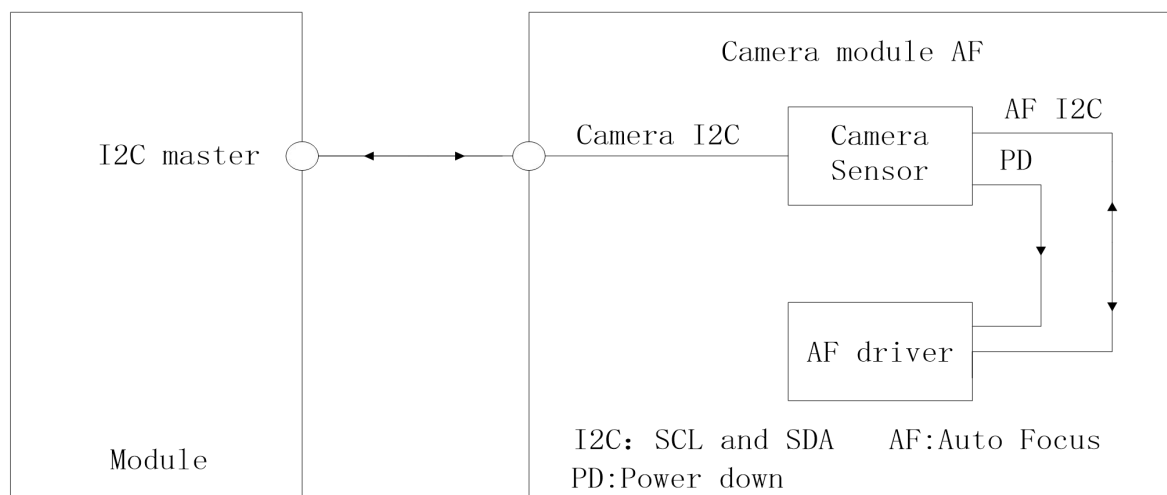


Figure 4.16: Correct CAMERA connection diagram

The MIPI interface has a high rate. The user should control the impedance by $85(\pm 10\%)$ ohms during the routing. Please pay attention to the length of the trace. It is not recommended to add a small capacitor on the MIPI signal line. This may affect the rising edge of the MIPI data. This in turn causes the MIPI data to be invalid.

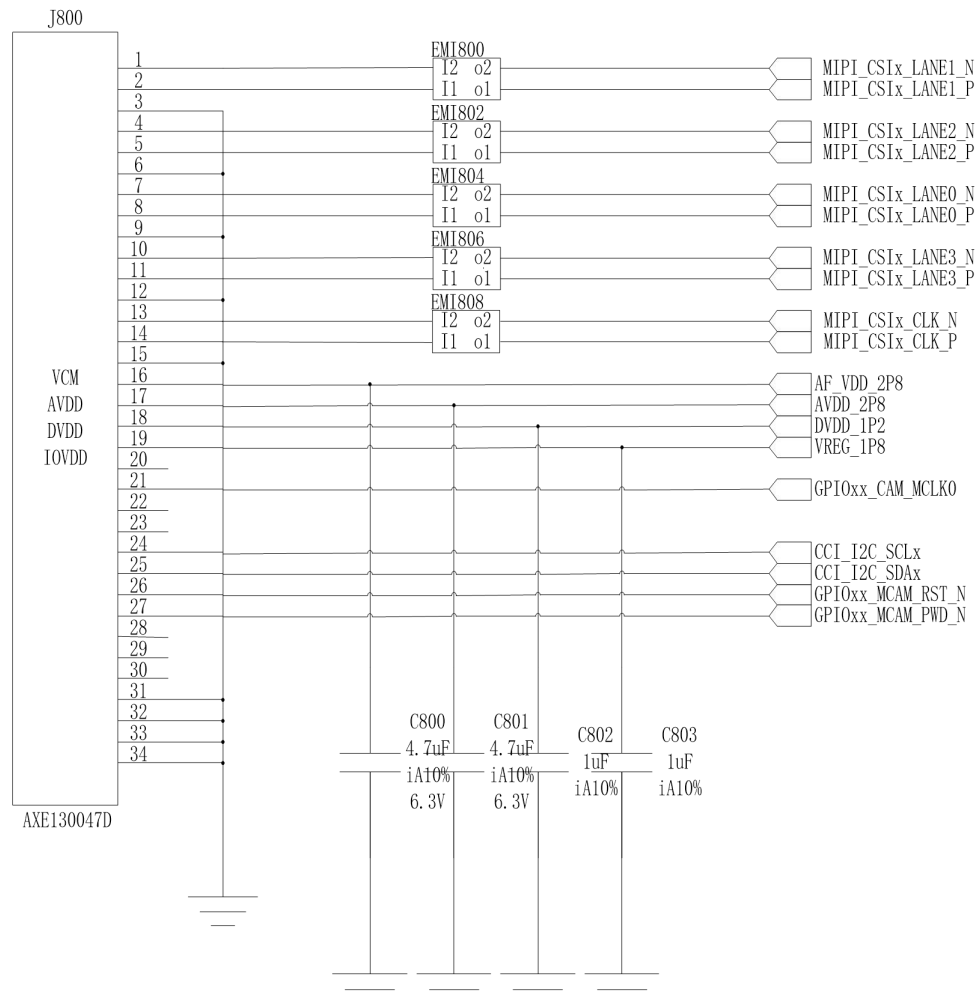


Figure 4.17: MIPI Camera Reference Circuit

MIPI is a high-speed signal line, users must pay attention to the protection of the layout stage, so that it is away from the signal line is easy to be interfered with, it must be done up and down the left and right packet GND processing, the alignment for the differential pair of ways to do the 85 ohm differential impedance matching, in order to ensure the consistency of the impedance as far as possible do not cross the different GND plane.

MIPI interface in the selection of ESD devices, please select a small capacitance TVS, it is recommended that the parasitic capacitance is less than 1pF.

The MIPI alignment requirements are as follows: :

- The total length of the alignment should not exceed 200mm.
- 85 ohm differential impedance control with ± 15 ohm error is required.
- Differential line length error within the group is controlled within 0.7mm.
- The length error between groups is controlled within 1.4mm.

4.7 Capacitive Touch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touches while providing the required power and interrupt pins. The default interface pins for capacitive touch software are defined as follows:

Table 4.7: Capacitive Touch Interface Definitions

Name	Pin	Input/Output	Description
GPIO44/TS_SPI_MISO_I2C_SDA	177	I/O	TP_SPI clock, Multiplexing TP_I2C data
GPIO45/TS_SPI_MOSI_I2C_SCL	180	I/O	TP_SPI chip-select, Multiplexing TP_I2C clock
GPIO46/TS_SPI_CLK	159	DO	TP_SPI clock
GPIO47*/TS_SPI_CS_N	162	DO	TP_SPI chip-select
GPIO25*/TS_INT_N	349	DI	TP interrupt
GPIO24/TS_RESET_N	341	DO	TP reset

Note:

The interface definition of the capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.8 PCIE Interface

The module provides a set of PCIe x2 interfaces that can be used to expand Ethernet or USB interfaces. The interface pins are defined in the following table:

Table 4.8: PCIE Pin Definitions

Name	Pin	Input/ Output	Description
PCIE1_TX0_M	22	AO	PCIE1 differential data
PCIE1_TX0_P	25	AO	

PCIE1_RX0_M	29	AI	
PCIE1_RX0_P	27	AI	
PCIE1_TX1_M	23	AO	
PCIE1_TX1_P	24	AO	
PCIE1_RX1_M	444	AI	
PCIE1_RX1_P	443	AI	
PCIE1_REFCLK_M	26	AO	PCIE differential clock
PCIE1_REFCLK_P	28	AO	
GPIO97/PCIE1_RESET_N	49	DO	PCIE1 reset
GPIO98/PCIE1_CLKREQN	50	DO	PCIE1 clock require
GPIO99/PCIE1_WAKE_N	52	DO	PCIE1 wake-up

4.9 I2S Interface

There are five sets of I2S interfaces inside the module, and the pins used for this function are listed in the table below:

Table 4.9: I2S pin definitions

Name	Pin	Input/ Output	Description
I2S0_SCK	103	DO	Generic I2S
I2S0_WS	104	DO	
I2S0_DATA0	106	I/O	
I2S0_DATA1	107	I/O	
LPI_I2S1_CLK	121	DO	Generic I2S
LPI_I2S1_WS	122	DO	
LPI_I2S1_DATA0	123	I/O	
LPI_I2S1_DATA1	124	I/O	
LPI_I2S2_CLK	125	DO	Generic I2S
LPI_I2S2_WS	126	DO	
LPI_I2S2_DATA0	127	I/O	
LPI_I2S2_DATA1	128	I/O	
GPIO170_LPI_I2S0_DATA3	120	I/O	Generic I2S
GPIO166*_LPI_I2S0_WS	363	DO	

GPIO169_LPI_I2S0_DATA2	411	I/O	
GPIO168_LPI_I2S0_DATA1	486	I/O	
GPIO165_LPI_I2S0_SCK	487	DO	
GPIO167_LPI_I2S0_DATA0	489	I/O	
PRI_I2S_MCLK	100	DO	Primary I2S main clock

4.10 USB Interface

SNM970 supports one USB 2.0 interface, one USB 3.0 interface, in the Layout must control the 90 ohm differential impedance, and control the external cable length.

The module also supports OTG function. If this function is required, please refer to Figure 4.19 to add an external +5 V power supply.

The VBUS voltage input range is shown in the table below:

Table 4.10: VBUS input range

Name	Description	Minimum	Typical	Maximum	Unit
USB_VBUS	Input range	3.7	-	21.5	V

The USB plug-in detection of the module is realized by the VBUS and DP/DM data lines. When the USB cable is inserted, the VBUS voltage is detected first, and then the DM/DP pull-up state is detected to determine whether the USB data line or the charger is inserted. Therefore, if you need to use the USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is a high-speed mode. It is recommended to connect a common-mode inductor to the side of the USB connector to effectively suppress EMI interference. At the same time, the USB interface is an external interface. The DM/DP must add a TVS tube to prevent static damage caused by plugging and unplugging the data cable. When selecting the TVS, the user should pay attention to the load capacitance of less than 1pf. VBUS also needs to increase the TVS tube. If there is anti-surge demand, it is also necessary to increase the anti-surge tube. The connection diagram is as follows:

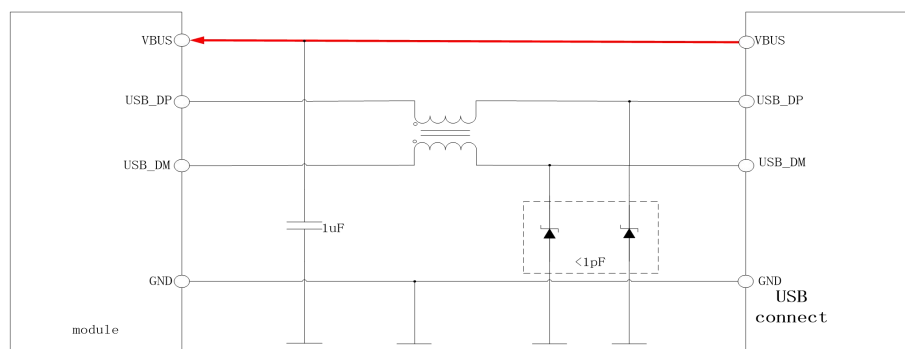


Figure 4.18: USB Connection Diagram

4.10.1 USB OTG

The SNM970 module can provide USB OTG function. The pins used in this function are as follows:

Table4.11: USB- OTG pin description

Pin name	Pin	Description
USB_VBUS	410, 436, 437, 438	USB_VBUS
USB0_HS_DM	145	USB 2.0 Data-
USB0_HS_DP	142	USB 2.0 Data+
USB_ID	399	USB ID

The recommended circuit diagram of USB OTG is as follows:

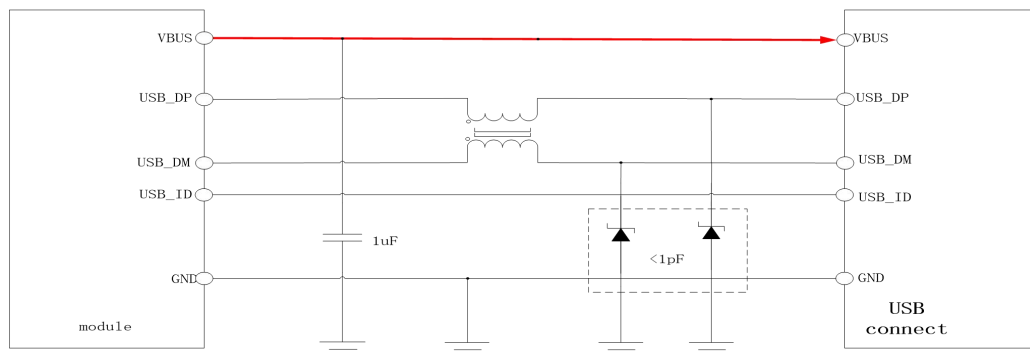


Figure 4.19: USB-OTG connection diagram

4.11 SD card Interface

SNM970 supports SD card interface.

The reference circuit is as follows:

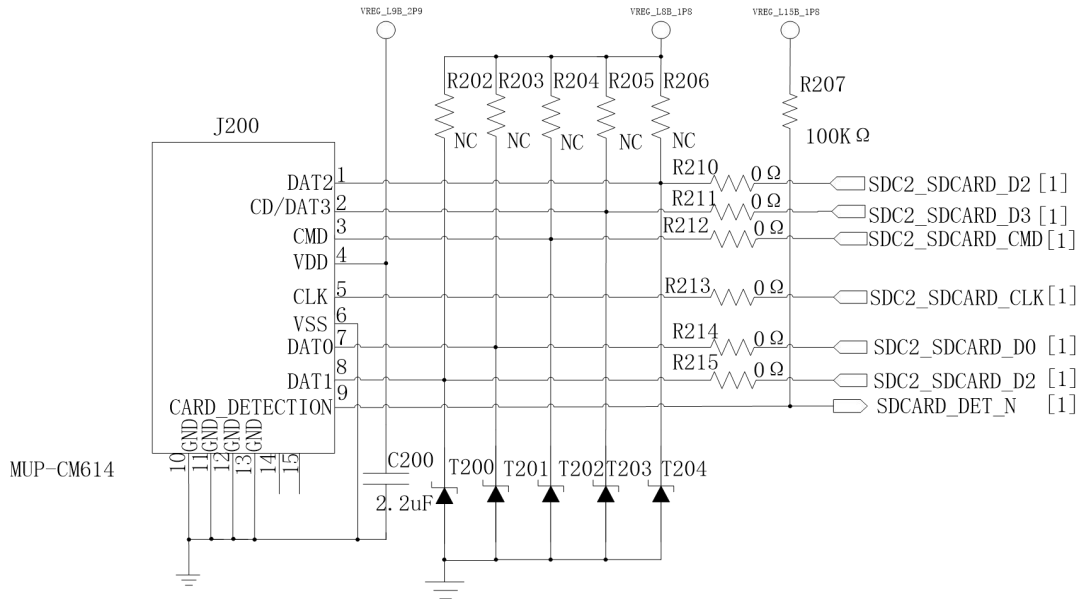


Figure 4.20: SD card interface circuit

4.12 I2C Bus Interface

The SNM970 module supports seven hardware I2C bus interfaces, four camera-specific CCI interfaces and three Sensor I2C interfaces. The pin definitions and default functions are listed in the table below:

Table 4.12: I2C interface pin description

Name	Pin	Default function
CCI_I2C0_SDA	39	CAM-specific I2C signals
CCI_I2C0_SCL	42	
CCI_I2C1_SDA	45	CAM-specific I2C signals
CCI_I2C1_SCL	48	
CCI_I2C2_SDA	51	CAM-specific I2C signals
CCI_I2C2_SCL	54	
GPIO208/CCI_I2C3_SDA	57	CAM-specific I2C signals
GPIO209/CCI_I2C3_SCL	60	
APPS_I2C_SDA	105	Generic I2C

APPS_I2C_SCL	108	
MAG_ALPS_I2C_SDA	134	I2C for Sensor
MAG_ALPS_I2C_SCL	135	
SENSOR_I2C_SDA	140	I2C for Sensor
SENSOR_I2C_SCL	141	
GPIO188*/I2C_SDA	340	I2C for Sensor
GPIO189/I2C_SDL	345	
GPIO4/I2C1_SDA	342	Generic I2C
GPIO5/I2C1_SCL	343	
GPIO8*/I2C6_SDA	283	Generic I2C
GPIO9*/I2C6_SCL	308	
GPIO28*/I2C3_SDA	380	Generic I2C
GPIO29/I2C3_SCL	381	
GPIO206/I2C4_SDA	412	Generic I2C
GPIO207/I2C4_SCL	413	
GPIO6/I2C5_SDA	291	Generic I2C
GPIO7/I2C5_SCL	290	
GPIO22/I2C2_SDA	287	Generic I2C
GPIO23/I2C2_SCL	286	

Note: Connect a 2.2K Ω pull-up resistor to 1.8V when used as an I2C bus interface, refer to Table 3.1- I2C Interface.

4.13 Analog to Digital Converter (ADC)

The SNM970 module is provided with 4 ADC input ports PM8550_ADC2 (PIN322), PM8550_ADC3 (PIN338), TOF_THERM_ADC (PIN294), and PM8550_NC_ADC (PIN295) by the power management chip with the following performance parameters:

Table 4.13: ADC performance parameters

Description	Minimum	Typical	Maximum	Unit
Input Voltage Range	0		1.875	V
Analog Input Bandwidth	-	500	-	kHz
Sampling Frequency	-	4.8	-	MHz

4.14 PWM

The PM8550_PWM_OUT_GPIO9(PIN205) pin can be used to do the backlight adjustment of the LCD to adjust the backlight brightness by adjusting the duty cycle.

4.15 Antenna Interface

The module provides 2 antenna interfaces for WiFi_6G, WiFi/ BT_2.4G antenna. In order to ensure that the user's product has good wireless performance, the antenna selected by the user should meet the requirements of input impedance of 50 ohms and VSWR of less than 2 in the operating frequency band.

4.15.1 Wi-Fi/BT antenna

The module provides the Wi-Fi/BT antenna pin RF_WIFI/BT. The antenna on the user's motherboard should be connected to the antenna pin of the module using a 50ohm microstrip line or strip line.

To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

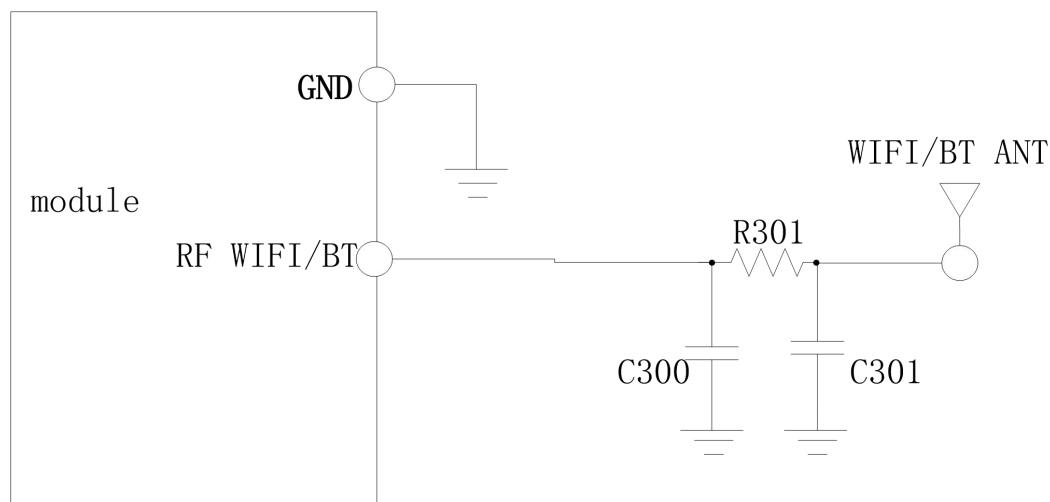


Figure 4.21: WiFi/BT antenna interface connection circuit

Note: In the figure, R301, C300, and C301 are antenna matching devices, and the specific component values can be determined after the antenna factory debugs the antenna. Among them, R301 defaults to 0R, C300 and C301 do not paste by default.

If there are fewer components between the antenna and the module output, or if the RF test head is not needed in the design, the antenna matching circuit can be simplified as shown below:

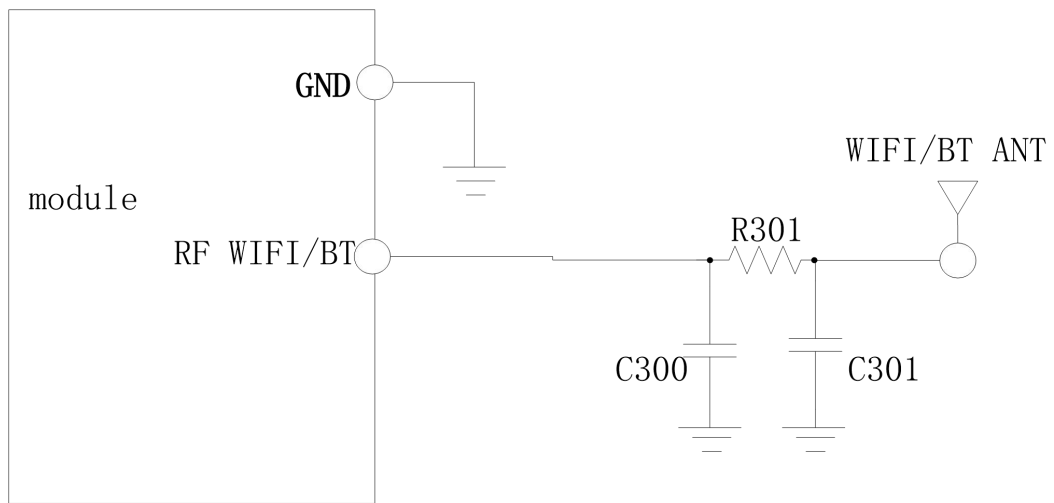


Figure 4.22: WIFI_BT antenna interface simplified connection circuit

Note: In the figure, R301 defaults to 0R, and C300 and C301 do not paste by default.

5 Electrical, Reliability

5.1 Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits can cause permanent damage to the module.

Table 5.1: Absolute Maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	-0.3	-	6	V
VBUS	--0.3	-	25	V
Peak current	-	-	3	A

5.2 Working Temperature

The table below shows the operating temperature range of the module:

Table 5.2: Module Operating Temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	°C
Storage temperature	-40	-	90	°C

5.3 Working Voltage

Table 5.3: Module Operating Voltage

Parameter	Minimum	Typical	Maximum	Unit
VBAT	3.5	3.8	4.2	V
VBUS	3.7	-	21.5	V
Hardware shutdown voltage		3.4	-	V

5.4 Digital Interface Features

Table 5.4: Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit
V _{IH}	Input high level voltage	1.17	-	2.1	V
V _{IL}	Input low level voltage	-0.3	-	0.63	V
V _{OH}	Output high level voltage	1.35	-	1.8	V
V _{OL}	Output low level voltage	0	-	0.45	V

5.5 PWRKEY Feature

Table 5.5: PWRKEY Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	1.8	-	V
	Low level	-	0	0.6	V
	Effective time	3000			ms

5.6 Electrostatic Protection

Table 5.6: VCOIN Characteristics

Parameter	Description	Minimum	Typical	Maximum	Unit
VCOIN-IN	VCOIN input voltage	2	3	3.25	V

IRTC-IN	VCOIN Current consumption	-	TBD	-	uA
VCOIN-OUT	VCOIN Output voltage	2.5	3	3.2	V
IRTC-OUT	VCOIN Output current	-	TBD	-	uA

5.7 Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling, and operating modules.

5.8 WIFI Main RF Performance

The table below lists the main RF performance under WIFI conduction.

Table 5.7: Main RF performance parameters under WIFI conduction

Transmission performance								
	2.4G			5-7G				
	802.11B	802.11G	802.11N	802.11N	802.11A	802.11AC	802.11AX/BE	
Transmit power (minimum rate)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dBm
Transmit power (maximum rate)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dBm
EVM (maximum rate)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dB
Receiving performance								
	2.4G			5-7G				
Receiving sensitivity	802.11B	802.11G	802.11N	802.11N	802.11A	802.11AC	802.11AX/BE	
Minimum rate	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dBm
Maximum rate	TBD	TBD	TBD	TBD	TBD	TBD	TBD	dBm

5.9 BT Main RF Performance

The table below lists the main RF performance under BT conduction.

Table 5.8: Main RF performance parameters under BT conduction

Transmission performance				
Transmit power	BR	EDR	BLE	
	TBD	TBD	TBD	dBm
Receiving performance				
Receiving sensitivity	BR	EDR	BLE	
	TBD	TBD	TBD	dBm

6 Production

6.1 Top and Bottom Views of The Module



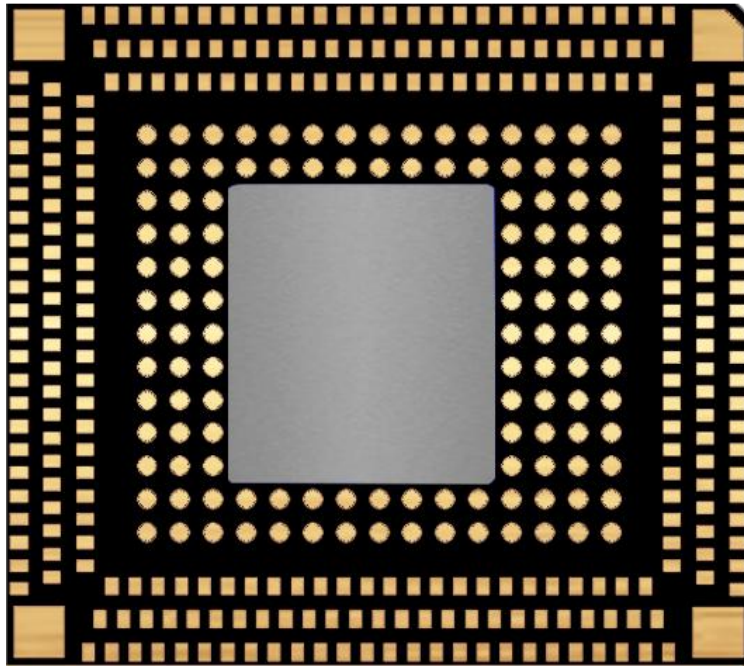


Figure 6.1: Module top
and bottom views

6.2 Recommended Soldering Furnace Temperature Curve

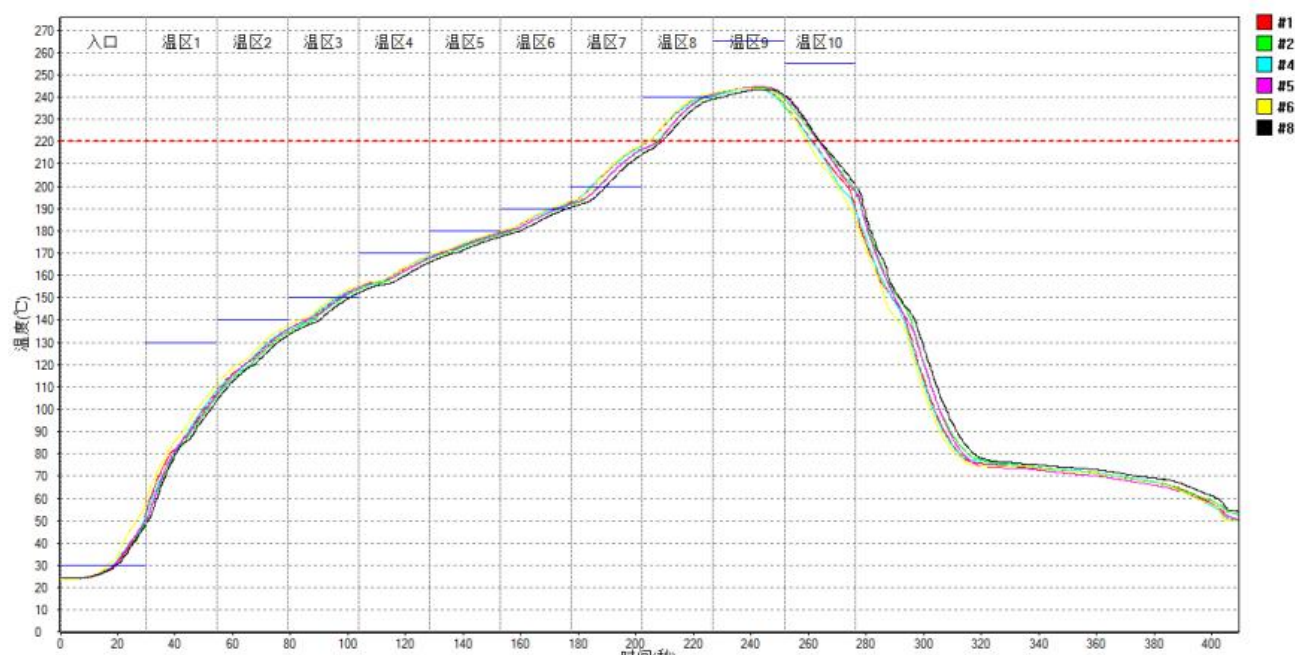


Figure 6.2: Module recommended soldering furnace temperature curve

6.3 Humidity Sensitivity (MSL)

The SNM970 module meets moisture sensitivity level 3. The dry package is subjected to the J-STD-020C specification in accordance with the IPC/JEDEC standard under ambient conditions of temperature $<30^{\circ}\text{C}$ and relative humidity $<60\%$. Under ambient conditions of temperature $<40^{\circ}\text{C}$ and relative humidity $<90\%$, the shelf life is at least 6 months without unpacking. After unpacking, The table below lists the shelf life of the modules for different moisture sensitivity levels.

Table6.1: Humidity sensitivity level distinction

Grade	Factory environment $\leq+30^{\circ}\text{C}/60\%\text{RH}$
1	Indefinite quality in the environment $\leq+30^{\circ}\text{C}/85\%\text{RH}$ Under conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Use it after forced baking. After baking, the module must be patched within the time

	limit specified on the label.
--	-------------------------------

After unpacking, the SMT patch should be taken within 168 hours under ambient conditions of $<30^{\circ}\text{C}$ and relative humidity $<60\%$. If the above conditions are not met, baking is required. Note: Oxidation risk: Baking SMD packages can cause metal oxidation and, if excessive, can cause solderability problems during board assembly. The temperature and time of the SMD package are baked, thus limiting solderability considerations. The accumulation of baking time should be no more than 96 hours at temperatures above 90°C and as high as 125°C .

6.4 Baking Requirements

Due to the humidity sensitivity of the module, the SNM970 should be thoroughly baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SNM970 should be baked for 192 hours in a cryogenic vessel at $40^{\circ}\text{C} +5^{\circ}\text{C}/-0^{\circ}\text{C}$ and a relative humidity of less than 5%, or in a high temperature vessel at $80^{\circ}\text{C}\pm 5^{\circ}\text{C}$. Bake for 72 hours. Users should note that the tray is not resistant to high temperatures. The user should take the module out of the tray for baking, otherwise the tray may be damaged by high temperature.

Table 6.2: Baking requirements

Baking temperature	Humidity	Baking time
$40^{\circ}\text{C}\pm 5^{\circ}\text{C}$	$<5\%$	192 hours
$120^{\circ}\text{C}\pm 5^{\circ}\text{C}$	$<5\%$	4 hours

6.5 Description of module warping and measurement method

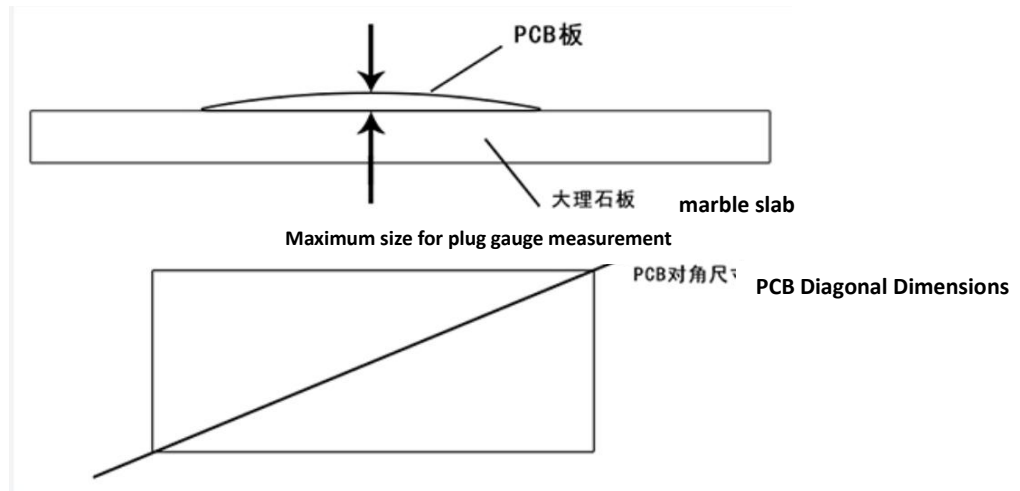


Figure 6.3: Module Measurement Diagram

Put the module to the absolute standard level, measured with a plug gauge ruler, the module warping degree $\leq 0.15\text{MM}$

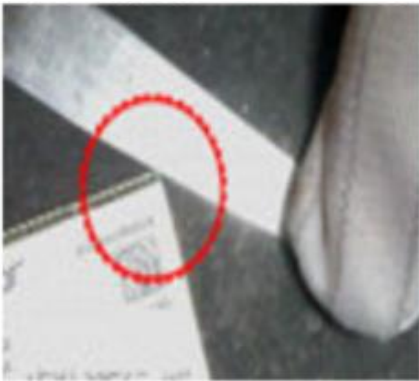
Measurement instructions:



Judgment Criteria:

1. Push the flattening plug gauge forward, if the module moves, it means that the module is flat and passes the leveling, regardless of whether it is tucked in or not;
2. Push the flattening plug gauge forward, if the module does not move, and the plug gauge can be easily plugged in, it means that the module has been deformed.

Typical wrong method as shown in the figure (plug in four corners)



7 Appendix

7.1 Related Documents

Table 7.1: Related documents

Serial number	File name	Comment
[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10:	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05:	Digital cellular telecommunications (Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment (DTE–DCE) interface for Short Message service (SMS)and Cell Broadcast Service (CBS)
[4]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[8]	AN_Serial Port	AN_Serial Port

7.2 Terms and Explanations

Table 7.2: Terms and explanations

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme

CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion

TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Phone book abbreviation	Explanations
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

7.3 Multiplexing function

Table 7.3: Multiplexing Functions

	GPIO	Pin	Multiplexing Functions				
			I2C	I3C	SPI	UART	HS-UART
QUP1_SE0	GPIO28	380	SDA	SDA	MISO	CTS	
	GPIO29	381	SCL	SCL	MOSI	RFR	
	GPIO30	382			SCLK	TX	
	GPIO31	383			CS_0	RX	
QUP1_SE1	GPIO32	376	SDA	SDA	MISO	CTS	
	GPIO33	377	SCL	SCL	MOSI	RFR	
	GPIO34	378			SCLK	TX	
	GPIO35	379			CS_0	RX	
QUP1_SE2	GPIO36	475	SDA		MISO	CTS	
	GPIO37	194	SCL		MOSI	RFR	
	GPIO38	195			SCLK	TX	
	GPIO39	196			CS_0	RX	
QUP1_SE4	GPIO44	177	SDA		MISO	CTS	
	GPIO45	180	SCL		MOSI	RFR	

	GPIO46	159			SCLK	TX	
	GPIO47	162			CS_0	RX	
QUP2_SE0[2]	GPIO56	43	SDA	SDA	MISO	CTS	
	GPIO57	44	SCL	SCL	MOSI	RFR	
	GPIO58	46			SCLK	TX	
	GPIO59	47			CS_0	RX	
QUP2_SE1	GPIO60	395	SDA	SDA	MISO	CTS	
	GPIO61	396	SCL	SCL	MOSI	RFR	
	GPIO62	393			SCLK	TX	
	GPIO63	394			CS_0	RX	
QUP2_SE2	GPIO64	37	SDA		MISO	CTS	
	GPIO65	38	SCL		MOSI	RFR	
	GPIO66	40			SCLK	TX	
	GPIO67	41			CS_0	RX	
QUP2_SE3	GPIO68	388	SDA		MISO	CTS	
	GPIO69	389	SCL		MOSI	RFR	
	GPIO70	390			SCLK	TX	
	GPIO71	391			CS_0	RX	
SSC_QUP_SE0	GPIO188	340	SDA	SDA	MISO	CTS	
	GPIO189	345	SCL	SCL	MOSI	RFR	
SSC_QUP_SE2	GPIO192	136	SDA	SDA	MISO	CTS	
	GPIO193	137	SCL	SCL	MOSI	RFR	
	GPIO194	138			SCLK	TX	
	GPIO195	139			CS_0	RX	
SSC_QUP_SE3	GPIO196	140	SDA		MISO	CTS	
	GPIO197	141	SCL		MOSI	RFR	
SSC_QUP_SE8	GPIO208	57	SDA		MISO	CTS	
	GPIO209	60	SCL		MOSI	RFR	
I2CHUB0_SE0	GPIO16	174	SDA				
	GPIO17	189	SCL				
I2CHUB0_SE1	GPIO18	320	SDA				
	GPIO19	288	SCL				
I2CHUB0_SE2	GPIO20 (APPS I2C SDA)	105	SDA				

	GPIO21 (APPS I2C SDA)	108	SCL				
I2CHUB0_SE3	GPIO22	287	SDA				
	GPIO23	286	SCL				
I2CHUB0_SE4	GPIO4	342	SDA				
	GPIO5	343	SCL				
I2CHUB0_SE5	GPIO6	291	SDA				
	GPIO7	290	SCL				
I2CHUB0_SE6	GPIO8	283	SDA				
	GPIO9	308	SCL				
I2CHUB0_SE7	GPIO10	53	SDA				
	GPIO11	402	SCL				
I2CHUB0_SE8	GPIO206	412	SDA				
	GPIO207	413	SCL				
I2CHUB0_SE9	GPIO84	171	SDA				
	GPIO85	346	SCL				

Note: Blue color is the default function, the multiplexing function of the same QUP/SE cannot be used at the same time (I2C and 2-wire URAT cannot be used at the same time).

8. Appendix B: Warning language

8.1 CE Warning Language

EU regulatory conformance:

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of 20cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

EU regulatory conformance:

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of 20cm between the device and the human body. To maintain compliance with RF

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exposure requirement, use product that maintain a 20cm distance between the device and human body.

CE DOC

Hereby,[MeiG Smart Technology Co., Ltd] declares that the radio equipment type [model] is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address:<https://www.meigsmart.com>.

Manufacturer information:

Company name: MeiG Smart Technology Co., Ltd

Address: 2nd Floor,Office Building,No.5 Lingxia Road,Fenghuang,Fuyong Street,Bao'an District,Shenzhen City. China

The 5150 to 5350 MHz and 5945 to 6425 frequency range is restricted to indoor use only in: AT, BE, BG, CH, CY,CZ, DE, DK, EE, EL, ES, FI, FR, HR, HU, IE, IS, IT, LI, LT, LU, LV, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR, UK(NI).

Operation temperature: -30℃~75℃

Operation frequency(Max power)

Bluetooth: 2402-2480 (12dBm)

Wifi:

2412MHz-2472MHz(17.6dBm)

5150MHz-5250MHz(19dBm)

5250MHz-5350MHz(18.9dBm)

5470MHz-5725MHz(19.1dBm)

5745MHz-5850MHz(13.9dBm)

5945MHz-6425MHz(16.6dBm)

8.2 FCC&IC Warning Language

OEM INTEGRATION INSTRUCTIONS:

This device is intended only for OEM integrators under the following conditions:

The module must be installed in the host equipment such that 20 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the internal on-board antenna that has been originally tested and certified with this module. External antennas are not supported. As long as these 3 conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

Validity of using the module certification:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

Upgrade Firmware:

The software provided for firmware upgrade will not be capable to affect any RF parameters as certified for the FCC for this module, in order to prevent compliance issues.

End product labeling:

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: 2APJ4-SNM970”.

Information that must be placed in the end user manual:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

WARNING

Changes or modifications not expressly approved by the manufacturer could void the user' s authority to operate the equipment.

“CAUTION : Exposure to Radio Frequency Radiation.

Antenna shall be mounted in such a manner to minimize the potential for human contact during normal operation. The antenna should not be contacted during operation to avoid the possibility of exceeding the FCC radio frequency exposure limit.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body

IC Information

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- (1) this device may not cause interference, and
- (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme avec Industrie Canada exempts de licence standard RSS (s). L'operation est soumise aux deux conditions suivantes:

- (1) cet appareil ne peut causer d'interferences, et*
- (2) cet appareil doit accepter toute interference, y compris les interferences qui peuvent causer un mauvais fonctionnement de l'appareil.*

The end product must be labeled to display the Industry Canada certification number of the module.

Contains transmitter module IC: 23860-SNM970

Le dispositif d'accueil doivent etre etiquetes pour afficher le numero de certification d'Industrie Canada du module. Contient module emetteur IC: 23860-SNM970

*** This device is going to be operated in 5 150 MHz ~ 5 250 MHz frequency range, it is restricted in indoor environment only.**

Information for OEM Integrator

This device is intended only for OEM integrators under the following conditions:

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

End product labelling

The label for end product must include

“Contains FCC ID: 2APJ4-SNM970, Contains IC: 23860-SNM970”.

“CAUTION: Exposure to Radio Frequency Radiation.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance of 20cm between the radiator

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and your body. This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users."

Requirement per KDB996369 D03

2.2 List of applicable FCC rules

List the FCC rules that are applicable to the modular transmitter. These are the rules that specifically establish the bands of operation, the power, spurious emissions, and operating fundamental frequencies. DO NOT list compliance to unintentional-radiator rules (Part 15 Subpart B) since that is not a condition of a module grant that is extended to a host manufacturer. See also Section 2.10 below concerning the need to notify host manufacturers that further testing is required.³

Explanation: This module meets the requirements of FCC part 15C(15.247). part 15E(15.407)

2.3 Summarize the specific operational use conditions

Describe use conditions that are applicable to the modular transmitter, including for example any limits on antennas, etc. For example, if point-to-point antennas are used that require reduction in power or compensation for cable loss, then this information must be in the instructions. If the use condition limitations extend to professional users, then instructions must state that this information also extends to the host manufacturer's instruction manual. In addition, certain information may also be needed, such as peak gain per frequency band and minimum gain, specifically for master devices in 5 GHz DFS bands.

Explanation: The EUT has a Dipole Antenna, and the antenna use a permanently attached antenna which is not replaceable.

2.4 Limited module procedures

If a modular transmitter is approved as a "limited module," then the module manufacturer is responsible for approving the host environment that the limited module is used with. The manufacturer of a limited module must describe, both in the filing and in the installation instructions, the alternative means that the limited module manufacturer uses to verify that the host meets the necessary requirements to satisfy the module limiting conditions.

A limited module manufacturer has the flexibility to define its alternative method to address the conditions that limit the initial approval, such as: shielding, minimum signaling amplitude, buffered modulation/data inputs, or power supply regulation. The alternative method could include that the limited module manufacturer reviews detailed test data or host designs prior to giving the host manufacturer approval.

This limited module procedure is also applicable for RF exposure evaluation when it is necessary to demonstrate compliance in a specific host. The module manufacturer must state how control of the product into which the modular transmitter will be installed will be maintained such that full compliance of the product is always ensured. For additional hosts other than the specific host originally

granted with a limited module, a Class II permissive change is required on the module grant to register the additional host as a specific host also approved with the module.

Explanation: The module is not a limited module.

2.5 Trace antenna designs

For a modular transmitter with trace antenna designs, see the guidance in Question 11 of KDB Publication 996369 D02 FAQ – Modules for Micro-Strip Antennas and traces. The integration information shall include for the TCB review the integration instructions for the following aspects: layout of trace design, parts list (BOM), antenna, connectors, and isolation requirements.

- a) Information that includes permitted variances (e.g., trace boundary limits, thickness, length, width, shape(s), dielectric constant, and impedance as applicable for each type of antenna);
- b) Each design shall be considered a different type (e.g., antenna length in multiple(s) of frequency, the wavelength, and antenna shape (traces in phase) can affect antenna gain and must be considered);
- c) The parameters shall be provided in a manner permitting host manufacturers to design the printed circuit (PC) board layout;
- d) Appropriate parts by manufacturer and specifications;
- e) Test procedures for design verification; and
- f) Production test procedures for ensuring compliance.

The module grantee shall provide a notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify the module grantee that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

Explanation: Yes, The module with trace antenna designs, and This manual has been shown the layout of trace design, antenna, connectors, and isolation requirements.

2.6 RF exposure considerations

It is essential for module grantees to clearly and explicitly state the RF exposure conditions that permit a host product manufacturer to use the module. Two types of instructions are required for RF exposure information: (1) to the host product manufacturer, to define the application conditions (mobile, portable – xx cm from a person's body); and (2) additional text needed for the host product manufacturer to provide to end users in their end-product manuals. If RF exposure statements and use conditions are not provided, then the host product manufacturer is required to take responsibility of the module through a change in FCC ID (new application).

Explanation: This module complies with FCC RF radiation exposure limits set forth for an uncontrolled environment, This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body." This module is designed to comply with the

FCC statement, FCC ID is: 2APJ4-SNM970.

2.7 Antennas

A list of antennas included in the application for certification must be provided in the instructions. For modular transmitters approved as limited modules, all applicable professional installer instructions must be included as part of the information to the host product manufacturer. The antenna list shall also identify the antenna types (monopole, PIFA, dipole, etc. (note that for example an “omni-directional antenna” is not considered to be a specific “antenna type”)).

For situations where the host product manufacturer is responsible for an external connector, for example with an RF pin and antenna trace design, the integration instructions shall inform the installer that unique antenna connector must be used on the Part 15 authorized transmitters used in the host product. The module manufacturers shall provide a list of acceptable unique connectors.

Explanation: The EUT has a Dipole Antenna, and the antenna use a permanently attached antenna which is unique.

Frequency range (MHz)		Manufacturer	Peak gain (dBi)	Antenna type
BT	2400-2483.5	TOXU TECHNOLOGY CO., LTD.	3.95	Dipole Antenna
WIFI 2.4G	2412-2472	TOXU TECHNOLOGY CO., LTD.		Dipole Antenna
WIFI 5G	5151-5250	TOXU TECHNOLOGY CO., LTD.	2.7	Dipole Antenna
	5250-5350	TOXU TECHNOLOGY CO., LTD.	2.07	Dipole Antenna
	5470-5725	TOXU TECHNOLOGY CO., LTD.	1.48	Dipole Antenna
	5725-5850	TOXU TECHNOLOGY CO., LTD.	1.48	Dipole Antenna
WIFI 6G	5925-6425	TOXU TECHNOLOGY CO., LTD.	0.96	Dipole Antenna
	6425-6525	TOXU TECHNOLOGY CO., LTD.	0.75	Dipole Antenna
	6525-6875	TOXU TECHNOLOGY CO., LTD.	0.77	Dipole Antenna
	6875-7125	TOXU TECHNOLOGY CO., LTD.	1.56	Dipole Antenna

2.8 Label and compliance information

Grantees are responsible for the continued compliance of their modules to the FCC rules. This includes advising host product manufacturers that they need to provide a physical or e-label stating “Contains FCC ID” with their finished product. See Guidelines for Labeling and User Information for RF Devices – KDB Publication 784748.

Explanation: The host system using this module, should have label in a visible area indicated the following texts: “Contains FCC ID: 2APJ4-SNM970”

2.9 Information on test modes and additional testing requirements%

Additional guidance for testing host products is given in KDB Publication 996369 D04 Module Integration Guide. Test modes should take into consideration different operational conditions for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.

The grantee should provide information on how to configure test modes for host product evaluation for different operational conditions for a stand-alone modular transmitter in a host, versus with multiple, simultaneously transmitting modules or

other transmitters in a host.

Grantees can increase the utility of their modular transmitters by providing special means, modes, or instructions that simulates or characterizes a connection by enabling a transmitter. This can greatly simplify a host manufacturer's determination that a module as installed in a host complies with FCC requirements.

Explanation: Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.

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