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SRM700U Hardware Design Manual

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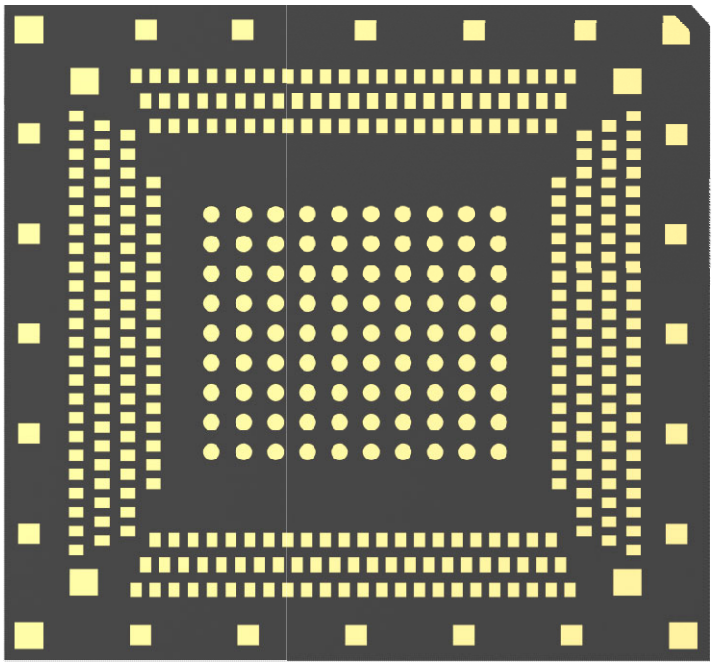

Top and bottom view

Foreword

Thanks for using SRM700U module provided by MeiGSmart. This product can provide data communication service. Please read the user manual carefully before use, you will appreciate its perfect function and simple operation method.

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Before the announcement, the company has the right to modify the contents of this manual according to the needs of technological development.

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Version History

Time	Version	Revision History	Author
2024-03-27	1.00	Initial establishment	Hardware Department

1. Introduction

This document describes the hardware application interfaces of the module,including circuit connections and radio frequency interfaces, which can help users quickly learn about the interface definition, electrical performance, and structural dimensions of the module. Combining this document with other application documents, customers can quickly design various mobile communication solutions.

2.Module Overview

The main chip of SRM700U series module is Qualcomm Snapdragon 5G SoC QCM4490, 8 Kryo™ CPU 6xx (2* GoldA78 2.4GHz + 6*SliverA55 2.0GHz) with 4nm FinFET process.

SRM700U is equipped with 64GB UFS2.2+ 4G LPDDR4X. and support multi-network system including 5GNR/TDD-LTE/FDD-LTE.

SRM700U supports the following operating frequency bands:

North American:

- 5GNR:N2/5/7/8/12/13/14/25/26/38/40/41/66/71/77/78/79
- TDD-LTE: B38/40/41（194M）
- FDD-LTE:B2/4/5/7/8/12/13/14/17/25/26/66/71
- WCDMA:B2/4/5/8

Eurasian:

- 5GNR:N1/3/5/7/8/20/28/38/40/41/77/78/79
- TDD-LTE: B38/40/41（194M）
- FDD-LTE: B1/3/5/7/8/20/26/28
- WCDMA：B1/5/8

China:

- 5GNR:N1/3/5/8/28/41/78/79
- TDD-LTE: B34/38/39/40/41（194M）
- FDD-LTE: B1/3/5/8/28
- WCDMA：B1/8
- CDMA：BC0

SRM700U integrates rich functional interfaces, which can be widely used in products such as video recorder, intelligent cockpit, intelligent POS cash register, logistics terminal, VR Camera, intelligent robot, video monitoring, security monitoring, intelligent information acquisition equipment, intelligent handheld terminal, unmanned aerial vehicle, etc.

The package is 458-pin LGA, and the hardware interface is as follows:

- 1 x LCD(MIPI-DSI)
- 3 x Camera (MIPI-CSI)
- 1 x USB2.0(It can be used as HOST/ DEVCI, and the status needs to be synchronized with USB3.1)
- 1 x USB3.1(It can be used as HOST/ DEVCI, and the status needs to be synchronized with USB2.0)
- 3 x analog MIC input
- 2 x digital MIC
- 2 x I2S(I2S and digital MIC multiplex the same set of physical interfaces)
- 3 x audio output(Headphones, earphones, AUX)

- 2 x USIM card
- 76 x GPIO, partially multiplexed
- 3 x 1.8V UART serial ports, one group supporting four wires and two groups supporting two wires.
- 8 x I2C
- 2 x SPI
- 1 x SD card
- Support GNSS, WiFi, Bluetooth 5.2
- 1 x PWM interface

2.1. Main Features

Table2.1:Main features

Feature	Descri tion
Platform	Qualcomm QCM4490
CPU	8 cores of Kryo CPU 4xx
GPU	Adreno GPU 6XX@812MHz

System memory		UFS2.2+DDR4X, 64GB+4GB/128GB+6GB
operating system		Android 11.0
measure		48.0x47.0x3.0mm, LGA-458pin
-C China		5GNR:N1/3/5/8/28/41/78/79 TDD-LTE: B34/38/39/40/41（194M） FDD-LTE:B1/3/5/8/28 WCDAM：B1/8 CDMA：BC0
-E Eurasia		5GNR:N1/3/5/7/8/20/28/38/40/41/77/78/79 TDD-LTE: B38/40/41（194M） FDD-LTE: B1/3/5/7/8/20/26/28 WCDMA：B1/5/8
-N North American		5GNR:N2/5/7/8/12/13/14/25/26/38/40/41/66/71/77/78/79 TDD-LTE: B38/40/41（194M） FDD-LTE: B2/4/5/7/8/12/13/14/17/25/26/66/71 WCDMA：B2/4/5/8
Wi-Fi		WCN6856: 2x2 IEEE 802.11a/b/g/n/ac/ax 2.4G&5G&6G
Bluetooth		BT 5.2
FM		not support
GNSS		GPS L1&L5/Beidou/Glonass/Galileo/NavIC/QZSS
data insert	5G NR	2.12GMbps/450Mbps
	LTE	Cat 16 FDD-LTE 1200/210Mbps
SIM		DSDSdual card dual standby 3.0/1.8V Support SIM card hot plug 5G SA/NSA + 5G SA/NSA/L/W/1X
Display		FHD+ 120Hz
		LCD Size: User defined
		Interface: LCM: MIPI DSI 4-lane;
Camera		Interface:Can support three groupsCSI, each group is 4-Lane, supporting D-PHY 1.2 or C-PHY 1.2.
		Triple 14-bit image signal processing (ISP) + two lite ISP 16 + 16 /22MP 25 MP/30 fps
		Video decode: 1080P60D for H.264/H.265/VP9
		Video encode: Up to 1080P60E for H.264/H.265
input device		Button(PWRKEY, Home, RESET, VOL+, VOL-）
		Capacitive TP
Reset		Support hardware reset
		Interface name: Main function description
		VBAT: 8pin, Module power input, 3.5V～4.2V, nominal value 3.8V.
		SDIO *1: TF Card, Maximum support 256GB.

Application interface	USB2.0	Support OTG(OTG power supply needs to be external, and HOST/ DEVCI needs to be synchronized with USB3.1). USB_BOOT (forced USB boot for emergency download)
	USB3.1	Support OTG(OTG power supply needs to be external, and HOST/ DEVCI needs to be synchronized with USB2.0). USB_BOOT (forced USB boot for emergency download)
	BLSP ports	QUP(SE0~SE7), QUP1(SE1~SE6), 4-bits each, multiplexed serial interface functions
	UART	By default, it supports 3-way UART (which can be extended through QUP interface).
	I2C*8	By default, 8 groups of I2C are supported, including 4 groupsof dedicated I2C (3 groups of CAM, 1 group of SENSOR), (which can be extended through QUP interface).
	SPI(master only)	Two groups of SPI are supported by default (which can be extended through QUP interface).
	ADC*2	Support 2 groups of ADC
	Charging	Support external expansion *
	motor	not support
	GPIO	76 GPIO interfaces, some of which are multiplexed
	VCOIN	RTC Battery
	RF interface	ANT0(3G/4G/N1/3/5/7/8/20/28TRX ,N41/77/78/79RX) ANT1(3G/4G/N1/3/5/7/8/20/28/40 RX,N41/77/78/79 RX) ANT2 (N41/77/78/79 TRX) ANT3 (N41/77/78/79 RX) GNSS (L1+L5 antenna) WiFi/BT ANT0 WiFi/BT ANT1
	Audio	Three groups of analog MIC interfaces (including analog headset MIC) Two groups of digital MIC interfaces 2 sets of I2S interfaces (physical interfaces multiplexed with digital MIC) 1 group of AUX signals (external audio PA required) 1 group of earphones 1 group of stereo headphones (including headphone MIC)

2.2. Block Diagram

The following figure lists the main functional parts of the module:

- QCM4490 Baseband chip
- PM4450, PM4450C, PMK4450Power management chip
- WCN6856-WIFI/BT 2-in-1 chip

- Antenna interface
- LCD/CAM-MIPI interface
- UMCP memory chip
- AUDIO interface
- USB, SD card interface, SIM card interface, etc.

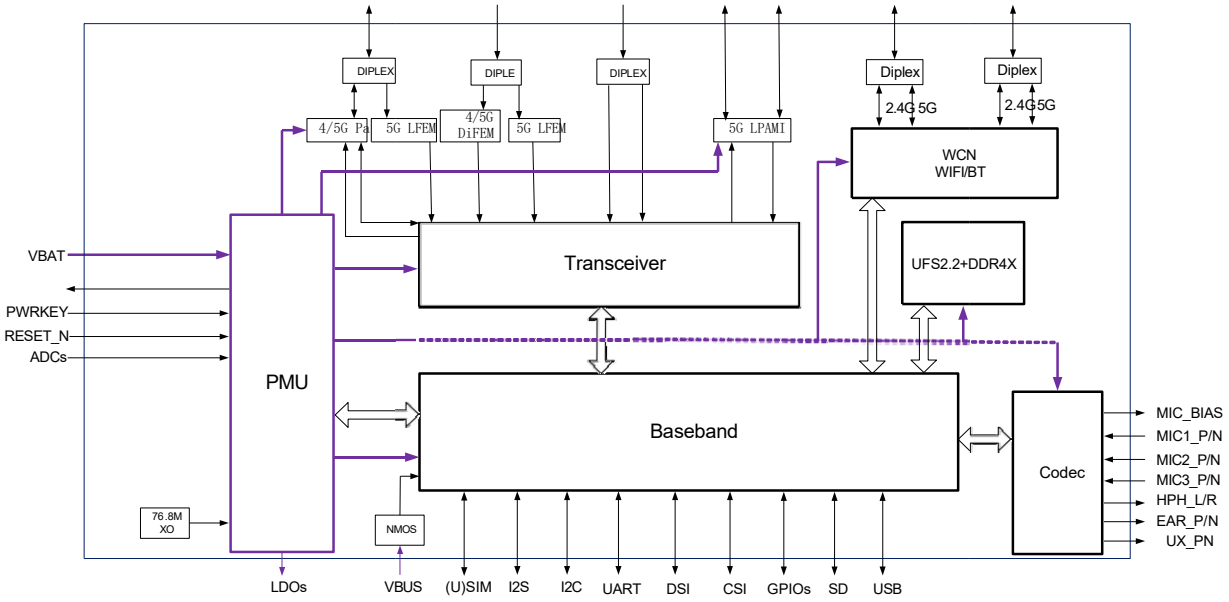


Fig2.1: Module function block diagram

3. Module Package

3.1. Pin Distribution Diagram

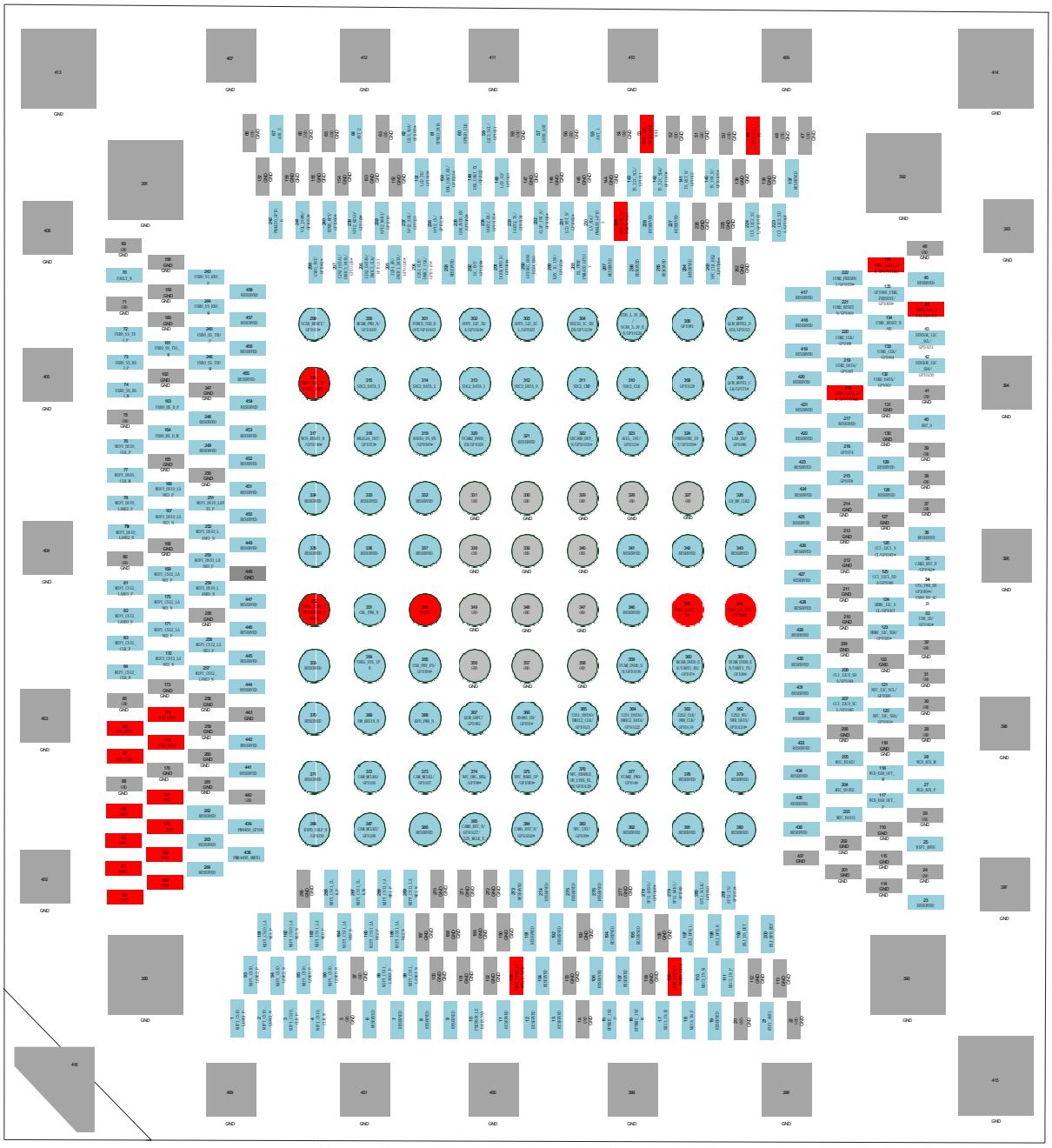


Fig3.1: Module pin diagram (top view)

3.2. Module Pin Description

Table3.1:Pin description

Pin Number	Pin Name	GPIO Interrupt	Pad Characteristics	Functional Description
1	MIPI_CSI0_LANE1_P		AI/AO	MIPI-CSI0Differential data signal
2	MIPI_CSI0_LANE1_N		AI/AO	
3	MIPI_CSI0_CLK_P		AI/AO	MIPI-CSI0Differential clock signal
4	MIPI_CSI0_CLK_N		AI/AO	
5	GND		GND	GND
6	RESERVED			Reserved
7	RESERVED			Reserved
8	RESERVED		AO	Reserved
9	RESERVED		AO	Reserved
10	PSENSOR_LEDA(VREG_L7E 3.3V)		PO	Optical distance sensing LED anode
11	RESERVED			Reserved
12	RESERVED			Reserved
13	RESERVED			Reserved
14	GND		GND	GND
15	HPHMIC_IN2_P		AI	Headphone MIC differential input
16	HPHMIC_IN2_M		AI	
17	MIC3_IN_M		AI	MIC3differential input
18	MIC3_IN_P		AI	
19	VREG_S9B（WCN1.8V）		PO	Reserved power PIN
20	GND		GND	GND
21	WIFI_ANT1		AI	WIFI antenna interface1
22	GND		GND	GND
23	RESERVED			Reserved
24	GND		GND	GND
25	WIFI_ANT0		AI	WIFI antenna interface0
26	GND		GND	GND
27	WCD_AUX_P		AO	Class AB output, which can be used as external PA input.
28	WCD_AUX_M		AO	
29	GND			GND
30	GND			GND
31	GND			GND
32	GND			GND
33	USB_ID/GPIO41*		B-PD:nppukp	USB ID
34	OTG_PWR_ENGPIO99*/USB0_HS_AC_EN	GPIO99*	B-PD:nppukp	Configurable I/O
35	CAM2_RST_N/GPIO42*	GPIO42*	B-PD:nppukp	Configurable I/O, Used as CAM2 reset signal by default.
36	RESERVED			Reserved
37	GND		GND	GND
38	GND		GND	GND

39	GND		GND	GND
40	ANT_0		AI/AO	Main antenna interface0
41	GND		GND	GND
42	SENSOR_I2C_SDA/GPIO130		B-PD:nppukp	Dedicated to Sensor I2C
43	SENSOR_I2C_SCL/GPIO131		B-PD:nppukp	
44	VREG_L28B_2P96(SDVIO)		PO	T-card signal pull-up power supply will be turned OFF when standby.
45	RESERVED			Reserved
46	GND		GND	GND
47	GND		GND	GND
48	GND		GND	GND
49	VREG_L2E_1P2		PO	Reserve power supply, default NC
50	GND		GND	GND
51	GND		GND	GND
52	GND		GND	GND
53	VREG_L6E_3P0(SENSOR_VDD)		PO	3V power output, which will be OFF when standby, is used for sensor and TP power supply
54	GND		GND	GND
55	ANT_1		AI/AO	Main antenna interface1
56	GND		GND	GND
57	GNSS_ANT		AI/AO	GNSSantenna interface
58	GND		GND	GND
59	I2C3_SCL/GPIO51		B-PD:nppukp	I2C3 is reserved for external charging IC.
60	SPMI0_CLK		AI/AO	Reserve PMI use
61	SPMI0_DATA		AI/AO	Reserve PMI use
62	I2C3_SDA/GPIO50*		B-PD:nppukp	I2C3 is reserved for external charging IC
63	GND		GND	GND
64	ANT_2		AI/AO	Main antenna interface2
65	GND		GND	GND
66	GND		GND	GND
67	ANT_3		AI/AO	Main antenna interface3
68	GND		GND	GND
69	GND		GND	GND
70	FAULT_N		AI	PMI_FAULTsignal
71	GND		GND	GND
72	USB0_SS_TX1_P		AO	USB3.1channel1Differential data signal
73	USB0_SS_RX1_P		AI	
74	USB0_SS_RX1_M		AI	
75	GND		GND	GND
76	MIPI_DSI0_CLK_P		AI/AO	MIPI-DSIDifferential clock signal
77	MIPI_DSI0_CLK_M		AI/AO	
78	MIPI_DSI0_LANE2_P		AI/AO	MIPI-DSIDifferential data signal
79	MIPI_DSI0_LANE2_N		AI/AO	
80	GND		GND	GND
81	MIPI_CSI2_LANE0_P		AI/AO	MIPI-CSI2Differential data signal

82	MIPI_CSI2_LANE0_N		AI/AO	
83	MIPI_CSI2_CLK_P		AI/AO	MIPI-CSI2Differential clock signal
84	MIPI_CSI2_CLK_N		AI/AO	
85	GND		GND	GND
86	USB_VBUS		AI	USB insertion detection interrupt
87	USB_VBUS		AI	
88	GND		GND	GND
89	VBAT		PI	Module power supply input, voltage range 3.5-4.2V, typical value 3.8V
90	VBAT		PI	
91	VBAT		PI	
92	VBAT		PI	
93	MIPI_CSI0_LANE2_P		AI/AO	MIPI-CSI0Differential data signal
94	MIPI_CSI0_LANE2_N		AI/AO	
95	MIPI_CSI0_LANE0_P		AI/AO	
96	MIPI_CSI0_LANE0_N		AI/AO	
97	GND		GND	GND
98	MIPI_CSI1_LANE3_P		AI/AO	MIPI-CSI1Differential data signal
99	MIPI_CSI1_LANE3_N		AI/AO	
100	GND		GND	GND
101	GND		GND	GND
102	GND		GND	GND
103	VREG_L21B_1P8(LCD_VIO)		PO	1.8V power output, ON in standby, can be used for LCD IO power supply.
104	RESERVED			Reserved
105	GND		GND	GND
106	RESERVED		AI/AO	MIPI-CSI3Differential data signal
107	RESERVED		AI/AO	
108	GND		GND	GND
109	VREG_3P072_L25B(USBHS_VIO)		PO	3.1V power output, which is used for USB_HS_3.0_VIO and other related power supplies and will be turned OFF when standby.
110	MIC3_IN_M		AI	MIC3Differential input
111	MIC3_IN_P		AI	
112	GND		GND	GND
113	GND		GND	GND
114	GND		GND	GND
115	GND		GND	GND
116	GND		GND	GND
117	WCD_EAR_OUT_P		AO	Earphone differential outputEarphone differential output
118	WCD_EAR_OUT_M		AO	
119	GND		GND	GND
120	GPIO91I2C_SDA *	GPIO91*	B-PD:nppukp	Configurable I/O
121	NFC_I2C_SCL/GPIC90	GPIO90	B-PD:nppukp	
122	GND		GND	GND
123	GPIO26*	GPIO26*	B-PD:nppukp	Configurable I/O

124	GPIO27*	GPIO27*	B-PD:nppu kp	
125	_I2C1_SDA/GPIO46		B-PD:nppu kp	I2C1 Dedicated to CAM
126	_I2C1_SCL/GPIO47*		B-PD:nppu kp	
127	GND		GND	GND
128	RESERVED			Reserved
129	RESERVED			Reserved
130	GND		GND	GND
131	GND		GND	GND
132	UIM1_DATA/GPIO63		B-PD:nppu kp	SIM card 1 data signal
133	UIM1_CLK/GPIO64		B-PD:nppu kp	Clock signal of SIM card 1
134	UIM1_RESET_N/65		B-PD:nppu kp	Reset signal of SIM card 1
135	GPIO66_UIM1_PRESENT/GPIO66*		B-PD:nppu kp	SIM card 1 hot plug signal
136	VREG_L26B_1P8/3P0(VSIM1)		PO	SIM card 1 power supply
137	RESERVED			Reserved
138	GND		GND	GND
139	GND		GND	GND
140	TS_INT_N/GPIO105*	GPIO105*	B-PD:nppu kp	Configurable I/O, Used as TP interrupt by default
141	TS_RST_N/GPIO12*	GPIO12*	B-PD:nppu kp	Configurable I/O, Used as TP reset by default
142	TS_I2C_SDA/GPIO10*		B-PD:nppu kp	Configurable I/O, Used as TP I2C by default
143	TS_I2C_SCL/GPIO11*		B-PD:nppu kp	
144	GND		GND	GND
145	GND		GND	GND
146	GND		GND	GND
147	GND		GND	GND
148	LCD_ID/GPIO40*	GPIO40*	B-PD:nppu kp	Configurable I/O
149	DBG_UART_TX/GPIO22*		B-PD:nppu kp	Used as a module debug UART by default
150	DBG_UART_RX/GPIO23*		B-PD:nppu kp	
151	LCD_TE/GPIO93*		B-PD:nppu kp	Configurable I/O, Used as LCD frame synchronization signal by default
152	GND		GND	GND
153	GND		GND	GND
154	GND		GND	GND
155	GND		GND	GND
156	GND		GND	GND
157	GND		GND	GND
158	GND		GND	GND
159	GND		GND	GND
160	GND		GND	GND

161	USB0_SS_TX1_M		AO	USB3.1channel1Differential data signal
162	GND		GND	GND
163	USB0_HS_D_P		AI/AO	USB2.0Differential data signal
164	USB0_HS_D_M		AI/AO	
165	GND		GND	GND
166	MIPI_DSI0_LANE3_P		AI/AO	MIPI-DSIDifferential data signal
167	MIPI_DSI0_LANE3_N		AI/AO	
168	GND		GND	GND
169	MIPI_CSI2_LANE1_P		AI/AO	MIPI-CSI2Differential data signal
170	MIPI_CSI2_LANE1_N		AI/AO	
171	MIPI_CSI2_LANE2_P		AI/AO	
172	MIPI_CSI2_LANE2_N		AI/AO	
173	GND		GND	GND
174	USB_VBUS		AI	USB interrupt detectionUSB interrupt detection
175	USB_VBUS		AI	
176	GND		GND	GND
177	VBAT		PI	Module power supply input, voltage range 3.5-4.2V, typical value 3.8V
178	VBAT		PI	
179	VBAT		PI	
180	VBAT		PI	
181	MIPI_CSI0_LANE3_P		AI/AO	MIPI-CSI0Differential data signal
182	MIPI_CSI0_LANE3_N		AI/AO	
183	MIPI_CSI1_LANE0_P		AI/AO	MIPI-CSI1Differential data signal
184	MIPI_CSI1_LANE0_N		AI/AO	
185	MIPI_CSI1_LANE2_P		AI/AO	
186	MIPI_CSI1_LANE2_N		AI/AO	
187	GND		GND	GND
188	GND		GND	GND
189	GND		GND	GND
190	GND		GND	GND
191	RESERVED			Reserved
192	RESERVED			
193	GND		GND	GND
194	RESERVED			Reserved
195	RESERVED			
196	GND		GND	GND
197	EAR_HPH_L		AO	Headphones left and right channels
198	EAR_HPH_R		AO	
199	EAR_HS_DET		DI	Earphone plugging and unplugging detection
200	EAR_HPH_REF		AI	Headphone ground reference
201	GND		GND	GND
202	GND		GND	GND
203	MIC_BIAS1		AO	MIC bias voltage output
204	MIC_BIAS2		AO	
205	MIC_BIAS3		AO	
206	GND		GND	GND
207	_I2C0_SCL/GPIO45		B-PD:nppu	I2C0 Dedicated to CAM

			kp	
208	_I2C0_SDA/GPIO44		B-PD:nppu kp	
209	GND		GND	GND
210	GND		GND	GND
211	GND		GND	GND
212	GND		GND	GND
213	GND		GND	GND
214	GND		GND	GND
215	GPIO78	GPIO78	B-PD:nppu kp	Configurable I/O, Used as GRFC interface by default
216	GPIO74	GPIO74	B-PD:nppu kp	Configurable I/O, Used as GRFC interface by default
217	RESERVED			Reserved
218	VREG_L27B_1P8_3P0(VSIM2)		PO	SIM card 2 power supply
219	UIM2_DATA/GPIO67*		B-PD:nppu kp	SIM card 2 data signal
220	UIM2_CLK/GPIO68		B-PD:nppu kp	Clock signal of SIM card 2
221	UIM2_RESET_N/GPIO69		B-PD:nppu kp	SIM card 2 reset signal
222	UIM2_PRESENT/GPIO70*	GPIO70*	B-PD:nppu kp	SIM card 2 hot plug detection signal
223	_I2C2_SDA/GPIO48		B-PD:nppu kp	I2C2 Dedicated to CAM
224	_I2C2_SCL/GPIO49		B-PD:nppu kp	
225	GND		GND	GND
226	GND		GND	GND
227	RESERVED			Reserved
228	RESERVED			Reserved
229	VREG_L3E_2P8(WCN_VDD)		PO	2.8V power output for WCN_VDD power supply
230	LV_ADC/PM4450_GPIO5	PM4450_GPIO5	B-PD:nppu kp	LV_ADC input(0-1.8V)/ PM4450Configurable I/O
231	LCD_RST_N/GPIO92*	GPIO92*	B-PD:nppu kp	Configurable I/O, Used as LCD reset by default
232	ALSP_INT_N/GPIO58*	GPIO58*	B-PD:nppu kp	Used asOptical distance sensing interruptionby default
233	UART_TX/GPIO134	GPIO134	B-PD:nppu kp	Configurable I/O, Configurable as UART2
234	UART_RX/GPIO135*	GPIO135*	B-PD:nppu kp	
235	CAM_AVDD_EN/GPIO62*	GPIO62*	B-PD:nppu kp	Configurable I/O
236	SPI2_CS/GPIO21*	GPIO21*	B-PD:nppu kp	Configurable I/O, Configurable as SP2
237	SPI2_SCK/GPIO20	GPIO20	B-PD:nppu kp	
238	SPI2_MOSI/GPIO19	GPIO19	B-PD:nppu kp	
239	SPI2_MISO/GPIO18*	GPIO18*	B-PD:nppu kp	
240	HOME_KEY/GPIO60*	GPIO60*	B-PD:nppu	Configurable I/O, The default is the

			kp	HOME key
241	VOL_DOWN/GPIO53*	GPIO53*	B-PD:nppu kp	Configurable I/O, The default is VOL-key
242	PM4450_GPIO6	PM4450_ GPIO6	B-PD:nppu kp	Configurable I/O
243	USB0_SS_RX0_P		AI	USB3.1channel0Differential data signal
244	USB0_SS_RX0_M		AI	
245	USB0_SS_TX0_P		AO	
246	USB0_SS_TX0_M		AO	
247	GND		GND	GND
248	RESERVED			Reserved
249	RESERVED			
250	GND		GND	GND
251	MIPI_DSI0_LANE1_P		AI/AO	MIPI-DSIDifferential data signal
252	MIPI_DSI0_LANE1_N		AI/AO	
253	MIPI_DSI0_LANE0_P		AI/AO	
254	MIPI_DSI0_LANE0_N		AI/AO	
255	GND		GND	GND
256	MIPI_CSI2_LANE3_P		AI/AO	MIPI-CSI2Differential data signal
257	MIPI_CSI2_LANE3_N		AI/AO	
258	GND		GND	GND
259	GND		GND	GND
260	GND		GND	GND
261	GND		GND	GND
262	RESERVED			Reserved
263	RESERVED			Reserved
264	RESERVED			Reserved
265	GND		GND	GND
266	MIPI_CSI1_CLK_P		AI/AO	MIPI-CSI1Differential clock signal
267	MIPI_CSI1_CLK_M		AI/AO	
268	MIPI_CSI1_LANE1_P		AI/AO	MIPI-CSI1Differential data signal
269	MIPI_CSI1_LANE1_N		AI/AO	
270	GND		GND	GND
271	GND		GND	GND
272	GND		GND	GND
273	RESERVED			Reserved
274	RESERVED			
275	RESERVED			
276	RESERVED			
277	GND		GND	GND
278	SPI1_MISO/GPIO0*	GPIO0*	B-PD:nppu kp	Configurable I/O, Configurable as SP1
279	SPI1_MOSI/GPIO1	GPIO1	B-PD:nppu kp	
280	SPI1_SCLK/GPIO2	GPIO2	B-PD:nppu kp	
281	SPI1_CS/GPIO3*	GPIO3*	B-PD:nppu kp	
282	GND		GND	GND
283	NFC_CLK_REQ/GPIO98	GPIO98*	B-PD:nppu	Configurable I/O

	*		kp	
284	RESERVED			Reserved
285	RESERVED			Reserved
286	RESERVED			Reserved
287	RESERVED			Reserved
288	BL_PWM/PM4450_GPIO7	PM4450_GPIO7	B-PD:nppukp	Configurable I/O, Used as backlight PWM modulation signal by default.
289	KEY_IC_INT/GPIO52*	GPIO52*	B-PD:nppukp	Configurable I/O
290	GPIO85_GNSS_ELNA_EN0	GPIO85	B-PD:nppukp	GRFC_GPIO
291	DCAM_PWD_N/GPIO84*	GPIO84*	B-PD:nppukp	Configurable I/O, By default, it is used as depth of field CAM sleep signal.
292	DC_INT/GPIO28*	GPIO28*	B-PD:nppukp	Configurable I/O
293	RESERVED			Reserved
294	I2S1_CLK/DMIC1_CLK/GPIO115*	GPIO115*	B-PD:nppukp	Configurable I/O, Can be configured as I2S1 or digital MIC interface.
295	I2S1_WS/DMIC1_DATA/GPIO116	GPIO116	B-PD:nppukp	
296	I2S2_DATA0/DMIC3_CLK/GPIO117	GPIO117	B-PD:nppukp	Configurable I/O, Can be configured as I2S2 or digital MIC interface.
297	I2S2_DATA1/DMIC3_DATA/GPIO118*	GPIO118*	B-PD:nppukp	
298	GYRO_INT/GPIO61*	GPIO61*	B-PD:nppukp	Used as gyro interrupt by default.
299	SCAN_RESET/GPIO13*	GPIO13*	B-PD:nppukp	Configurable I/O
300	MCAM_PWD_N/GPIO100	GPIO100	B-PD:nppukp	Configurable I/O, By default, it is used as the sleep signal of the rear camera
301	FORCE_USB_BOOT/GPIO103		B-PD:nppukp	Emergency download (active high)
302	APPS_I2C_SDA/GPIO24*	GPIO24*	B-PD:nppukp	Configurable I/O, Configurable as I2C
303	APPS_I2C_SCL/GPIO25	GPIO25	B-PD:nppukp	
304	RS232_IC_SHDN/GPIO123*	GPIO123*	B-PD:nppukp	Configurable I/O
305	EVB_3.3V_EN/SCAN_3.3V_EN/GPIO126	GPIO126	B-PD:nppukp	Configurable I/O
306	GPIO81	GPIO81	B-PD:nppukp	Configurable I/O
307	QCM_RFFE1_DATA/GPIO72	GPIO72	B-PD:nppukp	GPIO Dedicated to RF (external pull-up and pull-down are not allowed)
308	QCM_RFFE1_CLK/GPIO71*	GPIO71*	B-PD:nppukp	GPIO Dedicated to RF (external pull-up and pull-down are not allowed)
309	GPIO128	GPIO128	B-PD:nppukp	Configurable I/O
310	SDC2_CLK		DO-NP:pdpukp	T card clock signal
311	SDC2_CMD		BH-NP:pdpukp	T card control signal
312	SDC2_DATA_0		BH-NP:pdp	T-card data signal

			ukp	
313	SDC2_DATA_1		BH-NP:pdpukp	
314	SDC2_DATA_2		BH-NP:pdpukp	
315	SDC2_DATA_3		BH-NP:pdpukp	
316	VREG_24B_2P96(SD_VDD)		PO	T-card power supply, which will turn OFF when standby
317	WCD_RESET_N/GPIO96*	GPIO96*	B-PD:nppukp	Dedicated to external codec reset
318	WK2124_INT/GPIO73*	GPIO73*	B-PD:nppukp	Configurable I/O
319	AUDIO_PA_EN/GPIO95*	GPIO95*	B-PD:nppukp	Configurable I/O, Used as PA enable by default
320	FCAM2_DVDD_EN/GPIO29	GPIO29	B-PD:nppukp	Configurable I/O
321	RESERVED			Reserved
322	SDCARD_DET_N/GPIO101*	GPIO101*	B-PD:nppukp	T card hot plug detection
323	ACCL_INT/GPIO33*	GPIO33*	B-PD:nppukp	Used as accelerometer interrupt by default.
324	PRESSURE_INT/GPIO59*	GPIO59*	B-PD:nppukp	Configurable I/O
325	LAN_EN/GPIO86	GPIO86	B-PD:nppukp	GPIODedicated to RF（External cannot be pulled up or down）
326	LN_BB_CLK2		AO	19.2MHz clock output, not configured
327	GND		GND	GND
328	GND		GND	GND
329	GND		GND	GND
330	GND		GND	GND
331	GND		GND	GND
332	RESERVED			Reserved
333	RESERVED			Reserved
334	RESERVED			Reserved
335	RESERVED			Reserved
336	RESERVED			Reserved
337	RESERVED			Reserved
338	GND		GND	GND
339	GND		GND	GND
340	GND		GND	GND
341	RESERVED			Reserved
342	RESERVED			Reserved
343	RESERVED			Reserved
344	VREG_L4E_3P0(TPVDD)		PO	3.0V power output, which can be used for TP VDD power supply, and can be turned OFF in standby
345	VREG_L21B_1P8		PO	1.8V power output, used for CPU, Memory, IO and other power supply.After turning on the machine, always output
346	QCM_RST_OUT_N		AO	Reserved
347	GND		GND	GND

348	GND		GND	GND
349	GND		GND	GND
350	VCOIN		AI/AO	RTC power supply
351	CBL_PWR_N		DI	Power-on automatic power-on signal, which can be used as AC plug-in automatic power-on (low effective)
352	VREG_L21B_1P8(SENSOR_VDDIO)		PO	1.8V power output, used as IO power supply for Sensor, CAM and TP
353	RESERVED			Reserved
354	VREG_SYS_1P8		PO	System 1.8V power output.Power supply alway outputs
355	USB_PHY_PS/GPIO94*		B-PD:nppukp	Dedicated GPIO port, used as USB interface selection, microUSB is connected to GND with 1K resistor
356	GND		GND	GND
357	GND		GND	GND
358	GND		GND	GND
359	FCAM_DVDD_EN/GPIO106	GPIO106	B-PD:nppukp	Configurable I/O
360	MCAM_DVDD_EN/UART1_RX/GPIO7*	GPIO7*	B-PD:nppukp	Configurable I/O, Can be configured as UART1
361	DCAM_DVDD_EN/UART1_TX/GPIO6*	GPIO6*	B-PD:nppukp	
362	I2S2_WS/SWR_DATA/GPIO120*	GPIO120*	B-PD:nppukp	Configurable I/O, Can be configured as I2S2
363	I2S2_CLK/SWR_CLK/GPIO119	GPIO119	B-PD:nppukp	
364	I2S1_DATA1/DMIC2_DATA/GPIO122	GPIO122	B-PD:nppukp	Configurable I/O, Can be configured as I2S1 or digital MIC interface
365	I2S1_DATA0/DMIC2_CLK/GPIO121*	GPIO121*	B-PD:nppukp	
366	RS485_EN/GPIO5*	GPIO5*	B-PD:nppukp	Configurable I/O
367	QCM_GRFC/GPIO82	GPIO82	B-PD:nppukp	GPIODedicated to RF
368	KPD_PWR_N		DI	On/off signal
369	PM_RESIN_N		DI	Module reset signal
370	RESERVED			Reserved
371	RESERVED			Reserved
372	CAM_MCLK0/GPIO36		B-PD:nppukp	Used as CAM master clock 0 by default
373	CAM_MCLK1/GPIO37		B-PD:nppukp	Used as CAM master clock 0 by default
374	NFC_DWL_REQ/GPIO8*	GPIO8	B-PD:nppukp	Configurable I/O, Configurable as UART1 CTS
375	NFC_WAKE_UP/GPIO83*	GPIO83*	B-PD:nppukp	Configurable I/O
376	NFC_ENABLE_OR_LVDS_BL_EN/GPIO129	GPIO129	B-PD:nppukp	Configurable I/O
377	FCAM2_PWD/GPIO4*	GPIO4*	B-PD:nppukp	Configurable I/O, It is used as the sleep signal of the front camera by default.
378	RESERVED			Reserved

379	RESERVED			Reserved
380	RESERVED			Reserved
381	RESERVED			Reserved
382	RESERVED			
383	NFC_INT/GPIO9*	GPIO9*	B-PD:nppu kp	Configurable I/O, Can be configured as UART RFR_N
384	CAM1_RST_N/GPIO102 *	GPIO102 *	B-PD:nppu kp	Configurable I/O , Used as CAM1 reset signal by default
385	CAM0_RST_N/GPIO127 /I2S_MCLK_E	GPIO127	B-PD:nppu kp	Configurable I/O , Used as the input of CAM0 reset signal /I2S MCLK by default
386	RESERVED			Reserve
387	CAM_MCLK2/GPIO38		B-PD:nppu kp	Used as CAM master clock 2 by default
388	KYPD_VOLP_N /GPIO30*	GPIO30*	B-PD:nppu kp	Used as volume-key by default
389	GND		GND	GND
390	GND		GND	GND
391	GND		GND	GND
392	GND		GND	GND
393	GND		GND	GND
394	GND		GND	GND
395	GND		GND	GND
396	GND		GND	GND
397	GND		GND	GND
398	GND		GND	GND
399	GND		GND	GND
400	GND		GND	GND
401	GND		GND	GND
402	GND		GND	GND
403	GND		GND	GND
404	GND		GND	GND
405	GND		GND	GND
406	GND		GND	GND
407	GND		GND	GND
408	GND		GND	GND
409	GND		GND	GND
410	GND		GND	GND
411	GND		GND	GND
412	GND		GND	GND
413	GND		GND	GND
414	GND		GND	GND
415	GND		GND	GND
416	GND		GND	GND
417	RESERVED			Reserved
418	RESERVED			
419	RESERVED			
420	RESERVED			
421	RESERVED			
422	RESERVED			

423	RESERVED			
424	RESERVED			
425	RESERVED			Reserved
426	RESERVED			
427	RESERVED			Reserved
428	RESERVED			
429	RESERVED			Reserved
430	RESERVED			
431	RESERVED			
432	RESERVED			
433	RESERVED			
434	RESERVED			
435	RESERVED			
436	RESERVED			
437	GND		GND	GND
438	PMK4450_AMUX1		AI	LV_ADC input
439	PM4450_GPIO9		AI	PMU GPIO9
440	GND		GND	GND
441	RESERVED			Reserved
442	RESERVED			
443	GND		GND	GND
444	RESERVED			Reserved
445	RESERVED			Reserved
446	RESERVED			Reserved
447	RESERVED			Reserved
448	GND		GND	GND
449	RESERVED			Reserved
450	RESERVED			Reserved
451	RESERVED			Reserved
452	RESERVED			Reserved
453	RESERVED			Reserved
454	RESERVED			Reserved
455	RESERVED			Reserved
456	RESERVED			Reserved
457	RESERVED			Reserved
458	RESERVED			Reserved

remarks:

*: Interrupt pin that can wake up the system
B: Bidirectionaldigital with CMOS input
H: High-voltage tolerant
NP: pdpukp=defaultno-pull with programmable options following the colon (:)
PD: nppukp=defaultpulldown with programmable options following the colon (:)
PU: nppdkp=defaultpullup with programmable options following the colon (:)
KP: nppdpu=defaultkeeper with programmable options following the colon (:)

3.3. Mechanical Dimension

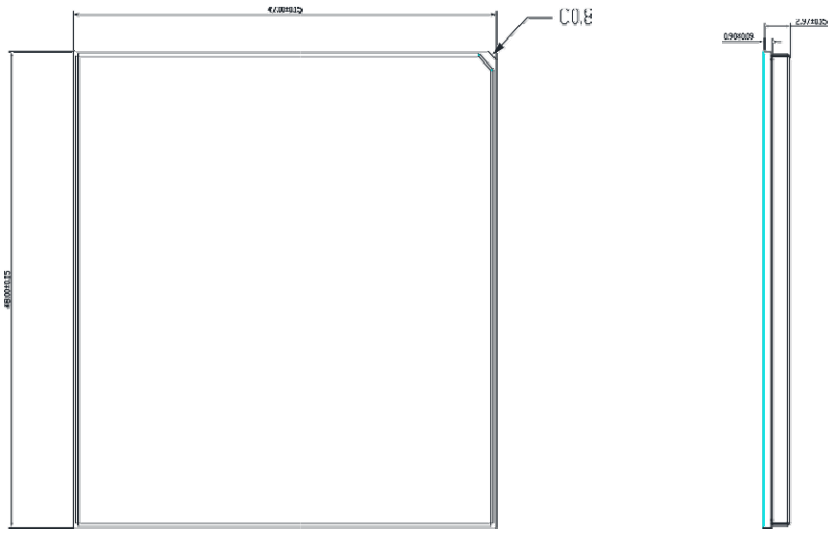


Fig3.2: Module dimension (top, side view)（mm）

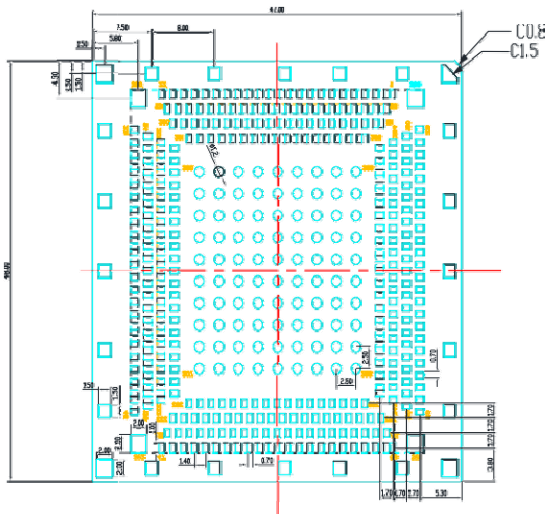


Fig3.3: Module dimension (bottom view)（mm）

4. Interface Application

4.1. Power Supply

For battery-powered devices, the VBAT module has a voltage input range of 3.5V to 4.2V. In 5G band, when the module is transmitted at maximum power, the current peak can reach up to 4A instantly, resulting in a large voltage drop on VBAT. It is recommended to use a large capacitor to stabilize voltage close to VBAT. It is recommended to use two47uF ceramic capacitors, parallel connection of 33pF and 10pF capacitors in parallel can effectively remove high-frequency interference. At the same time, in order to prevent ESD and surge damage to the chip, it is recommended to use appropriate TVS tube and 5.1V/500mW zener diodeat module VBAT pin. When PCB layout, capacitor and diode should be as close as possible to module VBAT pin. The user can directly power the module with a 3.8v lithium ion battery. When using the battery, the impedance between the VBAT pin and the battery should be less than 150mΩ.

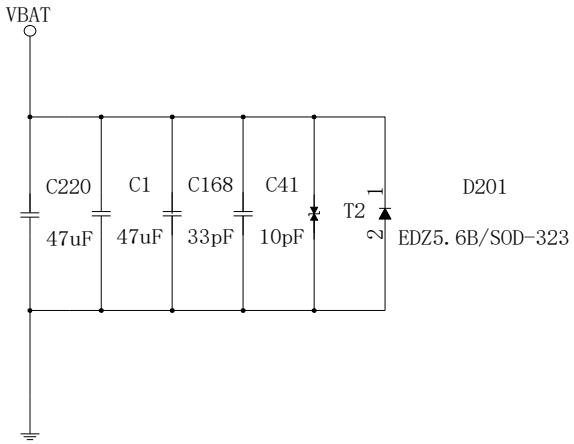


Fig4.1: VBAT input reference circuit

If it is a DC power supply device,DC input voltage is 5V-12V. The following figure shows the recommended circuit for using DC-DCpower supply:

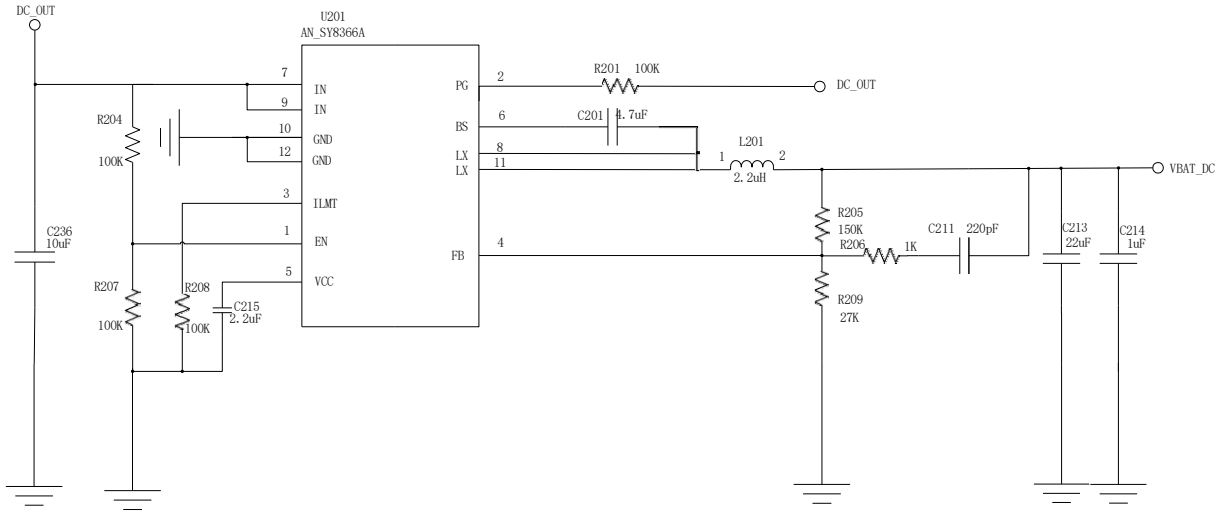


Fig4.2: DC-DC power supply circuit

4.1.1. Power Supply Pins

The VBAT pins (89, 90, 91, 92, 177, 178, 179, 180) are used for power input. In the user's design, please pay special attention to the design of the power supply part to ensure that the drop of VBAT is not less than 3.5V even when the module consumption reaches 4A. If the voltage drop is less than 3.5V, the module may shut down. PCB wiring from VBAT pins to the power supply should be wide enough to reduce voltage sags in transmission burst mode.

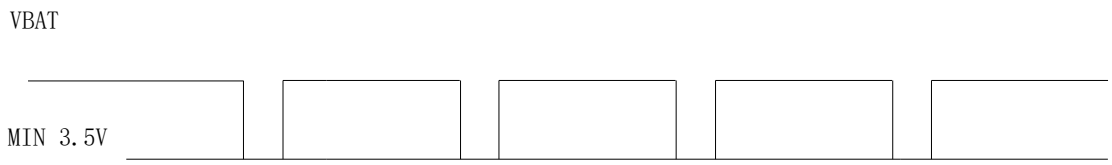


Fig4.3: VBAT lowest voltage sag

4.1.2. Power PCB Layout

Power supply wiring should not only consider VBAT, but also consider the return GND of power supply.The wiring of the positive electrode of VBAT must be short and thick. Be sure to pass through the large capacitor, Zener diode and then to the power supply PIN of the module.There are many exposed copper pads at the bottom of the module, so it is necessary to ensure that the GND path from these exposed copper areas to the power supply is the shortest and unobstructed.This can ensure the shortest current path of the whole power supply and the minimum interference.

4.2. Power on/off

Do not turn on the module when the temperature and voltage upper lim ts of the module are exceeded. In extreme cases such operations can cause permanent damage to the module.

4.2.1. Power on

The user can start the module by pulling down the KPD_PWR_N pin (368) for at least 3 seconds. The pin has been pulled up to the 1.8V power supply in the module.,Unsustainable pull-down.The recommended circuit is as follows:Or pull down the pin of CBL_PWR_N (351). CBL_PWR_N can realize the function of automatic power-on by pulling down the resistor to GND at 1K, and it is not necessary to release this signal after starting up.

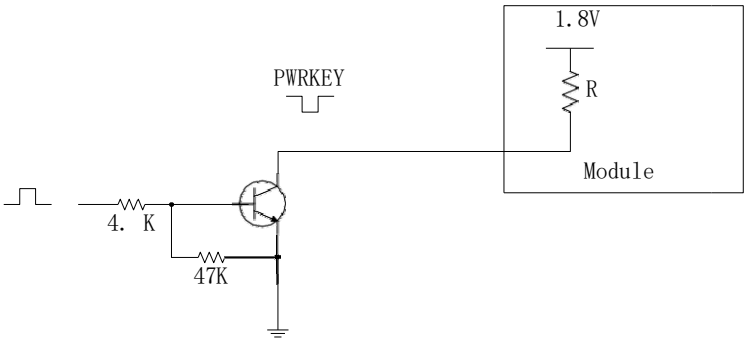


Fig4.4: Power on using external signal driver module

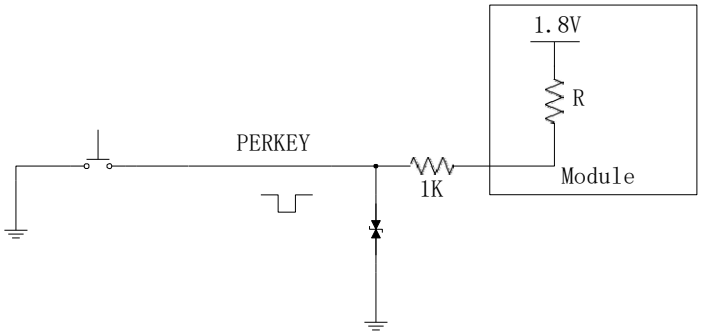


Fig4.5: Use the button circuit to boot

4.2.2. Module Shutdown

The user can shut down the machine using the PWRKEY pin.

4.2.2.1 PWRKEY Shutdown

The user can power off the device by lowering the PWRKEY signal for at least 3 seconds. Power off circuit can refer to the design of power on circuit. After the module detects the shutdown action, a prompt window will pop up on the screen to confirm whether to execute the shutdown action.

You can reset the hardware by pulling PWRKEY low for at least 15 seconds.

4.2.3. Module Reset

The SRM700U module supports the reset function. Users can quickly restart the module by pulling down thePM_RESIN_N(369) pin of the module.

Recommended circuits are as follows:

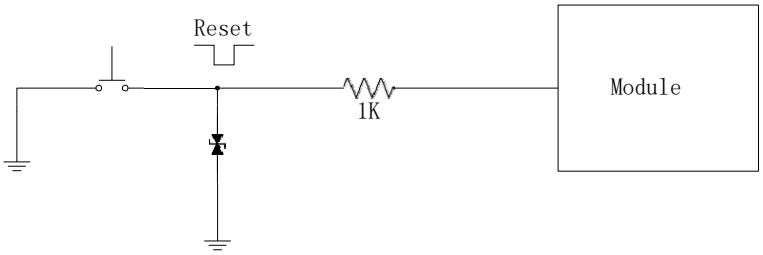


Fig4.6: Use the button circuit to reset

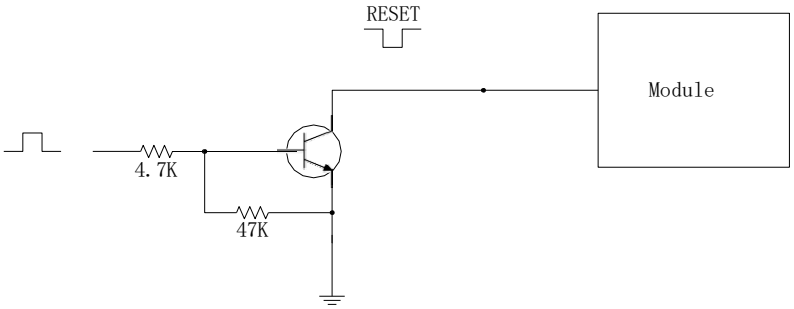


Fig4.7: Reset module using external signal

The typical voltage of the pin is 1.8V at high current level, so the user with 3V or 3.3V level can not directly use GPIO of MCU to drive the pin, and an isolation circuit is required.The hardware parameters of RESET can refer to the following table:

Table 4.1: RESET Hardware Parameters

PIN name	Function	Min	Typical	Max	Unit
RESET	Input high level	1.17	-	-	V
	Input low level	-	-	0.63	V
	Pull down the effective time	9		-	S

4.3. VCOIN

When the VBAT is disconnected and the user needs to save the real-time clock, the VCOIN(350) pin should not be suspended and should be connected to a large external capacitor or battery. When the external capacitor is connected, the recommended value is 100uF, which can keep the real-time clock for 20 seconds. The RTC power module uses an external capacitor or battery to supply power to the RTC inside the module.

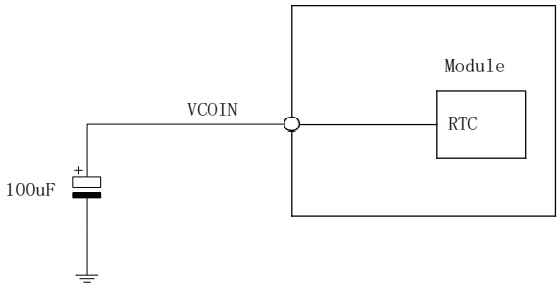


Fig4.8: The external capacitor supplies power to the RTC

Chargeable battery power:

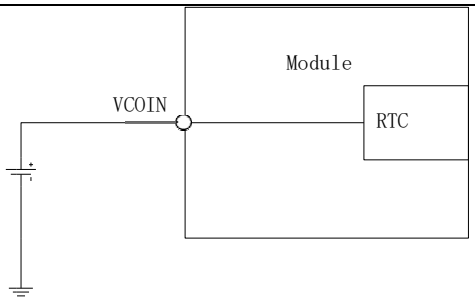


Fig4.9: Chargeable batteries power the RTC

Notes: This VCOIN power supply typical typically 3.0V.

4.4. Power Output

The SRM700U has multiple power outputs.Used for SD card, SIM card, sensor, touch panel, external LDO and so on. In application, it is suggested that adding 33PF and 10PF capacitors in parallel in each power supply can effectively remove high-frequency interference. Sleep = on/OFF, where on means that it cannot be turned off and off means that it can be turned off.

Table 4.2:The power to describe

signal	Defaultvoltage	Drive current
VREG_L21B_1P8（ON）	1.8	300mA（Press the power key to output）
VREG_L2E_1P2 (OFF)	1.2	600mA
VREG_L4E_2P8(SENSOR_VDD)(OFF)	2.8	200mA
VREG_L24B_2P96(SD_VDD)（OFF）	2.96	400mA
VREG_L28B_2P96(SDVIO) （OFF）	2.96	100mA
VDD_1P8_SYS(SYS_V1.8V) （ON）	1.8	300mA（VBAT is always on when it is powered on）
VREG_L6E_3P0(TPVDD) （OFF）	3.0	100mA
VREG_L3E_2P8(WCN_VDD2.8V) （OFF）	2.8	300mA
VREG_L25B_3P072(USBHS_VIO) （OFF）	3.0	100mA
VREG_L7E_3P304(VLEDA) （OFF）	3.3	200mA
VREG_S9B_1P8 WCN_VDD1.8V（ON）	1.8	300mA

4.5. Serial Port

SRM700U provides three serial ports for communication, one of which supports four-wire serial ports,the other two support two-wire serial ports. You can also expand the number of serial ports through the QUP interface.

Table4.3:UART Pin description

Name	Pin	Direction	Function
GPIO8_UART_CTS_N	374	DI	UART1_CTS
GPIO_9_UART_RFR_N	383	DO	UART1_RTS
GPIO_6_UART_TX_N	360	DO	UART1_TX
GPIO_7_UART_RX_N	361	DI	UART1_RX
DBG_UART_TX/GPIO22	149	DO	Debug UART data transmission
DBG_UART_RX/GPIO23*	150	DI	Debug UART data reception
UART_TX/GPIO134	233	DO	UART2_TX
UART_RX/GPIO135*	234	DI	UART2_RX

You can refer to the following connection mode:

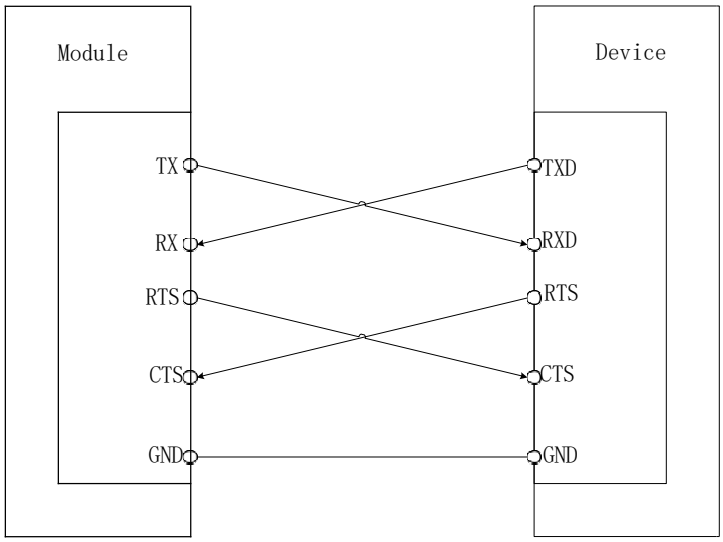


Fig4.10: Serial port connection diagram

When the serial port level used by the user does not match the module, in addition to increasing the level conversion IC, the figure below can also be used to achieve level matching. Here, only TX and RX matching circuits are listed, and other low-speed signals can refer to these two circuits.

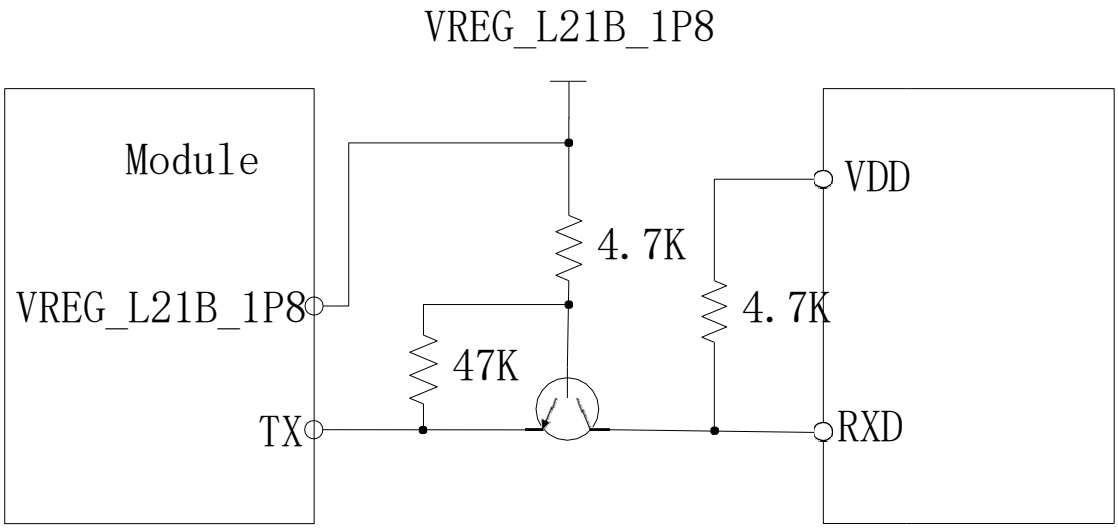


Fig4.11: TX connection diagram

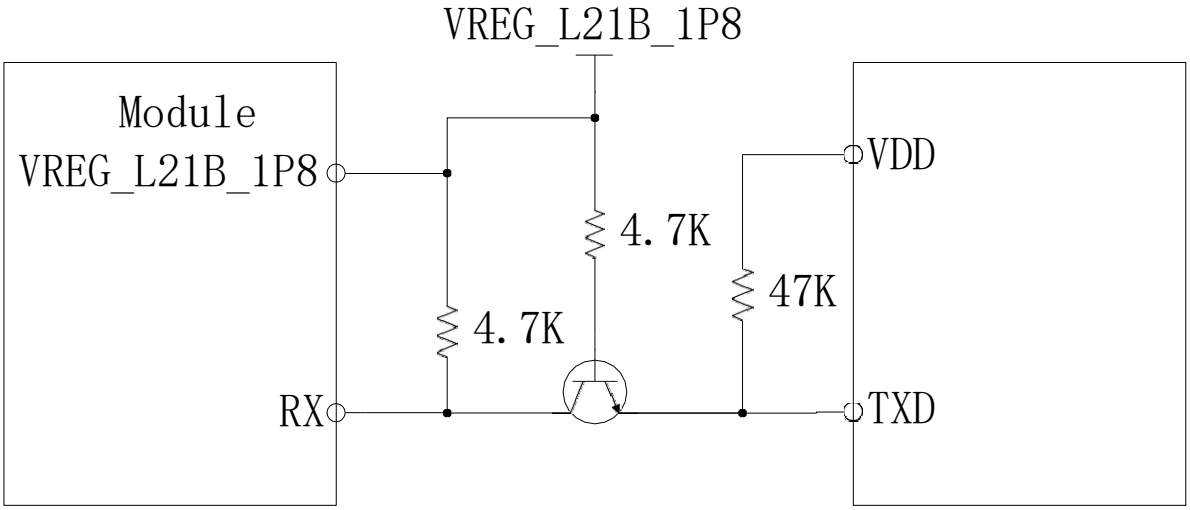


Fig4.12: RX connection diagram

Note: When using Figure 4.11 and4.12 for level isolation,It should be noted that to use VREG_L21B_1P8 as the pull-up power supply, VDD_1P8_SYS is the default normally open power supply of the system, which is not recommended.

Table4.4:Serial Port Hardware Parameters

Description	MIN	MAX	Unit
Input low level	-	0.63	V
Input high level	1.17	-	V
Output low level	-	0.45	V
Output high level	1.35	-	V

Note:

1. The serial port of the module is CMOS interface, which cannot be directly connected to RS232 signal. Use an RS232 converter chip if necessary.

2. If the 1.8V output of the module cannot meet the high level range of the client, please add a level conversion circuit.

4.6. MIPI Interface

SRM700U supports MIPI interface for Camera and LCD. MIPI is a high-speed signal line. In the Layout stage, please route the line strictly according to the requirements of impedance and length, and control the equal length within and between groups of differential pairs, with the total length as short as possible.

4.6.1. LCD Interface

SRM700U supports the MIPI interface of a group of LCD screens with the identification signal of compatible screens. The resolution of the screen can support up to FHD+. The signal interface is shown in the following table. When laying out, please strictly control the differential impedance of 85 15 ohms

and the equal length within and between signal lines. The MIPI interface of the module is a 1.2V power domain. When users need compatible screen design, they can use the LCD_ID pin of the module, and the LCD VCC can use VREG_L3C_3P0 or external LDO for power supply. The specific scheme can be selectedaccording to the current.

Table4.5:PIN Interface

Screen Interface		
MIPI_DSI0_CLK_M	77	MIPI_LCDclock line
MIPI_DSI0_CLK_P	76	
MIPI_DSI0_LANE0_N	254	MIPI_LCDdata line
MIPI_DSI0_LANE0_P	253	
MIPI_DSI0_LANE1_N	252	
MIPI_DSI0_LANE1_P	251	
MIPI_DSI0_LANE3_N	167	
MIPI_DSI0_LANE3_P	166	
MIPI_DSI0_LANE2_N	79	
MIPI_DSI0_LANE2_P	78	
LCD_RST_N/GPIO92*	231	LCD reset pin
LCD_TE/GPIO93*	151	LCDframe sync signal
LCD_ID/GPIO40*	148	LCD_IDsignal

The GPIO of the module can be used as the LCD_ID. If the GPIO is used as the LCD_ID, please confirm the internal circuit of the LCD. If the resistor divider mode is used in the LCD, please note that the high and low levelvoltage must meet the voltage range of GPIO.

MIPI is a high-speed signal cable. To avoid EMI interference, you are advised to place a common-mode inductor near the LCD.

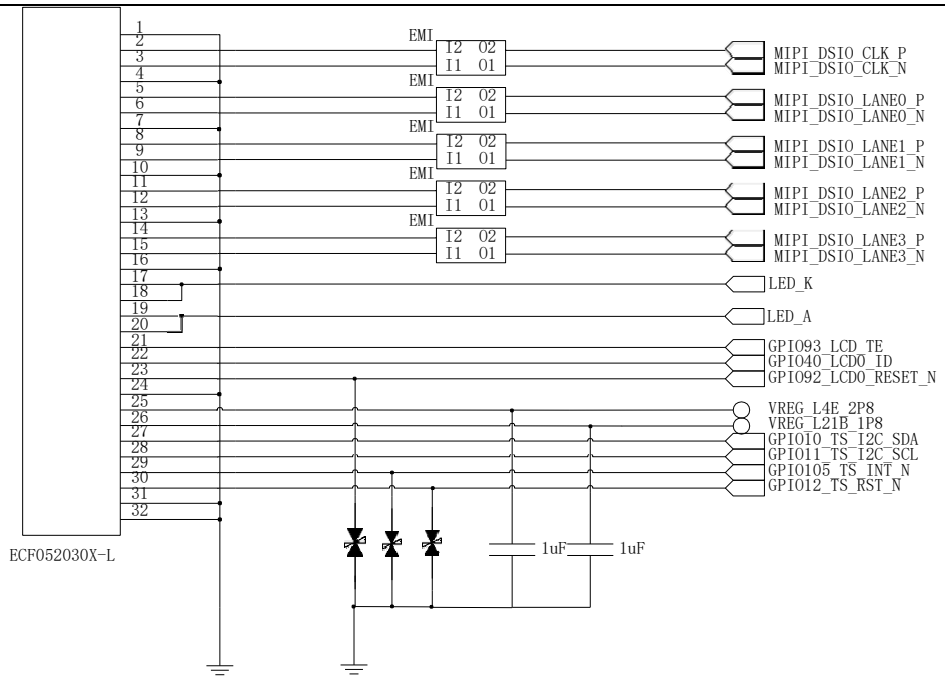


Fig4.13: LCD Interface

SRM700U module comes with four series backlight drive outputs, and customers can directly use this function to drive LCM backlight. The backlight drive features of the SRM700U are as follows: SRM700U can control the external backlight chip to adjust the backlight brightness through the PMU4450_GPIO07_PWM (PIN288) signal of the module, and the modulation mode is PWM

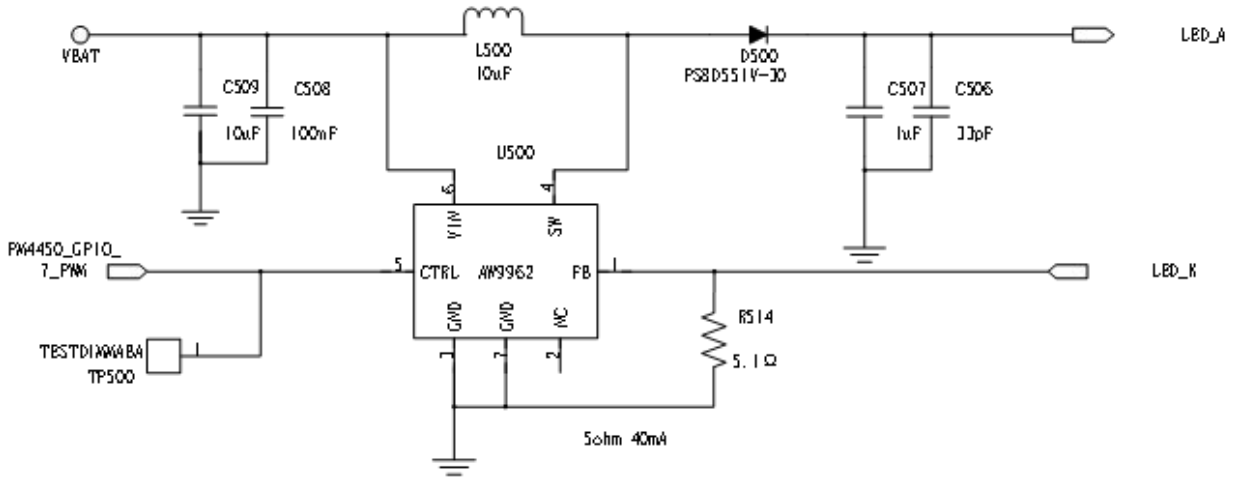


Fig4.14: LCD backlight drive circuit

Note:

1. Backlight circuit should choose the chip according to the backlight circuit of LCD, and users should read the LCD document carefully and choose the correct driver chip. The reference circuit provided in this document is a series PWM dimming backlight driving circuit; If it is a series one-line dimming backlight driving circuit, it needs to be controlled by GPIO.

4.6.2. MIPI Camera Interface

SRM700U module supports three groups of MIPI interface Camera, each group supports four data lines, and can support up to 64M pixels. CSI0~3 interface, which supports four groups of data lines and can support 8M pixels. Can be the main camera, auxiliary camera, and other designs; It can also be used as the design of MIPI interface scanning head. The module does not provide the power needed by the Camera, including AVDD-2.8V, AFVDD-2.8V (focusing motor power supply) all need external LDO generation, and DVDD-1.2V(CAM core voltage) is generated by external DC/DC.

Table4.6:MIPI Camera Interface

Rear camera interface		
MIPI_CSI0_CLK_P	3	CSI0MIPICLOCK
MIPI_CSI0_CLK_N	4	
MIPI_CSI0_LANE1_P	1	CSI0 MIPIDATA
MIPI_CSI0_LANE1_N	2	
MIPI_CSI0_LANE2_P	93	
MIPI_CSI0_LANE2_N	94	
MIPI_CSI0_LANE0_P	95	
MIPI_CSI0_LANE0_N	96	
MIPI_CSI0_LANE3_P	181	
MIPI_CSI0_LANE3_N	182	
_I2C0_SCL/GPIO45	207	CSI0 I2C_SCL
_I2C0_SDA/GPIO44	208	CSI0 I2C_SDA
MCAM_PWD_N/GPIO100	300	CSI0Sleepsignal
MCAM_DVDD_EN/UART1_RX/ NFC_REQ/GPIO7*	360	CSI0 DVDD LDOEnable signal
GPIO62*_CAM_AVDD_EN	235	CSI0 AVDD LDOEnable signal
CAM_MCLK0/GPIO36	372	CSI0Main clock
CAM0_RST_N/GPIO127	385	CSI0Resetsignal
Secondary camera interface		
MIPI_CSI1_CLK_P	266	CSI1 MIPICLOCK
MIPI_CSI1_CLK_M	267	
MIPI_CSI1_LANE1_P	268	CSI1 MIPI DATA
MIPI_CSI1_LANE1_N	269	
MIPI_CSI1_LANE2_P	185	
MIPI_CSI1_LANE2_N	186	
MIPI_CSI1_LANE0_P	183	
MIPI_CSI1_LANE0_N	184	
MIPI_CSI1_LANE3_P	98	
MIPI_CSI1_LANE3_N	99	

_I2C1_SCL/GPIO47*	126	CSI1 I2C_SCL
_I2C1_SDA/GPIO46	125	CSI1 I2C_SDA
DCAM_PWD_N/GPIO84*	291	CSI1Sleepsignal
DCAM_DVDD_EN/UART1_TX/ GPIO6*	361	CSI1 DVDD LDOEnable signal
GPIO62*_CAM_AVDD_EN	235	CSI1 AVDD LDOEnable signal
CAM_MCLK0/GPIO36	373	CSI1Main clock
CAM1_RST_N/GPIO102*	384	CSI1Resetsignal
Front camera interface		
MIPI_CSI2_CLK_P	83	CSI2 MIPICLOCK
MIPI_CSI2_CLK_N	84	
MIPI_CSI2_LANE1_P	169	CSI2 MIPI DATA
MIPI_CSI2_LANE1_N	170	
MIPI_CSI2_LANE2_P	171	
MIPI_CSI2_LANE2_N	172	
MIPI_CSI2_LANE0_P	81	
MIPI_CSI2_LANE0_N	82	
MIPI_CSI2_LANE3_P	256	
MIPI_CSI2_LANE3_N	257	
_I2C2_SCL/GPIO49	224	CSI2 I2CCLOCKsignal
_I2C2_SDA/GPIO48	223	CSI2I2CDATA signal
FCAM2_PWD/GPIO4*	377	CSI2Sleepsignal
NFC_CLK_REQ/GPIO98*	283	CSI2 DVDD LDOEnable signal
GPIO62*_CAM_AVDD_EN	235	CSI2 AVDD LDOEnable signal
CAM_MCLK2/GPIO38	387	CSI2Main clock signal
CAM2_RST_N/GPIO42*	35	CSI2Resetsignal

If the user designs a CAMERA module with auto-focus function, please note that the I2C of the module cannot be directly connected to the AF device, and the I2C of the AF device should be connected to the driver chip of the CAMERA.

The rate of the MIPI interface is high. During cabling, use 85±15 ohm impedance to control the cable, and pay attention to the cable length. Do not add a small capacitor to the MIPI signal cable, because the rising edge time of MIPI data may be affected and MIPI data may be invalid.

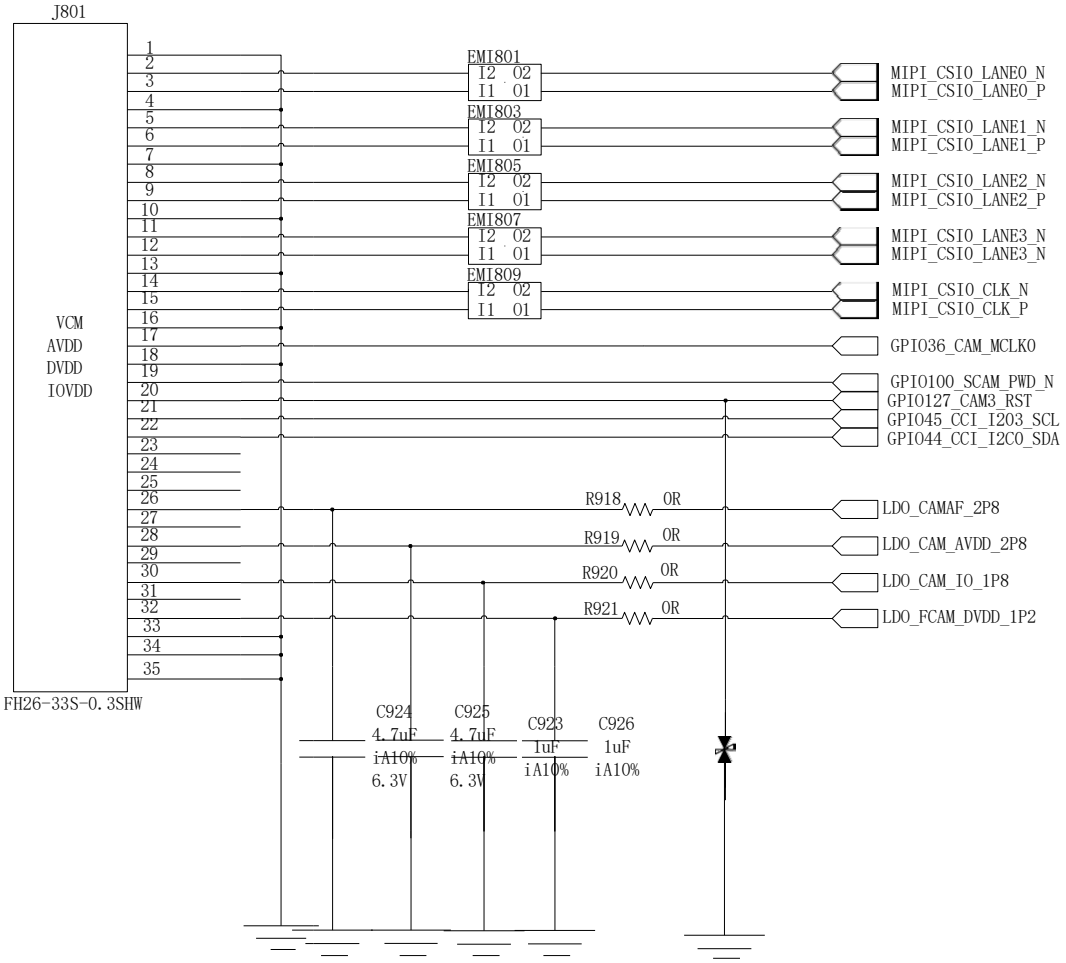


Fig4.15: MIPI Camera1 reference circuit

4.6.3. MIPI PCB Layout

MIPI is a high-speed signal line, so users must pay attention to protect it away from the signal line that is easily disturbed in the layout stage. GND processing must be done in the way of upper, lower, left and right packages, and the wiring is in a differential pair, and 85 ohm differential impedance matching should be done. In order to ensure the consistency of impedance, try not to cross different GND planes as much as possible. Please select TVS with small capacitance when selecting ESD devices for MIPI interface, and it is recommended that the parasitic capacitance be less than 1pF.

MIPI wiring requirements are as follows:

The total length of wiring shall not exceed 110mm;

It is required to control the differential impedance of 85 ohms with an error of 15 ohms;

The length error of intra-group differential line is controlled within 0.7mm;

The length error between groups is controlled within 1.4mm;

4.7. Capacitive Touch Interface

The module provides a set of I2C interfaces that can be used to connect capacitive touch. The default interface pins of capacitive touch are defined as follows:

Table4.7:Capacitive touch interface definition

Name	Pin	IN/OUT	Description
TS_I2C_SDA/GPIO10*	142	OD	I2Csignal
TS_I2C_SCL/GPIO11*	143	OD	I2Csignal
TS_INT_N/GPIO105*	140	OD	TPinterruptsignal
TS_RST_N/GPIO12*	141	OD	TPResetsignal
VREG_L21B_1P8	352	PO	VIO_1.8VPower Supply
VREG_L4E_2P8(TP2.8V)	344	PO	VDD_2.8VPower Supply

Note: The interface definition for capacitive touch can be adjusted by software, and users can change GPIO and I2C according to design needs.

4.8. Audio Interface

The module provides three analog audio inputs, MIC1_P/N is used to connectthe main mic; HPHMIC_IN2_P/Ncan be used to connect the headset mic, and MIC3_P/N can be used to connect the noise-canceling mic. The module also provides three channels of analog audio output (HSJ_HPH_L/R, WCD_EAR_OUT_P/N, AUDIO_PA_EN/GPIO55*). The definition of audio PIN is as follows:

Table4.8:Audio pindefinition

MIC1_IN_M	17	AI	Main MIC negative electrode(-)	
MIC1_IN_P	18	AI	Main MIC positive electrode(+)	
HPHMIC_IN2_P	15	AI	Headphone MIC positive electrode(+)	
HPHMIC_IN2_M	16	AI	Headphone MIC negative electrode(-)	
MIC3_IN_M	110	AI	Noise reduction MIC negative electrode(-)	
MIC3_IN_P	111	AI	Noise reduction MIC positive electrode(+)	
MIC_BIAS1	203	AO	BIAS voltage of main mic and auxiliary mic, used for silicon wheat design.	
MIC_BIAS2	204	AO	BIAS voltage of earphone MIC	
MIC_BIAS3	205	AO	BIAS voltage of mic4, used for silicon wheat design.	
HSJ_HPH_R	198	AO	Headphone right channel	
HSJ_HPH_L	197	AO	Headphone left channel	
HSJ_HS_DET	199	DI	Earphone unplugging detection	
HSJ_HPH_REF	200	AI	Headphone reference ground	
WCD_EAR_OUT_P	117	AO	Handset output positive pole	

WCD_EAR_OUT_M	118	AO	Receiver output negative electrode	
WCD_AUX_P	27	AO	External power amplifier input positive pole	External power amplifier input
WCD_AUX_M	28	AO	External power amplifier input negative pole	
I2S1_DATA1/DMIC2_DATA/GPIO122 *	364	I/O	Digital MIC2 data signal	PDM
I2S1_DATA0/DMIC2_CLK/GPIO121*	365	I/O	Digital MIC2 clock signal	
I2S1_CLK/DMIC1_CLK/GPIO115*	294	I/O	Digital MIC1 clock signal	PDM
I2S1_WS/DMIC1_DATA/GPIO116	295	I/O	Digital MIC1 data signal	
I2S2_DATA0/DMIC3_CLK/GPIO117	296	I/O	Digital MIC3 clock signal	PDM
I2S2_DATA1/DMIC3_DATA/GPIO118* *	297	I/O	Digital MIC3 data signal	

It is recommended that users choose the following circuit according to the actual application situation to get better sound effect.

4.8.1. Receiver Interface Circuit

The following devices are placed near the REC end in the REC interface circuit. R602 and R603 can be changed into magnetic beads according to the actual effect.

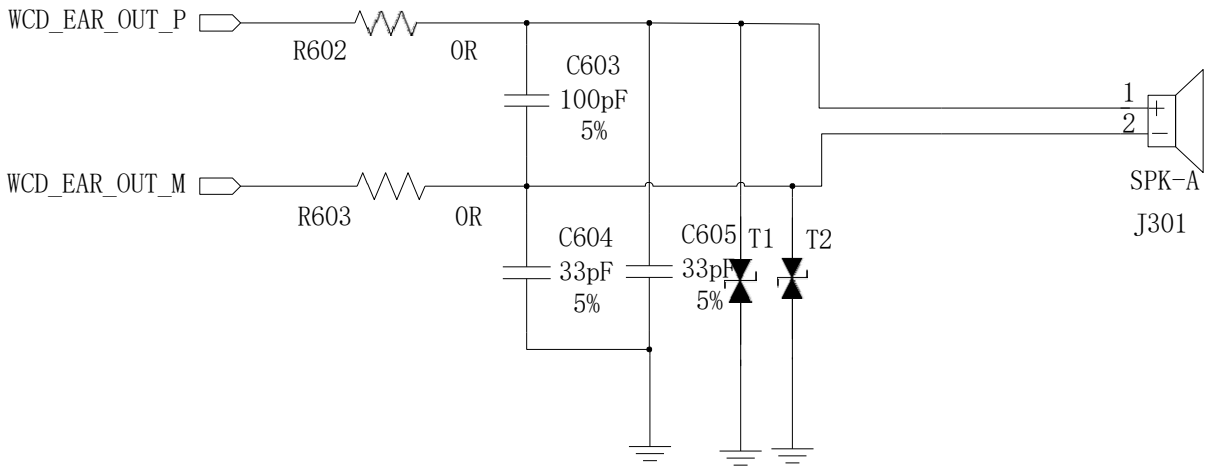


Fig4.16: REC interface circuit

4.8.2. Microphone Receiving Circuit

The following figure shows the interface circuit of electret microphone and MEMS microphone. Please follow the reference circuit design in strict accordance with the following figure according to the different types of users' microphones.

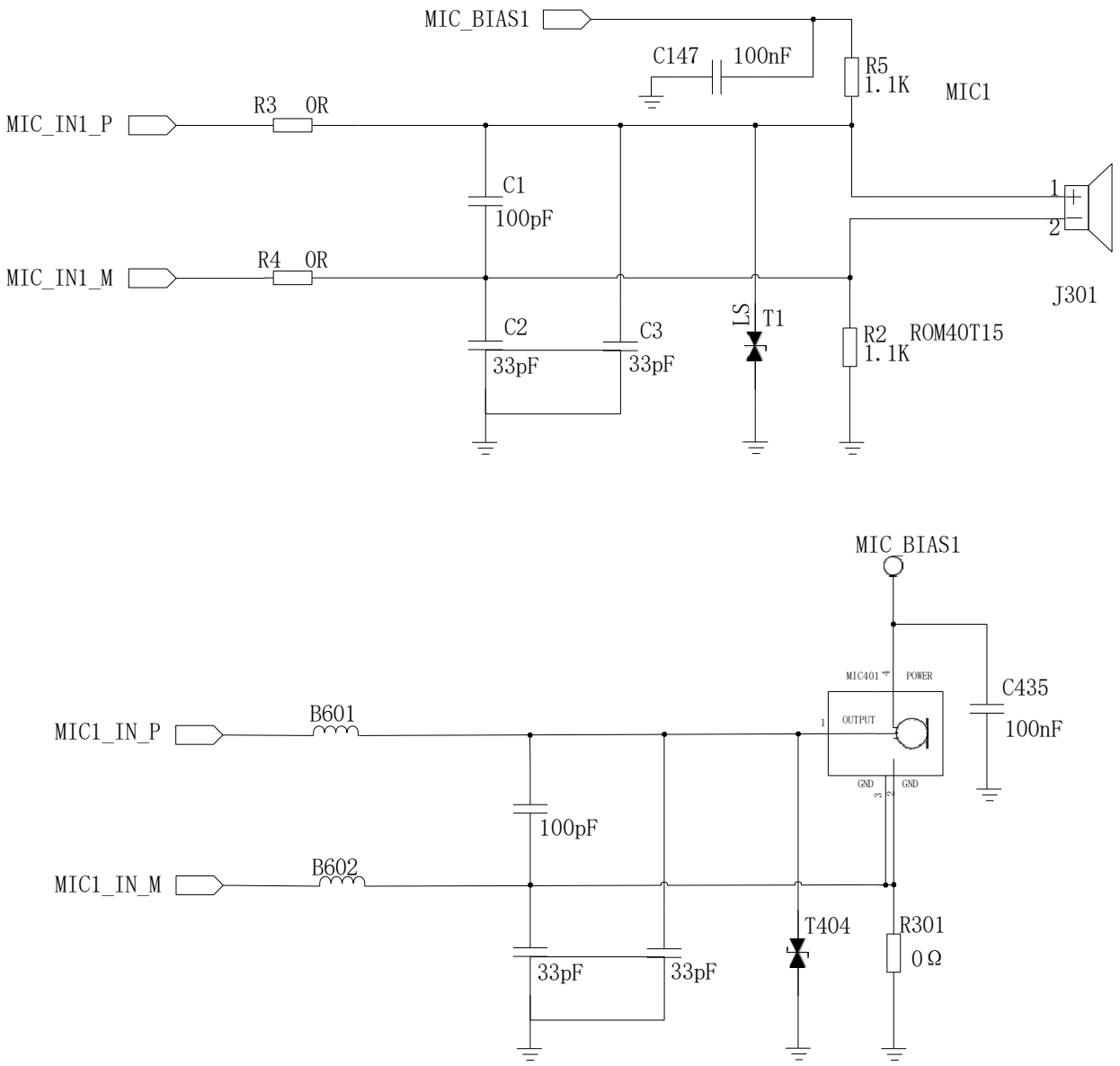


Fig4.17: Electret microphone, analog silicon-wheat interface circuit

4.8.3. Headphone Interface Circuit

The module integrates a stereo headphone jack. You are advised to reserve ESD devices during the design phase to prevent ESD damage. The HSJ_HS_DET pin of the module can be set as interrupt. By default, this pin is headset interrupt in the software. Users can use this pin to detect the plug and unplug of the headset.

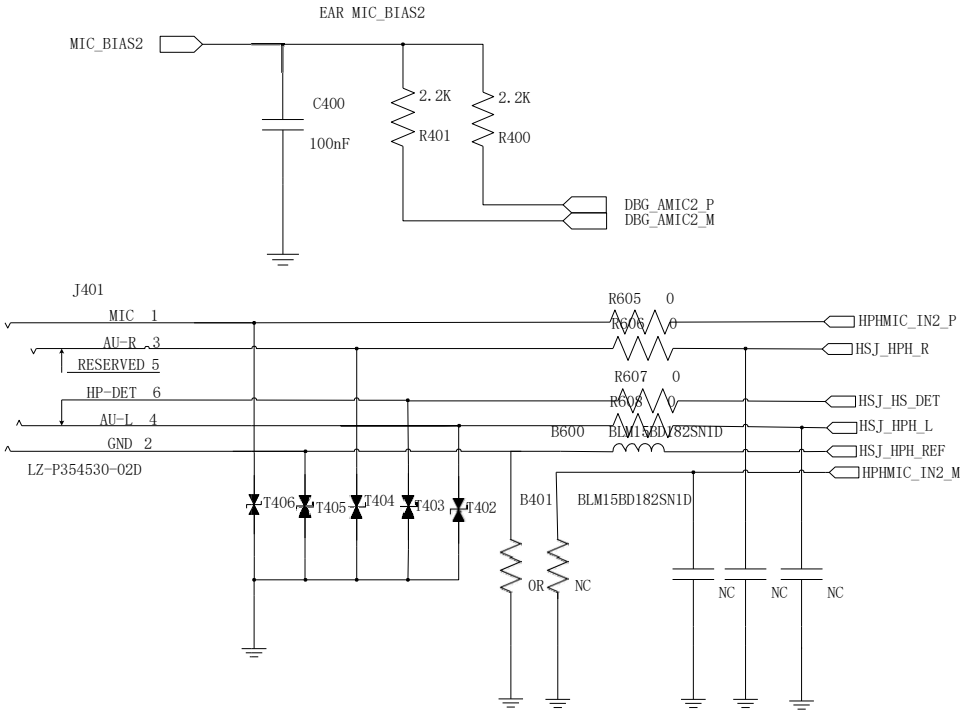


Fig4.18: Headphone interface circuit

Note:

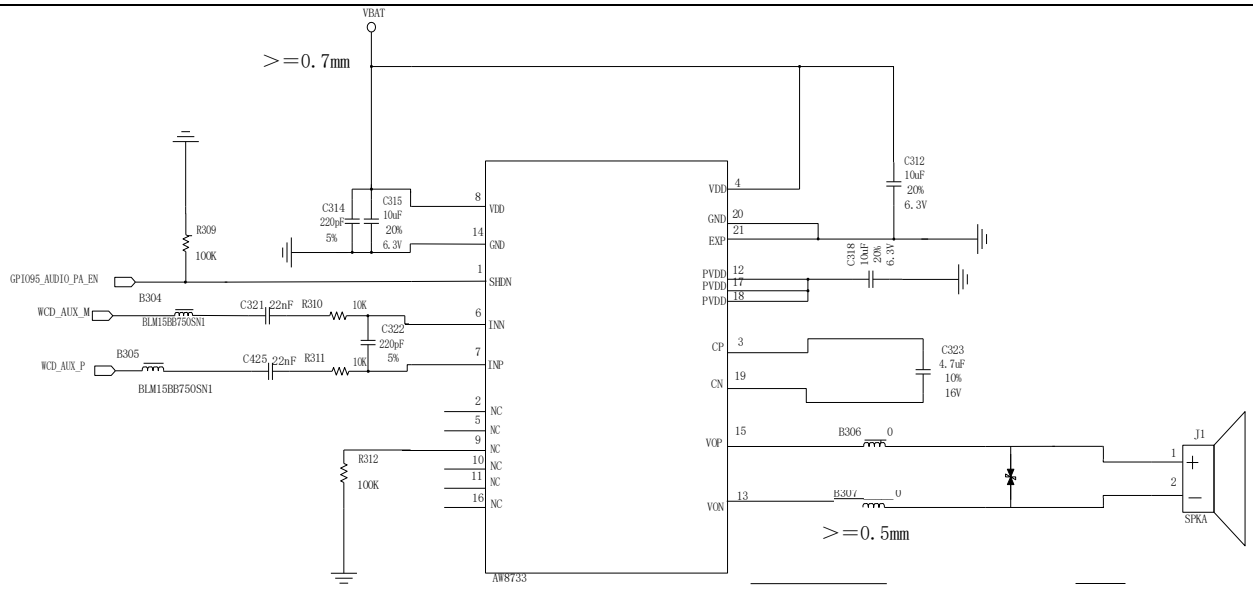
1. The headphone jack in Figure 4.18 is normally closed. If the user uses a normally open headphone jack, please modify the detection circuit according to the actual pin and modify the software accordingly.

2. We recommend that the earphone detection pins HSJ_HS_DET and HSJ_HPH_L form a detection circuit (the connection mode in the above figure), because there is a pull-down resistor in the chip, which can ensure that HSJ_HS_DET and HSJ_HPH_L are at a low level when connected. If the user connects HSJ_HS_DET with HSJ_HPH_R, please reserve the position of 1K pull-down resistor on HSJ _ HPH _ R.

3. The standard of the illustrated earphone interface is American CTIA. If you need to design European OMPT interface, you need to exchange GND and MIC signals in the network.If we want to be compatible with two earphone standards, we need an external dedicated chip, such as TI-TS3A226AE.

4.8.4. Speaker Interface Circuit

There is no built-in audio power amplifier in the module, so an audio power amplifier needs to be added externally. WCD_AUX_P and WCD_AUX_M are used as differential input signals. The reference circuit is shown in the following



4.19: Recommended circuit with external audio amplifier

4.8.5. I2S Interface

There are two sets of GPIO compatible I2S interfaces inside the module. The pins used for this function are listed below:

Name	Pin	IN/OUT	Description
I2S1_CLK/DMIC1_CLK/GPIO115	294	I/O	LPI_I2S1_CLK
I2S1_WS/DMIC1_DATA/GPIO116	295	I/O	LPI_I2S1_WS
I2S1_DATA0/GPIO117	295	I/O	LPI_I2S1_DATA0
I2S1_DATA1/GPIO118	297	I/O	LPI_I2S1_DATA1
I2S2_DATA0/DMIC2_CLK/GPIO121	365	I/O	LPI_I2S2_DATA0
I2S2_DATA1/DMIC2_DATA/GPIO122	364	I/O	LPI_I2S2_DATA1
I2S2_CLK/SWR_CLK/GPIO119	363	I/O	LPI_I2S2_ SLK
I2S2_WS/SWR_DATA/GPIO120	362	I/O	LPI_I2S2_WS

4.8.6. AUDIO PCB Layout

Analog signals are easily interfered by high-speed digital signals. So please stay away from high-speed digital signal lines. The module supports GSM system, and GSM signals can interfere with audio through coupling and conduction. Users can add 33pF and 10pF capacitors on the audio path to filter out coupling interference. The 33pF capacitor mainly filters out the interference in GSM850/EGSM900 band, and the 10pF capacitor mainly filters out the interference in DCS1800 band. The coupling interference of TDD is closely related to the user's PCB design. In some cases, the TDD in GSM850/EGSM900 band is more serious, while in some cases, the TDD interference in DCS1800 band is more serious. Therefore, the user can choose the required filter capacitor according to the actual test results, and sometimes it is even unnecessary to attach the filter capacitor.

GSM antenna is the main interference source of TDD coupling, so users should pay attention to keeping audio routing away from GSM antenna and VBAT when PCB layout and routing. It is best to place one

set of audio filter capacitors near the module end and another set near the interface end. Audio output should be routed according to the differential signal rule.

Conducted interference is mainly caused by the voltage drop of VBAT. If AudioPA is directly powered by VBAT, it is easier to hear the "squeak" sound at the output end of SPK, so it is better to connect some large capacitance capacitors and series magnetic beads in parallel at the input end of AudioPA in schematic design. TDD is also closely related to GND. If GND is not handled properly, many high-frequency interference signals will interfere with MIC and Speaker through bypass capacitors and other devices, so users should ensure the good performance of GND in PCB design stage.

4.9. USB Interface

4.9.1. USB Interface

SRM700U supports 1 USB 2.0 interface (for HOST use only) and 1 USB 3.1 interface. When laying out, it is necessary to control the differential impedance of 90 ohms and the external trace length. It is important to note that SRM700U module only supports Micro-USB interface by default. If Type-C interface is needed, USB_CC signal needs to be generated by CC logic chip.

Table4.10:USB interface switching pin definition

USB0_HS_D_P	163	AI/AO	USB 2.0 DPsignal	
USB0_HS_D_M	164	AI/AO	USB 2.0 DMsignal	
USB0_SS_TX1_P	72	AO	USB3.1 channel 1 differential transmit positive electrode	
USB0_SS_TX1_M	161	AO	USB3.1 channel 1 differential transmission negative electrode	
USB0_SS_RX1_P	73	AI	USB3.1 channel 1 differential receiving positive electrode	
USB0_SS_RX1_M	74	AI	USB3.1 channel 1 differential receiving negative electrode	
USB0_SS_TX0_P	245	AO	USB3.1 channel 0 differential transmit positive electrode	
USB0_SS_TX0_M	246	AO	USB3.1 channel 0 differential transmission negative electrode	
USB0_SS_RX0_P	243	AI	USB3.1 channel 0 differential receiving positive electrode	
USB0_SS_RX0_M	244	AI	USB3.1 channel 0 differential receiving negative electrode	
USB_ID/GPIO41*	33	DI	USB ID signal	
USB_PHY_PS/GPIO94*	355	DI	USB_PHY_PS	Need to connect 1K resistor to the ground.

The module also supports OTG function. However, OTG power supply needs to be generated by an additional boost circuit.

The USB insertion detection of the module is realized by VBUS and DP/DM data cable. When the USB cable is inserted, the VBUS voltage is detected first, and then the USB cable or charger is determined by detecting the pull up and down state of DM/DP. Therefore, if the user needs to use USB function, please be sure to connect VBUS to the 5V power supply on the data line.

USB is in high-speed mode. You are advised to connect a serial common-mode inductor close to the USB connector to effectively suppress EMI interference. At the same time, The USB interface is an external interface. It must to add TVS to prevent electrostatic damage caused by plugging and unplugging data cables. Users should pay attention to the load capacitance of TVS should be less than 1PF when selecting TVS. TVS tubes should also be added to VBUS, and surge protection tubes should be added if there is surge protection demand.The connection diagram is as follows:

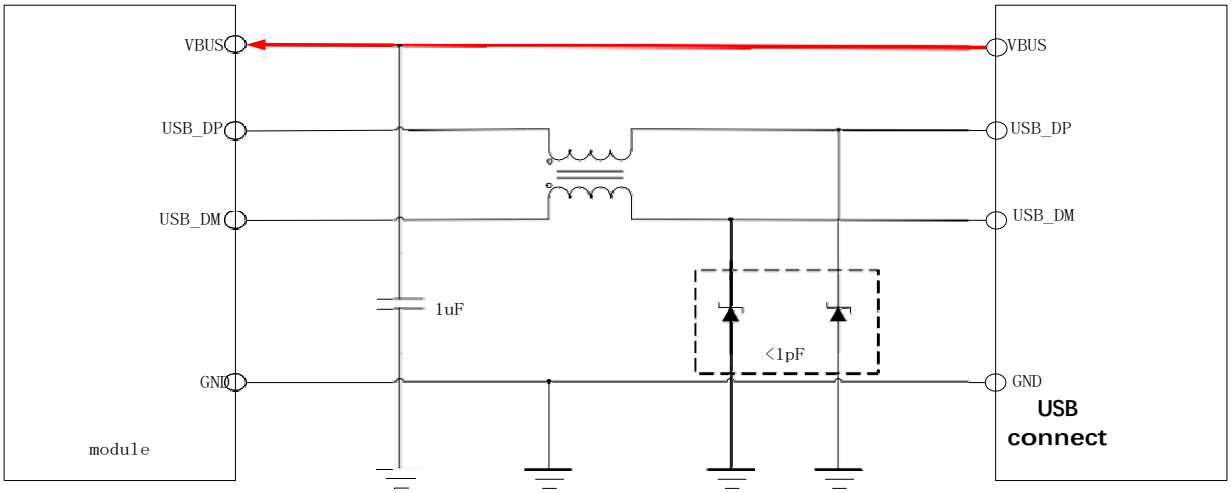


Fig4.20: USB Connection diagram

4.9.2. USB PCB Layout

The module supports high-speed USB interface. Users suggest adding a common mode choke in the schematic design stage, which can effectively suppress EMI interference. If users need to increase electrostatic protection, please be sure to choose TVS tubes with parasitic capacitance less than 1pF.

Please refer to the following precautions when laying out:

Common mode choke, please be near the USB connector side;

It is required to control the differential impedance of 90 ohms with an error of 10%;

The error of differential line length is controlled within 6mm;

If USB has charging function, please pay attention to the width of VBUS wiring as wide as possible;

If there are test points, try to avoid wiring bifurcation and put the test points on the path of wiring.

Table4.11 USB Type-C receptacle pins

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	
GND	TX1+	TX1-	VBUS	CC1	D+	D-		SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+		CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6		B5	B4	B3	B2	B1

4.10. UIM Interface

4.10.1. UIM card Interface circuit

The SRM700U supports two SIM card interfaces to achieve dual-card dual-standby. It supports hot swap of SIM cards and automatically identifies 1.8V and 3.0V cards. Below is the recommended SIM interface circuit. To protect SIM cards, TVS devices are recommended for static protection. The peripheral circuit of the SIM card should be close to the SIM card holder.

The reference circuit is as follows:

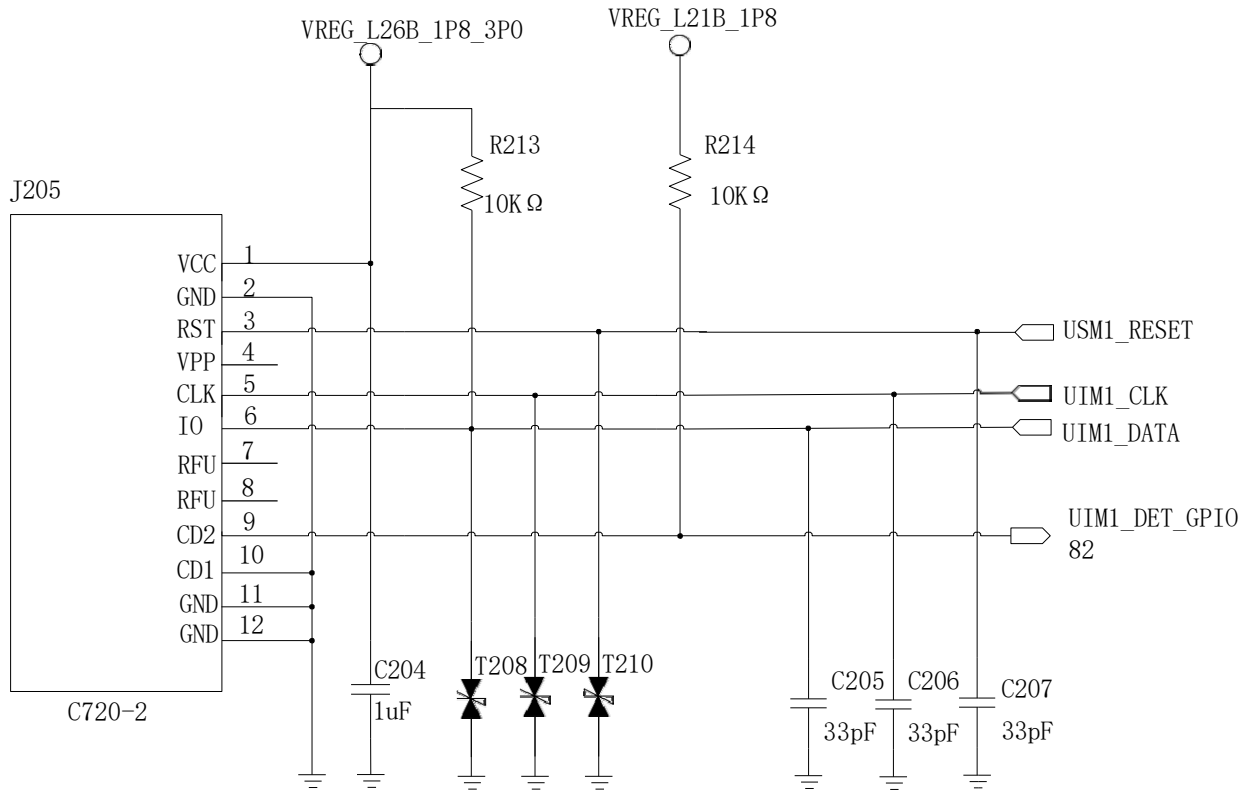


Fig4.22: UIM card interface circuit

4.10.2. UIM PCB Layout

The SIM card has a large area, and it has no anti-EMI devices, so it is easy to be disturbed. Therefore, in layout, first ensure that the SIM card is far away from the antenna and the antenna extension line inside the product, and place it as close as possible to the module. When wiring the PCB, pay attention to protecting the SIM_CLK signal. The SIM_DATA, SIM_RST and SIM_VDD signals of the SIM card should be far away from the power supply and high-speed signal lines. If it is not handled properly, it will easily lead to card ignorance or card drop, so please follow the following principles when designing:

In the PCB layout stage, the SIM card holder must be kept away from the GSM antenna;

SIM card wiring should be as far away from RF lines, VBAT and high-speed signal lines as possible, and the SIM card wiring should not be too long;

The GND of the SIM card holder should maintain good connectivity with the GND of the module to make them equipotential;

In order to prevent SIM_CLK from interfering with other signals, it is suggested that SIM_CLK be protected;

It is suggested to place a 100nF capacitor near the SIM card holder on the SIM_VDD signal line;

Place TVS near the SIM card holder, the parasitic capacitance of the TVS should not be greater than 50pF, and the 51Ω resistor connected in series with the module can enhance ESD protection;

Add 22pf capacitance to the ground on the signal line of SIM card to prevent RF interference;

There is a large current flowing through the return path of VBAT, so the SIM card should try to avoid the return path of VBAT.

4.11. SD Interface

SRM700U supports SD card interface, with a maximum support of 256GB. Please wrap the CLK signal (PIN 310: SDC2 _ CLK) of T card separately, appropriately increase the ground hole for the ground wire of the ground wrapping path, and combine the other data wires to wrap the ground in a three-dimensional way; The total load capacitance of each signal line is less than 5pF (including TVS capacitance and filter capacitance).

The reference circuit is as follows:

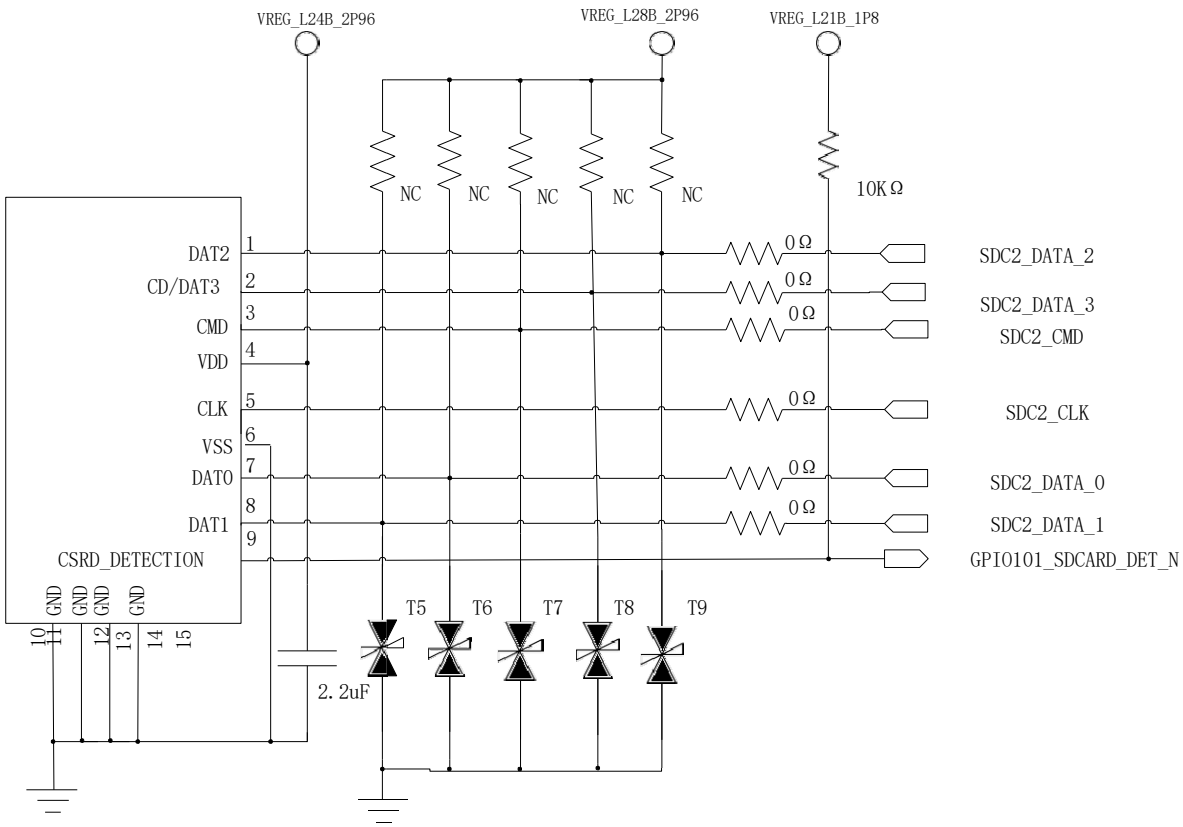


Fig4.23: SD interface circuit

4.12. I2C Bus Interface

The SRM700U module supports 8 hardware I2C bus interfaces, 3 camera interfaces, 1 sensor interface, 1 TP interface, 1 PMIC interface and 2 general interfaces.Pin definitions and default functions are as follows:

Table4.12:I2C interface

SENSOR_I2C_SDA/GPIO130*	42	OD	SENSOR_I2Csignal	Pull up toVREG_L21B_1P8
SENSOR_I2C_SCL/GPIO131	43	OD		
NFC_I2C_SDA/GPIO91*	120	OD	UniversalI2Csignal	Pull up toVREG_L21B_1P8
NFC_I2C_SCL/GPIO90	121	OD		
PMIC_I2C_SCL	59	OD	PMIC I2Csignal	Pull up toVREG_L21B_1P8
PMIC_I2C_SDA	62	OD		
TS_I2C_SDA/GPIO10*	142	OD	TP_I2Csignal	Pull up toVREG_L21B_1P8
TS_I2C_SCL/GPIO11*	143	OD		
APPS_I2C_SDA/GPIO24*	302	OD	UniversalI2Csignal	Pull up toVREG_L21B_1P8
APPS_I2C_SCL/GPIO25	303	OD		
CCI_I2C0_SCL/GPIO45	207	OD	R-CAM I2Csignal	Pull up toVREG_L21B_1P8
CCI _I2C0_SDA/GPIO44	208	OD		
CCI _I2C2_SCL/GPIO49	224	OD	F-CAM I2Csignal	Pull up toVREG_L21B_1P8
CCI _I2C2_SDA/GPIO48	223	OD		
CCI _I2C1_SCL/GPIO47*	126	OD	D-CAM I2Csignal	Pull up toVREG_L21B_1P8
CCI _I2C1_SDA/GPIO46	125	OD		

Note: When used as I2C bus interface, connect the 2.2KΩ pull-up resistor to 1.8V.

4.13. ADC

The SRM700U module uses a power management chip to provide two ADC functional signals: PM4450_GPIO5_AMUX5（230PIN）and PMK4450_GPIO1_AMUX1（438PIN）.

4.14. PWM

PM4450_GPIO7_BL_PWM（288PIN）can be used to do LCD backlight adjustment, by adjusting the duty ratio to adjust the backlight brightness.

4.15. Antenna Interface

The module provides seven antenna interfaces: ANT_0, ANT_1, ANT_2, ANT_3, WIFI_ANT0, WIFI_ANT1, GNSS_ANT.etc. To ensure good wireless performance of the user's product, the user should select an antenna whose input impedance is 50 ohm and standing wave coefficient is less than 2 in the working frequency band.

4.15.1. WAN ANT(ANT_0/1/2/3)

The module provides **ANT_0/1/2/3** antenna interface. The antenna on the user's MAIN board shall be connected to the antenna pin of the module with a characteristic impedance of 50 ohm micro-strip line or ribbon line.

To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

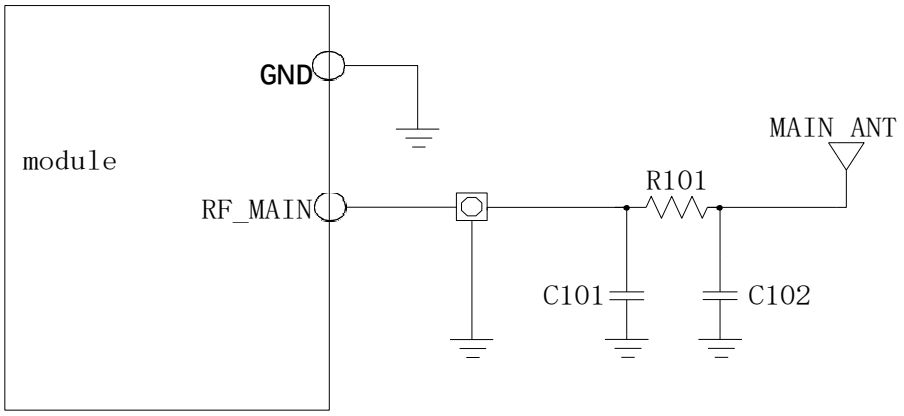


Fig4.24: ANT_0/1/2/3 Antenna interface connects the circuit

In the figure, R101, C101 and C102 are antenna matching devices. The specific component values can be determined after the antenna is debugging in the antenna factory. Among them, R101 defaults is pasted0R, and C101 and C102 default to dispasted.

If there are fewer components that can be placed between the antenna and the output end of the module, or RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the figure below:

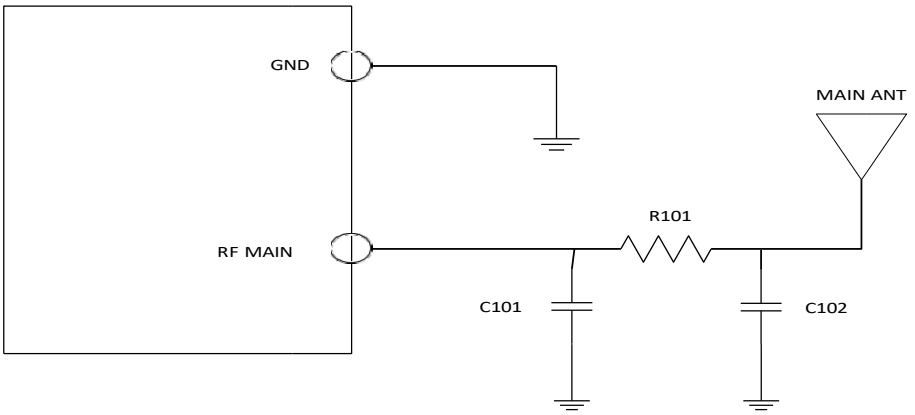


Fig4.25: ANT_0/1/2/3 antenna interface simplifies the connection circuit

Note: In the figure above, R101 is pasted by default, C101 and C102 are not pasted by default.

4.15.2. GPS Antenna

GNSS antenna pin RF_GPS is provided by the module. The antenna on the user's motherboard shall be

connected to the antenna pin of the module using a micro-strip line or ribbon line with a characteristic impedance of 50 ohm.

There is no integrated LNA inside the module.

To improve GNSS reception performance, customers can use external active antennas. The recommended circuit connection is shown in the figure below:

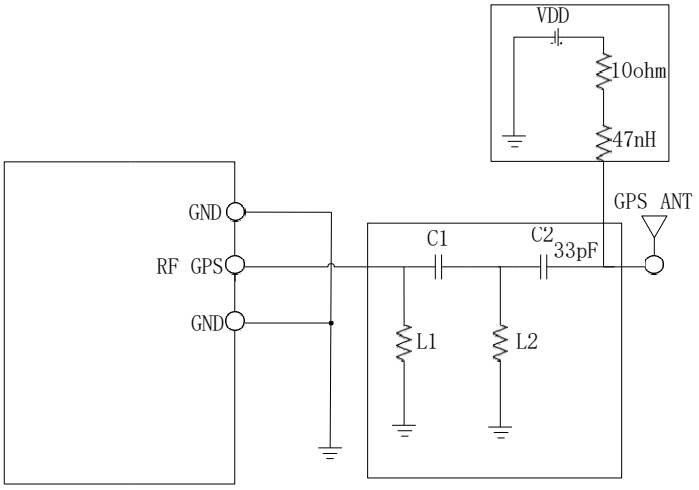


Fig4.26: Connect active antenna

4.15.3. WiFi/BT Antenna

The module providesWifi ANT_0/1 antenna pinT. The antenna on the user's motherboard shall be connected to the antenna pin of the module using a micro-strip line or ribbon line with a characteristic impedance of 50 ohm.

To facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

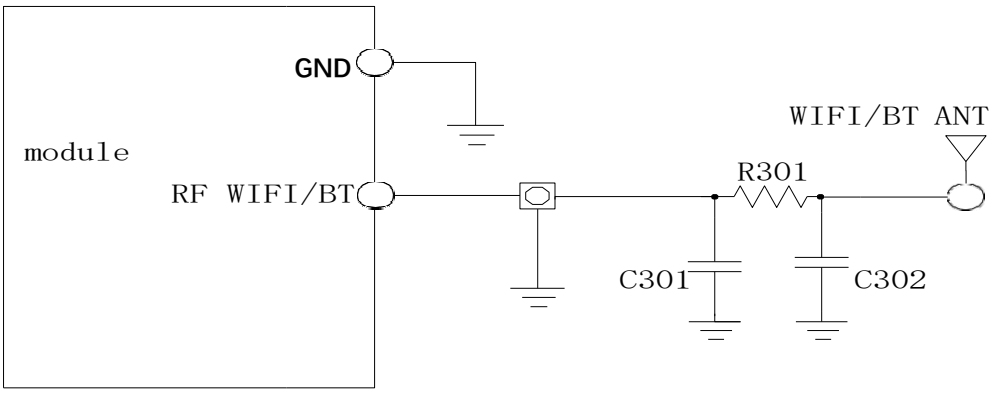


Fig4.27: WiFi_BT antenna interface connection circuit

Note: R301, C301, C302 are antenna matching devices. The specific component values can be determined after the antenna is debugging in the antenna factory. 0R is displayed by default for R301, C301 and C302 are not displayed by default.

If there are fewer components that can be placed between the antenna and the output end of the module, or RF test head is not required in the design, the antenna matching circuit can be simplified as shown in

the figure below:

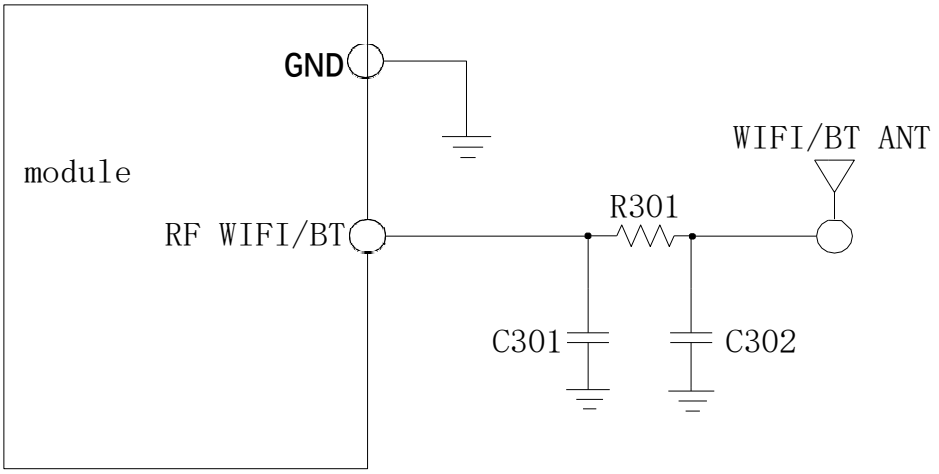


Fig4.28: WIFI_BT antenna interface simplifies connection circuit

Note: R301 is pasted by default, C301 and C302 are not pasted by default.

4.15.4. Antenna PCB Layout

In the antenna design, attention should be paid to the placement of components and RF routing:

The RF test head is used to test the conducted RF performance and should be placed as close as possible to the antenna pin of the module;

The antenna matching circuit needs to be placed near the antenna end;

The wiring from the antenna pin of the module to the antenna matching circuit must be controlled by 50 ohm impedance; Devices and wires between the antenna pin of the module and the antenna connector must be far away from high-speed signal lines and strong interference sources, and avoid crossing or parallel with any signal lines in the adjacent layer;

The length of the RF wire between the antenna pin of the module and the antenna connector should be as short as possible, and the situation of crossing the whole PCB board should be absolutely avoided;

If the antenna is connected by coaxial RF wire, care should be taken to avoid making the coaxial RF wire span the SIM card, power supply circuit and high-speed digital circuit to minimize the mutual influence.

5. Electrical, Reliability

5.1. Absolute Maximum

The table below shows the absolute maximum values that the module can withstand. Exceeding these limits may cause permanent damage to the module.

Table 5.1:Absolute maximum

Parameter	Minimum	Typical	Maximum	Unit
VBAT	--0.5	-	6	V
VBUS	--0.3	-	6	V
Peak current	-	-	4	A

5.2. Working Temperature

The following table shows the operating temperature range of the module:

Table 5.2:Module operating temperature

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-25	-	75	℃
Storage temperature	-40	-	90	℃

5.3. Working voltage

Table 5.3:Module operating voltage

Parameter	inimum	Typical	Maximum	Unit
VBAT	3.5	3.8	4.2	V
VBUS	4	5	6	V

5.4. Digital Interface Features

Table 5.4:Digital Interface Features (1.8V)

Parameter	Description	Minimum	Typical	Maximum	Unit

V_{IH}	Input high level voltage	1.17	1.8	2.1	V
V_{IL}	Input low level voltage	-0.3	0	0.63	V
V_{OH}	Output high level voltage	1.35	-	1.8	V
V_{OL}	Output low level voltage	0	-	0.45	V

5.5. SIM_VDD Features

Table 5.5:SIM_VDD Features

Parameter	Description	Minimum	Typical	Maximum	Unit
V_O	Output voltage	1.65	1.8	1.95	V
		-	2.95	-	
I_O	Output current	-	-	100	mA

5.6. PWRKEY Features

Table 5.6:PWRKEY features

Parameter	Description	Minimum	Typical	Maximum	Unit
PWRKEY	High level	1.4	-	-	V
	Low level	-	-	0.6	V
	Valid time	3000			ms

5.7. VCOIN Features

Table 5.7:VCOIN features

Parameter	Description	Minimum	Typical	Maximum	Unit
$VCOIN_{-IN}$	VCOIN Input voltage	2.5	3.0	3.1	V
$VCOIN_{-OUT}$	VCOIN Output voltage	-	3.0	-	V

5.8. Consumption (VBAT=3.8V)

Table 5.8:Consumption

Parameter	Description	Conditions	Minimum	Typical	Maximum	Unit

VBAT	Power supply voltage	The voltage must be between the maximum and minimum	3.5	3.8	4.2	V
Ivbat	Average current	Shutdown mode	-	-	139	uA
		WCDMAStandbyconsumption	-	-	6.3	mA
		FDDStandby consumption	-	-	7	mA
		TDDStandby consumption	-	-	7	mA
		CDMAStandby consumption	-	-	7	mA

5.9. Electrostatic Protection

The module is not protected against electrostatic discharge. Therefore, you must pay attention to ESD protection when producing, assembling, and operating modules.

5.10. Module Operating Frequency Band

The following table lists the operating bands of the modules in accordance with 3GPP TS 05.05 technical specification.

Table 5.9:Module operating frequency band

Band	Receiving	Transmitting	Physical Channel
CDMA BC0	869 ~ 894MHz	824 ~ 849MHz	TX:1～799 ； 991～1023
			RX: 2937~3088
WCDMA B1	2110 ~ 2170 MHz	1920 ~ 1980 MHz	TX: 9612~9888
			RX: 10562~10838
WCDMA B5	869 ~ 894MHz	824 ~ 849MHz	TX: 4132~4233
			RX: 4357~4458
WCDMA B8	925 ~ 960MHz	880 ~ 915MHz	TX: 2712~2863
			RX: 2937~3088
LTE B1	2110 ~ 2170 MHz	1920 ~ 1980 MHz	TX: 18000 ~ 18599
			RX: 0~599
LTE B3	1805 ~ 1880 MHz	1710 ~ 1785 MHz	TX: 19200~19949
			RX: 1200~1949
LTE B5	869 ~ 894MHz	824 ~ 849MHz	TX: 20400~20649
			RX: 2400~2649
LTE B7	2620 ~ 2690MHZ	2500 ~ 2570MHZ	TX: 20750~21449
			RX: 2750~3449
LTE B8	925 ~ 960MHz	880 ~ 915MHz	TX: 21450~21799
			RX: 3450~3799
LTE B20	791 ~	832 ~ 862MHz	TX: 24150~24449
			RX: 6150~6449

	821MHZ		
LTE B28	758 ~ 803MHZ	703 ~ 748MHz	TX: 27210~27660 RX: 9210~9560
LTE B34	2010 ~ 2025 MHz	2010 ~ 2025 MHz	36200 ~ 36349
LTE B38	2570 ~ 2620 MHz	2570 ~ 2620 MHz	37750 ~ 38249
LTE B39	1880 ~ 1920 MHz	1880 ~ 1920 MHz	38250 ~ 38649
LTE B40	2300 ~ 2400 MHz	2300 ~ 2400 MHz	38650 ~ 39649
LTE B41	2496 ~ 2690 MHz	2496 ~ 2690 MHz	39650 ~ 41589
N1	2110 ~ 2170 MHz	1920 ~ 1980 MHz	TX: 384000 ~ 396000 RX: 422000~434000
N3	1805 ~ 1880 MHz	1710 ~ 1785 MHz	TX: 342000~357000 RX: 361000~376000
N5	869 ~ 894MHZ	824 ~ 849MHz	TX: 164800~169800 RX: 173800~178800
N7	2620 ~ 2690MHZ	2500 ~ 2570MHz	TX: 500000~514000 RX: 524000~538000
N8	925 ~ 960MHZ	880 ~ 915MHz	TX: 176000~183000 RX: 185000~192000
N20	791 ~ 821MHZ	832 ~ 862MHz	TX: 166400~172400 RX: 158200~164200
N28	758 ~ 803MHZ	703 ~ 748MHz	TX: 140600~149600 RX: 151600~160600
N41	2496 ~ 2690 MHz	2496 ~ 2690 MHz	500202 ~ 537000
N77	3300 ~ 4200 MHz	3300 ~ 4200MHz	620000 ~ 680000
N78	3300 ~ 3800 MHz	3300 ~ 3800MHz	620000 ~ 653332
N79	4400 ~ 5000MHz	4400 ~ 5000 MHz	693334 ~ 733332

5.11. RF Characteristics

The table below lists the conducted RF output power of the module in accordance with 3GPP TS 05.05 technical specification, 3GPP TS 134121-1 standard.

Table 5.10:Conducted output power

Band	**Standard Output(dBm)**	**Output Tolerance(dBm)**
CDMA	23 dBm	±2
WCDMA	23 dBm	+1/-3
LTE-TDD/FDD	23 dBm	±2
NR-FDD	23 dBm	+2/-3
NR-TDD	26 dBm	+2/-3

5.12. Module Conduction Receiving Sensitivity

The following table lists the conductive reception sensitivity of the module, which is tested under static conditions.

Table 5.11:Conduction reception sensitivitydual antenna

Band	Reception Sensitivity（TYP）	Reception Sensitivity（MAX）
N1	-98(10M)	3GPPrequirements
N3	-98(10M)	3GPPrequirements
N5	-98(10M)	3GPPrequirements
N7	-97(10M)	3GPPrequirements
N8	-98(10M)	3GPPrequirements
N20	-97(10M)	3GPPrequirements
N28	-98(10M)	3GPPrequirements
N38	-92(100M)	3GPPrequirements
N40	-92(50M)	3GPPrequirements
N41	-92(100M)	3GPPrequirements
N77	-93(100M)	3GPPrequirements
N78	-93(100M)	3GPPrequirements
N79	-91(100M)	3GPPrequirements
LTE FDD/TDD	See table6.12	3GPPrequirements

Note: N38/41/77/78/79 indicators of four antennas.

Table 5.12:LTE reference sensitivity 3GPP Dual Antenna Requirements (QPSK)

E-UTRA Band Number	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex Mode
1	-	-	-100	-97	-95.2	-94	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	FDD
5	-103.2	-100.2	-98	-95			FDD

6	-	-	-100	-97			FDD
7	-	-	-98	-95	-93.2	-92	FDD
8	-102.2	-99.2	-97	-94			FDD
9	-	-	-99	-96	-94.2	-93	FDD
10	-	-	-100	-97	-95.2	-94	FDD
11	-	-	-100	-97			FDD
12	-101.7	-98.7	-97	-94			FDD
13			-97	-94			FDD
14		-	-97	-94			FDD
...							
17	-	-	-97	-94			FDD
18	-	-	-1007	-977	-95.27	-	FDD
19	-	-	-100	-97	-95.2	-	FDD
20			-97	-94	-91.2	-90	FDD
21			-100	-97	-95.2		FDD
22			-97	-94	-92.2	-91	FDD
23	-104.7	-101.7	-100	-97	-95.2	-94	FDD
24			-100	-97			FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	FDD
26	-102.7	-99.7	-97.56	-94.56	-92.76		FDD
27	-103.2	-100.2	-98	-95			FDD
28		-100.2	-98.5	-95.5	-93.7	-91	FDD
31	-99.0	-95.7	-93.5				FDD
...							
33	-	-	-100	-97	-95.2	-94	TDD
34	-	-	-100	-97	-95.2	-	TDD
35	-106.2	-102.2	-100	-97	-95.2	-94	TDD
36	-106.2	-102.2	-100	-97	-95.2	-94	TDD
37	-	-	-100	-97	-95.2	-94	TDD
38	-	-	-100	-97	-95.2	-94	TDD
39	-	-	-100	-97	-95.2	-94	TDD
40	-	-	-100	-97	-95.2	-94	TDD
41	-	-	-98	-95	-93.2	-92	TDD

5.13. WIFI Main RF Performance

The following table lists the main RF performance under WIFI conduction.

Table 5.13:WIFI Main RFperformance parameters under conduction

2.4G Launch Performance					
	802.11B	802.11G	802.11N	802.11AX	
Transmitted power (minimum rate)	19	18	17	17	dBm

Transmitted power (maximum rate)	18	16	15	12	dBm
EVM (Maximum rate)	20%	-25	-28	-35	dB
2.4Greception performance					
Reception sensitivity	802.11B	802.11G	802.11N	802.11AX	
Minimum speed	-96	-91	-90	-91	dBm
Maximum speed	-88	-74	-71	-60	dBm
5G Launch Performance					
	802.11A	802.11N	802.11AC	802.11AX	
Transmitted power (minimum rate)	17	17	16	17	dBm
Transmitted power (maximum rate)	15	14	12	11	dBm
EVM (Maximum rate)	-25	-28	-30	-35	dB
5Greception performance					
Reception sensitivity	802.11A	802.11N	802.11AC	802.11AX	
Minimum speed	-90	-86	-90	-90	dBm
Maximum speed	-74	-71	-70	-60	dBm

5.14. BT Main RF Performance

The following table lists the main rf properties under BT conduction.

Table 5.14:Main RF performance parameters under BT conduction

Launch Performance				
Transmission power	DH5	2DH5	3DH5	
	11	6	6	dBm
Receiving Performance				
Reception sensitivity	DH5	2DH5	3DH5	
	-94.5	-94.5	-86	dBm

5.15. Main RF Performance of GNSS

The main RF performance under GNSS conduction is listed in the following table.

Table 5.15:Main RF performance parameters under GNSS conduction

GNSS Working Band::L1 1575.42MHZ; L5 1176.45MHZ

GNSS Carrier to noise ratio CN0: 35dB/Hz				
GNSSSensitivity:	Capture (cold start)	Capture (hot start)	tracking	
	-148	-156	-160	dBm
GNSSStartup time	hot start	Warmstart	cold start	
	5	20	38	s

6. Production

6.1. Top and Bottom Views

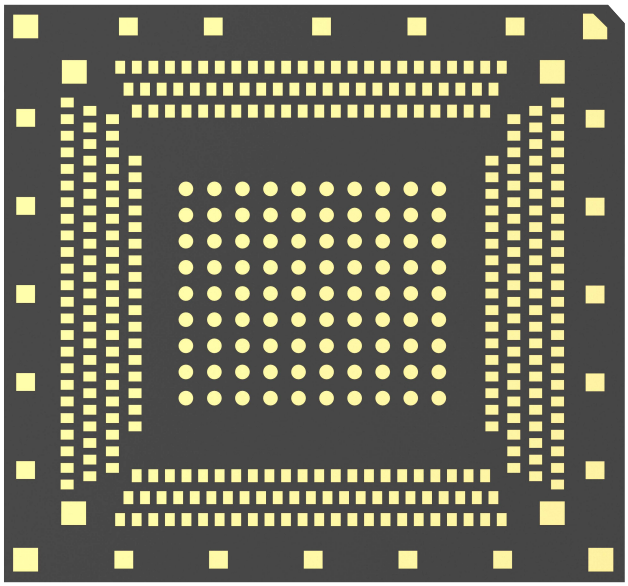


Fig6.1: Top and bottom views of modules

6.2. Recommended Welding Furnace Temperature Curve

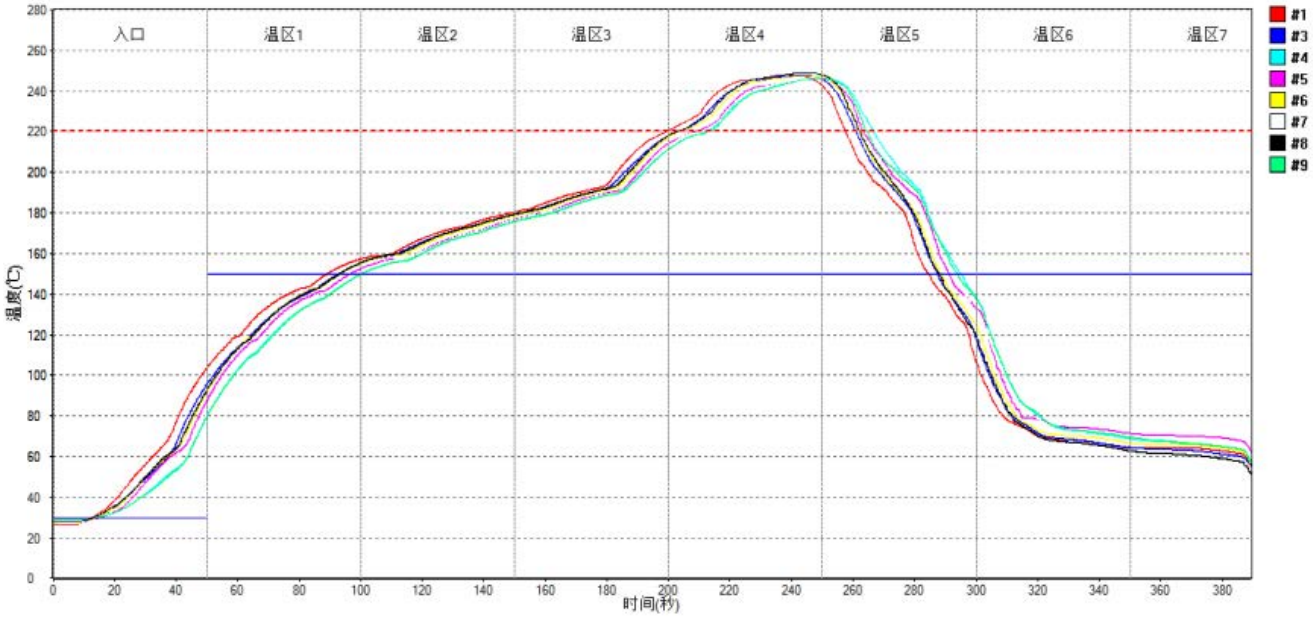


Fig6.2: Recommended welding furnace temperature curve

6.3. Humidity Sensitive Characteristic (MSL)

The SRM700U meets humidity sensitivity level 3. Under the environmental conditions of temperature < 30 degrees and relative humidity < 60%, dry packaging according to IPC/JEDEC standard J-STD-020C specification. Under the environmental conditions of temperature < 40 degrees and relative humidity < 90%, the shelf life is at least 6 months without unpacking. After unpacking, table 6.1 lists the shelf life of modules corresponding to different moisture sensitivity levels.

Table 6.1:Humidity sensitivity level differentiation

Level	Factory environment ≦ +30℃/60%RH
1	Indefinite quality at ambient ≦ Under +30℃/85% RH condition
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Force bake before use. After baking, the module must be fitted within the time limit specified on the label.

After unpacking, Under the environmental conditions of temperature < 30 degrees and relative humidity < 60%, SMT within 168 hours in 60% of environmental conditions. Bake if the above conditions are not met. Note: Oxidation risk: Baking SMD packaging can cause metal oxidation and, if excessive, can lead to solder ability problems during circuit board assembly. Baking SMD packages for temperature and time, thus limiting solder ability considerations. The accumulated baking time at temperatures greater than 90°C and up to 125°C should not exceed 96 hours.

7. Appendix

7.1. Related Documents

Table 7.1:The related documents

Serial number	File Name	Comment
[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10:	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05:	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)

[4]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+);Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+);Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[8]	AN_Serial Port	AN_Serial Port

7.2. Terminology and Interpretation

Table 7.2:Terminology and Interpretation

Term	Explanation
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol

PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
Telephone book abbreviation	explain
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

Shenzhen MeiG Smart Technology Co., Ltd. Shanghai Branch
Add: 5th Floor, Building G, No. 2337, Gudai Road, Minhang District, Shanghai
Zip: 201100
Tel:+862154278676
Fax:+862154278679
Http:www.meigchina.com

Doc：

Products with CE Marking comply with the radio Equipment Directive（2014/53/EU）and UK Radio Equipment Regulations (SI 2017/1206) The full text of the EU declaration of conformity is available at the following internet address: http://www.meigsmart.com

RF exposure statement：

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of d=20 cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

Temperature: -40° C ~ +75° C

Bands:

The Radio equipment operation with following frequecy bands Maximum tune-up power(dBm)

BT3.0: 10dBm(eirp)

Ble: 5dBm(eirp)

2.4GWIFI:19dBm(eirp)

5GWIFI: 16dBm(eirp)

5.8GWIFI:13dBm(eirp)

6G WIFI:13dBm(eirp)

Band 1: 23.72 dBm

Band 8: 23.47 dBm

Band 1: 23.11 dBm

Band 3: 24.38 dBm

Band 7: 24.36 dBm

Band 8: 23.24 dBm

Band 20: 23.25 dBm

Band 28: 22.89 dBm

Band 38: 22.92 dBm

Band 40: 23.05 dBm

n1: 23.63 dBm

n3: 23.51 dBm

n5: 24.01 dBm

n7: 24.45 dBm

n8: 24.30 dBm

n20: 23.75 dBm

n28: 23.99 dBm

n38: 23.72 dBm

n40: 23.72 dBm

n41: 24.10 dBm

n77: 24.88 dBm

n78: 25.12 dBm

5G WIFI restricetion info:

This device may be operated in all members states of the EU and UK. Observe national and local regulation where the device is used. This device maybe restricted for use, depending on local network. More details as below.

1. The 5150-5250MHz frequency band: Indoor, including installations inside road vehicles, trains and aircraft, and limited outdoor use (note 1).

2. The 5250-5350MHz frequency band: Indoor use, inside buildings only. Installations in road vehicles, trains and aircraft are not permitted (note 2).Outdoor use is not permitted.

3. The 5470-5725MHz frequency band: Indoor and outdoor use. Installations in road vehicles, trains and aircraft and use for UAS are not permitted (note3).

4. In accordance with the relevant statutory requirements in UK, the 5150-5350MHz frequency range is restricted to indoor use only in UK.

Note1: If used outdoors, equipment shall not be attached to a fixed installation or to the external body of road vehicles, a fixed infrastructure or a fixed outdoor antenna.

Note2：Operation of WAS/RLAN installations in large aircraft (excluding multi-engined helicopters) is permitted until 31 December 2028 with a maximum mean e.i.r.p. for in-band emissions of 100mW.

Note3: Operation of WAS/RLAN installations in large aircraft (excluding multi-engined helicopters), except in the frequency band 5600-5650MHz, is permitted until 31 December 2028 with a maximum mean e.i.r.p. for in-band emissions of 100mW.

	UK		AT	BE	BG	CH	CY	CZ	DE
			DK	EE	EL	ES	FI	FR	HR
			HU	IE	IS	IT	LT	LI	LU
			LV	MT	NL	NO	PL	PT	RO
			SE	SK	TR	SI	UK(NI)		

15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

15.21 Changes or modification warning.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help

RF warning for Mobile device:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 15

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not application

2.5 Trace antenna designs

Not application

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

Antenna Type(Dipole)	BT/2.4Gwifi 3.95 dBi; U-NII-1 1.46dBi; U-NII-2A 1.52dBi; U-NII-2C 1.29dBi; U-NII-3 1.48dBi; U-NII-5 0.96dBi; U-NII-6 0.75dBi; U-NII-7 0.77dBi; U-NII-8 1.56dBi;
Antenna connector	SMA

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: “Contains FCC ID: 2APJ4-SRM700”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

Industry Canada statement

This K019-CW43-DW complies with ISED's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Le présent appareil est conforme aux CNR d' ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) le dispositif ne doit pas produire de brouillage préjudiciable, et (2) ce dispositif doit accepter tout brouillage reçu, y compris un brouillage susceptible de provoquer un fonctionnement indésirable.

5G WIFI statement

The device is restricted to indoor use when operated in 5150MHz~5350MHz to reduce the potential for interference

Radiation Exposure Statement:

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with greater than 20cm between the radiator & your body.