

ME3630

HARDWARE DEVELOPMENT GUIDE

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LTE Module Series

REVISION HISTORY

Version	Date	Description
1.0	2017-01-18	1 st released version
1.1	2017-10-23	Add information of ME3630-E&ME3630-J2A& ME3630-J2AS
1.2	2018-01-31	Add ME3630-E2C Update pin POWER_ON
1.3	2018-04-23	Add ME3630-A1C Update parts of reference circuit Add the pin assignment
1.4	2018-04-28	Update the document format
1.5	2019-04-28	Complete mechanical dimensions Update the power supply Improve the figure pixel

ABOUT THIS DOCUMENT

A. Application Range

This document is the Product Technical Specification for the ME3630 GSM/WCDMA/LTE-FDD module. It defines the high level product features and illustrates the interface for these features. This document is intended to cover the hardware aspects of the product, including electrical and mechanical.

B. Reading Note

The symbols below are the reading notes you should pay attention on:



WARNING or ATTENTION



NOTE or REMARK

C. Purpose

This document provides the hardware solutions and development fundamentals for a product with the module. By reading this document, the user can have an overall knowledge of the module and a clear understanding of the technical parameters. With this document, the user can successfully fulfill the application and development of wireless Internet product or equipment.

Besides the product features and technical parameters, this document also provides the product reliability tests and related testing standards, RF performance indexes and a guide on the design of user circuits, to provide the user with a complete design reference.



NOTE:

To ensure the module manufacturing and welding quality, do as the chapter 7 of Manufacturing Guide in this document. The force on the squeegee should be adjusted so as to produce a clean stencil surface on a single pass and ensure the module soldering quality.

D. Abbreviations

Table below is a list of abbreviations involved in this document, as well as the English full names.

Abbreviations	Full Name
3GPP	Third Generation Partnership Project
AP	Another name of DTE
CHAP	Challenge Handshake Authentication Protocol
CE	European Conformity
CMOS	Complementary Metal Oxide Semiconductor
DCE	Data Communication Equipment
DL	Downlink
DTE	Data Terminal Equipment
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
ESD	Electro-Static discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
GPIO	General-purpose I/O
LCC	Leadless Chip Carrier

LDO	Low-Dropout
LED	Light Emitting Diode
LTE	Long Term Evolution
ME	Mobile Equipment
MO	Mobile Origination Call
MT	Mobile Termination Call
MSB	Most Significant Bit
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PAP	Password Authentication Protocol
PPP	Point to Point Protocol
RTC	Real Time Clock
SMS	Short Messaging Service
SMT	Surface Mount Technology
SPI	Serial Peripheral Interface
TBD	To Be Determined
TCP	Transmission Control Protocol
TIS	Total Isotropic Sensitivity
TRP	Total Radiated Power
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UL	Up Link
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
URC	Unsolicited result code
VIH	Logic High level of input voltage
VIL	Logic Low level of input voltage
VOH	Logic High level of output voltage
VOL	Logic Low level of output voltage

SAFETY INFORMATION

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating ME3610 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. If not so, GOSUNCN does not take on any liability for customer failure to comply with these precautions.

	Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a hands free kit) cause distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers a Airplane Mode which must be enabled prior to boarding an aircraft.
	Switch off your wireless device when in hospitals or clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.
	GSM cellular terminals or mobiles operate over radio frequency signal and cellular network and cannot be guaranteed to connect in all conditions, for example no mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.
	Your cellular terminal or mobile contains a transmitter and receiver. When it is on, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres including fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

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1. PRODUCT OVERVIEW

1.1. GENERAL DESCRIPTION

ME3630-U& ME3630-E&ME3630-J &ME3630-A is a LTE/WCDMA/GSM wireless communication module with LCC interface. It is widely applied to but not limited to the various products and equipment such as laptops, vehicle-mounted terminals, and electric devices, by providing data services.

Customer can choose the dedicated type based on the wireless network configuration and using area. The following table shows the entire radio band configuration of ME3630 series.

Table 1–ME3630 Supported Band

PID	RF support	RF Band	Transmit Frequency (TX)	Receive Frequency (RX)
ME3630-U1A(CAT4)	LTE FDD	B2	1850 to 1910 MHz	1930 to 1990 MHz
ME3630-U1C(CAT1)		B4	1710 to 1755 MHz	2110 to 2155 MHz
		B5	824 to 849 MHz	869 to 894 MHz
		B12	698 to 716 MHz	728 to 746 MHz
		B17	704 to 716 MHz	734 to 746 MHz
	WCDMA	B2	1850 to 1910 MHz	1930 to 1990 MHz
		B5	824 to 849 MHz	869 to 894 MHz
ME3630-E1C(CAT4)	LTE FDD	B1	1920 to 1980 MHz	2110 to 2170 MHz
ME3630-E2C(CAT1)		B3	1710 to 1785 MHz	1805 to 1880 MHz
		B7	2500 to 2570 MHz	2620 to 2690 MHz
		B8	880 to 915 MHz	925 to 960 MHz
		B20	832 to 862MHz	791 to 821 MHz
	WCDMA	B1	1920 to 1980 MHz	2110 to 2170 MHz
		B8	880 to 915 MHz	925 to 960 MHz
	GSM	B3	1710 to 1785 MHz	1805 to 1880 MHz
		B8	880 to 915 MHz	925 to 960 MHz
ME3630-J2A(CAT4)	LTE FDD	B1	1920 to 1980 MHz	2110 to 2170 MHz
ME3630-J2AS(CAT 1)		B3	1710 to 1785 MHz	1805 to 1880 MHz
		B5	824 to 849 MHz	869 to 894 MHz
		B7	2500 to 2570 MHz	2620 to 2690 MHz
		B8	880 to 915 MHz	925 to 960 MHz
		B18	815 to 830 MHz	860 to 875 MHz
		B19	830 to 845 MHz	875 to 890 MHz
		B21	1447.9 to 1462.9 MHz	1459.9 to 1510.9 MHz

ME3630	WCDMA	B1	1920 to 1980 MHz	2110 to 2170 MHz
		B5	824 to 849 MHz	869 to 894 MHz
		B6	830 to 840 MHz	875 to 885 MHz
		B8	880 to 915 MHz	925 to 960 MHz
		B19	830 to 845 MHz	875 to 890 MHz
	LTE	B2	1850 to 1910 MHz	1930 to 1990 MHz
		B5	824 to 849 MHz	869 to 894 MHz
		B7	2500 to 2570 MHz	2620 to 2690 MHz
	WCDMA	B2	1850 to 1910 MHz	1930 to 1990 MHz
		B5	824 to 849 MHz	869 to 894 MHz
	GSM	B2	1850 to 1910 MHz	1930 to 1990 MHz
		B5	824 to 849 MHz	869 to 894 MHz

1.2. KEY FEATURES

The table below describes the detailed features of the ME3630 module.

Table 1–2 ME3630 Key Features

Feature	Description	
Physical	Small form factor-30 mm × 30 mm × 2.3mm LCC with 80 pins	
Power Supply	The range of voltage supply is 3.4V-4.2V, typical value is 3.8V	
Frequency Bands	A1C (For America)	LTE B2, B5,B7 WCDMA B2,B5 GSM B2,B5
	U1A&U1C	LTE FDD: B2,B4 ,B5,B12,B17 WCDMA: B2,B5
	E1C&E2C (For Europe)	LTE FDD: B1,B3,B7,B8,B20 WCDMA: B1,B8 GSM: B3, B8
	J2A&J2AS	LTE FDD: B1, B3, B5, B7,B8, B18, B19, B21 WCDMA: B1, B5, B6, B8, B19
Rx Diversity	A1C (For America)	LTE B2, B5,B7,,B40 WCDMA B2,B5
	U1A&U1C	LTE FDD:B2,B4,B5,B12,B17 WCDMA:B2,B5
	E1C&E2C	LTE FDD: B1,B3,B7,B8,B20

		WCDMA: B1,B8
	J2A&J2AS	LTE FDD: B1, B3, B5, B7,B8, B18, B19, B21 WCDMA: B1, B5, B6, B8, B19
Transmission Rate	LTE FDD (CAT4): Max 150Mbps(DL)/Max 50Mbps(UL)	
Network Protocols	Support TCP/PPP/UDP/FTP protocols Support PAP, CHAP protocols used for PPP connection.	
USIM Interface	1.8V/3V support SIM extraction/hot plug detection Support SIM and USIM	
UART Interface	Support two UART interface: main UART interface and debug UART interface Main UART interface: Eight lines on main UART interface Support RTS and CTS hardware flow control Baud rate can reach up to 921600 bps,115200 bps by default Used for AT command, data transmission or firmware upgrade Debug UART interface: Two lines on debug UART interface, can be used for software debug, firmware upgrade	
USB Interface	Compliant with USB 2.0 specification (slave only) Used for AT command communication, data transmission, software debug and firmware upgrade.	
USB Driver	Support Windows XP, Windows Vista, Windows 7, Windows 8, Windows 10, Windows CE5.0/6.0 and later, Linux 2.6.20 and later, Android 2.3 / 4.X/ 5.X	
SDIO interface	1.8V support (full speed) 4bits,SDIO compatible to WLAN (802.11)	
Antenna Interface	Include main antenna ,diversity antenna and GNSS antenna	
Rx-diversity	Support WCDMA/LTE Rx-diversity	
AT commands	Compliant with 3GPP TS 27.007,27.005 and GOSUNCN enhanced AT commands	
Network Indication	Use LED_MODE to indicate network connectivity status	
SMS	Text and PDU mode Point to point MO and MT SMS saving/reading to SIM card or module storage SMS cell broadcast	
Temperature Range	Normal operation: -30°C to +75°C Restricted operation: -40°C~ -30°C and +75°C~ +85°C ¹⁾ Storage temperature: -40°C to +85°C	
Firmware Upgrade	USB interface or UART interface or OTA(WEFOTA)	

1.3. FUNCTION DIAGRAM

The figure below shows a block diagram of the ME3630 and illustrates the major functional parts.

- Power management
- Baseband
- Memory
- RF send-receive
- Peripheral interface
 - UART interface
 - USIM card interface
 - USB interface
 - SDIO interface
 - SPI interface
 - I2C interface
 - ADC interface
 - Status interface (LED)

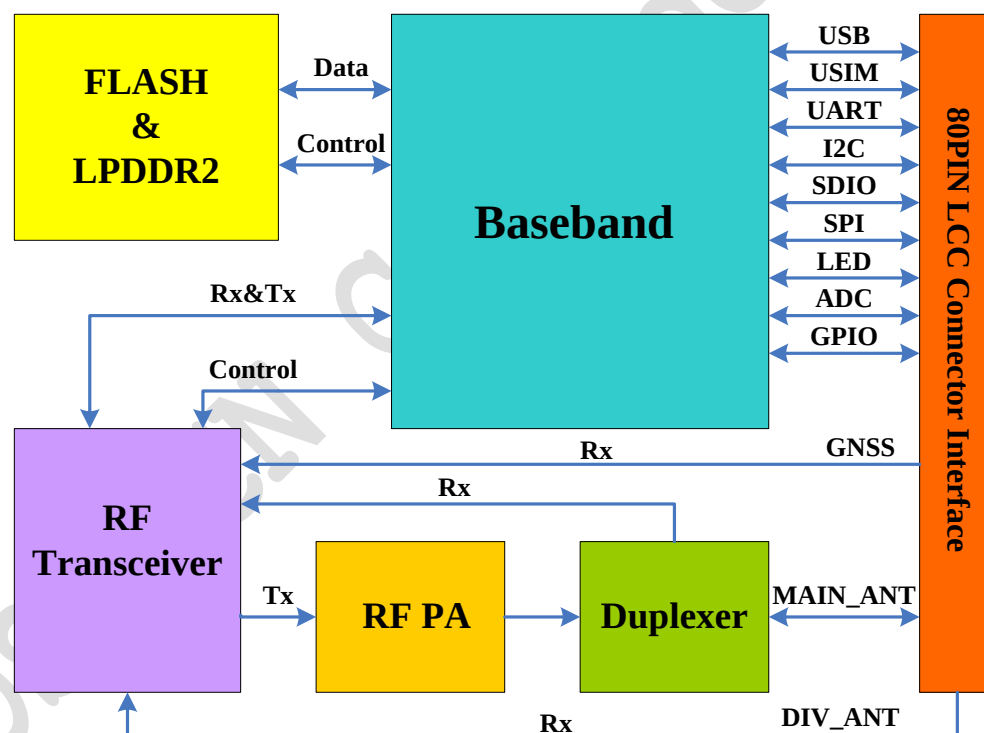


Figure 1-1 System Connection Structure

1.4. EVALUATION BOARD

In order to help you to develop applications with ME3630, GOSUNCN supplies an evaluation board (G2000/GE2015), RS-232 to USB cable, USB data cable, power adapter, antenna and other peripherals to control or test the module. For details, please refer to the related document [\[GE2015 Dev Board User Guide\]](#).

2. APPLICATION INTERFACE

2.1. GENERAL DESCRIPTION

ME3630 is equipped with an 80-pin 0.72mm pitch SMT pads plus 16-pin ground pads and reserved pads that connect to customer's cellular application platform. Sub-interface included in these pads is described in detail in the following chapters:

- Pin assignment
- Pin description
- Power supply
- Turn on/off scenarios
- USIM interface
- USB interface
- UART interface
- Network status indication
- ADC interface
- WAKEUP_IN signal
- WAKEUP_OUT signal
- GPIO interface

2.2. PIN ASSIGNMENT

The following figure shows the pin assignment of the ME3630 module.

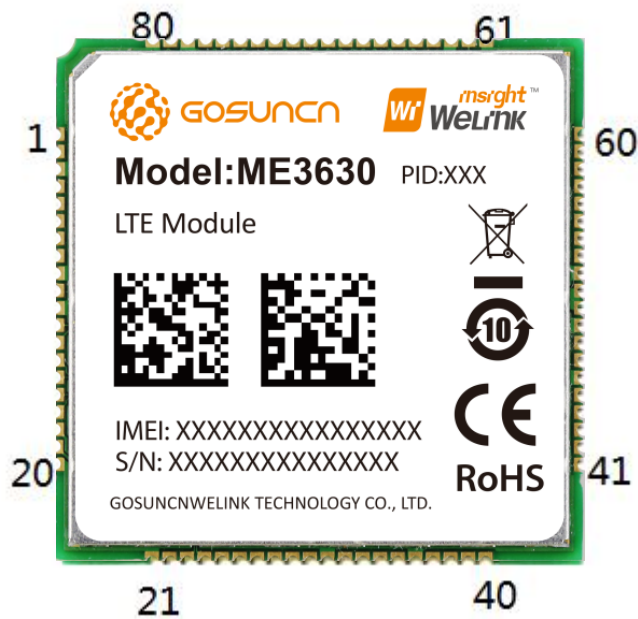
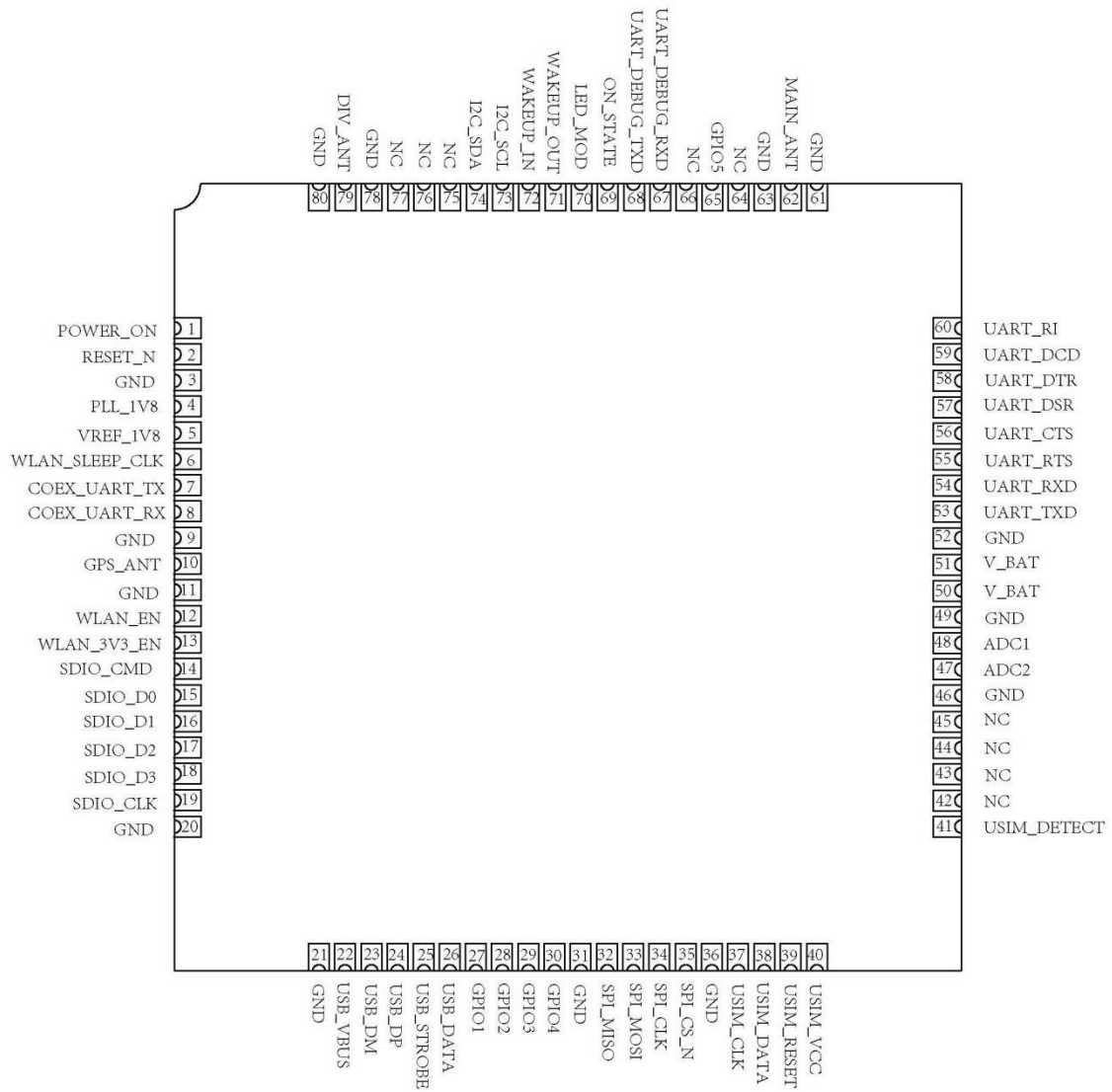


Figure 2–1 Pin Assignment

**NOTE:**

Keep all NC pins unconnected.

2.3. PIN DESCRIPTION

The following table shows the IO Parameters Definition.

Table 2–1 IO Parameters Definition

Type	Description
IO	Bidirectional input/output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

The logic levels are described in the following table.

Table 2–2 Logic levels Description

Parameter	Min	Max	Unit
VIH	$0.65 \cdot VDD_IO$	$VDD_IO + 0.3$	V
VIL	-0.3	$0.35 \cdot VDD_IO$	V
VOH	$VDD_IO - 0.45$	VDD_IO	V
VOL	0	0.45	V

**NOTE:**

VDD_IO is the voltage level of pins.

The following tables show the ME3630's pin definition.

Table 2–3 Pin Description

Power Supply					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
V_BAT	50,51	PI	Power supply for module	Vmax = 4.2V Vmin = 3.4V Vnorm = 3.8V	It must be able to provide sufficient current in a transmitting burst which typically rises to 2.0A
VREF_1V8	5	PO	Provide 1.8V for external circuit	Vnorm = 1.8V Imax = 300mA	Power supply for external GPIO'S pull up circuits
PLL_1V8	4	PO	Provide 1.8V for external circuit	Vnorm = 1.8V Imax = 20mA	This pin can only be used for WiFi interface, and can left unconnected when not used.
GND	3,9,11,20,21,31,36, 46,49,52, 61,63,78,		Ground		

	80,				
Turn On/Off					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
POWER_ON	1	DI	Turn on/off module	V _{IH} max = 2.1V V _{IH} min = 1.17V V _{IL} max = 0.63V	Pull-up to 0.8V internally, active low
RESET_N	2	DI	Reset module	V _{IH} max = 2.1V V _{IH} min = 1.17V V _{IL} max = 0.63V	Active low
Status Indication					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
ON_STATE	69	DO	Module power on/off status indicator	V _{OH} min = 1.35V V _{OL} max = 0.45V	1.8V power domain
LED_MODE	70	DO	Indicate the module network registration mode	V _{OH} min = 1.35V V _{OL} max = 0.45V	1.8V power domain
USB Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
USB_DP	24	IO	USB differential data bus		Compliant with USB 2.0 standard specification Require differential impedance of 90Ω
USB_DM	23	IO			
USB_VBUS	22	DI	USB plug detect pin, not USB power		USB plug detect
HSIC Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
USB_STROBE	25	IO	HSIC strobe	InterChip USB(HSIC)	line impedance 50 ohm, isometric constraint is less than 2 mm, line length is less than 10 cm
USB_DATA	26	IO	HSIC data		
USIM Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
USIM_VCC	40	PO	Power supply for USIM card	For 1.8V USIM: V _{max} = 1.9V V _{min} = 1.7V For 3.0V USIM: V _{max} = 3.05V V _{min} = 2.7V I _O max = 50mA	Either 1.8V or 3V is supported by the module automatically
USIM_DATA	38	IO	Data signal of USIM card	For 1.8V USIM: V _{IL} max = 0.63V	Pull-up to USIM_VCC with 10k resistor internally

				V_{IH} min = 1.17V V_{OL} max = 0.45V V_{OH} min = 1.35V For 3V USIM: V_{IL} max = 1.05V V_{IH} min = 1.95V V_{OL} max = 0.45V V_{OH} min = 2.6V	
USIM_CLK	37	DO	Clock signal of USIM card	For 1.8V USIM: V_{OL} max = 0.45V V_{OH} min = 1.35V For 3V USIM: V_{OL} max = 0.45V V_{OH} min = 2.6V	
USIM_RST	39	DO	Reset signal of USIM card	For 1.8V USIM: V_{OL} max = 0.45V V_{OH} min = 1.35V For 3V USIM: V_{OL} max = 0.45V V_{OH} min = 2.6V	
USIM_DETECT	41	DI	USIM card input detection	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain. Active low If no need of USIM detect, leave this pin not connected.
ADC Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
ADC1	48	AI	Analog to digital	0.05V to 4.15V	External sensor signal detection
ADC2	47	AI	Analog to digital	0.05V to 4.15V	External sensor signal detection
Main UART Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
UART_TXD	53	DO	Transmit data	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain
UART_RXD	54	DI	Receive data	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain
UART_RTS	55	DO	Request to send	V_{IL} min = -0.3V V_{IL} max = 0.63V V_{IH} min = 1.17V V_{IH} max = 2.1V	1.8V power domain
UART_CTS	56	DI	Clear to send	V_{OL} max = 0.45V V_{OH} min = 1.35V	1.8V power domain

UART_DSR	57	DO	Data set ready	V _{IL} min = -0.3V V _{IL} max = 0.63V V _{IH} min = 1.17V V _{IH} max = 2.1V	1.8V power domain.
UART_DTR	58	DI	Data terminal ready	V _{IL} min = -0.3V V _{IL} max = 0.63V V _{IH} min = 1.17V V _{IH} max = 2.1V	1.8V power domain.
UART_DCD	59	DO	Data carrier detection	V _{OL} max = 0.45V V _{OH} min = 1.35V	1.8V power domain
UART_RI	60	DO	Ring indicator	V _{OL} max = 0.45V V _{OH} min = 1.35V	1.8V power domain, DO not pull-up external
Debug UART Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
UART_DEBUG_TXD	68	DO	Transmit data	V _{OL} max = 0.45V V _{OH} min = 1.35V	1.8V power domain
UART_DEBUG_RXD	67	DI	Receive data	V _{IL} min = -0.3V V _{IL} max = 0.63V V _{IH} min = 1.17V V _{IH} max = 2.1V	1.8V power domain
RF Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
MAIN_ANT	62	IO	Main antenna	50Ω impedance	
DIV_ANT	79	AI	Diversity antenna	50Ω impedance	
GNSS_ANT	10	IO	GNSS antenna	50Ω impedance	
I2C Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
I2C_SCL	73	DO	I2C serial clock	V _{OL} max = 0.45V V _{OH} min = 1.35V	Pull-up to 1.8V through external 2.2K resistance, active low
I2C_SDA	74	IO	I2C serial data	V _{OL} max = 0.45V V _{OH} min = 1.35V V _{IL} min = -0.3V V _{IL} max = 0.63V V _{IH} min = 1.17V V _{IH} max = 2.1V	Pull-up to 1.8V through external 2.2K resistance, active low
SDIO Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
SDIO_CMD	14	IO	Secure digital CMD	V _{OL} max = 0.45V V _{OH} min = 1.35V V _{IL} min = -0.3V	Pull-up to 1.8V through external 10K resistance, active low

				$V_{IL} \text{ max} = 0.63V$ $V_{IH} \text{ min} = 1.17V$ $V_{IH} \text{ max} = 2.1V$	
SDIO_D0	15	IO	Secure digital IO data bit 0	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$ $V_{IL} \text{ min} = -0.3V$ $V_{IL} \text{ max} = 0.63V$ $V_{IH} \text{ min} = 1.17V$ $V_{IH} \text{ max} = 2.1V$	1.8V power domain
SDIO_D1	16	IO	Secure digital IO data bit 1	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$ $V_{IL} \text{ min} = -0.3V$ $V_{IL} \text{ max} = 0.63V$ $V_{IH} \text{ min} = 1.17V$ $V_{IH} \text{ max} = 2.1V$	1.8V power domain
SDIO_D2	17	IO	Secure digital IO data bit 2	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$ $V_{IL} \text{ min} = -0.3V$ $V_{IL} \text{ max} = 0.63V$ $V_{IH} \text{ min} = 1.17V$ $V_{IH} \text{ max} = 2.1V$	1.8V power domain
SDIO_D3	18	IO	Secure digital IO data bit 3	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$ $V_{IL} \text{ min} = -0.3V$ $V_{IL} \text{ max} = 0.63V$ $V_{IH} \text{ min} = 1.17V$ $V_{IH} \text{ max} = 2.1V$	1.8V power domain
SDIO_CLK	19	DO	Secure digital CLK	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$	1.8V power domain
SDIO Interface					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
SPI_MISO	32	IO	SPI main input slave output	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$ $V_{IL} \text{ min} = -0.3V$ $V_{IL} \text{ max} = 0.63V$ $V_{IH} \text{ min} = 1.17V$ $V_{IH} \text{ max} = 2.1V$	1.8V power domain
SPI_MOSI	33	IO	SPI main output slave input	$V_{OL} \text{ max} = 0.45V$ $V_{OH} \text{ min} = 1.35V$ $V_{IL} \text{ min} = -0.3V$ $V_{IL} \text{ max} = 0.63V$	1.8V power domain

				V _{IH} min = 1.17V V _{IH} max = 2.1V	
SPI_CLK	34	DO	SPI clock	V _{OL} max = 0.45V V _{OH} min = 1.35V	1.8V power domain
SPI_CS_N	35	DO	SPI segment	V _{OL} max = 0.45V V _{OH} min = 1.35V	1.8V power domain
WiF PINs					
WLAN_SLEEP_CLK	6	DO	WLAN sleep clock	V _{OL} max = 0.45V V _{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
COEX_UART_TX	7	DO	LTE transmitter sync for coexistence with UART	V _{OL} max = 0.45V V _{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
COEX_UART_RX	8	DI	LTE receiver sync for coexistence with UART	V _{IL} max = 0.63V V _{IH} min = 1.17V	Only supported by firmware with WiFi. Other firmware, this pin is NC When pull-up this pin to 1.8V, the module will enter emergency download mode.
WLAN_EN	12	DO	WLAN enable	V _{OL} max = 0.45V V _{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
WLAN_3V3_EN	13	DO	WLAN power enable	V _{OL} max = 0.45V V _{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
WLAN_SLEEP_CLK	6	DO	WLAN sleep clock	V _{OL} max = 0.45V V _{OH} min = 1.35V	Only supported by firmware with WiFi. Other firmware, this pin is NC
Other Pins					
Pin Name	Pin NO.	I/O	Description	DC Characteristics	Comment
WAKEUP_IN	72	DI	Sleep mode control, External device wakeup module	V _{IL} min = -0.3V V _{IL} max = 0.45V V _{IH} min = 1.53V V _{IH} max = 2.1V	1.8V power domain. Pull-down internally. Edge-triggered, Rising edge wake up module; Falling edge modules can enter sleep
WAKEUP_OUT	71	DO	Output wakeup signal, wake up the external devices	V _{OL} max = 0.8V V _{OH} min = 1.35V	Wakeup external circuits
GPIO	27, 28, 29, 30, 65	IO	General input/output	V _{OL} max = 0.45V V _{OH} min = 1.35V V _{IL} min = -0.3V V _{IL} max = 0.63V V _{IH} min = 1.17V V _{IH} max = 2.1V	If unused, keep them floating. DO not pull-up PIN77 external
NC	66,64,75,76,77,4 5,44,43,42		No connection		NC, there is no connection internal, please keep them floating .

2.4. POWER SUPPLY

2.4.1. POWER SUPPLY PINS

The ME3630 is supplied through the V_BAT signal with the following characteristics.

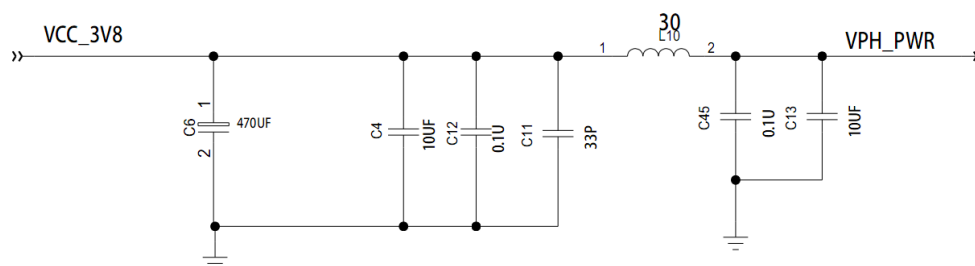
Table 2-4 Power Supply

Pin Name	Pin NO.	Description	Minimum	Typical	Maximum	Unit
V_BAT	50,51	Power supply for module	3.4	3.8	4.2	V
GND	3, 9, 11, 20, 21, 31, 36, 46, 49, 52, 61, 63, 78, 80,	Ground	-		-	

GND signal (Pin No: 3/9/11/20/21/31/36/46/49/52/61/63/78/80) is the power and signal ground of the module, which needs to be connected to the ground on the system board. If the GND signal is not connected completely, the performance of module will be affected.

2.4.2. DECREASE VOLTAGE DROP

The power supply range of the module is 3.4V~ 4.2V. So we recommended to add Energy storage capacitor (C6: 470μF). Filter capacitor(10μF, 0.1μF, 33pF) need to be added to reduce interference. The capacitors should be placed close to the ME3630's V_BAT pins. The following figure shows structure of the power supply.



PLACE CLOSE TO MODULE

Figure 2-2 The input reference circuit of VBAT

In poor situation of the network, the antenna will transmit at the maximum power, so it's recommended that continuous power supply capacity is up to 2.5A when the module supports GSM mode, and it's up to 1.5A in other modes.

The PCB traces from the V_BAT pins to the power source must be wide enough to ensure that there isn't too much voltage drop occurs in the transmitting procedure. The width of V_BAT trace should be no less than 2mm, and the principle of the V_BAT trace is the longer, the wider.

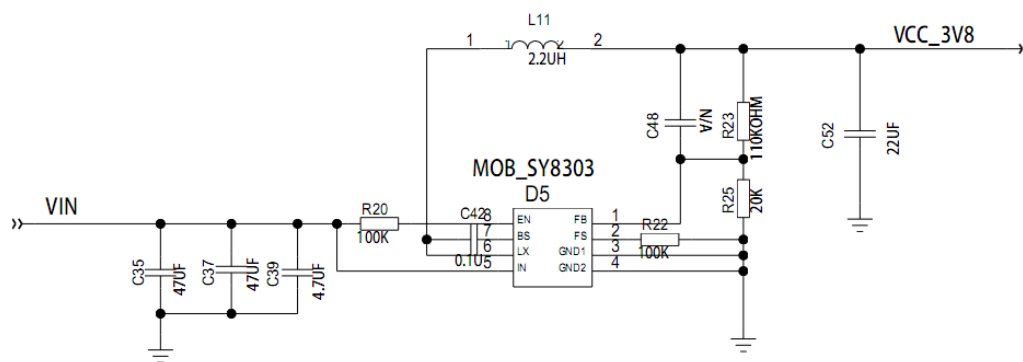
In addition, make the ground plane as complete as possible, and play more holes.

2.4.3. REFERENCE CIRCUIT OF POWER SUPPLY

• Option 1:DC-DC switching

The over-current capability requirement of DC/DC switching power supply needs to be above 2.5A. When the input and output voltage difference is large, you need to select Buck circuit to improve translate efficiency.

The reference power supply circuit design with DC-DC is shown as figure below:



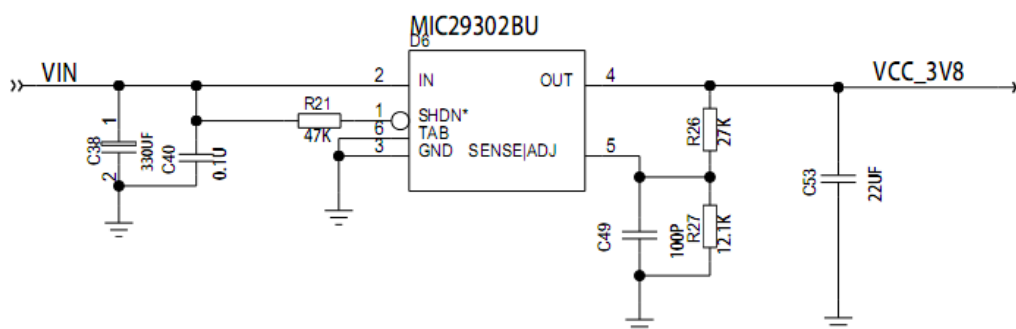
FB: 0.6V
 VIN: 4.5V-40V 3.0A
 D5 TYPE: SY8303AIC

Figure 2-3 Reference circuit of DC-DC

- Option 2: LDO

The over-current capability of LDO is above 2.5A. This LDO is apply to this situation: input and output voltage difference is small.

The reference power supply circuit design with LDO is shown as figure below:



FB: 1.24V
 VIN: 16V 3A
 D6 TYPE: MIC29302WU
 XRP29302ETBTR-L

Figure 2-4 Reference circuit of LDO

2.5. TURN ON SCENARIOS

When MCU can provide high/low level pulse with adjustable length, the reference circuit to turn-on/off module is as shown in the following figure below.

The resistors in Figures below are only the recommended value and they need to adjust according to the actual situation.

Power-on by dynatron, the circuit ① connect ON/OFF to high level to power-on the module, the circuit ② can connect ON/OFF to low level to power-on the module

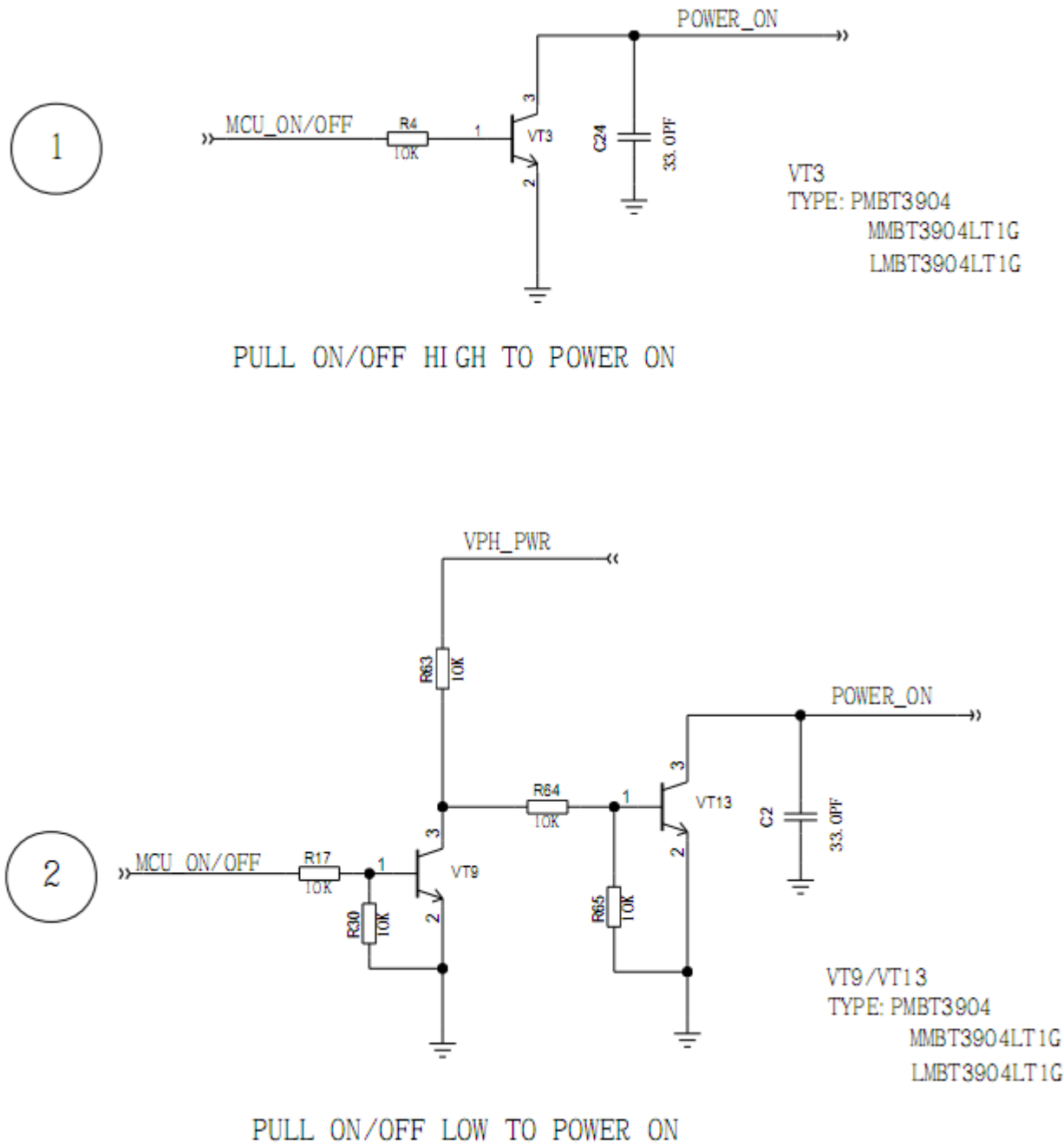


Figure 2-5 Reference circuit of POWER_ON

The table below is the information of power-on/off pin

Table 2-5 Definition of POWER_ON

Pin Name	Pin NO.	I/O	Description	Comment
POWER_ON	1	DI	Turn on/off the module	low active. Pull-up to 0.8V internally

The power on scenarios is illustrated as the following figure, the module will power on and working when the POWER_ON pin keep in low level for T1, in this process , please ensure VBAT steady.

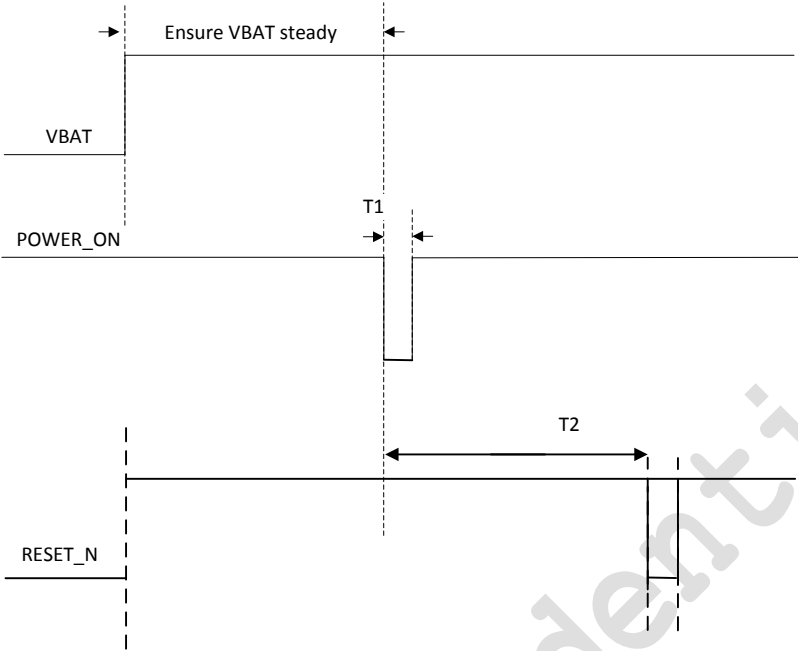


Figure 2-6 Timing of Turning on Mode

Table 2-6 Power-on Time

Parameter	Description	Min	Typical	Max	Unit
T1	The period that the Power-on signal for power on operation is kept on the low PWL	0.1	0.2	--	Second
T2	The minimum interval between the POWER_ON and RESET signals if you want to reset the module after power-on.	10	15	--	Second

2.6. TURN OFF SCENARIOS

The module supports two modes to turn off:

Mode 1:

Pull down pin1 (POWER_ON) for 2.5-3s will turn off the module. The power off process will take 22s at least. The reference circuit can refer to the figure 2-5.

Table 2-7 Power-off Time

Parameter	Description	Min	Typical	Max	Unit
T2	The period that the POWER_ON signal for power off operation is kept on the low PWL	2.5	3	--	second
T3	The period that the VBAT signal should be kept after power off operation is down	22	--	--	second

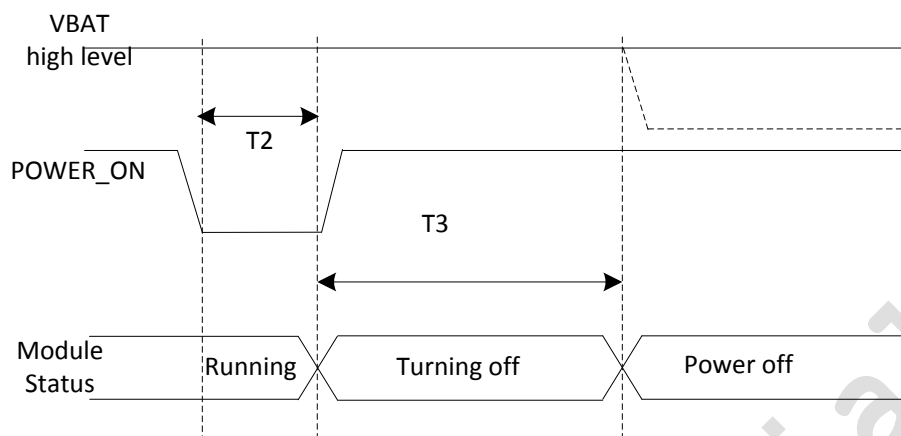


Figure 2-7 Timing of Turning off Mode

Mode 2:

Send command of AT+ZTURNOFF, and the power off process will take 15s at least.

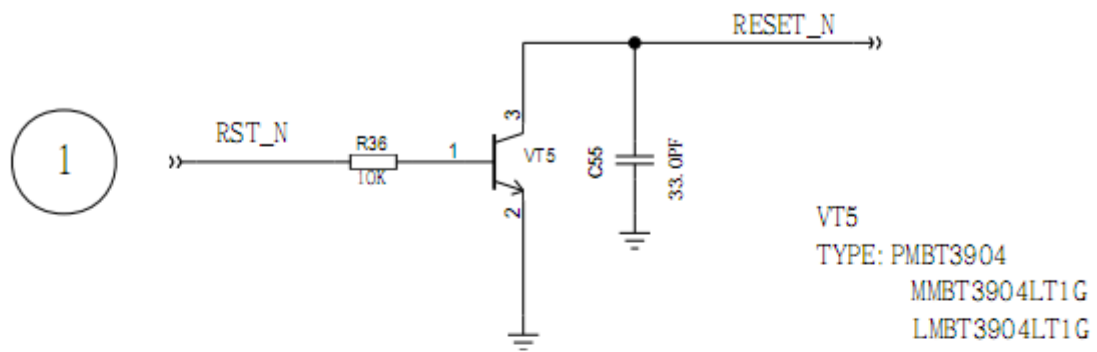
Note:when using modules, you need to avoid power off abnormally and frequently, as it will cause several risks shwon as below:

1. it will damage the flash permanently.
2. it can' t send deregiter message to e-NodeB, and the MMS takes for the module is still registering to network, and it won' t remind "the user can' t reach" or "the user has turn down" when it' s called(MT).

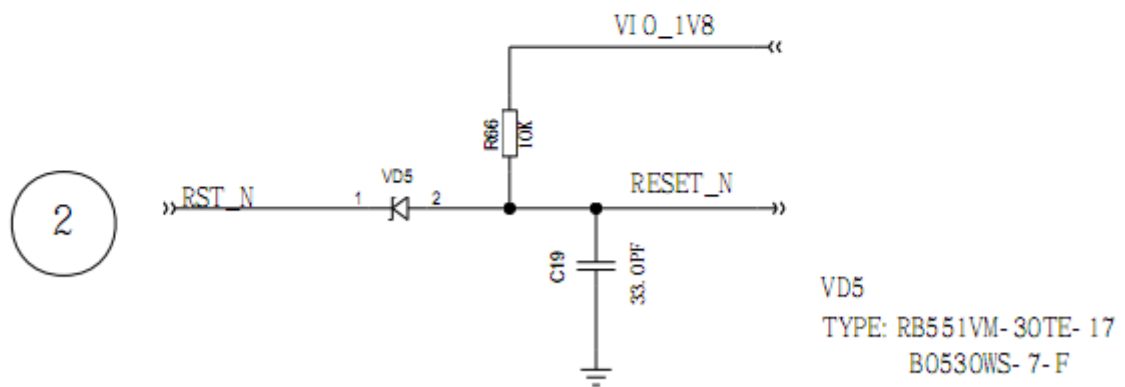
2.7. RESET SCENARIOS

When the software stops response, you can pulled down RESET_N pin(pin2) for 1 second to reset the module's system.

When MCU can provide high/low level pulse with 1 second, the reference circuit to reset module is as shown in the following figure below. The resistors in Figures below are only the recommended value and they need to adjust according to the actual situation.



PULL RST_N HIGH TO RESET



PULL RST_N LOW TO RESET

Figure 2-8 reference circuit to reset module

The reset scenario is illustrated as the following figure,

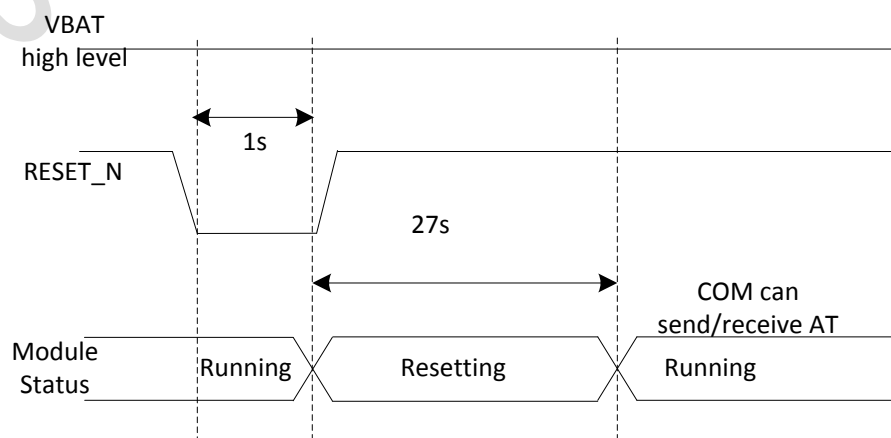


Figure 2-9 Timing of Reset Mode

Mode 2:

Send command of AT+ZRST, and the RESET process until the AT port can communicate will take 27s at least.

Figure 2–10 Reference Circuit of the 8 Pin USIM Card

ME3630 supports USIM card hot-plugging via the USIM_DETECT pin. For details, refer to document *[AT Command Reference Guide of Module Product ME3630]*. If you do not need the USIM card detect function, keep USIM_DETECT unconnected.

The reference circuit for using a 6-pin USIM card socket is illustrated as the following figure.

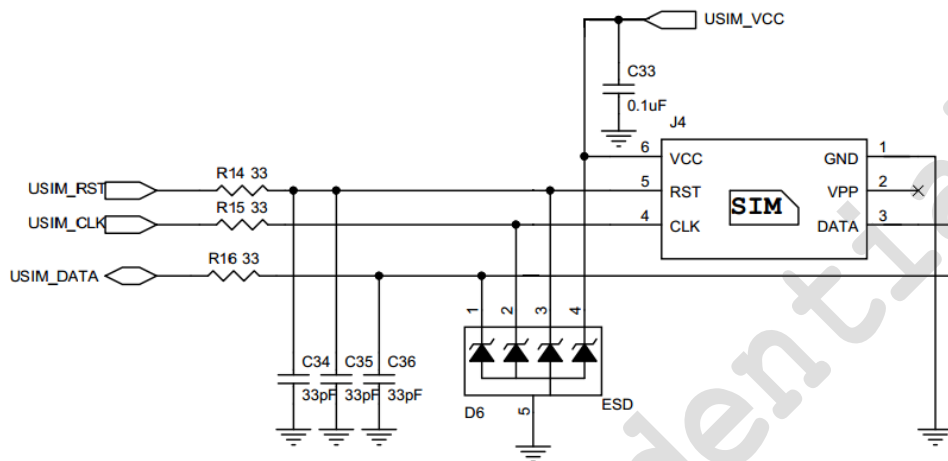


Figure 2–11 Reference Circuit of the 6 Pin USIM Card

NOTE:

- ✓ R14~R16 and D6 are applied to suppress the EMI spurious transmission and enhance the ESD protection. D6 should be closed to J4
- ✓ The value of C33 should be less than 1uF.

In order to enhance the reliability and availability of the USIM card in customer's application, please follow the following criterion in the USIM circuit design:

- Keep layout of USIM card as close as possible to the module. Assure the possibility of the length of the trace is less than 50mm.
- Keep USIM card signal away from RF and V_BAT alignment.
- Assure the ground between module and USIM cassette short and wide. Keep the width of ground and USIM_VCC no less than 0.5mm to maintain the same electric potential. The decouple capacitor of USIM_VCC should be less than 1uF and must be near to USIM cassette.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away with each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add TVS such as WILL (<http://www.willsemi.com>) ESDA6V8AV6. The 33Ω resistors should be added in series between the module and the USIM card so as to suppress the EMI spurious transmission and enhance the ESD protection. Please note that the USIM peripheral circuit should be close to the USIM card socket.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion is applied.

2.8.2. DESIGN CONSIDERATIONS FOR USIM CARD HOLDER

For 8-pin USIM card holder, it is recommended to use Molex 91228.

Please visit <http://www.molex.com> for more information.

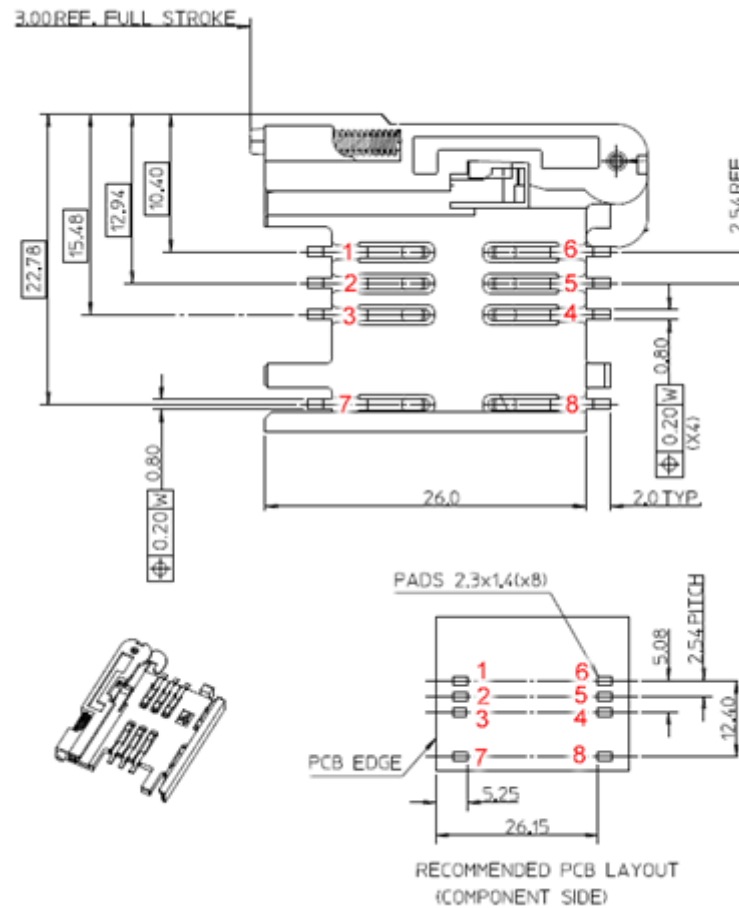


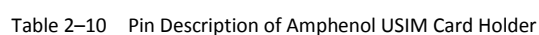
Figure 2-12 Molex 91228 USIM Card Holder

Table 2-9 Pin Description of Molex USIM Card Holder

Pin Name	Pin NO.	Function
GND	1	Ground
VPP	2	Not connected
DATA I/O	3	USIM card data
CLK	4	USIM card clock
RST	5	USIM card reset
VDD	6	USIM card power supply
DETECT	7	USIM card Detection
NC	8	Not defined, Connect to Ground

For 6-pin USIM card holder, it is recommended to use Amphenol C707 10M006 512 2.

Please visit <http://www.amphenol.com> for more information.

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RST	5	USIM card reset
VDD	6	USIM card power supply

2.9. USB INTERFACE

ME3630 contains one integrated USB transceiver which complies with the USB 2.0 specification and supports high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps) mode. The USB interface is primarily used for AT command, data transmission, software debug and firmware upgrade. The following table shows the pin definition of USB interface.

Table 2-11 USB Pin Description

Pin Name	Pin NO.	I/O	Description	Comment
USB_DP	24	IO	USB differential data bus (positive)	Require differential impedance of 90Ω
USB_DM	23	IO	USB differential data bus (negative)	Require differential impedance of 90Ω
USB_VBUS	22	DI	USB plug detect pin, not USB power	USB plug detect
GND	21		Ground	

More details about the USB 2.0 specifications, please visit <http://www.usb.org/home>.

For different use purposes, different designs can be referred to:

- Connect USB interface to USB connector directly. The following figure shows the reference circuit of USB interface

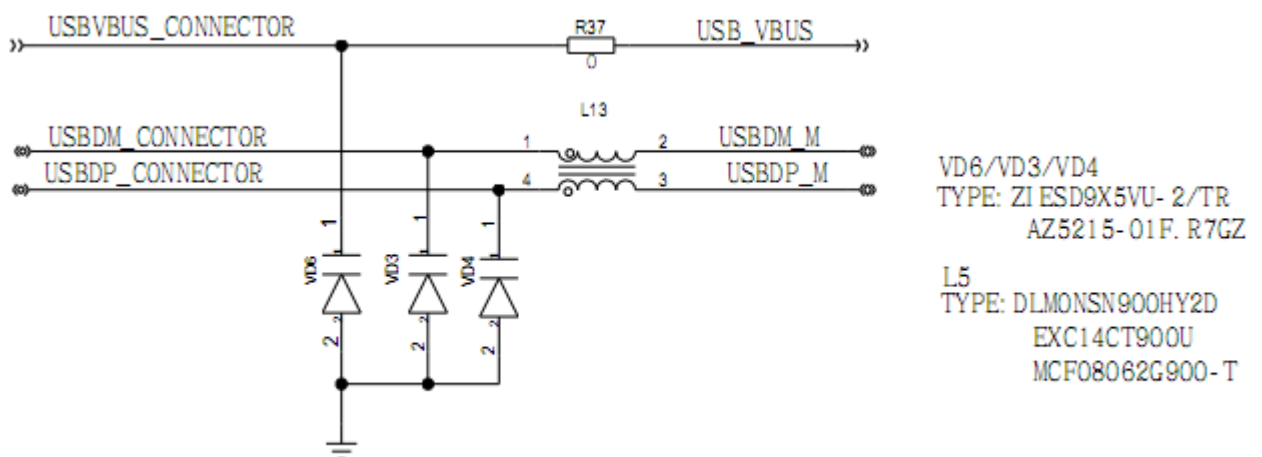


Figure 2-14 Reference Circuit of USB Application

- Reference Circuit of USB Communication between module and AP is the one below. The 0Ω in the figure should be placed near pin.

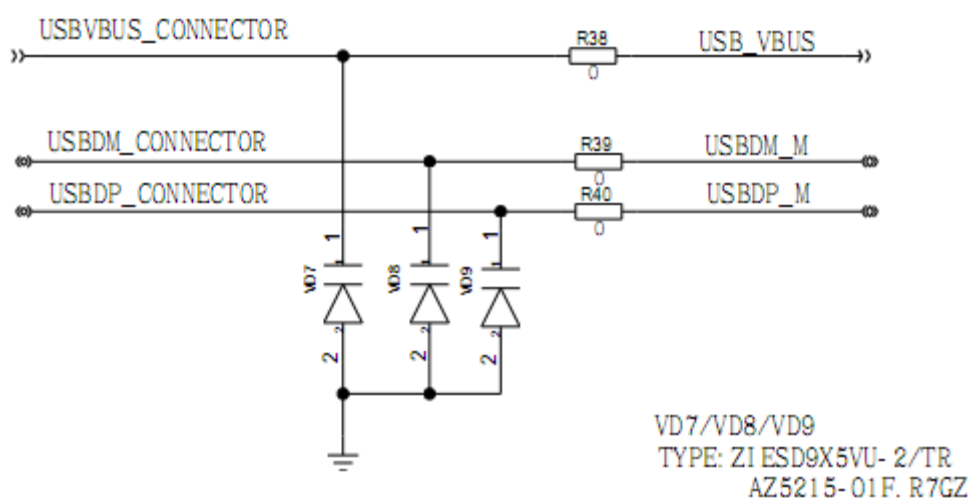


Figure 2-15 Reference Circuit of USB Communication between module and AP

- When USB is not the desired function, connect differential signal, power and GND via test points. We recommend to connect these pins to the standard pin header in order to convenient for debugging and upgrading.

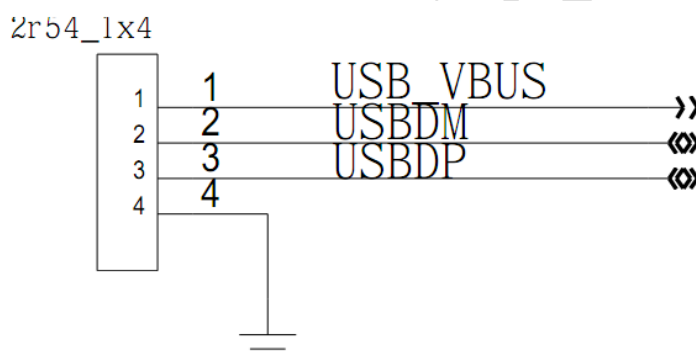


Figure 2-16 Reference circuit of USB when USB is not the desired function

Note: we recommend connecting the USB interface for update and debugging the module.

In order to ensure the USB interface design corresponding with the USB 2.0 specification, please comply with the following principles.

It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90ohm.

Pay attention to the influence of junction capacitance of ESD component on USB data lines. Typically, the capacitance value should be less than 3pF.

Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding not only upper and lower layer but also right and left side.

Keep the ESD components as closer to the USB connector as possible.

2.10. UART INTERFACE

The module provides two UART interfaces: Main UART Port and Debug UART Port. The Main UART Port can work in full

function mode while the Debug UART Port is used for software debugging . The following show the different features.

Main UART interface support 1200 2400 4800 9600 19200 38400 57600 115200 230400 460800 921600 1000000 1500000 2000000 2500000 3000000 3500000bps baud rate, the default is 115200bps, This interface can be used for data transmission; AT communication or firmware upgrade (upgrade is not supported currently).

Debug UART interface supports 115200bps baud rate. It can be used for software debug and firmware upgrade. The module is designed as the DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection.

The following tables show the pin definition of these two UART interfaces.

Table 2–12 Pin Definition of the Main UART Interface

Pin Name	Pin NO.	I/O	Description	Comment
UART_RI	60	DO	Ring indicator	1.8V power domain
UART_DCD	59	DO	Data carrier detection	1.8V power domain
UART_CTS	56	DI	Clear to send	1.8V power domain
UART_RTS	55	DO	Request to send	1.8V power domain
UART_DTR	58	DI	Data terminal ready	1.8V power domain.
UART_DSR	57	DO	Data set ready	1.8V power domain.
UART_TXD	53	DO	Transmit data	1.8V power domain
UART_RXD	54	DI	Receive data	1.8V power domain

Table 2–13 Pin Definition of the Debug UART Interface

Pin Name	Pin NO.	I/O	Description	Comment
UART_DEBUG_TXD	68	DO	Transmit data	1.8V power domain
UART_DEBUG_RXD	67	DI	Receive data	1.8V power domain

2.10.1. UART CONNECTION

Three normal connections for UART are shown in the figures below:

1. 8-wires UART connection mode, mainly used for MODEM mode(PPP dialing for example)

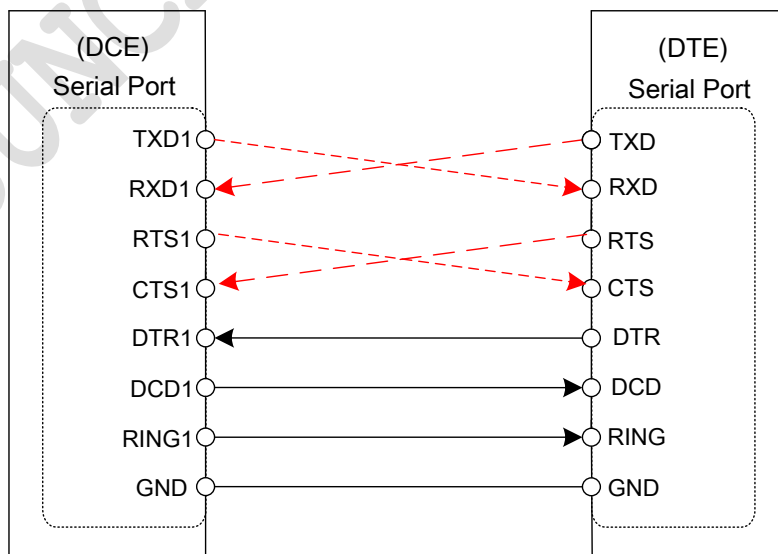


Figure 2–17 Schematic of 8-wire UART Connection

2. 3-wire UART connection:

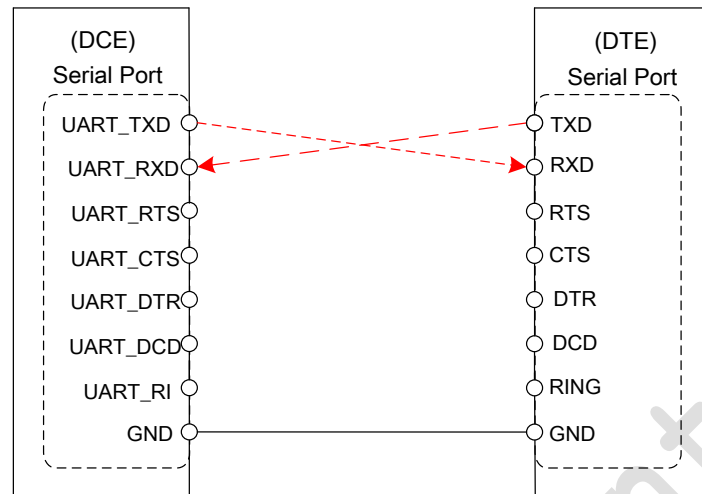


Figure 2-18 Schematic of 3-wire UART Connection

3. 4-wire UART connection, with hardware flow control:

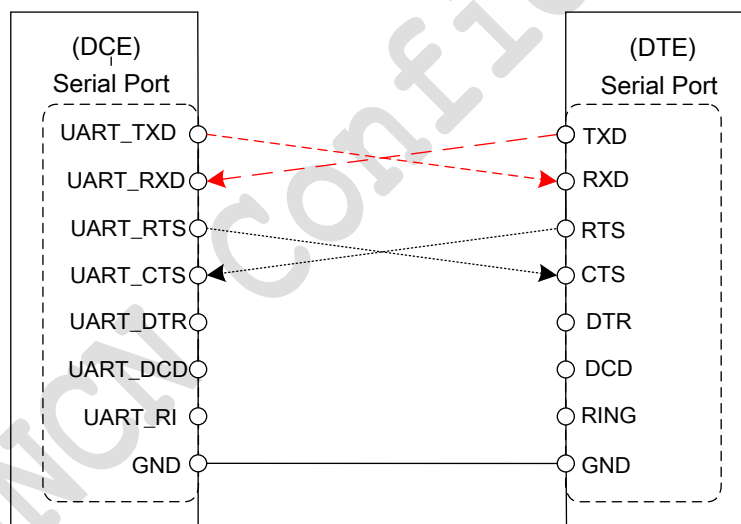


Figure 2-19 Schematic of 4-wire UART Connection

2.10.2. UART LEVEL MATCH

Notice the level match when connect module to external MCU. Level must be less than 3.0V under normal operation, and its default speed rate is 115200 bps.

We recommend to use audion or IC for UART level match circuit. The pictures below are the recommended level switch circuit for TXD, RXD, CTS, RTS. Each pin recommend two kinds of circuit, and you can select any one if necessarily.

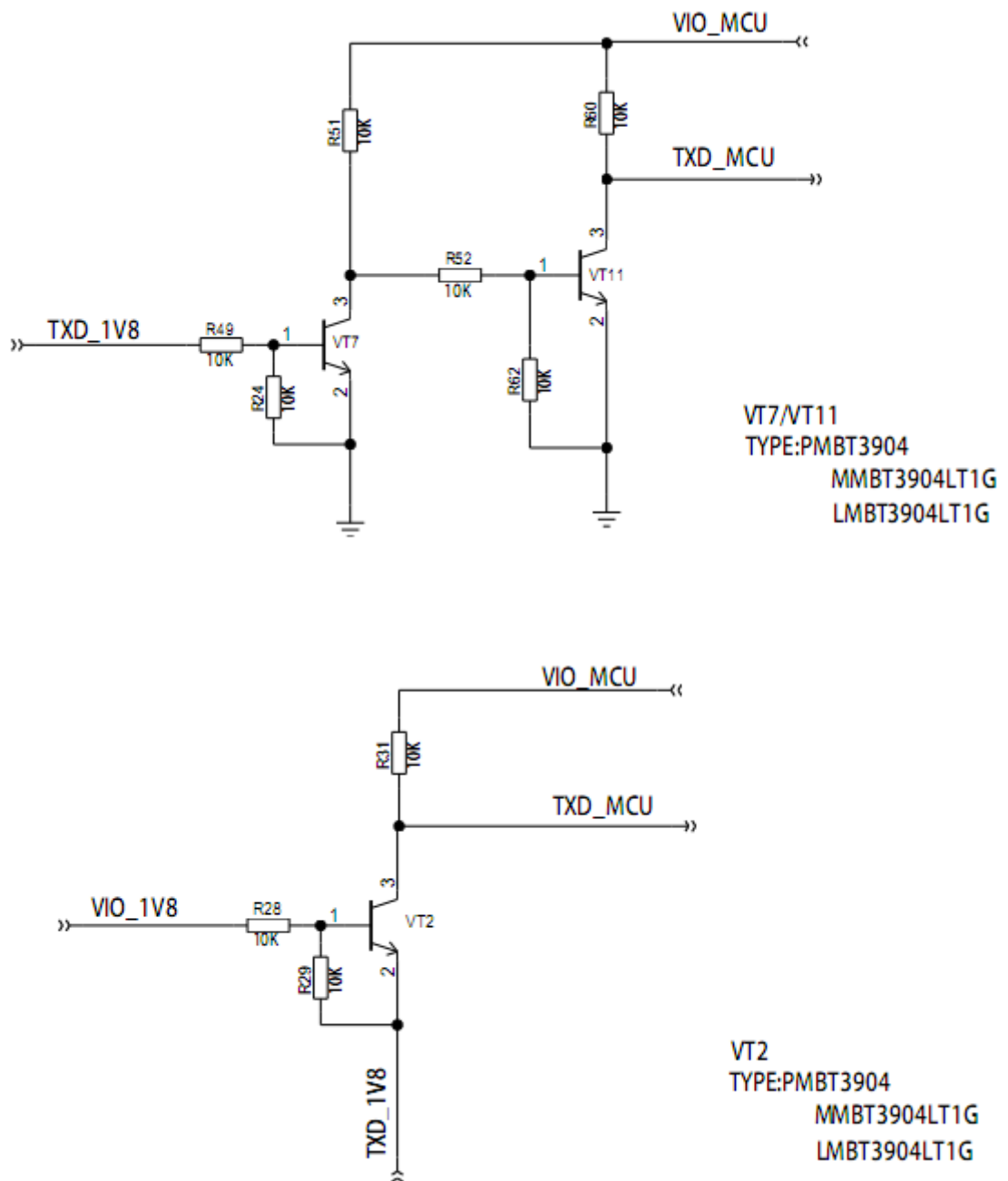
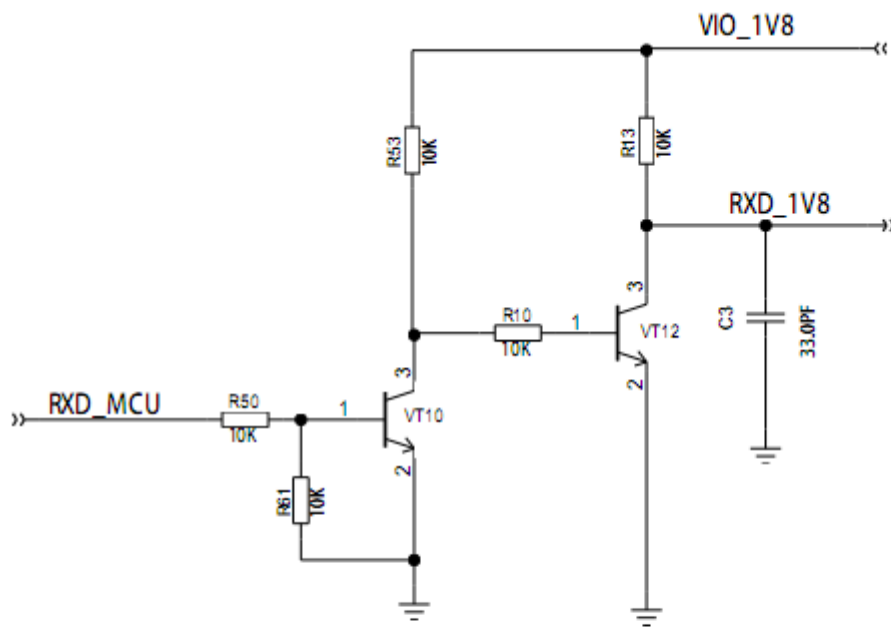
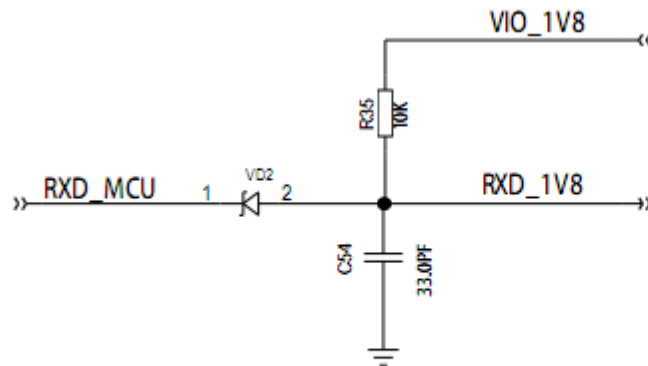


Figure 2-20 Recommended TXD circuit



VT10/VT12
 TYPE:PMBT3904
 MMBT3904LT1G
 LMBT3904LT1G



VD2 TYPE:RB551VM-30TE-17
 B0530WS-7-F

Figure 2-21 Recommended RXD circuit

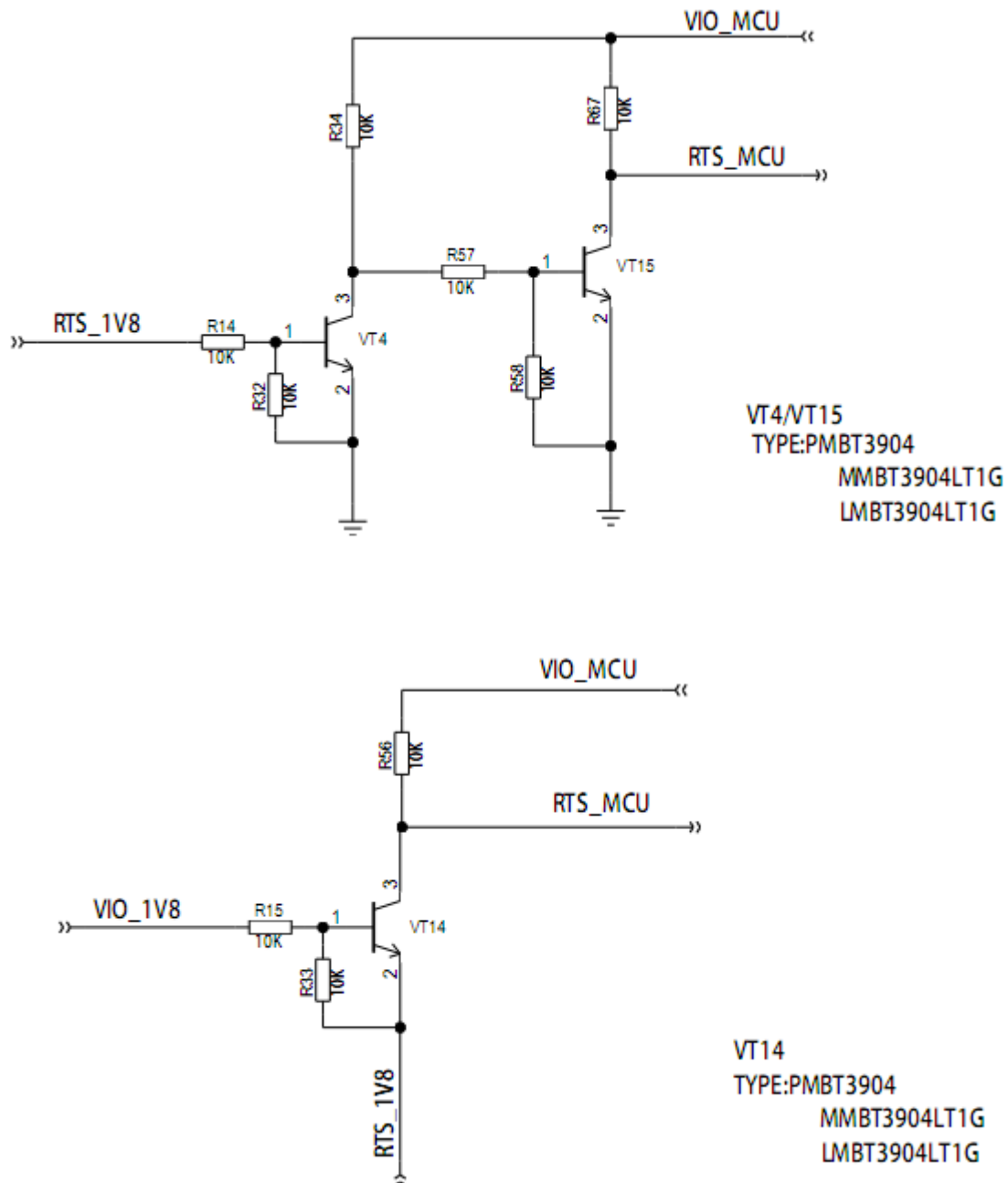


Figure 2-22 Recommended RTS circuit

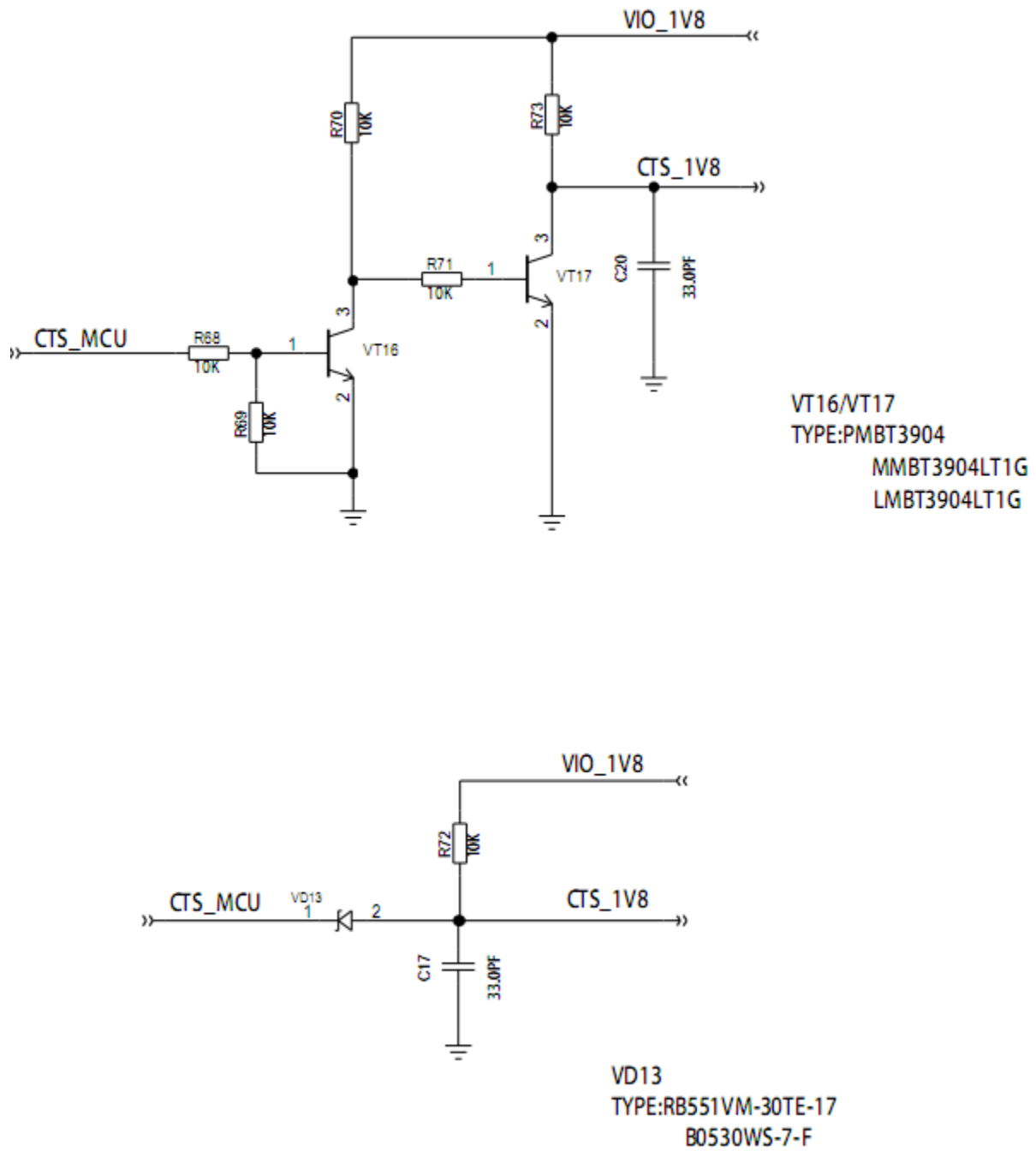
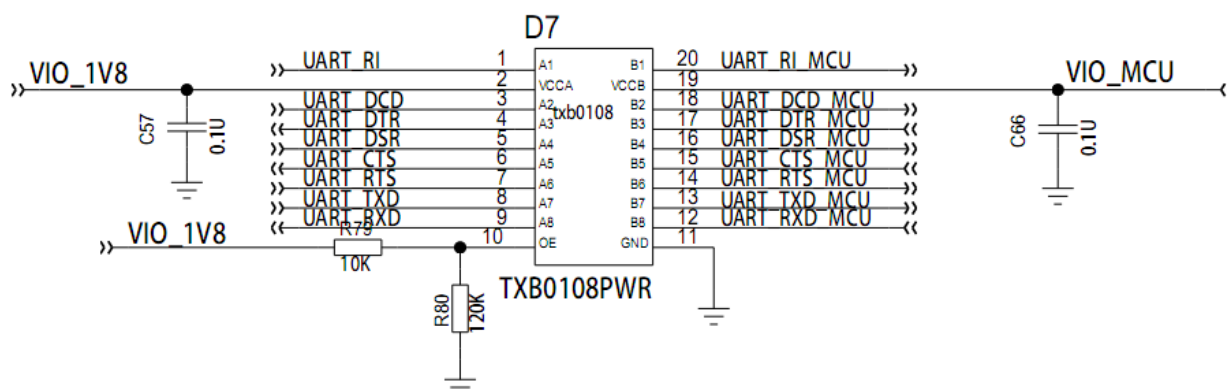


Figure 2-23 Recommended CTS circuit

2.10.3. USE IC FOR LEVEL SWITCH



NOTES:

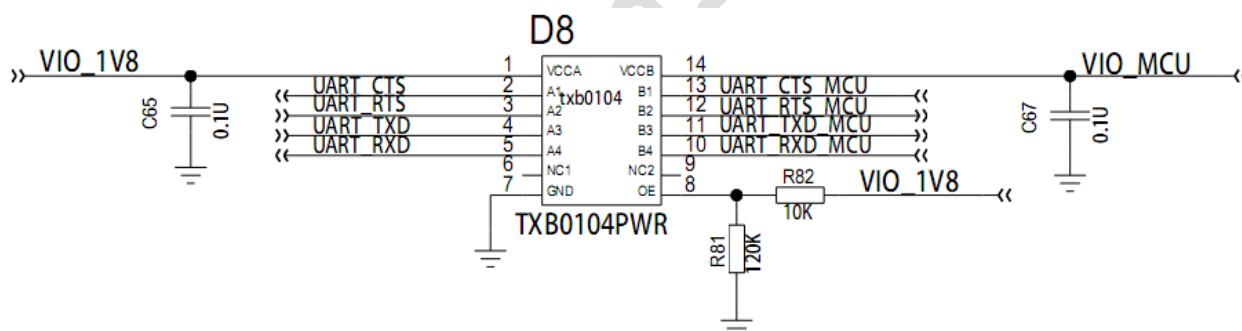
1.THE VOLTAGE DOMAIN OF UART IS 1.8V.

TXB0108 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.

2.VCCA SHOULD NOT EXCEED VCCB.

3.FOR MORE INFORMATION ABOUT TXB0108, PLEASE REFER TO THE DATASHEET.

Figure 2-24 Recommended 8-wires UART level switch circuit



NOTES:

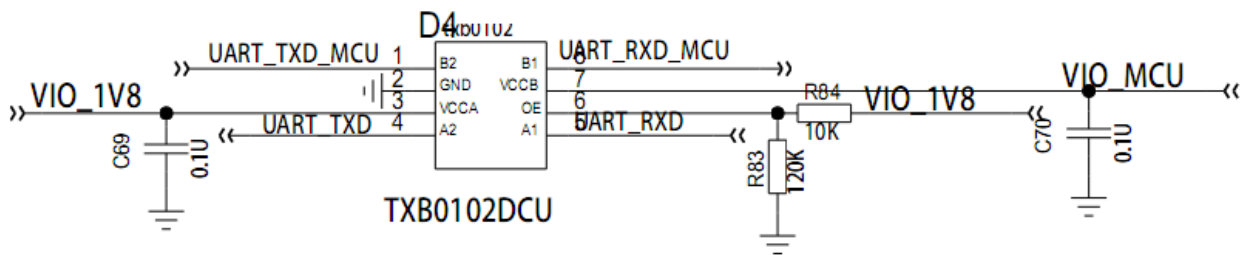
1.THE VOLTAGE DOMAIN OF UART IS 1.8V.

TXB0104 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.

2.VCCA SHOULD NOT EXCEED VCCB.

3.FOR MORE INFORMATION ABOUT TXB0104, PLEASE REFER TO THE DATASHEET.

Figure 2–25 Recommended 4-wires UART level switch circuit

**NOTES:**

1.THE VOLTAGE DOMAIN OF UART IS 1.8V.

TXB0102 REALIZE THE VOLTAGE LEVEL TRANSLATION BETWEEN MODULE AND MCU.

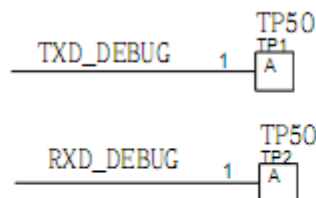
2.VCCA SHOULD NOT EXCEED VCCB.

3.FOR MORE INFORMATION ABOUT TXB0102, PLEASE REFER TO THE DATASHEET.

Figure 2–26 Recommended 2-wires UART level switch circuit

- **Debug UART Interface**

Debug UART Interface is 2-wires interface, we recommend the use to connect this two pins to test points or jumper header.



DEBUG UART(PIN67/68) SHOULD ADD TEST POINTS FOR DEBUG.

Figure 2–27 The test point of debug UART

2.11. NETWORK STATUS INDICATION

The network indication pin LED_MODE can be used to drive a network status indicator LED. The different modes of status indicator flashing indicate different network statuses. The following tables describe pin definition and logic level changes in different network status.

Table 2-14 Pin Definition of Network Indicator

Pin Name	Pin NO.	I/O	Description	Comment
LED_MODE	70	DO	Indicate the module network registration mode	1.8V power domain

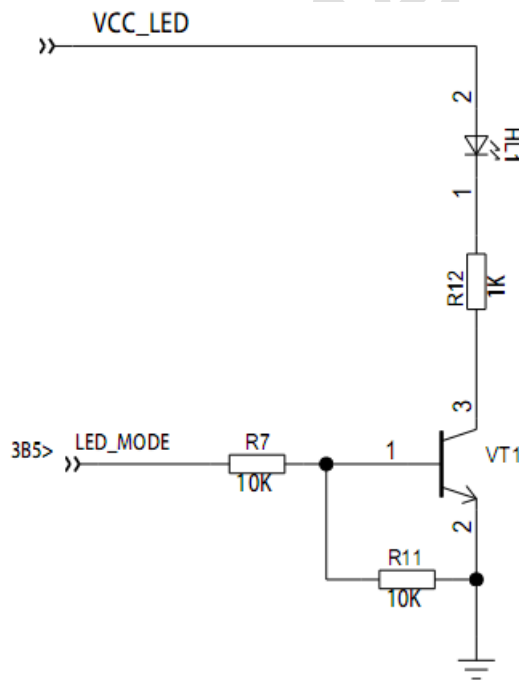
Table 2-15 Working State of the Network Indicator

LED Status	Module status
High level, LED on	Module register to network success
Low level, LED off	Module not register to network(module is in flight mode or power off)
Low level 1s(LED off), High level 1s(LED on)	PDP activated, and get the IP address or Socket established

Figure below is the reference circuit design diagram.

 NOTE:

The resistors R11, R12 and R7 in Figures below are only the recommended value and they need to adjust according to the actual situation.



VT1
TYPE: PMBT3904
MMBT3904LT1G
LMBT3904LT1G

NOTES:

BEFORE DESIGN, PLEASE CHECK IF LED_NET IS A GPIO.
IF IT IS, ITS DESIGN CAN REFER THIS SCH.
IF IT IS NOT, IT CAN NOT USE THIS REF DESIGN.

Figure 2–28 Reference Circuit of the Network Indicator

2.12. POWER_ON/OFF STATUS INDICATOR ON_STATE

PIN69 (ON_STATE) is used to indicate the status of POWER_ON/OFF

Table 2–16 Pin Definition of ON_STATE

Pin Name	Pin NO.	Description
ON_STATE	69	High level: module power on and ready, it can send/receive AT command. Low level: module power off/reset state, and can't send/receive AT command.

The recommend connection mode of this pin are shown as below, you can select one property mode according to you necessary:

Mode 1: this pin is used as GPIO output pin, the MCU can judge the state of module according to the high/low level.

Mode 2: connect this pin to LED to indicate the status of module, the reference circuit you can refer to chapter 2.11.

Mode 3: you can connect this pin to test point when in the development stage.

2.13. ADC INTERFACE

The module provides two ADCs to digitize the analog signal to 10-bit digital data such as battery voltage, temperature and so on. Using AT command "AT+ZADC1?" can read the voltage value on ADC1 pin. Using AT command "AT+ZADC2?" can read the voltage value on ADC2 pin. The read value is expressed in mV. For more details of these AT commands, please refer to document **[AT Command Reference Guide of Module Product ME3630]**.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 2–17 Pin Definition of the ADC

Pin Name	Pin NO.	Description
ADC1	48	General purpose analog to digital converter.
ADC2	47	General purpose analog to digital converter.

The following table describes the characteristic of the ADC function.

Table 2–18 Characteristic of the ADC

Item	Min	Max	Unit
ADC1 voltage range	0.05	4.15	V
ADC2 voltage range	0.05	4.15	V

2.14. WAKEUP_IN SIGNAL

The module provides an AP control interface for communicating with external Application Processor including WAKEUP_IN. The following table shows the pin definition of AP control interface.

Table 2–19 Pin Definition of WAKEUP_IN

Pin Name	Pin NO.	I/O	Description	Comment
WAKEUP_IN	72	DI	Input control signal	1.8V power domain. Pull-down internally. Edge-triggered, Rising edge wake up module; Falling edge modules can enter sleep

When the module needs to be waken up, input a related signal via WAKEUP-IN. The following figure is the signal waveform:

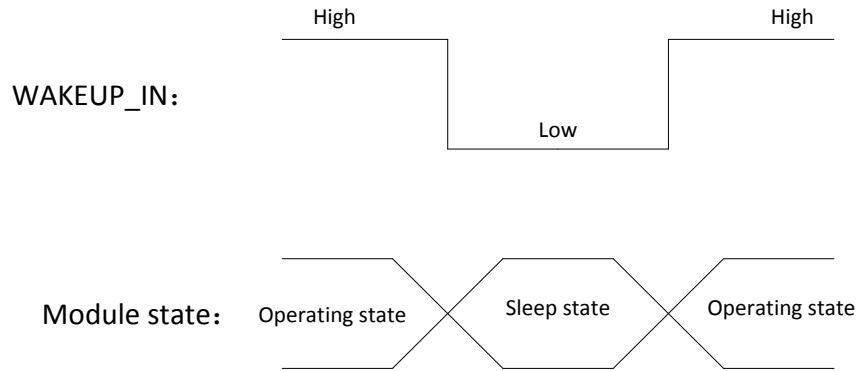


Figure 2-29 WAKEUP_IN input sequence

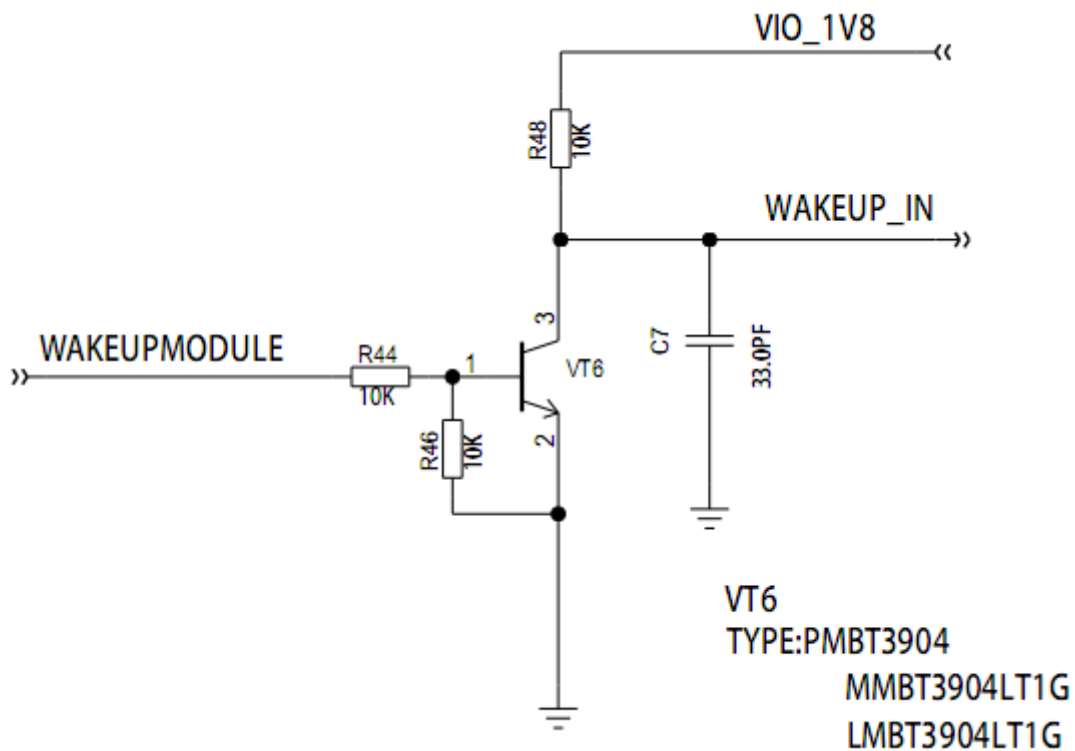


Figure 2-30 Connections of the WAKEUP_IN pin

NOTE:

There is Anti-shake design with WAKEUP_IN pin internal, when pull up or down this pin by external processor, the level must last more than 500ms. WAKEUP_IN Usage scenario you can refer to the document named GOSUNCN ME3630 Module Power Management Design Guide.pdf

2.15. WAKEUP_OUT SIGNAL

The module provides the WAKEUP_OUT pin which is used to wake up the external devices.

Table 2–20 Pin Definition of WAKEUP_OUT

Pin Name	Pin NO.	I/O	Description	Comment
WAKEUP_OUT	71	DO	Output wakeup signal	1.8V power domain The pin output a high-level voltage by default. When a wake-up source (such as new SMS receive, call, network data) arrives, the pin output a low-level-voltage pulse lasting for 1s

For instance, When a wake-up source arrives, the module will output the level shown as the figure below through pin 71.

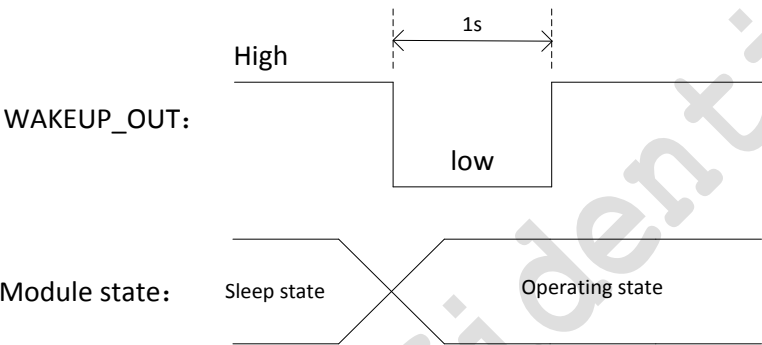


Figure 2–31 The output signal of WAKEUP_OUT

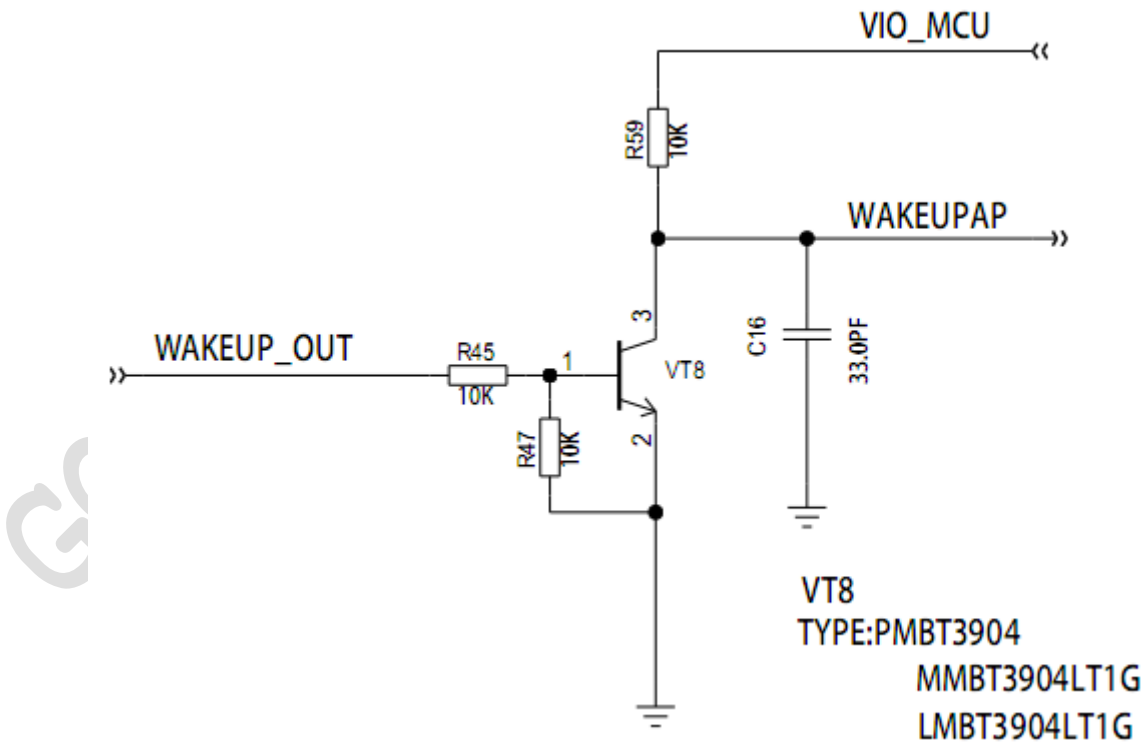


Figure 2–32 Connections of the WAKEUP_OUT pin

**NOTE:**

WAKEUP_OUT Usage scenario you can refer to the document named [GOSUNCN ME3630 Module Power Management Design Guide.pdf](#)

2.16. GPIO INTERFACE

Module provides 5 GPIO pins. The direction and output voltage level of the GPIO can be set by AT command "AT+ZGPIO". The input voltage level of the GPIO can also be read by AT command "AT+ZGPIO". For more details of these AT commands, please refer to document [\[AT Command Reference Guide of Module Product ME3630\]](#).

NOTE: All the GPIO pins are pull-down internally and are input pins in default.

Table 2–21 Pin Definition of GPIO

Pin Name	Pin NO.	I/O	Description	Comment
GPIO1	27	IO	General input/output	1.8V power domain,
GPIO2	28	IO	General input/output	1.8V power domain
GPIO3	29	IO	General input/output	1.8V power domain
GPIO4	30	IO	General input/output	1.8V power domain
GPIO5	65	IO	General input/output	1.8V power domain

3. ANTENNA INTERFACE

ME3630 antenna interface includes a main antenna, an Rx-diversity antenna and a GNSS antenna to improve receiving performance. The antenna interface has an impedance of 50Ω.

3.1. PIN DEFINITION

The main antenna and Rx-diversity antenna pins definition are shown below.

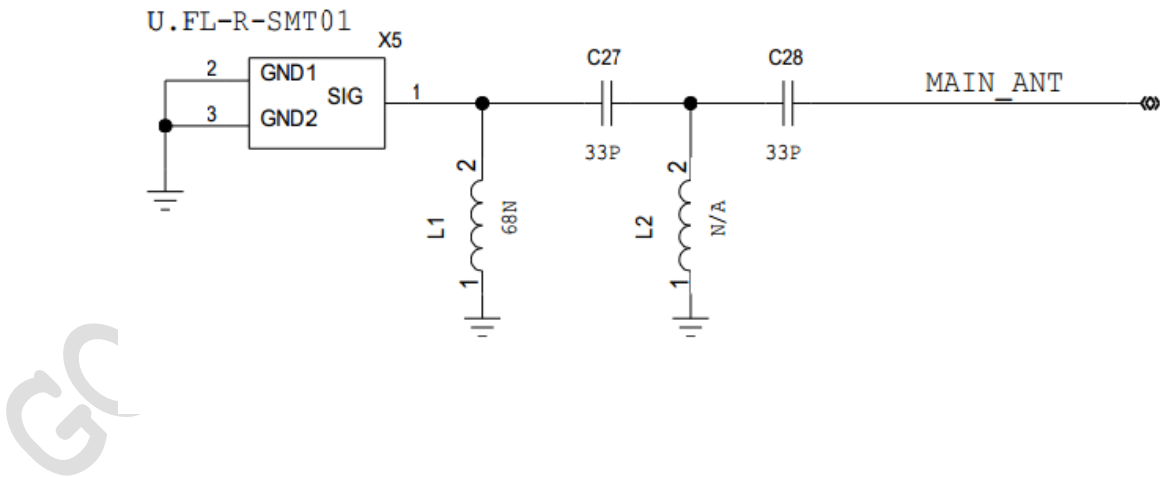
Table 3–1 Pin Definition of Antenna

Pin Name	Pin NO.	I/O	Description	Comment
MAIN_ANT	62	IO	Main antenna	50Ω impedance
DIV_ANT	79	AI	Diversity antenna	50Ω impedance
GNSS_ANT	10	IO	GNSS antenna	50Ω impedance

3.2. REFERENCE DESIGN

The antenna is a sensitive device and its performance is greatly affected by external environments. The radiation performance of the antenna is affected by the module dimensions, antenna position, occupied space size of the antenna, and the grounding of surrounding components of the antenna. Besides, the fixed assembly of the antenna, the wiring of RF cables on the antenna, and the fixed position of the antenna all affect the radiation performance of the antenna too.

The reference design of main antenna and Rx-diversity antenna is shown as below. It should reserve a double-L-type matching circuit for better RF performance, and place these components as close as possible to the module. The capacitors are not mounted by default.



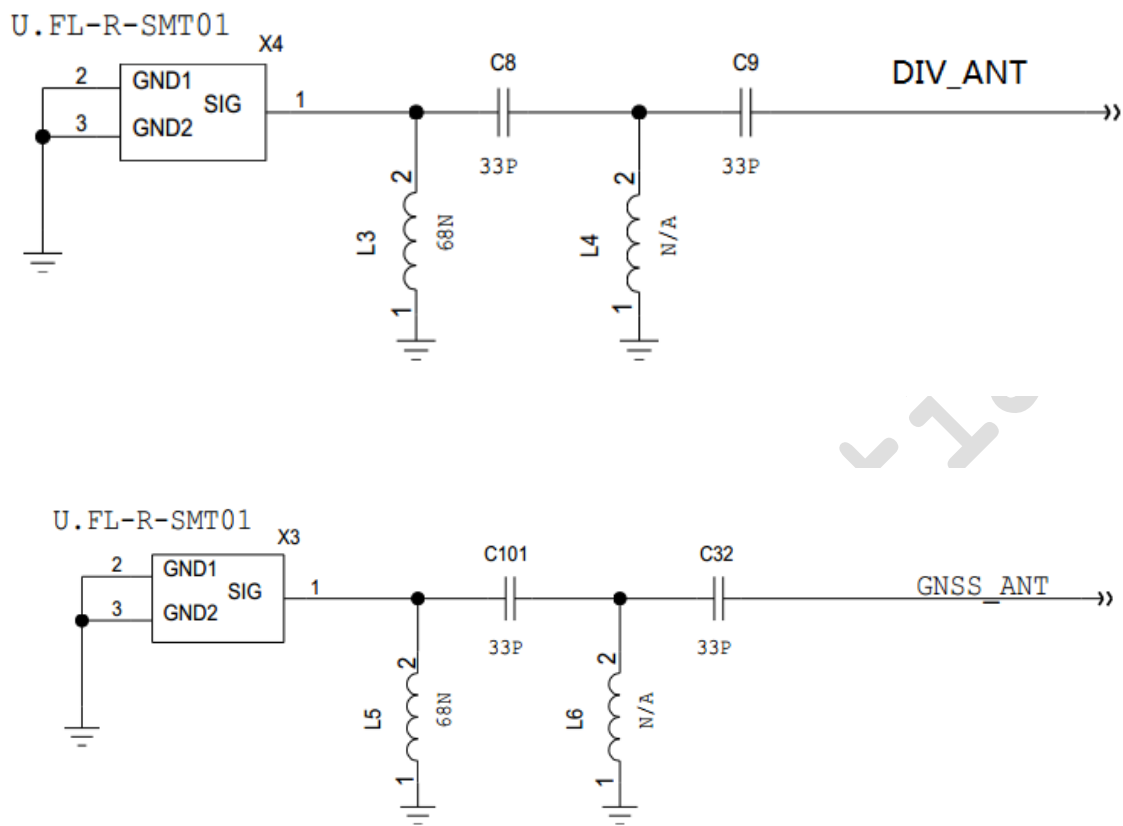


Figure 3-1 Reference Circuit of Antenna Interface

The following picture is the reference of GNSS active antenna, VDD is its power, power supply should be designed by actual requirements.

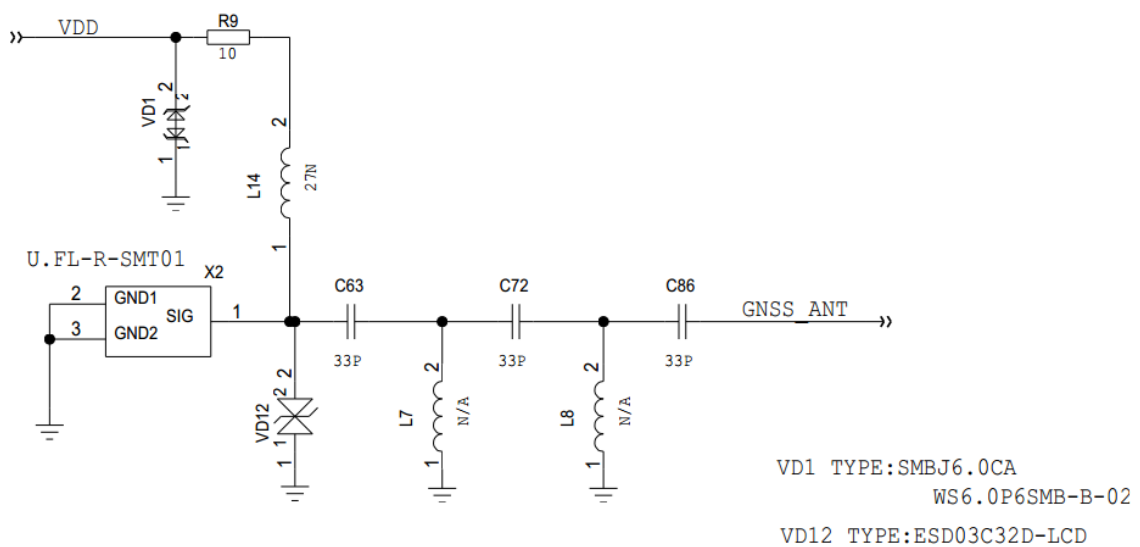


Figure 3-2 Reference Circuit of GNSS Antenna



NOTE:

Keep a proper distance between main and diversity antenna to improve the receiving sensitivity.

3.3. REFERENCE PCB LAYOUT OF ANTENNA

Please follow the following criterion in the process of antenna line PCB layout design:

Make sure that the transmission line's characteristic impedance is 50ohm;

Keep line on the PCB as short as possible, since the antenna line loss shall be less than 0.3 dB;

Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves;

It is wise to surround the PCB transmission line with ground, avoid having other signal tracks facing directly the antenna line track.

Keep at least one layer of the PCB used only for the ground plane; and use this layer as reference ground plane for the transmission line;

- The ground surrounding the antenna line on PCB has to be strictly connected to the main Ground Plane by means of via holes (once per 2mm at least), placed close to the ground edges facing line track;
- Place EMI noisy devices as far as possible from modules antenna line;
- Keep the antenna line far away from the module power supply lines;

3.4. SUGGESTIONS FOR EMC & ESD DESIGN

3.4.1. EMC DESIGN REQUIREMENTS

During the design of the whole device, the user needs to fully consider the EMC problem caused by the signal integrity and power integrity.

During the product design, it is better to separate the module from the mainboard PCB, instead of installing the module on the ground of the mainboard. If they cannot be separated, the module should be far from modules and components that might generate EMI, such as chip and memory, power interface, and data cable interface.

Because the mainboard of PAD, CPE, and Internet laptops does not have a shielding cover, as that of mobile terminals, to shield most circuits to avoid overflow of electromagnetic interference, you can spray conductive paint on the surface on non-antenna areas within the structural components above and below the mainboard, and the conductive paint should be connected to the ground on the mainboard by several points to shield electromagnetic interference.

Besides, data cables of the LCD and the camera might introduce interference signals, which affect the receiving performance of the antenna. Thus, it is necessary to wrap conductive cloth around the two data cables and connected them to the ground.

RF cables of the antenna should be far from modules and components that might generate EMI, such as chip and memory, power interface, and data cable interface. The wiring of RF cables should be close to the ground of the mainboard.

During the layout and wiring of peripheral circuits, for the wiring of power and signal cables, keep a distance of 2 times of the line width, so as to effectively reduce the coupling between signals and keep a clean reflux path for the signal.

During the design of peripheral power circuits, the de-coupled capacitor should be placed closed to the module power PIN, the high-frequency high-speed circuit and the sensitive circuit should be placed far away from the border of PCB. They should better be separated during layout, so as to reduce the interference between them and protect the sensitive signal.

For the circuit or device on the side of system board that might interfere with the module, it should be shielded during design.

3.4.2. ESD DESIGN REQUIREMENTS

Module is embedded on the side of system board, so the user needs to make the ESD protection during design. For the key input/output signal interface, such as the (U)SIM card signal interface, the ESD device should be placed closely for protection. Besides, on the side of main board, the user should reasonably design the structure and PCB layout, guarantee that the metallic shielding shell is fully grounded, so as to leave a smooth discharge channel for ESD.

3.5. TEST METHODS FOR WHOLE-SET ANTENNA OTA

Figure below is the diagram of OTA test system of CTIA. The system is mainly composed of test chamber, high-precision positioning system and its controller, Windows based PC running test software and RF test instruments with automatic test program. The main RF instruments are integrated RF test equipment, Spectrum Analyzer, Network Analyzer.

The radio equipments, Relay Switch Unit and PC with automatic test software are communicated via GPIB interface.

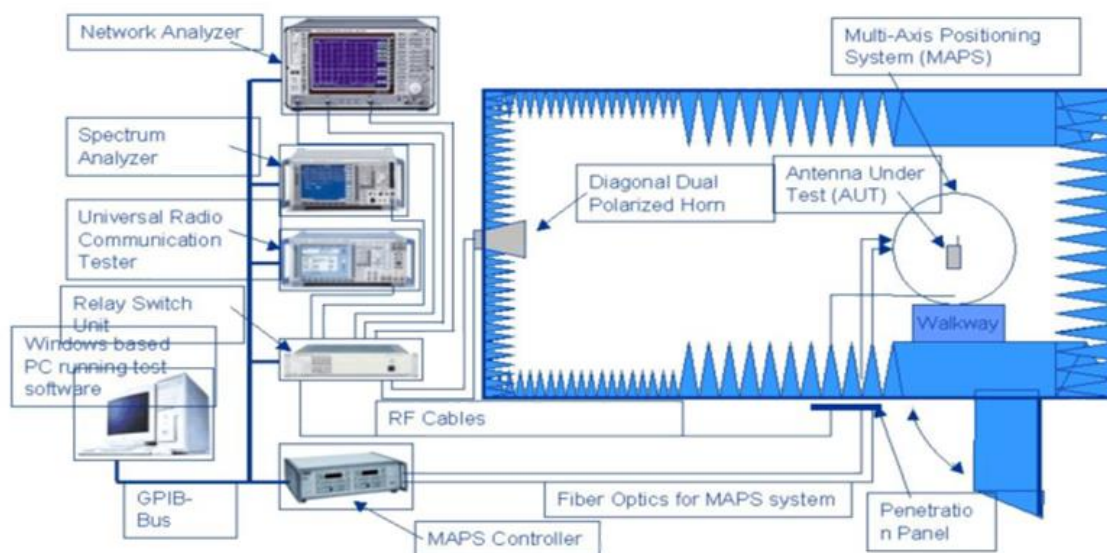


Figure 3-3 The OTA test system of CTIA

4. ELECTRICAL, RELIABILITY AND RADIO CHARACTERISTICS

4.1. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings for power supply and voltage on digital and analog pins of module are listed in the following table:

Table 4-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_BAT	3.4	4.2	V
Peak current of V_BAT	0	2	A
Voltage at digital pin	-0.3	2.1	V
Voltage at ADC1	0.05	4.15	V
Voltage at ADC2	0.05	4.15	V

4.2. OPERATING TEMPERATURE

The operating temperature is listed in the following table.

Table 4-2 Operating Temperature

Parameter	Min	Typ.	Max	Unit
Normal Temperature	-30	25	75	°C
Storage Temperature	-40	/	85	°C
Extreme Operating Temperature	-40°C~ -30°C	/	+75°C~ +85°C	°C

4.3. ELECTROSTATIC DISCHARGE

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 4-3 ESD characteristic

Tested Points	Contact discharge	Air Discharge	Unit
V_BAT	± 5	± 10	kV
All antenna interfaces	±4	± 8	kV
Other interfaces	± 0.5	± 1	kV

4.4. ME3630-U TEST

4.4.1. CURRENT CONSUMPTION

The values of current consumption in different operating mode are shown below.

Table 4-4 Averaged standby DC power consumption [1]

Parameter	Condition	Typical Value	Unit
OFF state	Power down	45	uA
Base Current	Flight Mode[Sleep]	0.9	mA

Table 4-5 Averaged working current [1]

Parameter	Condition	Typical Value	Unit
-----------	-----------	---------------	------

Bandwidth		5MHz	10MHz	15MHz	20MHz	
LTE	LTE FDD Band 2, Pout=23dBm	575	575	620	630	mA
	LTE FDD Band 4, Pout=23dBm	515	530	550	600	mA
	LTE FDD Band 5 ,Pout=23dBm	610	610			mA
	LTE FDD Band 12,Pout=23dBm	620	630			mA
	LTE FDD Band 17, Pout=23dBm	550	600			mA

Table 4-6 Averaged working current [2]

Parameter	Condition	Typical Value	Unit
WCDMA	Band2, Pout=24dBm	532	mA
	Band5, Pout=24dBm	526	mA

4.4.2. RF OUTPUT POWER

The following table shows the RF output power of ME3630 module.

Table 4-7 Conducted RF Output Power

Frequency	Max	Min
LTE FDD Band 2	23±2.7dBm	-39dBm
LTE FDD Band 4	23 ±2.7dBm	-39dBm
LTE FDD Band 5	23 ±2.7dBm	-39dBm
LTE FDD Band 12	23 ±2.7dBm	-39dBm
LTE FDD Band 17	23 ±2.7dBm	-39dBm
WCDMA Band 2	24+1/-3 dBm	-50dBm
WCDMA Band 5	24+1/-3 dBm	-50dBm

4.4.3. RF RECEIVING SENSITIVITY

The following table shows the conducted RF receiving sensitivity typical value of ME3630 module.

Table 4-8 Conducted RF Receiving Sensitivity Typical Value [1]

Band	5 MHz(dBm)	10 MHz(dBm)	20 MHz(dBm)
LTE FDD Band 2	-98 dBm	-95 dBm	-92 dBm
LTE FDD Band 4	-100 dBm	-97 dBm	-94 dBm
LTE FDD Band 5	-98 dBm	-95 dBm	/
LTE FDD Band 12	-97 dBm	-94 dBm	/
LTE FDD Band 17	-97 dBm	-94 dBm	/

Table 4-9 Conducted RF Receiving Sensitivity Typical Value [2]

Band	Sensitivity
WCDMA Band 2	-104.7 dBm
WCDMA Band 5	-104.7 dBm

4.5. GNSS TECHNICAL PARAMETERS

The following table shows the GNSS technical parameters of ME3630 module.

Table 4-10 GNSS Technical Parameters

GNSS (GNSS/GLONASS)	Technical specification
GNSS Frequency	1575.42±1.023 MHz

Tracking sensitivity	-156dbm
Cold-start sensitivity	-144dbm
TTFF (Open Sky)	Hot start: 4s Cold start: 32s
Receiver Type	Qualcomm GNSS Gen8C
GNSS L1 Frequency	1575.42MHz
Update rate	2-4 HZ
GNSS (GNSS/GLONASS) data format	NMEA data protocol/GOSUNCN defined at commands
GNSS (GNSS/GLONASS) Current consumption	65mA
GNSS (GNSS/GLONASS) antenna	Passive/Active antenna

4.6. ME3630-E TEST

4.6.1. CURRENT CONSUMPTION

The values of current consumption in different operating mode are shown below.

Table 4–11 Averaged standby DC power consumption [1]

Parameter	Condition	Typical Value	Unit
Sleep state	Sleep mode (LTE)	2.5	mA
	Sleep mode (WCDMA)	1.8	mA
	Sleep mode (GSM)	2.7	mA

Table 4–12 Averaged working current [1]

Parameter	Condition	Typical Value	Unit
LTE	LTE FDD Band 1, Pout=23dBm	785	mA
	LTE FDD Band 3, Pout=23dBm	731	mA
	LTE FDD Band 7 ,Pout=23dBm	902	mA
	LTE FDD Band 8,Pout=23dBm	671	mA
	LTE FDD Band 20, Pout=23dBm	915	mA

Table 4–13 Averaged working current [2]

Parameter	Condition	Typical Value	Unit
WCDMA	Band1, Pout=24dBm	670	mA
	Band8, Pout=24dBm	558	mA

Table 4–14 Averaged working current [3]

Parameter	Condition	Typical Value	Unit
GSM	Band3, Pout=24dBm	290	mA
	Band8, Pout=24dBm	199	mA

4.6.2. RF OUTPUT POWER

The following table shows the RF output power of ME3630 module.

Table 4–15 Conducted RF Output Power

Frequency	Max	Min
LTE FDD Band 1	23±2.7dBm	-39dBm
LTE FDD Band 3	23 ±2.7dBm	-39dBm
LTE FDD Band 7	23 ±2.7dBm	-39dBm
LTE FDD Band 8	23 ±2.7dBm	-39dBm
LTE FDD Band 20	23 ±2.7dBm	-39dBm
WCDMA Band 1	24+1/-3 dBm	-50dBm
WCDMA Band 8	24+1/-3 dBm	-50dBm
GSM Band3	33+2/-2 dBm	0±5dBm
GSM Band8	30+2/-2 dBm	5±5dBm

4.6.3. RF RECEIVING SENSITIVITY

The following table shows the conducted RF receiving sensitivity typical value of ME3630 module.

Table 4–16 Conducted RF Receiving Sensitivity Typical Value [1]

Band	10 MHz(dBm)	20 MHz(dBm)
LTE FDD Band 1		-94
LTE FDD Band 3		-94.2
LTE FDD Band 7		-92.4
LTE FDD Band 8	-93.7	
LTE FDD Band 20		-96.5

Table 4–17 Conducted RF Receiving Sensitivity Typical Value [2]

Band	Sensitivity
WCDMA Band 1	-109.8 dBm
WCDMA Band 8	-110.2 dBm

Table 4–18 Conducted RF Receiving Sensitivity Typical Value [3]

Band	Sensitivity
GSM Band3	-109 dBm
GSM Band8	-109dBm

4.7. ME3630-J2A TEST

4.7.1. CURRENT CONSUMPTION

The values of current consumption in different operating mode are shown below.

Table 4–19 Averaged standby DC power consumption [1]

Parameter	Condition	Typical Value	Unit
Sleep state	Sleep mode	2.43	mA

Table 4–20 Averaged working current [1]

Parameter	Condition	Typical Value				Unit
Bandwidth		5MHz	10MHz	15MHz	20MHz	
LTE	LTE FDD Band 1, Pout=23dBm				629	mA

LTE FDD Band 3, Pout=23dBm				645	mA
LTE FDD Band 5, Pout=23dBm				523	mA
LTE FDD Band 7, Pout=23dBm				662	
LTE FDD Band 8, Pout=23dBm		512			mA
LTE FDD Band18, Pout=23dBm			597		mA
LTE FDD Band19, Pout=23dBm			617		mA
LTE FDD Band21, Pout=23dBm			586		mA

Table 4-21 Averaged working current [2]

Parameter	Condition	Typical Value	Unit
WCDMA	Band1, Pout=24dBm	514	mA
	Band5, Pout=24dBm	496	mA
	Band6, Pout=24dBm	580	mA
	Band8, Pout=24dBm	502	mA
	Band19, Pout=24dBm	572	mA

4.7.2. RF OUTPUT POWER

The following table shows the RF output power of ME3630 module.

Table 4-22 Conducted RF Output Power

Frequency	Max (uplimit/downlimit)	Min
LTE FDD Band 1	23±2.7dBm	-39dBm
LTE FDD Band 3	23 ±2.7dBm	-39dBm
LTE FDD Band5	23 ±2.7dBm	-39dBm
LTE FDD Band 7	23 ±2.7dBm	-39dBm
LTE FDD Band 8	23 ±2.7dBm	-39dBm
LTE FDD Band18	23 ±2.7dBm	-39dBm
LTE FDD Band 19	23 ±2.7dBm	-39dBm
LTE FDD Band21	23 ±2.7dBm	-39dBm
WCDMA Band 1	24+1/-3 dBm	-50dBm
WCDMA Band5	24+1/-3 dBm	-50dBm
WCDMA Band6	24+1/-3 dBm	-50dBm
WCDMA Band 8	24+1/-3 dBm	-50dBm
WCDMA Band 19	24+1/-3 dBm	-50dBm

4.7.3. RF RECEIVING SENSITIVITY

The following table shows the conducted RF receiving sensitivity typical value of ME3630 module.

Table 4-23 Conducted RF Receiving Sensitivity Typical Value [1]

Band	5 MHz(dBm)	10 MHz(dBm)	15 MHz(dBm)	20 MHz(dBm)
LTE FDD Band 1	-99.6			-94.1
LTE FDD Band 3	-99.8			-94.4
LTE FDD Band5	-101.2	-98.7		

LTE FDD Band 7	-101.5			-92.1
LTE FDD Band 8	-101.2	-98.7		
LTE FDD Band18	-100.9		-96.2	
LTE FDD Band 19	-101		-96.5	
LTE FDD Band 21	-105		-98.9	

Table 4-24 Conducted RF Receiving Sensitivity Typical Value [2]

Band	Sensitivity(dBm)
WCDMA Band 1	-110.6
WCDMA Band5	-110.8
WCDMA Band6	-110.3
WCDMA Band 8	-110.1
WCDMA Band 19	-110.2

4.8. ME3630-A1C TEST

4.8.1. CURRENT CONSUMPTION

The values of current consumption in different operating mode are shown below.

Table 4-25 Averaged standby DC power consumption [1]

Parameter	Condition	Typical Value	Unit
Sleep state	Sleep mode	2.95	mA

Table 4-26 Averaged working current [1]

Parameter	Condition	Typical Value				Unit
Bandwidth		5MHz	10MHz	15MHz	20MHz	
LTE	LTE FDD Band 2, Pout=23dBm		635			mA
	LTE FDD Band 5, Pout=23dBm		595			mA
	LTE FDD Band 7 ,Pout=23dBm		780			mA
	LTE FDD Band 40,Pout=23dBm		455			mA

Table 4-27 Averaged working current [2]

Parameter	Condition	Typical Value	Unit
WCDMA	Band2, Pout=24dBm	485	mA
	Band5, Pout=24dBm	470	mA

Table 4-28 Averaged working current [2]

Parameter	Condition	Typical Value	Unit
GSM	Band2, Pout=33dBm	278	mA
	Band5, Pout=30dBm	245	mA

4.8.2. RF OUTPUT POWER

The following table shows the RF output power of ME3630 module.

Table 4-29 Conducted RF Output Power

Frequency	Max (uplimit/downlimit)	Min
LTE FDD Band 2	23±2.7dBm	-39dBm
LTE FDD Band 5	23 ±2.7dBm	-39dBm
LTE FDD Band7	23 ±2.7dBm	-39dBm
LTE FDD Band 40	23 ±2.7dBm	-39dBm
WCDMA Band 2	24+1/-3 dBm	-50dBm
WCDMA Band5	24+1/-3 dBm	-50dBm
GSM B2	30±2 dBm	0dBm
GSM B5	33±2 dBm	5dBm

4.8.3. RF RECEIVING SENSITIVITY

The following table shows the conducted RF receiving sensitivity typical value of ME3630 module.

Table 4-30 Conducted RF Receiving Sensitivity Typical Value [1]

Band	5 MHz(dBm)	10 MHz(dBm)	15 MHz(dBm)	20 MHz(dBm)
LTE FDD Band 2		-97.2		
LTE FDD Band 5		-98.5		
LTE FDD Band7		-95		
LTE FDD Band 40		-96.3		

Table 4-31 Conducted RF Receiving Sensitivity Typical Value [2]

Band	Sensitivity(dBm)
WCDMA Band 1	-109.5
WCDMA Band5	-110

Table 4-32 Conducted RF Receiving Sensitivity Typical Value [2]

Band	Sensitivity(dBm)
GSM B2	-109
GSM B5	-109

5. MECHANICAL DIMENSIONS

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm.

5.1. MECHANICAL DIMENSIONS OF THE MODULE

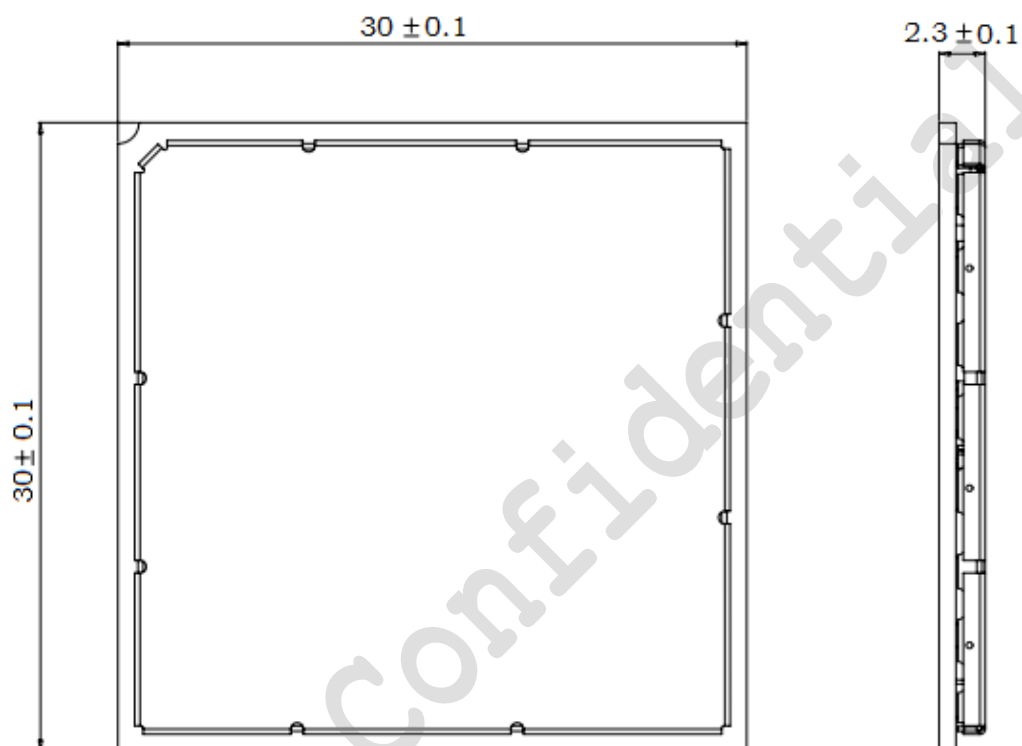


Figure 5-1 ME3630 Top and Side Dimensions

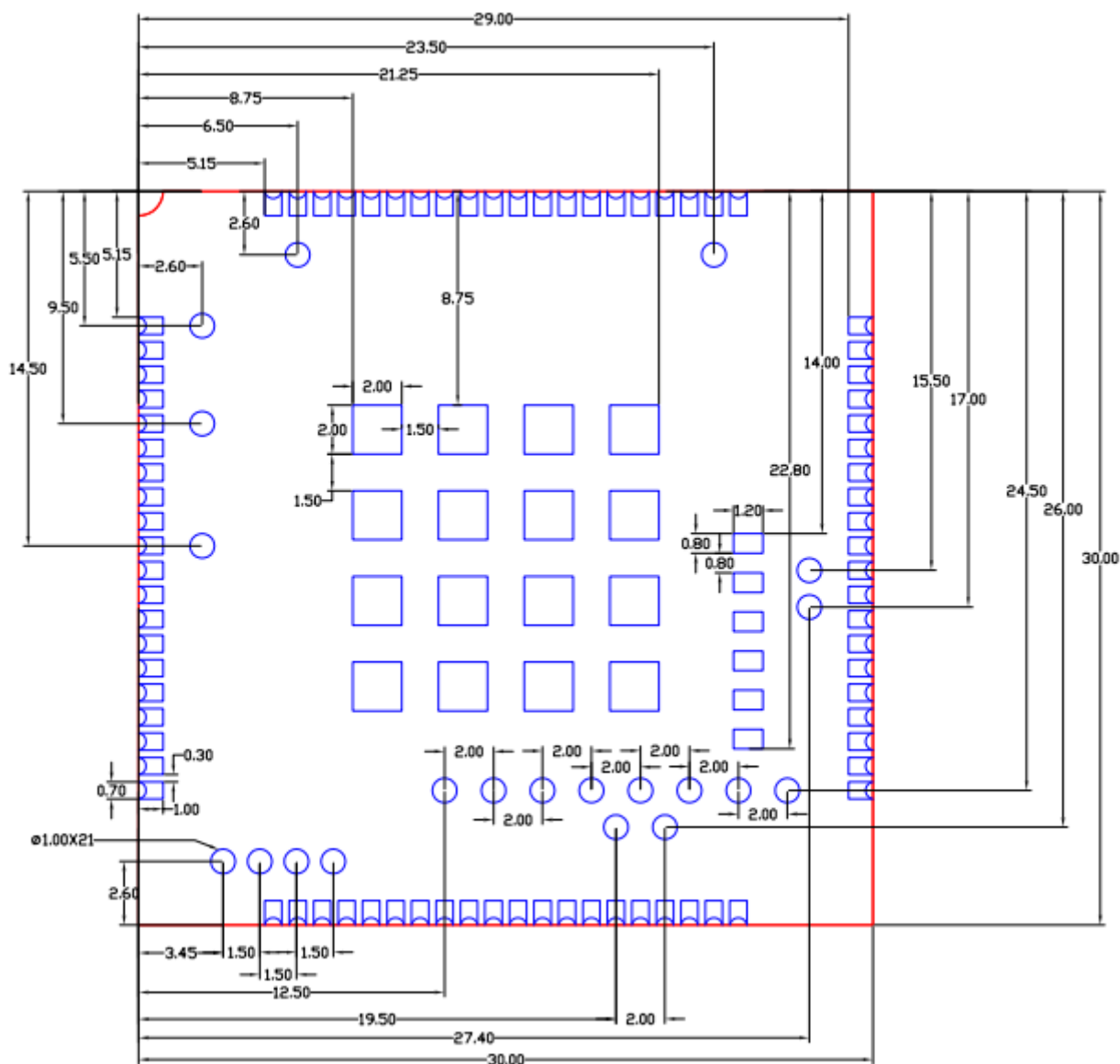


Figure 5-2 ME3630 Bottom Dimensions (perspective view)

Note:

The diameter of test point is 1mm.

5.2. FOOTPRINT OF RECOMMENDATION

6. RELATED TEST & TEST STANDARD

6.1. TESTING REFERENCE

The related tests of MODULE comply with the IEC standard, including the equipment running under high/low temperature, storage under high/low temperature, temperature shock and EMC. Table 6-1 is the list of testing standard, which includes the related testing standards for MODULE.

Table 6-1 Testing Standard



NOTE:

- ☒ **IEC: International Electro technical Commission;**
- ☒ **GB/T: Recommended national standard**

Test Standard	Document Reference
IEC6006826	Environmental testing-Part2.6: Test FC: Sinusoidal Vibration
IEC60068234	Basic environment testing procedures part2.
IEC60068264	Environmental testing-part2-64: Test FH: vibration, broadband random and guidance.
IEC60068214	Environmental testing-part 2-14: Test N: change of temperature
IEC60068229	Basic environmental testing procedures-part2: Test EB and guidance.
IEC6006822	Environmental testing-part2-2: Test B:dry heat
IEC6006821	Environment testing-part2-1: Test A: cold.
GB/T 15844.2	MS telecommunication RF wireless phone-set environment requirement & experimental method – part 4: Strict level of experimental condition
GB/T 2423.17	Basic environment experiment of electronic products-Experiment Ka: Salt mist experiment method
GB/T 2423.5	Basic environment experiment of electronic products-Part2: Experiment method Try Ea & Introduction: Shock
GB/T 2423.11	Basic environment experiment of electronic products-Part2: Experiment method Try Fd: Broad frequency band random vibration (General requirement)
TIA/EIA 603 3.3.5	TIA Standard-part3-5:Shock Stability

6.2. DESCRIPTION OF TESTING ENVIRONMENT

The working temperature range of MODULE is divided into the normal working temperature range and the extreme working temperature range. Under the normal working temperature range, the testing result of RF complies with the requirements of 3GPP specifications, and its function is normal. Under the extreme temperature range, the RF index basically complies with the 3GPP specifications, and the quality of data communication is affected to a certain extent, but its normal function is not affected. MODULE has passed the EMC test. Table 6-2 is the requirement for the testing environment, and Table 6-3 lists out the instruments and devices that might be used during the test.



WARNING:

Table 6-2 lists the extreme working conditions for the Module. Using the Module beyond these conditions may result in permanent damage to the module.

Table 6-2 Testing Environment

Working Condition	Min Temperature	Max Temperature	Remark
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Normal working condition	-30°C	75°C	All the indexes are good.
Extreme working condition	-40~ -30°C	75~85°C	Some indexes become poorer.
Storage	-40°C	85°C	Storage environment of module

Table 6-3 Testing Instrument & Device

Testing Item	Instrument & Device
RF test	Comprehensive testing device
	RF cable
	Tower antenna
	Microwave darkroom
High/Low-temperature running & storage test	High/Low-temperature experimental box
Temperature shock test	Temperature shock experimental box
Vibration test	Vibration console

6.3. RELIABILITY TESTING ENVIRONMENT

The reliability test includes the vibration test, high/low-temperature running, high/low-temperature storage and temperature shock experiment test. Refer to **Table 6-4** for the specific parameters.

Table 6-4 Reliability Features

Test Item	Test Condition	Test Standard
Random vibration	Frequency range: 5-20Hz, PSD: 1.0m2/s3 Frequency range: 20-200Hz, -3dB/oct 3 axis, 1 hour for each axis	IEC 68-2-6
Temperature shock	Low temperature: -40°C ± 2°C High temperature: +80°C ± 2°C Temperature changing period: less than 30s Test duration: 2 hours Cycle: 10	IEC 68-2-14 Na
High-temperature running	Normal high temperature: 75 °C Extreme high temperature: 85°C Duration: 24 hours	GOSUNCN standard
Low-temperature running	Normal low temperature: -30°C Extreme low temperature: -40°C Duration: 24 hours	GOSUNCN standard
High temperature & high humidity	Temperature: +60°C Humidity: 95% Duration: 48 hours	GOSUNCN standard
High temperature storage	Temperature: 85°C Duration: 24 hours	IEC 68-2-1 Ab
Low temperature storage	Temperature: -40°C Duration: 24 hours	IEC 68-2-2 Bb

7. SMT PROCESS AND BAKING GUIDE

This chapter describes module's storage, PAD design, SMT process parameters, baking requirements, etc., and it is applicable for the process guide to second-level assembly of LCC encapsulation module.

7.1. STORAGE REQUIREMENTS

Storage conditions: temperature<40℃, relative humidity<90% (RH), 12 months weld ability guaranteed under this circumstances of excellent sealing package.

The Moisture sensitivity level for all modules is level 3 (Conforming to IPC/JEDEC J-STD-020). After opening the package, mount within 168 hours under the environment conditions of temperature<30℃, relative humidity<60% (RH). If it doesn't meet the above requirements, perform the baking process. See the baking parameters in Table below:

Table 7-1 Baking parameters

Temperature	Baking conditions	Baking time	Remarks
125± 5℃	Moisture: ≤60%RH	8 hours	The accumulated baking time must be less than 96 hours
45± 5℃	Moisture: ≤5%RH	192 hours	

The product's transportation, storage and processing must conform to IPC/JEDEC J-STD-033

When in the process of PAD designing of module, refer to IPC-SM-782A and the chapter 6.2 below.

7.2. MODULE PLAINNESS STANDARD

Plainness of the module is required to be less than 0.15mm.

Measurement method: put the module on the marble plane, use the feeler gage to measure the gap width at the position of maximum warp, and do not exert force on the module during the measurement.

7.3. PROCESS ROUTING SELECTION

The modules are manufactured with the lead-free process and meet the ROHS requirements, therefore it's recommended to follow the lead-free manufacturing process upon the selection of process routing for module board and main board.

7.3.1. SOLDER PASTE SELECTION

The solder pastes with metal particle TYPE3 and TYPE4 can fulfill the welding requirements. It is accordingly recommended to use the no-clean solder paste. If the solder paste which needs cleaning is used, we cannot guarantee the components on the module board could withstand the washing of the cleaning solvents. This might cause the functional problems of such components and affect the appearance of the module. During the printing process, make sure the solder paste's thickness at the position of module's PAD is within 0.18mm~0.20mm.

7.3.2. DESIGN OF MODULE PAD'S STEEL MESH OPENING ON MAIN BOARD

The thickness of the steel mesh on main board is selected according to the encapsulation type of components on the main board. Pay attention to the following requirements:

Make sure to design the module PAD on main board according to chapter 5.

The thickness of steel mesh is 0.15mm or 0.18mm, but the thickness at the position of module pad can be increased to 0.18~0.20mm or the thickness of steel mesh is directly 0.18mm~0.20mm on main board.

Requirements on the thickness of solder paste: control the thickness between 0.18mm and 0.20mm.

See the LCC module PAD's steel mesh opening in the following table:

Table 7-2 LCC module PAD's steel mesh opening

Module PAD GAP (G)=Center Distance (e) – PAD width (X)	Steel mesh opening
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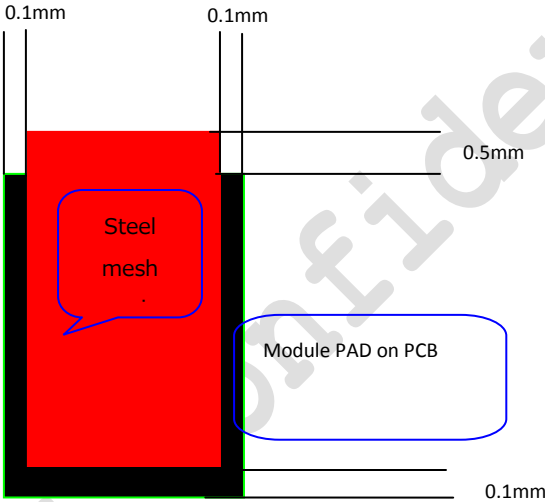
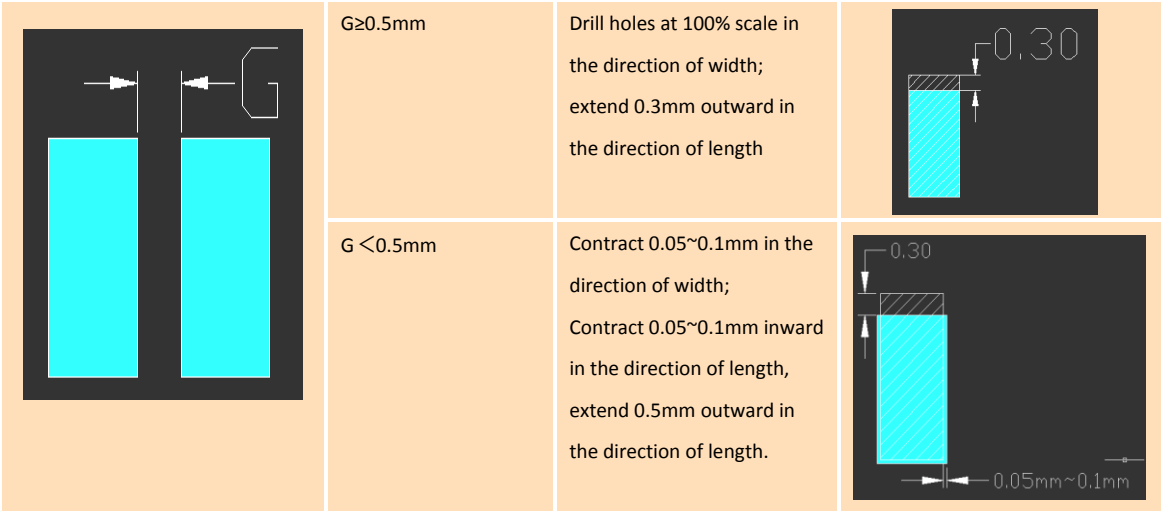


Figure 7-1 Module Board's Steel Mesh Diagram

7.3.3. MODULE BOARD'S SMT PROCESS

1) SMT Tape Reel:

The tape reels, which are suitable for SMT, have been made for most GOSUNCN modules. If the module has provided the tape reel itself and meets the SMT requirements, customers can directly use it for module SMT.



Figure 7-2 Material Module Pallet

 NOTE:

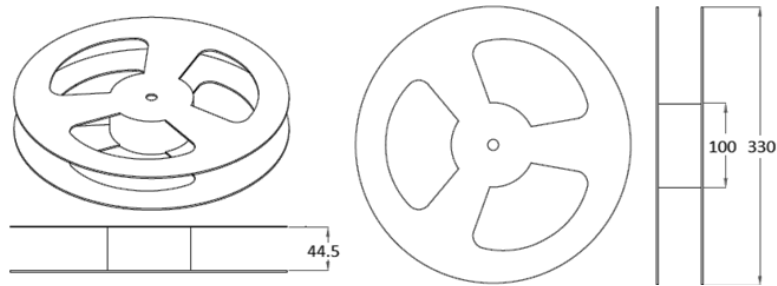
Figure7-2 is just for reference, it doesn't represent the actual Material Module Tape Reel.

Otherwise, customers need make a loading tool similar to the tape reel. Customers can take out the module from the packaging box, put them into the tape according to the sequence and direction, and then start SMT.

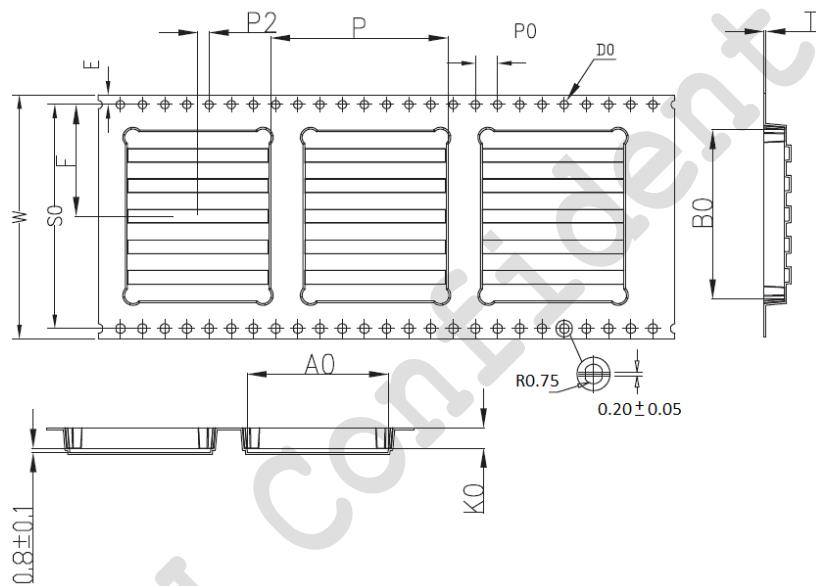
2) Tape Reel Dimension (unit: mm):

The following picture is the tape reel specific dimension for your reference:

A: Whole dimension:



B: Detailed dimension:



ITEM	W	A0	B0	K0	K1	P	F	E	S0	D0	D1	P0	P2	T
DIM	44.00 $\pm$ 0.30	25.50 $\pm$ 0.15	30.50 $\pm$ 0.15	3.80 $\pm$ 0.15	0.00 $\pm$ 0.00	32.00 $\pm$ 0.18	20.20 $\pm$ 0.15	1.75 $\pm$ 0.10	40.40 $\pm$ 0.18	1.50 $\pm$ 0.08	0.00 $\pm$ 0.00	4.00 $\pm$ 0.10	2.00 $\pm$ 0.10	0.35 $\pm$ 0.05
ALTERNATE														

Figure 7-3 Tape Reel Dimension

3) Mounting Pressure:

In order to ensure a good contact between the module and the solder paste on main board, the pressure of placing the module board on main board should be 2-5N according to our experiences. Different modules have different numbers of pads, therefore the pressure selected are different. Customers can select proper pressure based on their own situations to suppress the module paste as little as possible, in order to avoid the surface tension of the solder paste melts too much to drag the module during reflow.

7.3.4. MODULE SOLDERING REFLOW CURVE

Module soldering furnace temperature curve is:

- Peak value: 245 $\pm$ 0/-5 $^{\circ}$ C
- $\geq 217^{\circ}$ C: 30 $\sim$ 60S
- 150 $\sim$ 200 $^{\circ}$ C: 60 $\sim$ 120S
- Temperature rise slope: <3 $^{\circ}$ C/S

- Temperature drop rate: $-2 \sim -4^{\circ}\text{C}/\text{s}$

**NOTE:**

The test board of furnace temperature must be the main board with the module board mounted on, and there must be testing points at the position of module board.

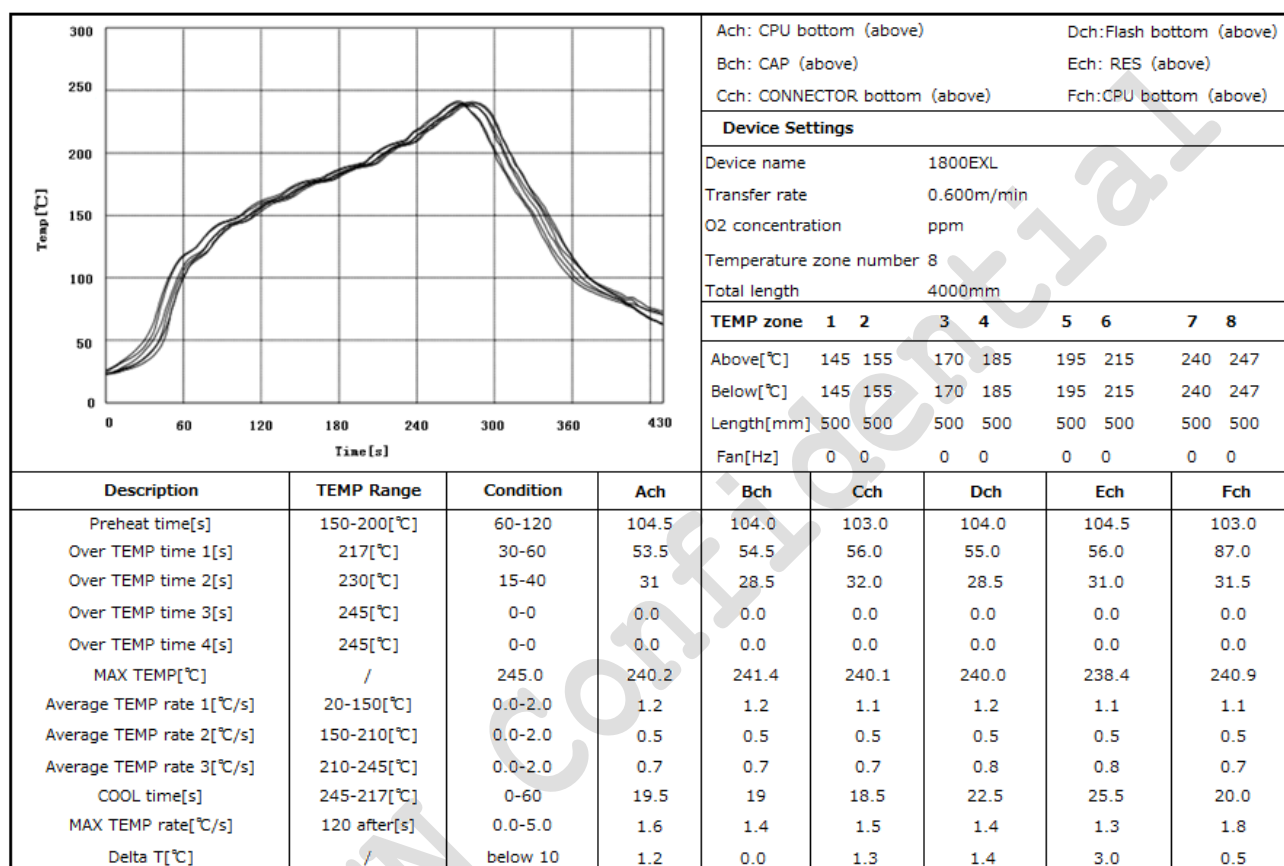


Figure 7-4 Module Furnace Temperature Curve Reference Diagram

7.3.5. REFLOW METHOD

If the main board used by customers is a double-sided board, it is recommended to mount the module board at the second time. In addition, it is preferable for the main board to reflow on the mesh belt when mounting at the first time and the second time. If such failure is caused by any special reason, the fixture should be also used to make such main board reflow on the track so as to avoid the deformation of PCB during the reflow process.

7.3.6. MAINTENANCE OF DEFECTS

If poor welding occurs to the module board and main board, e.g., pseudo soldering of the module board and main board, the welder can directly use the soldering iron to repair welding according to the factory's normal welding parameters.

7.4. MODULE'S BAKING REQUIREMENTS

The module must be baked prior to the second reflow.

7.4.1. MODULE'S BAKING ENVIRONMENT

The operators must wear dust-free finger cots and anti-static wrist strap under the lead-free and good static-resistant environment. Refer to the following environment requirements:

! WARNING:

Lead-free



Anti-static



Caution



Wear a wrist strap



Wear finger cots

The product's transportation, storage and processing must conform to IPC/JEDEC J-STD-033.

7.4.2. BAKING DEVICE AND OPERATION PROCEDURE

Baking device: Any oven where the temperature can rise up to 125°C or above.

Precautions regarding baking: during the baking process, the modules should be put in the high-temperature resistant pallet flatly and slightly to avoid the collisions and frictions between the modules. During the baking process, do not overlay the modules directly because it might cause damage to the module's chipset.

7.4.3. MODULE BAKING CONDITIONS

See the baking parameters in **Table 7-1**.

8. OEM/INTEGRATORS INSTALLATION MANUAL**Important Notice to OEM integrators**

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: 2APNR-ME3630"

The FCC ID ID can be used only when all FCC compliance requirements are met.

Antenna Installation

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed for use with this device is 5 dBi.
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.