DKL 1613_V.1 User Manual

Single Chip 2.4GHz Module

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FEATURES

- Low Power
  - 16mA TX at 0dBm output power
  - 15mA RX at 1Mbps air data rate
  - 2uA in power down
- Low Cost BOM
  - Few external components Four Capacitors, One crystal oscillator
- High Performance
  - Excellent Receiver sensitivity
    -88dBm@1Mbps
    -93dBm@250Kbps
  - Programmable Output Power Up to 13dBm

APPLICATIONS

- TV and STB remote controls
- Wireless Mouse and keyboard
- Toys and wireless audio
- Wireless gamepads
- Active RFID
- Smart home automation

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GENERAL DESCRIPTION

The XN297L is a single chip 2.4GHz transceiver, designed for operation in the worldwide ISM frequency band at 2.400~2.483GHz. The XN297L integrates radio frequency (RF) transmitter and receiver, frequency synthesizer, crystal oscillator, baseband GFSK modem, and other function blocks. The XN297L supports multiple networks and communication with ACK. TX power, frequency channel, and data rate can be set by SPI.

1Mbps, 250kbps optional data rate	Up to 8Mbps SPI interface rate
Support 32 and 64 bytes payload length	Compact 20-pin 3×3mm QFN package
Support ±20ppm 16MHz crystal	Operating voltage is 2.2V~3.3V
GFSK Modulation	Support automatic reply and automatic retransmission
Support RSSI detector	Support Data whitening and CRC

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1 Electrical Characteristics

Table1 XN297L Electrical Characteristics

Symbol	Condition at VCC = 3V±5%, T=25℃	Parameter			Unit
		Min	Typ	Max	
ICC	Sleep		2		uA
	Standby I		30		uA
	Standby III		650		uA
	Standby Ⅱ		780		uA
	TX at -35dBm output power		9		mA
	TX at -20dBm output power		9.5		mA
	TX at 0dBm output power		16		mA
	TX at 2dBm output power		19		mA
	TX at 8dBm output power		30		mA
	TX at 13dBm output power		66		mA
	RX at 1Mbps		15.5		mA
	RX at 250kbps		15		mA
General RF					
f_{OP}	Operating frequency	2400		2483	MHz
PLL_{res}	PLL Programming resolution		1		MHz
f_{XTAL}	Crystal frequency		16		MHz
DR	Data rate	0.25		1	Mbps
Δf_{250K}	Frequency deviation at 250kbps		125		KHz
Δf_{1M}	Frequency deviation at 1Mbps		160	250	KHz
FCH_{250K}	Channel spacing at 250Kbps		1		MHz
FCH_{1M}	Channel spacing at 1Mbps		1		MHz
Transmitter					
PRF	Typical output power	2	8	13	dBm
$PRFC$	Output Power Range	-35		13	dBm
$PBW2$	20dB Bandwidth for Modulated Carrier at 1Mbps		1		MHz

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$PBW3$	20dB Bandwidth for Modulated Carrier at 250Kbps		500		KHz
Receiver					
RX_{max}	Maximum received signal at <0.1% BER		0		dBm
$RXSENS2$	Sensitivity (0.1%BER) @1Mbps		-87		dBm
$RXSENS3$	Sensitivity (0.1%BER) @250Kbps		-93		dBm
C/I_{CO}	C/I Co-channel (@1Mbps)		10		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		1		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-18		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-23		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I		-32		dBc
C/I_{6TH}	6th Adjacent Channel Selectivity C/I		-35		dBc
C/I_{CO}	C/I Co-channel (@250Kbps)		2		dBc
C/I_{1ST}	1st Adjacent Channel Selectivity C/I		-8		dBc
C/I_{2ND}	2nd Adjacent Channel Selectivity C/I		-18		dBc
C/I_{3RD}	3rd Adjacent Channel Selectivity C/I		-24		dBc
C/I_{4TH}	4th Adjacent Channel Selectivity C/I		-28		dBc
C/I_{5TH}	5th Adjacent Channel Selectivity C/I		-32		dBc
C/I_{6TH}	6th Adjacent Channel Selectivity C/I		-35		dBc
Operating conditions					
VDD	Supply voltage	2.2	3	3.3	V
VSS	Ground		0		V
V_{OH}	Output high level voltage	VDD-0.3		VDD	V
V_{OL}	Output low level voltage	VSS		VSS+0.3	V
V_{IH}	Input high level voltage	2.0	3	3.6	V

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V_{IL}	Input low level voltage	VSS		VSS+0.3	V

* Note: In the channels, such as 2416 and 2432 MHz, integer times of 16MHz crystal, receiver sensitivity degrades about 2dB; and modulation quality of the emission signal (EVM) falls by 10%.

* Note: In 250Kbps mode, payload length should not be more than 16 bytes, because of frequency drift in open-loop transmitting mode.

2 Absolute Maximum Ratings

Table 2 XN297L Absolute Maximum Ratings

Symbol	Condition	Parameter			Unit
		Min	Typ	Max	
maximum ratings					
V_{DD}	Supply voltage	-0.3		3.6	V
V_I	Input voltage	-0.3		5	V
V_O	Output voltage	VSS		VDD	
Pd	Total Power Dissipation (TA=-40℃~85℃)			300	mW
T_{OP}	Operating Temperature	-40		85	℃
T_{STG}	Storage Temperature	-40		125	℃

* Note: Exceeding one or more of the limiting values may cause permanent damage to XN297L.
* Caution: Electrostatic sensitive device, comply with protection rules when operating.

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5 Operational Modes

This chapter describes XN297L' s all kinds of working modes, and is used to control the chip into the working mode method. XN297L' s state machine is controlled by chip internal registers configuration values and external signal pin.

5.1 State Diagram

Table 4 shows six kinds of work modes, which gives the corresponding mode of control registers and FIFO registers.

Table 4 Control BIT and Function Description

MODE	PWR_DN	STB1	STB3	STB2	RX	TX
CONTROL BIT						
PWR_UP	0	1	1	1	1	1
EN_PM	0	0	1	1	1	1
CE	0	0	0	1	1	1
PRIM_RX	X	X	X	0	1	0
FUNCTION DESCRIPTION						
SPI operation	√	√	√	√	√	√
Keep register value	√	√	√	√	√	√
Crystal oscillator work	X	√	√	√	√	√
Crystal oscillator output	X	X	X	√	√	√
Main power management work	X	X	√	√	√	√
TX work	X	X	X	X	X	√
RX work	X	X	X	X	√	X

5.2 State Diagram

Figure 3 shows XN297L' s working state diagram, giving six working modes between jump XN297L in VDD is larger than 2.2V to work properly into sleeping

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mode, the MCU can be sent via SPI configuration commands and CE pin into the other five states.

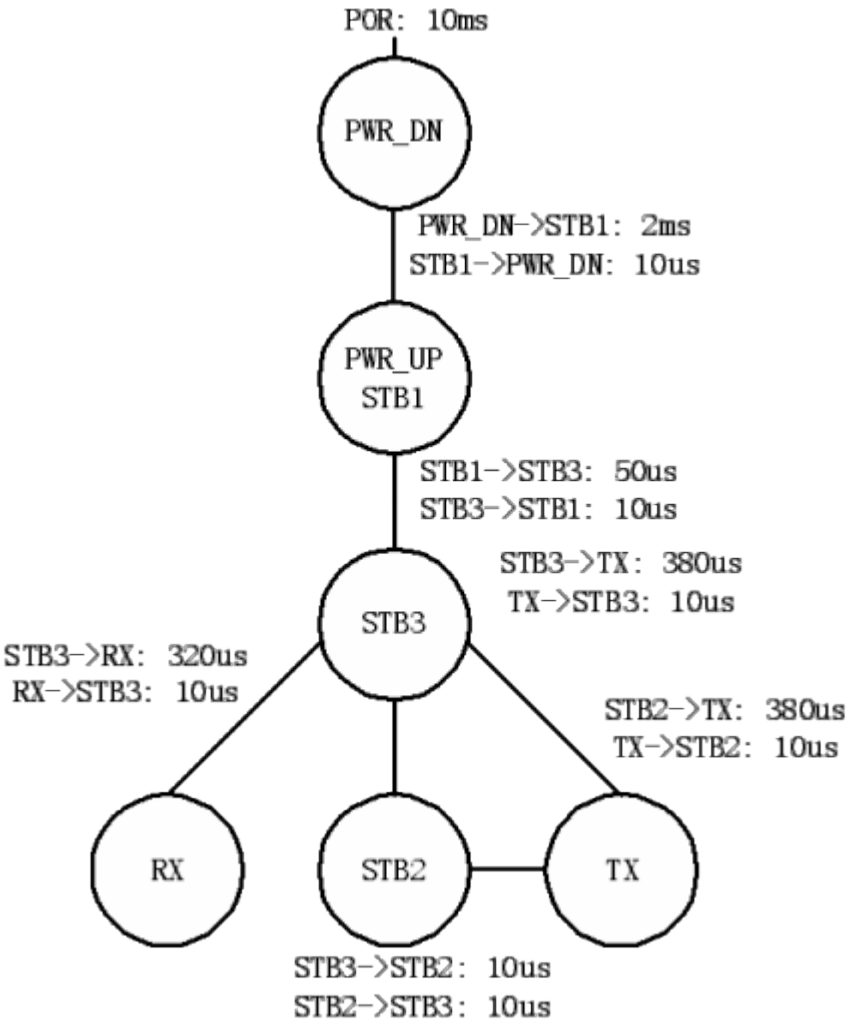

Figure3 State Diagram

5.3 IRQ PIN

When the status register TX_DS RX_DR or MAX_RT is 1, reporting and the corresponding interrupt enable bit is 0, IRQ pins interrupts trigger. The MCU writes 1 to the corresponding interrupt source, clear the interrupt. IRQ pins interrupt trigger can be blocked or enabled, report by setting the interrupt enable bit is 1, ban IRQ pins interrupt triggered.

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6 DATA FIFO

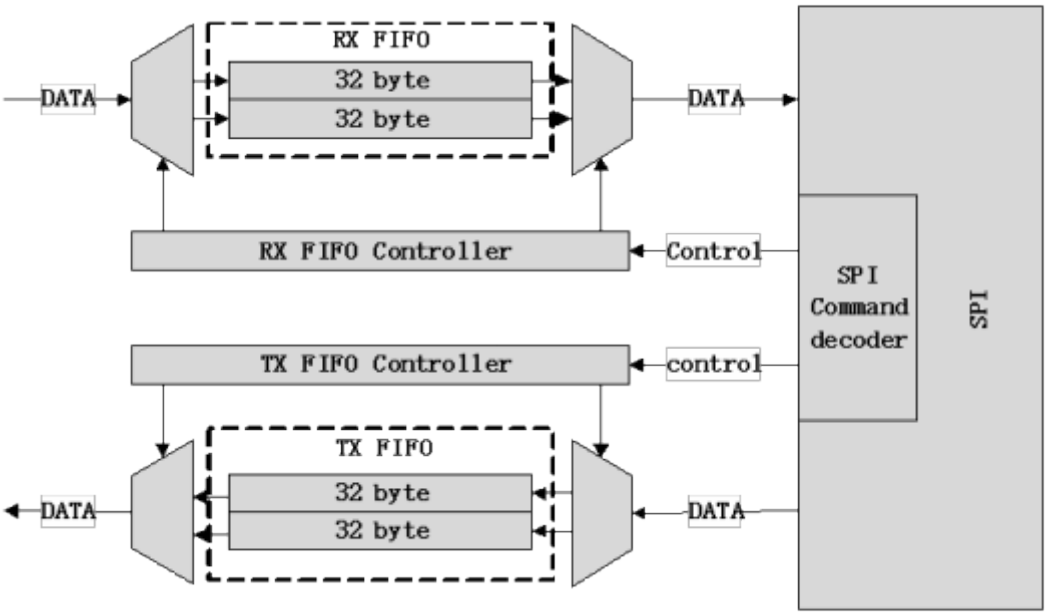

Figure 4 FIFO Block Diagram

The XN297L contains TX FIFO and RX FIFO. It is sent via SPI read/write command. It writes TX FIFO in TX mode by W_TX_PAYLOAD and W_TX_NO_ACK instructions. If MAX_RT interruption, data will be cleared in the TX FIFO. It reads PAYLOAD in RX FIFO in receiving mode by R_RX_PAYLOAD, and it reads the length of the PAYLOAD by R_RX_PL_WID instruction. FIFO_STATUS register indicates FIFO states.

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7 SPI CONTROL

The XN297L is controlled by SPI port for read and write registers, and command. The XN297L is a slave terminal, SPI transfer rate depends on the MCU interface speed, and the maximum data transfer rate is 8 Mbps.

SPI interface is a standard SPI interface are shown in table 5, you can use the general I/O for MCU simulation SPI interface. CSN pin to 0, SPI interface instructions to be performed. From 1 to 0 a CSN pin changes execute one instruction. After the change from 1 to 0 CSN pin can be read by MISO status register contents.

Table 5 SPI Port

PIN	I/O DIRECTION	FUNCTION DESCRIPTION
CSN	Input	SPI Chip Select
SCK	Input	Clock
MOSI	Input	Serial Data Input
MISO	Output	Serial Data Output

7.1 SPI Commands

Table 6 SPI Command Format

<Command word: MSBit to LSBit (one byte)>

<Data bytes: LSByte to MSByte, MSBit in each byte first>

COMMAND	COMMAND WORD (BINARY)	DATA BYTES	OPERATION
R_REGISTER	000A AAAA	1 to 5	Read registers. AAAAA =5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5	Write registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32/64	Read RX-payload. A read operation starts at byte 0. Payload is deleted from RX

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			FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32/64	Write TX-payload. A write operation starts at byte 0. Used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode
REUSE_TX_PL	1110 0011	0	Used for a PTX device, reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH_TX is executed.
ACTIVATE DEACTIVE	0101 0000	1	This write command followed by data 0x73 activates the following features: • R_RX_PL_WID • W_TX_PAYLOAD_NOACK • W_ACK_PAYLOAD This is executable in power down or standby modes only. This write command followed by data 0x8C deactivates the following features:
R_RX_PL_WID	0110 0000	0	Read RX-payload width for the top, R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	1010 1PPP	1 to 32/64	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum two ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle.
W_TX_PAYLOAD_NO ACK	1011 0000	1 to 32/64	Write Payload to be transmitted, used in TX mode. Disable auto ACK on this packet.
CE_FSPI_ON	1111 1101	1	SPI command CE internal logic 1, use the command followed by the data 0x00

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CE_FSPI_OFF	1111 1100	1	SPI command CE internal logic 0, use the command followed by the data 0x00
RST_FSPI_HOLD RST_FSPI_RELS	0101 0011	1	With the command followed by data 0x5A, makes the XN297L into reset and maintain With the command followed by data 0xA5, release the XN297 reset and start to work normally
NOP	1111 1111	0	No Operation.

The R_REGISTER and W_REGISTER commands can operate on single or multi-byte registers. When accessing multi-byte registers, firstly read or write the MSBit of LSByte. Terminate the writing before all bytes in a multi-byte register are written, then it leaves the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register.

7.2 SPI Timing

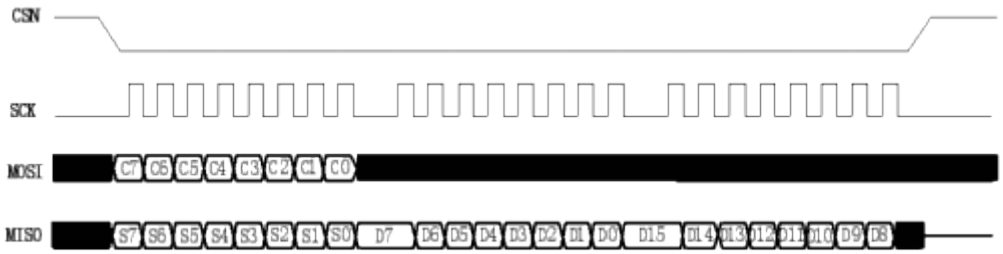

Figure 5 SPI read operation

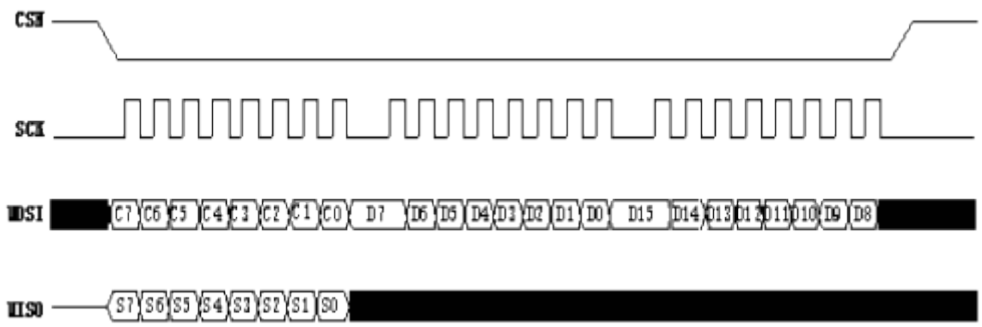

Figure 6 SPI Write Operation

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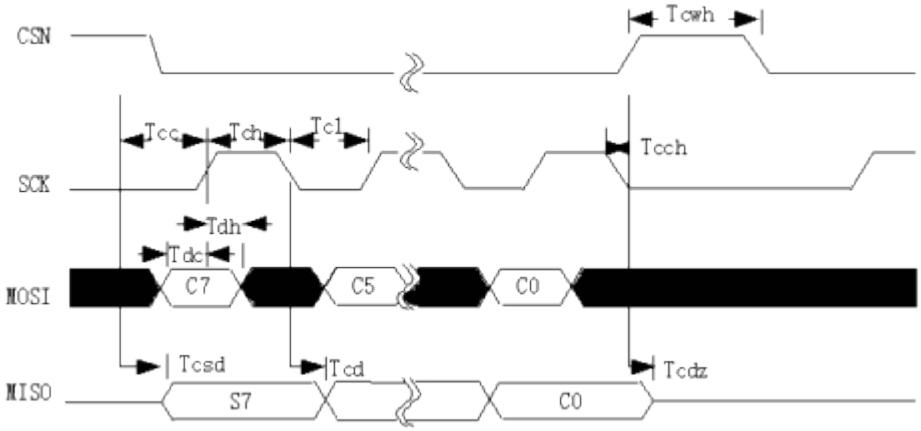

Figure 7 SPI NOP Timing Diagram

8 Control Registers

You can configure and control XN297L by accessing the register map through the SPI by using read and write commands.

Table 9 Control Registers(The Registers with * need to be modified)

ADDRESS (HEX)	REGISTERS	BIT	DEFAULT VALUE AFTER RESTORATION	READ AND WRITE	EXPLANATION
00*	CONFIG				Configuration Register
	EN_PM	7	0	R/W	Into STB3 mode (When PWR_UP=1) 1: Into STB3 mode 0: Into STB1 mode (When changing to other modes, wait more than 50us in STB3 mode)
	MASK_RX_DR	6	0	R/W	The interrupt when receiving data successfully reports to the Enable_bit. 1: Interrupt not reflected on the IRQ pin. 0: Reflect RX_DR as active low interrupt on the IRQ pin.
	MASK_TX_DS	5	0	R/W	The interrupt when sending data successfully reports to the Enable_bit. 1: interrupt not reflect on the IRQ pin. 0: reflect TX_DS as active low interrupt on the IRQ pin.

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	MASK_MAX_RT	4	0	R/W	The interrupt reaching maximum transmission times when sending data unsuccessfully reports to the Enable_bit 1: interrupt not reflected on the IRQ pin. 0: reflect MAX_RT as active low interrupt on the IRQ pin.
	EN_CRC	3	1	R/W	Enable CRC.. 1: CRC enable , 2byte 0: CRC disable and verification.
	N/A	2	0	R/W	Retain and set to 1
	PWR_UP	1	0	R/W	The Enable_bit 1: POWER_UP 0: POWER_DOWN
	PRIM_RX	0	0	R/W	RX/TX Control 1: PRX 0: PTX
01	EN_AA Enhanced Burst				The auto_response enable of reception channel （If the EN_AA of receiving terminal isn’t 0X00, the system is set to enhancement mode）
	Reserved	7:6	00	R/W	Only 00 allowed
	ENAA_P5	5	0	R/W	Enable pipe5 auto-response
	ENAA_P4	4	0	R/W	Enable pipe4 auto-response
	ENAA_P3	3	0	R/W	Enable pipe3 auto-response
	ENAA_P2	2	0	R/W	Enable pipe2 auto-response
	ENAA_P1	1	0	R/W	Enable pipe1 auto-response
	ENAA_P0	0	1	R/W	Enable pipe0 auto-response
02	EN_RXADDR				Enable reception channel
	Reserved	7:6	00	R/W	Only 00 allowed
	ERX_P5	5	0	R/W	enable data pipe 5
	ERX_P4	4	0	R/W	enable data pipe 4
	ERX_P3	3	0	R/W	enable data pipe 3
	ERX_P2	2	0	R/W	enable data pipe 2
	ERX_P1	1	0	R/W	enable data pipe 1
	ERX_P0	0	1	R/W	enable data pipe 0
03	SETUP_AW				Setup of Address Widths
	Reserved	7:2	000000	R/W	Only 000000 allowed
	AW	1:0	11	R/W	RX/TX Address Field Width 00: Illegal 01: 3 bytes 10: 4 bytes 11: 5 bytes LSByte is used if address width is below 5 bytes

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04	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmit Delay 0000 :250μs 0001 :500μs 0010 :750μs …… 1111: 4000μs
	ARC	3:0	0011	R/W	Auto retransmit count 0000: re-transmit disabled 0001 ~ 1111: Enhance mode 0001: up to 1 re-transmit on fail of AA 0010: up to 2 re-transmit on fail of AA …… 1111: up to 15 re-transmit on fail of AA
05	RF_CH				RF channel
	Reserved	7	0	R/W	Only 0 allowed
	RF_CH	6:0	1001110	R/W	Set the frequency channel RF_CH + 2400
06*	RF_SETUP				RF Setup Register
	RF_DR	7:6	00	R/W	Data rate 01: retain 00: 1Mbps 11: 250kbps 10: retain
	PA_GC	5:3	111	R/W	The output amplitude of PA' s driver can adjust the transmitting power. 111: The amplitude is high. …… 000: The amplitude is low.
	PA_PWR	2:0	111	R/W	The output amplitude of PA' s output power can adjust the transmitting power. 111: The output power is high. …… 000: The output power is low.
07	STATUS				Status Registers
	Reserved	7	0	R/W	Only 0 allowed
	RX_DR	6	0	R/W	Data ready RX FIFO interrupt. Asserted when new data arrives RX FIFO. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data sent TX FIFO interrupt. Asserted when packet transmitted on TX. if AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.

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	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable furtuer communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO. 000-101: pipe number 110: Not Used 111: RX_FIFO empty
	TX_FULL	0	0	R	TX FIFO full flag 1: TX FIFO full 0: Available locations in TX FIFO
08	OBSERVE_TX				Transmit Observe Register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
09*	DATAOUT				Data read registers (DATAOUT_SEL=0)
	ANADATA7	7	0	R	The 3rd bit of receiver' s RSSI value(the maxmum bit)(for test)
	ANADATA6	6	0	R	The 2nd bit of receiver' s RSSI value(the maxmum bit)(for test)
	ANADATA5	5	0	R	The 1st bit of receiver' s RSSI value(the maxmum bit)(for test)
	ANADATA4	4	0	R	The 0 bit of receiver' s RSSI value(the maxmum bit)(for test)
	ANADATA3	3	0	R	The 3rd bit of receiver' s receiving packet(the maximum bit)
	ANADATA2	2	0	R	The 2nd bit of receiver' s receiving packet
	ANADATA1	1	0	R	The 1st bit of receiver' s receiving packet
	ANADATA0	0	0	R	The 0 bit of receiver' s receiving packet
0A	RX_ADDR_P0	39:0	0xE7E7E 7E7E7	R/W	Receive address data pipe 0.5 bytes maximum length.(LSByte is written first. Write the number of bytes defined by SETUP_AW)
0B	RX_ADDR_P1	39:0	0xC2C2C 2C2C2	R/W	Receive address data pipe 1 bytes maximum length.(LSByte is written first. Write the number of bytes defined by SETUP_AW)

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0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2 bytes maximum length. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3 bytes maximum length. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4 bytes maximum length. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5 bytes maximum length. Only LSB. MSBytes is equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E 7E7E7	R/W	Transmit address. Used for a PTX device only.(LSByte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX Device with enhanced shockburst enabled.
11	RX_PW_P0				The data length of data pipe 0’ s RX payload
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P0	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 0(1 to 32/64 bytes) 0 pipe not used 1=1 byte …… 32/64=32/64 bytes
12	RX_PW_P1				The data length of data pipe 1’ s RX payload.
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P1	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 1(1 to 32/64 bytes) 0 pipe not used 1=1 byte …… 32/64=32/64 bytes
13	RX_PW_P2				The data length of data pipe 2’ s RX payload.
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P2	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 2(1 to 32/64 bytes) 0 pipe not used 1=1 byte …… 32/64 = 32/64 bytes

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14	RX_PW_P3				The data length of data pipe 3’ s RX payload.
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P3	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 3(1 to 32/64 bytes) 0 pipe not used 1=1 byte …… 32/64 = 32/64 bytes
15	RX_PW_P4				The data length of data pipe 4’ s RX payload.
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P4	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 4(1 to 32/64 bytes) 0 pipe not used 1=1 byte …… 32/64 = 32/64 bytes
16	RX_PW_P5				The data length of data pipe 5’ s RX payload.
	Reserved	7	0	R/W	Only 0 allowed
	RX_PW_P5	6:0	0000000	R/W	Number of bytes in RX payload in data pipe 5(1 to 32/64 bytes) 0 pipe not used 1=1 byte …… 32/64 = 32/64 bytes
17*	FIFO_STATUS				FIFO Status Register
	N/A	7	0	R	retain
	TX_REUSE	6	0	R	Reuse last transmitted data packet if set high. the packet repeatedly retransmitted as long as CE is high. TX_REUSE is set by the SPI command REUSE_TX_PL , and is reset by the SPI commands W_TX_PAYLOAD_NOACK、DEACTIVATE 、FLUSH TX.。
	TX_FULL	5	0	R	TX FIFO full flag. 1:TX FIFO full. 0:Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1:TX FIFO empty. 0:Data in TX FIFO.
	N/A	3	0	R	Retain
	N/A	2	0	R	Retain
	RX_FULL	1	0	R	RX FIFO full flag. 1: RX FIFO full.

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					0: Available locations in RX FIFO.
	RX_EMPTY	0	1	R	RX FIFO empty flag. 1: RX FIFO empty. 0: Data in RX FIFO.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 2-32 bytes or 1-64 bytes FIFO.
N/A	RX_PLD	255:0	X	R	Written by separate SPI command RX data payload register 2-32 bytes or 1-64 bytes FIFO. All RX channels share the same FIFO.
19*	DEMOD_CAL	7:0			Modulation-demodulation parameter registers(configure by program)
	CHIP	7	0	R/W	Configure if the chip is in test mode 1: Enter test mode 0: Quit test mode
	CARR	6:5	00	R/W	Configure if the chip is in carrier test mode 11: Enter single carrier mode and the chip is set to 1 00: Quit single carrier mode
	GAUS_CAL	4:1	0111	R/W	The amplitude adjustment of signal from Gaussian filter to DAC, which is one of the key factor to decide the value of transmitting modulation frequency offset. 1111: The amplitude is high .... 1000: The amplitude is average .... 0000: The amplitude is high
	Scramble_en	0	1	R/W	If the scrambler function is enabled. Open scrambler function can make a vernacular operation to the ready-to-sent data, which reduces the length of 1 & the length of 0. enable srambler function needs a same configuration in both of the receiving and transmitting terminals. 1: Enable scrambler function 0: Turn off scrambler function
1A*	RF_CAL2	47:0			Add RF registers(Default value is recommended)
	N/A	47:46	01	R/W	Retain
	BW_500K	45	0	R/W	The bandwidth of filter 0: Narrow bandwidth

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					1: Wide bandwidth
	GC_500K	44	1	R/W	The gain of filter 0：Low gain 1：High gain
	IRQ_inv_sel	43	0	R/W	If the output of IRQ(EN_PA)is inverse. 1：The output is inverse 0：The output isn’t inverse
	CLKOUT_Z_sel	42	0	R/W	If the pin of CLKOUT is output in high resistance. 1：CLKOUT PIN is output in high resistance. 0：CLKOUT PIN is as output.
	CE_L_sel	41	0	R/W	If the pins of CE weak pulldown resistors are enabled. 1：The pins of CE weak pulldown resistors are enabled 0：The pins of CE weak pulldown resistors aren’t enabled.
	MISO_Z_sel	40	0	R/W	If the pins of MISO is output in high resistance. 1：MISO PIN is output in high resistance. 0：MISO PIN is output.
	IRQ_Z_sel	39	0	R/W	If the pins of IRQ are output in high resistance. 1：IRQ PIN is output in high resistance. 0：IRQ PIN is output.
	PA_ramp_sel	38:37	01	R/W	Choose the way of PA ramp up 00：No ramp up 01：4us ramp each step 10：ramp begins with half current 11：2us ramp each step
	OSC_IC	36	1	R/W	Choose OSC’s exciting current 1：×1 0：×0.75
	CLK_SEL	35:34	10	R/W	Choose the output frequency of internal crystal signal. 00: 16MHz 01: 8MHz 10: 4MHz 11: 2MHz
	EN_STBII_RX2TX	33	1	R/W	PTX terminal enters standby-II mode briefly when converting from transmitting mode into receiving mode. The other LDOs except DVDD are powered down once when entering standy-II mode.

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					1: Enable 0: Disenable
	BPF_CTRL_BW	32	0	R/W	Choose the bandwidth of 1dB receiving intermediate-frequency filter. 1: ×1 0: ×0.85
	BPF_CTRL_GAIN	31	1	R/W	Choose the gain of receiving intermediate-frequency filter. 1: 5dB 0: 19dB
	VCOBUF_IC	30:29	01	R/W	Choose the driving MIXH current. 00: 600uA 01: 800uA 10: 1mA 11: 1.2mA
	VCO_CT	28:27	01	R/W	Choose the VCO load capacitors. 00: There are few capacitors, and the frequency of VCO is high. 11: There are more capacitors, and the frequency of VCO is low.
	CAL_VREF_SEL	26	1	R/W	Choose the autocorrection reference voltage. 1: 1.15V 0: 1.25V
	SPI_CAL_EN	25	0	R/W	The process of VCO single trigger autocorrection when this bit is configured from 0 to 1. In addition, when changing work channel and entering sending and receiving state, the VCO can also be autocorrected.
	PREAMP_CTM	24:22	011	R/W	Choose the driver load capacitors. 000: 399fF 100: 171fF 111: 0fF
	DA_LPF_BW	21	1	R/W	Choose the DAC's filtering bandwidth. 1: Wide bandwidth 0: Narrow bandwidth
	RX_CTM	20:19	01	R/W	Choose LNA's resonant frequency(load capacitors) 00: 2.45GHz 01: 2.52GHz 10: 2.59GHz 11: 2.66GHz
	RCCAL_EN	18	1	R/W	Enable Receiving bandwidth filter's autocorrenction function. 1: Enable

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					0: Disable
	EN_VCO_CAL	17	1	R/W	The bit to enable VCO's autocorrenction 1: Enable 0: Disable
	PRE_BC	16:14	100	R/W	Choose the prescaler's direct current 000: ×1 001&010: ×1.5 100&011: ×2 101&110: ×2.5 111: ×3
	VCO_CODE_IN	13:10	1000	R/W	Choose VCO's frequency band Only enable when EN_VCO_CAL is 0 1111: High frequency band 0000: Low frequency band
	RCCAL_IN	9:4	010100	R/W	Configure the receiving band-pass filter's intermediate frequency correction. Only available when RCCAL_EN is 0 111111: Low intermediate mid-frequency 000000: High intermediate mid-frequency
	CPSEL	3:2	01	R/W	Configure the PLL charge pump's current. RX TX 00: 26uA 26uA 01: 26uA 52uA 10: 52uA 78uA 11: 78uA 104uA
	DATAOUT_SEL	1	0	R/W	Configure the data-read bit to 0.
	RSSI_SEL	0	1	R/W	Choose RSSI signal sampling points. 1: The RSSI signal goes through filter. 0: The RSSI signal doesn't go through filter.
1B	DEM_CAL2	23:0			Replenish and demodulate reference registers(use default value in general)
	PIN	23:21	000	R/W	Configure the output PIN after the chip entering test mode(MISO pin/IRQ pin) 000(the chip is 0) operation mode data output and interrupt output 000(the chip is 1) testing sensitivity mode demodulate data and clock output 110(the chip is 1) testing receiving mode output in 2 different ways in

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					both limit I and Q
	EN_RX	20	0	R/W	If both the receiving channel and PLL are open at the same time 1: Open at the same time 0: Open at the different time
	DELAY1	19	0	R/W	If the PLL’s open loop is enabled, the enabling of PLL’s open loop state can test the transmitting of carrier drift 1: PLL open loop enables. 0: PLL open loop is controlled by state machine.
	DELAY0	18	0	R/W	If the demodulator can add the initial offset, the demodulator which doesn’t add the initial offset can test the receiving sensitivity. 1: do not add initial offset. 0: add initial offset, counteract the error code in receiving state.
	TH1	17	1	R/W	In standby-II mode, if the LDO(except DVDD’s LDO) is enabled, in test mode, the bit is configured to 1 when testing transmitting single carrier and receiving sensitivity. 1: Enable 0: Dienable
	PTH	16:13	0110	R/W	Configure the threshold value of receiver digital demodulator’s lead code. The threshold of 24bits lead code=PTH+16 1000: 24bits 0110: 22bits 0000: 16bits
	SYNC_SEL	12	1	R/W	Receiver digital demodulator’s 4 times sampling, calculate some relevant data. 1: 3bit 0: 2bit
	DECOD_INV	11	1	R/W	If reverse the lead code, configure to 1 in general. Enable this function in the both the receiving and transmitting terminals. 1: Do not reverse in bits 0: Reverse in bits
	GAIN1	10:7	1110	R/W	Adjust the central amplitude of the loop reference waveform, configure to 1110
	GAIN2	6:1	000101	R/W	Adjust the speed of the loop reference waveform, configure to 000101

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	AGGRESSIVE	0	1	R/W	Choose the speed of demodulator' s code unit rate synchronizaton 1: Adjust in large steps, the speed is fast 0: Adjust in small steps, the speed is low
1C	DYNPD				Enable dynamic PAYLOAD' s length
	Reserved	7:6	00	R/W	Only 00 allowed
	DPL_P5	5	0	R/W	Enable the length of PIPE 5' s dynamic PAYLOAD(EN_DPL and ENAA_P5 are needed)
	DPL_P4	4	0	R/W	Enable the length of PIPE 4' s dynamic PAYLOAD(EN_DPL and ENAA_P4 are needed)
	DPL_P3	3	0	R/W	Enable the length of PIPE 3' s dynamic PAYLOAD(EN_DPL and ENAA_P3 are needed)
	DPL_P2	2	0	R/W	Enable the length of PIPE 2' s dynamic PAYLOAD(EN_DPL and ENAA_P2 are needed)
	DPL_P1	1	0	R/W	Enable the length of PIPE 1' s dynamic PAYLOAD(EN_DPL and ENAA_P1 are needed)
	DPL_P0	0	0	R/W	Enable the length of PIPE 0' s dynamic PAYLOAD(EN_DPL and ENAA_P0 are needed)
1D*	FEATURE	7:0		R/W	Feature registers
	Reserved	7	0	R/W	Only 00 allowed
	MUX_PA_IRQ	6	0	R/W	Choose IRQ signal output or EN_PA signal output to PIN 0 : IRQ signal output to PIN 1 : EN_PA signal output to PIN
	CE_SEL	5	0	R/W	Open CE with command mode 0 : CE is controlled by pins 1 : CE is controlled by command
	DATA_LEN_SEL	4:3	00	R/W	Choose the length of data 11: 64byte (512bit) mode 00: 32byte (256bit) mode
	EN_DPL	2	0	R/W	Enable the length of dynamic PAYLOAD
	EN_ACK_PAY	1	0	R/W	Enable ACK which has PAYLOAD
	EN_NOACK	0	0	R/W	enable W_TX_PAYLOAD_NOACK command
1E*	RF_CAL	23:0		R/W	RF parameter registers(configure by programme)
	EN_CLK_OUT	23	0	R/W	Choose the external crystal signal 1: clock signal output to CLK_OUT' s

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					PAD 2: no output
	DA_VREF_MB	22:20	101	R/W	The reference voltage of DAC's comparison circuit If the reference voltage is high, the DAC's output range is high 111: positive reference voltage is high 000: positive reference voltage is low
	DA_VREF_LB	19:17	110	R/W	The reference voltage of DAC's comparison circuit If the reference voltage is high, the DAC's output range is high 111: negative reference voltage is high 000: negative reference voltage is low
	DA_LPF_CTRL	16	1	R/W	The command bit of DAC's output range 1: output range×0.8 0: output range×0.5倍
	RSSI_EN	15	0	R/W	Enable RSSI 1: RSSI enable 0: RSSI disenable
	RSSI_Gain_CTR	14:13	01	R/W	The bit to choose RSSI's signal gain attenuation. 00: no attenuation 01: -6dB 10: -12dB 11: -18dB
	MIXL_GC	12	1	R/W	Choose the gain of receiving MIXL 1: 14dB 0: 8dB
	PA_BC	11:10	11	R/W	Choose PA's output direct current 00: ×1 01: ×2 10: ×3 11: ×4
	LNA_GC	9:8	11	R/W	Choose LNA's gain 11: 17dB 10: 11dB 01: 5.4dB 00: -0.4dB
	VCO_BIAS	7:5	111	R/W	Configure VCO's current 000: 900uA 001: 1050uA 010: 1200uA 011: 1350uA 100: 1500uA 101: 1650uA 110: 1800uA

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					111: 1950uA
	RES_SEL	4:3	10		Choose chip offset current load 00: 26kR 01: 24kR 10: 22kR 11: 20kR
	LNA_HCURR	2	1	R/W	Configure LNA’s high current 1: high current 0: low current
	MIXL_BC	1	1	R/W	Choose MIXL’s receiving current 1: ×1 0: ×0.5
	IB_BPF_TRIM	0	0	R/W	Choose receiving bandwidth filter’s current 1: ×1 0: ×0.5
1F*	BB_CAL	7:0 15:8 23:16 31:24 39:32		R/W	Digital base bandwidth registers(default value in general)
	Reserved	39:32	01000110	R/W	Only 0X01000110 allowed
	INVERTER	31	1	R/W	If reverse the data before entering RX_block 1: reverse 0: retain
	DAC_MODE	30	0	R/W	If dac_out[5:0] need to be reversed , dac_out[5:0] is DAC’s output terminal 1:dac_out[5:0]<= [0:5] 0:dac_out[5:0]<= [5:0]
	DAC_BASAL	29:24	011100	R/W	Pre-sending DAC’s initial value
	TRX_TIME	23:21	011	R/W	The internal from PLL’s open-loop state to data-sending state, the length of time is: TRX_TIME×8+7.5 , the unit is us
	EX_PA_TIME	20:16	00111	R/W	The internal of Transmitting PLL enabling PA, the length of time is: EX_PA_TIME×16 , the unit is us
	TX_SETUP_TIME	15:11	01101	R/W	The internal of Transmitting PLL enabling PA, the length of time is: TX_SETUP_TIME×16 , the unit is us
	RX_SETUP_TIME	10:6	10100	R/W	The stable time of RF RX circuit : RX_SETUP_TIME×16 , the unit is us
	RX_ACK_TIME	5:0	001010	R/W	The longest time of PTX converting to receiving mode, it’s a failure when time is out.

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					The length of time in 1Mbps mode: RX_ACK_TIME×32 , the unit is us The length of time in 250kbps mode: RX_ACK_TIME×128 , the unit is us

9 Packet Format Description

9.1 Packet Format for Normal Burst

Table 7 Packet Format for Normal Burst

Preamble (3 byte)	Address (3~5 byte)	Payload (1~32/64 byte)	CRC (0/2 byte)

It can choose Address and Payload part to scramble, according to scrambler configuration bits.

9.2 Packet Format for Enhanced Burst

Table 8 Packet Format for Enhanced Burst

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			Payload (1~32/64 byte)	CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)		

It can choose Address, Package control field and Payload part to scramble, according to scrambler configuration bits.

9.3 Packet Format for Enhanced Burst ACK

Table 9 Packet Format for Enhanced Burst ACK

Preamble (3 byte)	Address (3~5 byte)	Package control field (10bit)			CRC (0/2 byte)
		Payload length (7bit)	PID (2bit)	NO_ACK (1bit)	

It can choose Address, Package control field to scramble, according to scrambler

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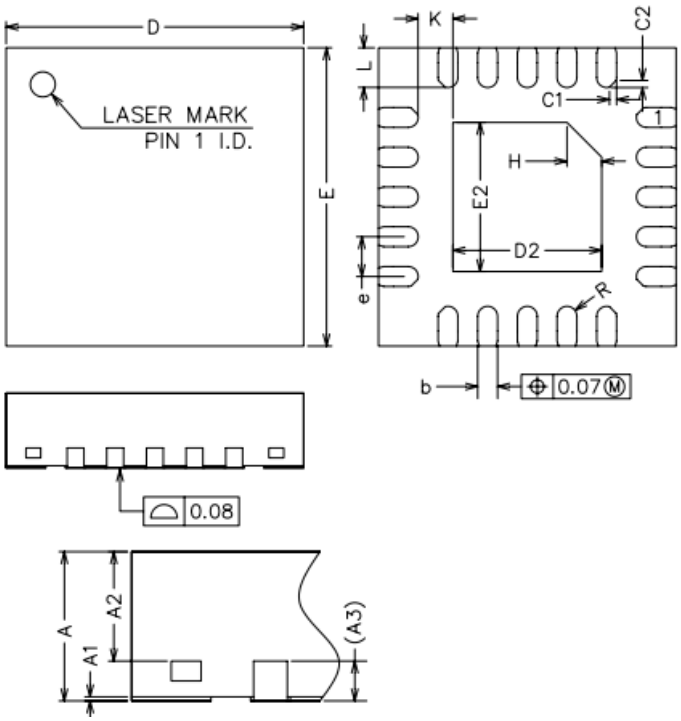
11 Package Size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.40	1.50	1.60
E2	1.40	1.50	1.60
e	0.30	0.40	0.50
H		0.35REF	
K		0.35REF	
L	0.35	0.40	0.45
R	0.085	–	–
C1	–	0.07	–
C2	–	0.07	–

Figure 9 QFN20L 0303 Package Size

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Specification

Operation frequency:2402MHz~2465MHz
Maximum power: 6.27dBm(EIRP)

Statement

1. The device complies with RF specifications when the device used at 0mm form your body.
2. This product is a category 1 receiver device.
3. The operating temperature of the EUT can't exceed 55℃ and shouldn't be lower than -20℃.
4. This product can be used across EU member states.

Hereby, DA KAI INDUSTRIES LIMITED. declares that the product compliance with essential requirements and other relevant provisions of Directive 2014/53/EU.

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configuration bits.

FCC Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-- Reorient or relocate the receiving antenna.

-- Increase the separation between the equipment and receiver.

-- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-- Consult the dealer or an experienced radio/TV technician for help.

§15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§15.21 Information to user.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

RF exposure

This equipment complies with FCC and ISED radiation exposure limits set forth for an uncontrolled environment. The RF exposure compliance of the distance of 0 mm between the radiator and your body. Antenna gain must be below 0.4dBi.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093.

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

Labelling Requirements for the Host device

The host device shall be properly labeled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and ISED of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Model: 2.4G module

Contains FCC ID：2APYU-DKL1613

The host OEM user manual must also contain clear instructions on how end users canfind and/or access the module and the FCC ID and ISED.

Model: 2.4G module

Contains FCC ID：2APYU-DKL1613

The transmitter module may not be co-located with any other transmitter or antenna. Module Antenna Type: Integral Antenna,ANT Gain: 0.4dBi

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OEM Statement

a. The module manufacturer must show how compliance can be demonstrated only for specific host or hosts

b. The module manufacturer must limit the applicable operating conditions in which t transmitter will be used, and

c. The module manufacturer must disclose that only the module grantee can make the te evaluation that the module is compliant in the host. When the module grantee either refuses to make this evaluation, or does not think it is necessary, the module certification is rendered invalid for use in the host, and the host manufacturer has no choice other than to use a different module, or take responsibility (§ 2.929) and obtain a new FCC ID for the product.

d. The module manufacturer must provide the host manufacturer with the follow requirements:

e. The host manufacturer is responsible for additional testing to verify compliance as composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions).

Validity of using the module certification:
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

KDB Ref Sect	**Requirements of KDB 996369 D03**	**Description**
2.2	List of applicable FCC rules	This product compliance with FCC Part 15C section 15.249, section 15.203,section 15.207,section 15.209, section 15.215.
2.3	Summarize the specific operational use conditions	This product has an Integral antenna
2.4	Limited module procedures	This product is a limited module
2.5	Trace antenna designs	This product without trace antenna designs
2.6	RF exposure considerations	race antenna designs compliance RF exposure limits
2.7	Antennas	This product has an Integral antenna
2.8	Label and compliance information	The host system using this module , should label in a visible area indicated the following texts: "Contains FCC ID : 2APYU-DKL1613"
2.9	Information on test modes and additional testing requirements	Data transfer module demo can control the EUT works in RF test mode and specified channel
2.10	Additional testing, Part 15 Subpart B disclaimer	The module without unintentional-radiator digital circuit, so the module does not require an evaluation by FCC part 15 Subpart B. The host should be evaluated by FCC part 15 Subpart B

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