

# **W-LAN+Bluetooth Combo Module Data Sheet**

**Cypress Chipset**  
**for 802.11b/g/n + Bluetooth® v5.1**

**Sample P/N : LBEE5KL1DX-TEMP**

## The revision history of the product specification

| Issued Date   | Revision Code | Revision Page                             | Changed Items                                                                                                                                                                | Change Reason                                      |
|---------------|---------------|-------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|
| Dec.1, 2014   | -             | -                                         | First Issue                                                                                                                                                                  |                                                    |
| Dec.4, 2014   | A             | P.4<br>P.8                                | m1 and m2 of Dimensions.<br>VDDIO of Rating.                                                                                                                                 | Correction                                         |
| Jan.23, 2015  | B             | P.4                                       | Dimensions                                                                                                                                                                   | Correction                                         |
| Feb.9, 2015   | C             | P.3                                       | Block Diagram                                                                                                                                                                | Correction                                         |
| Mar.4, 2015   | D             | P.8<br>P.15-17                            | VBAT voltage<br>DC/RF Characteristics                                                                                                                                        | Correction                                         |
| Mar.26, 2015  | E             | P.5<br>P.15-18<br>P.17<br>P.20<br>P.21-23 | Terminal Configurations (16)<br><br>Characteristics (Fix values on items described TBD)<br><br>Conditions VBAT voltage<br><br>Reference circuit<br><br>Tape and Reel Packing | Correction<br>Spec. fixed                          |
| Jun.19, 2015  | F             | P7<br>P19                                 | Add note of SDIO<br>Add BLE spec                                                                                                                                             |                                                    |
| Jul.21, 2015  | G             | P8<br><br>P23                             | Conditions VBAT voltage<br>Specification Temperature Range<br><br>Add recommend parts name                                                                                   | Correction                                         |
| Aug.26 2015   | H             | P14-17                                    | Typ values                                                                                                                                                                   | Addition                                           |
| Sep. 26. 2015 | I             | P4<br>P23                                 | 4. Dimensions, Marking and Terminal Configurations<br>11. Land pattern                                                                                                       | Addition                                           |
| Feb.8.2016    | J             | P22                                       | Add BLE Rx spec                                                                                                                                                              | Addition                                           |
| Feb.29.2016   | K             | P4<br>P5<br>P6                            | Add marking information<br><br>Terminal Conditions(14)<br><br>6.2 Power Up Sequence                                                                                          | Addition<br>Correction<br>Correction               |
| Mar.18.2016   | L             | P4<br>P6                                  | Add structure<br><br>Terminal Conditions(37)                                                                                                                                 | Addition<br>Correction                             |
| Nov.24.2016   | M             | P3<br>P5                                  | Add certification information<br><br>Add Pin Layout                                                                                                                          | Addition                                           |
| Dec.14.2016   | N             | P33                                       | APPENDIX                                                                                                                                                                     | Addition                                           |
| Feb.28.2017   | O             |                                           | IC Part Number                                                                                                                                                               | Changed                                            |
| Mar.20.2018   | P             | P25                                       | 13. Reference Circuit                                                                                                                                                        | Added 32.768kHz X'tal in the reference circuit.    |
| May.08.2018   | Q             | P3                                        | 1. Scope<br><br>4.2. Bluetooth® Qualification                                                                                                                                | Updated Bluetooth version with 4.2<br>Updated QDID |
| Jun.14.2018   | R             | P4                                        | 5.1. Dimensions                                                                                                                                                              | Correction                                         |
| July 11, 2018 | S             | P3                                        | 4.1 4. Certification Information                                                                                                                                             | Updated (Europe)                                   |
| May 16, 2019  | T             | P31<br>P38                                | 16. PRECONDITION TO USE OUR PRODUCTS<br>Appendix                                                                                                                             | Updated<br><br>Added user manual for Japan         |

| Issued Date | Revision Code | Revision Page | Changed Items                             | Change Reason                                      |
|-------------|---------------|---------------|-------------------------------------------|----------------------------------------------------|
| Dec 6, 2019 | U             | P3            | 1. Scope<br>4.2. Bluetooth® Qualification | Updated Bluetooth version with 5.1<br>Updated QDID |
|             |               |               |                                           |                                                    |

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***Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.***

## 1. Scope

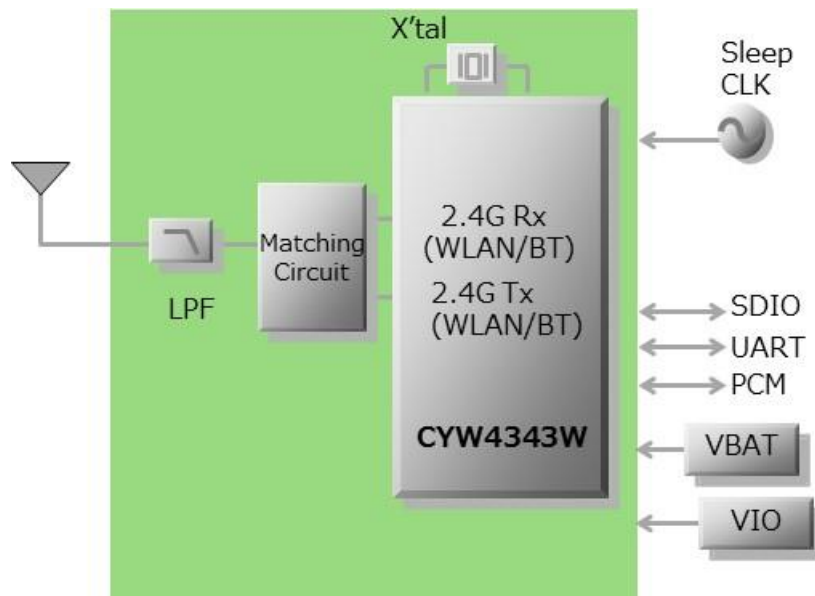
This specification is applied to the IEEE802.11b/g/n W-LAN + Bluetooth® v5.1 (BR/EDR/BLE) module.

- Interface : SDIO (WLAN), UART (BT)
- IC/Firmware : Cypress/CYW4343W
- Reference Clock : Reference clock is embedded.
- MSL : Level 3
- RoHS : This module is compliant with the RoHS directive.

## 2. Part Number

|                    |                   |
|--------------------|-------------------|
| Sample Part Number | LBEE5KL1DX-TEMP   |
| EVK Part Number    | LBEE5KL1DX-TEMP-D |

## 3. Block Diagram



## 4. Certification Information

### 4.1. Radio Certification

#### USA/Canada

FCC ID : VPYLB1DX

IC : 772C-LB1DX

\*Please follow installation manual of Appendix

#### Europe

EN300328 v2.1.1 conducted test report is prepared.

#### Japan

Japanese type certification is prepared.

[R]01- P00840

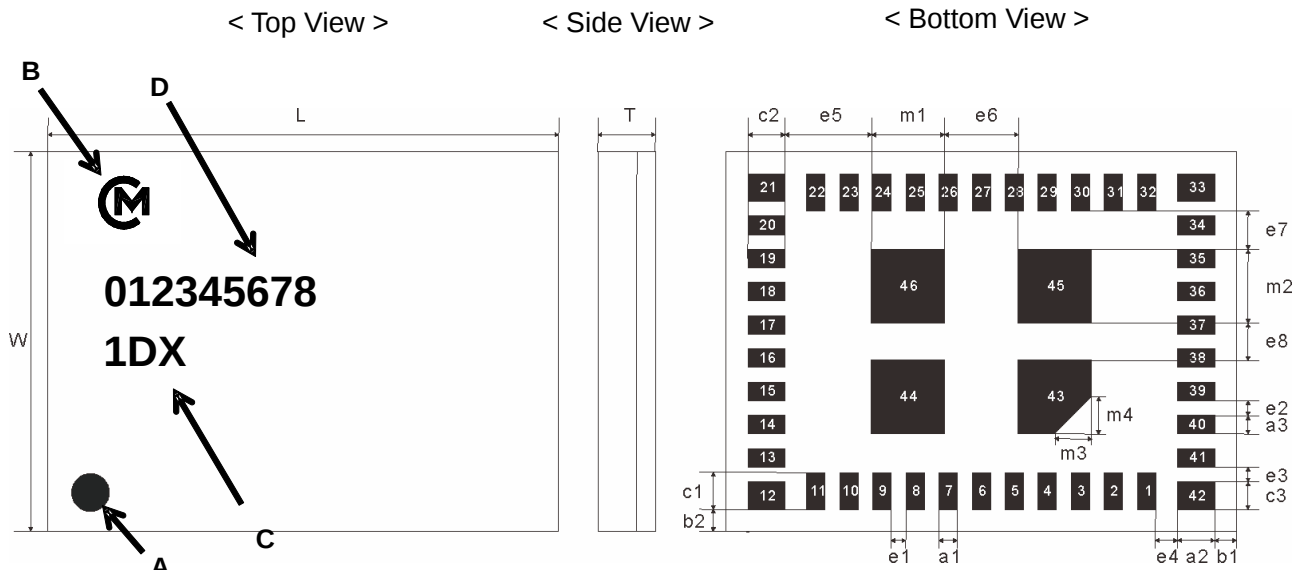
\*Please follow user manual of Appendix

### 4.2. Bluetooth® Qualification

QDID: 140301

## 5. Dimensions, Marking and Terminal Configurations

### 5.1. Dimensions



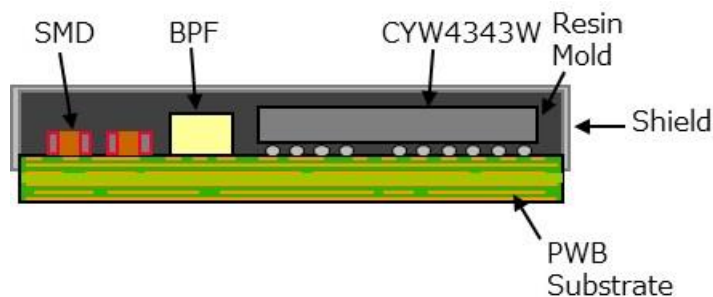
| Marking | Meaning           |
|---------|-------------------|
| A       | Pin 1 Marking     |
| B       | Murata Logo       |
| C       | Module Type       |
| D       | Inspection Number |

#### Dimensions

(unit : mm)

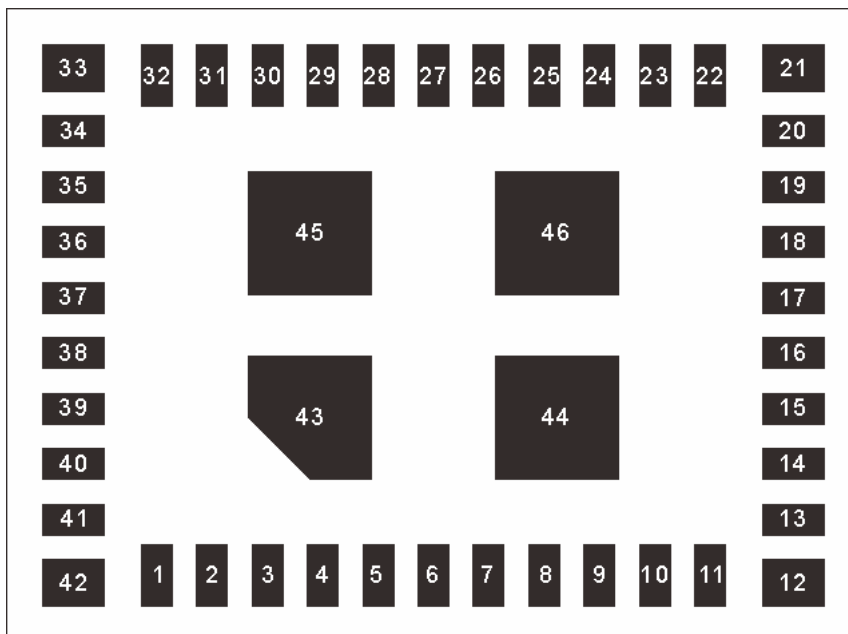
| Mark | Dimensions      | Mark | Dimensions      | Mark | Dimensions      |
|------|-----------------|------|-----------------|------|-----------------|
| L    | 6.95 +/- 0.2    | W    | 5.15 +/- 0.2    | T    | 1.1 max.        |
| a1   | 0.25 +/- 0.10   | a2   | 0.5 +/- 0.1     | a3   | 0.25 +/- 0.10   |
| b1   | 0.30 +/- 0.2    | b2   | 0.30 +/- 0.2    | c1   | 0.50 +/- 0.1    |
| c2   | 0.50 +/- 0.1    | c3   | 0.375 +/- 0.100 | e1   | 0.2 +/- 0.1     |
| e2   | 0.2 +/- 0.1     | e3   | 0.2 +/- 0.1     | e4   | 0.3 +/- 0.1     |
| e5   | 1.175 +/- 0.100 | e6   | 1.0 +/- 0.1     | e7   | 0.525 +/- 0.100 |
| e8   | 0.50 +/- 0.10   | m1   | 1.0 +/- 0.1     | m2   | 1.0 +/- 0.1     |
| m3   | 0.5 +/- 0.1     | m4   | 0.5 +/- 0.1     |      |                 |

#### Structure



## 5.2. Pin Layout

Top View



| No. | Terminal Name | No. | Terminal Name       | No.   | Terminal Name  |
|-----|---------------|-----|---------------------|-------|----------------|
| 1   | GND           | 15  | WL_GPIO_4           | 29    | GND            |
| 2   | BT_UART_RXD   | 16  | BT_I2S_dO           | 30    | VBAT           |
| 3   | BT_UART_TXD   | 17  | WL_GPIO_2           | 31    | VIN_LDO        |
| 4   | BT_UART_CTS_N | 18  | WL_GPIO_1           | 32    | GND (SR_PVSS)  |
| 5   | BT_UART_RTS_N | 19  | GND                 | 33    | GND (SR_PVSS)  |
| 6   | BT_GPIO_3     | 20  | SDIO_CLK            | 34    | SR_VLX         |
| 7   | BT_GPIO_4     | 21  | GND                 | 35    | GND            |
| 8   | BT_PCM_SYNC   | 22  | SDIO_CMD            | 36    | VIO            |
| 9   | BT_PCM_IN     | 23  | SDIO_DATA_2         | 37    | LPO_IN (32kHz) |
| 10  | BT_PCM_OUT    | 24  | SDIO_DATA_0         | 38    | BT_HOST_WAKE   |
| 11  | BT_PCM_CLK    | 25  | SDIO_DATA_3         | 39    | BT_DEV_WAKE    |
| 12  | GND           | 26  | SDIO_DATA_1         | 40    | GND            |
| 13  | BT_GPIO_5     | 27  | WL_GPIO_0_HOST_WAKE | 41    | ANT            |
| 14  | BT_REG_ON     | 28  | WL_REG_ON           | 42~46 | GND            |

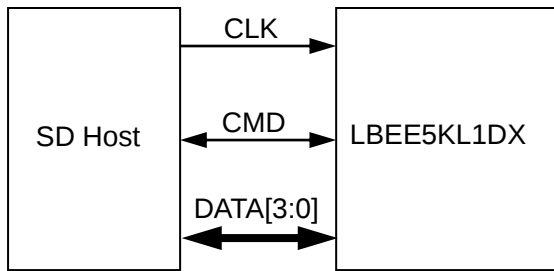
### 5.3. Module PIN Descriptions

| No.  | Terminal Name | Type | Connection to IC Terminal | Description                                                                                                                                                                                                                                                                                      |
|------|---------------|------|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| (1)  | GND           |      |                           |                                                                                                                                                                                                                                                                                                  |
| (2)  | BT_UART_RXD   | I    | BT_UART_RXD               | UART serial input. Serial data input for the HCI UART interface.                                                                                                                                                                                                                                 |
| (3)  | BT_UART_TXD   | O    | BT_UART_TXD               | UART serial output. Serial data output for the HCI UART interface.                                                                                                                                                                                                                               |
| (4)  | BT_UART_CTS_N | I    | BT_UART_CTS_N             | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.                                                                                                                                                                                                                  |
| (5)  | BT_UART_RTS_N | O    | BT_UART_RTS_N             | UART request-to-send. Active-low request-to-send signal for the HCI UART interface.                                                                                                                                                                                                              |
| (6)  | BT_GPIO_3     |      | BT_GPIO_3                 |                                                                                                                                                                                                                                                                                                  |
| (7)  | BT_GPIO_4     |      | BT_GPIO_4                 |                                                                                                                                                                                                                                                                                                  |
| (8)  | BT_PCM_SYNC   | I/O  | BT_PCM_SYNC               | PCM sync; can be master (output) or slave (input)                                                                                                                                                                                                                                                |
| (9)  | BT_PCM_IN     | I    | BT_PCM_IN                 | PCM data input sensing                                                                                                                                                                                                                                                                           |
| (10) | BT_PCM_OUT    | O    | BT_PCM_OUT                | PCM data output                                                                                                                                                                                                                                                                                  |
| (11) | BT_PCM_CLK    | I/O  | BT_PCM_CLK                | PCM clock; can be master (output) or slave (input)                                                                                                                                                                                                                                               |
| (12) | GND           |      |                           |                                                                                                                                                                                                                                                                                                  |
| (13) | BT_GPIO_5     |      | BT_GPIO_5                 |                                                                                                                                                                                                                                                                                                  |
| (14) | BT_REG_ON     | I    | BT_REG_ON                 | Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k $\Omega$ pull-down resistor that is enabled by default. It can be disabled through programming. |
| (15) | WL_GPIO_4     |      | GPIO_4                    |                                                                                                                                                                                                                                                                                                  |
| (16) | BT_I2S_dO     |      |                           |                                                                                                                                                                                                                                                                                                  |
| (17) | WL_GPIO_2     |      | GPIO_2                    |                                                                                                                                                                                                                                                                                                  |
| (18) | WL_GPIO_1     |      | GPIO_1                    |                                                                                                                                                                                                                                                                                                  |
| (19) | GND           |      |                           |                                                                                                                                                                                                                                                                                                  |
| (20) | SDIO_CLK      | I    |                           | SDIO clock input                                                                                                                                                                                                                                                                                 |
| (21) | GND           |      |                           |                                                                                                                                                                                                                                                                                                  |

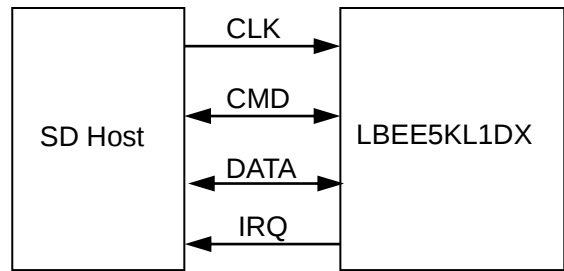
|                   |                     |     |                              |                                                                                                                                                                                                                                                                                        |
|-------------------|---------------------|-----|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| (22)              | SDIO_CMD            | I/O | SDIO_CMD                     | SDIO command line                                                                                                                                                                                                                                                                      |
| (23)              | SDIO_DATA_2         | I/O | SDIO_DATA_2                  | SDIO data line 2                                                                                                                                                                                                                                                                       |
| (24)              | SDIO_DATA_0         | I/O | SDIO_DATA_0                  | SDIO data line 0                                                                                                                                                                                                                                                                       |
| (25)              | SDIO_DATA_3         | I/O | SDIO_DATA_3                  | SDIO data line 3                                                                                                                                                                                                                                                                       |
| (26)              | SDIO_DATA_1         | I/O | SDIO_DATA_1                  | SDIO data line 1                                                                                                                                                                                                                                                                       |
| (27)              | WL_GPIO_0_HOST_WAKE |     | GPIO_0                       |                                                                                                                                                                                                                                                                                        |
| (28)              | WL_REG_ON           | I   | WL_REG_ON                    | Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when deasserted, this pin holds the WLAN section in reset. This pin has an internal 200k $\Omega$ pull-down resistor that is enabled by default. It can be disabled through programming. |
| (29)              | GND                 |     |                              |                                                                                                                                                                                                                                                                                        |
| (30)              | VBAT                |     | LDO_VDDBAT5V,<br>SR_VDDBAT5V |                                                                                                                                                                                                                                                                                        |
| (31)              | VIN_LDO             |     | LDO_VDD1P5,<br>WLRV_VDD_1P35 |                                                                                                                                                                                                                                                                                        |
| (32)              | GND (SR_PVSS)       |     |                              |                                                                                                                                                                                                                                                                                        |
| (33)              | GND (SR_PVSS)       |     |                              |                                                                                                                                                                                                                                                                                        |
| (34)              | SR_VLX              |     | SR_VLX                       | CBUCK switching regulator output.                                                                                                                                                                                                                                                      |
| (35)              | GND                 |     |                              |                                                                                                                                                                                                                                                                                        |
| (36)              | VIO                 |     | SCC_VDDIO,<br>SYS_VDDIO      |                                                                                                                                                                                                                                                                                        |
| (37)              | LPO_IN (32kHz)      | I   | LPO_IN                       | External sleep clock input (32.768kHz).                                                                                                                                                                                                                                                |
| (38)              | BT_HOST_WAKE        | I/O | BT_HOST_WAKE                 | HOST_WAKE or general-purpose I/O signal                                                                                                                                                                                                                                                |
| (39)              | BT_DEV_WAKE         | I/O | BT_DEV_WAKE                  | DEV_WAKE or general-purpose I/O signal                                                                                                                                                                                                                                                 |
| (40)              | GND                 |     |                              |                                                                                                                                                                                                                                                                                        |
| (41)              | ANT                 |     |                              |                                                                                                                                                                                                                                                                                        |
| (42)<br>~<br>(46) | GND                 |     |                              |                                                                                                                                                                                                                                                                                        |

## SDIO Pin Description

| No. | Pin Name | (i) SD 4-bit Mode |                        | (ii) SD 1-bit Mode |              |
|-----|----------|-------------------|------------------------|--------------------|--------------|
| 20  | SDIO_CLK | CLK               | Clock                  | CLK                | Clock        |
| 24  | SDIO_D0  | DATA0             | Data line 0            | DATA               | Data line    |
| 26  | SDIO_D1  | DATA1             | Data line 1 /Interrupt | IRQ                | Interrupt    |
| 23  | SDIO_D2  | DATA2             | Data line 2            | NC                 | Not used     |
| 25  | SDIO_D3  | DATA3             | Data line 3            | NC                 | Not used     |
| 22  | SDIO_CMD | CMD               | Command line           | CMD                | Command line |



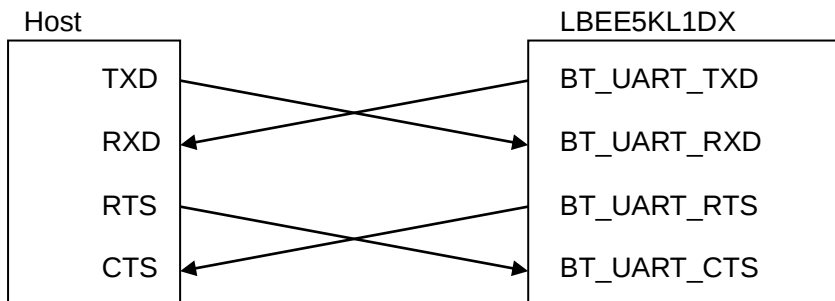
(i) SD 4-bit Mode



(ii) SD 1-bit Mode

Note : 10 to 100k $\Omega$  pull-ups are required on the four DATA lines and the CMD line. This requirement must be met during all operating states by using external pull-up resistors or properly programming internal SDIO host pull-ups.

## UART connection



UART Connection

## 6. Rating

|                     |       | min. | max. | unit  |
|---------------------|-------|------|------|-------|
| Storage Temperature |       | -40  | +85  | deg.C |
| Supply Voltage      | VBAT  | -0.5 | 5.0  | V     |
|                     | VDDIO | -0.5 | 3.9  | V     |

\* Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

## 7. Operating Condition

### 7.1. Operating condition

|                                 |       | min. | typ.       | max. | unit  |
|---------------------------------|-------|------|------------|------|-------|
| Operating Temperature Range     |       | -30  | +25        | +70  | deg.C |
| Specification Temperature Range |       | -10  | +25        | +55  | deg.C |
| Operating Voltage               | VBAT  | 3.0  | 3.6        | 4.8  | V     |
|                                 | VDDIO | 1.71 | 1.8 or 3.3 | 3.63 | V     |
| Specification Voltage           | VBAT  | 3.2  | 3.6        | 4.2  | V     |
|                                 | VDDIO | 1.71 | 1.8 or 3.3 | 3.63 | V     |

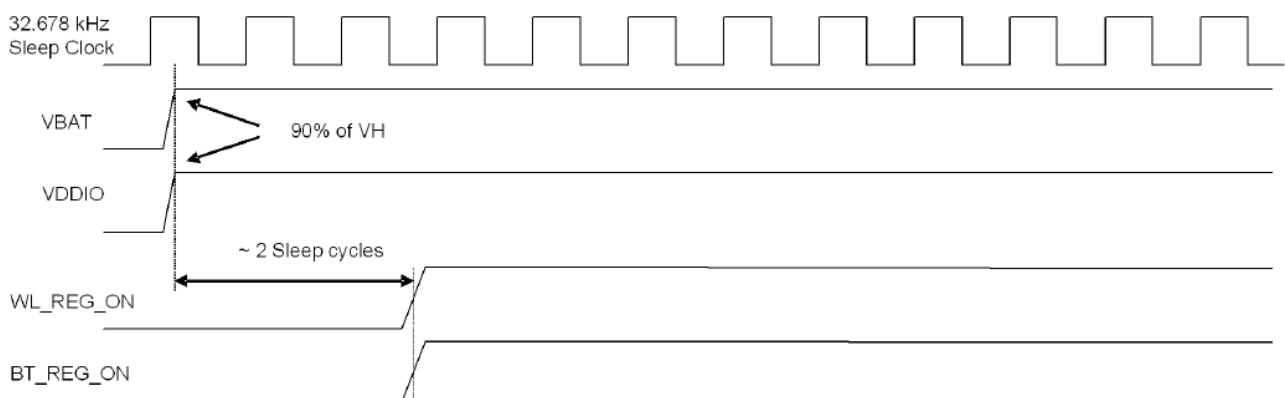
[Note] All RF characteristics in this datasheet are defined by Specification Temperature Range and Specification Voltage.

### 7.2. Power Up Sequence

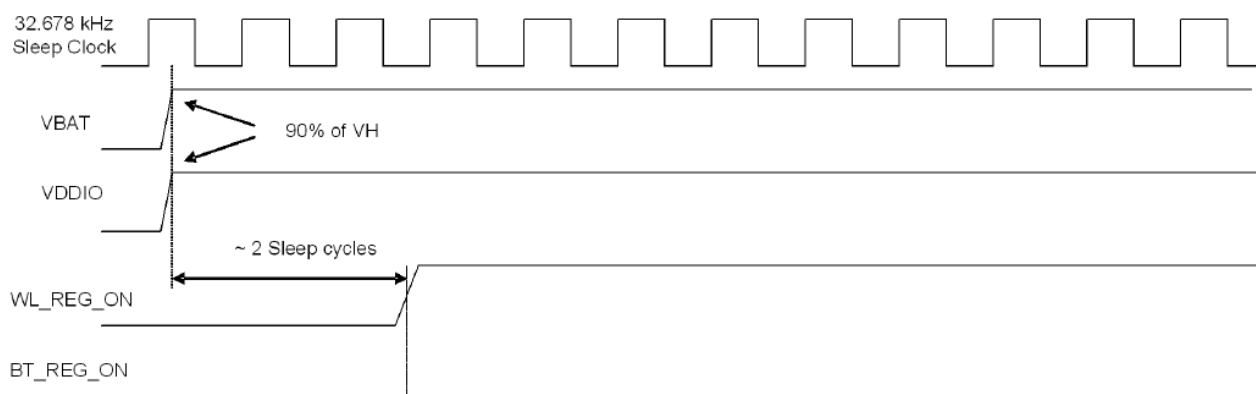
-VBAT should not rise 10%-90% faster than 40 microsecond.

-VBAT should be up before or at the same time as VIO. VIO should NOT be present fast or be held high before VBAT is high.

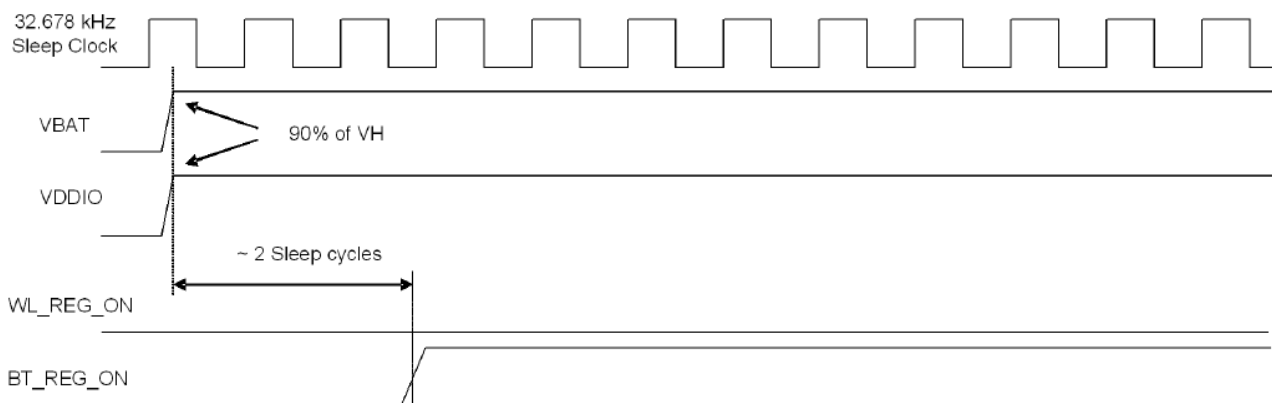
### Power On Sequence for WLAN ON and BT ON



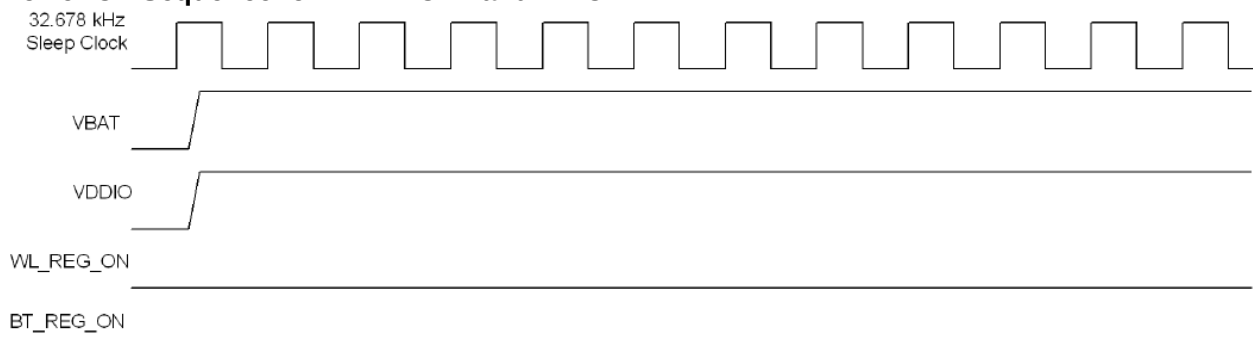
### Power On Sequence for WLAN ON and BT Off



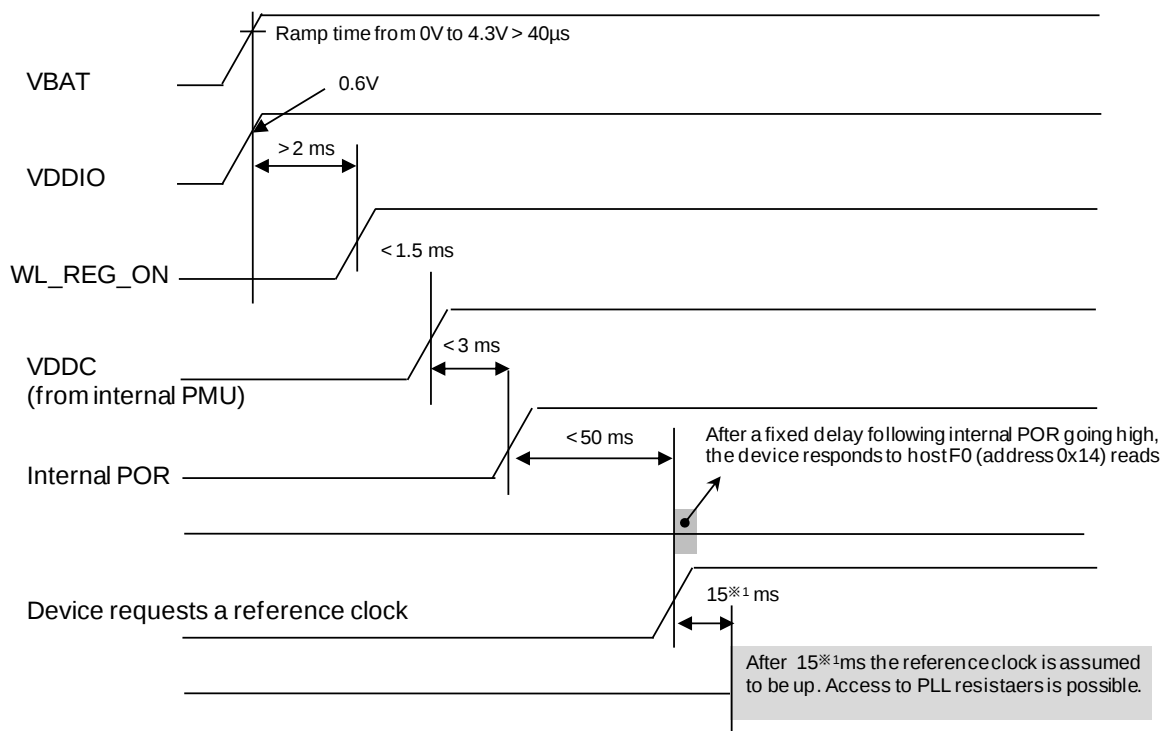
### Power On Sequence for WLAN OFF and BT ON



### Power On Sequence for WLAN OFF and BT OFF

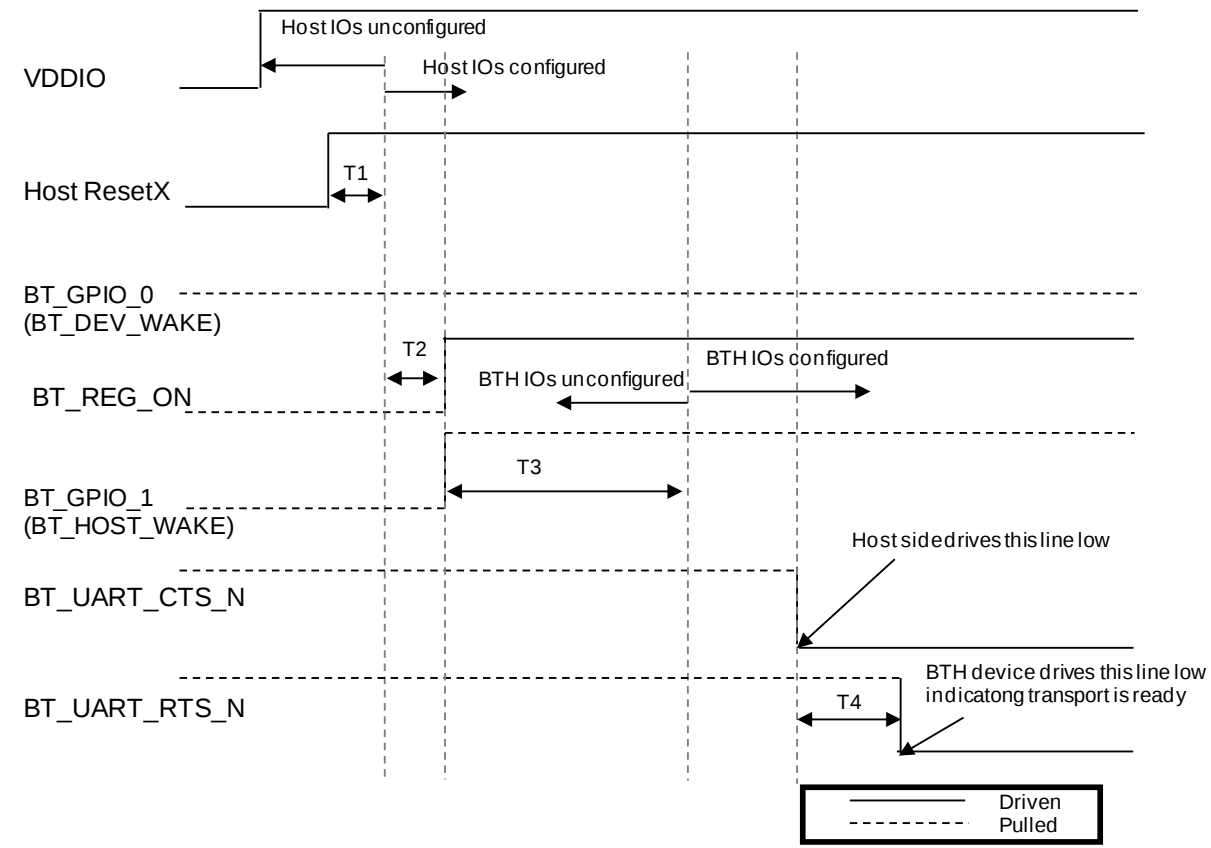


## WLAN Boot up Sequence



※1 This wait time is programmable in sleep-clock increments from 1 to 255 (30us to 15ms)

## Startup Signaling Sequence



T1 is the time for host to settle its IOs after a reset.

T2 is the time for host to drive BT\_REG\_ON high after the Host IOs are configured.

T3 is the time for BTH (Bluetooth) device to settle its IOs after a reset and reference clock settling time has elapsed.

T4 is the time for BTH device to drive BT\_UART\_RTS\_N low after the host drives BT\_UART\_CTS\_N low. This assumes the BTH device has already completed initialization.

Timing diagram assumes VBAT is present.

## 8. Digital I/O Requirements

| SDIO Interface I/O Pins                       | Sym             | min.        | max.        | unit |
|-----------------------------------------------|-----------------|-------------|-------------|------|
| Input low voltage (VDDIO = 3.3V)              | V <sub>IL</sub> | -           | 0.25*VDDIO  | V    |
| Input high voltage (VDDIO = 3.3V)             | V <sub>IH</sub> | 0.625*VDDIO | -           | V    |
| Input low voltage (VDDIO = 1.8V) <sup>1</sup> | V <sub>IL</sub> | -           | 0.58        | V    |
| Input high voltage (VDDIO = 1.8V)             | V <sub>IH</sub> | 1.27        | -           | V    |
| Output low voltage (VDDIO = 3.3V)             | V <sub>OL</sub> | -           | 0.125*VDDIO | V    |
| Output high voltage (VDDIO = 3.3V)            | V <sub>OH</sub> | 0.75*VDDIO  | -           | V    |
| Output low voltage (VDDIO = 1.8V)             | V <sub>OL</sub> | -           | 0.45        | V    |
| Output high voltage (VDDIO = 1.8V)            | V <sub>OH</sub> | 1.40        | -           | V    |

| Other Digital I/O Pins                        | Sym             | min.       | max.       | unit |
|-----------------------------------------------|-----------------|------------|------------|------|
| Input low voltage (VDDIO = 3.3V)              | V <sub>IL</sub> | -          | 0.8        | V    |
| Input high voltage (VDDIO = 3.3V)             | V <sub>IH</sub> | 2.0        | -          | V    |
| Input low voltage (VDDIO = 1.8V) <sup>1</sup> | V <sub>IL</sub> | -          | 0.35*VDDIO | V    |
| Input high voltage (VDDIO = 1.8V)             | V <sub>IH</sub> | 0.65*VDDIO | -          | V    |
| Output low voltage (VDDIO = 3.3V)             | V <sub>OL</sub> | -          | 0.40       | V    |
| Output high voltage (VDDIO = 3.3V)            | V <sub>OH</sub> | VDDIO-0.4  | -          | V    |
| Output low voltage (VDDIO = 1.8V)             | V <sub>OL</sub> | -          | 0.45       | V    |
| Output high voltage (VDDIO = 1.8V)            | V <sub>OH</sub> | VDDIO-0.45 | -          | V    |

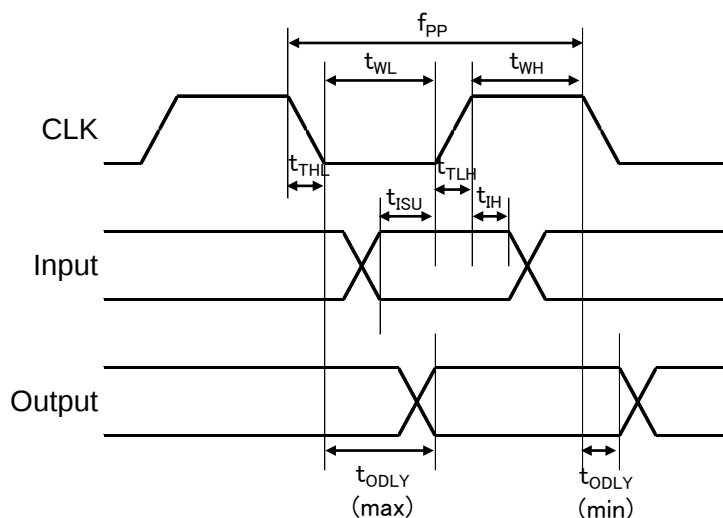
## 9. External LPO Specification

| Parameter                    | Condition/Notes          | Specification |         |         |         |
|------------------------------|--------------------------|---------------|---------|---------|---------|
|                              |                          | Minimum       | Typical | Maximum | Units   |
| Frequency                    | -                        | -             | 32.768  | -       | KHz     |
| Frequency accuracy           | -                        | -200          | -       | +200    | ppm     |
| Duty cycle                   | -                        | 30            | -       | 70      | %       |
| Input amplitude              | -                        | 200           | -       | 3300    | mV, p-p |
| Signal type                  | Square wave or sine wave | -             | -       | -       | -       |
| Input impedance <sup>a</sup> | Resistive                | 100           | -       | -       | kΩ      |
|                              | Capacitive               | -             | -       | 5       | pF      |
| Clock jitter                 | -                        | -             | -       | 10,000  | ppm     |

a. When power is applied or switched off.

## 10. Interface Timing

### 10.1. SDIO Timing (Default Mode)

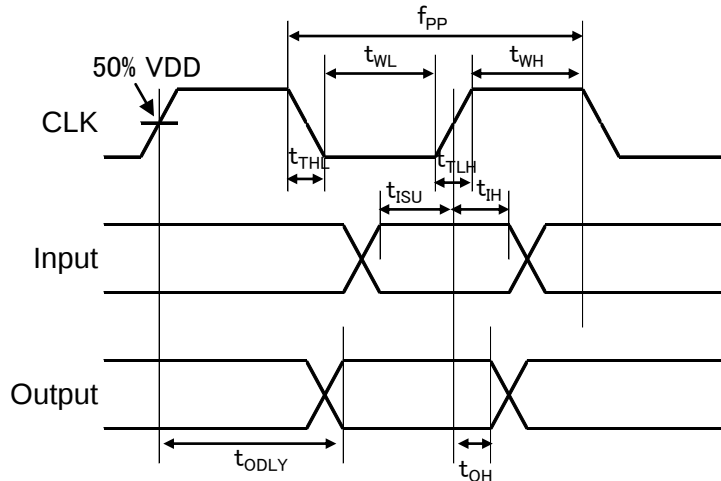


| Parameter                                                                    | Symbol | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|------------------------------------------------------------------------------|--------|--------------------|--------------------|--------------------|------|
| Clock CLK (All values are referred to min. VIH and max. VIL <sup>(2)</sup> ) |        |                    |                    |                    |      |
| Frequency-Data Transfer Mode                                                 | fPP    | 0                  | -                  | 25                 | MHz  |
| Frequency-Identification Mode                                                | fOD    | 0                  | -                  | 400                | kHz  |
| Clock Low Time                                                               | tWL    | 10                 | -                  | -                  | ns   |
| Clock High Time                                                              | tWH    | 10                 | -                  | -                  | ns   |
| Clock Rise Time                                                              | tTLH   | -                  | -                  | 10                 | ns   |
| Clock Fall Time                                                              | tTHL   | -                  | -                  | 10                 | ns   |
| Inputs: CMD, DAT (referenced to CLK)                                         |        |                    |                    |                    |      |
| Input Setup Time                                                             | tISU   | 5                  | -                  | -                  | ns   |
| Input Hold Time                                                              | tIH    | 5                  | -                  | -                  | ns   |
| Outputs: CMD, DAT (referenced to CLK)                                        |        |                    |                    |                    |      |
| Output Delay time-Data Transfer Mode                                         | tODLY  | 0                  | -                  | 14                 | ns   |
| Output Delay time-Identification Mode                                        | tODLY  | 0                  | -                  | 50                 | ns   |

(1). Timing is based on  $CL \leq 40pF$  load on CMD and Data.

(2). Min (Vih) =  $0.7 \cdot VDDIO$  and max (Vil) =  $0.2 \cdot VDDIO$ .

## 10.2. SDIO Timing (High Speed Mode)

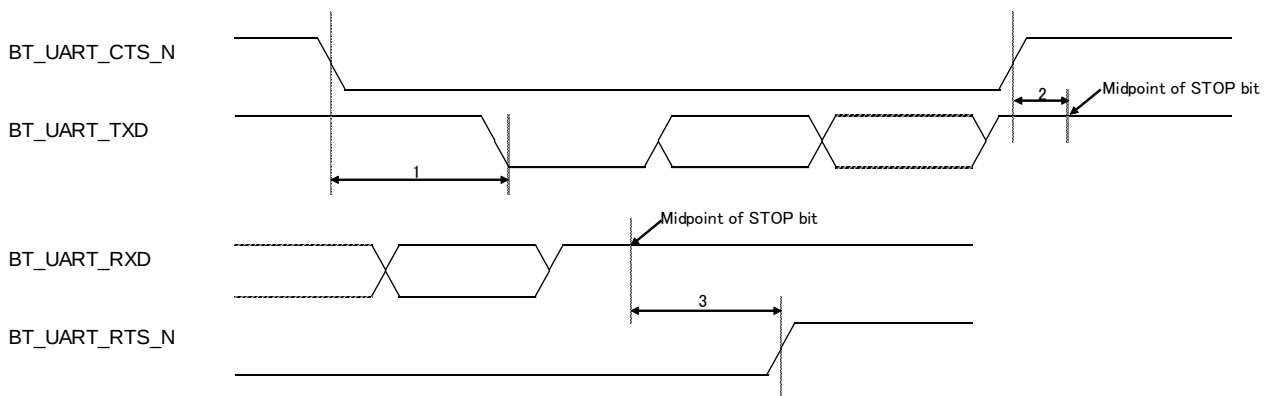


| Parameter                                                                    | Symbol | Min <sup>(1)</sup> | Typ <sup>(1)</sup> | Max <sup>(1)</sup> | Unit |
|------------------------------------------------------------------------------|--------|--------------------|--------------------|--------------------|------|
| Clock CLK (All values are referred to min. VIH and max. VIL <sup>(2)</sup> ) |        |                    |                    |                    |      |
| Frequency-Data Transfer Mode                                                 | fPP    | 0                  | -                  | 50                 | MHz  |
| Frequency-Identification Mode                                                | fOD    | 0                  | -                  | 400                | kHz  |
| Clock Low Time                                                               | tWL    | 7                  | -                  | -                  | ns   |
| Clock High Time                                                              | tWH    | 7                  | -                  | -                  | ns   |
| Clock Rise Time                                                              | tTLH   | -                  | -                  | 3                  | ns   |
| Clock Fall Time                                                              | tTHL   | -                  | -                  | 3                  | ns   |
| Inputs: CMD, DAT (referenced to CLK)                                         |        |                    |                    |                    |      |
| Input Setup Time                                                             | tISU   | 6                  | -                  | -                  | ns   |
| Input Hold Time                                                              | tIH    | 2                  | -                  | -                  | ns   |
| Outputs: CMD, DAT (referenced to CLK)                                        |        |                    |                    |                    |      |
| Output Delay time-Data Transfer Mode                                         | tODLY  | -                  | -                  | 14                 | ns   |
| Output Hold time                                                             | tOH    | 2.5                | -                  | -                  | ns   |
| Total System Capacitance (each line)                                         | CL     | -                  | -                  | 40                 | pF   |

(1). Timing is based on  $CL \leq 40\text{pF}$  load on CMD and Data.

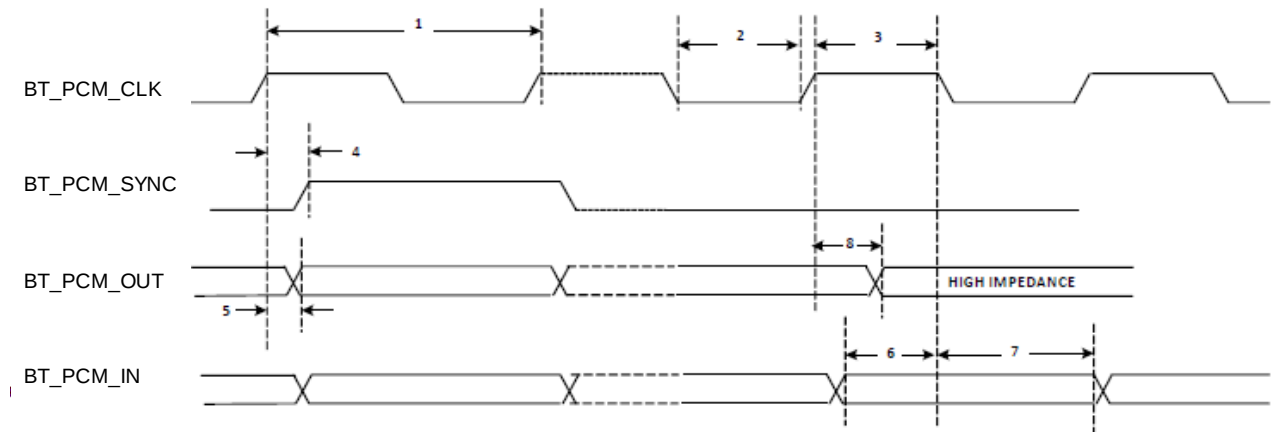
(2). Min (Vih) =  $0.7 \times VDDIO$  and max (Vil) =  $0.2 \times VDDIO$ .

## 10.3. Bluetooth UART Timing (Default Mode)



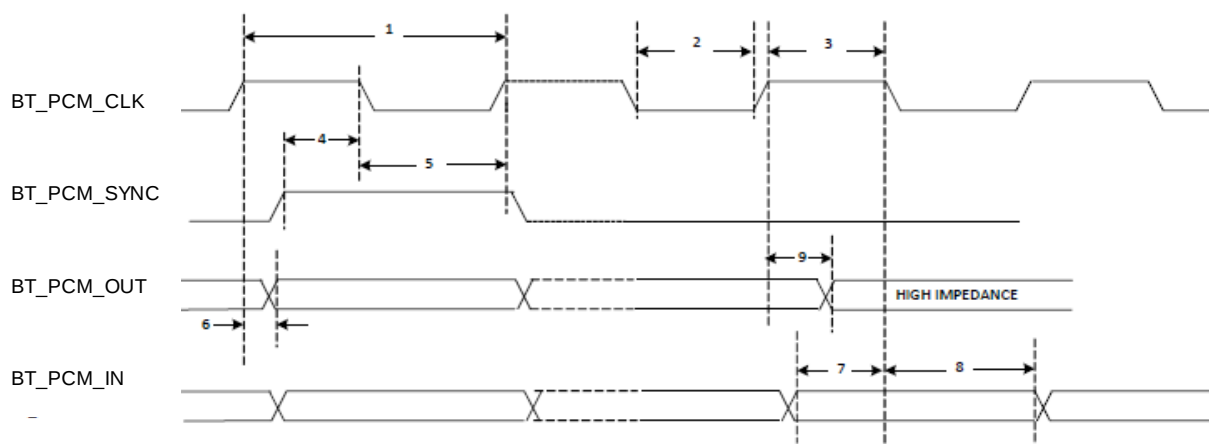
| Reference | Description                                             | Min | Typ | Max | Unit        |
|-----------|---------------------------------------------------------|-----|-----|-----|-------------|
| 1         | Delay time, UART_CTS_N low to UART_TXD valid            | -   | -   | 1.5 | Bit periods |
| 2         | Setup time, UART_CTS_N high before midpoint of stop bit | -   | -   | 0.5 | Bit periods |
| 3         | Delay time, midpoint of stop bit to UART_RTS_N high     | -   | -   | 0.5 | Bit periods |

#### 10.4. PCM Timing Short Frame Sync, Master Mode



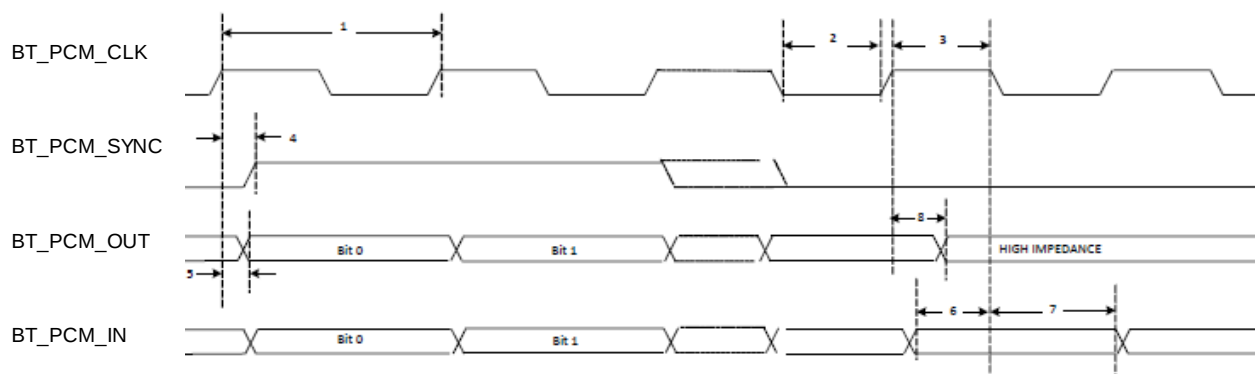
| Reference | Description                                                                                 | Min | Typ | Max | Unit |
|-----------|---------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                     | -   | -   | 12  | MHz  |
| 2         | PCM bit clock low                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock high                                                                          | 41  | -   | -   | ns   |
| 4         | PCM_SYNC delay                                                                              | 0   | -   | 25  | ns   |
| 5         | PCM_OUT delay                                                                               | 0   | -   | 25  | ns   |
| 6         | PCM_IN setup                                                                                | 8   | -   | -   | ns   |
| 7         | PCM_IN hold                                                                                 | 8   | -   | -   | ns   |
| 8         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

## 10.5. PCM Timing Short Frame Sync, Slave Mode



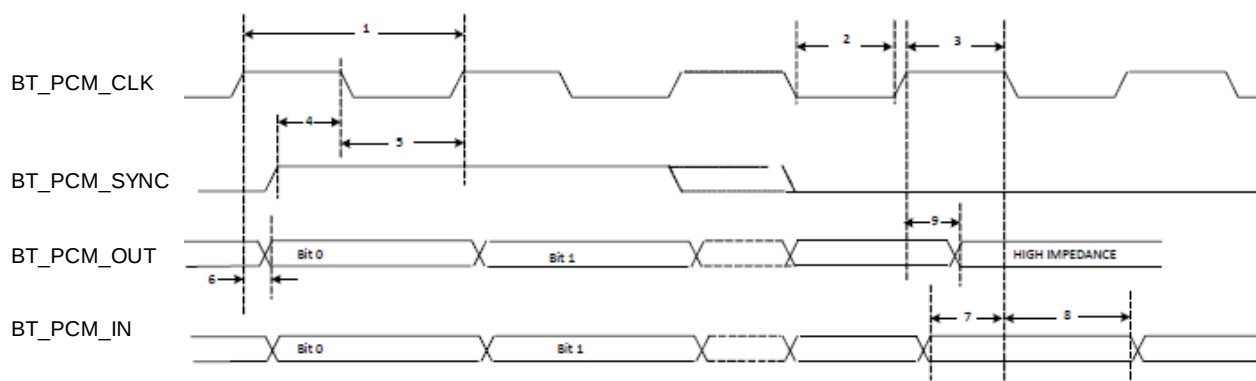
| Reference | Description                                                                                 | Min | Typ | Max | Unit |
|-----------|---------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                     | -   | -   | 12  | MHz  |
| 2         | PCM bit clock Low                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock High                                                                          | 41  | -   | -   | ns   |
| 4         | PCM_SYNC setup                                                                              | 8   | -   | -   | ns   |
| 5         | PCM_SYNC hold                                                                               | 8   | -   | -   | ns   |
| 6         | PCM_OUT delay                                                                               | 0   | -   | 25  | ns   |
| 7         | PCM_IN setup                                                                                | 8   | -   | -   | ns   |
| 8         | PCM_IN hold                                                                                 | 8   | -   | -   | ns   |
| 9         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

## 10.6. PCM Timing Long Frame Sync, Master Mode



| Reference | Description                                                                                 | Min | Typ | Max | Unit |
|-----------|---------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                     | -   | -   | 12  | MHz  |
| 2         | PCM bit clock low                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock high                                                                          | 41  | -   | -   | ns   |
| 4         | PCM_SYNC delay                                                                              | 0   | -   | 25  | ns   |
| 5         | PCM_OUT delay                                                                               | 0   | -   | 25  | ns   |
| 6         | PCM_IN setup                                                                                | 8   | -   | -   | ns   |
| 7         | PCM_IN hold                                                                                 | 8   | -   | -   | ns   |
| 8         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

## 10.7. PCM Timing Long Frame Sync, Slave Mode



| Reference | Description                                                                                 | Min | Typ | Max | Unit |
|-----------|---------------------------------------------------------------------------------------------|-----|-----|-----|------|
| 1         | PCM bit clock frequency                                                                     | -   | -   | 12  | MHz  |
| 2         | PCM bit clock low                                                                           | 41  | -   | -   | ns   |
| 3         | PCM bit clock high                                                                          | 41  | -   | -   | ns   |
| 4         | PCM_SYNC setup                                                                              | 8   | -   | -   | ns   |
| 5         | PCM_SYNC hold                                                                               | 8   | -   | -   | ns   |
| 6         | PCM_OUT delay                                                                               | 0   | -   | 25  | ns   |
| 7         | PCM_IN setup                                                                                | 8   | -   | -   | ns   |
| 8         | PCM_IN hold                                                                                 | 8   | -   | -   | ns   |
| 9         | Delay from rising edge of PCM_CLK during last bit period to PCM_OUT becoming high impedance | 0   | -   | 25  | ns   |

## 11. DC/RF Characteristics

### 11.1. DC/RF Characteristics for IEEE802.11b

|               |                   |
|---------------|-------------------|
| Specification | IEEE802.11b       |
| Mode          | DSSS / CCK        |
| Frequency     | 2400 - 2483.5MHz  |
| Data rate     | 1, 2, 5.5, 11Mbps |

Conditions : 25deg.C, VBAT=3.6V, VDDIO= 3.3V, Output power setting=17dBm, 11Mbps mode

| Items                                  | Contents |      |      |      |
|----------------------------------------|----------|------|------|------|
| - DC Characteristics -                 | min.     | typ. | max. | unit |
| DC current                             |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval) |          | 320  | 370  | mA   |
| 2) Rx mode                             |          | 47   | 60   | mA   |
| - Tx Characteristics -                 | min.     | typ. | max. | unit |
| Output Power (tolerance)               | 15       | 17   | 19   | dBm  |
| Spectrum Mask                          |          |      |      |      |
| 1) 1st side lobes                      | -        | -43  | -30  | dBr  |
| 2) 2nd side lobes                      | -        | -54  | -50  | dBr  |
| Power-on and Power-down ramp           | -        |      | 2.0  | μsec |
| RF Carrier Suppression                 | 15       |      | -    | dB   |
| Modulation Accuracy (EVM)              | -        | 15   | 35   | %    |
| Outband Spurious Emissions             |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)           | -        | -    | -36  | dBm  |
| 2) 1GHz to 12.75GHz (BW=100kHz)        | -        | -    | -30  | dBm  |
| 3) 1.8GHz to 1.9GHz (BW=100kHz)        | -        | -    | -47  | dBm  |
| 4) 5.15GHz to 5.3GHz (BW=100kHz)       | -        | -    | -47  | dBm  |
| - Rx Characteristics -                 | min.     | typ. | max. | unit |
| Minimum Input Level (FER ≤ 8%)         | -        | -89  | -76  | dBm  |
| Maximum Input Level (FER ≤ 8%)         | -10      | -    | -    | dBm  |
| Adjacent Channel Rejection (FER ≤ 8%)  | 35       | -    | -    | dB   |

## 11.2. DC/RF Characteristics for IEEE802.11g

|               |                                  |
|---------------|----------------------------------|
| Specification | IEEE802.11g                      |
| Mode          | OFDM                             |
| Frequency     | 2400 - 2483.5MHz                 |
| Data rate     | 6, 9, 12, 18, 24, 36, 48, 54Mbps |

Conditions : 25deg.C, VBAT=3.6V, VDDIO= 3.3V, Output power setting=13dBm, 54Mbps mode

| Items                                  | Contents |      |      |      |
|----------------------------------------|----------|------|------|------|
| - DC Characteristics -                 | min.     | typ. | max. | unit |
| DC current                             |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval) |          | 270  | 310  | mA   |
| 2) Rx mode                             |          | 47   | 60   | mA   |
| - Tx Characteristics -                 | min.     | typ. | max. | unit |
| Output Power (tolerance)               | 11       | 13   | 15   | dBm  |
| Spectrum Mask                          |          |      |      |      |
| 1) 9MHz to 11MHz (0dB ~ -20dB)         |          | -33  | -20  | dBr  |
| 2) 11MHz to 20MHz (-20dB ~ -28dB)      |          | -41  | -28  | dBr  |
| 3) 20MHz to 30MHz (-28dB ~ -40dB)      |          | -53  | -40  | dBr  |
| 4) 30MHz to 33MHz (-40dB)              |          | -53  | -40  | dBr  |
| Constellation Error (EVM)              | -        | -30  | -25  | dB   |
| Outband Spurious Emissions             |          |      |      |      |
| 1) 30MHz to 1GHz (BW=100kHz)           | -        | -    | -36  | dBm  |
| 2) 1GHz to 12.75GHz (BW=100kHz)        | -        | -    | -30  | dBm  |
| 3) 1.8GHz to 1.9GHz (BW=100kHz)        | -        | -    | -47  | dBm  |
| 4) 5.15GHz to 5.3GHz (BW=100kHz)       | -        | -    | -47  | dBm  |
| - Rx Characteristics -                 | min.     | typ. | max. | unit |
| Minimum Input Level (PER ≤ 10%)        | -        | -75  | -65  | dBm  |
| Maximum Input Level (PER ≤ 10%)        | -20      | -    | -    | dBm  |
| Adjacent Channel Rejection (PER ≤ 10%) | -1       | -    | -    | dB   |

### 11.3. DC/RF Characteristics for IEEE802.11n

|               |                                         |
|---------------|-----------------------------------------|
| Specification | IEEE802.11n                             |
| Mode          | OFDM                                    |
| Frequency     | 2400 - 2483.5MHz                        |
| Data rate     | 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps |

Conditions : 25deg.C, VBAT=3.6V, VDDIO= 3.3V, Output power setting=12dBm, 65Mbps mode

| Items                                  | Contents |      |      |      |
|----------------------------------------|----------|------|------|------|
| - DC Characteristics -                 | min.     | typ. | max. | unit |
| DC current                             |          |      |      |      |
| 1) Tx mode (1024byte, 20usec interval) |          | 260  | 300  | mA   |
| 2) Rx mode                             |          | 47   | 60   | mA   |
| - Tx Characteristics -                 | min.     | typ. | max. | unit |
| Output Power (tolerance)               | 10       | 12   | 14   | dBm  |
| Spectrum Mask                          |          |      |      |      |
| 1) 9MHz to 11MHz (0dB ~ -20dB)         |          | -33  | -20  | dBr  |
| 2) 11MHz to 20MHz (-20dB ~ -28dB)      |          | -41  | -28  | dBr  |
| 3) 20MHz to 30MHz (-28dB ~ -45dB)      |          | -53  | -45  | dBr  |
| 4) 30MHz to 33MHz (-45dB)              |          | -53  | -45  | dBr  |
| Constellation Error (EVM)              | -        | -31  | -27  | dB   |
| Outband Spurious Emissions             |          |      |      |      |
| 1) 30MHz to 1GHz                       | -        | -    | -36  | dBm  |
| 2) 1GHz to 12.75GHz                    | -        | -    | -30  | dBm  |
| 3) 1.8GHz to 1.9GHz                    | -        | -    | -47  | dBm  |
| 4) 5.15GHz to 5.3GHz                   | -        | -    | -47  | dBm  |
| - Rx Characteristics -                 | min.     | typ. | max. | unit |
| Minimum Input Level (PER≤10%)          | -        | -73  | -64  | dBm  |
| Maximum Input Level (PER ≤ 10%)        | -20      | -    | -    | dBm  |
| Adjacent Channel Rejection (PER ≤ 10%) | -2       | -    | -    | dB   |

#### 11.4. DC/RF Characteristics for Bluetooth

Normal conditions : 25deg.C, VBAT = 3.6V, VDDIO = 3.3V

| Items                                                   | Contents                   |      |        |          |
|---------------------------------------------------------|----------------------------|------|--------|----------|
| Bluetooth specification (power class)                   | Version 2.1 + EDR (Class1) |      |        |          |
| Channel frequency (spacing)                             | 2402 to 2480 MHz (1MHz)    |      |        |          |
| Current Consumption                                     | min.                       | typ. | max.   | unit     |
| (a) Tx=Rx=DH5 (fully occupied)                          | -                          | 28   | 60     | mA       |
| (b) Tx=Rx=2DH5 (fully occupied)                         | -                          | 25   | 50     | mA       |
| (c) Tx=Rx=3DH5 (fully occupied)                         | -                          | 25   | 50     | mA       |
| Transmitter                                             | min.                       | typ. | max.   | unit     |
| Output Power                                            | 6                          | 10   | 14     | dBm      |
| Frequency range                                         | 2400                       | -    | 2483.5 | MHz      |
| 20dB bandwidth                                          | -                          | -    | 1      | MHz      |
| Adjacent Channel Power *1                               |                            |      |        |          |
| (a) [M-N] =2                                            | -                          | -    | -20    | dBm      |
| (b) [M-N] ≥3                                            | -                          | -    | -40    | dBm      |
| Modulation characteristics                              |                            |      |        |          |
| (a) Modulation Δf1avg                                   | 140                        | -    | 175    | kHz      |
| (b) Modulation Δf2max                                   | 115                        | -    | -      | kHz      |
| (c) Modulation Δf2avg / Δf1avg                          | 0.8                        | -    | -      |          |
| Carrier Frequency Drift                                 |                            |      |        |          |
| (a) 1slot                                               | -25                        | -    | +25    | kHz      |
| (b) 3slot / 5slot                                       | -40                        | -    | +40    | kHz      |
| (c) Maximum drift rate                                  | -                          | -    | 20     | kHz/50us |
| EDR Relative Power                                      | -4                         | -    | +1     | dB       |
| EDR Carrier Frequency Stability and Modulation Accuracy |                            |      |        |          |
| (a) ωi                                                  | -75                        | -    | +75    | kHz      |
| (b) ωi+ωo                                               | -75                        | -    | +75    | kHz      |
| (c) ωo                                                  | -10                        | -    | +10    | kHz      |
| (d) RMS DEVM (DQPSK)                                    | -                          | -    | 20     | %        |
| (e) Peak DEVM (DQPSK)                                   | -                          | -    | 35     | %        |
| (f) 99% DEVM (DQPSK)                                    | -                          | -    | 30     | %        |
| (g) RMS DEVM (8DPSK)                                    | -                          | -    | 13     | %        |
| (h) Peak DEVM (8DPSK)                                   | -                          | -    | 25     | %        |
| (i) 99% DEVM (8DPSK)                                    | -                          | -    | 20     | %        |
| Out-of-Band Spurious Emissions                          |                            |      |        |          |
| (a) 30-1000MHz                                          | -                          | -    | -36    | dBm      |
| (b) 1000-12750MHz                                       | -                          | -    | -30    | dBm      |
| (c) 1800-1900MHz                                        | -                          | -    | -47    | dBm      |
| (d) 5150-5300MHz                                        | -                          | -    | -47    | dBm      |
| Receiver                                                | Min.                       | Typ. | Max.   | unit     |
| Sensitivity (BER≤0.1%)                                  | -                          | -91  | -80    | dBm      |
| C/I Performance (BER≤0.1%) *2                           |                            |      |        |          |
| (a) co-channel                                          | -                          | -    | 11     | dB       |
| (b) 1MHz                                                | -                          | -    | 0      | dB       |
| (c) 2MHz                                                | -                          | -    | -30    | dB       |
| (d) 3MHz                                                | -                          | -    | -40    | dB       |
| (e) image (+4MHz)                                       | -                          | -    | -9     | dB       |
| (f) image +/- 1MHz                                      | -                          | -    | -20    | dB       |
| Maximum Input Level (PER≤0.1%)                          | -20                        | -    | -      | dBm      |
| EDR Sensitivity (PER≤0.007%)                            |                            |      |        |          |
| (a) 8DPSK                                               | -                          | -88  | -77    | dBm      |

\*1: Up to three spurious responses within Bluetooth limits are allowed.

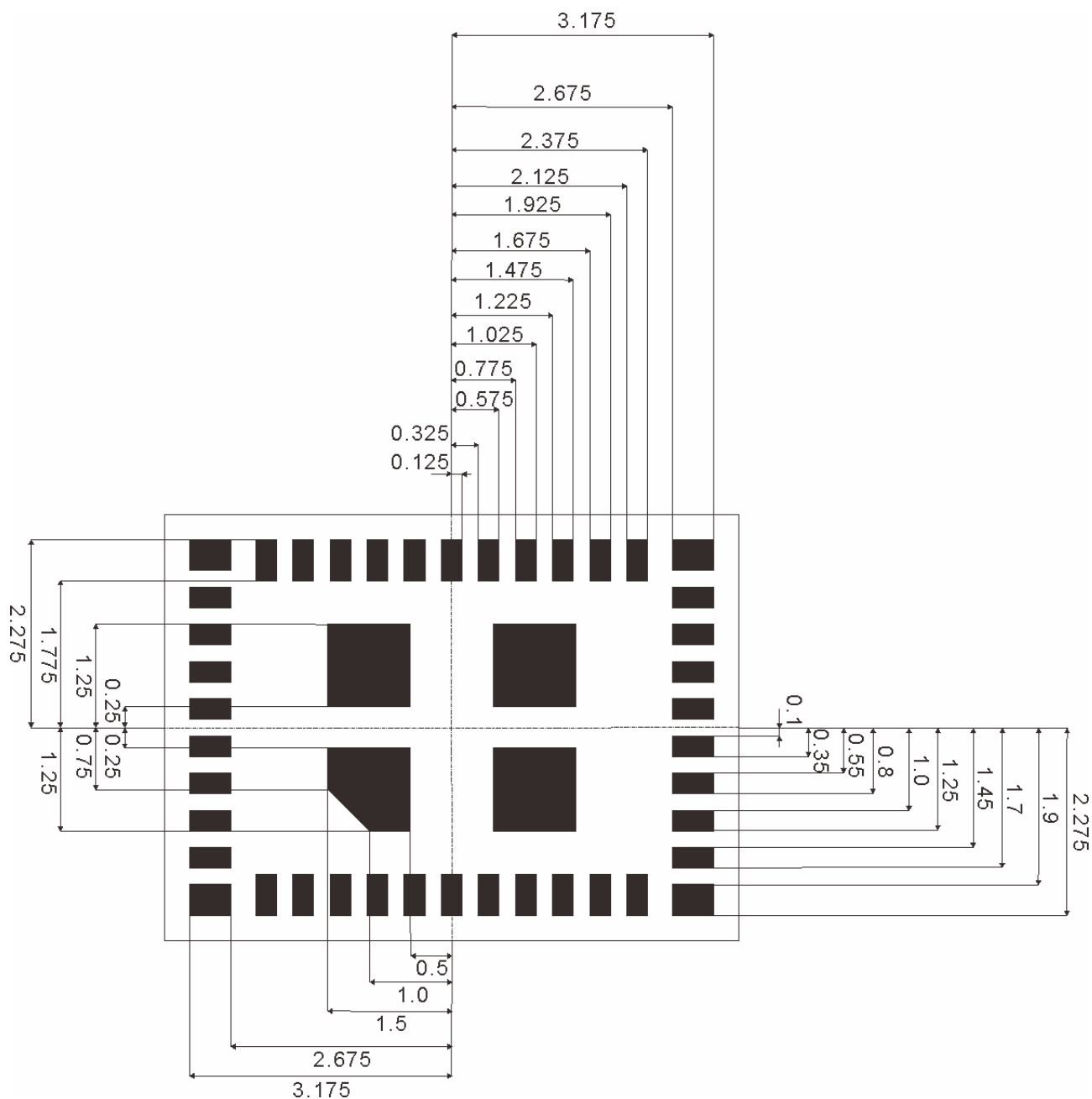
\*2: Up to five spurious responses within Bluetooth limits are allowed.

### 11.5. DC/RF Characteristics for Bluetooth(LE)

Conditions : 25deg.C, VBAT=3.6V, VDDIO= 3.3V

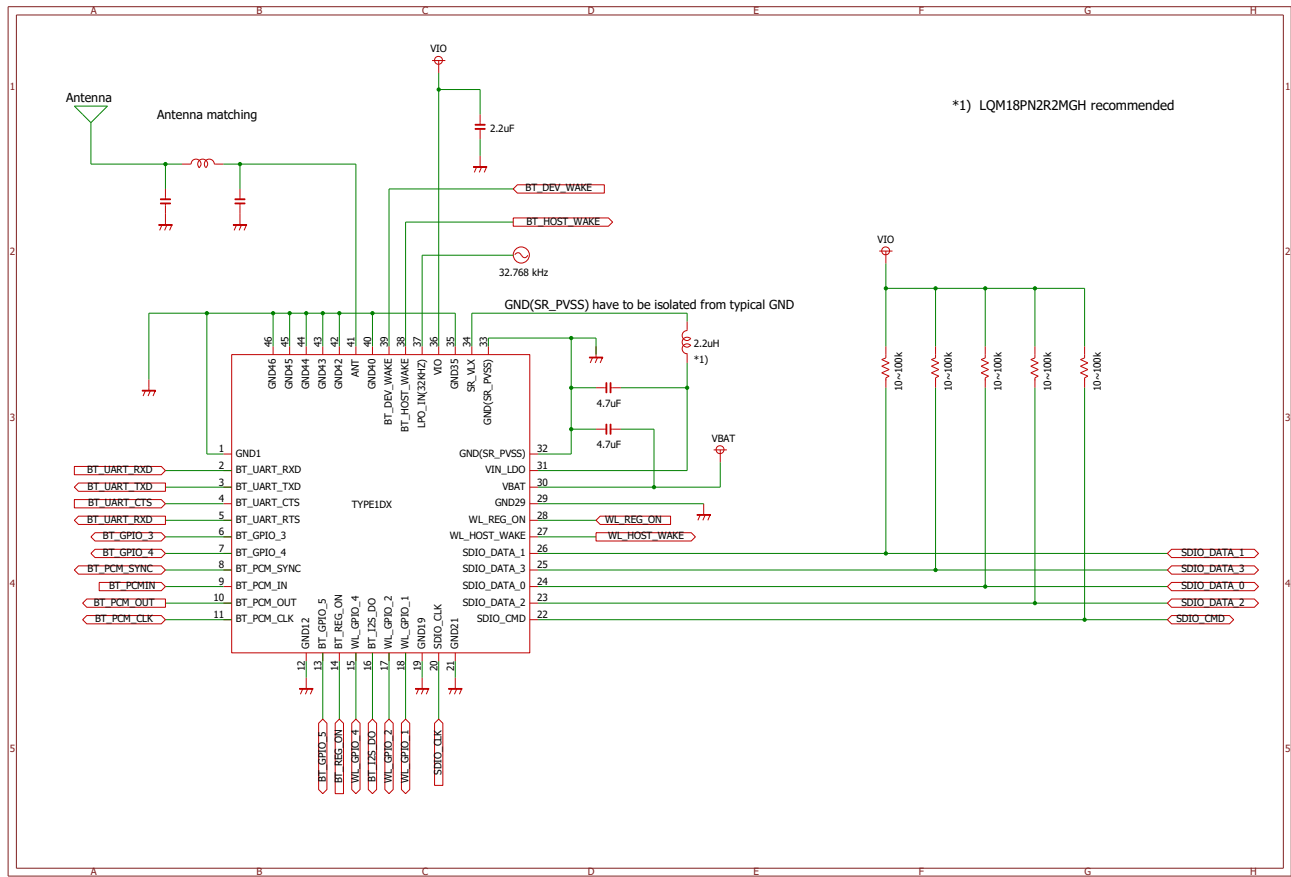
| Items                                                | Contents                |      |      |      |
|------------------------------------------------------|-------------------------|------|------|------|
| Bluetooth specification (power class)                | Version 5.1(LE)         |      |      |      |
| Channel frequency (spacing)                          | 2402 to 2480 MHz (2MHz) |      |      |      |
| Number of RF Channel                                 | 40                      |      |      |      |
| Item / Condition                                     | Min.                    | Typ. | Max. | Unit |
| Center Frequency                                     | 2402                    | -    | 2480 | MHz  |
| Channel Spacing                                      | -                       | 2    | -    | MHz  |
| Number of RF channel                                 | -                       | 40   | -    | -    |
| Output power                                         | -                       | -    | 10   | dBm  |
| Modulation Characteristics                           |                         |      |      |      |
| 1) $\Delta f_{1\text{avg}}$                          | 225                     | -    | 275  | kHz  |
| 2) $\Delta f_{2\text{max}}$ (at 99.9%)               | 185                     | -    | -    | kHz  |
| 3) $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8                     | -    | -    | -    |
| Carrier frequency offset and drift                   |                         |      |      |      |
| 1) Frequency offset                                  | -                       | -    | 150  | kHz  |
| 2) Frequency drift                                   | -                       | -    | 50   | kHz  |
| 3) Drift rate                                        | -                       | -    | 20   | kHz  |
| Receiver sensitivity (PER < 30.8%)                   | -                       | -95  | -70  | dBm  |
| Maximum input signal level (PER < 30.8%)             | -10                     | -    | -    | dBm  |
| PER Report Integrity (-30dBm input)                  | 50                      | -    | 65.4 | %    |

## 12. Land pattern



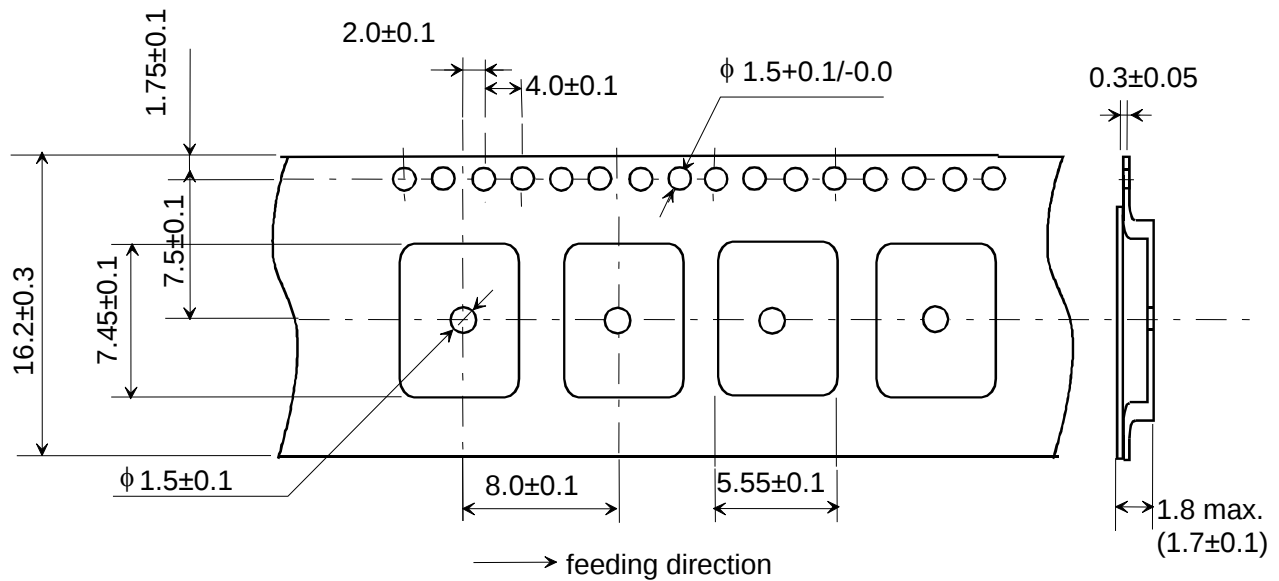
Top View. Unit : mm

### 13. Reference Circuit



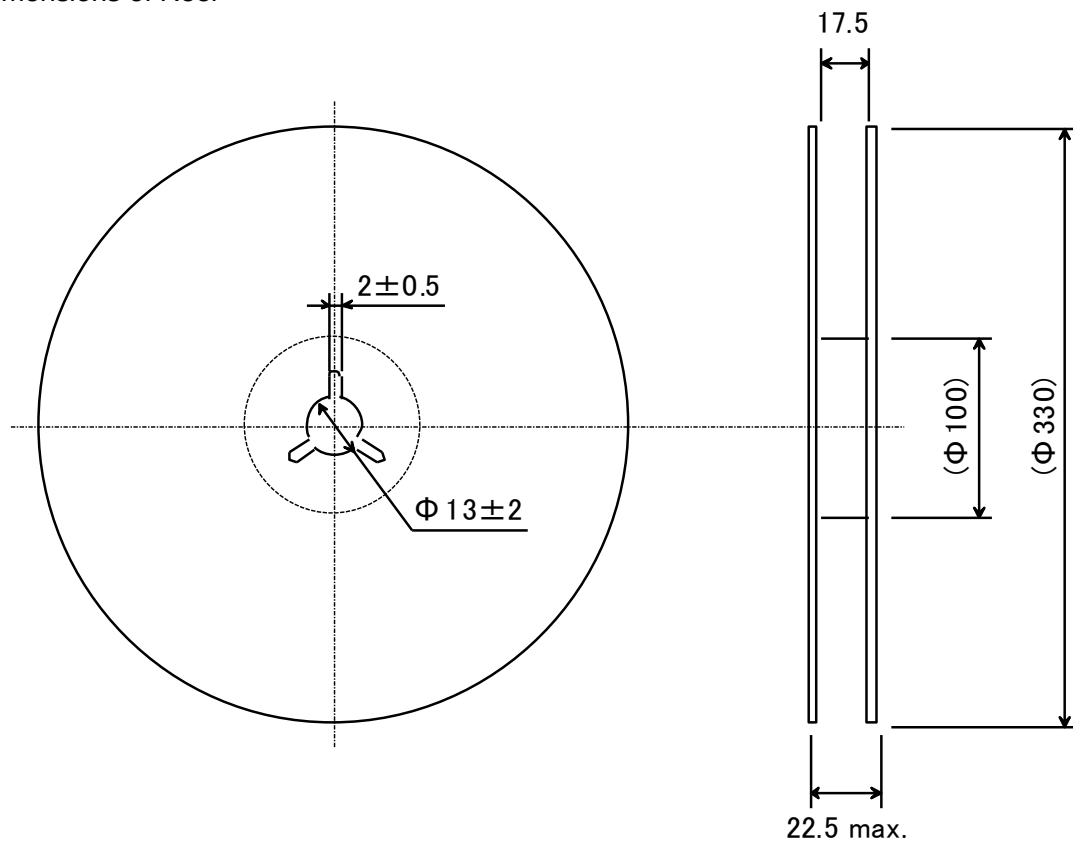
## 14. Tape and Reel Packing

### (1) Dimensions of Tape (Plastic tape)



- 1) The corner and ridge radiuses (R) of inside cavity are 0.3mm max.
- 2) Cumulative tolerance of 10 pitches of the sprocket hole is  $\pm 0.2$ mm
- 3) Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

### (2) Dimensions of Reel



(unit : mm)

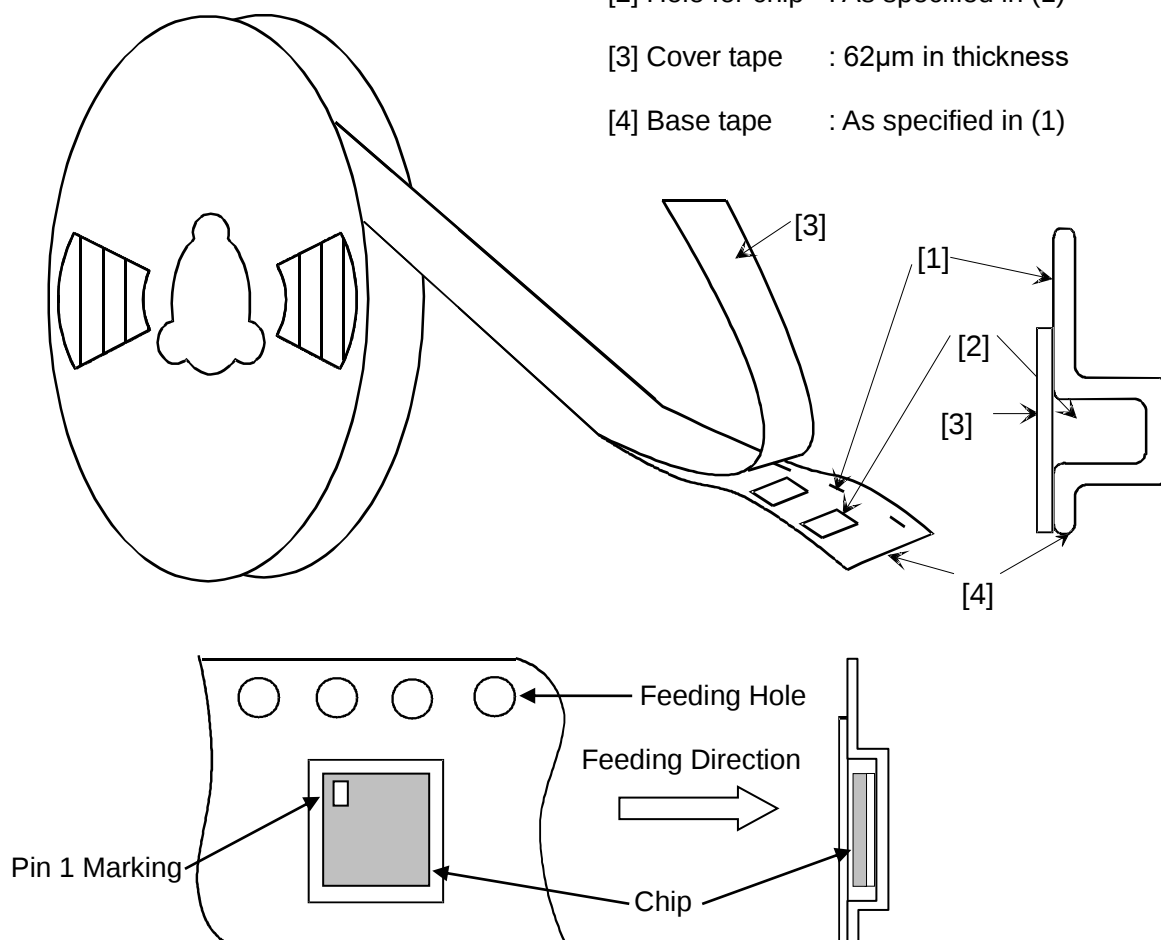
### (3) Taping Diagrams

[1] Feeding Hole : As specified in (1)

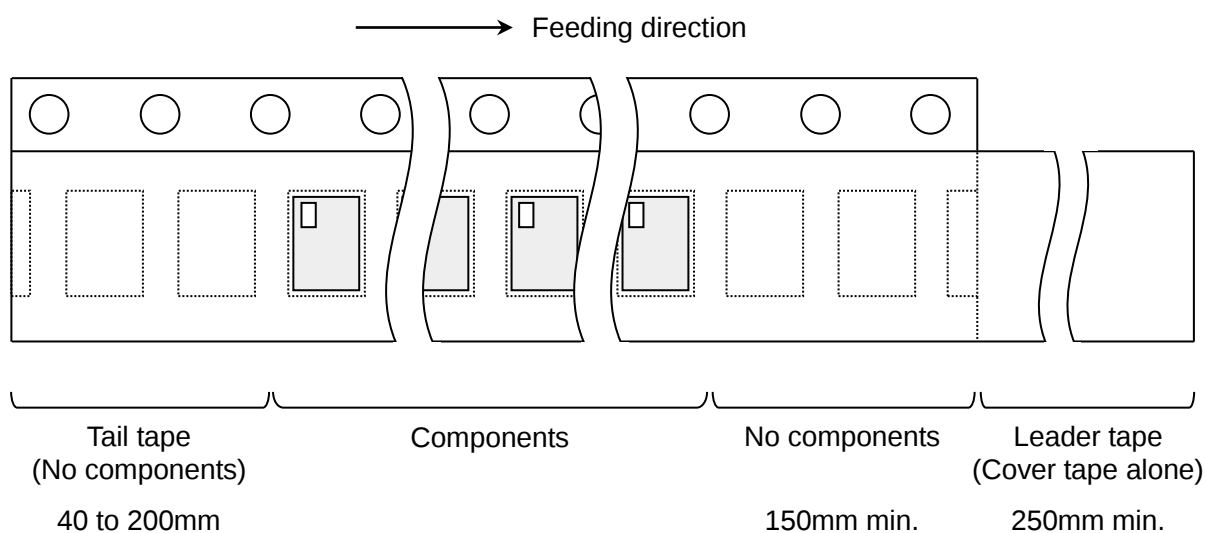
[2] Hole for chip : As specified in (1)

[3] Cover tape : 62μm in thickness

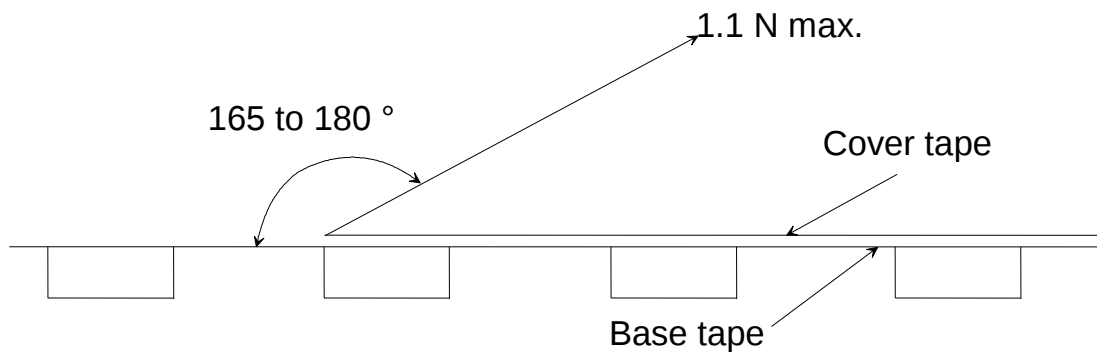
[4] Base tape : As specified in (1)



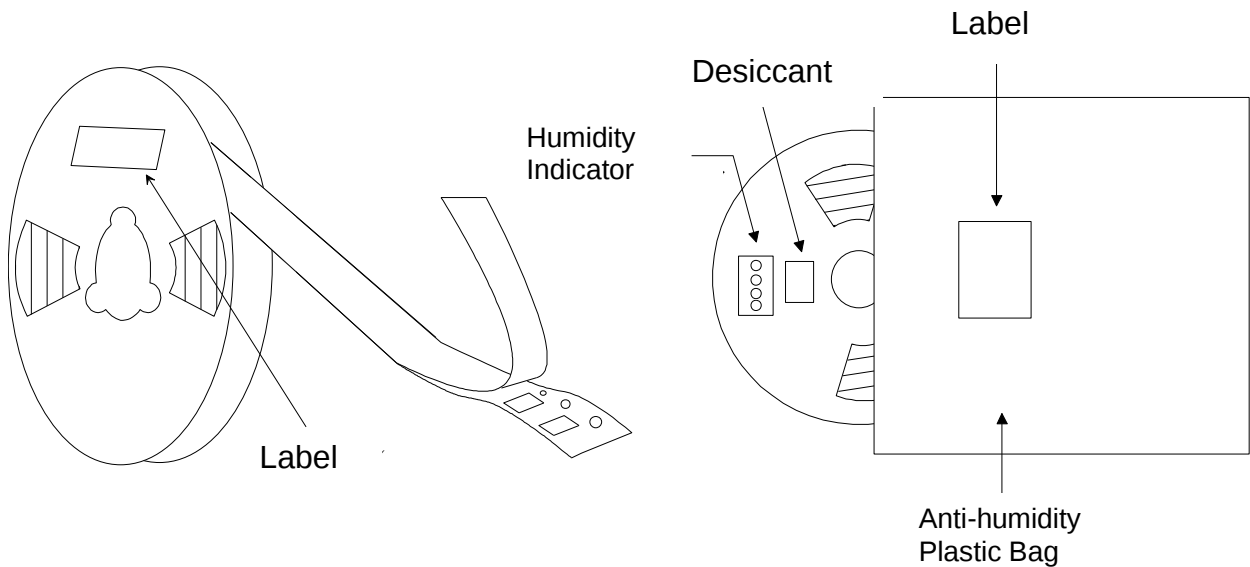
### (4) Leader and Tail tape



- (5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- (6) The cover tape and base tape are not adhered at no components area for 250mm min.
- (7) Tear off strength against pulling of cover tape : 5N min.
- (8) Packaging unit : 1000pcs./ reel
- (9) material : Base tape : Plastic  
Real : Plastic  
Cover tape, cavity tape and reel are made the anti-static processing.
- (10) Peeling of force : 1.1N max. in the direction of peeling as shown below.



- (11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

## **15. NOTICE**

### **15.1. Storage Conditions:**

Please use this product within 6month after receipt.

- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.

(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)

- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.

- The product shall be stored in non corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>2</sub>, NO<sub>x</sub>, etc.).

- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)

- After the packing opened, the product shall be stored at ≤30deg.C / ≤60%RH and the product shall be used within 168hours.

- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125+5/-0deg.C, 24hours, 1time

The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

### **15.2. Handling Conditions:**

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability and destroy by static electrical charge.

### **15.3. Standard PCB Design (Land Pattern and Dimensions):**

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

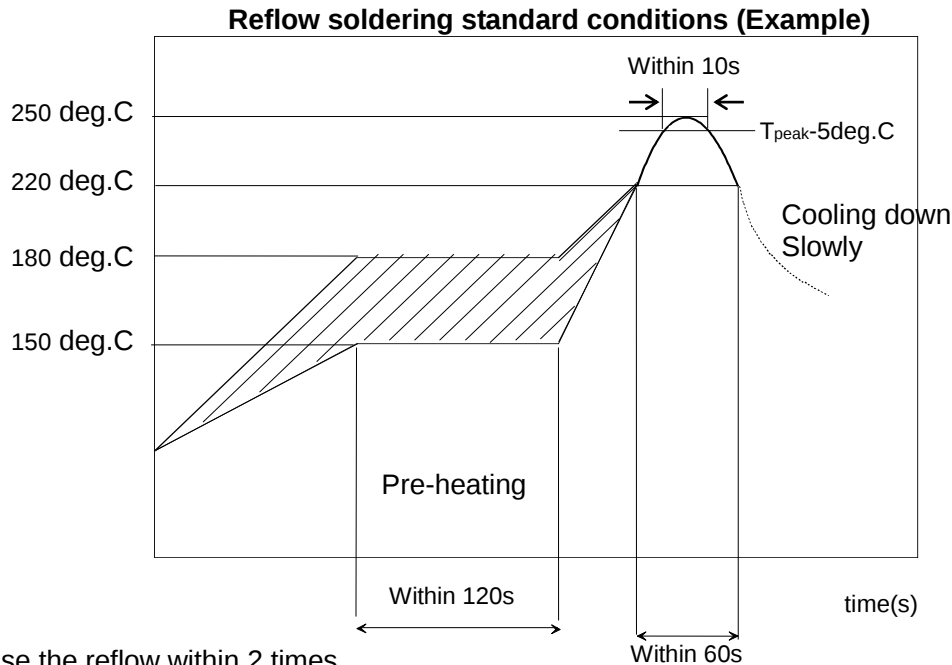
### **15.4. Notice for Chip Placer:**

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

### 15.5. Soldering Conditions:

The recommendation conditions of soldering are as in the following figure.

Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

### 15.6. Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

### 15.7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>x</sub>, NO<sub>x</sub>, etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

### 15.8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specifications.

Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

## **16. PRECONDITION TO USE OUR PRODUCTS**

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

WE HEREBY DISCLAIMS ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

You agree that you will use any and all software or program code (including but not limited to hcd, firmware, nvram, and blob) we may provide or to be embedded into our product ("Software") provided that you use the Software bundled with our product. YOU AGREE THAT THE SOFTWARE SHALL BE PROVIDED TO YOU "AS- IS" BASIS, MURATA MAKES NO REPRESENTATIONS OR WARRANTIES THAT THE SOFTWARE IS ERROR-FREE OR WILL OPERATE WITHOUT INTERRUPTION. AND MORE, MURATA MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED WITH RESPECT TO THE SOFTWARE. MURATA EXPRESSLY DISCLAIM ANY AND ALL WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE NOR THE WARRANTY OF TITLE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

You shall indemnify and hold harmless us, our affiliates and our licensor from and against any and all claims, costs, expenses and liabilities (including attorney's fees), which arise in connection with the using the Software.

The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.                      - Aerospace equipment                      - Undersea equipment.
- Power plant control equipment      - Medical equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Traffic signal equipment.              - Disaster prevention / crime prevention equipment.
- Burning / explosion control equipment
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.

Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

- the use of the engineering sample other than for evaluation purposes, particularly the installation or integration in the product to be sold by you,
- deviation or lapse in function of engineering sample,
- improper use of engineering samples.

We disclaim any liability for consequential and incidental damages.

If you can't agree the above contents, you should inquire our sales.

## APPENDIX

## 1DX Installation Manual (FCC)

FCC ID of this product is as follows.

FCC ID:VPYLB1DX

For OEM integration only – device cannot be sold to general public.

Therefore we will ask OEM to include the following statements required by FCC on the product and in the Installation manual Notice.

Contents

1. Antenna
2. Notice

### 1. Antenna

■ Please perform the antenna design that followed the specifications of the antenna.

The concrete contents of a check are the following three points.

- 1) It is the same type as the antenna type of antenna specifications.  
Confirm the same size as the Gerber file.
- 2) An antenna gain is lower than a gain given in antenna specifications.  
Measure the gain, and confirm the peak gain is less than the application value (1.4dBi)
- 3) The emission level is not getting worse.  
Measure the spurious, and confirm degradation of less than 3dB than spurious value of worst of report used for the application. However it is spurious defined below.

Please send those reports to Murata.

### 2. Notice

For OEM integration only – device cannot be sold to general public.

Therefore we will ask OEM to include the following statements required by FCC/IC on the product and in the Installation manual Notice.

Please describe the following warning on the final product which contains this module.

|                                             |
|---------------------------------------------|
| Contains Transmitter Module FCC ID:VPYLB1DX |
|---------------------------------------------|

or

|                          |
|--------------------------|
| Contains FCC ID:VPYLB1DX |
|--------------------------|

● Please describe the following warning to the manual.

|                                                                                                                                                                                                                                                                                        |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:<br>(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|                    |
|--------------------|
| <b>FCC CAUTION</b> |
|--------------------|

|                                                                                                                                                   |
|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. |
|---------------------------------------------------------------------------------------------------------------------------------------------------|

|                                                                                                           |
|-----------------------------------------------------------------------------------------------------------|
| This transmitter must not be co-located or operated in conjunction with any other antenna or transmitter. |
|-----------------------------------------------------------------------------------------------------------|

※When the product is small, as for these words mentioned above, the posting to a manual is possible.

- When installing it in a mobile equipment. Please describe the following warning to the manual.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines. This equipment should be installed and operated keeping the radiator at least 20cm or more away from person's body.

RF Exposure requirements are met when installed in mobile equipment.

This module cannot be installed in portable equipment without further testing and a change to FCC's grant of authorization.

Contact Murata regarding portable applications.

Note)

Portable equipment : Equipment for which the spaces between human body and antenna are used within 20cm.

Mobile equipment : Equipment used at position in which the spaces between human body and antenna exceeded 20cm.

**This device is intended only for OEM integrators under the following conditions:**

- 1)The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2)The transmitter module may not be co-located with any other transmitter or antenna.
- 3)The use of an antenna with gain less than 1.4 dBi.

As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed

**IMPORTANT NOTE:** In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

**End Product Labeling**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID:XXXXXXXXXX". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

**Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

## 1DX Installation Manual (IC)

IC No. of this product is as follows.

IC : 772C-LB1DX

For OEM integration only – device cannot be sold to general public.

Therefore we will ask OEM to include the following statements required by IC on the product and in the Installation manual Notice.

Contents

1. Antenna
2. Notice

### 1. Antenna

■ Please perform the antenna design that followed the specifications of the antenna.

The concrete contents of a check are the following three points.

- 1) It is the same type as the antenna type of antenna specifications.  
Confirm the same size as the Gerber file.
- 2) An antenna gain is lower than a gain given in antenna specifications.  
Measure the gain, and confirm the peak gain is less than the application value (1.4dBi)
- 3) The emission level is not getting worse.  
Measure the spurious, and confirm degradation of less than 3dB than spurious value of worst of report used for the application. However it is spurious defined below.

Please send those reports to Murata.

### 2. Notice

For OEM integration only – device cannot be sold to general public.

Therefore we will ask OEM to include the following statements required by FCC/IC on the product and in the Installation manual Notice.

Please describe the following warning on the final product which contains this module.

Contains IC:772C-LB1DX

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes :

- 1) l'appareil ne doit pas produire de brouillage;
- 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

※When the product is small, as for these words mentioned above, the posting to a manual is possible

●When installing it in a mobile equipment. Please describe the following warning to the manual.

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment and meets RSS-102 of the IC radio frequency (RF) Exposure rules. This equipment should be installed and operated keeping the radiator at least 20cm or more away from person's body.

Cet équipement est conforme aux limites d'exposition aux rayonnements énoncées pour un environnement non contrôlé et respecte les règles d'exposition aux fréquences radioélectriques (RF) CNR-102 de l'IC. Cet équipement doit être installé et utilisé en gardant une distance de 20 cm ou plus entre le radiateur et le corps humain.

RF Exposure requirements are met when installed in mobile equipment.

This module cannot be installed in portable equipment without further testing and a change to FCC's grant of authorization.

Contact Murata regarding portable applications.

Note)

Portable equipment : Equipment for which the spaces between human body and antenna are used within 20cm.

Mobile equipment : Equipment used at position in which the spaces between human body and antenna exceeded 20cm.

**This device is intended only for OEM integrators under the following conditions: (For module device use)**

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.
- 3) The use of an antenna with gain less than 1.4 dBi.

As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

**Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)**

- 1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
- 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 3 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

**IMPORTANT NOTE:**

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

**NOTE IMPORTANTE:**

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

**End Product Labeling**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC:     ".

**Plaque signalétique du produit final**

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC:     ".

**Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

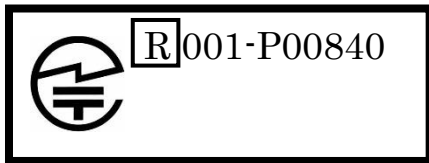
The end user manual shall include all required regulatory information/warning as show in this manual.

**Manuel d'information à l'utilisateur final**

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

■Regarding Japan Radio Certification of 1DX



This module is the product that has been authorized “Japan Radio Certification” (Certification of Construction Type) based on type approval system.

Also it is recommended to describe the following contents in the end product that is built in this module or the user manual.

[This product has built-in specified radio equipment which authorized “Japan Radio Certification” (certification number: 001-P00840) based on type approval system.]