



Foxx IQ50

Hardware Design Manual

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Revision History

Version	Date	Author	Reason for Revision
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1 Introduction

This document defines IQ50 module air interface and hardware interface for connecting the module to applications of customers.

This document can help customers quickly understand the interface specifications, electrical characteristics, mechanical specifications and related product information of IQ50 module. With the help of this document, according to our application manual and user guide, customers can quickly apply IQ50 module to wireless applications.

IQ50 wireless module is a type of wireless broadband terminal product suitable for various network standards such as TDD-LTE/FDD-LTE/5G NR SA.

IQ50 can support the following access rates:

- LTE up to: 200Mbps/75Mbps;
- FDD-5G NR up to: 223Mbps/123Mbps;

IQ50 not only provides high-speed broadband data access, but also provides voice, SMS, address book, GPS/Beidou and other functions, which can be widely used in mobile broadband access, video surveillance, security, vehicle equipment and other products.

1.1 Safety Instructions

By complying with the following safety principles, you can ensure personal safety and protect the products and working environment from potential damage:

	Driving safety first! When you drive, do not use handheld mobile terminal device unless it has a hands-free function. Please stop the car before calling!
	Please turn off the mobile terminal device before boarding. The wireless function of mobile terminal shall not be turned on in the aircraft to prevent interference with the aircraft communication system. Ignoring this reminder may affect flying safety or even violate the law.
	In hospitals or health care facilities, pay attention to whether there are restrictions on the use of mobile terminal device. RF interference will cause medical equipment to be abnormal, so mobile terminal device may need to be turned off.
	Mobile terminal device cannot always be effectively connected, for example, if the mobile device has no expense or the SIM is invalid. When you encounter the above situations in an emergency, please make an emergency call, meanwhile, ensure that your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and transmit radio frequency signals when it is turned on. There will be radio frequency interference when it is close to TV, radio, computer or other electronic equipment.
	Please keep mobile device away from inflammable gases. Please turn off the mobile terminal device when you are near a fueling station, oil depot, chemical plant or explosion site. There will be potential safety hazards when operating electronic equipment in any place with potential explosion hazard.

1.2 Purpose of the Document

This document details the basic functions, main features, hardware interfaces and usage, structural characteristics, power consumption indexes and electrical characteristics of IQ50 wireless module, and guides users to embed IQ50 module in various application terminals.

1.3 List of Contents

This document is divided into the following parts:

- Chapter 1 mainly describes safety instructions, purpose of the document and overview of contents, etc;
- Chapter 2 describes the basic functions and main features of IQ50 wireless module;
- Chapter 3 describes the functions, features and usage of each hardware interface of IQ50 in detail;
- Chapter 4 GNSS related features;
- Chapter 5 related contents and precautions of antenna interface;
- Chapter 6 describes the electrical characteristics of IQ50 in detail;
- Chapter 7 describes the structural characteristics and precautions of IQ50 in detail;
- Chapter 8 describes the storage and production considerations of IQ50 in detail;
- Chapter 9 Annex A Reference Documents and Abbreviations.

2 Product Overview

2.1 Basic Description

IQ50 is a wireless communication module that supports TDD-LTE/FDD-LTE/5G NR SA. Support 5G NR SA network data connection, and compatible LTE network data connection, can provide customers with voice (PCM), analog voice, SMS, address book and other functions. There are three series of IQ50 modules with three sub-models: IQ50-CN, IQ50-NA, and IQ50-EA. Customers can choose the model according to the region or carrier. The following lists the frequency bands supported by the CN/NA/EA models of the IQ50 module:

Table 1 IQ50 Support Frequency

Network	IQ50-CN	IQ50-NA	IQ50-EA
TDD-LTE	B34/B38/B39/B40/B41	B38/B41/B42/B43/B48	B38/B40/B41/B42/B43
FDD-LTE	B1/B3/B5/B8	B2/B4/B5/B7/B12/B13/B14/ B17/B25/B26/B30/B66/B71	B1/B3/B5/B7/B8/B20/B28
TDD-5G NR	N41/78	N38/N41/N48/N77/N78	N1/N3/N5/N7/N8/N20/N28
FDD-5G NR	N1/N5/N8/N28	N2/N5/N7/N12/N13/N14/N2 5/N26/N30/N66/N70/N71	N38/N40/N41/N77/N78
GPS L1	Support	Support	Support
GPS L5	/	Support	/

Note:

IQ50 adopts advanced and highly integrated design scheme, integrating RF and baseband on a single PCB to complete wireless receiving, transmission, baseband signal processing and audio signal processing functions. It adopts single-sided layout, the module structure size is: 32.0×29.0×2.4mm. It can meet almost M2M application requirements, such as: mobile broadband access, video surveillance, handheld terminals, vehicular devices, ultra-books and other products.

2.2 Main Performance

The following table details the performance of IQ50 module.

Table 2 Main Features of the Module

Parameter	Description
Power supply	- VBAT supply voltage range: 3.3V~4.3V - Typical supply voltage: 3.8V
Transmitting power	- Class 3 (23dBm±2dB) for TDD-5G NR bands - Class 3 (23dBm±2dB) for FDD-5G NR bands - Class 3 (23dBm±2dB) for FDD-LTE bands - Class 3 (23dBm±2dB) for TDD-LTE bands
LTE features	- Maximum support non-CA CAT4 - Support 1.4 ~ 20MHz RF bandwidth - Downlink supports multi-user MIMO - The maximum upline rate is 75Mbps and the maximum downlink rate is 200Mbps
5G NR SA features	- Supports 3GPP R17 RedCap - Supports 16-QAM, 64-QAM, 256QAM and QPSK modulation - The maximum upline rate is 123Mbps and the maximum downlink rate is 223Mbps
Network protocol features	- Support TCP/UDP/PPP/FTP/HTTP/NTP/PING /QMI protocol - Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol)
SMS	- Text and PDU mode - Point-to-point MO and MT - Cell broadcast short message - Short message storage: stored in modules by default
USIM card interface	Support 2 channel USIM/SIM card: 1.8V and 3V
Audio features	- Support 1 digital audio interface: PCM interface - LTE: AMR/AMR-WB
PCM interface	- Audio frequency use, need to external codec chip. - Supports 8-bit A-law, u-law and 16-bit linear encoding formats - Supports long frame mode and short frame mode - Master mode and slave mode are supported, but can only be used as master mode in long frames
USB interface	- Compatible with USB2.0 specifications. Maximum transmission rate up to 480Mbps - For AT command, data transfer, GNSS NMEA output, software debugging and upgrade - USB driver: Support Windows XP, Windows Vista, Windows7, Windows 8/8.1, Windows10, Windows CE 5.0/6.0/7.0, Linux 2.6 and

later version, Android 2.3/4.0/4.2/4.4/5.0

Serial port	Master serial port: ● Used for AT command and data transmission ● The maximum baud rate is 460800bps, and the default is 115200bps ● Support RTS and CTS hardware flow control Debug serial port: ● Used for Linux control, log output ● The baud rate is 115200bps
RX-diversity	● Support LTE/5G NR RX diversity
AT command	● Compliant with 3GPP TS 27.007 and 27.005, support AT command
Network indication	● NET_STATUS, NET_MODE these two pins indicate network status
Antenna interface	● Include main antenna (ANT_MAIN), RX-diversity antenna (ANT_DIV) and GNSS antenna (ANT_GNSS)
Physical properties	● Size: 32.0×29.0×2.4mm ● Weight: 5.16g
Temperature range	● Normal working temperature: -30℃~+75℃ ● Extended working temperature: -40℃~+85℃ ● Storage temperature: -45℃~+90℃
Software upgrade	● USB interface
RoHS	● All devices comply fully with EU RoHS standards
Ambient humidity	● 5%~95%
ESD	● VBAT, GND: Air discharge±10KV, Contact discharge±5KV ● Ant interface: Air discharge±8KV, Contact discharge±4KV ● Other interface: Air discharge±1KV, Contact discharge±0.5KV
Power consumption	● Shutdown leakage current: 114uA ● Bottom current: 1.93mA ● Sleep mode: 2.01mA ● Idle mode: 30.78mA ● Data mode: 326.45mA
Interface	● 204 pins LGA interface
LGA functional Interface	● Power interface ● Hardware reset interface ● USB2.0 High-Speed interface ● USIM/SIM card interface (support 3V、1.8V) ● UART interface ● ADC interface ● PCM interface ● I2C interface ● SPI interface

- PCIe interface
- SGMII interface
- SDIO interface*
- Indicator light interface
- Sleep control interface
- Flight mode control interface

*SDIO interface, under development, temporarily not supported.

2.3 Functional Block Diagram

The following is a block diagram of IQ50, which elaborates its main functional parts.

- Power management
- Baseband chip
- DDR+NAND memory
- RF part
- Peripheral interface

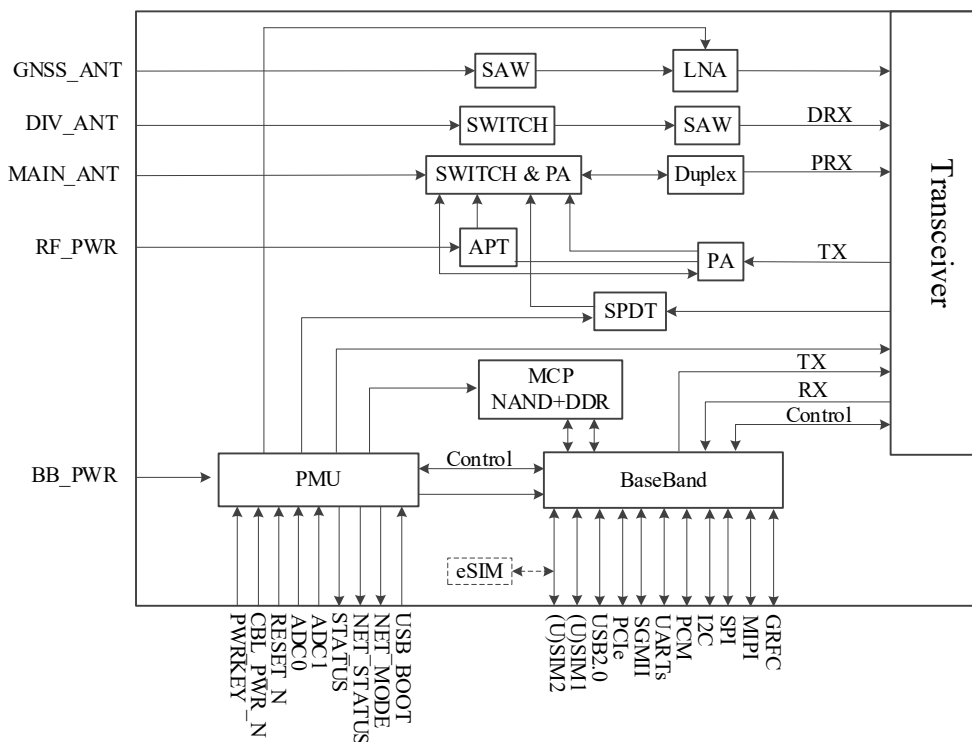


Figure 1 Functional Block Diagram

2.4 Evaluation Board

To help test and use IQ50 module, FOXX provides a set of evaluation board. Evaluation board tools include USB data cable, antenna and other peripherals.

For details on how to use the evaluation board, please refer to the *IQ50_EVB User Manual*.

3 Application Interface

3.1 Basic Description

IQ50 has 204 pins, and provides the following functional interfaces:

- Power interface
- Hardware reset interface
- USB interface
- USIM/SIM interface
- UART interface
- ADC interface
- PCM interface
- I2C interface
- SPI interface
- PCIe interface
- SGMII interface
- SDIO interface*
- Indicator light interface
- Sleep control interface
- Flight mode control interface

3.2 LGA Card Interface Definition

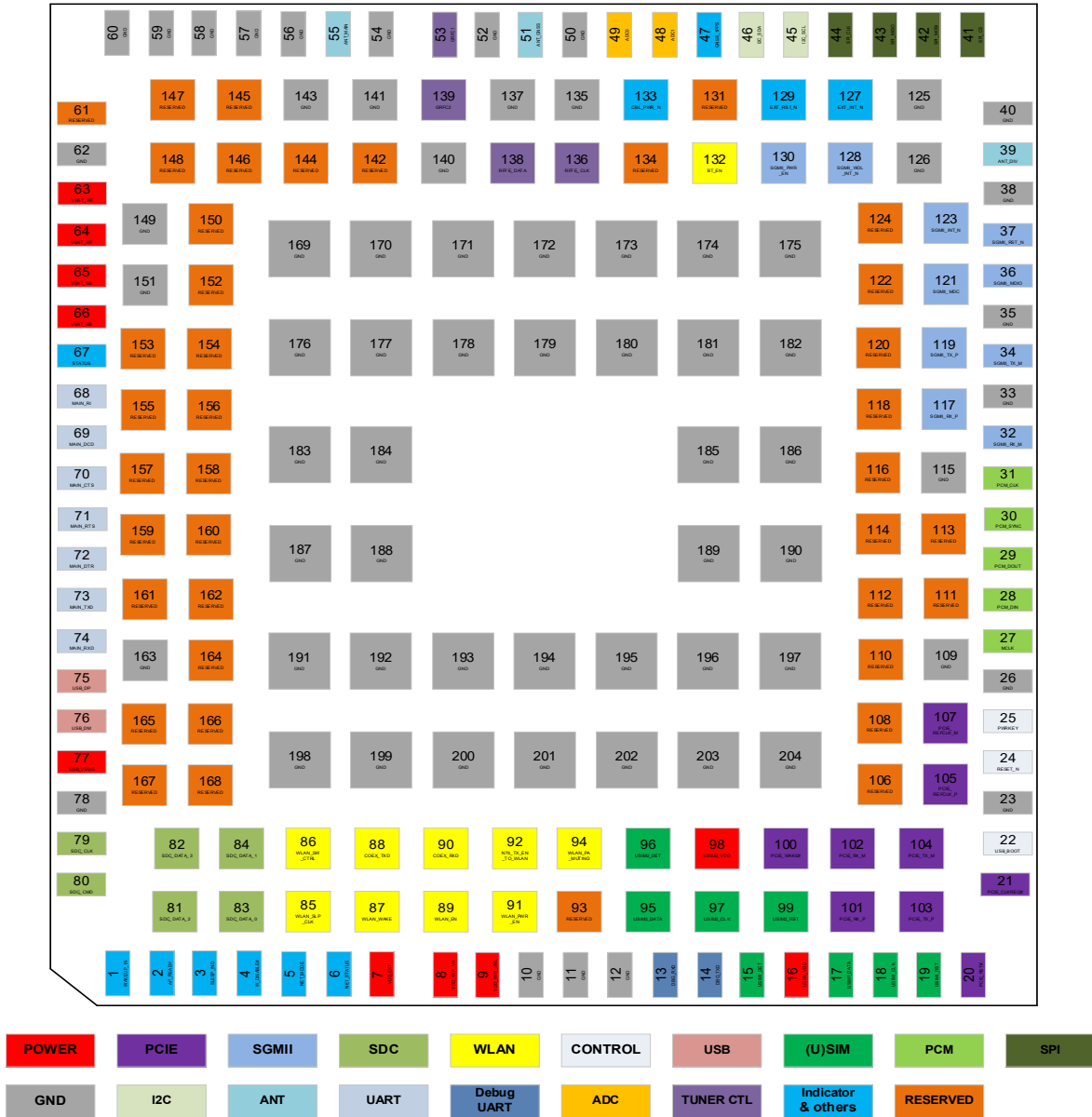


Figure 2 Module NUMBER Pin Diagram

3.3 Pin Description

The table below shows the definition of each pin of the IQ50 module.

Table 3 IO Parameter Definition

Type	Description
IO	Input and output two-way signal
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open-drain output signal

Table 4 Pin Description

Power					
Pin Name	Pin No.	I/O	Description	DC Features	Remarks
VBAT_BB	65, 66	PI	Module baseband power supply	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide the current up to 1A.
VBAT_RF	63, 64	PI	Module RF power supply	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide the current up to 2A.
VDD_EXT	7	PO	Module output 1.8V	Vnorm=1.8V I _o max=50mA	It can provide pull-up for external GPIO. If unused, keep it open.
VDD_WIFI_VH	8	PO	Module output WiFi power supply	-	Can power external WiFi chips

VDD_WIFI_VML	9	PO	Module output WiFi power supply	-
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Ground

Pin Name	Pin No.	Remarks
GND	10~12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56~60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141, 143, 149, 151, 163, 169~204	-

On / Off / Reset

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
PWRKEY	25	DI	Module on/off	-	1.5 V power domain, internal pull-up
CBL_PWR_N	133	DI	Ground trigger automatic start	-	When grounded, it can be powered on automatically, internal pull-up, if not used, it is recommended to reserve test points
RESET_N	24	DI	Reset module	-	1.5V power domain, active low level, internal pull-up, if not used, it is recommended to reserve test points

Module Status Indication

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
STATUS	67	OD	Indicate the running status of the module	-	External pull-up is required, disconnect when not in use.
NET_MODE	5	DO	Indicate the network registry status of the module	VDD_EXT	Disconnect when not in use.
NET_STATUS	6	DO	Indicate the network operation status of the module	VDD_EXT	Disconnect when not in use.

USB Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
USB_VBUS	77	PI	USB detection	Vmax=5.25V Vmin=3.3V Vnorm=5.0V	It is recommended to reserve test points.
USB_DP	75	IO	USB differential data positive signal	Compliant with USB2.0 specifications	90Ω differential impedance is required. It is recommended to reserve test points.
USB_DM	76	IO	USB differential data negative signal	Compliant with USB2.0 specifications	90Ω differential impedance is required. It is recommended to reserve test points.

USIM Card Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
USIM1_VDD	16	PO	USIM 1 card power supply	Low level: Vmin=1.26V Vnom=1.8V Vmax=2.1V High level: Vmin=2.06V Vnom=3.0V Vmax=3.25V	Module automatically identifies 1.8V or 3.0V USIM card
USIM1_DATA	17	IO	USIM1 card data	USIM1_VDD	Internal pull-up via 10 kΩ resistor
USIM1_CLK	18	DO	USIM1 card clock	USIM1_VDD	-
USIM1_RST	19	DO	USIM1 card reset	USIM1_VDD	-
USIM1_DET	15	DI	USIM1 card detection	VDD_EXT	Disconnect when not in use.
USIM2_VDD	98	PO	USIM2 card power supply	Low level: Vmin=1.26V Vnom=1.8V Vmax=2.1V High level: Vmin=2.06V Vnom=3.0V Vmax=3.25V	Module automatically identifies 1.8V or 3.0V USIM card
USIM2_DATA	95	IO	USIM2 card data	USIM2_VDD	Internal pull-up via 10 kΩ resistor
USIM2_CLK	97	DO	USIM2 card clock	USIM2_VDD	-

USIM2_RST	99	DO	USIM2 card reset	USIM2_VDD	-
USIM2_DET	96	DI	USIM2 card detection	VDD_EXT	Disconnect when not in use.

Primary Serial Port

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
MAIN_RI	68	DO	Module output ringing prompt	VDD_EXT	Disconnect when not in use.
MAIN_DCD	69	DO	Module output carrier detection	VDD_EXT	Disconnect when not in use.
MAIN_CTS	70	DO	Module clear send	VDD_EXT	CTS connected to MCU, disconnect when not in use.
MAIN_RTS	71	DI	DTE Request to Send Data	VDD_EXT	RTS connected to MCU, disconnect when not in use..
MAIN_DTR	72	DI	DTE ready, sleep mode control	VDD_EXT	Disconnect when not in use.
MAIN_TXD	73	DO	Module sending data	VDD_EXT	Disconnect when not in use.
MAIN_RXD	74	DI	Module receiving data	VDD_EXT	Disconnect when not in use.

Debug Serial Port

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
DBG_TXD	14	DO	Module transmits data	VDD_EXT	It is suggested to reserve test points, disconnect when not in use.
DBG_RXD	13	DI	Module receives data	VDD_EXT	It is suggested to reserve test points, disconnect when not in use.

ADC Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
ADC0	49	AI	Universal analog-to-digital conversion	0V~VBAT_BB	Disconnect when not in use.
ADC1	48	AI	Universal analog-to-digital conversion	0V~VBAT_BB	Disconnect when not in use.

PCM Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
MCLK	27	DO	CODEC master clock	VDD_EXT	Disconnect when not in use.
PCM_DIN	28	DI	PCM input data	VDD_EXT	Disconnect when not in use.
PCM_DOUT	29	DO	PCM data output	VDD_EXT	Disconnect when not in use.
PCM_SYNC	30	IO	PCM data synchronization signal	VDD_EXT	Disconnect when not in use.
PCM_CLK	31	IO	PCM clock	VDD_EXT	Disconnect when not in use.

I2C Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
I2C_SCL	45	OD	I2c clock	VDD_EXT	External pull-up required, disconnect when not in use.
I2C_SDA	46	OD	I2c data	VDD_EXT	External pull-up required, disconnect when not in use.

PCIe Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
PCIE_RX_P	101	AI	PCIe data reception positive signal	-	85Ω differential impedance required, 220nF capacitor connected in series near PHY chip end
PCIE_RX_M	102	AI	PCIe data reception negative signal	-	
PCIE_TX_P	103	AO	PCIe data transmission positive signal	-	85Ω differential impedance required, 220nF capacitor connected in series near module end
PCIE_TX_M	104	AO	PCIe data transmission negative signal	-	
PCIE_CLK_P	105	AIO	PCIe clock positive signal	-	85Ω differential impedance required
PCIE_CLK_M	107	AIO	PCIe clock negative signal	-	
PCIE_RST_N	20	DIO	PCIe reset signal	VDD_EXT	-

PCIE_CLKREQ_N	21	DIO	PCle clock request signal	VDD_EXT	-
PCIE_WAKE_N	100	DIO	PCle wake-up signal	VDD_EXT	-

Coexistence and Control Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
WLAN_EN	89	DO	WLAN enable control	VDD_EXT	-
BT_EN	132	DO	BT enable control	VDD_EXT	Active high
WLAN_SLP_CLK	85	DO	WLAN sleep clock	VDD_EXT	-
WLAN_PWR_EN	91	DO	WLAN power enable control	VDD_EXT	Active high
WLAN_WAKE	87	DI	WLAN wake up module	VDD_EXT	-
COEX_RXD	90	DI	5G/LTE/WLAN& BT coexistence received signal	VDD_EXT	-
COEX_TXD	88	DO	5G/LTE/WLAN& BT coexistence transmission signal	VDD_EXT	-
N79_TX_EN_TO_WLAN	92	DO	Notification n79 transmitted from SDR Lost to WLAN	VDD_EXT	-
WLAN_PA_MUTING	94	DO	SDX control turn off WLAN PA	VDD_EXT	-
WLAN_SW_CTRL	86	DI	WiFi clock request	VDD_EXT	-

SPI Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
SPI_CS	41	DO	SPI chip select	VDD_EXT	Only main mode is supported
SPI_MOSI	42	DO	SPI master output slave input	VDD_EXT	Only main mode is supported
SPI_MISO	43	DI	PI master input slave output	VDD_EXT	Only main mode is supported

SPI_CLK	44	DO	SPI clock	VDD_EXT	Only main mode is supported
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SGMII Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
SGMII_RST_N	37	DO	SGMII regeneration	VDD_EXT	Disconnect when not in use.
SGMII_INT_N	123	DI	SGMII 中断信号	VDD_EXT	-
SGMII_WOL_INT_N	128	DI	SGMII Remote Wake-Up Interrupt Signal	VDD_EXT	-
SGMII_PWR_EN	130	DO	SGMII PHY Power Enable	VDD_EXT	-
SGMII_MDIO	36	IO	SGMII MDIO	VDD_EXT	Disconnect when not in use.
SGMII_MDC	121	DO	Sgmii mdio time	VDD_EXT	Disconnect when not in use.
SGMII_TX_P	119	AO	SGMII data Send a positive signal	-	90Ω differential impedance required, 100nF capacitor connected in series near module end
SGMII_TX_M	34	AO	SGMII data Send a negative signal	-	
SGMII_RX_P	117	AI	SGMII data receive positive signal	-	90Ω differential impedance required, 100nF capacitor connected in series near PHY chip end
SGMII_RX_M	32	AI	SGMII data receive negative signal	-	

RF Interface/Antenna Control Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
ANT_DIV	39	AI	Diversity antenna	-	50Ω characteristic impedance required, disconnect when not in use.
ANT_MAIN	55	AIO	Main antenna	-	50Ω characteristic impedance required, disconnect when not in use.
ANT_GNSS	51	AI	GNSS antenna	-	50Ω characteristic impedance

					required, disconnect when not in use.
RFFE_CLK	136	DO	MIPI clock	VDD_EXT	-
RFFE_DATA	138	DIO	MIPI data	VDD_EXT	-
GRFC1	53	DO	Radio-frequency control	VDD_EXT	Disconnect when not in use.
GRFC2	139	DO	Radio-frequency control	VDD_EXT	Disconnect when not in use.

GPIO Interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
WAKEUP_IN	1	DI	module wake-up control	VDD_EXT	High wake-up module, disconnect when not in use.
AP_READY	2	DI	Application Processor Sleep State Detection	VDD_EXT	Disconnect when not in use.
WAKEUP_OUT	3	DO	Module sleep status indication	VDD_EXT	Disconnect when not in use.
W_DISABLE_N	4	DI	Flight mode controls	VDD_EXT	Default pull-up; low, module goes into flight mode, disconnect when not in use.
GNSS_1PPS	47	DO	Support timing and relay functions; support 1PPS pulse output and frame synchronization	VDD_EXT	Disconnect when not in use.
EXT_INT_N	127	DI	External audio interrupt input	VDD_EXT	Disconnect when not in use.
EXT_RST_N	129	DO	External audio reset control	VDD_EXT	Disconnect when not in use.

SDIO Interface*

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
SDC_CLK	79	DO	WLAN SDIO signal clock	-	50Ω impedance required, disconnect when not in use.

SDC_CMD	80	IO	WLAN SDIO signal instruction	-	50Ω impedance required, disconnect when not in use.
SDC_DATA_3	82	IO	WLAN SDIO Signal data line 3	-	50Ω impedance required, disconnect when not in use.
SDC_DATA_2	81	IO	WLAN SDIO Signal data line 2	-	50Ω impedance required, disconnect when not in use.
SDC_DATA_1	84	IO	WLAN SDIO Signal data line 1	-	50Ω impedance required, disconnect when not in use.
SDC_DATA_0	83	IO	WLAN SDIO Signal data line 0	-	50Ω impedance required, disconnect when not in use.

DLOAD interface

Pin Name	Pin No.	I/O	Description	DC Features	Remarks
USB_BOOT	22	DI	Forced download mode control	VDD_EXT	Do not pull up to high level until startup is successful. It is recommended to reserve test points

Reserve Pin

Pin Name	Pin No.	Remarks
RESERVED	61, 93, 106, 108, 110~114, 116, 118, 120, 122, 124, 131, 134, 142, 144~148, 150, 152~162, 164~168	Keep it open

*SDIO interface, under development, temporarily not supported.

3.4 Working Modes of the Module

Table 5 Working Modes

Modes	Description	
TDD-LTE mode	TDD-LTE IDLE	The module is ready for TDD-LTE data transmission. But no data is being sent or received at this time. Module power consumption depends on network Settings

	TDD-LTE DATA	In TDD-LTE data transmission, module power consumption depends on network Settings (such as power control level), data uplink and downlink rates, and TDD-LTE related Settings
FDD-LTE mode	FDD-LTE IDLE	The module is ready for FDD-LTE data transmission. But no data is being sent or received at this time. Module power consumption depends on network Settings
	FDD-LTE DATA	In FDD-LTE data transmission, module power consumption depends on network Settings (such as power control level), data uplink and downlink rates, and FDD-LTE related Settings
5G mode	5G IDLE	The module is ready for 5G data transmission. However, there is no data transmission at this time. Module power consumption depends on network settings.
	5G DATA	In 5G data transmission, module power consumption depends on network settings (such as power control level), data uplink and downlink rates, and 5G related settings.
Minimum function mode	VBAT is continuously powered. Use AT+CFUN=0 to make the module enter the minimum function mode. RF transceiver of the module is turned off. Use the AT+CFUN=1 module to re-open the transceiver registration network to normal function mode	
Flight mode	Use AT+CFUN=4 or pull down the W_DISABLE_N pin to set the module to flight mode. In this mode, the RF does not work.	
Sleep mode	In this mode, the power consumption of the module is reduced to a very low level, but the module can still receive paging, SMS, phone, and TCP/UDP data	
Power off mode	VBAT Low voltage shutdown. In this mode, the PMU stops supplying power to baseband (BB) and radio frequency (RF), the software stops working, and the serial port is disconnected	

3.5 Energy Saving Function

3.5.1 Sleep Mode

In sleep mode, IQ50 can reduce power consumption to the lowest level. The following sections will detail the sleep mode of IQ50.

3.5.1.1 UART Application

If the module and MCU communicate via UART, the following conditions need to be met simultaneously to put the module into sleep mode:

- Execute AT+WAKEUPCFG=1 command Keep WAKEUP_IN low or unconnected.
- Keep MAIN_DTR low level.

The reference circuit is as below:

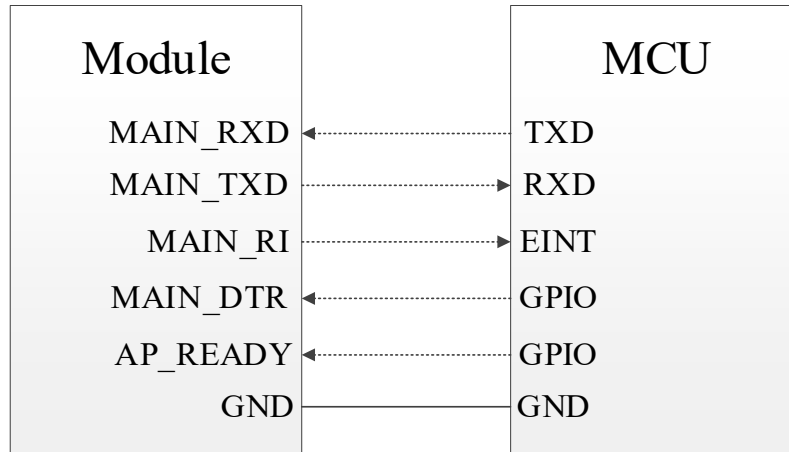


Figure 3 UART Application in Sleep Mode

- Wake-up module by MCU pulling HIGH MAIN_DTR of module.
- When the module has URC to report, MAIN_RI signal will wake up MCU.
- AP_READY detects the sleep state of MCU, which can be configured as high level or low level detection.

3.5.1.2 USB Suspend and Wake Applications Supported

If the host "supports USB suspend and wake up and USB remote wake up function" and "supports USB suspend and wake up and MAIN_RI function", the following conditions shall be met at the same time to make the module enter sleep mode:

- Execute AT+WAKEUPCFG=1 command.
- Keep MAIN_DTR low level.
- The host USB bus connected to the module's USB interface enters a suspended state.

3.5.1.2.1 Support USB Suspend and Wake Up and USB Remote Wake Up Function

If the host supports USB suspend and wake-up, and USB remote wake-up.

The reference circuit is as below:

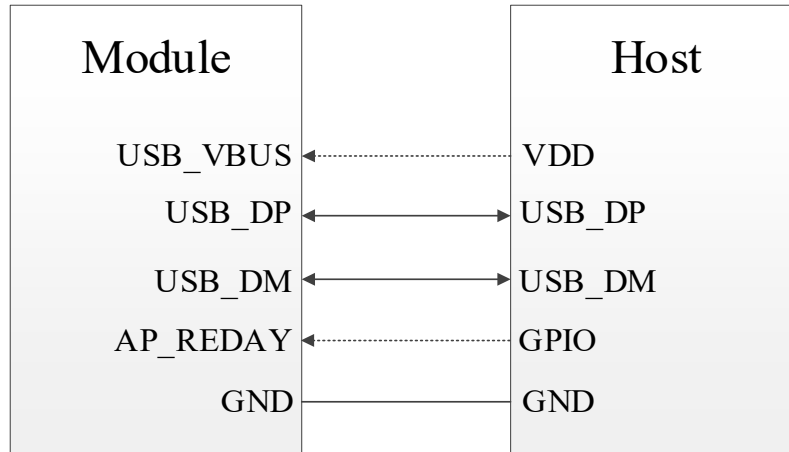


Figure 4 Application with USB Remote Wake-up Function in Sleep Mode

- Sending data to the module via USB will wake up the module
- When the module has a URC report, the module sends a remote wake-up signal over the USB bus to wake up the host.

3.5.1.2.2 Support USB Suspend and Wake Up and MAIN_RI Function

If the host supports USB suspend and wake-up, but does not support USB remote wake-up function, it is necessary to wake up the host with the MAIN_RI signal of the module.

The reference circuit is as below:

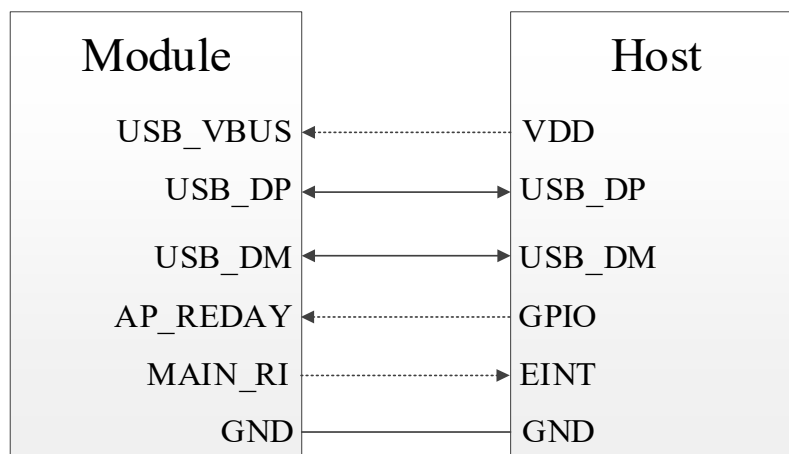


Figure 5 Application of MAIN_RI Function in Sleep Mode

- Sending data to the module via USB will wake up the module.
- When the module has URC report, the module will wake up the host through MAIN_RI signal.

3.5.1.3 USB Suspend is not Supported

If the host does not support USB suspend function, the following conditions must be met at the same time to put the module into sleep mode:

- Execute AT+WAKEUPCFG=1 command.
- Keep MAIN_DTR low level.
- Disconnect USB_VBUS power.

The reference circuit is as below:

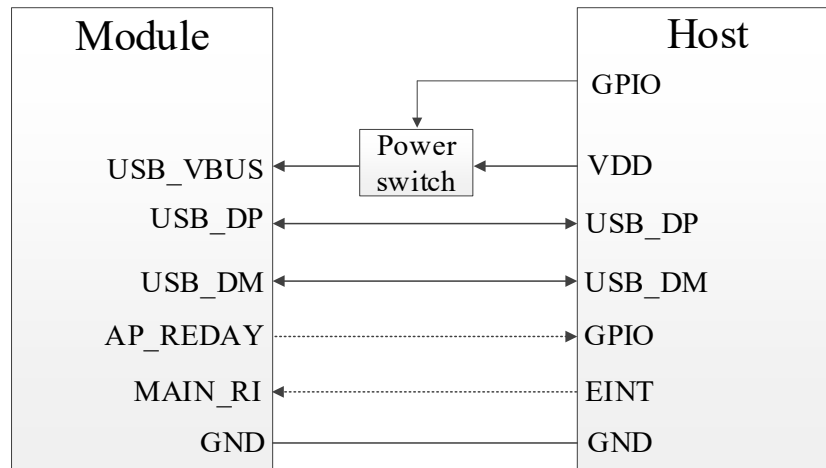


Figure 6 Sleep Applications that do not Support Suspend Function

- The module will wake up by restoring USB_VBUS power.

3.5.2 Flight Mode

When the module enters flight mode, the RF function is disabled and all AT commands related to radio frequency are not accessible. The module can enter the flight mode through hardware interface and software command control.

3.5.2.1 Hardware I/O Interface Controls Flight Mode

A low level signal is given to the module via the W_DISABLE_N Pin (Pin 4) of the IQ50 and the module enters flight mode, at which point the RF transceiver unit stops working. Pull up Pin4 and the module will enter normal mode again.

Module control signal levels support 1.8V logic levels.

3.5.2.2 AT Command Controls Flight Mode

Send AT+CFUN=4, the module will enter flight mode, at which time the RF transceiver unit will stop

working. Send AT+CFUN=1 and the module will re-enter normal mode.

3.6 Power Supply Design

3.6.1 Pin Description

This section describes the interface related to power supply and power-off. The interfaces involved are as follows:

Table 6 Power Related Interface

Pin name	Pin No.	Description	Min	Typical	Max	Unit
VBAT_BB	65, 66	Module baseband power supply	3.3	3.8	4.3	V
VBAT_RF	63, 64	Module RF Power supply	3.3	3.8	4.3	V
VDD_EXT	7	Output 1.8V	-	1.8	-	V
GND	10, 11, 12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56~60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141, 143, 149, 151, 163, 169~204	ground	-	0	-	V

3.6.2 Reduce Voltage Drop

IQ50 power supply range is 3.3V~4.3V, in the data transmission or call, the instantaneous high-power emission will form a peak current, resulting in large ripple, such as the instantaneous voltage drop caused by the supply voltage is too low, the module will shut down. To ensure the normal operation of the module, the power supply must have sufficient power supply capability. Ensure that the input voltage is not lower than 3.3V. The following figure is the voltage drop during burst transmission under 4G and 5G networks.

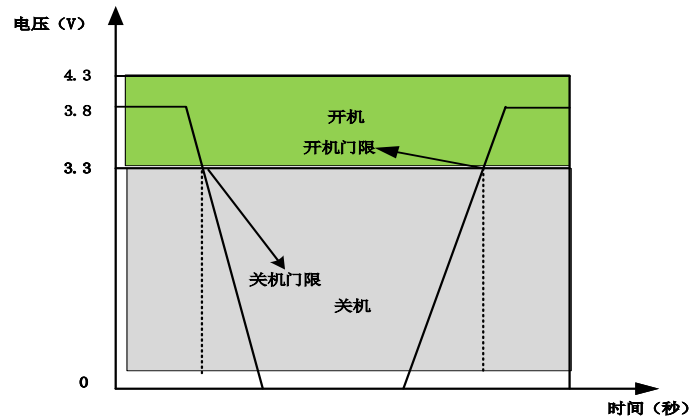


Figure 7 Burst Transmission Power Requirements

The graph below is the voltage drop when registering a burst transmission under the network.

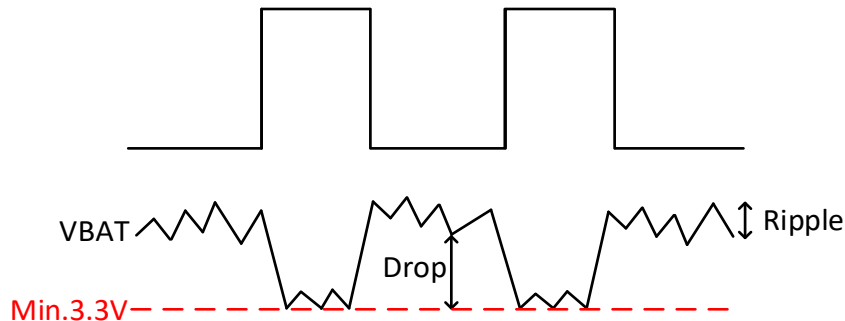


Figure 8 Power Requirements of Burst Transmission

To reduce voltage drop, 100uF filter capacitors with low ESR are needed. The chip multilayer ceramic capacitor (MLCC) has the best ESR. It is recommended to add three ceramic capacitors (100nF, 33pF, 10pF) to the VBAT_BB and VBAT_RF pins respectively, and the capacitors should be placed near the VBAT pins.

At the same time, in order to ensure better power supply performance, a TVS tube is added near the module VBAT input to improve the surge voltage tolerance of the module. The recommended model is SYT01S05DWC. If VBAT has high-frequency interference, it is recommended to add magnetic bead filtering. The recommended magnetic bead is MGLB3216M601T2R0-LF. When external power supplies are connected to modules, VBAT_BB and VBAT_RF must use star cabling. The cable width of each network should not be less than 2mm. In principle, the longer the VBAT line, the wider the line width.

The reference circuit is as follows:

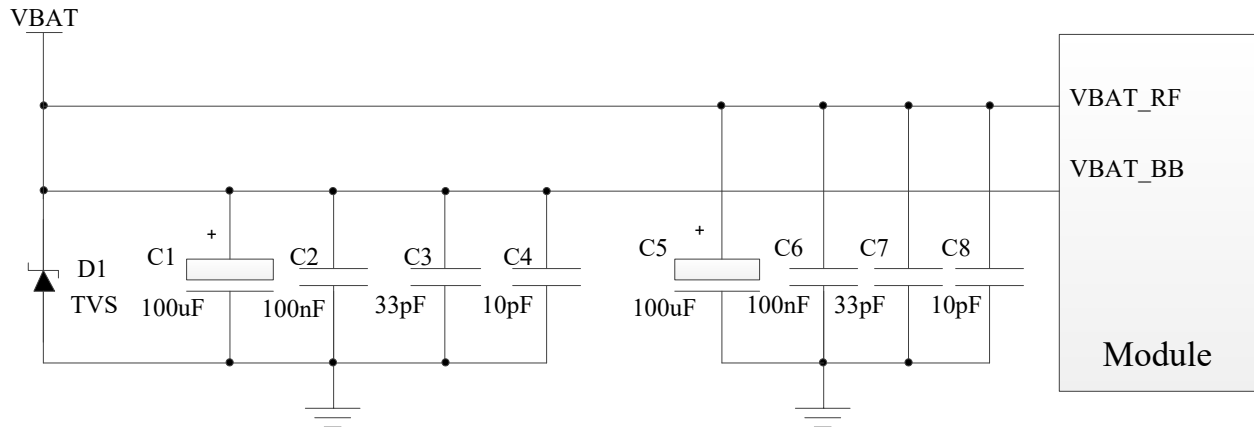


Figure 9 Power Supply Circuit of Module

3.6.3 Power Supply Reference Circuit

The design of the module power supply is very important because a large part of the performance of the module depends on the power supply. The power supply can provide at least 2A current. If the voltage difference between input and output is not very large, it is recommended to use LDO power supply module; If the voltage difference between input and output is large, the DCDC is preferred as the power supply.

The diagram below shows a reference design +5V input power supply, the design output voltage is +3.8V (typical value 3.8V), and the maximum load current is 3A.

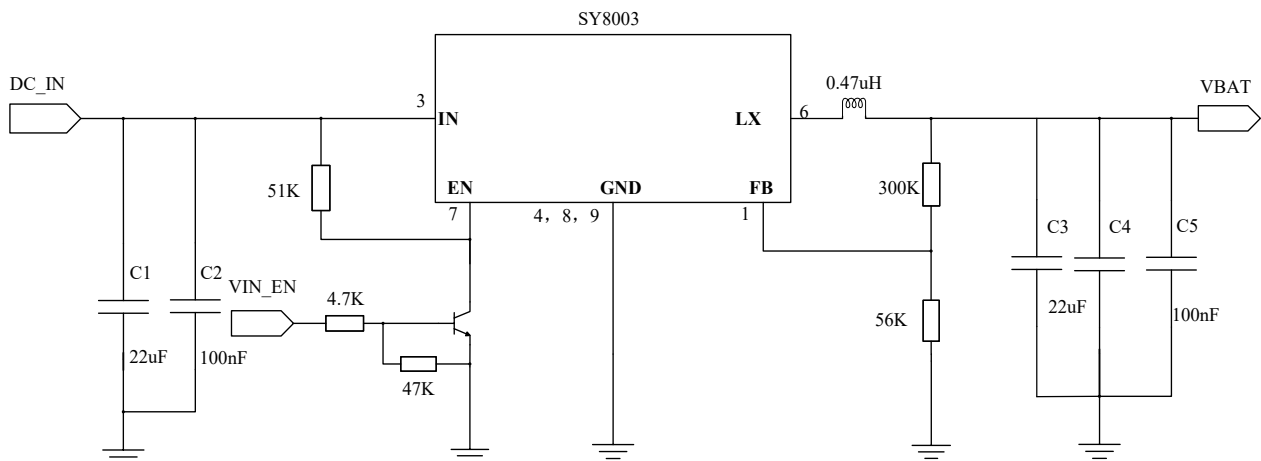


Figure 10 DC Supply Circuit

3.6.4 VDD_EXT Voltage Output

When the IQ50 module is powered on normally, there is a voltage output on the Pin7, the output voltage is 1.8V, and the current load is 50mA. This output voltage can be used for external power supply, such as

level reference, and the level state of the Pin can also be read to determine whether the module is powered on.

3.7 Power on/off

IQ50 supports the power-on mode by pressing the button. Users can judge whether the module is powered on by querying whether the VDD_EXT pin outputs a high level.

3.7.1 PWRKEY Pin Power On

Table 7 PWRKEY Pin Description

Pin name	No.	I/O	Description	Remark
PWRKEY	25	DI	Module on/off	1.5 V power domain, internal pull-up

IQ50 module is in power off mode and can be turned on by depressing the PWRKEY by at least 500ms. An open set drive circuit is recommended to control the PWRKEY pins., with the following reference circuit:

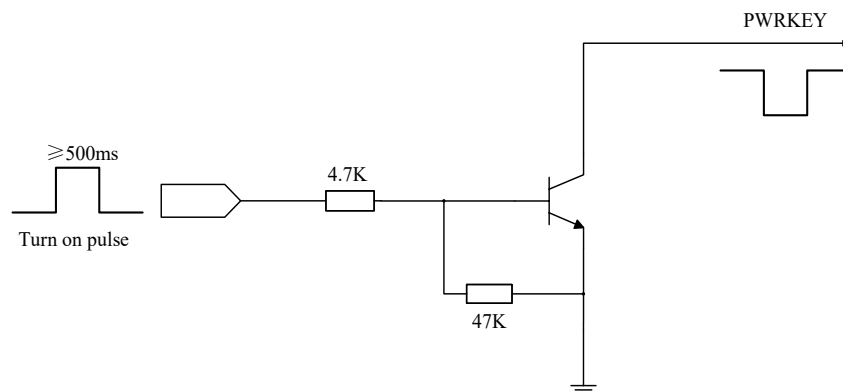


Figure 11 Reference Starting Circuit of Open-Collector Drive

Another way to control PWRKEY pin is to use a button switch directly. A TVS shall be placed near the button for ESD protection. The reference circuit is as below:

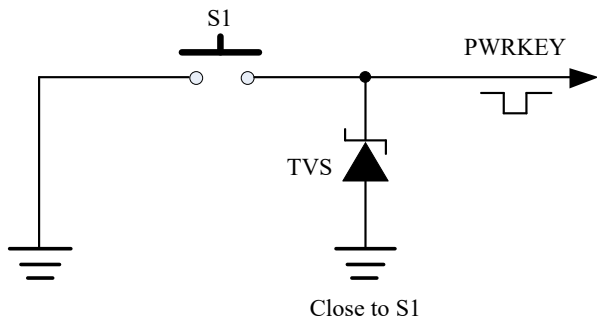


Figure 12 Reference Circuit of Starting by Button

The power on sequence is shown in the figure below

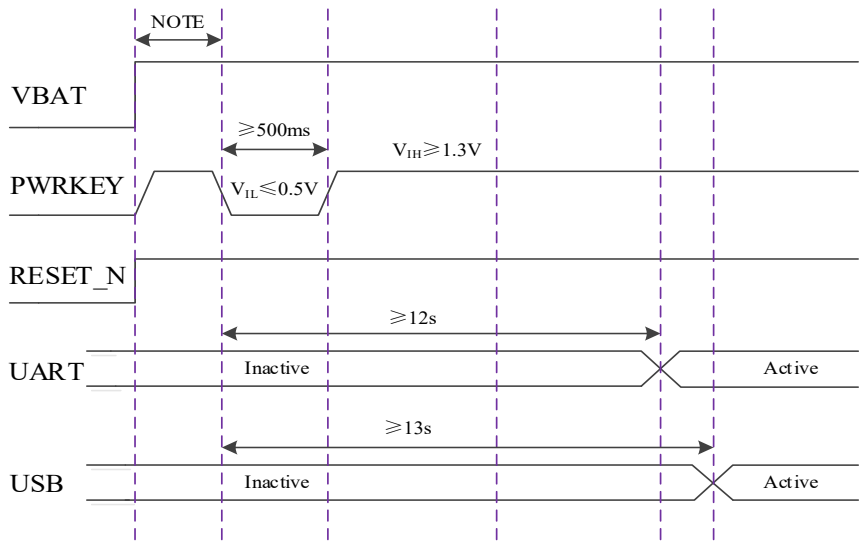


Figure 13 Power-on Sequence Diagram

Note: Tnote > 30ms.

3.7.2 Power Off

When the module is powered on, pull down the PWRKEY pin for at least 500ms and release it. The module will execute the power off process. Power off timing is shown below:

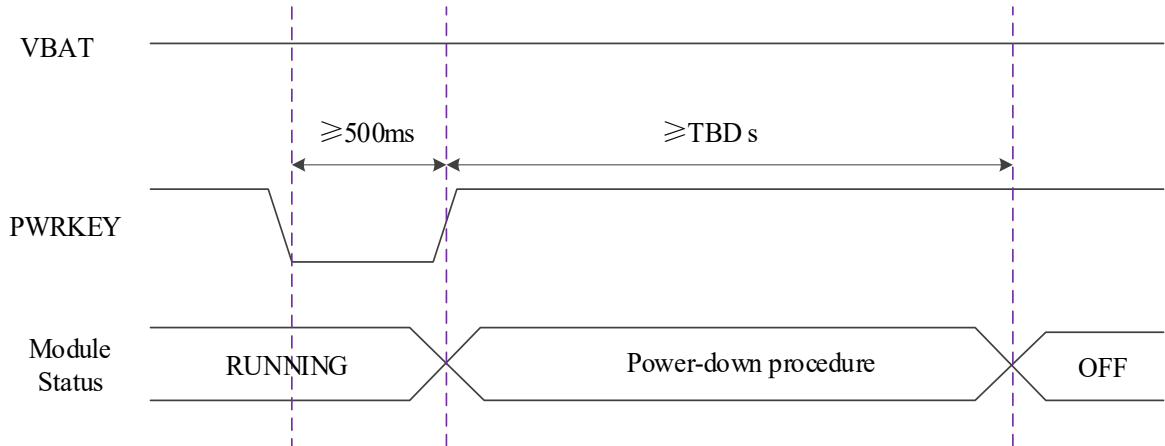


Figure 14 Power-off Sequence Diagram

3.8 Rest Function

There are two reset modes for the IQ50: hardware reset and AT command reset.

3.8.1 Reset by Hardware

When the module is working, give RESET_N a low level above Tst (500ms) to reset the module.

Table 8 RESET_N Pin Description

Pin name	No.	I/O	Description	Remark
RESET_N	24	DI	Reset module	1.5V power domain, active low level, internal pull-up, if not used, it is recommended to reserve test points

The reference circuit diagram is as follows: Customers can control the RESET_N pin using an open set drive circuit or a button.

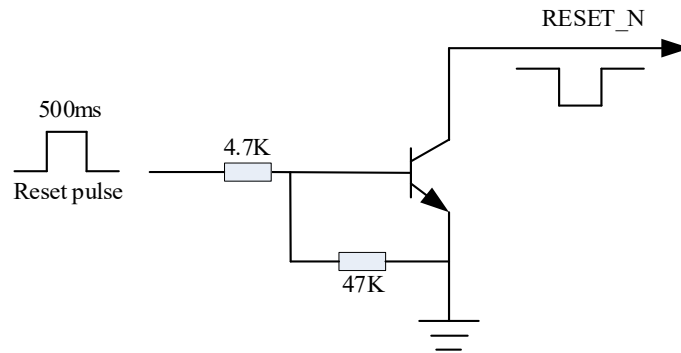


Figure 15 RESET_N Resets the Open Set Reference Circuit

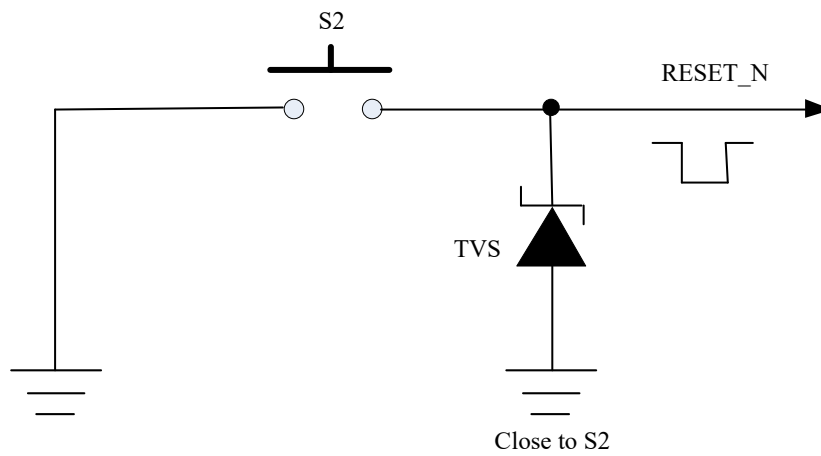


Figure 16 RESET_N Reset Button Reference Circuit

The reset sequence diagram is as follows:

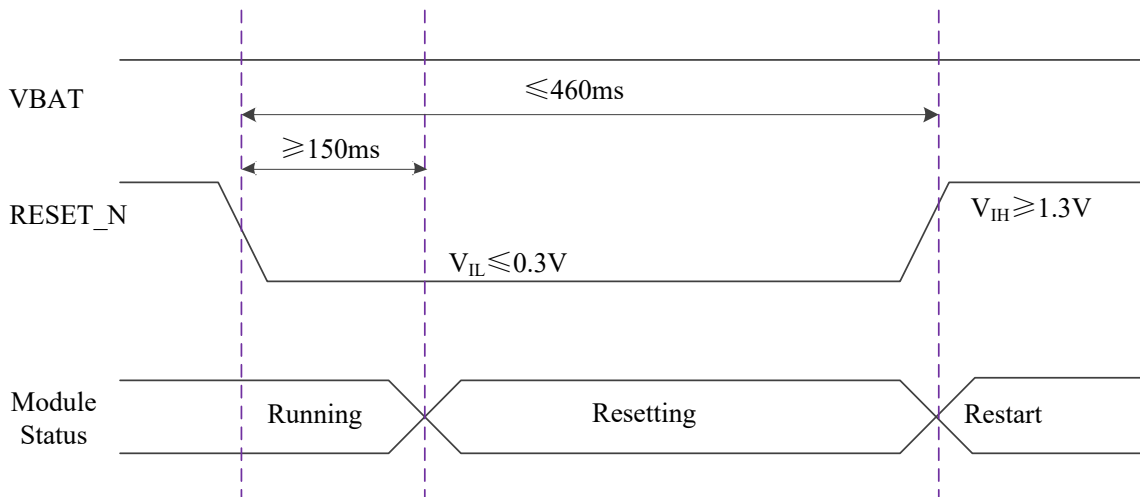


Figure 17 RESET_N Reset Sequence Diagram

3.8.2 Reset by AT Command

Run the AT+RESET command through the IQ50 UART or USB AT port to reset the IQ50.

3.9 USIM/SIM Interface

USIM card interface circuits comply with ETSI and IMT-2000 SIM interface requirements. The IQ50 supports 1.8V and 3.0V USIM cards.

USIM/SIM interface signals for the IQ50 are shown in the table below.

Table 9 USIM/SIM Interface

Pin name	No.	I/O	Description	Remark
USIM1_VDD	16	PO	USIM1 card power supply	Module automatically identifies 1.8V or 3.0V USIM card
USIM1_DATA	17	IO	USIM1 card data	Internal pull-up via 10 kΩ resistor
USIM1_CLK	18	DO	USIM1 card clock	-
USIM1_RST	19	DO	USIM1 card reset	-
USIM1_DET	15	DI	USIM1 card detection	Disconnect when not in use.
USIM2_VDD	98	PO	USIM2 card power supply	Module automatically identifies 1.8V or 3.0V USIM card
USIM2_DATA	95	IO	USIM2 card data	Internal pull-up via 10 kΩ resistor
USIM2_CLK	97	DO	USIM2 card clock	-
USIM2_RST	99	DO	USIM2 card reset	-
USIM2_DET	96	DI	USIM2 card detection	Disconnect when not in use.

IQ50 module supports USIM card hot swap through USIM_DET pins and supports high level detection. By default, the hot plug function is disabled. In the figure, the USIM_DET pin is high and grounded after the SIM card is inserted.

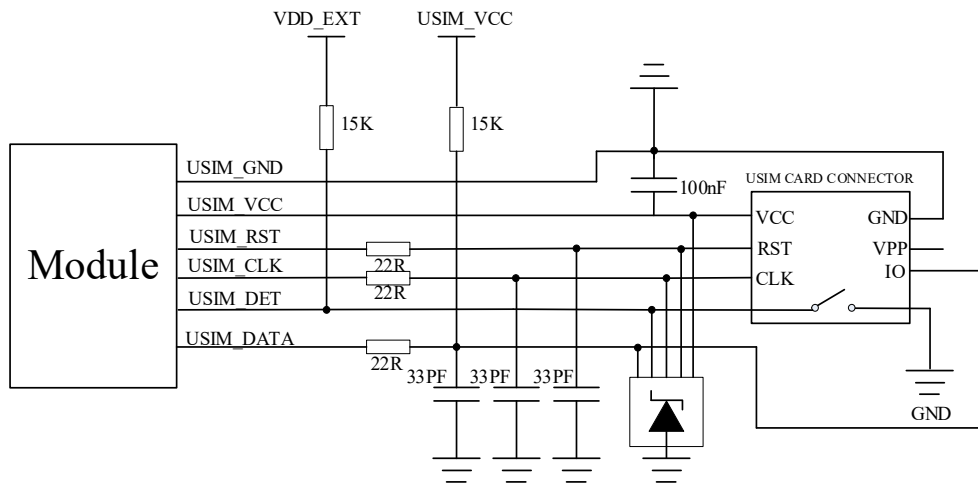


Figure 18 Reference Design Drawing of 8-Pin USIM/SIM Card Connector

If you do not need to use the USIM card detection function, keep the USIM_DET pin in the air. The following figure is the 6-pin USIM card interface reference circuit:

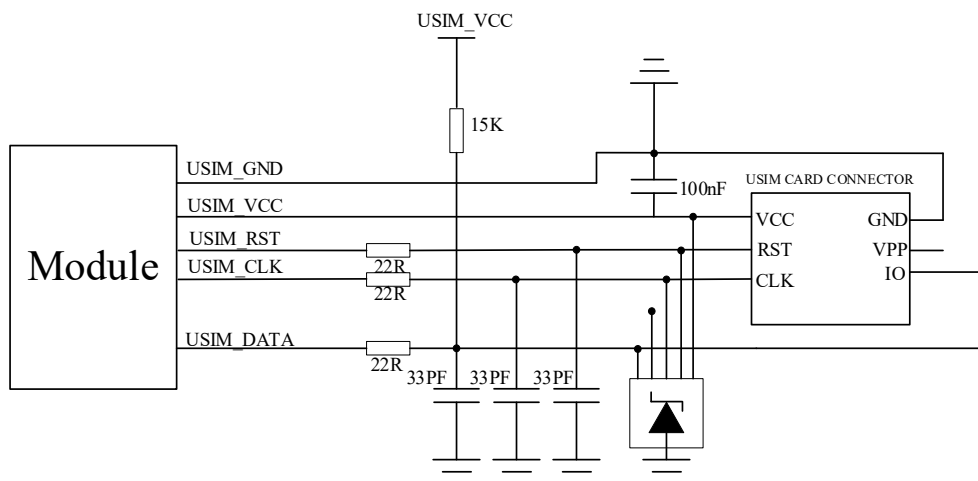


Figure 19 Reference Design Drawing of 6-Pin USIM/SIM Card Connector

In the circuit design of the USIM card interface, in order to ensure the good performance and reliability of the USIM card, the following design principles are recommended in the circuit design:

- USIM_DATA requires a pull-up resistor to USIM_VDD, which is 15kΩ. This pull-up resistance is conducive to increasing the anti-jamming capability of the SIM card. When the USIM card is running too long or the interference source is relatively close, it is recommended to increase the pull-up resistance near the card seat.
- String a 22Ω resistor on the USIM_DATA, USIM_CLK and USIM_RST lines to suppress stray EMI and enhance ESD protection.
- In order to improve the antistatic ability, TVS tubes are added to the USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST lines, and ESD protection devices with parasitic capacitance less than 15Pf are installed.

- Parallel 33pF capacitors on USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST lines to filter out GSM900 interference.
- The USIM card seat is placed close to the module, and the wiring length of the USIM card signal line is not more than 200mm.
- USIM card signal cable wiring away from RF line and VBAT power cable.
- In order to prevent crosstalk between USIM_CLK signal and USIM_DATA, the wiring of the two wires should not be too close, and the shielding between the two wires should be increased.
- For USIM/SIM hot swap function, hot swap is not supported by default, please contact us for more details.

Note: If SIM Connectors that do not support hot plug are directly used for hot plug of USIM, SIM card, it may damage USIM/SIM card or IQ50 USIM/SIM interface.

3.10 USB Interface

IQ50 provides a USB 2.0 compliant USB interface that supports both high-speed (480Mbps) and full-speed (12Mbps) modes. The USB port is used for AT command interaction, data transmission, software debugging, and version upgrade.

3.10.1 USB Pin Description

IQ50 module provides one channel USB2.0 High-Speed interface.

Table 10 USB Interface Description

Name	No.	I/O	Description	Remark
USB_VBUS	77	PI	USB detection	It is recommended to reserve test points
USB_DP	75	IO	USB differential data positive signal	It is recommended to reserve test points, 90Ω differential impedance is required
USB_DM	76	IO	USB differential data negative signal	It is recommended to reserve test points, 90Ω differential impedance is required

3.10.2 USB Reference Circuit

The following figure shows the USB interface reference circuit of the IQ50 module.

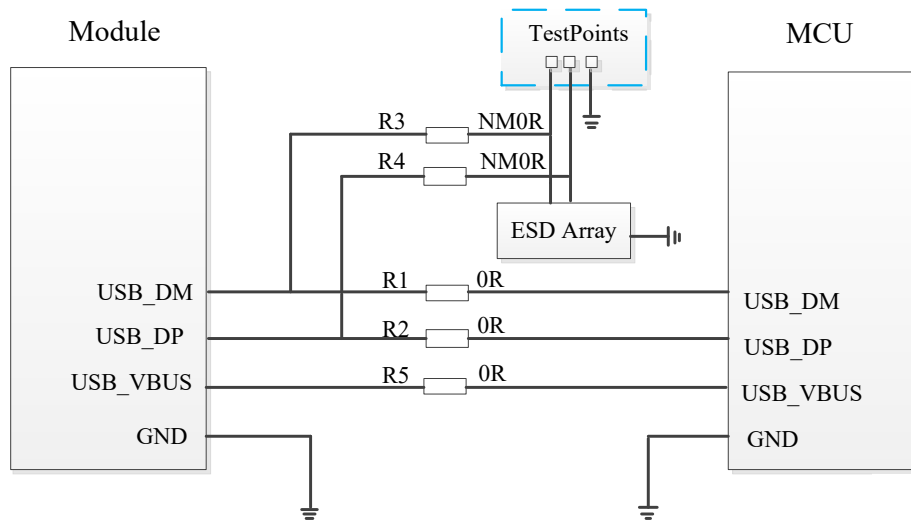


Figure 20 USB Interface Reference Design

To meet USB data cable signal integrity requirements, resistors R1/R2/R3/R4 must be placed close to the module, and the resistors must be placed close to each other. The branch connecting the test point must be as short as possible.

In USB interface circuit design, to ensure USB performance, it is recommended to follow the following principles in circuit design:

- Module USB_VBUS is not used to supply power to the module, but is used to detect the insertion and removal of USB.
- In order to reduce the signal interference during USB high-speed data transmission, connecting R1 and R2 on the USB_DM and USB_DP interface circuits can improve the data transmission accuracy, and 0Ω is recommended for both R1 and R2.
- To improve the antistatic performance of the USB interface, it is recommended to add ESD protection devices on the circuits of the USB_DP and USB_DM interfaces. It is recommended to use ESD devices with junction capacitance less than 1pF.
- In order to ensure the reliable work of USB, the design also need to consider more protection of USB, such as Layout of USB protection, need to do 90Ω impedance control of USB_DP, USB_DM, strictly according to the difference requirements of the line, as far as possible away from interference signals;
- Do not walk the USB cable under the crystal oscillator, oscillator, magnetic device and RF signal, it is recommended to walk the inner differential cable and cover the ground up and down.

3.10.3 USB Driver

IQ50 module supports various operating systems, such as PC operating systems: Windows 2000, Windows XP, Windows 10, Windows Vista32/64, Windows 7/8, embedded operating systems: Windows CE5.0/6.0 and Windows Mobile5.0/6.0 require dedicated USB driver support.

USB drivers provide different driver files based on the operating system, VID, and PID. For details, contact support personnel.

IQ50 also supports Linux and Android series embedded operating systems. As a Linux kernel system, the system will have its own driver usbserial.ko, there is no special IQ50 USB driver, is to load the system's usbserial.ko to achieve the loading of the IQ50 module USB, the key is to find the usbserial.ko driver file, Load the PID and VID into the system.

3.11 Serial Port

IQ50 module has 2 serial ports: Main serial port and debug serial port. The main features of these two serial ports are described below.

- Main serial port supports the baud rates of 9600,19200,38400,57600,115200,230400,460800bps. The default baud rate is 115200bps. Used for data transmission and AT command transmission;
- Debug serial port supports the baud rate of 115200bps, used for Linux control and log printing.

3.11.1 Serial Port Description

Table 11 Pin Description of Main Serial Port

Pin name	Pin No.	I/O	Description	Remark
MAIN_RI	68	DO	Module output ringing prompt	Disconnect when not in use.
MAIN_DCD	69	DO	Module output carrier detection	Disconnect when not in use.
MAIN_CTS	70	DO	Module clear send	CTS connected to MCU, disconnect when not in use.
MAIN_RTS	71	DI	DTE Request to Send Data	RTS connected to MCU,disconnect when not in use.
MAIN_DTR	72	DI	DTE ready, sleep mode control	Disconnect when not in use.
MAIN_TXD	73	DO	Module sending data	Disconnect when not in use.
MAIN_RXD	74	DI	Module receiving data	Disconnect when not in use.

Table 12 Pin Description of Debug Serial Port

Pin name	Pin No.	I/O	Description	Remark
DBG_TXD	14	DO	Module transmits data	It is suggested to reserve test points, disconnect when not in

use.

DBG_RXD	13	DI	Module receives data	It is suggested to reserve test points, disconnect when not in use.
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Table 13 Serial Port Logic Level

Parameter	Min	Max	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V
V_{OH}	1.35	1.8	V

IQ50 module provides 1.8V serial port. The customer needs to add a level converter for 3.3V serial port applications. TI's TXB0104PWR is recommended. The following is the reference design:

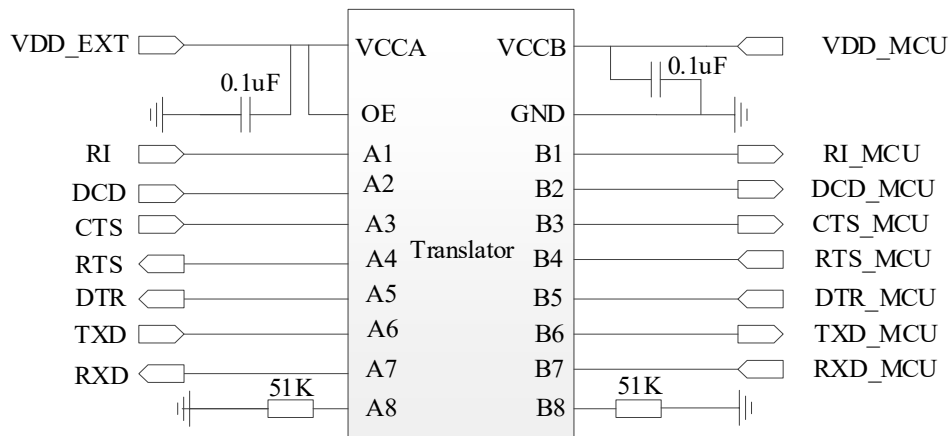


Figure 21 Reference Circuit of Level Translator Chip

3.12 ADC Function

IQ50 provides 2-channel analog-to-digital conversion interfaces. The voltage value of ADC0 can be read with AT+QADC=0, and the voltage value of ADC1 can be read with AT+QADC=1.

Table 14 ADC Pin Description

Pin name	Pin No.	Description	Voltage Range	Remark
----------	---------	-------------	---------------	--------

ADC0	49	Universal analog-to-digital conversion	0V~VBAT_BB	Disconnect when not in use.
ADC1	48	Universal analog-to-digital conversion	0V~VBAT_BB	Disconnect when not in use.

3.13 PCM and I2C Interface

IQ50 provides one PCM interface that supports the following 2 modes:

- Short frame mode: The module can be used as a master unit or slave;
- Long frame mode: The module can only be used as a master unit.

In short frame mode, data is sampled along the falling edge of PCM_CLK and sent along the rising edge. The falling edge of PCM_SYNC represents the high significant bit. PCM_CLK supports 128,256,512,1024 and 2048kHz voice codec.

In long frame mode, data is sampled along the falling edge of PCM_CLK and sent along the rising edge. The rising edge of PCM_SYNC represents the high significant bit. Only 128 kHz PCM_CLK and 8kHz, 50% duty cycle PCM_SYNC are supported.

IQ50 module supports 8-bit A-law, u-law, and 16-bit linear encoding formats. The following two diagrams are short frame mode timing diagram (PCM_SYNC=8 kHz, PCM_CLK=2048kHz) and long frame mode timing diagram (PCM_SYNC=8 kHz, PCM_CLK=128kHz).

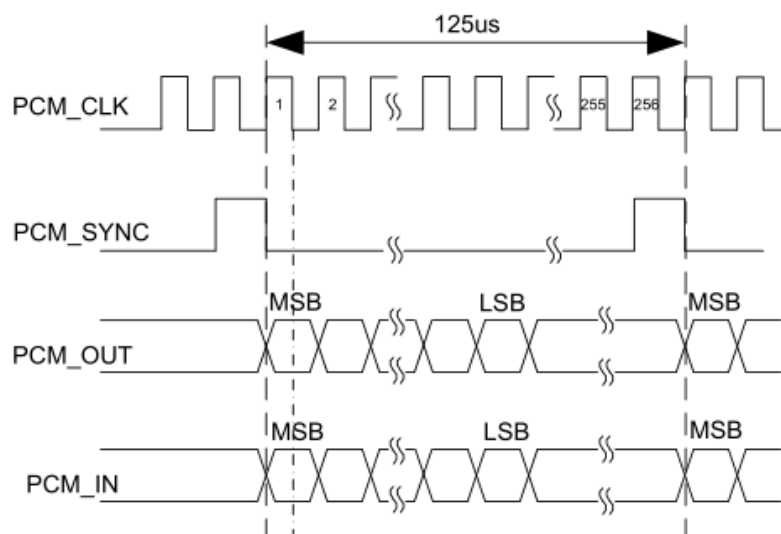


Figure 22 Sequence Diagram of Short Frame Mode

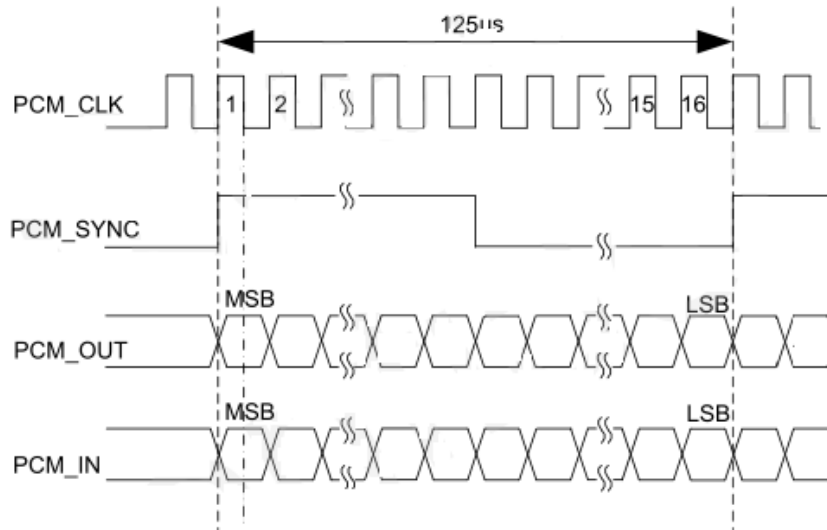


Figure 23 Sequence Diagram of Long Frame Mode

Table 15 PCM Interface Pin Description

Pin name	Pin No.	I/O	Description	Remark
PCM_DIN	28	DI	PCM input data	Disconnect when not in use.
PCM_DOUT	29	DO	PCM data output	Disconnect when not in use.
PCM_SYNC	30	IO	PCM data synchronization signal	Disconnect when not in use.
PCM_CLK	31	IO	PCM clock	Disconnect when not in use.
I2C_SCL	45	OD	I2C clock	External pull-up required, disconnect when not in use.
I2C_SDA	46	OD	I2C data	External pull-up required, disconnect when not in use.

The clock and mode can be set through the AT instruction, the default setting is short frame mode, PCM_SYNC=8kHz, PCM_CLK=2048kHz.

The following is a reference design for the PCM interface with an external Codec chip:

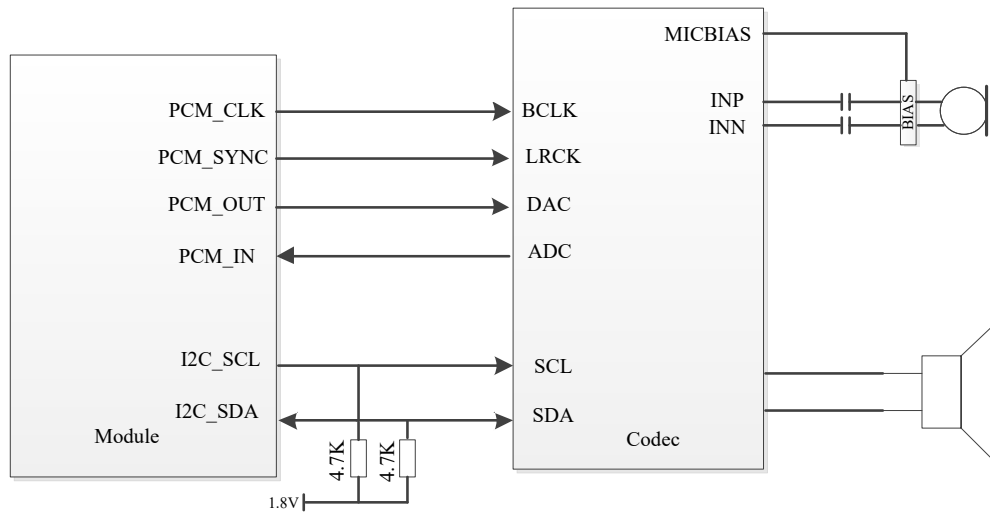


Figure 24 PCM Circuit Reference Design

3.14 SPI Interface

IQ50 Series supports one master mode SPI interface with maximum clock frequency of 50 MHz.

Table 16 PCM Interface Pin Description

Pin name	Pin No.	I/O	Description	Remark
SPI_CS	41	DO	SPI chip select	Only main mode is supported
SPI_MOSI	42	DO	SPI master output slave input	Only main mode is supported
SPI_MISO	43	DI	SPI Master Input Slave Output	Only main mode is supported
SPI_CLK	44	DO	SPI clock	Only main mode is supported

The SRM 813Q module provides a 1.8V SPI, and the customer needs to add a level shifter for 3.3V applications. The reference design is shown below:

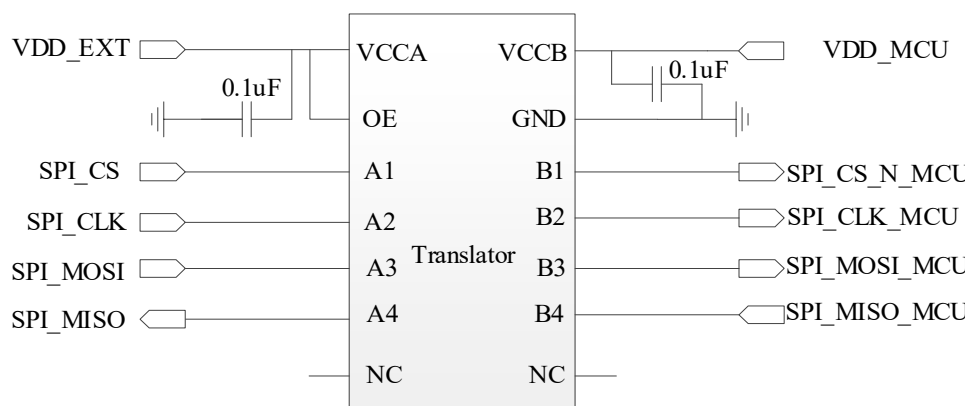


Figure 25 Reference Circuit of Level Conversion Chip

3.15 PCIe Interface

IQ50 provides a PCIe 2.0 interface.

Table 17 PCIe2.0 Interface Pin Description

PCIe Interface				
Pin name	Pin No.	I/O	Description	DC Characteristics
PCIE_RX_P	101	AI	PCIe data receive positive signal	85Ω differential impedance required, 220nF capacitor connected in series near PHY chip end
PCIE_RX_M	102	AI	PCIe data receive negative signal	
PCIE_TX_P	103	AO	PCIe data send positive signal	85Ω differential impedance required, 220nF capacitor connected in series near module end
PCIE_TX_M	104	AO	PCIe data sends a negative signal	
PCIE_CLK_P	105	AIO	PCIe clock positive signal	85Ω differential impedance required
PCIE_CLK_M	107	AIO	PCIe clock negative signal	
PCIE_RST_N	20	DIO	PCIe reset signal	-
PCIE_CLKREQ_N	21	DIO	PCIe clock request signal	-
PCIE_WAKE_N	100	DIO	PCIe wake-up signal	-
Coexistence and Control Interface				
Pin name	Pin No.	I/O	Description	DC Characteristics
WLAN_EN	89	DO	WLAN enable control	-

BT_EN	132	DO	BT enable control	High level effective
WLAN_SLP_CLK	85	DO	WLAN Sleep Clock	-
WLAN_PWR_EN	91	DO	WLAN power enable control	High level effective
WLAN_WAKE	87	DI	WLAN wake up module	-
COEX_RXD	90	DI	5G/LTE/WLAN&BT coexistence received signal	-
COEX_TXD	88	DO	5G/LTE/WLAN&BT coexistence transmission signal	-
N79_TX_EN_TO_WLAN	92	DO	Notification n79 transmitted from SDR Lost to WLAN	-
WLAN_PA_MUTING	94	DO	SDX Control Turn off WLAN PA	-
WLAN_SW_CTRL	86	DI	WiFi clock request	-

The following figure shows the PCIe interface reference design.

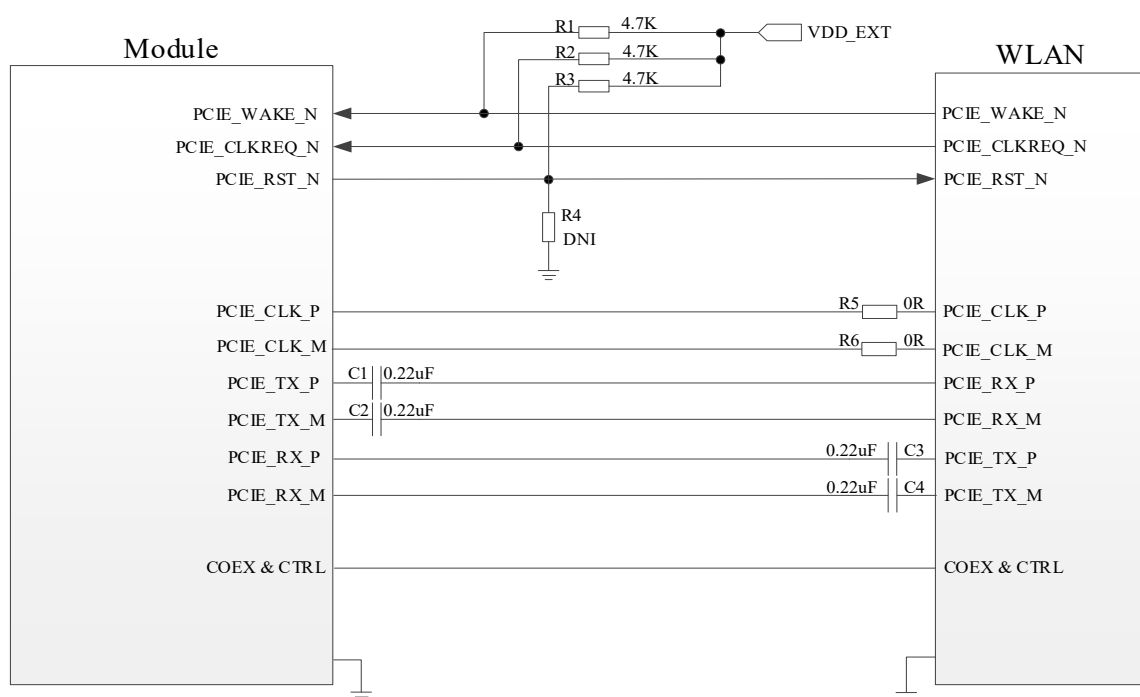


Figure 26 PCIe Interface Reference Design

Design the PCIe interface circuit according to the following principles:

- PCIe data and control signal cables are far away from RF and VBAT.
- The line length shall not exceed 250mm, and the difference line group shall be less than 0.7mm;
- The differential impedance of the PCIe data line is controlled within $85\ \Omega \pm 10\%$.
- In order to reduce mutual interference, the TX and RX adjacent distance of the same layer must be greater than 3 times the line width, and the adjacent distance with other signal lines must be greater than 4 times the line width.

3.16 SGMII Interface

IQ50 includes an integrated Ethernet MAC SGMII interface and one management interfaces (MDIO). The main features of the SGMII interface are as follows:

- Comply with IEEE802.3 standard;
- 1000Mbps full duplex;
- 10/100Mbps half/full duplex;
- Support VLAN tag;
- Support IEEE1588 and Precise Time Protocol (PTP).

Table 18 SGMII Interface Pin Description

Pin name	Pin No.	I/O	Description	Remark
SGMII_RST_N	37	DO	SGMII regeneration	-
SGMII_INT_N	123	DI	SGMII interrupt signal	-
SGMII_WOL_INT_N	128	DI	SGMII Remote Wake-Up Interrupt Signal	-
SGMII_PWR_EN	130	DO	SGMII PHY Power Enable	Disconnect when not in use.
SGMII_MDIO	36	IO	SGMII MDIO	
SGMII_MDC	121	DO	Sgmii mdiotime	Disconnect when not in use.
SGMII_TX_P	119	AO	SGMII data send positive signal	
SGMII_TX_M	34	AO	SGMII data sends negative signal	90 Ω differential impedance required, 100nF capacitor

						connected in series near module end
SGMII_RX_P	117	AI	SGMII data receive signal	positive		90Ω differential impedance required, 100nF capacitor connected in series near PHY chip end

The following is the application block diagram of Ethernet:

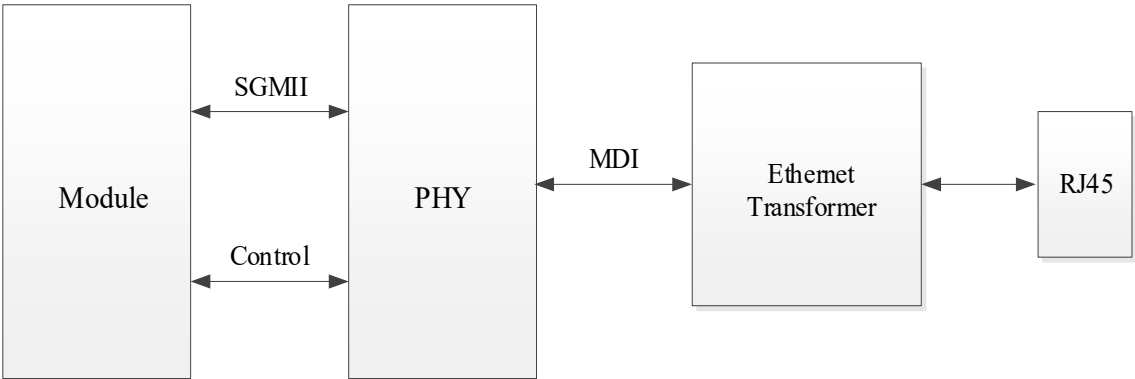


Figure 27 Ethernet Application Diagram

In order to improve the reliability of customers in the application, please follow the Ethernet PHY circuit design standards, mainly pay attention to the following points:

- SGMII data and control signal lines are kept away from RF and VBAT;
- The line length is not more than 10 inches, and the difference line group is less than 20mil;
- The differential impedance of SGMII data line is controlled within 90Ω ±10%;
- In order to reduce mutual interference, the adjacent distance of the same layer of tracks must be greater than or equal to 40mil.

3.17 SDIO Interface*

The IQ50 provides a low power WLAN SDIO 3.0 interface.

Table 19 Pin Description for Wireless Connection Interface

WLAN Part				
Pin name	Pin No.	I/O	Description	Remark

SDC_CLK	79	DO	WLAN SDIO signal clock	50Ω impedance required, disconnect when not in use.
SDC_CMD	80	IO	WLAN SDIO signal command	50Ω impedance required, disconnect when not in use.
SDC_DATA_3	82	IO	WLAN SDIO signal data line 3	50Ω impedance required, disconnect when not in use.
SDC_DATA_2	81	IO	WLAN SDIO signal data line 2	50Ω impedance required, disconnect when not in use.
SDC_DATA_1	84	IO	WLAN SDIO signal data line 1	50Ω impedance required, disconnect when not in use.
SDC_DATA_0	83	IO	WLAN SDIO signal data line 0	50Ω impedance required, disconnect when not in use.

SDIO is a high-speed signal, SDIO interface design needs to comply with the SDIO 3.0 specification, in the circuit design is recommended to follow the following principles:

- SDIO signal line impedance control within 50 Ω (±10%), GND shielding treatment is recommended;
- SDIO signal line away from other sensitive signals, such as RF circuits, analog signals, clock signals, DCDC and other noise signals;
- The trace length difference between CLK and DATA/CMD is less than 1mm, and the total length is less than 50mm;
- Prevent SDIO_CLK and SDIO_DATA/SDIO_CMD from interfering with each other, the distance between adjacent traces is greater than 2W, and the bus parasitic capacitance is less than 15pf;
- The series matching resistor on the clock signal near the module end is between 15 and 24Ω, and the distance between the resistor and the wiring of the module is no more than 5 mm.

*SDIO interface, under development, temporarily not supported.

3.18 STATUS Status Indication

STATUS Indicates the working status of the module. When the module is powered on normally, STATUS outputs a low level.

Table 20 STATUS Pin Description

Pin name	Pin No.	I/O	Description	Remark
STATUS	67	OD	Indicate that operational status of the module	External pull-up is required, disconnect when not in use.

The following figure shows the reference circuit design of STATUS:

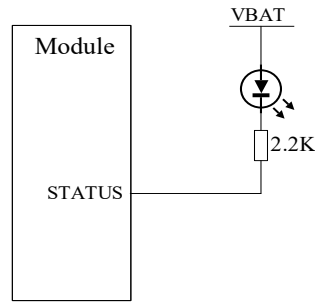


Figure 28 STATUS Reference Circuit

3.19 Network Status Indication

The network status indicator pin can be used to drive one network status indicator. The IQ50 module provides two pins: NET_MODE and NET_STATUS. The following two tables describe pin definitions and logic levels for different network states.

Table 21 Network Indication Pin Description

Pin name	Pin No.	I/O	Description	Remark
NET_MODE	5	DO	Indicate the network registry status of the module	Disconnect when not in use.
NET_STATUS	6	DO	Indicate the network operation status of the module	Disconnect when not in use.

Table 22 Working Status of Network Indication Pin

Mode	Status	Description
NET_MODE	High level	Register 5G network
	Slow Flash (500ms OFF/2000ms ON)	Register 3G/4G network
	Low level	Other
NET_STATUS	Quick blink (800ms OFF/100ms ON)	Search network state
	Slow Flash (3000ms OFF/100ms ON)	Standby mode
	Speed flashing (300ms OFF/100ms ON)	Data transmission mode
	High level	Other

The reference circuit of the NET indicating interface of IQ50 is shown in the following figure, and the current limiting resistor can be selected according to the actual situation:

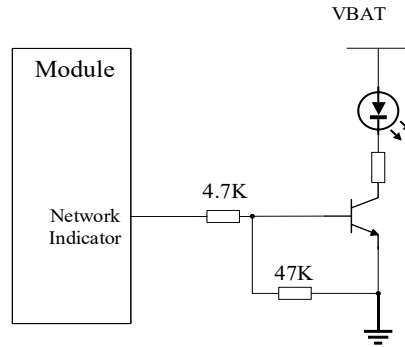


Figure 29 Reference Design Drawing of Network Indication

3.20 DLOAD Interface

IQ50 supports DLOAD. The customer can pull the DLOAD to VDD_EXT(1.8V) before the module is turned on, and the module will enter the forced download mode after it is turned on. In this mode, modules can be upgraded via USB interface.

Table 23 DLOAD Pin Description

Pin name	Pin No.	I/O	Description	Remark
USB_BOOT	22	DI	Forced download mode control	Do not pull up to high level until startup is successful. It is recommended to reserve test points

The reference circuit is as follows:

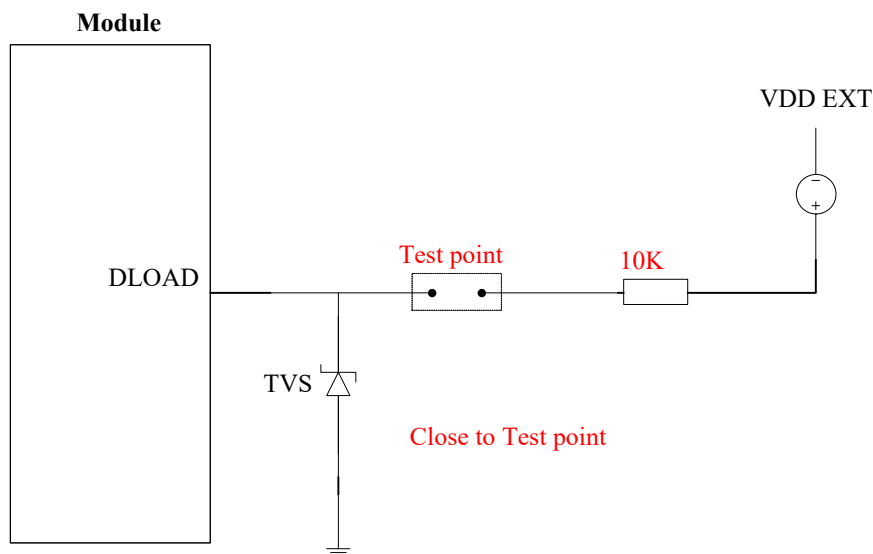


Figure 30 DLOAD Interface Reference Circuit

4 GNSS

4.1 Basic Description

The IQ50 includes a complete embedded GNSS solution.

The IQ50 module supports the standard NMEA-0183 protocol and outputs 1Hz NMEA statements through the USB interface by default.

4.2 GNSS Performance

The following table lists the GNSS performance of the IQ50 module.

Table 24 GNSS Performance List

Parameter	Description	Performance index
Positioning accuracy (open field)	CEP-50	< 3m
	Cold start	35s
First location Time TTFF (open field)	Warm start	29s
	Hot start	2s
Sensitivity	Capture	-145dBm
	Recapture	-155dBm
	Tracking	-156dBm

4.3 Layout Guide

The customer needs to follow the following layout guidelines in the design:

- The distance between GNSS antenna, main antenna and diversity antenna should be as large as possible;
- Digital signals such as USIM card, USB interface, camera module, display interface and SD card should be away from the antenna;

- Sensitive analog signals should be kept away from GNSS signal paths, and ground holes should be added for isolation and protection.
- ANT_GNSS Maintains the characteristic impedance of 50Ω.

GNSS reference design and antenna considerations refer to Chapter 5.

5 Antenna Interface

5.1 Introduction to Antenna Interfaces

IQ50 provides 3 antenna pins:

Table 25 Antenna Interface Pin Definition

Pin name	No.	Description	I/O	Remark
ANT_MAIN	55	Main antenna	IO	50Ω impedance
ANT_DIV	39	Diversity antenna	AI	50Ω impedance
ANT_GNSS	51	GNSS antenna	AI	50Ω impedance

Optional connection diversity antennas can be used to improve the TDD-LTE/FDD-LTE/NR reception performance of the product.

It is recommended that users use a 50Ω impedance antenna that matches the RF connector at the module end.

Special note: To ensure the communication ability of all frequency bands, please connect both the main and auxiliary antennas.

It is recommended that the application end carefully select the RF conversion cable, and select the RF conversion cable with the lowest loss as possible. The following RF conversion cables with RF loss requirements are recommended:

- TDD-5G NR<1.5dB;
- FDD-5G NR<1.5dB;
- TDD-LTE<1.5dB;
- FDD-LTE<1.5dB.

5.2 RF Reference Circuit

The reference design circuit for connecting ANT_MAIN and ANT_DIV antennas is shown in the figure below. To obtain better RF performance, schematic design and PCB layout need to pay attention to the following four points:

1. Schematic design, close to the module RF port reserved π -type matching circuit, capacitor default is not attached;
2. Schematic design, redundant RF connector between module RF port and antenna, used for certification test, RF connector can't be affixed after mass production and delivery; (Reference: RF connector -1P-H176)
3. Schematic design, reserve π -type matching circuit near the antenna end, capacitor is not attached by default;
4. PCB layout, the route between the RF port of the module and the antenna is as short as possible, and the board factory needs to do 50 Ω impedance control of the RF route.

Note: The customer needs to consider the impedance matching between the baseboard and the module, and the reserved matching should be optimized according to the actual situation to ensure the best performance.

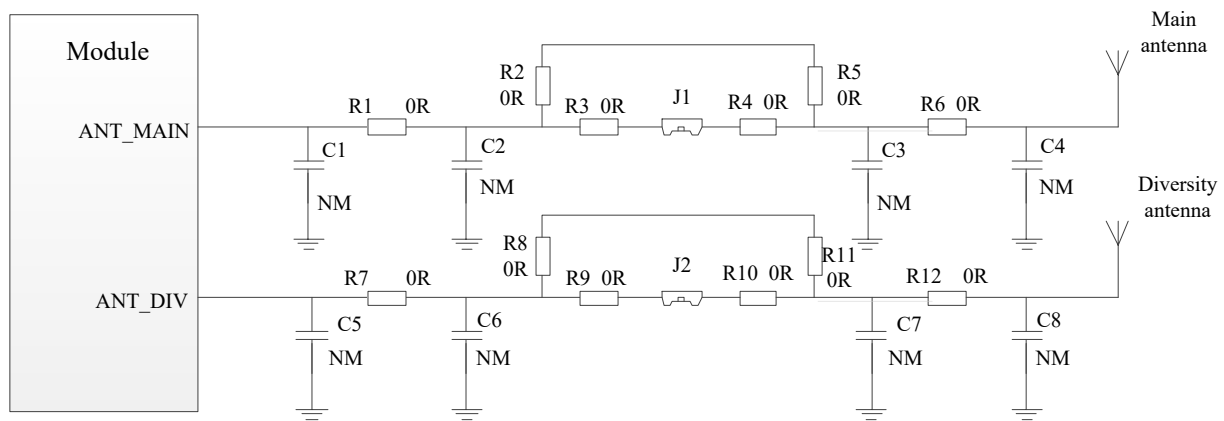


Figure 31 RF Reference Circuit

The GNSS antenna reference design is shown in the figure below:

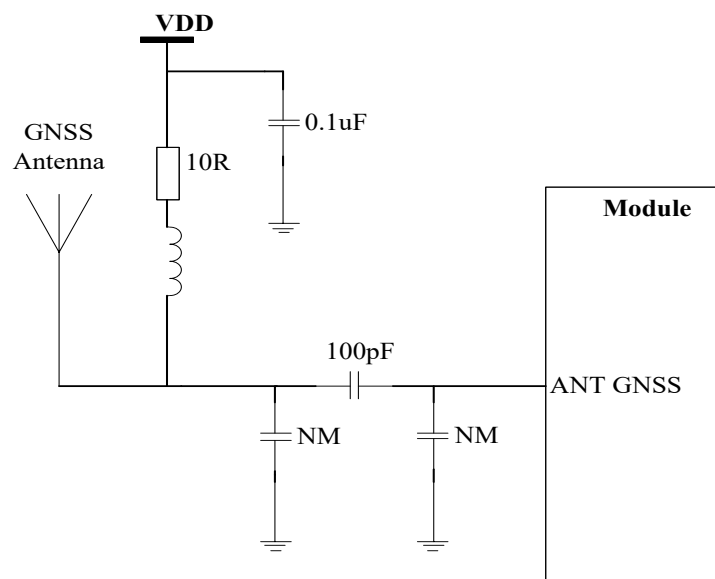


Figure 32 GNSS Antenna Reference Circuit

Note:

1. Customers can choose external LDO power supply according to the type of active antenna;
2. If passive antenna is selected for customer design, there is no need to design VDD circuit.

5.3 RF Reference Circuit

5.3.1 Antenna Requirements

The requirements of main antenna and diversity receiving antenna are shown in the following table:

Table 26 Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1561-1615MHz
	Polarization: RHCP or linear
	VSWR: < 2 (Typ)
	Passive antenna gain: > 0 dBi
	Active antenna noise factor: < 1.5 dB
	Active antenna gain: > -2 dBi
	Active antenna embedded LNA gain: 20 dB (typical value)
	Total gain of active antenna:> 18 dBi (typical value)
TDD-5G NR/FDD-5G NR/TDD-LTE/FDD-LTE	VSWR: < 2
	Gain (dBi): 1
	Maximum input power (W): 2
	Input impedance (ohm): 50
	Polarization type: vertical direction
	Cable insertion loss: < 1dB
	(LTE B5/B12/B13/B14/B17/B26/B71, 5G NR N5/N12/N13/N14/N26/N71) Cable insertion loss: < 1.5dB

(LTE B2/B4/B25/B66,5G NR N2/N25/N66/N70) Cable insertion loss: < 1.5dB

(LTE B7/B30/B38 /B41/B42/B43/B48,5G NR N7/N38 /N41/N48/N77/N78) Cable insertion loss: < 2dB

5.3.2 RF Output Power

The RF output power of IQ50 is shown in the table below.

Table 27 RF Transmit Power

Network mode	Band	Max	Min
TDD-5G NR	N38	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N41	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N48	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N77	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N78	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
FDD-5G NR	N2	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N5	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N7	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N12	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N13	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N14	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N25	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N26	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N30	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N66	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N70	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	N71	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm

TDD-LTE	Band38	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band41	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band42	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band43	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band48	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
FDD-LTE	Band2	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band4	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band5	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band7	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band12	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band13	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band14	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band17	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band25	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band26	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band30	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band66	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm
	Band71	23dBm $\pm$ 2.7 dB	$\leq$ -44 dBm

5.3.3 RF Receiving Sensitivity

Table 28 RF Receiving Sensitivity

Network mode	Band	Receive sensitivity
TDD-5G NR	N38	$<$ -96dBm @10MHz BW
	N41	$<$ -96dBm @10MHz BW

	N48	<-96dBm @10MHz BW
	N77	<-96dBm @10MHz BW
	N78	<-96dBm @10MHz BW
FDD-5G NR	N2	<-99dBm @5MHz BW
	N5	<-99dBm @5MHz BW
	N7	<-99dBm @5MHz BW
	N12	<-99dBm @5MHz BW
	N13	<-99dBm @5MHz BW
	N14	<-99dBm @5MHz BW
	N25	<-99dBm @5MHz BW
	N26	<-99dBm @5MHz BW
	N30	<-99dBm @5MHz BW
	N66	<-99dBm @5MHz BW
	N70	<-99dBm @5MHz BW
	N71	<-99dBm @5MHz BW
TDD-LTE	Band38	<-99dBm @5MHz BW
	Band41	<-100dBm @5MHz BW
	Band42	<-100dBm @5MHz BW
	Band43	<-100dBm @5MHz BW
	Band48	<-99dBm @5MHz BW
FDD-LTE	Band2	<-99dBm @5MHz BW
	Band4	<-99dBm @5MHz BW
	Band5	<-99dBm @5MHz BW
	Band7	<-99dBm @5MHz BW

Band12	<-99dBm @5MHz BW
Band13	<-99dBm @5MHz BW
Band14	<-99dBm @5MHz BW
Band17	<-99dBm @5MHz BW
Band25	<-99dBm @5MHz BW
Band26	<-99dBm @5MHz BW
Band30	<-99dBm @5MHz BW
Band66	<-99dBm @5MHz BW
Band71	<-99dBm @5MHz BW

5.3.4 Working Frequency

Table 29 Working Frequency

Network mode	Band	Receive	Transmit
TDD-5G NR	N38	2570~2620MHz	2570~2620MHz
	N41	2496~2690MHz	2496~2690MHz
	N48	3550~3700MHz	3550~3700MHz
	N77	3300~4200MHz	3300~4200MHz
	N78	3300~3800MHz	3300~3800MHz
FDD-5G NR	N2	2010~2070MHz	1920~1980MHz
	N5	869~894MHz	824~849MHz
	N7	2620~2690MHz	2500~2570MHz
	N12	729~746MHz	699~716MHz
	N13	880~915MHz	777~787MHz
	N14	758~768MHz	788~798MHz

	N25	1930~1995MHz	1850~1915MHz
	N26	859~894MHz	814~849MHz
	N30	2350~2360MHz	2305~2315MHz
	N66	2110~2200MHz	1710~1780MHz
	N70	1995~2020MHz	1695~1710MHz
	N71	617~652MHz	663~698MHz
TDD-LTE	Band38	2570~2620MHz	2570~2620MHz
	Band41	2496~2690MHz	2496~2690MHz
	Band42	3400~3600MHz	3400~3600MHz
	Band43	3600~3800MHz	3600~3800MHz
	Band48	3550~3700MHz	3550~3700MHz
FDD-LTE	Band2	1930~1990MHz	1850~1910MHz
	Band4	2110~2150MHz	1710~1750MHz
	Band5	869~894MHz	824~849MHz
	Band7	2620~2690MHz	2500~2570MHz
	Band12	729~746MHz	699~716MHz
	Band13	746~756MHz	777~787MHz
	Band14	758~768MHz	788~798MHz
	Band17	734~746MHz	704~716MHz
	Band25	1930~1995MHz	1850~1915MHz
	Band26	859~894MHz	814~849MHz
	Band30	2350~2360MHz	2305~2315MHz
	Band66	2110~2180MHz	1710~1780MHz
	Band71	617~652MHz	663~698MHz

5.3.5 Antenna Requirement

Table 30 Antenna Index Requirement

Network Mode	Band	Vswr	Gain Peak	Avg.	Effi.	SAR	TRP (dBm)	TIS (dBm)
TDD-5G NR	N38						19	<-93
	N40						19	<-93
	N41						19	<-93
	N77						19	<-93
	N78						19	<-93
FDD-5G NR	N1						19	<-93
	N3						19	<-93
	N5						18	<-92
	N7						19	<-93
	N8						18	<-92
	N20	<2.5:1	>0dBi	>-4dBi	>40%	<1.6W/Kg	18	<-92
	N28						18	<-92
TDD-LTE	Band34						19	<-93
	Band38						19	<-93
	Band39						19	<-93
	Band40						19	<-93
	Band41						19	<-93
	Band42						19	<-93
	Band43						19	<-93
FDD-LTE	Band1						19	<-93

Band3	19	<-93
Band5	18	<-92
Band7	19	<-93
Band8	18	<-92
Band20	18	<-92
Band28	18	<-92

Table 31 Diversity Antenna Index Requirements

Mode	Band	VSWR	Gain /Avg.	Efficiency	ρ	Isolation
TDD-5G NR	N38					
	N40					
	N41					
	N77					
	N78					
FDD-5G NR	N1					
	N3					
	N5	<2.5:1	>-4dBi	>25%	<0.5	<-8dB
	N7					
	N8					
	N20					
	N28					
TDD-LTE	Band34					
	Band38					
	Band39					

FDD-LTE	Band40
	Band41
	Band42
	Band43
	Band1
	Band3
	Band5
	Band7
	Band8
	Band20
	Band28

6 Electrical Characteristics

6.1 Limiting Voltage Range

The limit voltage range refers to the maximum voltage range that the module supply voltage and the digital and analog input/output interfaces can withstand. Work outside the scope may cause damage to the product.

The limit voltage range of IQ50 is shown in the table below.

Table 32 Limiting Working Voltage Range of the Module

Parameter	Description	Min	Typical	Max	Unit
VBAT	IQ50 power supply	3.3	3.8	4.3	V
	RMS average supply current	0	TBD	TBD	A
	At instantaneous voltage drop per slot, IVBAT peak current may reach 2A (power emission per 4.6ms slot)	-	-	400	mV
GPIO	Digital IO level supply voltage	-0.3	1.8	2.0	V
	Shutdown mode power supply voltage	-0.25	0	0.25	V

6.2 Ambient Temperature Range

IQ50 module is recommended to operate at -30~+75°C. Advised to consider temperature control measures when the environment is harsh. At the same time, the extended operating temperature range of the module is provided. When used at the extended temperature, the function is normal, and some RF indicators may deteriorate. At the same time, it is recommended that the module application terminal be stored under certain temperature conditions. Modules outside this range may not work properly or be damaged.

Table 33 Temperature Range of the Module

Parameter	Min	Typical	Max	Unit
Working temperature	-30	+25	+75	°C
Extended working temperature	-40~-30		75~+85	°C

Storage temperature	-45	+90	°C
---------------------	-----	-----	----

6.3 Electrical Characteristics of Interface in Working Status

V_L : logic low level;

V_H : High logic level.

Table 34 Logic Levels of Ordinary Digital IO Signals

Signals	VL Min	Max	VH Min	Max	Unit
Digital input	-0.3	$0.3 \cdot V_{pin_min}$	$0.3 \cdot V_{pin_max}$	V_{pin_max}	V
Digital output	GND	0.2	$V_{pin_min} - 0.2$	V_{pin}	V

Note: $V_{pin_min} = 1.45V$, $V_{pin_max} = 2.0V$ (V_{pin} is the high level of digital interface, $V_{pin} = 1.8V$)

Table 35 Electrical Characteristics of Power Supply in Working Status

Parameter	I/O	Min	Typical	Max	Unit
VBAT	I	3.3	3.8	4.3	V
SIM_VCC	O	1.7/2.75	1.8/2.85	1.9/2.95	V

6.4 Power Consumption

Below is the power consumption of the IQ50 module in each operating mode, please contact us for more frequency band information.

Table 36 Power Consumption

Mode	Conditions	Power	Average Current	Units
Sleep mode	AT+CFUN=0	-	1.93	mA
	AT+CFUN=4	-	2.01	mA
	LTE FDD PF = 128	-	2.57	mA
	LTE TDD PF = 128	-	2.56	mA

	SA FDD PF = 128	-	TBD	mA
	SA TDD PF = 128	-	TBD	mA
Mode	Conditions	Power	Average Current	Units
Idle mode	AT+CFUN=0	-	28.01	mA
	AT+CFUN=4	-	27.87	mA
	LTE FDD PF = 128	-	30.47	mA
	LTE TDD PF = 128	-	30.52	mA
	SA FDD PF = 128	-	30.73	mA
	SA TDD PF = 128	-	30.78	mA
Mode	Conditions	Power	Average Current	Units
LTE	B2 20M	22.1dBm	609.35	mA
	B4 20M	22.6dBm	647.55	mA
	B5 10M	23.2dBm	584.44	mA
	B7 20M	21.1dBm	742.33	mA
	B12 10M	23.3dBm	595.35	mA
	B13 10M	23.1dBm	538.32	mA
	B14 10M	23.1dBm	522.85	mA
	B17 10M	23.2dBm	537.68	mA
	B25 20M	22.1dBm	604.60	mA
	B26 15M	23.2dBm	596.80	mA
	B30 10M	20.8dBm	718.35	mA

B66 20M	22.6dBm	645.76	mA
B71 20M	23.4dBm	595.29	mA
B38 20M	20.9dBm	354.08	mA
B41 20M	22.1dBm	496.17	mA
B42 20M	21.2dBm	340.45	mA
B43 20M	21.5dBm	341.37	mA
B48 20M	21.5dBm	325.20	mA

Mode	Conditions	Power	Average Current	Units
5G SA	N2 20M	22.8dBm	526.79	mA
	N5 20M	22.7dBm	531.50	mA
	N7 20M	22.2dBm	663.42	mA
	N12 15M	21..9dBm	472.20	mA
	N13 10M	21.8dBm	390.78	mA
	N14 10M	21.8dBm	388.794	mA
	N25 20M	22.5dBm	517.39	mA
	N26 20M	22.6dBm	501.45	mA
	N30 10M	21.8dBm	211.14	mA
	N66 20M	22.3dBm	565.81	mA
	N70 15M	22.38dBm	606.03	mA

N71 20M	23.9dBm	581.46	mA
N38 20M	22.1dBm	189.75	mA
N41 20M	21.8dBm	223.50	mA
N48 20M	21.7dBm	167.16	mA
N77 20M	23.4dBm	217.71	mA
N78 20M	22.8dBm	206.55	mA

6.5 Environmental Reliability Requirements

Table 37 Environmental Reliability Requirements

Test item	Test conditions	
Low temperature storage test	Temperature -45℃, 24 hours in shutdown status	
High temperature storage test	Temperature +90℃, 24 hours in shutdown status	
Aging test	Temperature +75℃, Redcap NR band cyclic emission p-MAX power lasting 168 hours	
High temperature and high humidity test	Temperature +85℃, humidity 85%RH, continuous 1000 hours under power-on state	
Low temperature operation test	Temperature -30℃, 24 hours in working status	
High temperature operation test	Temperature +75℃, 24 hours in working status	
Vibration test	Perform vibration test according to the requirements shown in the following table:	
	Frequency	Random vibration ASD (Acceleration Spectral Density)
	5~20Hz	0.96m ² /s ³
	20~500Hz	0.96m ² /s ³ (at 20Hz), other -3dB/octave
Life test of connectors	Board-to-board connector interface can be inserted and removed for 50 times; RF antenna interface cable can be inserted and removed for 30 times	
ESD test	1. The module tests the power PAD and large area under the call state, ESD meets:	
	① Contact discharge should pass ±4KV, ±5KV test grade	

-
- ② Air discharge should pass $\pm 8\text{KV}$, $\pm 10\text{KV}$ test grade
 - 2. When the module is powered off, test the SIM card of EVB, and ESD meets the following requirements:
 - ① Contact discharge should pass $\pm 4\text{KV}$ test grade
 - ② Air discharge should pass $\pm 8\text{KV}$ test grade
 - 3. Other interfaces of the module, ESD meets:
 - ① Contact discharge should pass $\pm 1\text{KV}$ test grade
 - ② Air discharge should pass $\pm 2\text{KV}$ test grade
-

6.6 ESD Features

IQ50 is a consumer end-product. Although ESD problems have been considered in the design of the module and ESD protection has been made, ESD problems may also occur in the transportation and secondary development of the IQ50 module, so developers should consider the ESD protection of the final product, in addition to the anti-static treatment of the packaging must be considered. For customer application, please refer to the recommended circuit of interface design in the documentation.

For the IQ50 module ESD allowable discharge range refer to the following table

Table 38 ESD Performance Parameters (temperature: 25°C, humidity: 45%)

Tested points	Contact discharge	Air discharge	Unit
VBAT, GND	± 5	± 10	KV
Antenna interfaces	± 4	± 8	KV
Other interfaces	± 0.5	± 1	KV

7 Mechanical Characteristics

7.1 Mechanical Dimensions of the Module

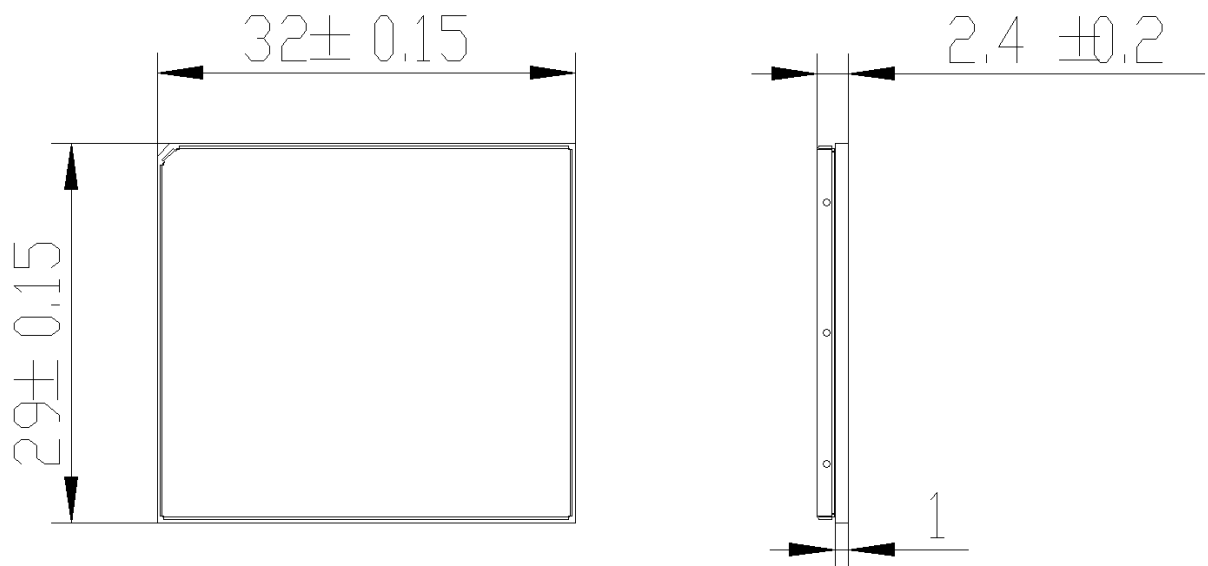


Figure 33 Top and Side Dimensional Drawing (Unit: mm)



7.3 Module Top View



Figure 36 Module Top View

7.4 Module Bottom View

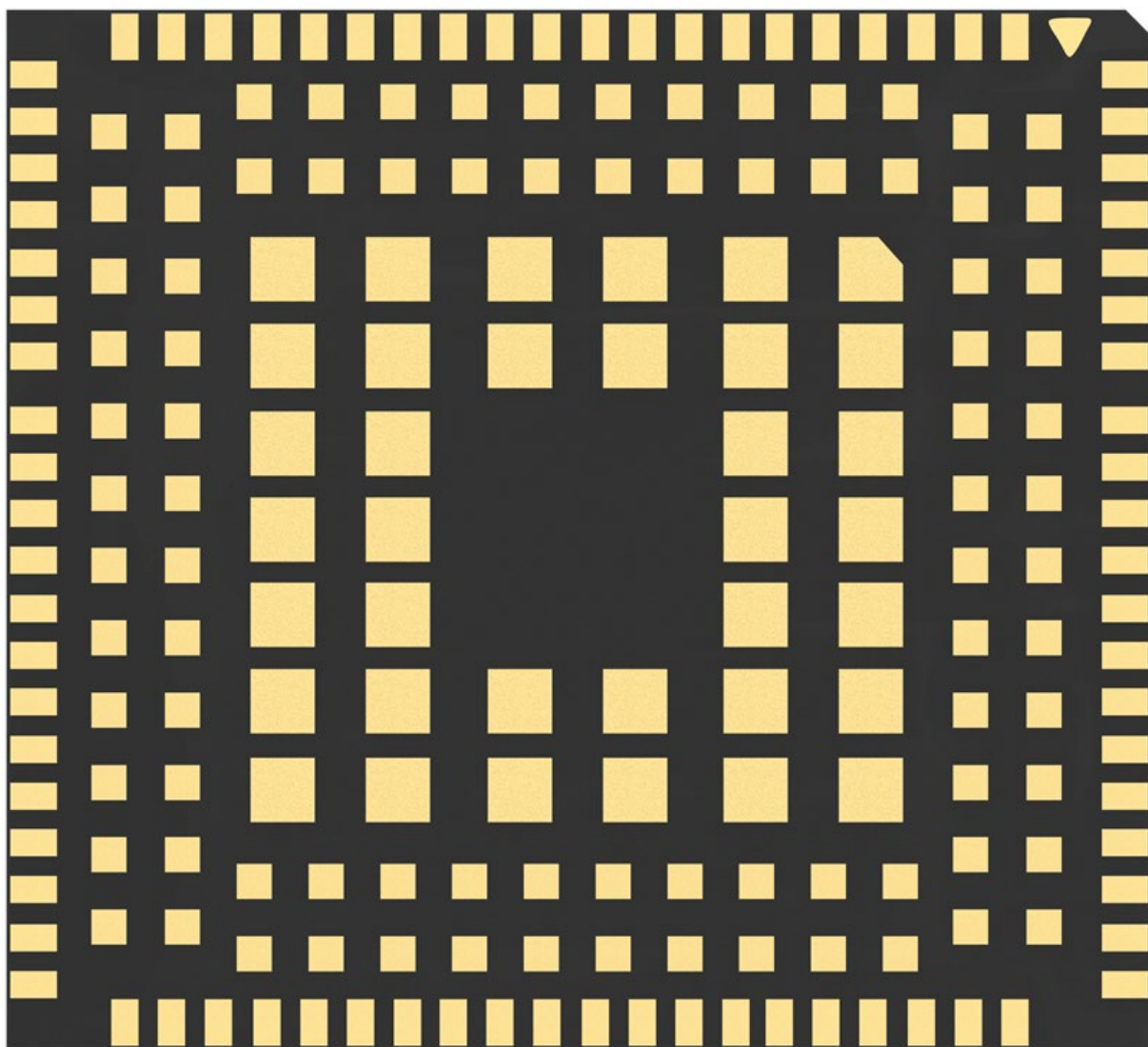


Figure 37 Module Bottom View

8 Storage and Production

8.1 Storage

IQ50 is delivered in a vacuum-sealed bag. The storage of the module must comply with the following conditions:

1. When the ambient temperature is below 40°C and the air humidity is lower than 90%, the module can be stored in a vacuum-sealed bag for 12 months;

2. After the vacuum-sealed bag is opened, you can directly conduct solder reflow or other high-temperature processes for the module if the following conditions are met:

- The air humidity for module storage is lower than 10%;
- The ambient temperature of the module is lower than 30°C, the air humidity is lower than 60%, and the factory completes the placement within 72 hours.

3. If the module is in the following conditions, it needs to be baked before placement:

- When the ambient temperature is 23°C (± 5 °C fluctuations are allowed), the humidity displayed by the humidity indicator card is greater than 10%;
- After the vacuum-sealed bag is opened, the ambient temperature of the module is lower than 30°C and the air humidity is lower than 60%, but the factory fails to complete the placement within 72 hours;
- After the vacuum-sealed bag is opened, the air humidity for module storage is greater than 10%.

4. If the module needs to be baked, bake it for 48 hours at 125°C (± 5 °C fluctuations are allowed).

Note: The package of the module cannot withstand such high temperature, please remove the package of the module before the module is baked.

8.2 Production Welding



Figure 38 Temperature Curve of Solder Reflow

9 Annex A Reference Documents and Abbreviations

9.1 Reference Documents

- IQ50 module specifications
- IQ50 AT command set
- IQ50 reference design circuit
- IQ50 B Application service process manual

9.2 Abbreviations

Table 39 Abbreviations

Abbreviations	Description
AMR	Adaptive Multi-rate
BER	Bit Error Rate
BTS	Base Transceiver Station
PCI	Peripheral Component Interconnect
CS	Circuit Switched (CS) domain
CSD	Circuit Switched Data
DCE	Data communication equipment
DTE	Data terminal equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM

EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FR	Frame Relay
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSPA	HSPA High-Speed Packet Access
HSPA+	HSPA High-Speed Packet Access+
IEC	International Electro-technical Commission
IMEI	International Mobile Equipment Identity
MEID	Mobile Equipment Identifier
I/O	Input/Output
ISO	International Standards Organization
ITU	International Telecommunications Union
bps	bits per second
LED	Light Emitting Diode
M2M	Machine to machine
MO	Mobile Originated
MT	Mobile Terminated
NTC	Negative Temperature Coefficient

PC	Personal Computer
PCB	Printed Circuit Board
PCS	Personal Cellular System
PCM	Pulse Code Modulation
PCS	Personal Communication System
PDU	Packet Data Unit
PPP	Point-to-point protocol
PS	Packet Switched
QPSK	Quadrature Phase Shift Keying
SIM	Subscriber Identity Module
TCP/IP	Transmission Control Protocol/ Internet Protocol
UART	Universal asynchronous receiver-transmitter
USIM	Universal Subscriber Identity Module
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
WCDMA	Wideband Code Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TDD-LTE	Time Division Long Term Evolution
FDD-LTE	Frequency Division Duplexing Long Term Evolution
V _{max}	Maximum Voltage Value
V _{norm}	Normal Voltage Value
V _{min}	Minimum Voltage Value
V _{IHmax}	Maximum Input High Level Voltage Value
V _{IHmin}	Minimum Input High Level Voltage Value

V_{ILmax}	Maximum Input Low Level Voltage Value
V_{ILmin}	Minimum Input Low Level Voltage Value
V_{OHmax}	Maximum Output High Level Voltage Value
V_{OHmin}	Minimum Output High Level Voltage Value
V_{OLmax}	Maximum Output Low Level Voltage Value
V_{OLmin}	Minimum Output Low Level Voltage Value

Federal Communication Commission Interference Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Caution: (1)Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.(2)This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

RF Exposure Information

This device meets the government's requirements for exposure to radio waves.

This device is designed and manufactured not to exceed the emission limits for exposure to radio frequency (RF) energy set by the Federal Communications Commission of the U.S. Government.

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment. In order to avoid the possibility of exceeding the FCC radio frequency exposure limits, human proximity to the antenna shall not be less than 20 cm during normal operation.

Antenna information

Antenna Specification are as follows:

Type: External Antenna

Gain: 2.15 dBi Max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has

been originally tested and certified with this module. The antenna must be either permanently attached or employ a “unique” antenna coupler.

As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “**Contains FCC ID: 2AQRM-IQ50**”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is FCC authorized only for the specific rule parts (i.e., FCC transmitter rules) listed on the grant. If the original equipment manufacturer markets their host product as compliant with Part 15 Subpart B (when it contains unintentional-radiator digital circuitry), the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.