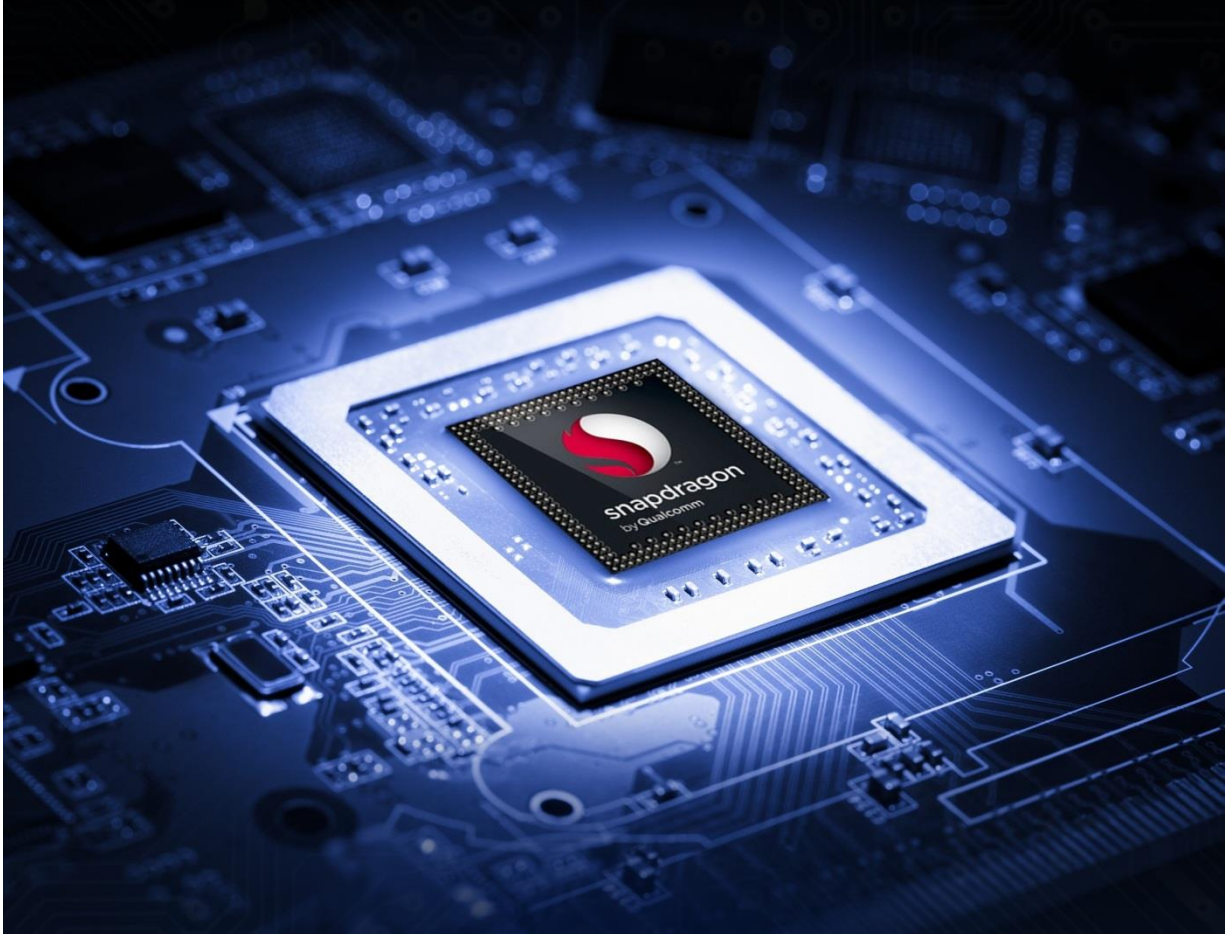
eragon 624

Hardware Reference Manual



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1 Document Details

1.1 Document History

Version	Author		Reviewer		Approver		Description Of Changes
	Name	Date	Name	Review Comment ID	Name	Date	
1.0	*eInfochips*	*18-July 19*	*eInfochips*				*Initial release*

Table 1: Document History

1.2 Definition, Acronyms and Abbreviations

Definition/Acronym/Abbreviation	Description
BLE	Bluetooth Low Energy
BOM	Bill of Material
BT	Bluetooth
CPU	Central Processing Unit
CSI	Camera Serial Interface
DC	Direct Current
DDR	Double Data Rate
DSI	Display Serial Interface
eI	eInfochips
GB	Giga Byte
GPIO	General Purpose Interface
GPS	Global Positioning System
HD	High Definition

HDMI	High Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
Inc.	Incorporated
JTAG	Joint Test Application Group
KB	Kilo Byte
LAN	Local Area Network
LPDDR	Lower Power DDR
MIPI	Mobile protocol working Alliance (not an Acronym)
MISO	Master In Slave Out
MMC	Multi Media Card
MOSI	Master Out Slave In
MP	Mega Pixel
OTG	On The Go
PLL	Phase Loop Locked
PMIC	Power Management IC
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
Rx	Receive
SOM	System On Module
SPI	Serial peripheral Interface
Tx	Transmit

UART	Universal Asynchronous Interface
USB	Universal Serial Bus
ADB	Android Debug Bridge
WLAN	Wireless LAN

Table 2 : Definition, Acronyms and Abbreviations

1.3 References

No.	Document	Version	Remarks
1	ERAGON624 SOM Schematic File	1.3	
2.	ERAGON624 Carrier Schematic File	1.3	

Table 3 : References

2 License Agreement

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3 Preface

This document provides an overview of the ERAGON624 SOM based on Qualcomm's APQ8053 SoC. It provides step-by-step information about hardware components and associated software release Android 8.1.0 (Oreo) used with Carrier KIT.

3.1 Intended Audience

This document is intended for technically qualified personnel. It is not intended for general audiences.

3.2 Intended Use

The development platform supports a wide range of industry interfaces and offers a comprehensive hardware and software design. It comes with Android software packages. This platform enables developers to evaluate and create solutions targeted at various market segments while customers and OEMs can build their products based on these designs directly or with customizations.

4 Overview

The ERAGON624 SoM provides an ideal building block for simple integration with a wide range of products in target markets requiring rich multimedia functionality, powerful graphics processing and video capabilities, as well as high-processing power, in a compact, RoHS compliant, fan less, cost effective SoM with low power consumption.

The ERAGON624 SoM leverages cutting edge mobile computing for embedded and industrial product designs, based on the Qualcomm Snapdragon™ 624 (APQ8053) 1.8 GHz octacore CPU, high performance Adreno™ 506 GPU and a dedicated DSP for advanced A/V processing.

The SOM is equipped with full range of interfaces available in the Qualcomm Snapdragon APQ8053 SoC, which are routed on the 300 pins of three (100 pins each) board-to-board connectors.

The APQ8053 SOM supports Android Oreo operating system

The ERAGON624 SoM is ideal for rapid prototyping of product which can be used in customized carried Board with same Pin-out by end customer. With support for almost all the peripherals, it reduces the design time of innovative applications and helps to achieve early time to market. With variety of peripherals, SOM is targeted for wide range of applications supporting bulk storage, faster connectivity, higher through put and performance at lower power.

4.1 Key Features

CPU
• Qualcomm Snapdragon 624
• Octa-core ARM® Cortex® A53 at up to 1.8 GHz per core.
• Both quad's with 512KB L2 cache
• 64-Bit processor
• Qualcomm Adreno 506 GPU.
• 1920 x 1080p video encoding/ decoding capability
• Dual 14 bit ISP(Image Signal Processing)
• Qualcomm Hexagon™ DSP
	Audio
	• **Input:**
	  ○ 6x Analog mic (WCD9335 Codec)
	  ○ 3xDigital mic (WCD9335 Codec)
	  ○ 2x Analog mic (PMIC Codec)
	  ○ 1xDigital mic (PMIC Codec)
	• **Output:**
	  ○ 1x Stereo Headset Output(WCD9335 Codec)
	  ○ 2x Speaker Output(WCD9335 Codec)
	  ○ 1x Earphone output(WCD9335 Codec)
	  ○ 2x Lineout(WCD9335 Codec)
	  ○ 1x Speaker Output(PMIC Codec)
	  ○ 1x Earphone output(PMIC Codec)
	  ○ 1x Lineout(PMIC Codec)

Memory • **RAM:** Up to 4GB LPDDR3 at up to 933 MHz clock • **Storage:** Up to 64 GB eMMC	**Connectivity** • WLAN 802.11 b/g/n 2.4GHz and 802.11 a/n/ac 5GHz • Bluetooth 4.2 • GPS
Camera • 3xMIPI CSI 4 Lane Camera Interface (Only two can work simultaneously).	**Display** • 2 X MIPI DSI 4 Lane Display Interface • Resolution up to FHD 1920 x 1200, 60fps
Operating System • Android 8.1.0	**Multimedia** • Audio and Video as mention above
USB & SD Card Interface • 1x USB 3.0 or 2.0 Port • SD Card (SDC2 - 4 bit)	**Miscellaneous** 2x UART, 1x I2C, 2x MI2S, 1x SPI, 2x GPIO's on LS-Expansion Connector.

Power Input & Consumption
 	
Voltage In: 3.8V (VBATT+) on J4805 connector from Carrier Board (J13)
	Physical & Operating Characteristics
	• **Dimension:**
	  ○ SOM: 60mm x 35mm
	• **Storage Temperature Range:**
	  ○ -20 to 70° C
	• **Operating Temperature Range:**
	  ○ 0 to 60° C

4.2 Applications

The ERAGON624 SoM is used in a wide range of products across many different target markets. Some of the typical applications are:

- Consumer Electronics
- Internet of Things
- Marine
- Automotive
- Domestic Robot
- Digital signage
- Security & Surveillance
- Biometric Access Control Systems
- Home and Health Hub
- Human-machine interface
- Home energy management systems
- In-flight entertainment
- Intelligent industrial control systems
- Portable medical

5 Getting Started

5.1 Prerequisites

Before user power up the ERAGON 624 SOM board for the first time, will need following things:

- Eragon 624 Carrier Board or Carrier Board with Exact Pin-outs and mating connectors
- WiFi BT U.FL connector on SOM should be connected to Antenna on Carrier Board
- Power input to Custom made Carrier/ Eragon 624 Carrier Board
- Display board embraces 1080p OTM1901A LCD and multi touch capacitive touch panel on Carrier board if provision is given.
- FFC Cable for connecting LCD display to the ERAGON 624 Board.

5.2 Starting the Eragon624 SOM for the first time with Eragon624 Carrier

To start the board, follow these simple steps:

Step 1. First, connect the ERAGON 624 Board to the Display board through FFC cable (DSI cable)

Step 2. Connect the Micro USB cable to connector J22 of carrier card

Step 3. Ensure that the boot switches SW1 are set to '000', all in off position.

Step 4. Connect the complaint power supply to power connector J23.

Step 5. Press switch SW6 on carrier card for 2-3 seconds and then release.

Now board is in the booting process.

Please note that the first boot takes several minutes due to Androids initialization. Subsequent boot times should be faster.

6 System Block Diagram

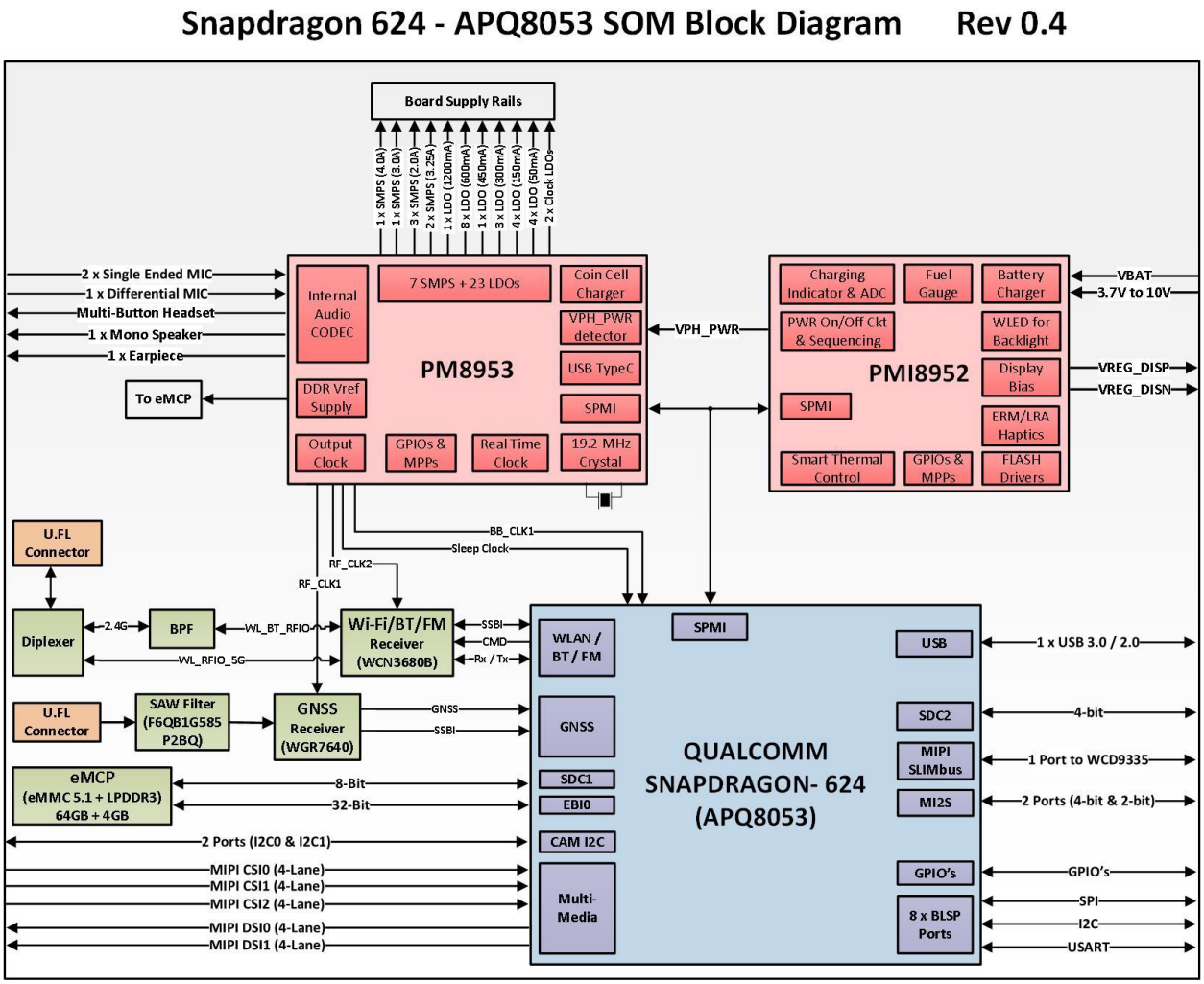

Figure 1 – ERAGON 624 SOM Block Diagram

6.1 ERAGON624 BOARD IMAGE

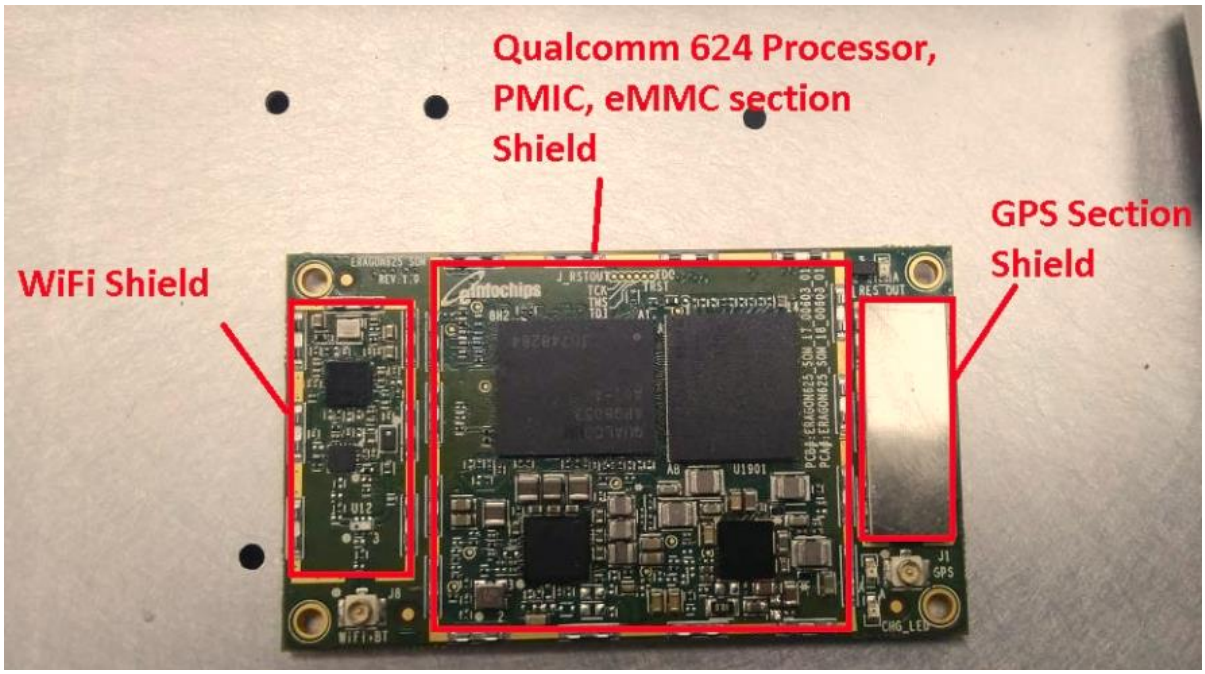

Figure 2 – ERAGON624 SOM Top View

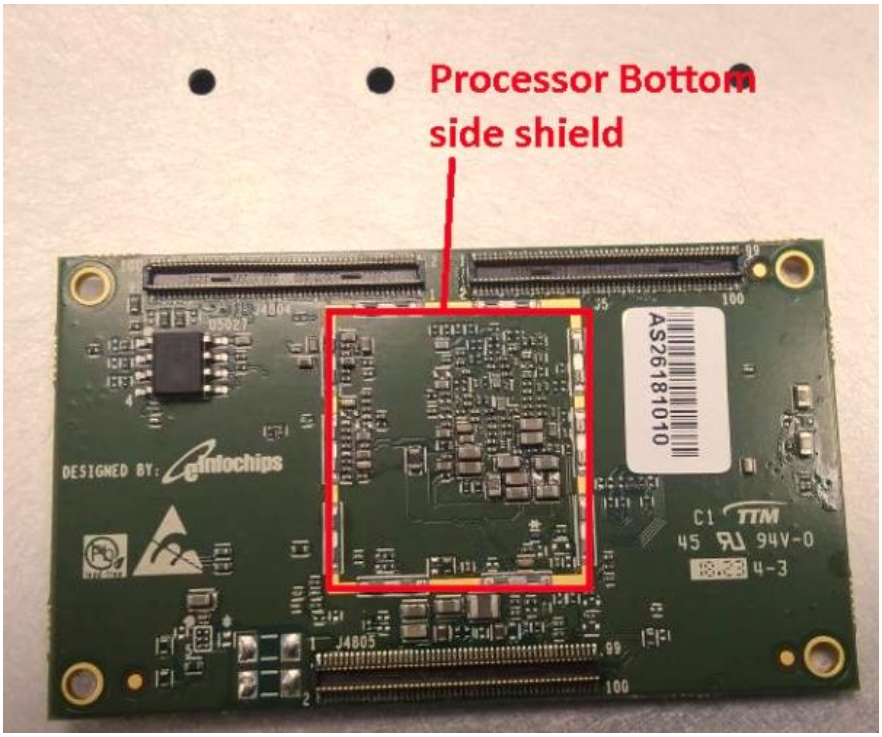

Figure 3 – ERAGON624 SOM BOT View

The ERAGON 624 SOM offers a wide boost of interfaces and peripherals, including several high-speed signals through its edge connectors.

The ERAGON624 SOM and Carrier are interfaced through three Hirose **DF40C-100DP-0.4V** Connectors. The pin outs for these three connectors is described below,

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J5.1	J11.1	CSI0_CAM_GPIO_1	CSI0 Camera GPIO	1.8V
J5.2	J11.2	CSI1_CAM_GPIO_1	CSI1 Camera GPIO	1.8V
J5.3	J11.3	CSI0_CAM_GPIO_2	CSI0 Camera GPIO	1.8V
J5.4	J11.4	CSI1_CAM_GPIO_2	CSI0 Camera GPIO	1.8V
J5.5	J11.5	CSI0_PWDN	CSI0 Power Down Signal	1.8V
J5.6	J11.6	CSI2_CAM_GPIO_1	CSI2 Camera GPIO	1.8V
J5.7	J11.7	CSI0_RST	CSI0 Camera Reset Signal	1.8V
J5.8	J11.8	CSI2_CAM_GPIO_2	CSI2 Camera GPIO	1.8V
J5.9	J11.9	CSI2_PWDN	CSI2 Camera Power Down signal	1.8V
J5.10	J11.10	GND	Ground	-
J5.11	J11.11	CSI2_RST	CSI2 Camera Reset Signal	1.8V
J5.12	J11.12	MIPI_CSI2_CLK_N	MIPI CSI2 Clock Negative	-
J5.13	J11.13	GND	Ground	-
J5.14	J11.14	MIPI_CSI2_CLK_P	MIPI CSI2 Clock Positive	-
J5.15	J11.15	MIPI_CSI1_CLK_P	MIPI CSI1 Clock Positive	-
J5.16	J11.16	GND	Ground	-
J5.17	J11.17	MIPI_CSI1_CLK_N	MIPI CSI1 Clock Negative	-
J5.18	J11.18	MIPI_CSI2_LANE1_P	MIPI CSI2 Lane 1 Positive	-
J5.19	J11.19	GND	Ground	-
J5.20	J11.20	MIPI_CSI2_LANE1_N	MIPI CSI2 Lane 1 Negative	-
J5.21	J11.21	MIPI_CSI1_LANE0_N	MIPI CSI1 Lane 0 Negative	-
J5.22	J11.22	GND	Ground	-
J5.23	J11.23	MIPI_CSI1_LANE0_P	MIPI CSI1 Lane 0 Positive	-
J5.24	J11.24	MIPI_CSI2_LANE0_N	MIPI CSI2 Lane 0 Negative	-
J5.25	J11.25	GND	Ground	-

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J5.26	J11.26	MIPI_CSI2_LANE0_P	MIPI CSI2 Lane0 Positive	-
J5.27	J11.27	MIPI_CSI1_LANE1_P	MIPI CSI1 Lane 1 Positive	-
J5.28	J11.28	GND	Ground	-
J5.29	J11.29	MIPI_CSI1_LANE1_N	MIPI CSI1 Lane 1 Negative	-
J5.30	J11.30	MIPI_CSI2_LANE2_P	MIPI CSI2 Lane 2 Positive	-
J5.31	J11.31	GND	Ground	-
J5.32	J11.32	MIPI_CSI2_LANE2_N	MIPI CSI2 Lane 2 Negative	-
J5.33	J11.33	MIPI_CSI1_LANE2_P	MIPI CSI1 Lane 2 Postive	-
J5.34	J11.34	GND	Ground	-
J5.35	J11.35	MIPI_CSI1_LANE2_N	MIPI CSI1 Lane 2 Negative	-
J5.36	J11.36	MIPI_CSI2_LANE3_P	MIPI CSI2 Lane 3 Positive	-
J5.37	J11.37	GND	Ground	-
J5.38	J11.38	MIPI_CSI2_LANE3_N	MIPI CSI2 Lane 3 Negative	-
J5.39	J11.39	MIPI_CSI1_LANE3_P	MIPI CSI1 Lane 3 Positive	-
J5.40	J11.40	GND	Ground	-
J5.41	J11.41	MIPI_CSI1_LANE3_N	MIPI CSI1 Lane 3 Negative	-
J5.42	J11.42	MIPI_DSI1_CLK_N	MIPI DSI1 Clock Negative	-
J5.43	J11.43	GND	Ground	-
J5.44	J11.44	MIPI_DSI1_CLK_P	MIPI DSI1 Clock Positive	-
J5.45	J11.45	MIPI_CSI0_CLK_P	MIPI CSI0 Clock Positive	-
J5.46	J11.46	GND	Ground	-
J5.47	J11.47	MIPI_CSI0_CLK_N	MIPI CSI0 Clock Negative	-
J5.48	J11.48	MIPI_DSI1_LANE0_N	MIPI DSI1 Lane0 Negative	-
J5.49	J11.49	GND	Ground	-
J5.50	J11.50	MIPI_DSI1_LANE0_P	MIPI DSI1 Lane0 Positive	-

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J5.51	J11.51	MIPI_CSI0_LANE0_N	MIPI CSI0 Lane0 Negative	-
J5.52	J11.52	GND	Ground	-
J5.53	J11.53	MIPI_CSI0_LANE0_P	MIPI CSI0 Lane0 Positive	-
J5.54	J11.54	MIPI_DSI1_LANE1_P	MIPI DSI1 Lane1 Positive	-
J5.55	J11.55	GND	Ground	-
J5.56	J11.56	MIPI_DSI1_LANE1_N	MIPI DSI1 Lane1 Negative	-
J5.57	J11.57	MIPI_CSI0_LANE1_P	MIPI CSI0 Lane1 Positive	-
J5.58	J11.58	GND	Ground	-
J5.59	J11.59	MIPI_CSI0_LANE1_N	MIPI CSI0 Lane1 Negative	-
J5.60	J11.60	MIPI_DSI1_LANE2_N	MIPI DSI1 Lane2 Negative	-
J5.61	J11.61	GND	Ground	-
J5.62	J11.62	MIPI_DSI1_LANE2_P	MIPI DSI1 Lane2 Positive	-
J5.63	J11.63	MIPI_CSI0_LANE2_P	MIPI CSI0 Lane2 Positive	-
J5.64	J11.64	GND	Ground	-
J5.65	J11.65	MIPI_CSI0_LANE2_N	MIPI CSI0 Lane2 Negative	-
J5.66	J11.66	MIPI_DSI1_LANE3_P	MIPI DSI1 Lane3 Positive	-
J5.67	J11.67	GND	Ground	-
J5.68	J11.68	MIPI_DSI1_LANE3_N	MIPI DSI1 Lane3 Negative	-
J5.69	J11.69	MIPI_CSI0_LANE3_P	MIPI CSI0 Lane3 Positive	-
J5.70	J11.70	GND	Ground	-
J5.71	J11.71	MIPI_CSI0_LANE3_N	MIPI CSI0 Lane3 Negative	-
J5.72	J11.72	MIPI_DSI0_CLK_N	MIPI DSI0 Clock Negative	-
J5.73	J11.73	GND	Ground	-
J5.74	J11.74	MIPI_DSI0_CLK_P	MIPI DSI0 Clock Positive	-
J5.75	J11.75	CSI1_RST	CSI1 Reset GPIO Signal	1.8V

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J5.76	J11.76	GND	Ground	-
J5.77	J11.77	CSI1_PWDN	CSI1 Power Down GPIO Signal	1.8V
J5.78	J11.78	MIPI_DSI0_LANE0_N	MIPI DSI0 Lane0 Negative	-
J5.79	J11.79	CSI_I2C1_SCL	CCI1 Camera I2C Clock Signal	1.8V
J5.80	J11.80	MIPI_DSI0_LANE0_P	MIPI DSI0 Lane0 Positive	-
J5.81	J11.81	CSI_I2C1_SDA	CCI1 Camera I2C Data Signal	1.8V
J5.82	J11.82	GND	Ground	-
J5.83	J11.83	CSI_I2C0_SCL	CCI0 Camera I2C Clock Signal	1.8V
J5.84	J11.84	MIPI_DSI0_LANE1_P	MIPI DSI0 Lane1 Positive	-
J5.85	J11.85	CSI_I2C0_SDA	CCI0 Camera I2C Data Signal	1.8V
J586	J11.86	MIPI_DSI0_LANE1_N	MIPI DSI0 Lane1 Negative	-
J5.87	J11.87	CAM_MCLK2	24Mhz Master Clock 2 signal	1.8V
J5.88	J11.88	GND	Ground	-
J5.89	J11.89	GND	Ground	-
J5.90	J11.90	MIPI_DSI0_LANE3_N	MIPI DSI0 Lane3 Negative	-
J5.91	J11.91	CAM_MCLK3	24Mhz Master Clock 3 signal	1.8V
J5.92	J11.92	MIPI_DSI0_LANE3_P	MIPI DSI0 Lane3 Positive	-
J5.93	J11.93	GND	Ground	-
J5.94	J11.94	GND	Ground	-
J5.95	J11.95	CAM_MCLK1	24Mhz Master Clock 1 signal	1.8V
J5.96	J11.96	MIPI_DSI0_LANE2_P	MIPI DSI0 Lane2 Positive	-
J5.97	J11.97	GND	Ground	-
J5.98	J11.98	MIPI_DSI0_LANE2_N	MIPI DSI0 Lane2 Negative	-
J5.99	J11.99	CAM_MCLK0	24Mhz Master Clock 0 signal	1.8V
J5.100	J11.100	GND	Ground	-

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4805.1	J13.1	VBAT	3.5V-4.4V Input voltage	3.8
J4805.2	J13.2	VBAT	3.5V-4.4V Input voltage	3.8
J4805.3	J13.3	VBAT	3.5V-4.4V Input voltage	3.8
J4805.4	J13.4	VBAT	3.5V-4.4V Input voltage	3.8
J4805.5	J13.5	VBAT	3.5V-4.4V Input voltage	3.8
J4805.6	J13.6	VBAT	3.5V-4.4V Input voltage	3.8
J4805.7	J13.7	VBAT	3.5V-4.4V Input voltage	3.8
J4805.8	J13.8	VBAT	3.5V-4.4V Input voltage	3.8
J4805.9	J13.9	VBAT	3.5V-4.4V Input voltage	3.8
J4805.10	J13.10	VBAT	3.5V-4.4V Input voltage	3.8
J4805.11	J13.11	VBAT	3.5V-4.4V Input voltage	3.8
J4805.12	J13.12	VBAT	3.5V-4.4V Input voltage	3.8
J4805.13	J13.13	VBAT	3.5V-4.4V Input voltage	3.8
J4805.14	J13.14	VBAT	3.5V-4.4V Input voltage	3.8
J4805.15	J13.15	VBAT	3.5V-4.4V Input voltage	3.8
J4805.16	J13.16	VBAT	3.5V-4.4V Input voltage	3.8
J4805.17	J13.17	GND	Ground	-
J4805.18	J13.18	VBAT	3.5V-4.4V Input voltage	3.8
J4805.19	J13.19	GND	Ground	-
J4805.20	J13.20	GND	Ground	-
J4805.21	J13.21	GND	Ground	-
J4805.22	J13.22	GND	Ground	-
J4805.23	J13.23	GND	Ground	-
J4805.24	J13.24	GND	Ground	-
J4805.25	J13.25	VBUS_USB_IN	USB Input from the USB 3.0 Connector	5

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4805.26	J13.26	GND	Ground	-
J4805.27	J13.27	VBUS_USB_IN	USB Input from the USB 3.0 Connector	5
J4805.28	J13.28	GND	Ground	-
J4805.29	J13.29	VBUS_USB_IN	USB Input from the USB 3.0 Connector	5
J4805.30	J13.30	VSENSE_BATT_M	PMIC VBATT Voltage negative sense input	-
J4805.31	J13.31	VBUS_USB_IN	USB Input from the USB 3.0 Connector	5
J4805.32	J13.32	VSENSE_BATT_P	PMIC VBATT Voltage positive sense input	
J4805.33	J13.33	VBUS_USB_IN	USB Input from the USB 3.0 Connector	5
J4805.34	J13.34	VREF_BAT_THERM	Reference Bias voltage for Battery Thermistor	2.7
J4805.35	J13.35	PMI_CHG_EN	PMI Charge Enable control signal	-
J4805.36	J13.36	BAT_THERM	PMI Battery Thermistor signal	-
J4805.37	J13.37	GND	Ground	-
J4805.38	J13.38	BAT_CON_ID	PMI Battery ID Signal	-
J4805.39	J13.39	USB3_SS_TX_P	USB 3.0 Superspeed transmit positive	-
J4805.40	J13.40	DSI_BACKLIGHT_PWM	Display backlight control signal	1.8
J4805.41	J13.41	USB3_SS_TX_M	USB 3.0 Superspeed transmit negative	-
J4805.42	J13.42	CODEC_DIV_CLK	9.6 MHz Audio codec Master clock	1.8
J4805.43	J13.43	GND	Ground	-
J4805.44	J13.44	CODEC_RST_N	Audio codec Reset signal	1.8
J4805.45	J13.45	USB3_SS_RX_P	USB 3.0 Superspeed receive positive	-
J4805.46	J13.46	AUDIO_INT1	Audio codec interrupt 1	1.8
J4805.47	J13.47	USB3_SS_RX_M	USB 3.0 Superspeed receive negative	-
J4805.48	J13.48	AUDIO_INT2	Audio interrupt 2	1.8
J4805.49	J13.49	GND	Ground	-
J4805.50	J13.50	PMIC_SPKR_DRV_M	PMIC speaker out negative	-

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4805.51	J13.51	USB_HS_D_M	USB2.0 High speed negative	-
J4805.52	J13.52	PMIC_SPKR_DRV_P	PMIC speaker out positive	-
J4805.53	J13.53	USB_HS_D_P	USB2.0 High speed positive	-
J4805.54	J13.54	PMIC_MIC3_IN_P	PMIC MIC3 Input positive	
J4805.55	J13.55	GND	Ground	-
J4805.56	J13.56	PMIC_MIC3_IN_M	PMIC MIC3 Input negative	-
J4805.57	J13.57	LCD_CABC	PMI Backlight control signal	-
J4805.58	J13.58	PMIC_HPH_R	PMIC Headphone right channel	-
J4805.59	J13.59	USB_SNS	PMI USB sense	5
J4805.60	J13.60	PMC_HPH_REF	PMIC Headphone reference	-
J4805.61	J13.61	LCD_BL_LED_K1	Display backlight LED cathode 1	-
J4805.62	J13.62	PMIC_HPH_L	PMIC Headphone left channel	-
J4805.63	J13.63	LCD_BL_LED_K2	Display backlight LED cathode 2	-
J4805.64	J13.64	PMIC_HS_DET	PMIC Headphone detect	-
J4805.65	J13.65	LCD_VSP	Display Bias supply positive	5.5
J4805.66	J13.66	PMIC_MIC2_IN	PMIC MIC2 Input	
J4805.67	J13.67	LCD_VSN	Display Bias supply negative	-5.5
J4805.68	J13.68	GND	Ground	-
J4805.69	J13.69	F_LED1	Flash LED out	-
J4805.70	J13.70	PMIC_MIC1_IN_M	PMIC MIC1 Input negative	-
J4805.71	J13.71	F_LED1	Flash LED out	-
J4805.72	J13.72	PMIC_MIC1_IN_P	PMIC MIC1 Input positive	-
J4805.73	J13.73	LCD_BL_LED_A	Display backlight LED anode	-
J4805.74	J13.74	EAR0_M	Earpiece out negative	-
J4805.75	J13.75	USB_CC1	USB type C input CC1	-

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4805.76	J13.76	EAR0_P	Earpiece out positive	-
J4805.77	J13.77	USB_CC2	USB type C input CC2	-
J4805.78	J13.78	TX_GTR_THRES	GPIO_112	1.8
J4805.79	J13.79	USB_ID	PMI USB ID input	1.8
J4805.80	J13.80	CDC_LO_M	Codec Lineout negative	-
J4805.81	J13.81	GND	Ground	-
J4805.82	J13.82	CDC_LO_P	Codec Lineout positive	-
J4805.83	J13.83	VREG_L2_1P1	PMIC LDO2 output voltage	1.2
J4805.84	J13.84	PMIC_MIC_BIAS1	PMIC MIC Bias 1 voltage out	-
J4805.85	J13.85	VREG_L2_1P1	PMIC LDO2 output voltage	1.2
J4805.86	J13.86	PMIC_MIC_BIAS2	PMIC MIC Bias 2 voltage out	-
J4805.87	J13.87	VREG_L2_1P1	PMIC LDO2 output voltage	1.2
J4805.88	J13.88	EXT_RF_CLK3	19.2 MHz RF clock 3	-
J4805.89	J13.89	USB_VCONN	USB Type C Vconn supply	-
J4805.90	J13.90	VREG_L11_2P95	PMIC LDO11 output voltage	2.95
J4805.91	J13.91	USB_VCONN	USB Type C Vconn supply	-
J4805.92	J13.92	VREG_L11_2P95	PMIC LDO11 output voltage	2.95
J4805.93	J13.93	VREG_L6_1P8	PMIC LDO6 output voltage	1.8
J4805.94	J13.94	VREG_L11_2P95	PMIC LDO11 output voltage	2.95
J4805.95	J13.95	AUDIO_SLIMBUS_CLK	Audio slimbus clock	1.8
J4805.96	J13.96	VCOIN	Coil cell voltage	-
J4805.97	J13.97	AUDIO_SLIMBUS_D0	Audio slimbus Data 0	1.8
J4805.98	J13.98	VREG_L12_VDDPX2_SDC	PMIC LDO12 output voltage	2.95
J4805.99	J13.99	AUDIO_SLIMBUS_D1	Audio slimbus Data 1	1.8
J4805.100	J13.100	VREG_L22_2P8	PMIC LDO22 output voltage	2.8

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4804.1	J16.1	DSI_TOUCH_INT	Display touch interrupt	1.8
J4804.2	J16.2	GND	Ground	-
J4804.3	J16.3	TOUCH_RST	Display touch reset	1.8
J4804.4	J16.4	APQ_BOOT_CONFIG1	Boot config pin 1	1.8
J4804.5	J16.5	FLASH_STROBE_NOW	PMI_MPP_4/Flash strobe	-
J4804.6	J16.6	APQ_BOOT_CONFIG3	Boot config pin 3	1.8
J4804.7	J16.7	LCD_RST_N	Display Reset	1.8
J4804.8	J16.8	APQ_BOOT_CONFIG2	Boot config pin 2	1.8
J4804.9	J16.9	LED_GPIO3	GPIO59/Red LED control	1.8
J4804.10	J16.10	GND	Ground	-
J4804.11	J16.11	GND	Ground	-
J4804.12	J16.12	BLSP1_SPI_MOSI	BLSP1 SPI MOSI	1.8
J4804.13	J16.13	SDC2_SDCARD_D3	SDC2 SDCARD Data 3	1.8/2.95
J4804.14	J16.14	BLSP1_SPI_MISO	BLSP1 SPI MISO	1.8
J4804.15	J16.15	SDC2_SDCARD_D2	SDC2 SDCARD Data 2	1.8/2.95
J4804.16	J16.16	BLSP1_SPI_CS0_N	BLSP1 SPI CS 0	1.8
J4804.17	J16.17	SDC2_SDCARD_D1	SDC2 SDCARD Data 1	1.8/2.95
J4804.18	J16.18	BLSP5_UART_CTS	BLSP5 UART CTS	1.8
J4804.19	J16.19	SDC2_SDCARD_CMD	SDC2 SDCARD command	1.8/2.95
J4804.20	J16.20	BLSP5_UART_RX	BLSP5 UART RX	1.8
J4804.21	J16.21	SDC2_SDCARD_D0	SDC2 SDCARD Data 0	1.8/2.95
J4804.22	J16.22	GND	Ground	-
J4804.23	J16.23	SDC2_SDCARD_CLK	SDC2 SDCARD clock	1.8/2.95
J4804.24	J16.24	HDMI_RST_N	HDMI Reset	1.8
J4804.25	J16.25	SDCARD_DET_N	SDCARD Detect	1.8

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4804.26	J16.26	BLSP1_SPI_CLK	BLSP1 SPI clock	1.8
J4804.27	J16.27	SD_WRITE_PROTECT	Test point	1.8
J4804.28	J16.28	BLSP5_UART_TX	BLSP5 UART TX	1.8
J4804.29	J16.29	GND	Ground	-
J4804.30	J16.30	BLSP5_UART_RTS	BLSP5 UART RTS	1.8
J4804.31	J16.31	USB_SS_SEL	USB switch select	1.8
J4804.32	J16.32	SPKR_AMP_EN2	Speaker amplifier Enable 2	1.8
J4804.33	J16.33	GPIO_140	GPIO 140	1.8
J4804.34	J16.34	nRESET/PME_CLEAR_EXP	LAN7801 reset	1.8
J4804.35	J16.35	TP_I2C_SCL	Display I2C clock	1.8
J4804.36	J16.36	SPKR_AMP_EN1	Speaker amplifier Enable 1	1.8
J4804.37	J16.37	TP_I2C_SDA	Display I2C data	1.8
J4804.38	J16.38	UART_MSM_TX	BLSP2 UART transmit/Debug UART transmit	1.8
J4804.39	J16.39	GND	Ground	-
J4804.40	J16.40	UART_MSM_RX	BLSP2 UART receive/Debug UART receive	1.8
J4804.41	J16.41	DMIC0_CLK	DMIC0 clock	-
J4804.42	J16.42	BLSP2_I2C_SDA	BLSP2 I2C Data	1.8
J4804.43	J16.43	DMIC0_DATA	DMIC0 Data	-
J4804.44	J16.44	BLSP2_I2C_SCL	BLSP2 I2C clock	1.8
J4804.45	J16.45	MAG_DRDY_INT	Magnetometer Interrupt	1.8
J4804.46	J16.46	LED_GPIO2	GPIO9/Blue LED control	1.8
J4804.47	J16.47	GYRO_INT	Gyro meter Interrupt	1.8
J4804.48	J16.48	HDMI_INT_GPIO	GPIO 54/HDMI Interrupt	1.8
J4804.49	J16.49	ACCL_INT1	Accelerometer Interrupt	1.8
J4804.50	J16.50	MI2S_2_D0	MI2S2 Data0	1.8

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4804.51	J16.51	ALSP_INT_N	ALSP sensor interrupt	1.8
J4804.52	J16.52	MI2S_2_D1	MI2S2 Data1	1.8
J4804.53	J16.53	GND	Ground	-
J4804.54	J16.54	MI2S_2_WS	MI2S2 Word Sync clock	1.8
J4804.55	J16.55	VREG_L5_1P8	PMIC LDO5 output	1.8
J4804.56	J16.56	MI2S_2_SCK	MI2S2 clock	1.8
J4804.57	J16.57	VREG_L5_1P8	PMIC LDO5 output	1.8
J4804.58	J16.58	BLSP4_UART_TX	BLSP4 UART transmit	1.8
J4804.59	J16.59	GND	Ground	-
J4804.60	J16.60	BLSP4_UART_RX	BLSP4 UART receive	1.8
J4804.61	J16.61	WDOG_DISABLE	Watchdog disable	1.8
J4804.62	J16.62	BLSP4_I2C_SDA	BLSP4 I2C Data	1.8
J4804.63	J16.63	USB_HUB_RST_N	USB HUB reset	1.8
J4804.64	J16.64	BLSP4_I2C_SCL	BLSP4 I2C clock	1.8
J4804.65	J16.65	MI2S_1_D3	MI2S1 Data3	1.8
J4804.66	J16.66	LED_GPIO1	GPIO8/Green LED control	1.8
J4804.67	J16.67	MI2S_1_D0	MI2S1 Data0	1.8
J4804.68	J16.68	MI2S_1_SCK	MI2S1 clock	1.8
J4804.69	J16.69	MI2S_1_WS	MI2S1 Word Sync	1.8
J4804.70	J16.70	MI2S_1_D2	MI2S1 Data2	1.8
J4804.71	J16.71	MAG_INT	Magnetometer Interrupt	1.8
J4804.72	J16.72	MI2S_1_D1	MI2S1 Data1	1.8
J4804.73	J16.73	TEMP_INT	Temperature sensor Interrupt	1.8
J4804.74	J16.74	GND	Ground	-
J4804.75	J16.75	FORCE_USB_BOOT	Force USB Boot	1.8

SOM Pin No.	Carrier Board Pin Number	Signal Name	Default Pin Function	Operating Voltage Level
J4804.76	J16.76	BLSP6_I2C_SDA	BLSP6 I2C Data	1.8
J4804.77	J16.77	KEY_SNAPSHOT	GPIO86/HDMI Hot Plug detect	1.8
J4804.78	J16.78	BLSP6_I2C_SCL	BLSP6 I2C clock	1.8
J4804.79	J16.79	KEY_VOL_UP_N	GPIO85/ Volume Up key	1.8
J4804.80	J16.80	BLSP6_UART_TX	BLSP6 UART transmit	1.8
J4804.81	J16.81	BLSP8_SPI_CS0_N	BLSP8 SPI CS0	1.8
J4804.82	J16.82	BLSP6_UART_RX	BLSP6 UART receive	1.8
J4804.83	J16.83	KEY_FOCUS	GPIO87/HDMI Interrupt	1.8
J4804.84	J16.84	BLSP8_SPI_CLK	BLSP8 SPI clock	1.8
J4804.85	J16.85	PMI_WLED_EN_N	PMI White LED Enable	-
J4804.86	J16.86	BLSP8_SPI_MOSI	BLSP8 SPI MOSI	1.8
J4804.87	J16.87	GND	Ground	-
J4804.88	J16.88	BLSP8_SPI_MISO	BLSP8 SPI MISO	1.8
J4804.89	J16.89	GND	Ground	-
J4804.90	J16.90	GND	Ground	-
J4804.91	J16.91	PRI_MI2S_MCLK_A	MI2S mater clock A	1.8
J4804.92	J16.92	PM_RESIN_N1	PM Reset input/ Volume Down	-
J4804.93	J16.93	GND	Ground	-
J4804.94	J16.94	KYPD_PWR_N1	Power ON key	1.8
J4804.95	J16.95	PRI_MI2S_MCLK_B	MI2S mater clock B	1.8
J4804.96	J16.96	GND	Ground	-
J4804.97	J16.97	GND	Ground	-
J4804.98	J16.98	PMI_HAP_OUT_N	PMI Haptics Out negative	-
J4804.99	J16.99	PRI_MI2S_MCLK_C	MI2S mater clock C	1.8
J4804.100	J16.100	PMI_HAP_OUT_P	PMI Haptics Out positive	-

6.2 Major Blocks of ERAGON624 SOM Module

6.2.1 Processor APQ8053 - Features and interfaces

- The Qualcomm APQ8053 includes a customized 64-bit ARM Cortex-A53, 1.8GHz high performance Octacore Processor.
- It embraces Qualcomm Adreno™ 506 Graphics Processing Unit; up to 650MHz 3D graphics accelerator with 64-bit addressing.
- Qualcomm Hexagon™ DSP to support always-on use cases.
- 512kB L2 cache memory

Memory Support Features

- Non-PoP LPDDR3 SDRAM; 32-bit wide; up to 933MHz RAM through EBI interface.
- Support up to 64GB external eMMC v5.1 memory via SDC1 interface.
- There is SD card connector also available on carrier card for external storage devices interfaced through SDC2.

Multimedia features

- Supports Three 4 Lane CSI Ports at 2.1 Gbps per lane data rate; however only two can work concurrently; as it has only two ISPs
- All three MIPI CSI ports supports up to 21MP CMOS and CCD sensors.
- Dual FHD (1900x1200) 60fps 4 Lane MIPI DSI ports supported.
- Support 1080p at 90fps video encoding.
- Two MI2S Ports for Audio interface.
- Processor supports one port SLIMbus interface to WCD9335 codec.
- APQ8053 also support CDC PDM port to interface with PM8953 for audio applications.

Web technologies

- V8 JavaScript Engine optimizations
- Webkit browser JPEG hardware decode acceleration
- Networking Stack IP and HTTP tuning
- Flash 10.x and video processor decode optimization.

Connectivity

- 8, 4-bits each BLSP Ports which can be configured as UART, I2C and SPI.
- One USB 3.0/2.0 Port.
- Gigabit Ethernet connectivity on Carrier card in USB3.0 HOST mode.

Wireless Connectivity

- With WCN3680B, it supports 802.11 b/g/n mode for 2.4GHz band and with external FEM module; it supports 802.11 a/n/ac mode for 5GHz band.
- WCN3680B also supports Bluetooth 4.2 LE and earlier.
- With WGR7640 receiver, APQ8053 supports GPS location suite.

Power Management

- Combination of PM8953 and PMI8952 interfaced through two 2-line SPMI.
- Dedicated clock and reset lines; plus other GPIOs as needed.

6.2.2 Memory Interface

In ERAGON 624 SOM APQ8053 integrates with single Embedded Multi Chip Package (eMCP) has dual function of LPDDR3 RAM and eMMC v5.1 flash. SOM supports up to 4GB of LPDDR3 RAM at max. 933MHz clock and 64GB of eMMC flash.

- The LPDDR3 has 32-bit wide bus width interfaced with APQ8053 through EBI.
- The eMMC v5.1 has 8-bit wide bus width interfacing with APQ8053 through SDC1 interface.

6.2.3 Wi-Fi + BT Interface

The ERAGON 624 board deployed Qualcomm's RF chip WCN3680B solution that integrates two different wireless connectivity technologies into a single device, the interfaces are:

- Dual-band 2.4GHz and 5GHz WLAN compliant with IEEE 802.11 a/b/g/n specifications and supports external PA for both bands. ERAGON624 uses external PA at 5GHz band which also supports IEEE802.11 ac mode for data rate up to MCS 9. .
- Bluetooth compliant with the BT specifications version 4.2 (BR/EDR + BLE).

All above RF signal is routed through a single antenna. To connect external antenna on ERAGON 624 SOM board, U.FL connector is provided. In addition, support for **chip antenna (PN# FR05-S1-NO-1-004 ; Gain of 1.5dBi on 2.4GHz & 4.7dBi on 5GHz)** is given on ERAGON 624 carrier card. In this case, RF signal from SOM to carrier is carried through U.FL to U.FL cable.

6.2.4 GPS Interface

The ERAGON 624 board supports GPS interface, for which APQ8053 is interfaced with Qualcomm's GNSS receiver chip WGR7640. U.FL connector is provided on both SOM and Carrier card which are connected through U.FL to U.FL cable. On carrier card **GPS chip antenna (PN# 1575AT54A0010 ; Peak gain = 1.3dBi)** is used to receive GPS signals. Also we can connect external antenna on U.FL connector on SOM module.

6.2.5 PMIC Interface

ERAGON624 SOM module has combination of PM8953 and PMI8952 for Power management. Both the PMICs are interfaced to APQ8053 through two-line SPMI bus.

6.2.6 System LEDs

There are three notification LEDs provided on SOM module as described below,

- LED2 (APQ reset out LED): It's glow indicates that processor came out of reset and booted successfully.
- LED3 (Charging LED): Indicates battery charging.
- LED4 (Green LED): Indicates that VPH power supply generated.

6.2.7 Shielding

Shields are Mounted on the WiFi (Top) Section, Processor + PMIC + eMMC (Top/Bottom) section & GPS section (Top), as per the FCC requirement for Single Module Certification.

6.3 Guidelines to Design Carrier Board

6.3.1 Power Supply

ERAGON624 SOM can be powered through 3.8V@4.2A DC input to give power to VBAT pins (as per pin-outs table between SOM & Carrier).

6.3.2 Boot Configuration

The ERAGON624 can be configured to function in different modes placing the switch on carrier card.

Below schematic can be followed for Boot configuration:

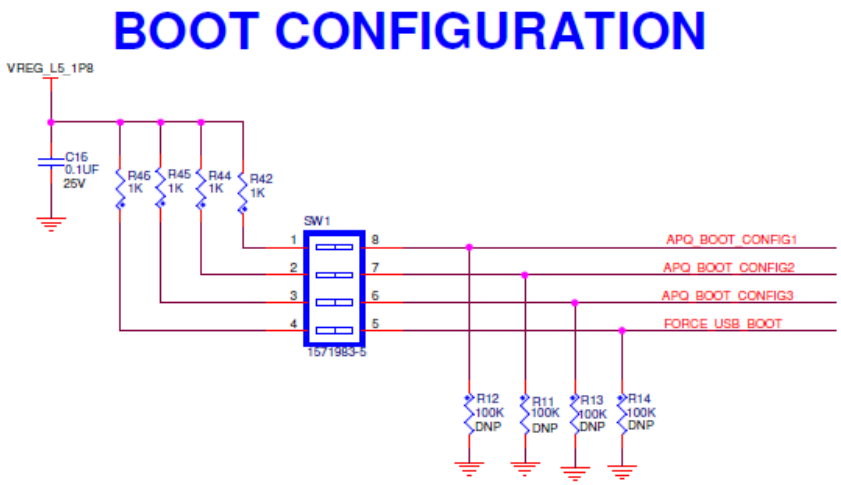

Figure 4 – Boot Configuration Switch (SW1) schematic

Below table mentions different boot configurations options,

CONFIG_1 (Position-1)	CONFIG_2 (Position-2)	CONFIG_3 (Position-3)	FORCE_USB_BOOT (Position-4)	Function
0	0	0	0	SDC1 -> SDC2 -> USB 3.0
0	1	0	0	SDC2 -> SDC1 -> USB 3.0
0	1	1	0	SDC1 -> USB 3.0
0	0	0	1	USB 3.0

Table 4: ERAGON 624 BOOT Configuration options

CONFIG switch in ON position indicates level 1. To boot through eMCP make sure switch is 0000.

Figure 5 – Boot Configuration Switch (SW1)

6.3.3 General Purpose Keys (as per Eragon624 Carrier Board)

There are three general-purpose keys provided on carrier card. Their applications are as below,

- SW6 (Power ON/Sleep mode switch): After power ON the board, this key need to be press for 2-3 seconds to boot SOM module. Also if board goes in the sleep mode, then by pressing SW6 we can get board out of sleep mode.
- SW5 (Volume up): This key is pressed to up the volume of media.
- SW4 (Fast boot switch or Volume down): This switch is pressed to get processor into Fast boot mode or to reduce the volume of media.

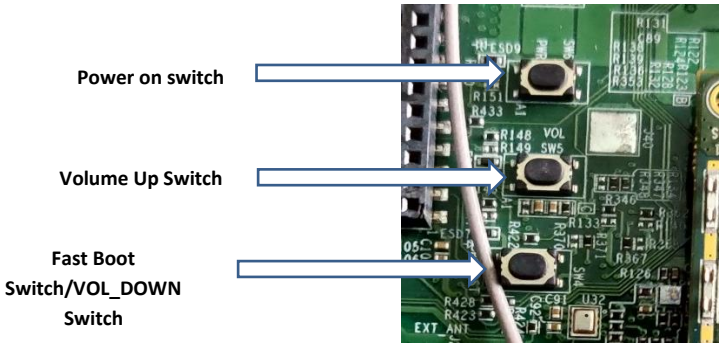

Figure 6 – General Purpose Keys

6.3.4 USB Interface

APQ8053 supports one USB2.0 high speed and one USB3.0 Super speed Port that comes to Carrier card through B2B connector. USB3.0 can be further used for ADB/OTG mode for debug purpose.

USB signals can further be used for Gigabit Ethernet (By using USB to Ethernet converter) for USB pen-drives or OTG purpose.

6.3.5 Audio Interface

ERAGON624 SOM can support PMIC's internal codec. On the carrier Board, WCD9335 daughter board (**eI PN# 17_00348_01**) can be connected by Placing connector **PN# DF40HC(3.0)-30DS-0.4V(51)**. This daughter board also has WSA8810 audio amplifier interfaced with codec.

ERAGON624 supports 5 analog MICs,1 headset MIC, 3 Digital MICs, 2 stereo speaker outputs, 1 headset output, 1 Earpiece output, 2 Line outputs and all these peripherals excluding can be connected on headset connector J19, Female headers J17 & J18. These Provisions can be given to carrier board for Audio interfaces.

Figure 7 – WCD9335 Audio Code Daughter Board (custom made by eInfochips)

Below is the Schematic portion for J28 & J29 to connect the Audio Daughter Board. For layout spacing, need to contact to eInfochips.

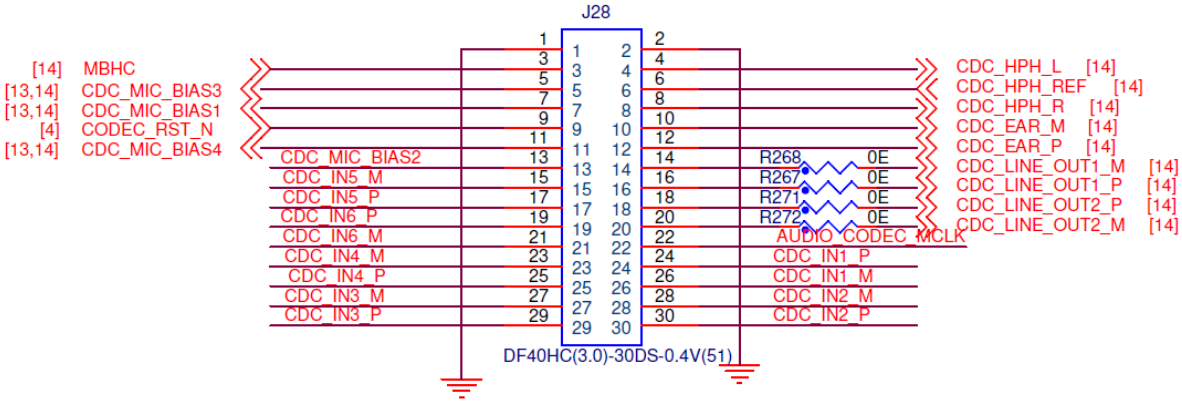

Figure 8 – Schematic-1 on Carrier Board for Audio Code Daughter Board

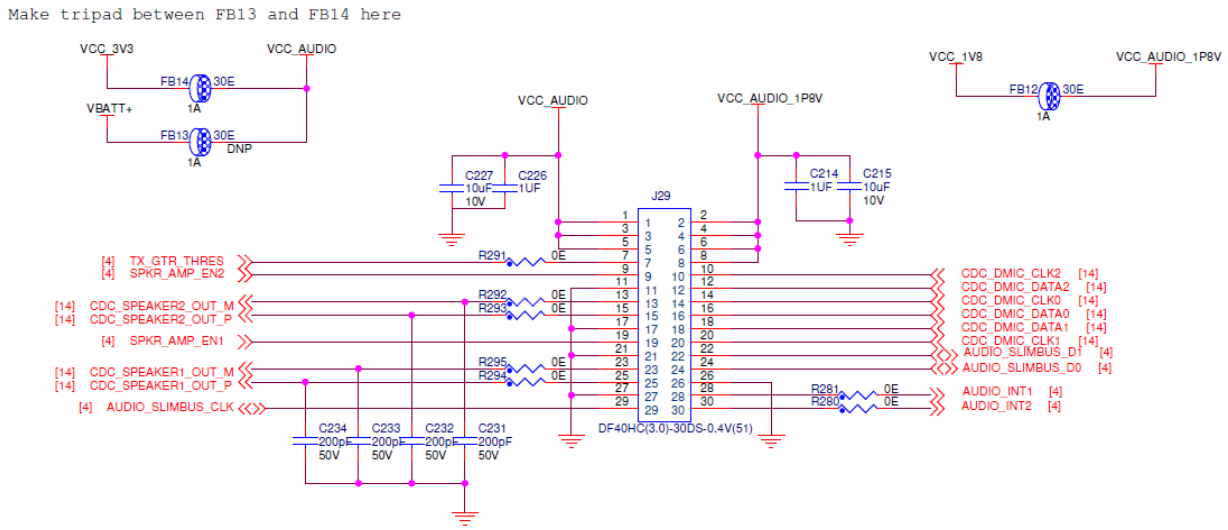

Figure 9 – Schematic-2 on Carrier Board for Audio Code Daughter Board

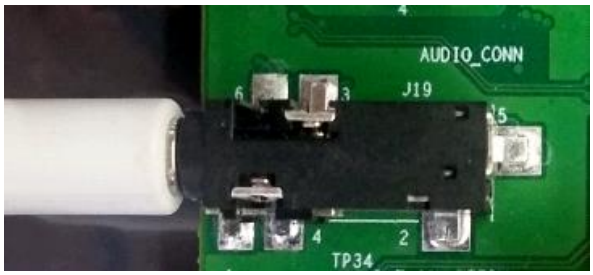

Figure 10 – Audio Headset Jack

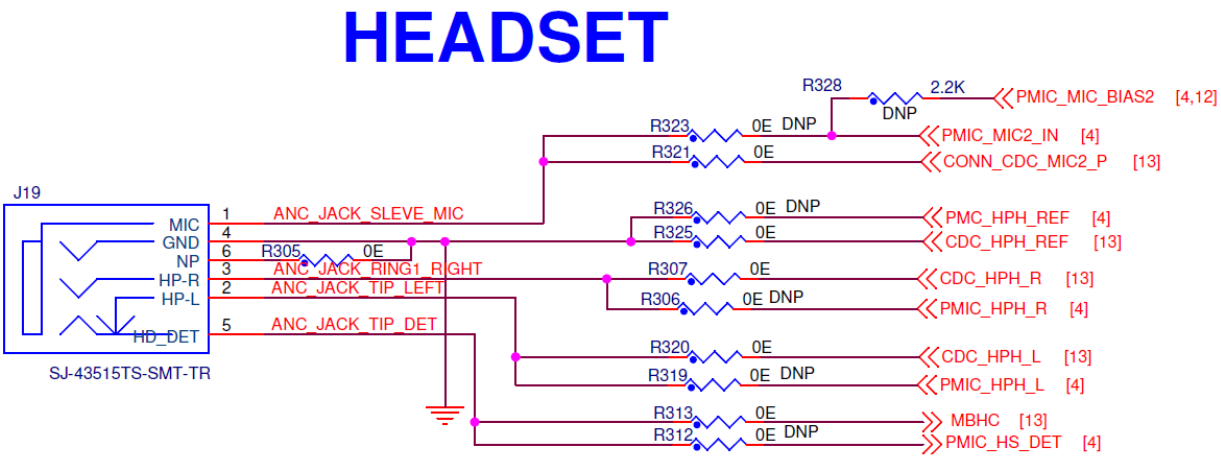

Figure 11 – Audio Headset Jack schematic

Below is the Pinout Specification of Headset Jack,

Pin Number	Net Name	Pin Function
J19.1	CONN_CDC_MIC2_P	MIC2 Input Positive
J19.2	CDC_HPH_L	Headphone Left Channel
J19.3	CDC_HPH_R	Headphone Right Channel
J19.4	CDC_HPH_REF	Headphone Reference Signal (Ground)
J19.5	MBHC	Headset Detect Signal
J19.6	NP	Connected to Ground

Table 5: Headset (J19) Pinout

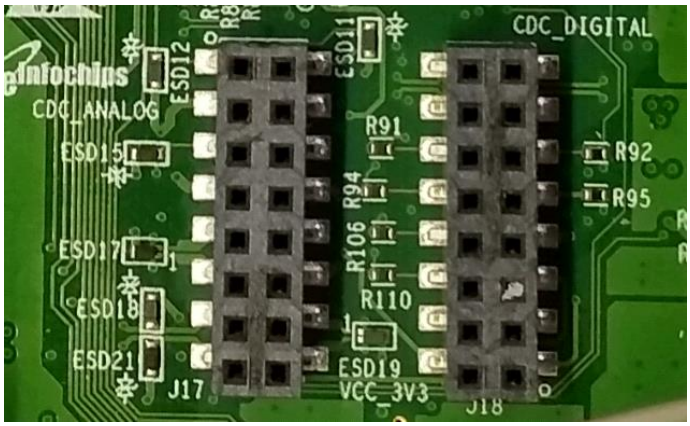

Figure 12 – Analog and Digital Codec Headers (J17 & J18)

Below is the Pinout Specification of J17,

Pin Number	Net Name	Pin Function
J17.1	CONN_CDC_MIC1_P	MIC1 Input Positive
J17.2	CONN_CDC_MIC5_P	MIC5 Input Positive
J17.3	GND	Ground
J17.4	GND	Ground
J17.5	CONN_CDC_MIC6_P	MIC6 Input Positive
J17.6	CONN_CDC_MIC3_P	MIC3 Input Positive
J17.7	GND	Ground
J17.8	GND	Ground
J17.9	CDC_SPEAKER1_OUT_P	Speaker1 Output Positive
J17.10	CONN_CDC_MIC4_P	MIC4 Input Positive
J17.11	CDC_SPEAKER1_OUT_M	Speaker1 Output Negative
J17.12	GND	Ground
J17.13	CDC_EAR_M	Earpiece Output Negative
J17.14	CDC_SPEAKER2_OUT_P	Speaker2 Output Positive
J17.15	CDC_EAR_P	Earpiece Output Positive

J17.16	CDC_SPEAKER2_OUT_M	Speaker2 Output Negative

Table 6: Audio Header (J17) Pinout

Below is the Pinout Specification of J18,

Pin Number	Net Name	Pin Function
J18.1	CDC_MIC_BIAS3	MIC Bias_3 Voltage
J18.2	CDC_MIC_BIAS4	MIC Bias_4 Voltage
J18.3	GND	Ground
J18.4	GND	Ground
J18.5	CDC_MIC_BIAS1	MIC Bias_1 Voltage
J18.6	CDC_DMIC_CLK1	Digital MIC_1 Clock
J18.7	GND	Ground
J18.8	CDC_DMIC_DATA1	Digital MIC_1 Data
J18.9	CDC_DMIC_CLK0	Digital MIC_0 Clock
J18.10	CDC_DMIC_CLK2	Digital MIC_2 Clock
J18.11	CDC_DMIC_DATA0	Digital MIC_0 Data
J18.12	CDC_DMIC_DATA2	Digital MIC_2 Data
J18.13	CDC_LINE_OUT2_P	Line Output_2 Positive
J18.14	CDC_LINE_OUT1_P	Line Output_1 Positive
J18.15	CDC_LINE_OUT2_M	Line Output_2 Negative
J18.16	CDC_LINE_OUT1_M	Line Output_1 Negative

Table 7: Audio Header (J18) Pinout

6.3.6 Sensors

ERAGON624 supports multiple sensors as below,

- Magnetometer, Accelerometer& Gyrometer, Pressure sensor and ALSP (Ambient Light and Proximity) sensor interfaced to APQ8053 through BLSP4_I2C Port
- Temperature sensor in interfaced to APQ8053 through BLSP6_I2C Port

6.3.7 Micro SD Card

The ERAGON624 carrier card could be connected with Micro SD card interface for external storage device (SD card). SD card is interfaced with APQ8053 (on SOM) through 4-bit SDC2 data signals along with SDC2 clock and SDC2 command signals. GPIO_133 of APQ8053 is used to detect SD card insertion and removal.

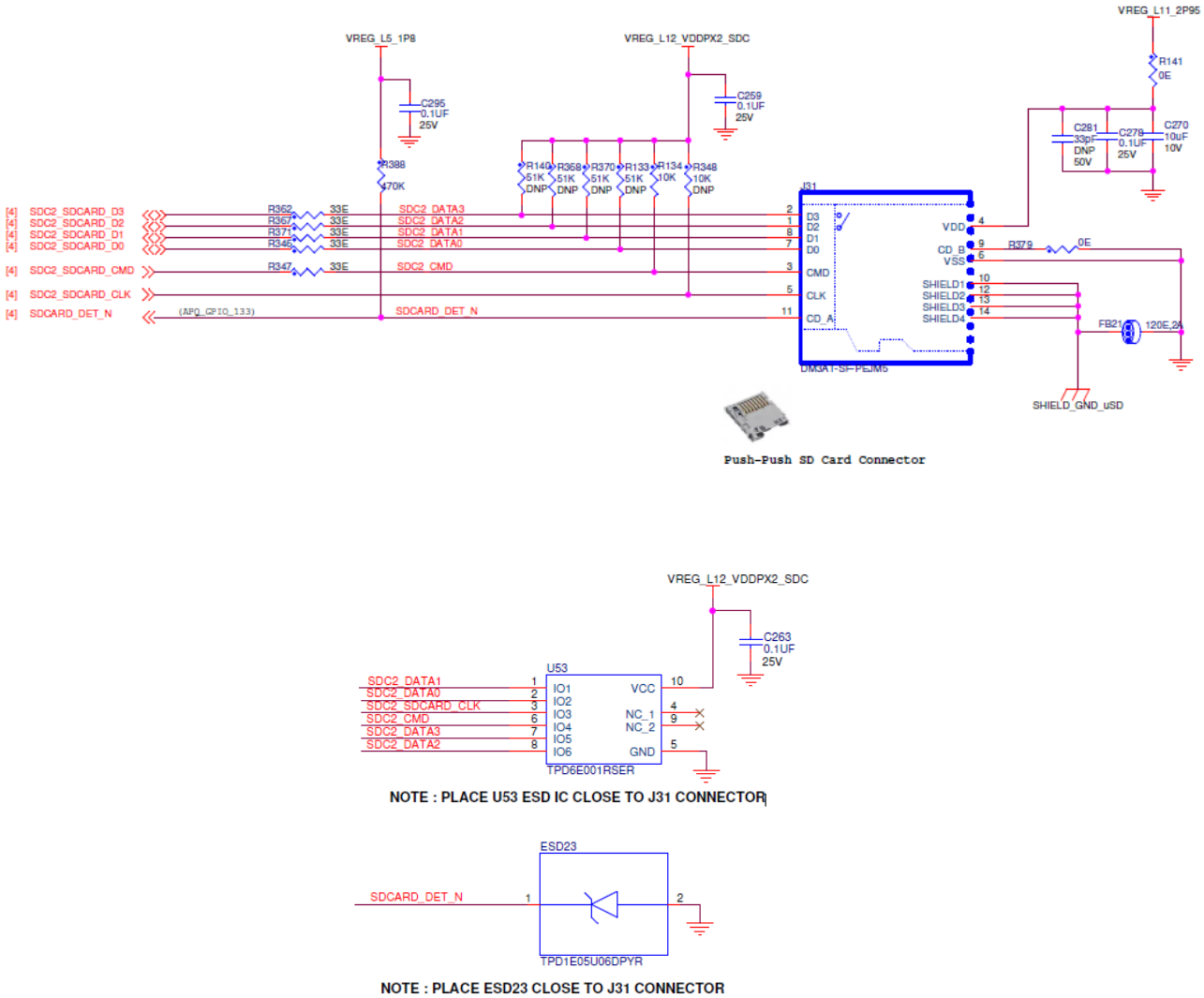

Figure 13 – Micro SD card connector schematic for carrier

6.3.8 DSI to HDMI

The Qualcomm APQ8053 Processor does not include a built-in HDMI interface. The ERAGON624 has the built-in MIPI-DSI 4 lanes interface, which is used, as a source for the HDMI output. A DSI to HDMI Bridge Board can be used to performs this task and it supports a resolution from 480p to 720p at 30Hz.

While the ADV7533 on the DSI to HDMI Bridge board supports automatic input video format timing detection (CEA-861E) and an I2C channel from the APQ8053 allows the user to configure the operation of this Bridge Board. The BLSP3_I2C interface is used from the SoC that connects to the Bridge board.

This **DSI to HDMI Bridge Board** (**eI PN# 17_00278_02**) supports audio as well. The ERAGON624 uses a single bit MI2S_1 interface from the APQ8053 chip which is mentioned in the below block. The ERAGON624 carrier should contains the 14 pin HDMI Audio Connector to connect to the Bridge Board.

A 3-wire (audio out only) I2S channel is routed directly from the APQ8053 SoC I2S interface pins to the DSI-HDMI bridge Board through HDMI Audio connector.

Figure 14 – DSI to HDMI Audio Connector J26

Pin specifications for J26 is mentioned below,

Pin Number	Net Name	Pin Function
J26.1	MI2S_1_D0	I2S Data 0 signal
J26.2	DSI2HDMI_INT_N	HDMI Interrupt Signal
J26.3	MI2S_1_WS	I2S Word Sync Clock l
J26.4	HDMI_HPD_N	HDMI Hot Plug Detect Signal
J26.5	MI2S_1_SCK	I2S Clock
J26.6	CEC_CLK/ PRI_MI2S_MCLK_A	9.6MHz System Clock frequency
J26.7	GND	Ground
J26.8	GND	Ground
J26.9	NC	Not Connected
J26.10	VCC_1V8	1.8V Supply
J26.11	NC	Not Connected
J26.12	VCC_5V0	5V Supply
J26.13	NC	Not Connected
J26.14	VCC_3V3	3.3V Supply

Table 8: HDMI Audio Connector (J26) Pinout

6.3.9 HDMI to CSI Audio interface

The Qualcomm APQ8053 Processor does not include a built-in HDMI interface. The ERAGON624 has the built-in MIPI-CSI 4 lanes interface, which is used, as HDMI input. A HDMI to CSI bridge chip TC358840 converts HDMI signals to MIPI CSI Signals. These CSI signals interfaced with APQ8053 through MIPI CSI connectors mentioned in CSI section.

This Bridge Board supports audio as well. The ERAGON624 uses a MI2S_1 interface from the APQ8053 chip which is mentioned in the below block. The ERAGON624 contains the 16 pin HDMI Audio Connector (J27) on the board. A 6-wire (audio input) I2S channel is routed directly from the APQ8053 SoC I2S interface pins to the HDMI to CSI Bridge Board through HDMI Audio connector.

Figure 15 – HDMI to CSI Audio Connector J27

Pin specifications for J27 is mentioned below,

Pin Number	Net Name	Pin Function
J27.1	VCC_3V3	3.3V Supply
J27.2	VCC_3V3	3.3V Supply
J27.3	VREG_L2_1P1	1.2V Supply
J27.4	VCC_1V8	1.8V Supply
J27.5	HDMI_I2C_SDA	HDMI I2C Data
J27.6	HDMI_I2C_SCL	HDMI I2C Clock
J27.7	MI2S_1_SCK	I2S Clock
J27.8	MI2S_1_WS	I2S Word Sync Clock
J27.9	MI2S_1_D3	I2S Data 3 Signal
J27.10	MI2S_1_D2	I2S Data 2 Signal
J27.11	MI2S_1_D1	I2S Data 1 Signal
J27.12	MI2S_1_D0	I2S Data 0 Signal
J27.13	HDMI_INT_GPIO	HDMI Interrupt
J27.14	HDMI_RST_N	HDMI Reset
J27.15	GND	Ground
J27.16	GND	Ground

Table 9: HDMI Audio Connector (J27) Pinout

6.3.10 WiFi + BT chip antenna

As mentioned in ERAGON624 SOM blocks, Wi-Fi + BT RF signal routed from SOM to Carrier card through U.FL-to-U.FL cable connected from connector J8 at SOM and connector J4 at Carrier card. After that, it is interfaced to Fractus chip antenna **FR05-S1-NO-1-004 (ref ANTENNA1)** to radiate. During the design of carrier Board, customer needs to use the same chip Antenna on application Board.

For Placement & routing of the Antenna on Carrier Board, contact eInfochips to get the detailed information.

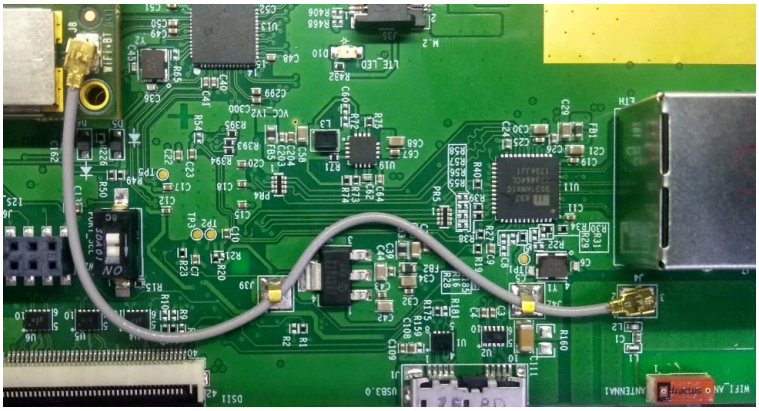

Figure 16 – Routing of UFL cable from SOM to Carrier

6.3.11 GPS chip antenna

GPS receiver signal received from GPS chip antenna 1575AT54A0010E mounted on Carrier card (ref ANT1) after passing through SAW filter and LNA is routed to SOM module through U.FL-to-U.FL cable connected from connector J21 at Carrier Card to connector J1 at SOM module.

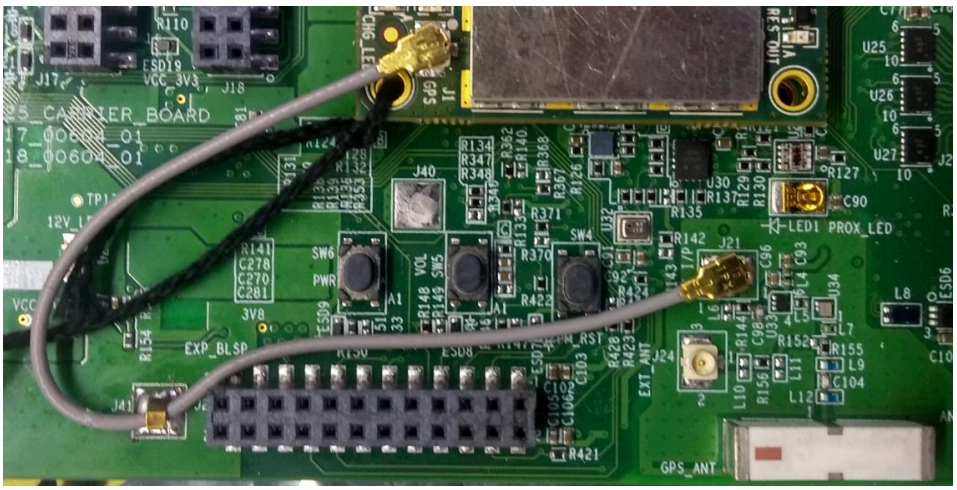

Figure 17 – Routing of UFL cable from SOM to Carrier

6.3.12 M.2 (4G LTE) connector

ERAGON624 SOM to plug 4G LTE modem on Carrier card by placing 75-pin M.2 connector on Carrier Board Design. This 4G module is interfaced with second downstream port of USB Hub (it can be used to expand USB ports) through which it is connected to APQ8053 processor, MI2S_2 interface, BLSP4 UART interface and few other GPIOs of APQ8053 and Dual SIM card connectors (SIM1-J38, SIM2-J36).

For more details, contact eInfochips.

Figure 18 – M.2 connector (J35)

Figure 19 – SIM card connectors (J38 & J36)

Pinout specifications of J35 are below,

Pin Number	Net Name	Pin Function
J35.1	CONFIG_3	DNP Pull up (1.8V) & Pull down (GND) Option
J35.2	VCC_3V7_LTE	3.7V Supply For LTE Modem
J35.3	GND	Ground
J35.4	VCC_3V7_LTE	3.7V Supply For LTE Modem
J35.5	GND	Ground
J35.6	LTE_MODEM_POWER	LTE Modem Power Control Signal
J35.7	USBDN_DP2	USB High Speed Data Positive Signal
J35.8	LTE_MODEM_W_DISABLE#1	LTE RF Radio Disable control GPIO
J35.9	USBDN_DM2	USB High Speed Data Negative Signal
J35.10	LTE_MODEM_LED#1	LED Driver Control GPIO
J35.11	GND	Ground
J35.12	NC	Not Connected
J35.13	NC	Not Connected
J35.14	NC	Not Connected
J35.15	NC	Not Connected
J35.16	NC	Not Connected
J35.17	NC	Not Connected
J35.18	NC	Not Connected
J35.19	NC	Not Connected
J35.20	MI2S_2_SCK	I2S_2 Bit Clock

J35.21	CONFIG_0	DNP Pull Up (1.8V) Option
J35.22	MI2S_2_D0	I2S_2 Data 0
J35.23	LTE_WAKE_HOST#	Wake Host Signal
J35.24	MI2S_2_D1	I2S_2 Data 1
J35.25	LTE_MODEM_DPR	Dynamic Power Control
J35.26	LTE_MODEM_W_DISABLE#2	LTE GNSS Radio Disable control GPIO
J35.27	GND	Ground
J35.28	MI2S_2_WS	I2S_2 Word Sync Clock
J35.29	USB_SSRXM_DN2	USB Super Speed Receive Data Negative
J35.30	SIM1_RST	SIM Card _1 Reset Signal

Pin Number	Net Name	Pin Function
J35.31	USB_SSRXP_DN2	USB Super Speed Receive Data Positive
J35.32	SIM1_CLK	SIM Card _1 Clock
J35.33	GND	Ground
J35.34	SIM1_DATA	SIM Card _1 Data Signal
J35.35	USB_SSTXM_DN2	USB Super Speed Transmit Data Negative
J35.36	SIM1_PWR	SIM Card _1 Power Supply
J35.37	USB_SSTXP_DN2	USB Super Speed Transmit Data Positive
J35.38	NC	Not Connected
J35.39	GND	Ground
J35.40	SIM2_DETECT	SIM Card _2 Detect Signal
J35.41	NC	Not Connected
J35.42	SIM2_DATA	SIM Card _2 Data Signal
J35.43	NC	Not Connected
J35.44	SIM2_CLK	SIM Card _2 Clock
J35.45	GND	Ground
J35.46	SIM2_RST	SIM Card _2 Reset Signal
J35.47	NC	Not Connected
J35.48	SIM2_PWR	SIM Card _2 Power Supply
J35.49	NC	Not Connected
J35.50	NC	Not Connected
J35.51	GND	Ground
J35.52	NC	Not Connected
J35.53	NC	Not Connected
J35.54	NC	Not Connected
J35.55	NC	Not Connected
J35.56	NC	Not Connected
J35.57	GND	Ground
J35.58	NC	Not Connected
J35.59	TP26	Test Point
J35.60	BLSP1_SPI_MISO	GPIO for Coexistence
J35.61	TP27	Test Point
J35.62	BLSP4_UART_TX	Coexistence UART Transmit

J35.63	TP28	Test Point
J35.64	BLSP4_UART_RX	Coexistence UART Receive
J35.65	TP29	Test Point
J35.66	SIM1_DETECT	SIM Card _1 Detect Signal
J35.67	LTE_MODEM_RST#	Modem Reset Signal
J35.68	NC	Not Connected
J35.69	CONFIG_1	DNP Pull Up (1.8V) Option
J35.70	VCC_3V7_LTE_RF	3.7V LTE RF Power Supply

Pin Number	Net Name	Pin Function
J35.71	GND	Ground
J35.72	VCC_3V7_LTE_RF	3.7V LTE RF Power Supply
J35.73	GND	Ground
J35.74	VCC_3V7_LTE_RF	3.7V LTE RF Power Supply
J35.75	CONFIG_2	DNP Pull Up (1.8V) Option

Table 10: M.2 connector (J35) Pinout

SIM Card_1 Connector Pin specifications are as follows,

Pin Number	Net Name	Pin Function
J38.1	SIM1_PWR_SOCKET	SIM1 Power Supply
J38.2	SIM1_RST_ESD	SIM1 Reset Signal
J38.3	SIM1_CLK_ESD	SIM1 Clock
J38.4	GND	Ground
J38.5	VPP	Vpp Output
J38.6	SIM1_DATA_ESD	SIM1 Data
J38.7	SIM1_DETECT	SIM1 Card Detect
J38.8 to J38.17	SIM_SHEILD_GND	Shield Ground

Table 11: SIM CARD_1 connector (J38) Pinout

SIM Card_2 Connector Pin specifications are as follows,

Pin Number	Net Name	Pin Function
J36.1	SIM2_PWR_SOCKET	SIM2 Power Supply
J36.2	SIM2_RST_ESD	SIM2 Reset Signal
J36.3	SIM2_CLK_ESD	SIM2 Clock
J36.4	GND	Ground
J36.5	VPP	Vpp Output
J36.6	SIM2_DATA_ESD	SIM2 Data
J36.7	SIM2_DETECT	SIM2 Card Detect
J36.8 to J36.17	SIM_SHEILD_GND	Shield Ground

Table 12: SIM CARD_2 connector (J36) Pinout

6.3.13 RTC

For Time and Date update, ERAGON624 has a support to connect external rechargeable Coin Cell battery on connector J8 at Carrier card.

Connect +Ve terminal of battery to J8.1 pin and GND to J8.2 pin.

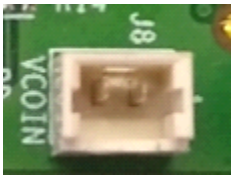

Figure 20 – RTC connector (J8)

6.3.14 Debug Port

ERAGON624 support a debug Port to capture the system logs. Carrier card has on board UART to USB converter chip FT230XQ-R (U55). It converts BLSP2 UART signals routed from SOM to carrier through B2B connectors to USB high-speed signals.
Therefore, to capture the logs, user only need to connect Micro USB cable to connector J22 on carrier card.

Figure 21 – Debug Port connection (J22)

Pinout specification of J22 mentioned below,

Pin Number	Net Name	Pin Function
J22.1	VBUS_5V	USB 5V Supply
J22.2	USB_DEBUG_DM	USB Data Negative
J22.3	USB_DEBUG_DP	USB Data Positive
J22.4	NC	Not Connected
J22.5	GND	Ground

Table 13: Debug Port Connector (J22) Pinout

7 Electrical Specification

7.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
VBATT+	Main Battery Input Supply Voltage	-0.3	6.0	V
VCOIN	RTC Input Supply Voltage	-0.5	3.5	V
USB_VBUS	USB VBUS Input Supply Voltage	-0.3	28	V

Table 14 : Absolute Maximum Ratings

7.2 Operating Conditions

Parameter		Min	Typ	Max	Unit
VBATT+	Main Battery Input Supply Voltage	2.5	3.6	4.75	V
VCOIN	RTC Input Supply Voltage	2.0	3.0	3.25	V
USB_VBUS	USB VBUS Input Supply Voltage	3.7	5.0	10	V

Table 15 : Operating Conditions

8 Mechanical Specification

8.1 SOM Board Dimensions

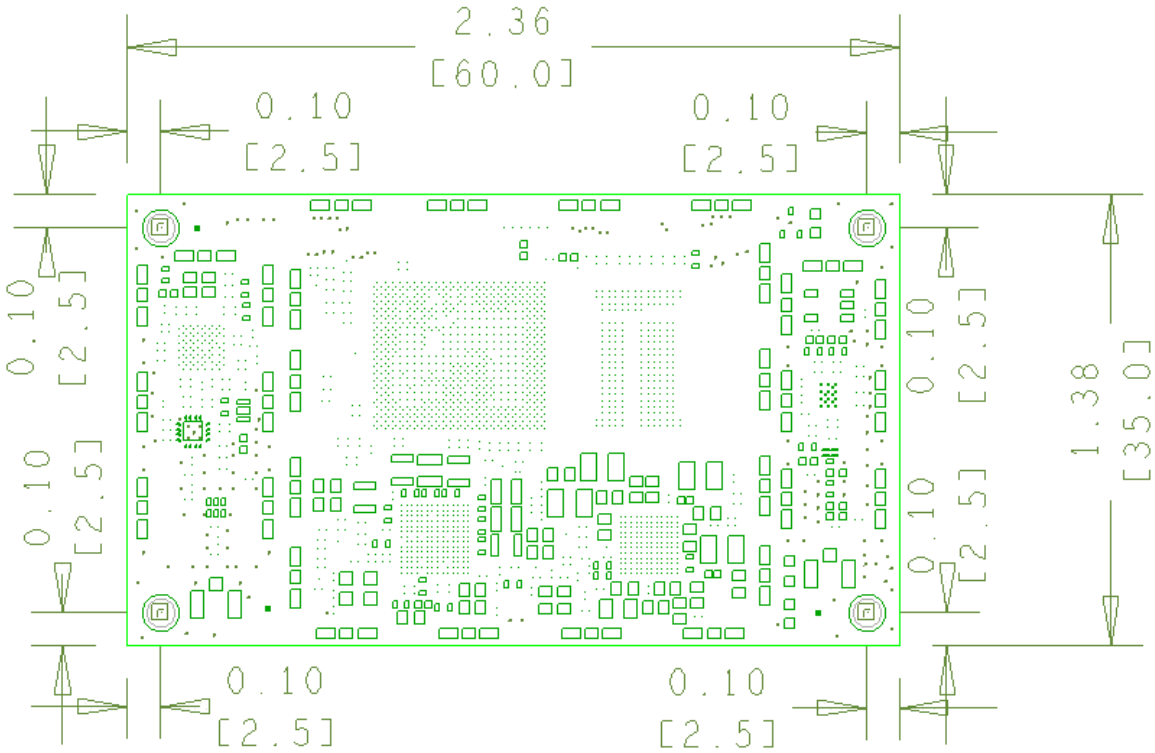

Figure 22 – SOM Module Dimension

8.2 Shields Dimensions

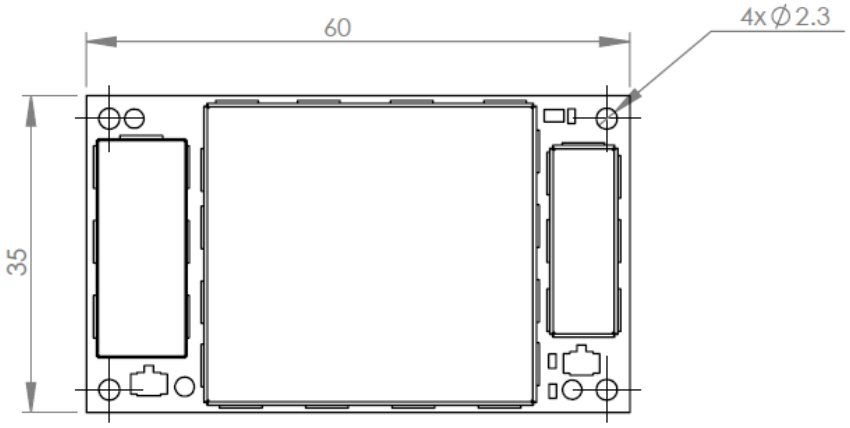

Figure 23 – SOM Module TOP side Shields

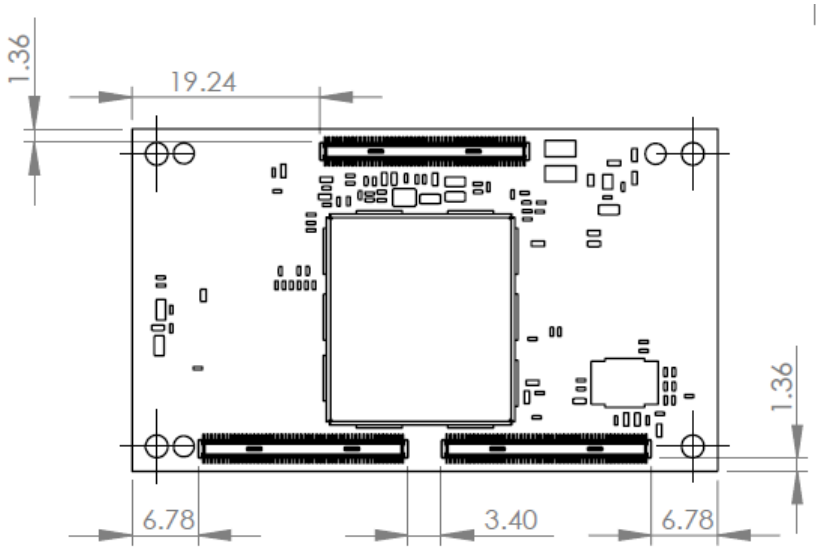

Figure 24 – SOM Module BOT side Shield

9 Special Care when using ERAGON624 SOM Board

9.1 Development Device Notice

This device contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is intended for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

9.2 Anti-Static Handling Procedure

This device has exposed PCB and chips. Accordingly, proper anti-static precautions should be employed when handling the kit, including:

- Use a grounded anti-static mat
- Use a grounded wrist or foot strap

10 About eInfochips

eInfochips is a partner of choice for Fortune 500 companies for product innovation and hi-tech engineering consulting. Since 1994, eInfochips has provided solutions to key verticals like Aerospace & Defense, Consumer Electronics, Energy & Utilities, Healthcare, Home, Office, and Industrial Automation, Media & Broadcast, Medical Devices, Retail & e-Commerce, Security & Surveillance, Semiconductor, Software/ISV and Storage & Compute.

Covering every aspect of the product lifecycle, eInfochips draws from an experience of building 500+ products that have over 10 Million units deployed – to provide solutions on Product Design and Development, QA and Certifications, Reengineering, Sustenance and Volume Production. Being an innovation driven company, 5% of our revenues are earmarked for building reusable IPs that will accelerate product design cycles and reduce product risks.

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Technical Assistance:	eInfochips Qualcomm portal (www.supportcenter.einfochips.com)
Technical Support:	QCSupport@einfochips.com
Sales/Marketing Support:	marketing@einfochips.com

FCC Warning

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help.

*RF warning for Mobile device:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IC Warning

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

*RF warning for Mobile device:
This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.
Cet appareil est conforme aux CNR exemptes de licence d'Industrie Canada . Son fonctionnement est soumis aux deux conditions suivantes :
(1) Ce dispositif ne peut causer d'interférences ; et
(2) Ce dispositif doit accepter toute interférence , y compris les interférences qui peuvent causer un mauvais fonctionnement de l'appareil.

la distance entre l'utilisateur et le dispositif ne doit pas être inférieure à 20 cm