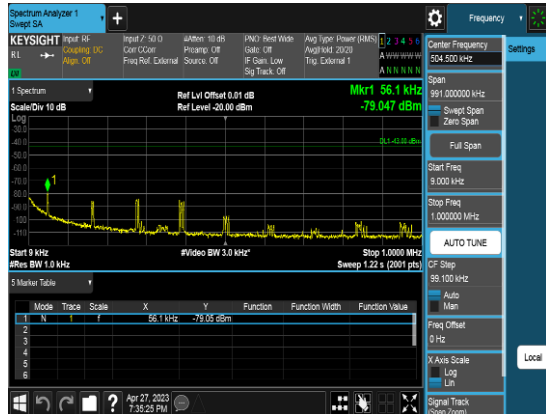


Port1_20M_3690MHz_TM3.1_CHH_CSE0a



Port1_20M_3690MHz_TM3.1_CHH_CSE0b



Port1_20M_3690MHz_TM3.1_CHH_CSE1



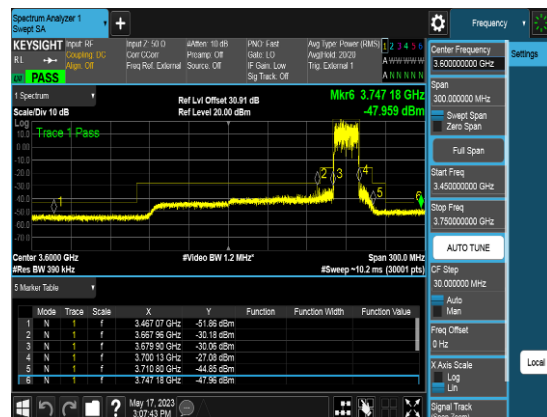
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Port1_20M_3690MHz_TM3.1_CHH_CSE3



Port1_20M_3690MHz_TM3.1_CHH_CSEpart96





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Port1_5M_3552.5MHz_TM3.1_CHL_CSE0a



Port1_5M_3552.5MHz_TM3.1_CHL_CSE0b



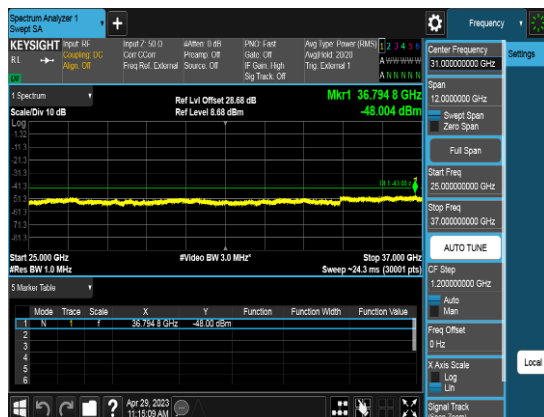
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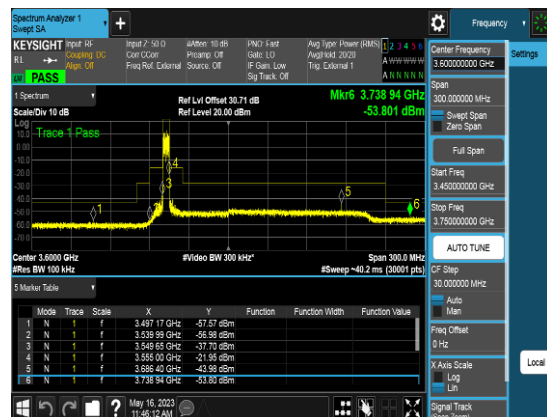
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Port1_5M_3552.5MHz_TM3.1_CHL_CSE3



Port1_5M_3552.5MHz_TM3.1_CHL_CSEpart96



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Port1_5M_3625MHz_TM3.1_CHM_CSE0a



Port1_5M_3625MHz_TM3.1_CHM_CSE0b



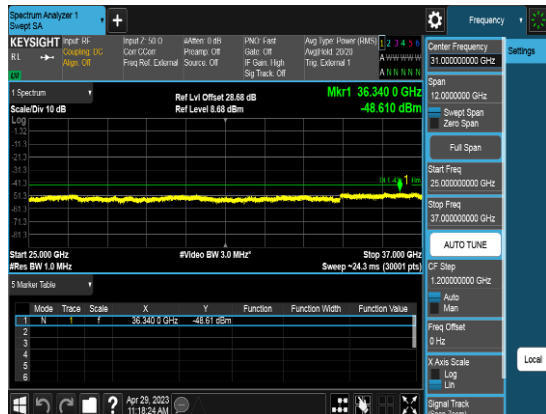
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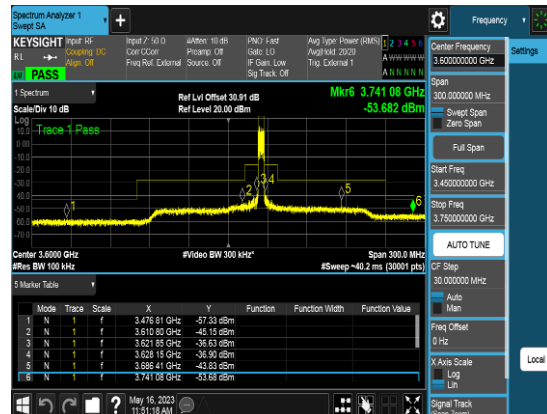
Port1_5M_3625MHz_TM3.1_CHM_CSE2



Port1_5M_3625MHz_TM3.1_CHM_CSE3



Port1_5M_3625MHz_TM3.1_CHM_CSEpart96



Port1_5M_3697.5MHz_TM3.1_CHH_CSE0a



Port1_5M_3697.5MHz_TM3.1_CHH_CSE0b



Port1_5M_3697.5MHz_TM3.1_CHH_CSE1



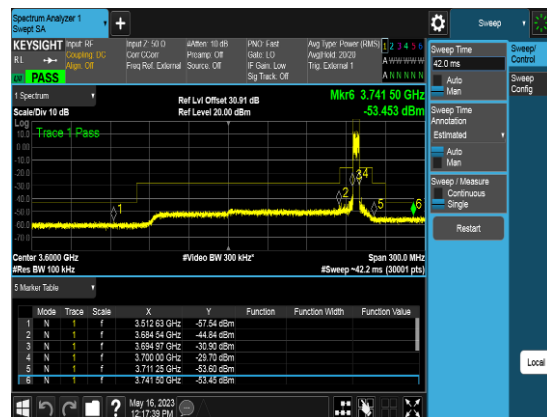
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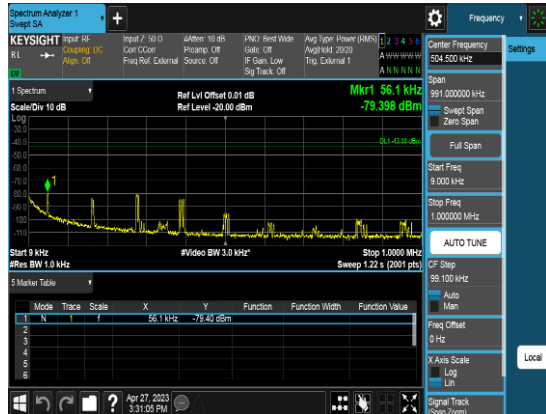
Port1_5M_3697.5MHz_TM3.1_CHH_CSE3



Port1_5M_3697.5MHz_TM3.1_CHH_CSEpart96



Port2_10M_3555MHz_TM3.1_CHL_CSE0a



Port2_10M_3555MHz_TM3.1_CHL_CSE0b



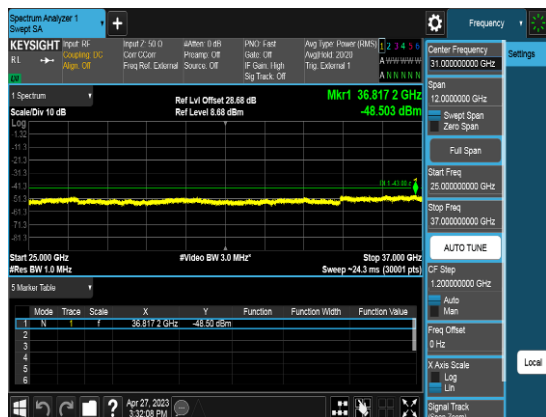
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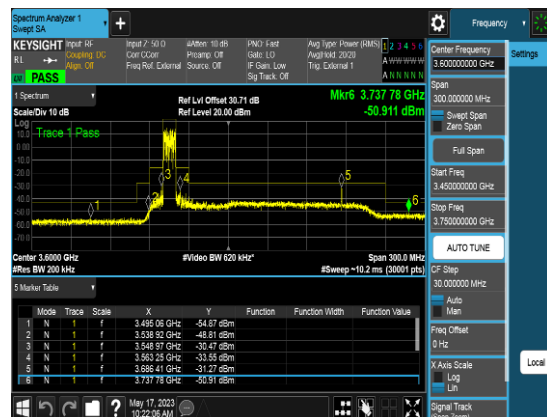
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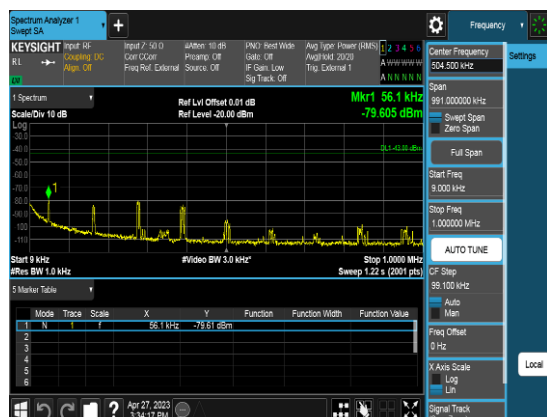
Port2_10M_3555MHz_TM3.1_CHL_CSE3



Port2_10M_3555MHz_TM3.1_CHL_CSEpart96



Port2 10M 3625MHz TM3.1 CHM CSE0a



Port2 10M 3625MHz TM3.1 CHM CSE0b



Port2 10M 3625MHz TM3.1 CHM CSE1



Port2 10M 3625MHz TM3.1 CHM CSE2



Port2 10M 3625MHz TM3.1 CHM CSE3



Port2 10M 3625MHz TM3.1 CHM CSEpart96



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Port2 10M 3695MHz TM3.1 CHH CSE0a



Port2 10M 3695MHz TM3.1 CHH CSE0b



Port2 10M 3695MHz TM3.1 CHH CSE1



Port2 10M 3695MHz TM3.1 CHH CSE2



Port2 10M 3695MHz TM3.1 CHH CSE3



Port2 10M 3695MHz TM3.1 CHH CSEpart96



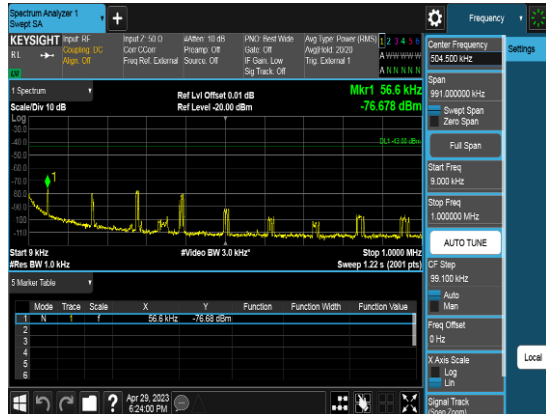
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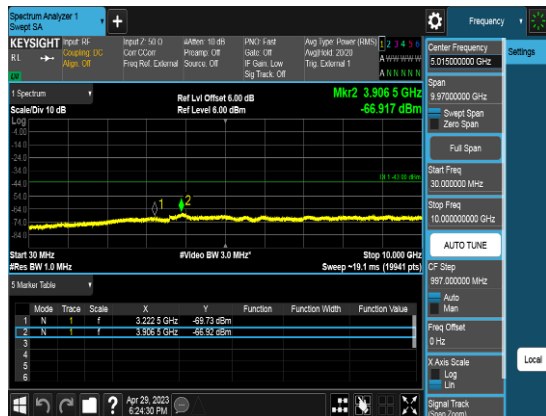
Port2_15M_3557.5MHz_TM3.1_CHL_CSE0a



Port2_15M_3557.5MHz_TM3.1_CHL_CSE0b



Port2_15M_3557.5MHz_TM3.1_CHL_CSE1



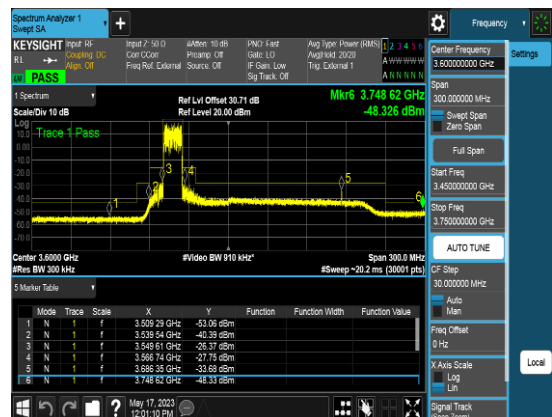
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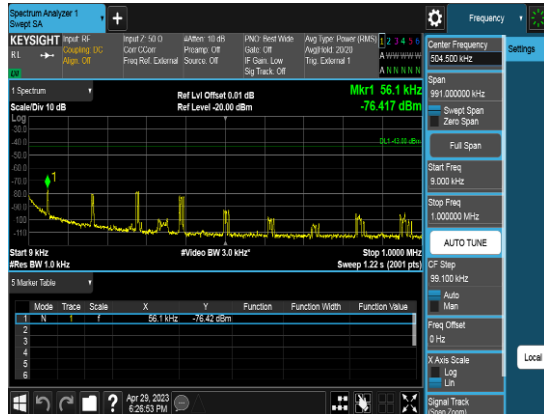
Port2_15M_3557.5MHz_TM3.1_CHL_CSE3



Port2_15M_3557.5MHz_TM3.1_CHL_CSEpart96



Port2_15M_3625MHz_TM3.1_CHM_CSE0a



Port2_15M_3625MHz_TM3.1_CHM_CSE0b



Port2_15M_3625MHz_TM3.1_CHM_CSE1



Port2_15M_3625MHz_TM3.1_CHM_CSE2



Port2_15M_3625MHz_TM3.1_CHM_CSE3



Port2_15M_3625MHz_TM3.1_CHM_CSEpart96



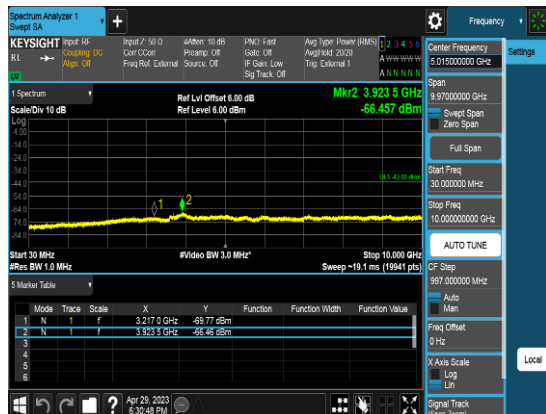
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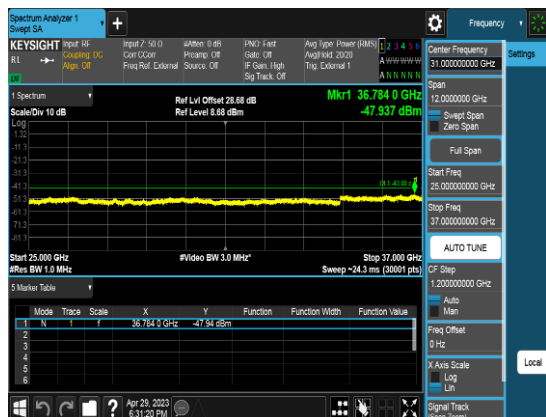
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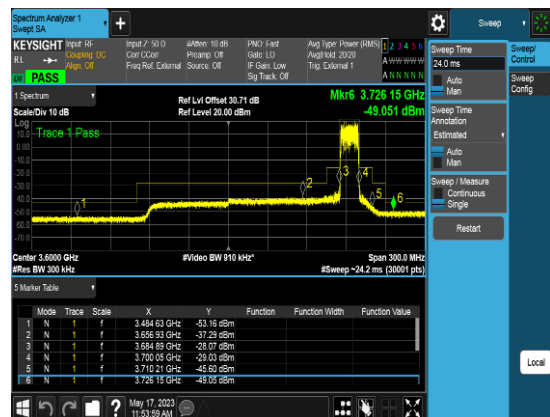
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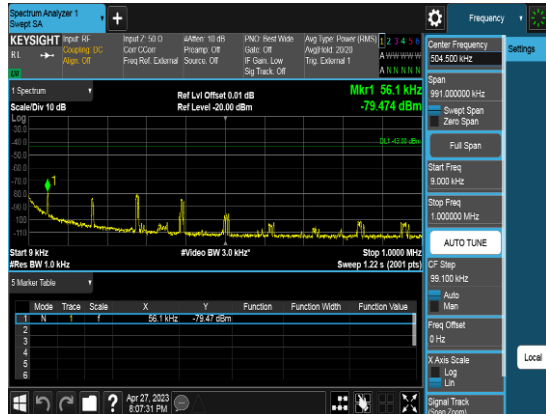
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Port2_15M_3692.5MHz_TM3.1_CHH_CSEpart96



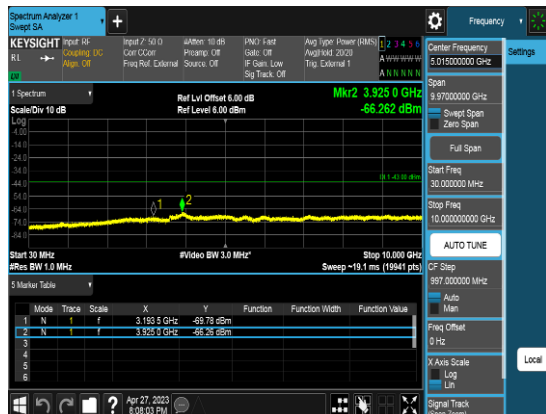
Port2_20M_3560MHz_TM3.1_CHL_CSE0a



Port2_20M_3560MHz_TM3.1_CHL_CSE0b



Port2_20M_3560MHz_TM3.1_CHL_CSE1



Port2_20M_3560MHz_TM3.1_CHL_CSE2



Port2_20M_3560MHz_TM3.1_CHL_CSE3



Port2_20M_3560MHz_TM3.1_CHL_CSEpart96

