

SCC_20M_3630MHz_QPSK_1RB_CSE0a



SCC_20M_3630MHz_QPSK_1RB_CSE0b



SCC_20M_3630MHz_QPSK_1RB_CSE1



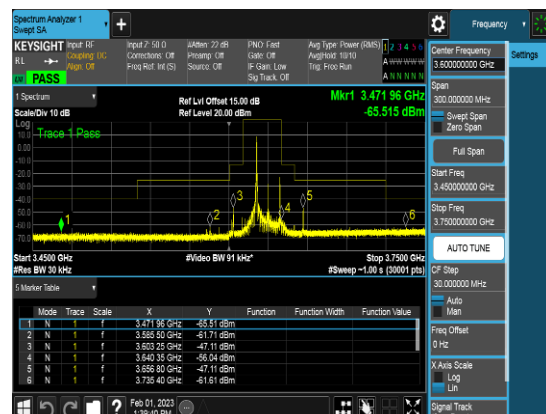
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SCC_20M_3630MHz_QPSK_1RB_CSE3



SCC_20M_3630MHz_QPSK_1RB_CSEpart96



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SCC_20M_3630MHz_QPSK_FULLRB_CSE0a



SCC_20M_3630MHz_QPSK_FULLRB_CSE0b



SCC_20M_3630MHz_QPSK_FULLRB_CSE1



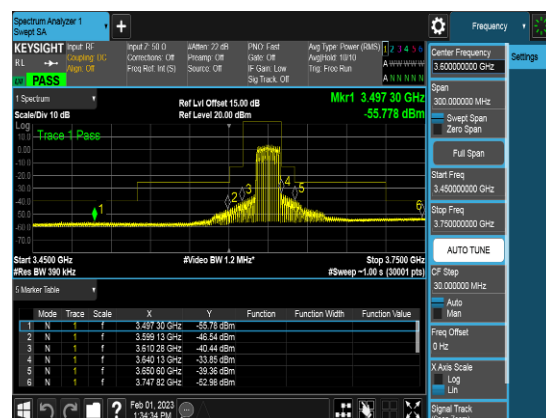
SCC_20M_3630MHz_QPSK_FULLRB_CSE2



SCC_20M_3630MHz_QPSK_FULLRB_CSE3



SCC_20M_3630MHz_QPSK_FULLRB_CSEpart9
6



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SCC_20M_3690MHz_Q16_1RB_CSE0a



SCC_20M_3690MHz_Q16_1RB_CSE0b



SCC_20M_3690MHz_Q16_1RB_CSE1



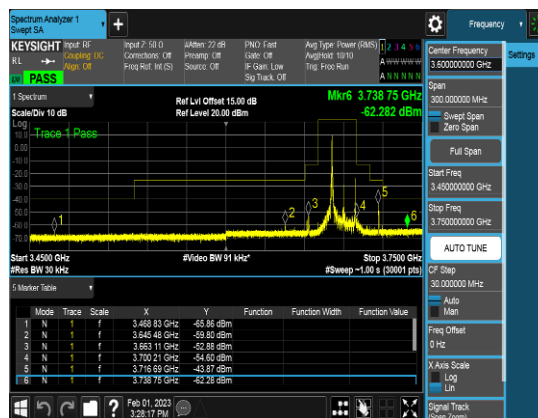
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SCC_20M_3690MHz_Q16_1RB_CSE3



SCC_20M_3690MHz_Q16_1RB_CSEpart96



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SCC_20M_3690MHz_Q16_FULLLRB_CSE0a



SCC_20M_3690MHz_Q16_FULLLRB_CSE0b



SCC_20M_3690MHz_Q16_FULLLRB_CSE1



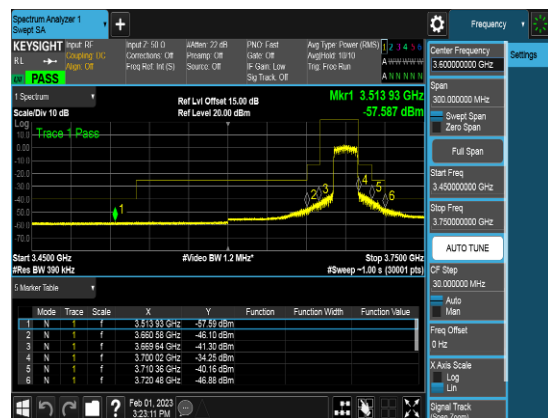
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SCC_20M_3690MHz_Q16_FULLLRB_CSE3



SCC_20M_3690MHz_Q16_FULLLRB_CSEpart96



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SCC_20M_3690MHz_Q64_1RB_CSE1



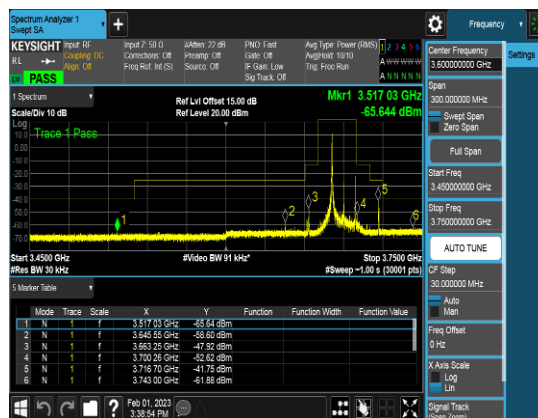
SCC_20M_3690MHz_Q64_1RB_CSE2



SCC_20M_3690MHz_Q64_1RB_CSE3



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SCC_20M_3690MHz_Q64_FULLLRB_CSE1



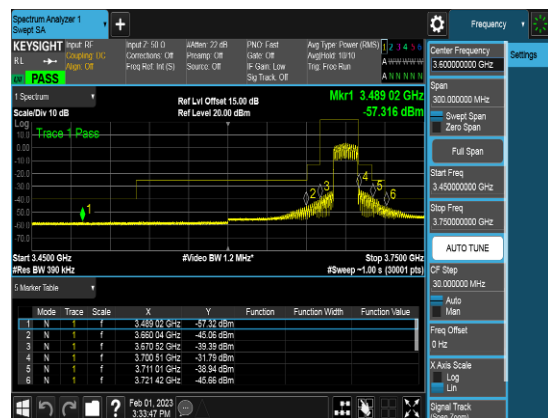
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SCC_20M_3690MHz_Q64_FULLLRB_CSE3



SCC_20M_3690MHz_Q64_FULLLRB_CSEpart96



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SCC_20M_3690MHz_QPSK_1RB_CSE1



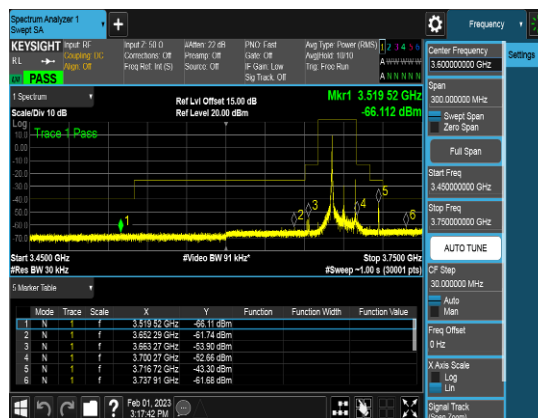
SCC_20M_3690MHz_QPSK_1RB_CSE2



SCC_20M_3690MHz_QPSK_1RB_CSE3



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SCC_20M_3690MHz_QPSK_FULLLRB_CSE0b



SCC_20M_3690MHz_QPSK_FULLLRB_CSE1



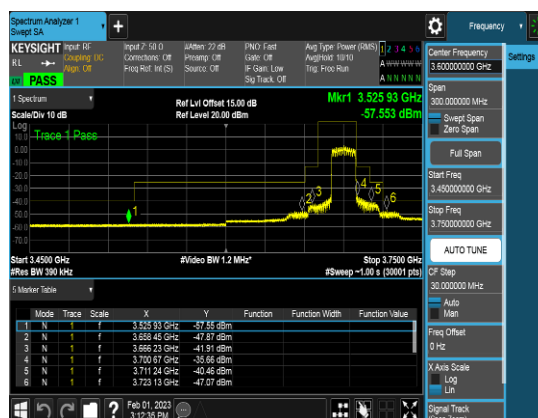
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SCC_20M_3690MHz_QPSK_FULLLRB_CSE3



SCC_20M_3690MHz_QPSK_FULLLRB_CSEpart9
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PCC 20MHz + SCC 10MHz

PCC_20M_3560MHz_Q16_1RB_CSE0a



PCC_20M_3560MHz_Q16_1RB_CSE0b



PCC_20M_3560MHz_Q16_1RB_CSE1



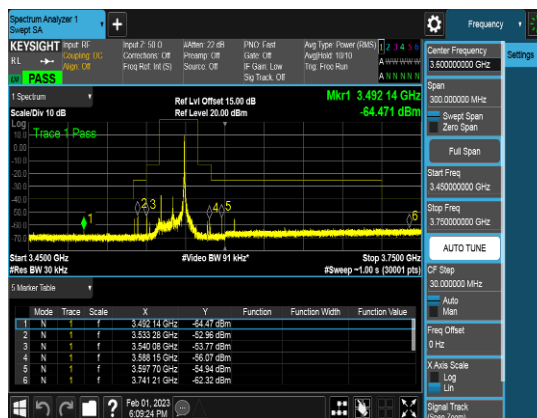
PCC_20M_3560MHz_Q16_1RB_CSE2



PCC_20M_3560MHz_Q16_1RB_CSE3



PCC_20M_3560MHz_Q16_1RB_CSEpart96



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PCC_20M_3560MHz_Q16_FULLLRB_CSE1



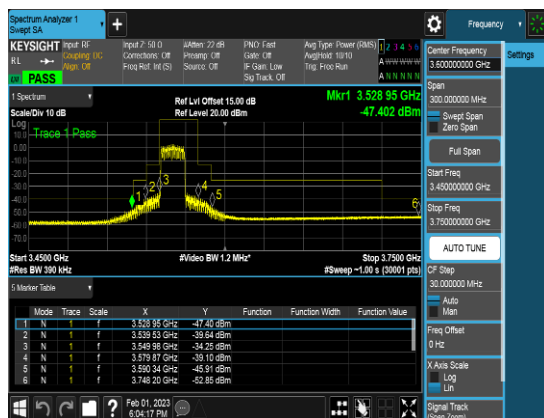
PCC_20M_3560MHz_Q16_FULLLRB_CSE2



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PCC_20M_3560MHz_Q64_1RB_CSE1



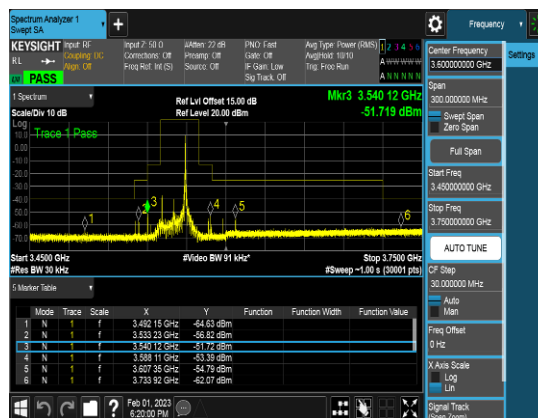
PCC_20M_3560MHz_Q64_1RB_CSE2



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