

Content Indexing

- 01.Index
- 02.Modify note
- 03.Block Diagram
- 04.Power Tree
- 05.System Power
- 06.RK3288 USB/HSIC Controler
- 07.USB HOST HUB/OTG Port
- 08.RK3288 RAM Controler
- 09.LPDDR3(178P)-2X32bit
- 10.Nand FLASH/eMMC/TF Card
- 11.RK3288 GPIO/POWER/Debug
- 12.HDMI OUT
- 13.eDP OUT/TP
- 14.RGB-EDP/LVDS OUT
- 15.RK3288 LCDC/I2S Controler
- 16.Audio/ALC5651/PA
- 17.RK3288 EthernetMAC Controler
- 18.10/100M-PHY/USB
- 19.RK3288 SDIO0 Controler
- 20.WIFI/BT
- 21.RK3288 Camera Interface
- 22.RS232
- 23.3G-miniPCIE

24.Customer Display 25.Printer/Cashbox

项目名称: CTD-RK3288台式机安卓主板

设计人员: _____

审核人员: _____

日期: _____

6 LAYERS PCB STACK

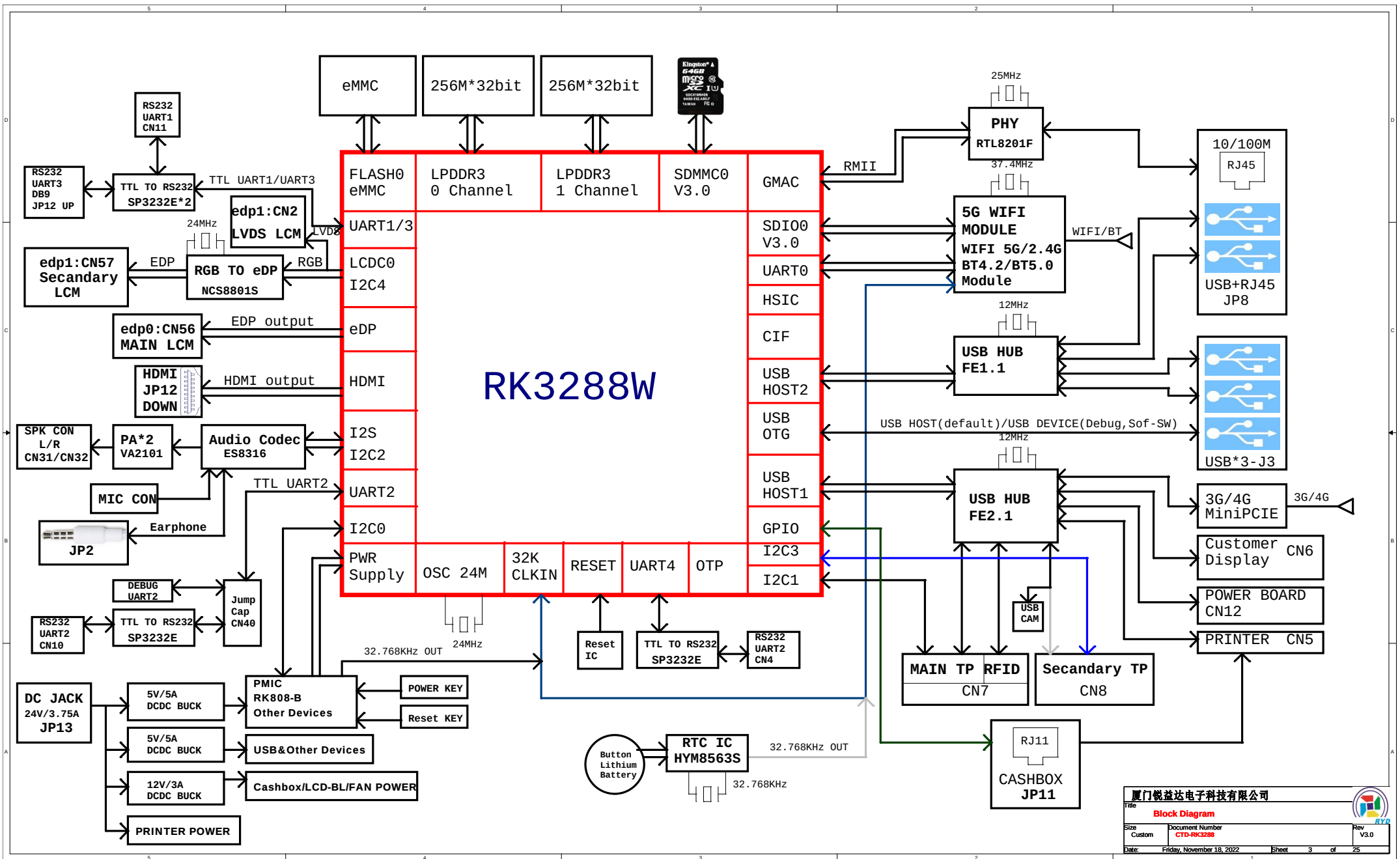
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POWER	FR4,thickness:8mil,Dielectric Constant:4.3	Cu,thickness:1.5mil, 1oz
FR4,thickness:adjust thickness according to the thickness of board ,Dielectric Constant:4.3		
Signal2	FR4,thickness:8mil,Dielectric Constant:4.3	Cu,thickness:1.5mil, 1oz
GND2	FR4,thickness:3.8mil,Dielectric Constant:4.3	Cu,thickness:1.5mil, 1oz
BOTTOM(Signal3)		Cu,thickness:0.7mil,Plating to 1oz

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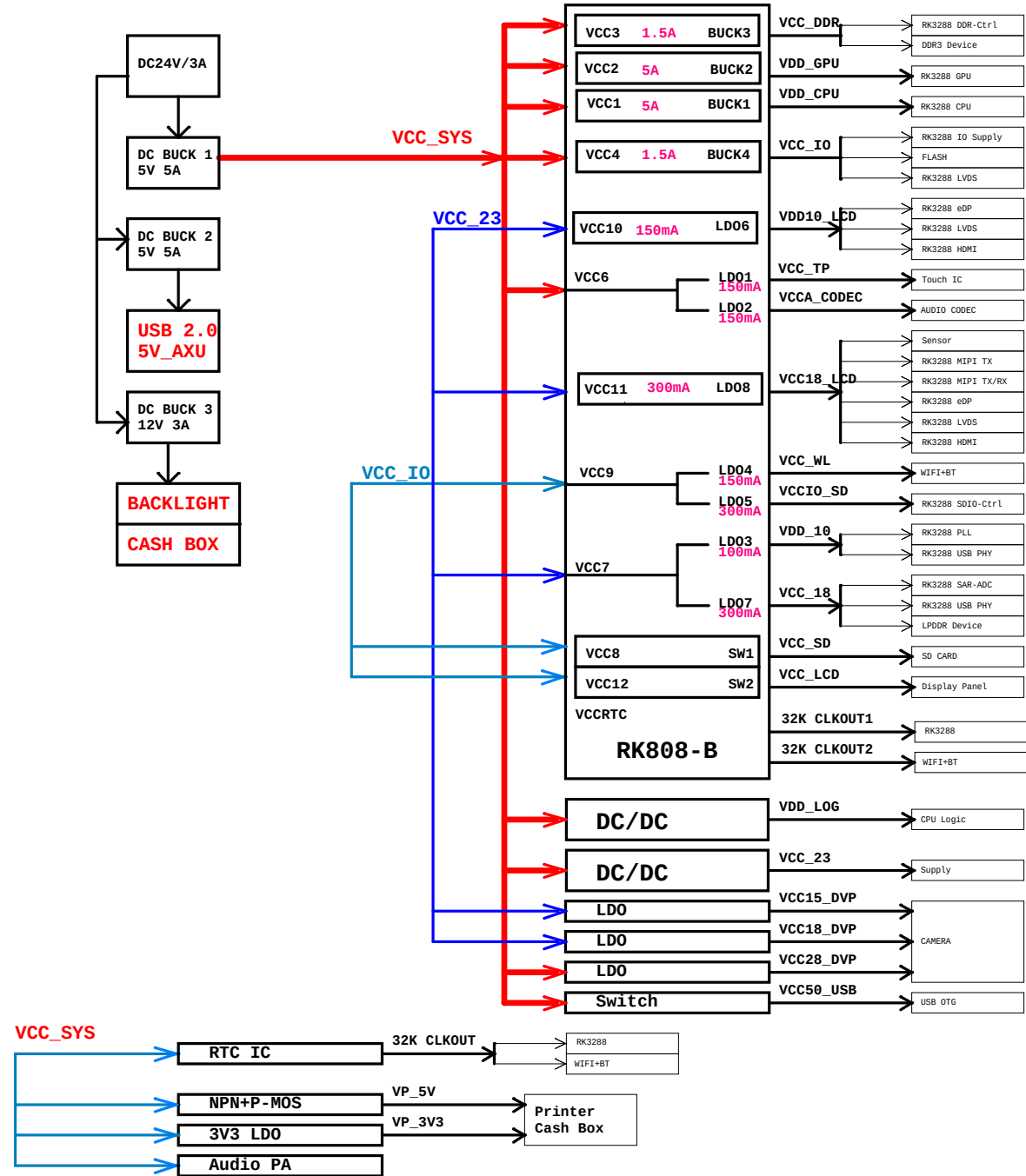
Title		
Index		
Size A4	Document Number CTD-RK3288	Rev V3.0
Date: Friday, November 18, 2022	Sheet 1	of 25



Version	Date	Author	Change Note	Approved
8843_V1.0	2019.07.18	LIN LINGMIN	First Editor	
CTD-RK3288_V1.0	2019.12.02	LIN LINGMIN	1、阻抗说明HDMI层贴图错误； 2、HDMI信号接口共模电阻补贴； 3、VCC_DDR更改为1.225V,R196:4.99K%1/R0402-->1K%1/R0402;R197:20K%1/R0402-->47K%1/R0402;增加电容C35:1nF/0402; 4、MASKROM烧写口电流160mA/5V左右； 5、钱箱控制需要更改，控制逻辑需要反向，按照windows方案； 6、主板加倒角； 7、LPDDR3物料描述修正； 8、U43及相关电路删除，U43不适合24V电路，直接短路到后端； 9、4G_PIN7上拉电阻去掉； 10、SMBJ18CA物料封装描述有误，SMB； 11、客户要求，把打印机24V控制开关电路取消； 12、更新PCB散热器封装heat_sink_40x40； 13、VDD_LED供电电源调整为3.3V； 14、RTC电源VCC_RTC_BAT加串一个电阻； 15、喇叭左右声道CODEC到PA信号L/R对换； 16、BOM的跳帽默认接法说明； 17、DDR电源休眠电路不贴； 18、LPDDR3的VDD1供电电源VCC18_DDR更改用LDO-1.8V供电，使能用VCC_DDR； 19、触摸屏电源3.3V更改为对应5V转3.3V-LDO输出； 20、SIM卡座侧边固定脚钢网不开孔； 21、HDMI增加工装测试TP点； 22、倒F排版方式，工艺边增加SMT方向箭头标识； 23、板号变更为CTD-RK3288；	
CTD-RK3288_V1.1	2020.10.13	LIN LINGMIN	1、TP1_USB_DM/P更改到CN8的PIN4和PIN6脚，同时预留电阻R477,R496到原PIN10和PIN12脚； 2、更改R569:6.8K/R0402-->3.6K/R0603； 3、R121:120K/R0402-->150K/R0402;R75:27K/R0402-->31.6K/R0402； 4、C852:4.7uF/C0603-->22uF/C0603；	1、客户增加副屏摄像头考虑； 2、副屏USB摄像头电流增大； 3、调整3G/4G电压VDD_3G为3.45V； 4、增大副屏USB摄像头电源电容；
CTD-RK3288_V2.0	2021.02.03	LIN LINGMIN	1.U25 USB HUB更换为FE1.1； 2.增加INCS8801S的PMD软件控制； 3.增加LVDS屏接口； 4.调整HDMI接口及DB9接口设计； 5.删除CPU晶振的分地电阻设计； 6.WIFI更改为AP6256；	
CTD-RK3288_V3.0	2021.04.26	LIN LINGMIN	1.Audio codec: ALC5651-->ES8316； 2.PMIC:ACT8846-->RK808-B； 3.FAN_CTRL用于控制9.7Inch LVDS LED；	
	2021.08.06	LIN LINGMIN	1.MQ20:N-MOS,VIC1231DJ-->P-MOS,VIC123DJ；	
	2022.08.06	LIN LINGMIN	1.EC_USB_EN2增加一个R554:100R/R0402电阻到EC_USB_EN1,R391:10K/R0402-->NC；	1.客户新增机型适配；



RK808-B Power Diagram and Sequence



Power Name	PMIC Channel	Time Slot (step 2ms)	Default ON/OFF	default voltage	sleep ON/OFF
VDD_10	VLD03	slot:1	ON	1.0V	ON
VDD_CPU	DDC1	slot:2	ON	1.1V	OFF
VDD_GPU	DDC2	slot:3	ON	1.1V	OFF
VCC_DDR	DDC3	slot:3	ON	DDR3 1.5V DDR3L 1.35V LPDDR 1.25V	ON
VCC_L06	EX_DDC	slot:3A	ON	1.1V	ON
VCC_18	VLD07	slot:3	ON	1.8V	ON
VCC_TP	VLD01	slot:4	ON	1.8V	ON
VCC_IO	DDC4	slot:4	ON	3.3V	ON
VCCI0_SD	VLD05	slot:5	ON	3.3V	OFF
VCC_SD	VSWOUT1	slot:5	ON	3.3V	OFF
VDD18_LCD	VLD06	N/A	OFF	1.8V	OFF
VCC18_LCD	VLD08	N/A	OFF	1.8V	OFF
VCCA_CODECC	VLD02	N/A	OFF	3.3V	OFF
VCC_WL	VLD04	N/A	OFF	1.8V	OFF
VCC_LCD	VSWOUT2	N/A	OFF	3.3V	OFF

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Power Tree

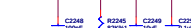
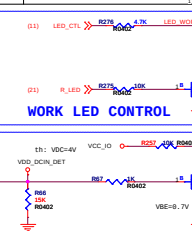
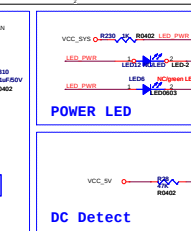
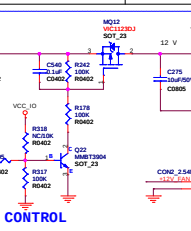
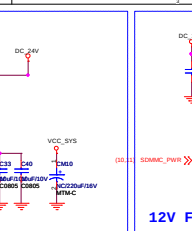
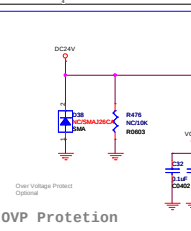
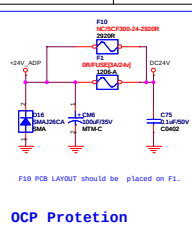
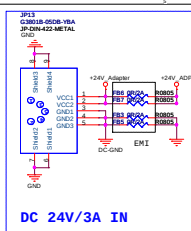
Size Custom Document Number CTD-RK3288

Date: Friday, November 18, 2022

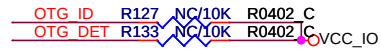
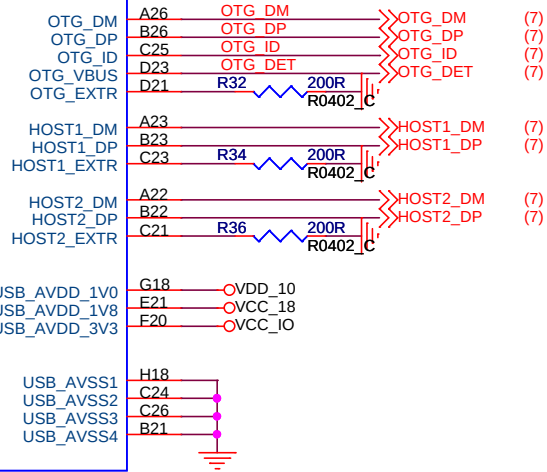
Sheet 4 of 25

Rev V3.0

RYD



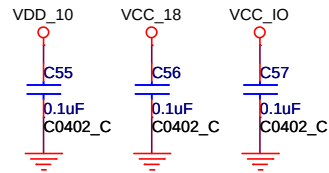
U1E
MCU_RK3288



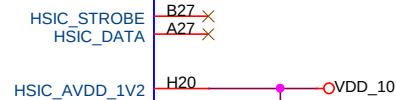
HOST1 only support USB 2.0 profile.No support USB1.1

HOST2 can support both USB 2.0/1.1 profile.
for sata

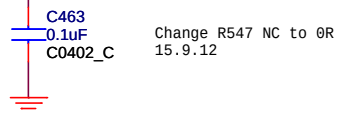
RK3288_E



U1U
MCU_RK3288



RK3288_U



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Title
RK3288 USB/HSIC Controller

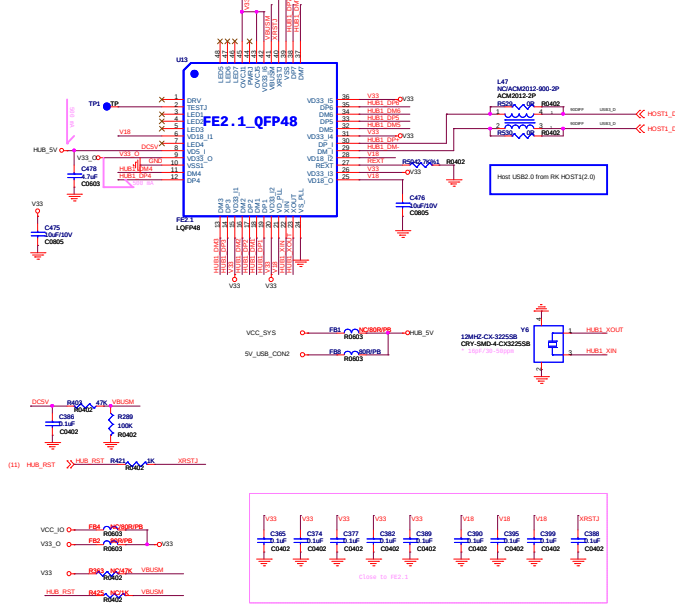
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CTD-RK3288



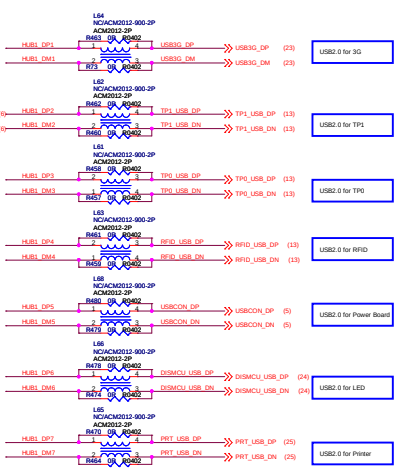
Rev
V3.0

Date: Friday, November 18, 2022 Sheet 6 of 25

USB HUB1

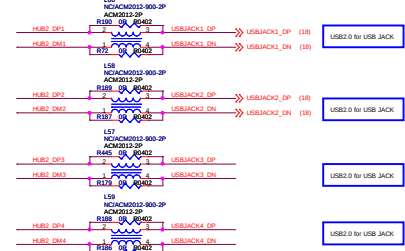


PLACED CLOSE TO INTERFACE CON

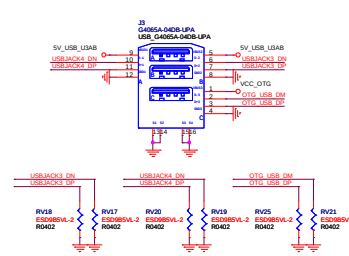
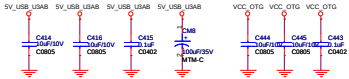


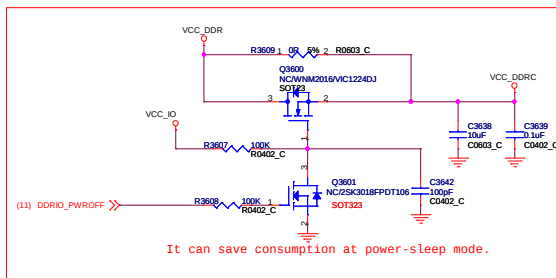
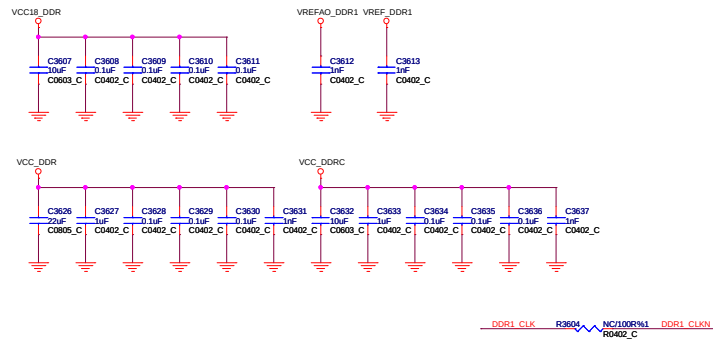
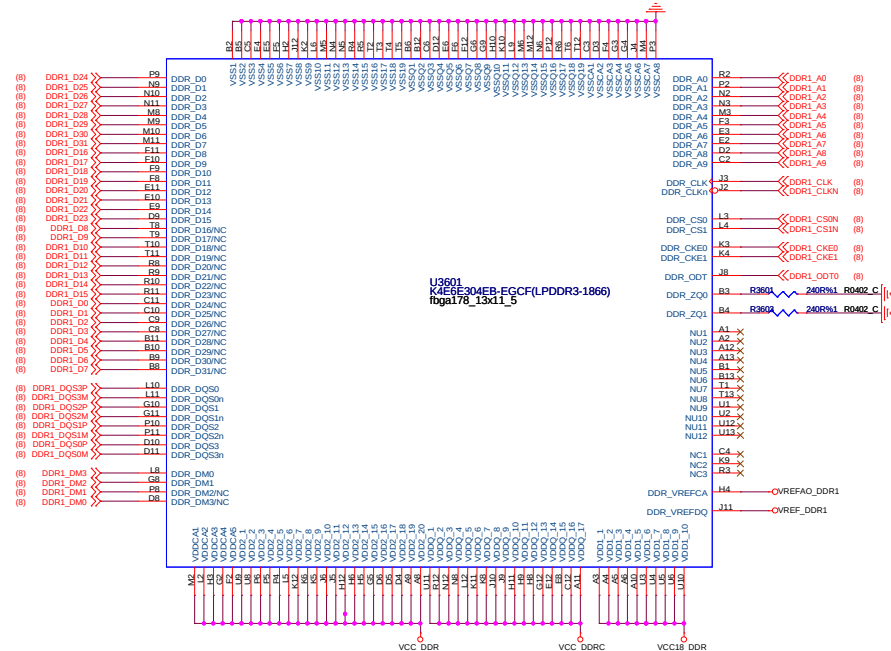
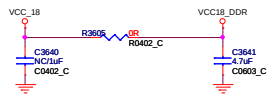
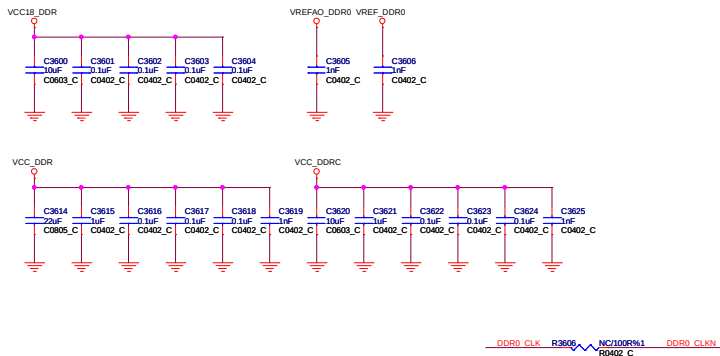
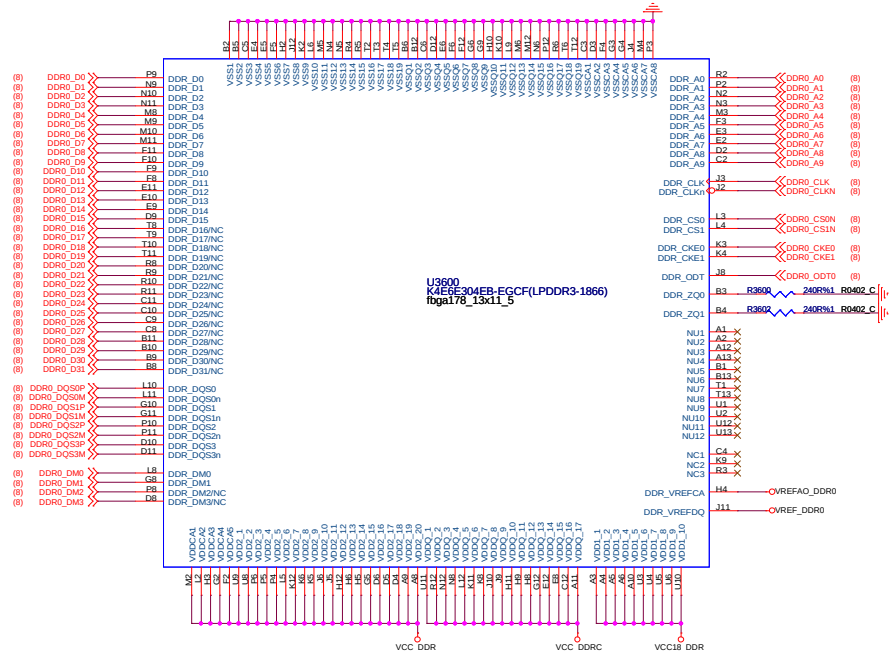
Host1-HUB1
HUB-USB1
HUB-USB2
HUB-USB3
HUB-USB4
HUB-USB5
HUB-USB6
HUB-USB7

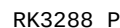
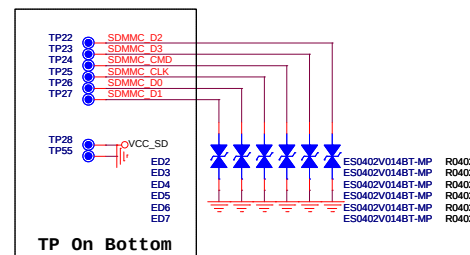
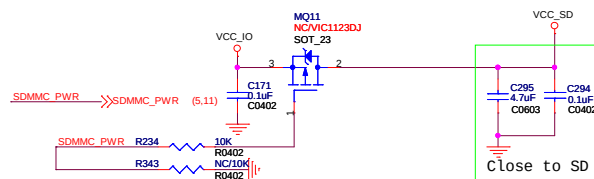
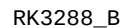
PLACED CLOSE TO INTERFACE CON



OTG
Host1-HUB2
HUB-USB1
HUB-USB2
HUB-USB3
HUB-USB4







接1.8V:1.8V
悬空: 3.3V

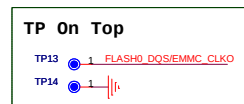
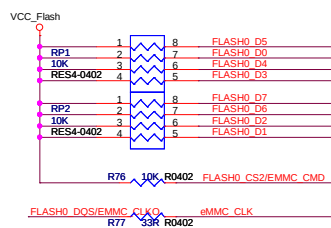
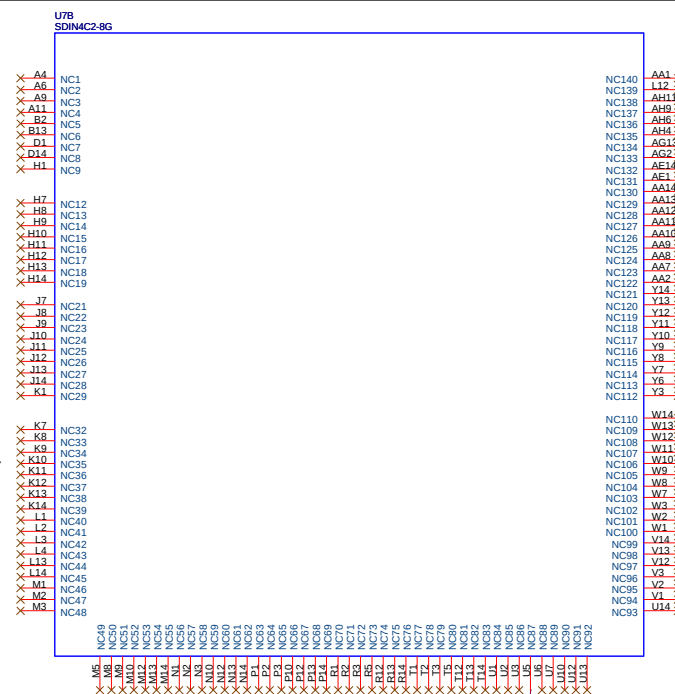


Note:
Reserve a PAD.

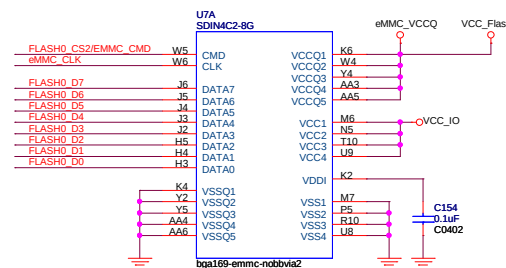
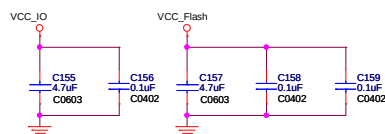


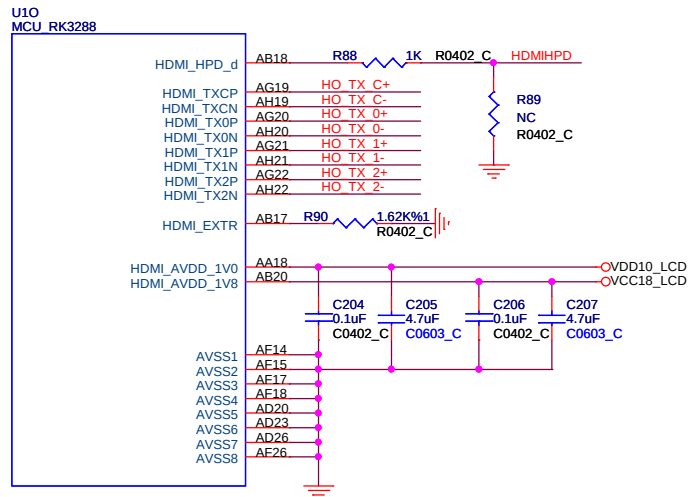
n1) 使用 eMMC 1.8V IO 时, Nand flash 的 FLASH0_RDY 上拉电阻不能贴, 否则 VCC_IO 电压会漏到 VCC_Flash 上, 造成 eMMC 没有读写时, VCC_Flash 电压会被拉到 2.2~2.4V。该参考图默认使用 1.8V IO eMMC, R68 电阻要更新为 NC, 不贴。

note: if use toshiba and sandisk DDR mode, R213 and R212 must be 0R.



Note:
Reserve a PAD.

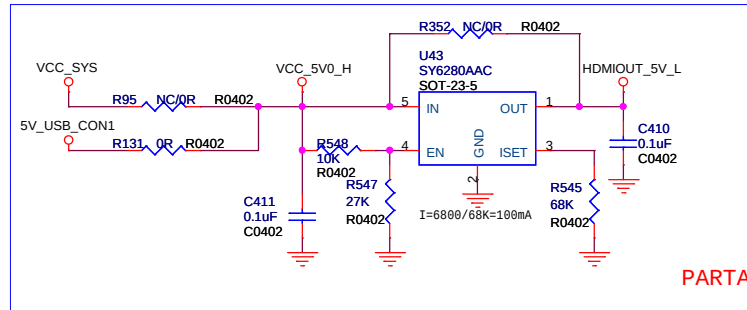
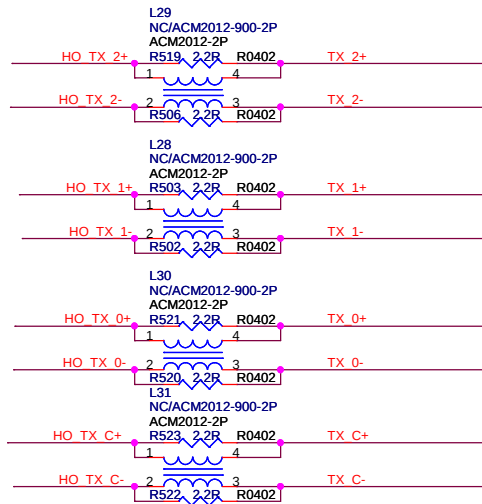




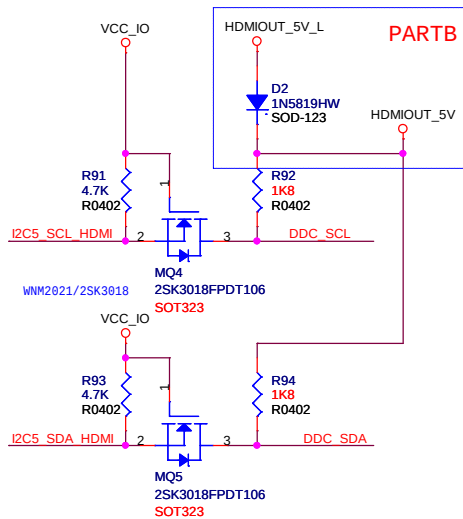
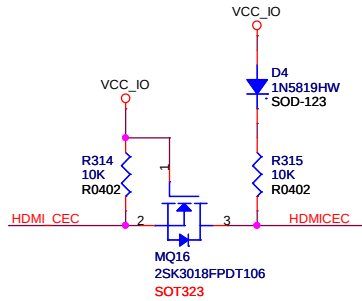
RK3288_0

I2C5_SDA_HDMI I2C5_SDA_HDMI (11)
I2C5_SCL_HDMI I2C5_SCL_HDMI (11)

HDMI_CEC HDMI_CEC (11)

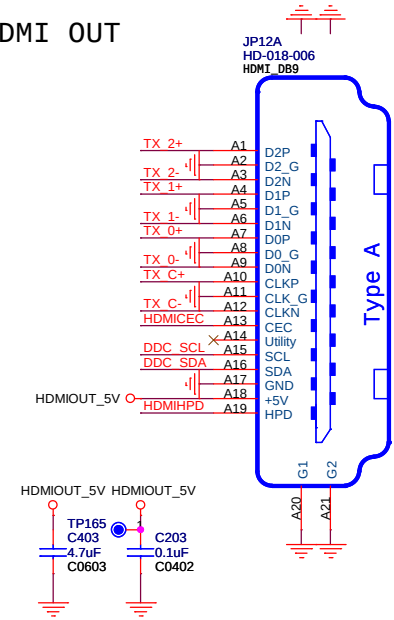


HDMI 5V Current limit
and intrusion prevention

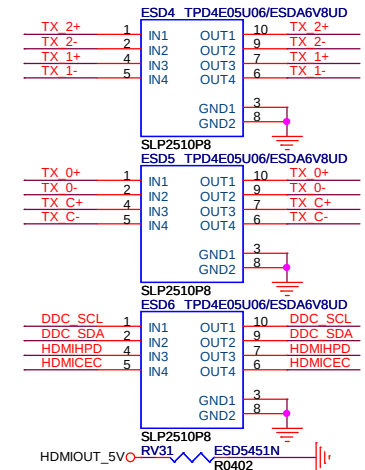


I2C5_SCL_HDMI 和 I2C5_SDA_HDMI 上拉电阻更新为 4.7K (原先是 1.5K),
解决有些电视 EDID 芯片驱动能力小,
造成 EDID 读取失败, 即提高 HDMI 兼容性;
另外软件上也需把内部的默认上拉关掉。

HDMI OUT

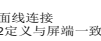
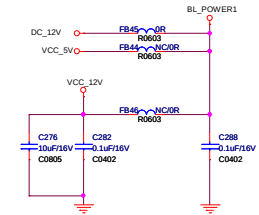
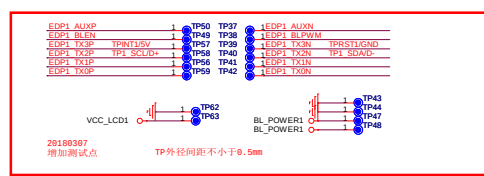
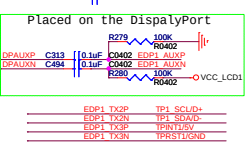
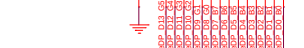
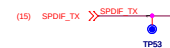
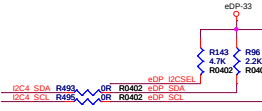


HDMI typed-A Connector



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Title	HDMI OUT		Rev
Size	Custom	Document Number	V3.0
Date:	Friday, November 18, 2022	Sheet	12 of 25



U1A
MCU RK3288

LCDC domain

LCDC0_HSYNC/GPIO1_D0_d
LCDC0_VSYNC/GPIO1_D1_d
LCDC0_DEN/GPIO1_D2_d
LCDC0_DCLK/GPIO1_D3_d

AA23 LCD HSYNC
AB24 LCD VSYNC
AA22 LCD DEN
AA24 LCD CLK

TRACE_D0/LCDC0_D0/LVDS_D0P
TRACE_D1/LCDC0_D1/LVDS_D0N
TRACE_D2/LCDC0_D2/LVDS_D1P
TRACE_D3/LCDC0_D3/LVDS_D1N
TRACE_D4/LCDC0_D4/LVDS_D2P
TRACE_D5/LCDC0_D5/LVDS_D2N
TRACE_D6/LCDC0_D6/LVDS_D3P
TRACE_D7/LCDC0_D7/LVDS_D3N
TRACE_D8/LCDC0_D8/LVDS_D4P
TRACE_D9/LCDC0_D9/LVDS_D4N
TRACE_D10/LCDC0_D10/LVDS_CLK0P
TRACE_D11/LCDC0_D11/LVDS_CLK0N
TRACE_D12/LCDC0_D12/LVDS_D5P
TRACE_D13/LCDC0_D13/LVDS_D5N
TRACE_D14/LCDC0_D14/LVDS_D6P
TRACE_D15/LCDC0_D15/LVDS_D6N
TRACE_CLK/LCDC0_D16/LVDS_D7P
TRACE_CTL/LCDC0_D17/LVDS_D7N
LCDC0_D18/LVDS_D8P
LCDC0_D19/LVDS_D8N
LCDC0_D20/LVDS_D9P
LCDC0_D21/LVDS_D9N
LCDC0_D22/LVDS_CLK1P
LCDC0_D23/LVDS_CLK1N

LVDS_EXTR

LVDS domain

LVDS_AVDD_1V0
LVDS_AVDD_1V8
LVDS_AVDD_3V3

AA20 OVDD10_LCD
AB21 OVCC18_LCD
AB23

R164 OR R0402 OVCC_LCD1

C327
0.1uF
C0402_C

R164建议预留不能删除。

U1I
MCU RK3288

I2S_SCLK/GPIO6_A0_d
I2S_LRCK_RX/GPIO6_A1_d
I2S_LRCK_TX/GPIO6_A2_d
I2S_SDI/GPIO6_A3_d
I2S_SDO0/GPIO6_A4_d
I2S_SDO1/GPIO6_A5_d
I2S_SDO2/GPIO6_A6_d
I2S_SDO3/GPIO6_A7_d
I2S_CLK/GPIO6_B0_d
I2C2_SDA/GPIO6_B1_u
I2C2_SCL/GPIO6_B2_u
SPDIF_TX/GPIO6_B3_d

APIO4_VDD

AD11 I2S SCLK
AG11 I2S LRCK RX
AF11 I2S LRCK TX
AE11 I2S SDI
AG12 I2S SDO0
AH13
AG13
AH12
AC12 I2S MCLK
AF12 I2C2 SDA
AD12 I2C2_SCL
AE12 SPDIF_TX

Y12 OVCCIO_CODEC
C239
0.1uF
C0402_C

LCD_HSYNC LCD_HSYNC (14)
LCD_VSYNC LCD_VSYNC (14)
LCD_DEN LCD_DEN (14)
LCD_CLK LCD_CLK (14)

LCD_D0 LCD_D0 (14)
LCD_D1 LCD_D1 (14)
LCD_D2 LCD_D2 (14)
LCD_D3 LCD_D3 (14)
LCD_D4 LCD_D4 (14)
LCD_D5 LCD_D5 (14)
LCD_D6 LCD_D6 (14)
LCD_D7 LCD_D7 (14)
LCD_D8 LCD_D8 (14)
LCD_D9 LCD_D9 (14)
LCD_D10 LCD_D10 (14)
LCD_D11 LCD_D11 (14)
LCD_D12 LCD_D12 (14)
LCD_D13 LCD_D13 (14)
LCD_D14 LCD_D14 (14)
LCD_D15 LCD_D15 (14)
LCD_D16 LCD_D16 (14)
LCD_D17 LCD_D17 (14)
LCD_D18 LCD_D18 (14)
LCD_D19 LCD_D19 (14)
LCD_D20 LCD_D20 (14)
LCD_D21 LCD_D21 (14)
LCD_D22 LCD_D22 (14)
LCD_D23 LCD_D23 (14)

I2S_SCLK I2S_SCLK (16)
I2S_LRCK_RX I2S_LRCK_RX (16)
I2S_LRCK_TX I2S_LRCK_TX (16)
I2S_SDI I2S_SDI (16)
I2S_SDO0 I2S_SDO0 (16)
I2S_MCLK I2S_MCLK (16)

SPDIF_TX SPDIF_TX (14)

RK3288_I

RK3288_A

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Title
RK3288 LCDC/I2S Controler

Size A4 Document Number
CTD-RK3288



Rev
V3.0

Date: Friday, November 18, 2022 Sheet 15 of 25

U1Q
MCU_RK3288

HOST_D0/MAC_TXD2/SDIO1_D0/FLASH1_D0/GPIO3_D0_u
HOST_D1/MAC_TXD3/SDIO1_D1/FLASH1_D1/GPIO3_D1_u
HOST_D2/MAC_RXD2/SDIO1_D2/FLASH1_D2/GPIO3_D2_u
HOST_D3/MAC_RXD3/SDIO1_D3/FLASH1_D3/GPIO3_D3_u
HOST_D4/MAC_TXD0/SDIO1_DET/FLASH1_D4/GPIO3_D4_u
HOST_D5/MAC_TXD1/SDIO1_WRPRT/FLASH1_D5/GPIO3_D5_u
HOST_D6/MAC_RXD0/SDIO1_BKPWR/FLASH1_D6/GPIO3_D6_u
HOST_D7/MAC_RXD1/SDIO1_INTn/FLASH1_D7/GPIO3_D7_u

HOST_CKOUTP/MAC_MDC/FLASH1_RDY/GPIO4_A0_u
HOST_CKOUTN/MAC_RXDV/FLASH0_CSn4/FLASH1_WP/GPIO4_A1_u
HOST_D8/MAC_RXER/FLASH0_CSn5/FLASH1_RDN/GPIO4_A2_u
HOST_D9/MAC_CLK/FLASH0_CSn6/FLASH1_ALE/GPIO4_A3_u
HOST_D10/MAC_TXEN/FLASH0_CSn7/FLASH1_CLE/GPIO4_A4_u
HOST_D11/MAC_MDIO/FLASH1_WRN/GPIO4_A5_u
HOST_D12/MAC_RXCLK/SDIO1_CMD/FLASH1_CSn0/GPIO4_A6_u
HOST_D13/MAC_CRS/SDIO1_CLKOUT/FLASH1_CSn1/GPIO4_A7_u
HOST_D14/MAC_COL/FLASH1_DQS/FLASH1_CSn3/GPIO4_B0_u
HOST_D15/MAC_TXCLK/SDIO1_PWREN/FLASH1_CSn2/GPIO4_B1_u

FLASH1_VDD

Y4
V6
AB1
AC1
AD1
AB2
AA3
AA4

AC3
AC2
AE1
AE2
AD2
Y5
AB5
AA6
AA5
V7

VCC_LAN

C247
0.1uF
C0402_C

RK3288_Q

MAC_TXD0
MAC_TXD1
MAC_RXD0
MAC_RXD1

MAC_MDC
MAC_CRS_DV
MAC_RXER
MAC_CLK
MAC_TXEN
MAC_MDIO

RMII_RST

RMII_TX_D0 (18)
RMII_TX_D1 (18)
RMII_RX_D0 (18)
RMII_RX_D1 (18)

RMII_MDCLK (18)
RMII_CSR_VALID (18)
RMII_RX_ERR (18)
RMII_CLKO (18)
RMII_TX_EN (18)
RMII_MD (18)

RMII_RST (18)

Table 41-1 RMII Interface Description

Module pin name	Direction	Pad name	IOMUX
RMII interface			
mac_clk	I/O	GPIO4_A[3]	GRF_GPIO4AL_IOMUX[14:12]=3'b011
mac_txen	O	GPIO4_A[4]	GRF_GPIO4AH_IOMUX[2:0]=3'b011
mac_tx1	O	GPIO3_D[5]	GRF_GPIO3DH_IOMUX[6:4]=3'b011
mac_tx0	O	GPIO3_D[4]	GRF_GPIO3DH_IOMUX[2:0]=3'b011
mac_rxdv	I	GPIO4_A[1]	GRF_GPIO4AL_IOMUX[6:4]=3'b011
mac_rxer	I	GPIO4_A[2]	GRF_GPIO4AL_IOMUX[10:8]=3'b011
mac_rxd1	I	GPIO3_D[7]	GRF_GPIO3DH_IOMUX[14:12]=3'b011
mac_rxd0	I	GPIO3_D[6]	GRF_GPIO3DH_IOMUX[10:8]=3'b011
Management interface			
mac_mdio	I/O	GPIO4_A[5]	GRF_GPIO4AH_IOMUX[5:4]=2'b11
mac_mdc	O	GPIO4_A[0]	GRF_GPIO4AL_IOMUX[1:0]=2'b11

MAC_TXD0 R406 4.7K R0402 VCC_LAN
MAC_TXD1 R432 4.7K R0402 VCC_LAN

MAC_MDIO R181 NC/1K5 R0402 VCC_LAN

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Title
RK3288 EthernetMAC Controller

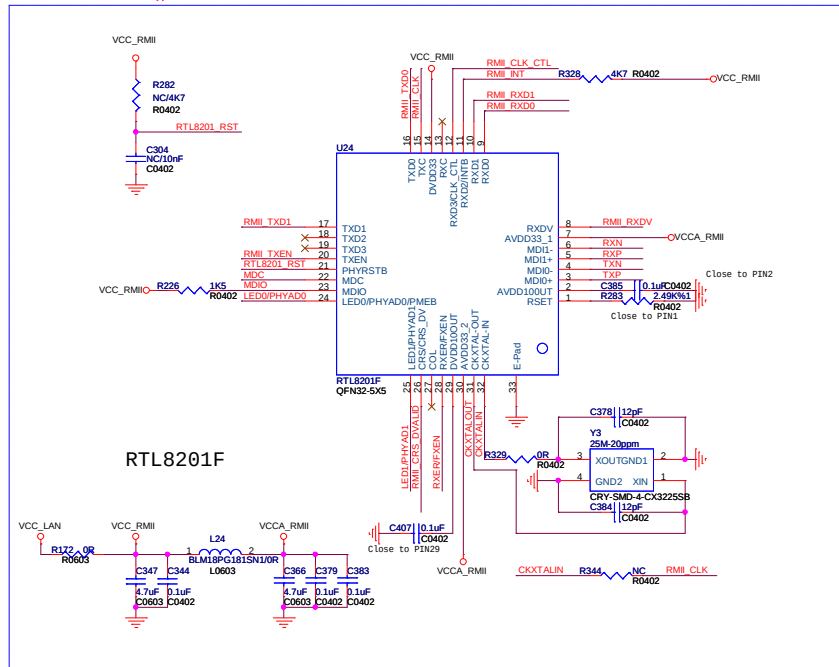
Size A4 Document Number
CTD-RK3288

Rev
V3.0

Date: Friday, November 18, 2022 Sheet 17 of 25

(17) RMII_TX_EN >> R154 33R R0402 RMII_TXEN
 (17) RMII_TX_D1 >> R155 33R R0402 RMII_TXD1
 (17) RMII_TX_D0 >> R166 33R R0402 RMII_TXD0
 (17) RMII_RX_D0 >> R163 33R R0402 RMII_RXD0
 (17) RMII_RX_D1 >> R168 33R R0402 RMII_RXD1
 (17) RMII_CLK >> R155 33R R0402 RMII_CLK
 (17) RMII_CSR_VALID >> R261 33R R0402 RMII_CSR_VALID
 (17) RMII_RX_ERR >> R231 33R R0402 RXER/FXEN
 (17) RMII_MD >> R250 33R R0402 MDIO
 (17) RMII_MDC >> R245 33R R0402 MDC
 (17) RMII_RST >> R251 33R R0402 RTL8201_RST

RMII_CLK NC C364 C0402



RMII REF_CLK direction

PHY Address/LED

Pull Low for RMII REF_CLK Output mode √ (8201F out)
 Pull High for RMII REF_CLK Input mode(default)

MII/RMII Selection

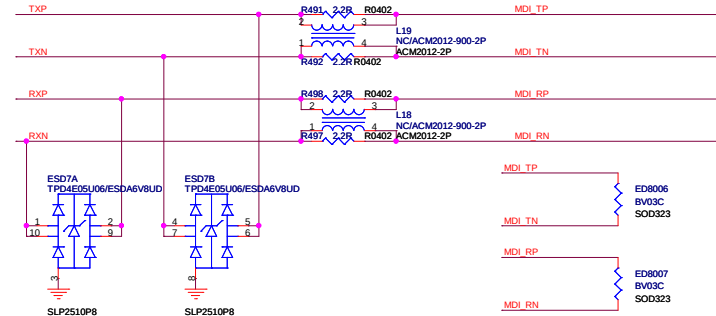
Pull High for RMII mode(default)

UTP / Fiber Selection

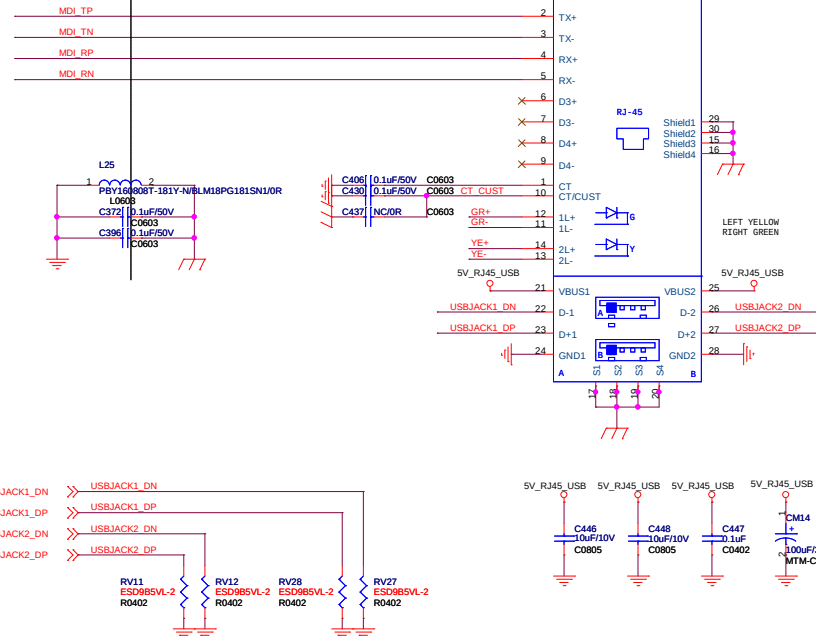
Pull Low for UTP Mode(default)
 Pull High for Fiber Mode

Pull Low for LED0 Mode(default)
 Pull High for WOL Mode
 WOL:Wake-on-LAN

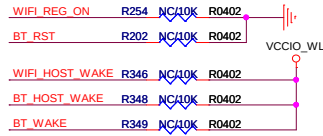
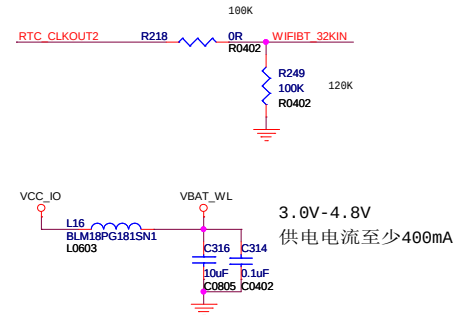
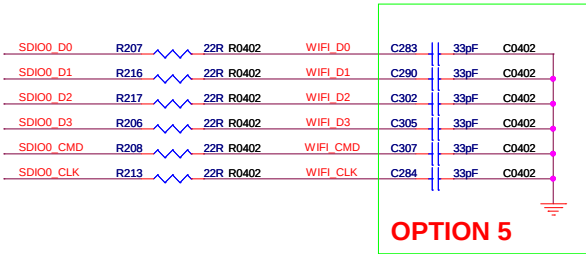
ESD



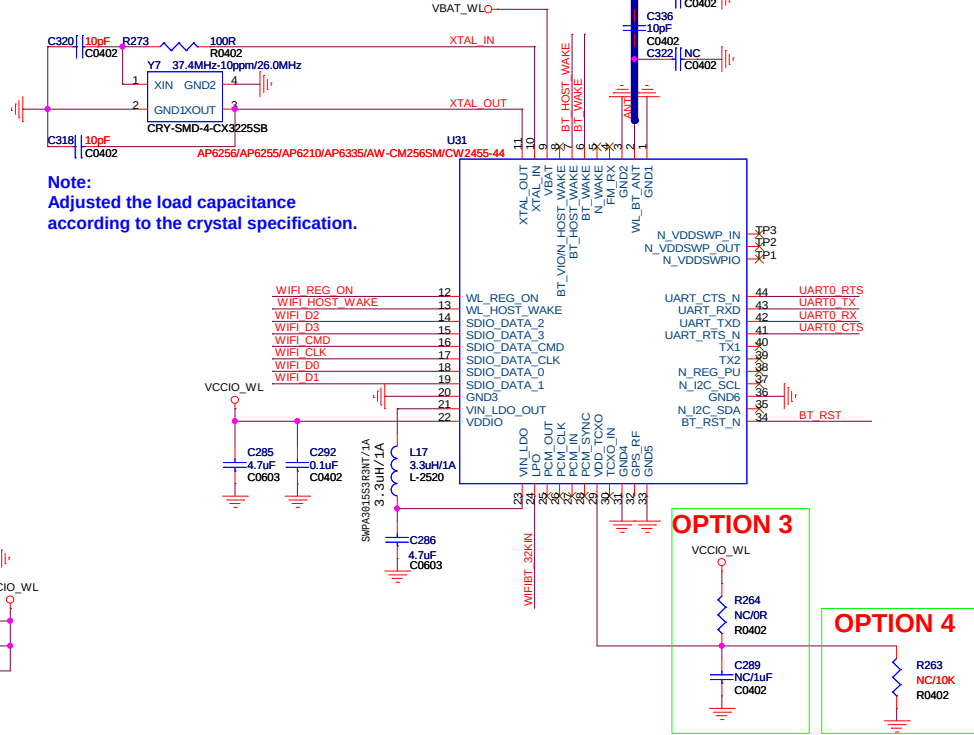
RJ45 Connector



UART0_RX >> UART0_RX (19)
 UART0_TX >> UART0_TX (19)
 UART0_CTS >> UART0_CTS (19)
 UART0_RTS >> UART0_RTS (19)
 SDIO0_D0 >> SDIO0_D0 (19)
 SDIO0_D1 >> SDIO0_D1 (19)
 SDIO0_D2 >> SDIO0_D2 (19)
 SDIO0_D3 >> SDIO0_D3 (19)
 SDIO0_CMD >> SDIO0_CMD (19)
 SDIO0_CLK >> SDIO0_CLK (19)
 BT_WAKE >> BT_WAKE (19)
 WIFI_REG_ON >> WIFI_REG_ON (19)
 BT_RST >> BT_RST (19)
 WIFI_HOST_WAKE >> WIFI_HOST_WAKE (19)
 BT_HOST_WAKE >> BT_HOST_WAKE (19)
 RTC_CLKOUT2 >> RTC_CLKOUT2 (5)



AP6234/AP6335/AP6255:37.4MHZ
Other:26MHZ



50 Ohm RF trace

For AP6255 R264/C289 KEEP NC;
Default 1.8V for SDIO3.0, R263 NC, VDDIO=1.8V;
3.3V only for SDIO2.0, R263 10K, VDDIO=3.3V;

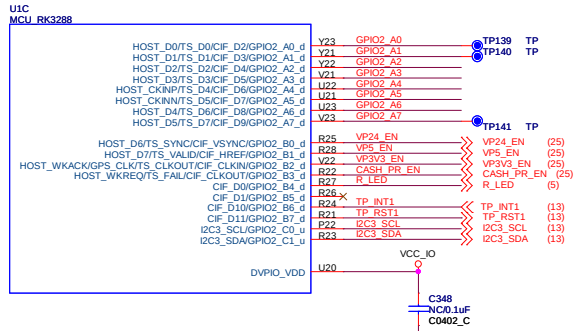
Note:
Yes: 框内要贴
No: 框内不贴

OPTION	WIFI				BT4.0	Crystals	VDDIO
	a	b/g/n	ac	5GHz			
AP6181		Yes				26MHz	1.71-3.6V
AP6234	Yes	Yes		Yes	Yes	37.4MHz	1.6-3.4V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V
AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V
AP6212		Yes			Yes	26MHz	
DEFAULT AP6255 /AP6256	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.71-3.63V 1.62-3.63V

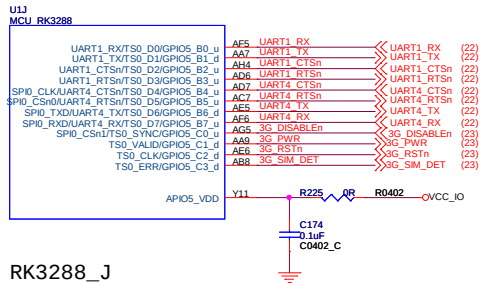
OPTION	3	4	5
AP6181	No	No	No
AP6234	No	No	No
AP6330	No	No	No
AP6335	No	Yes	Yes
AP6212	No	No	No
AP6255 /AP6256	No	ND/1.8V YES/3.3V	Yes

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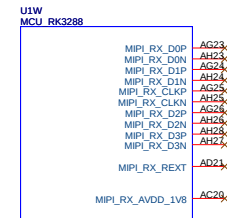
Title			
WIFI/BT			
Size	Document Number	Rev	
Custom	CTD-RK3288	V3.0	
Date:	Friday, November 18, 2022	Sheet 20 of 25	



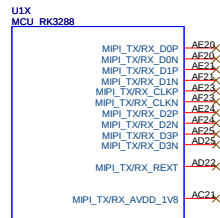
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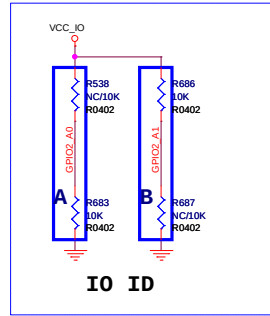
RK3288_J



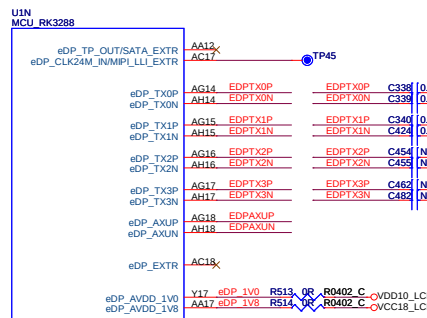
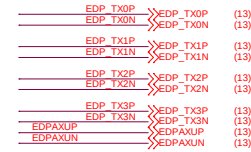
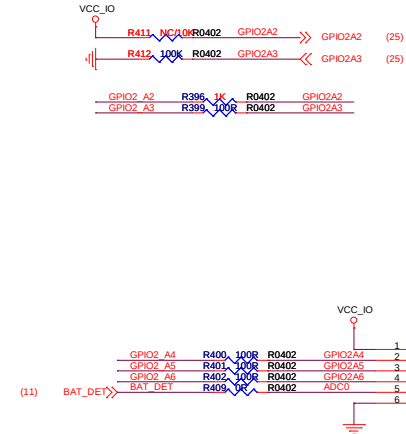
RK3288_W



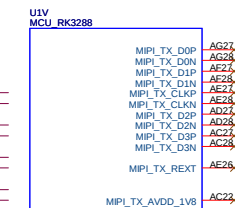
RK3288_X



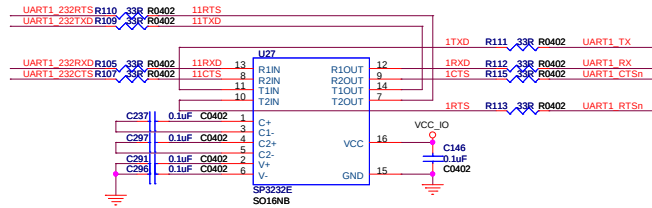
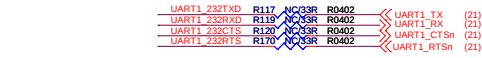
IO ID	A	B
CTD-RK3288-V1.0	0	0
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CTD-RK3288-V2.0	1	0
CTD-RK3288-V3.0	0	1



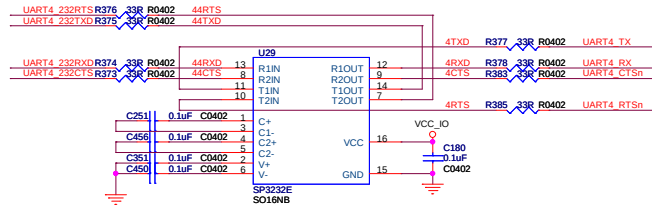
RK3288_N



RK3288_V

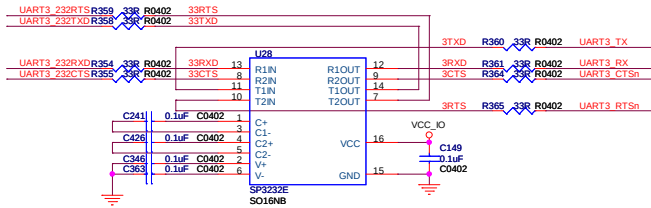
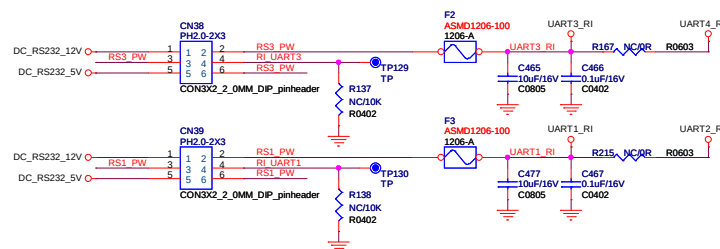
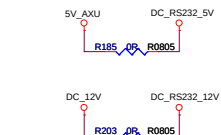


TTL-UART1 TO RS232-UART1

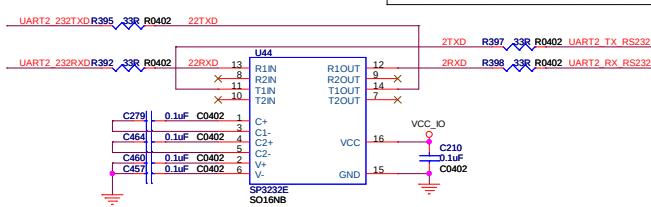


TTL-UART4 TO RS232-UART4

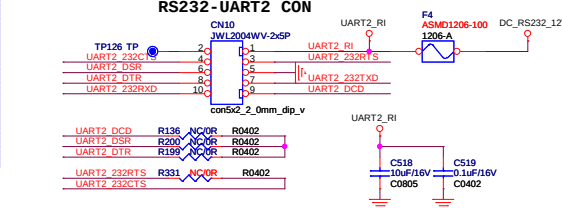
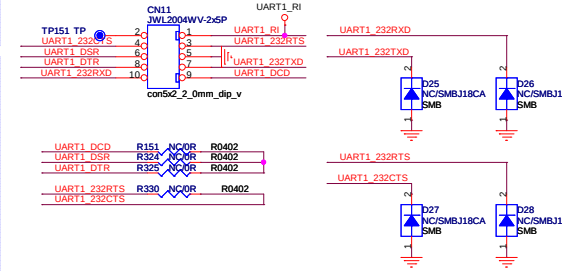
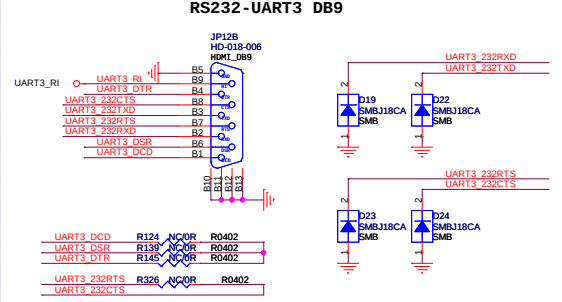
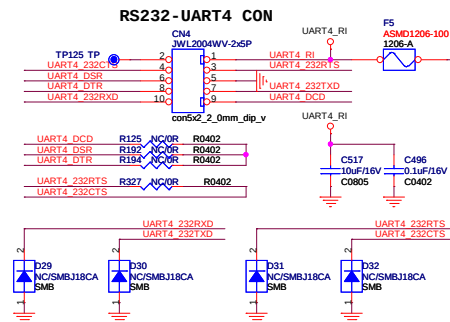
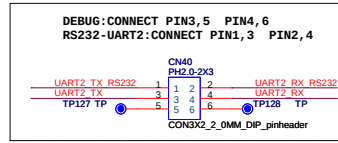
串口0 ===== BT
 串口1 ===== RS232
 串口2 ===== Debug/RS232
 串口3 ===== RS232
 串口4 ===== RS232

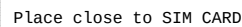
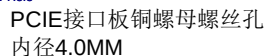


TTL-UART3 TO RS232-UART3



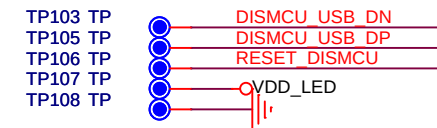
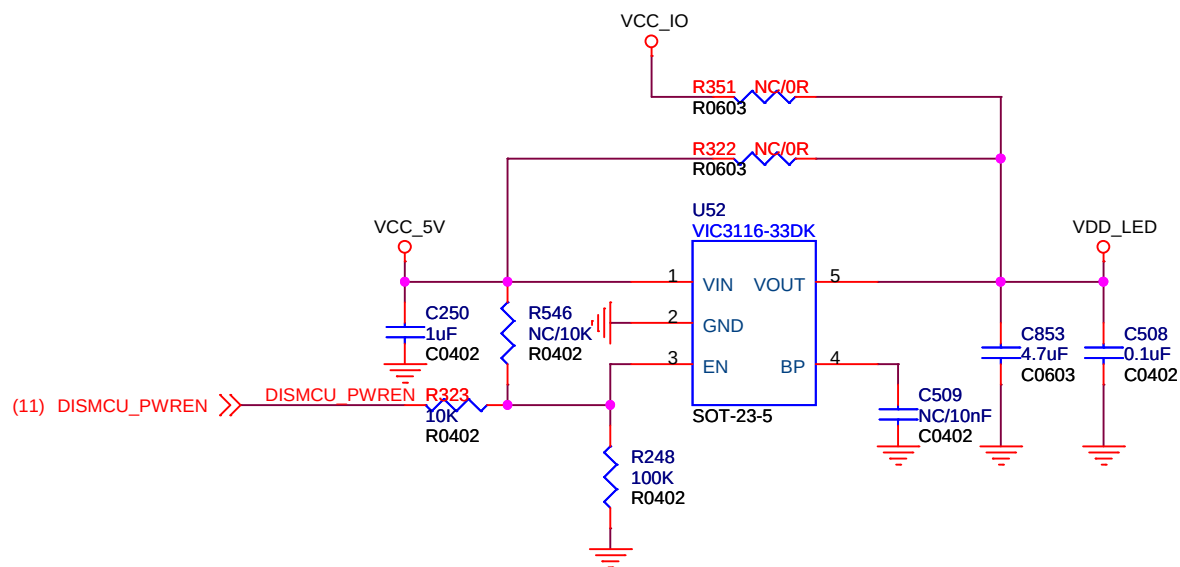
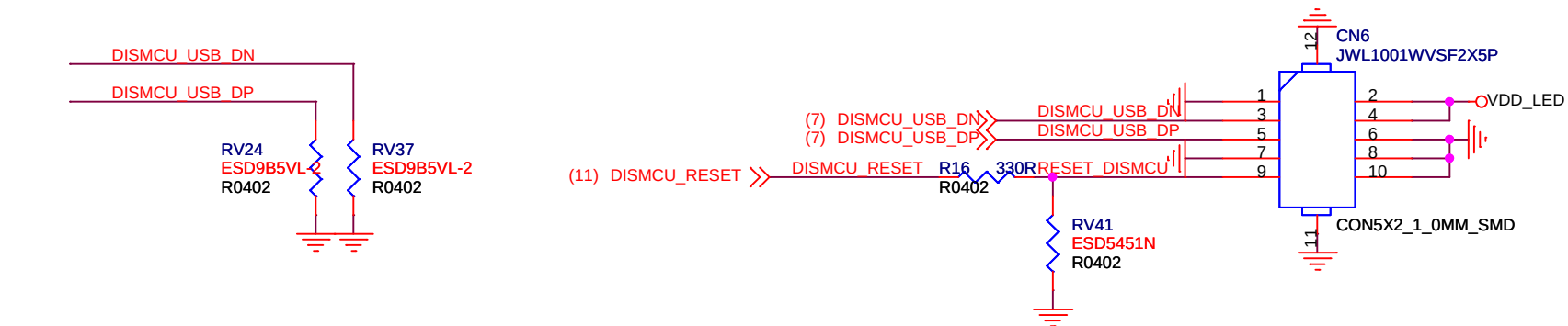
TTL-UART2 TO RS232-UART2





5. Under of RF alignment do not have any power traces or any data traces .





Placed in the same area on bottom.

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Title

Customer Display

Size
A

Document Number
CTD-RK3288

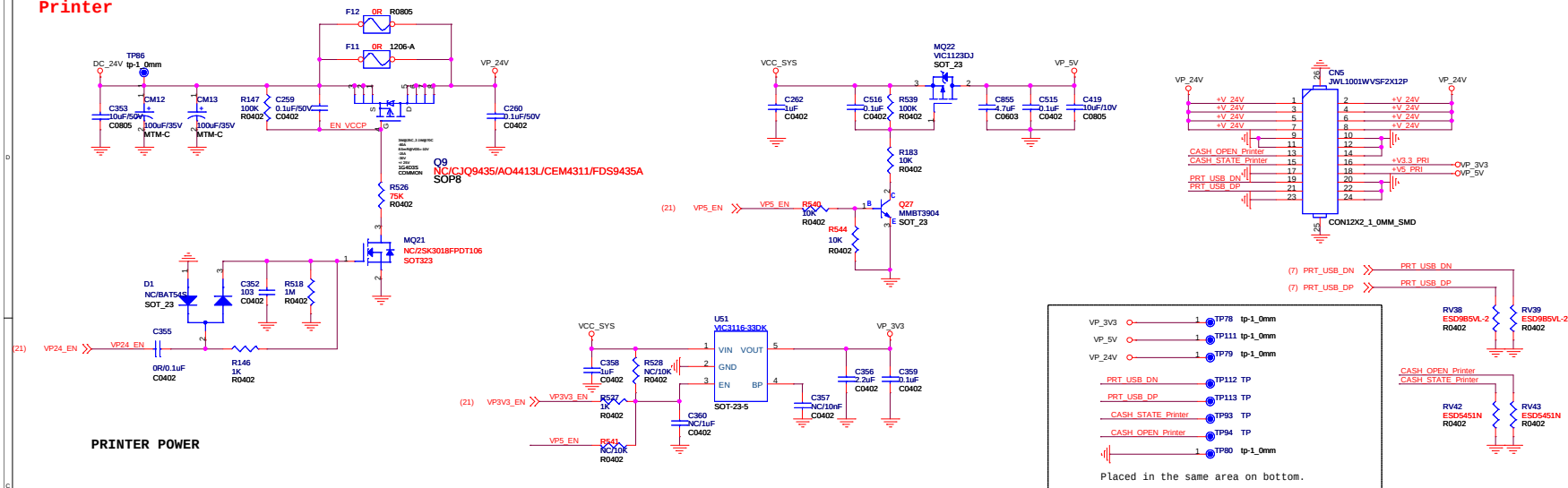
Rev
V3.0

Date: Friday, November 18, 2022

Sheet 24 of 25

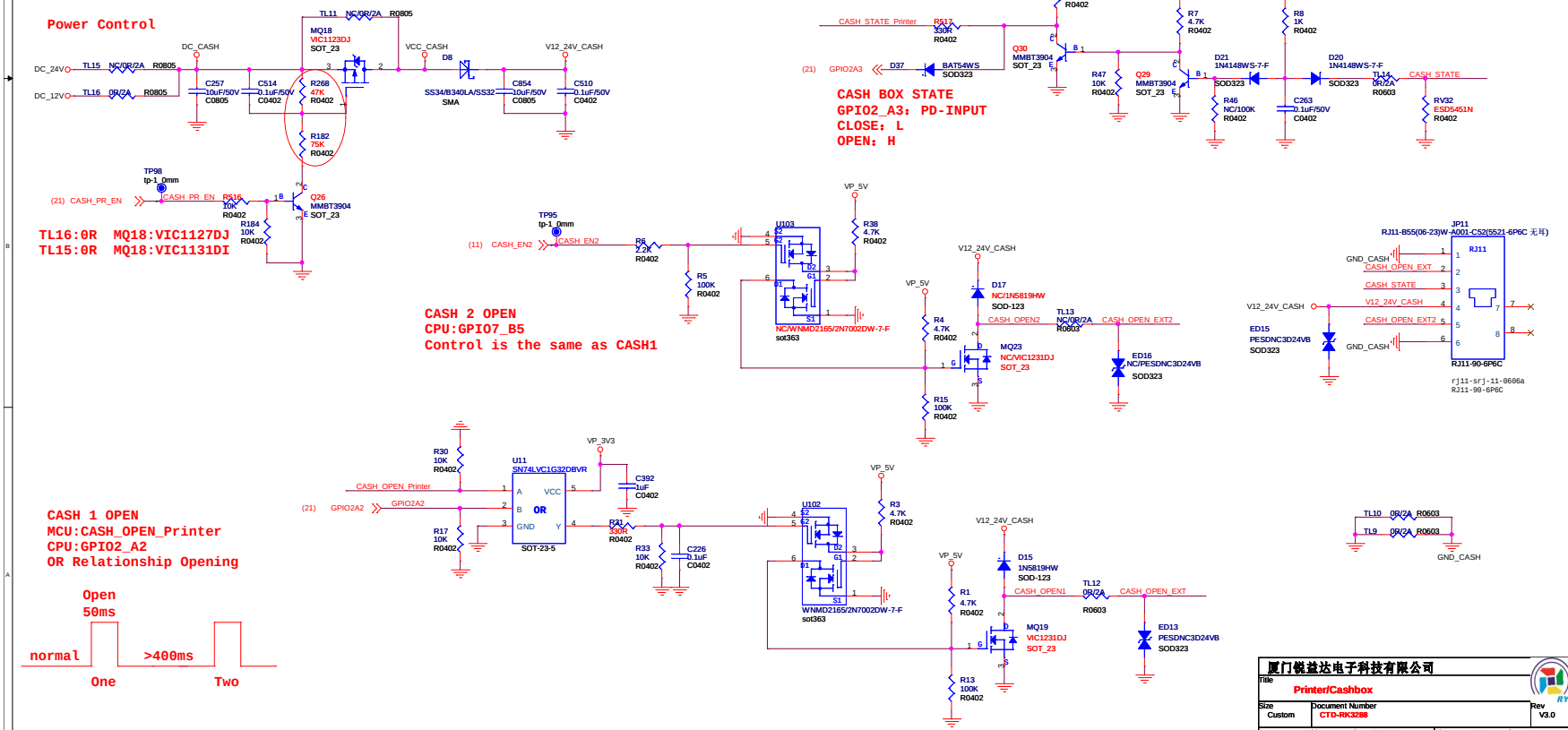


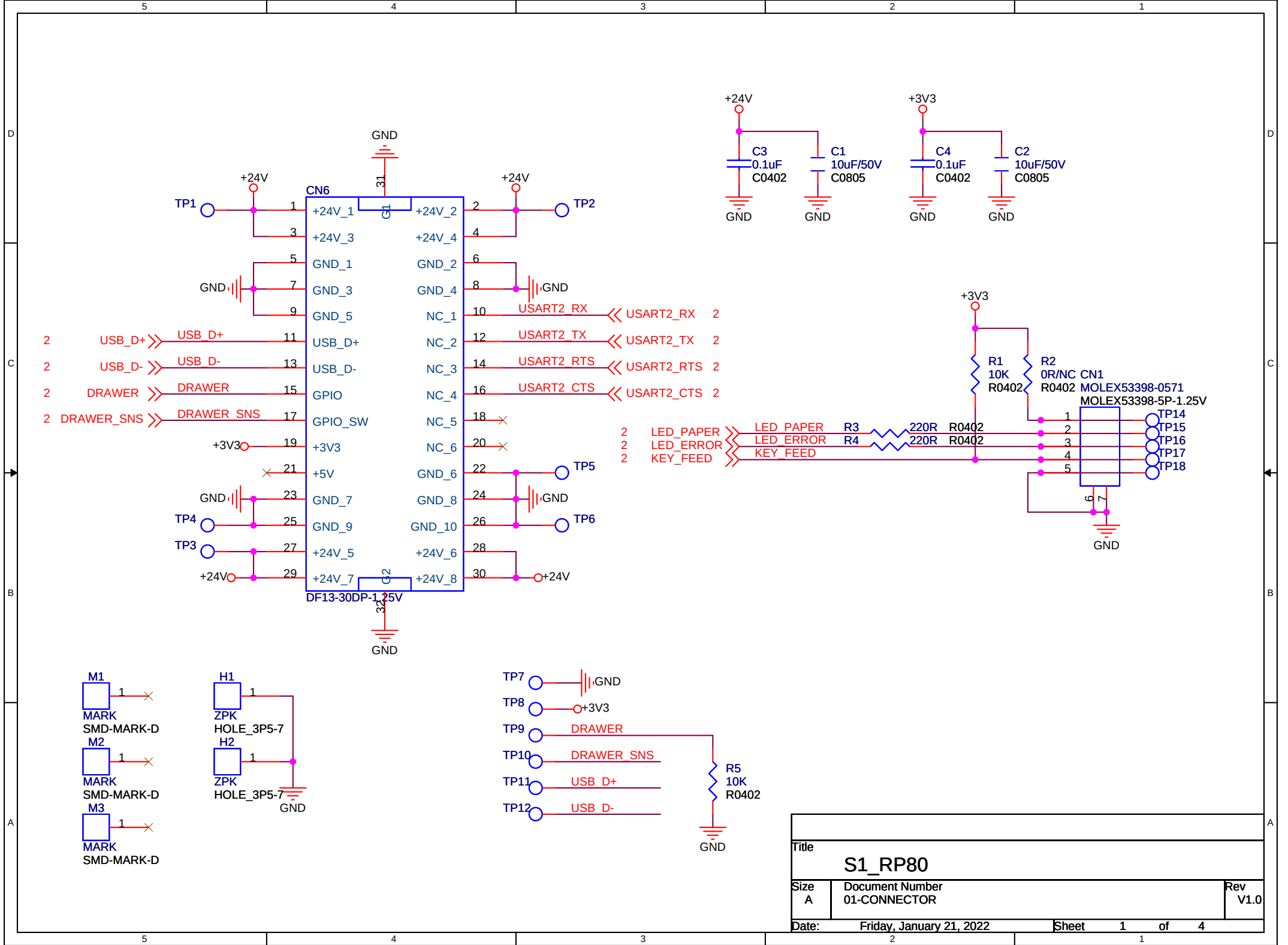
Printer

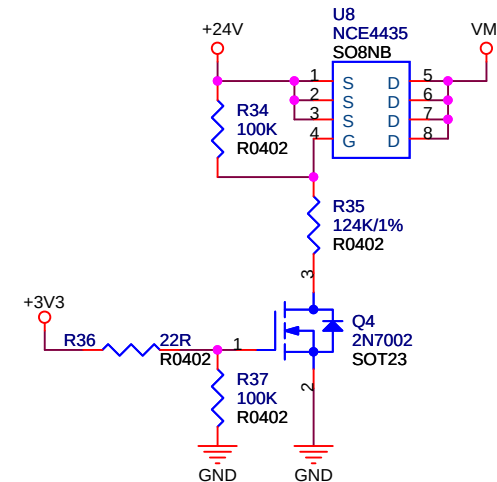
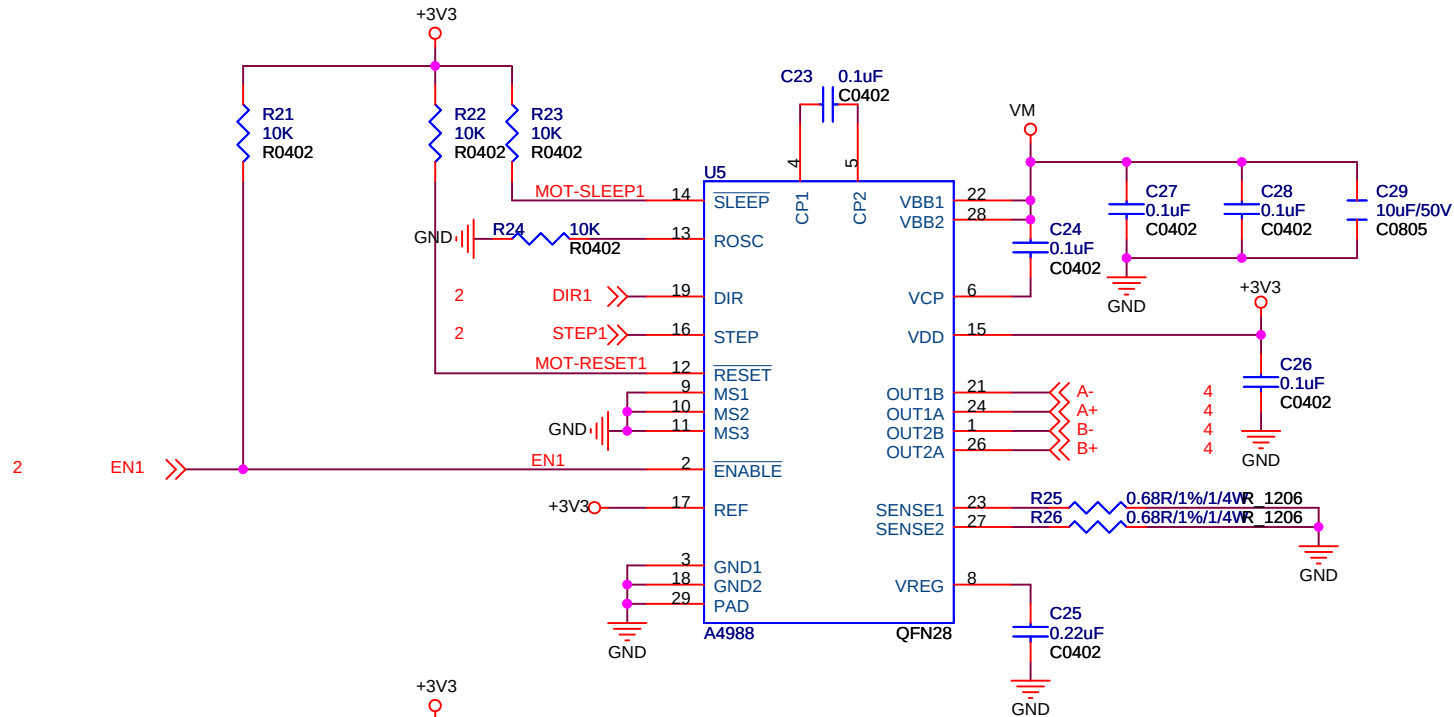


Cashbox

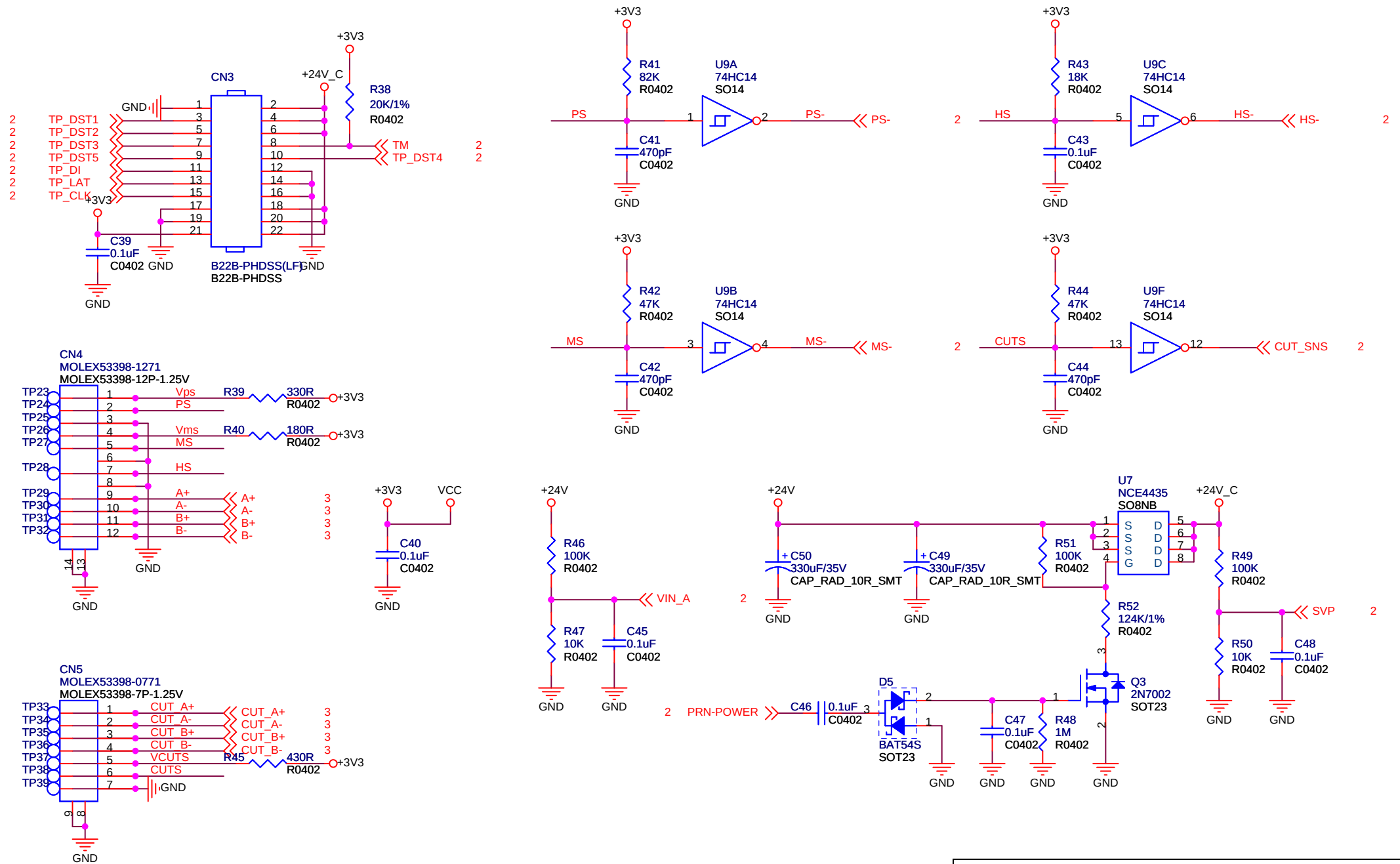
Power Control



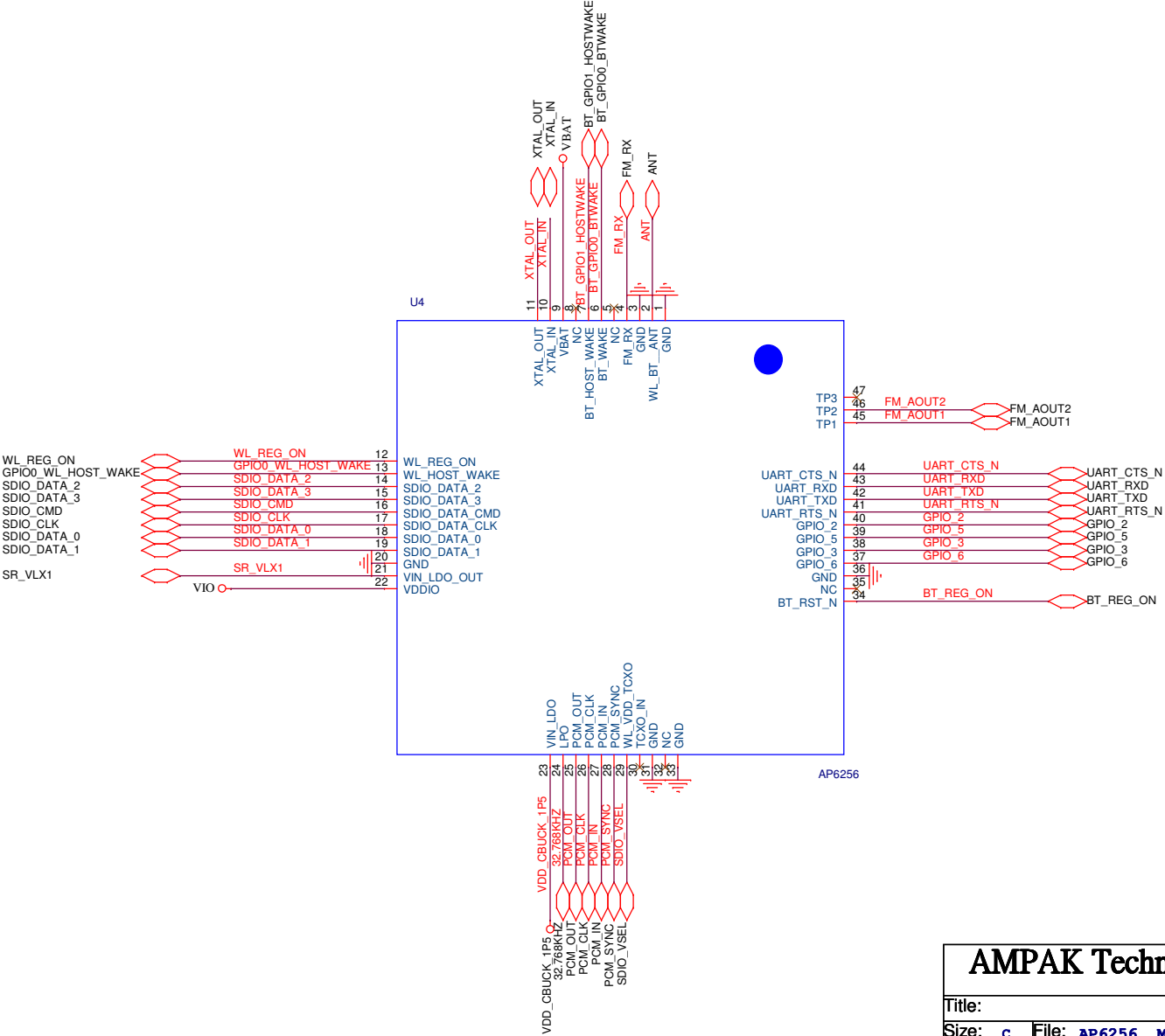




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S1_RP80		
Size	Document Number	Rev
A4	03-MOTOR DRIVER	V1.0
Date:	Friday, January 21, 2022	Sheet 3 of 4

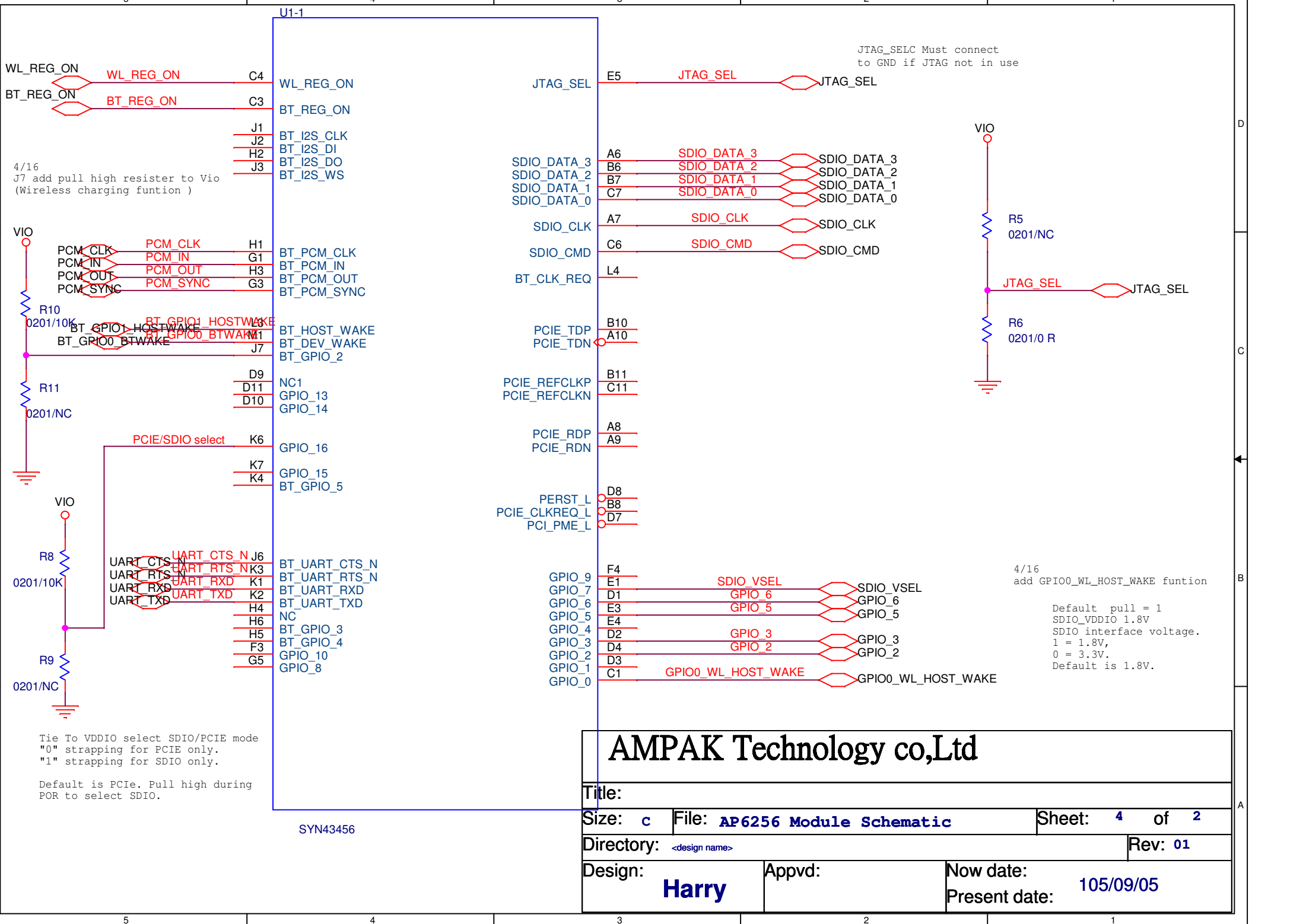


AP6256 Outline



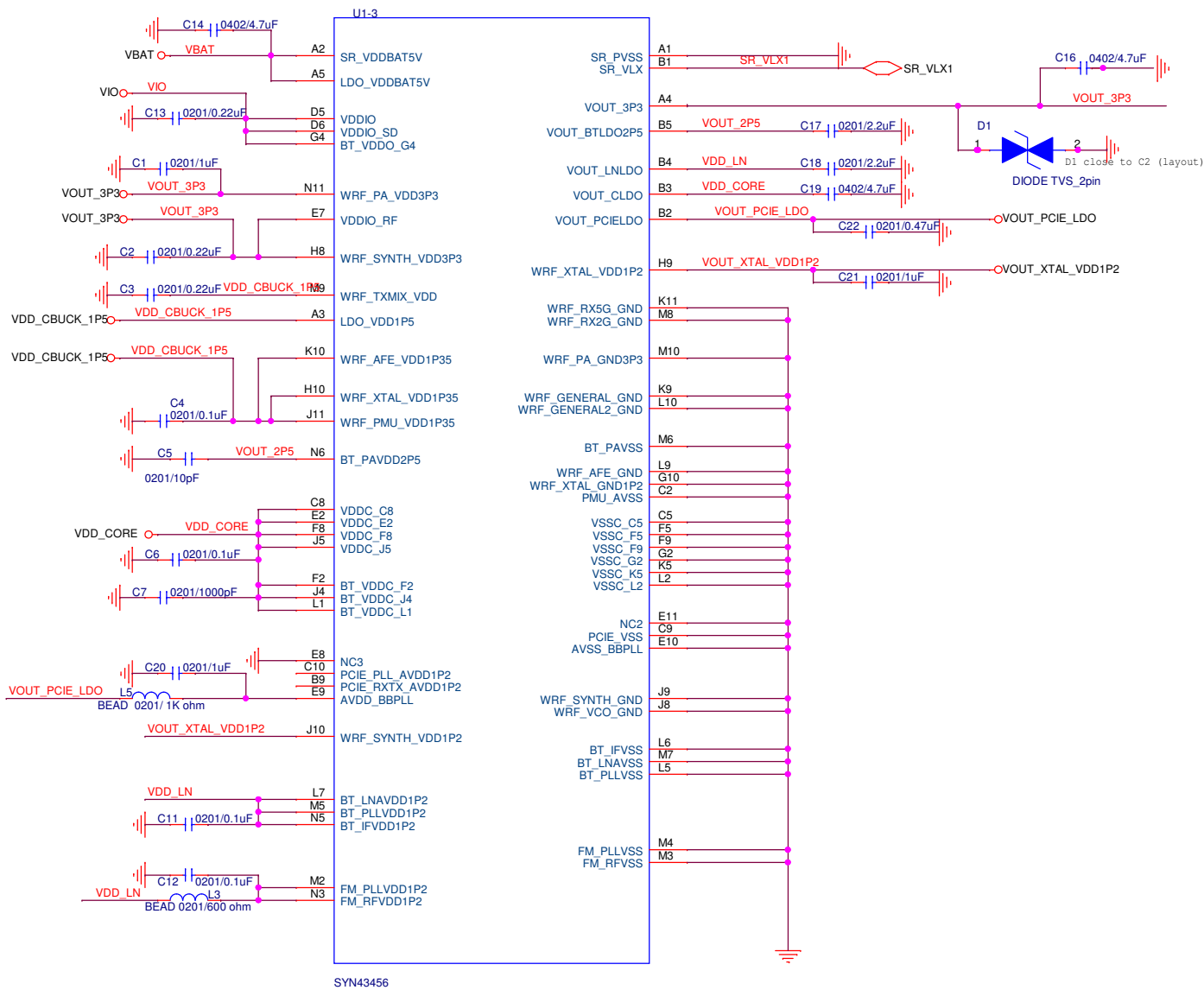
AP6255 SDIO 2.0/3.0 user guide for sdio_vsel
Default: pull = 1
SDIO_VDDIO 1.8V
SDIO interface voltage.
1 = 1.8V,
0 = 3.3V,
Default is 1.8V.

AMPAK Technology co,Ltd			
Title:			
Size: c	File: AP6256 Module Schematic	Sheet: 4	of 1
Directory:	<design name>		Rev: 00
Design:	Appvd:	Now date:	Present date: 106/09/05
Harry			

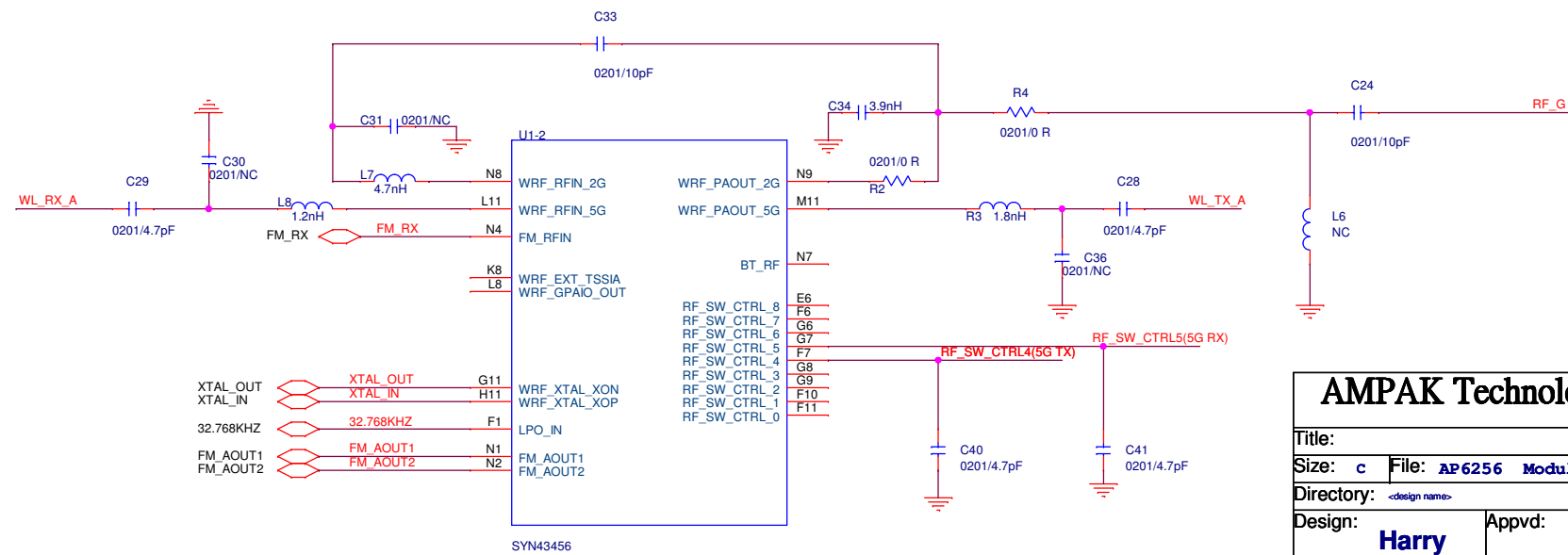
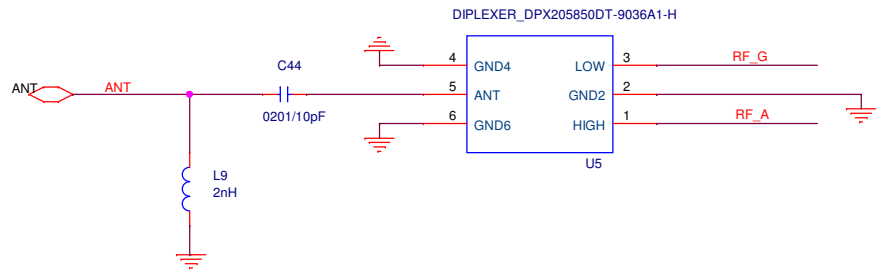
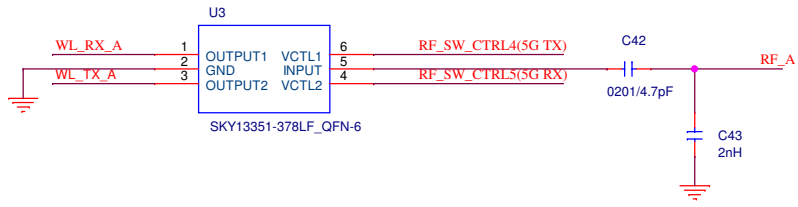


AMPAK Technology co,Ltd

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AMPAK Technology co,Ltd			
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Directory: <design name>			Rev: 00
Design: Harry	Appvd:	Now date: 106/09/05	Present date:



AMPAK Technology co,Ltd			
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Directory: <design name>		Rev: 00	
Design: Harry	Appvd:	Now date: 106/09/05	Present date: