# GOC- BA440

# Bluetooth+WIFI Module Specification

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**NOTES:**

**1.The module must use ladder steel net, and recommend ladder steel net thickness 0.16—0.20mm. The adaptability of the products is adjusted accordingly.**
**2.Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.**

# Release Record

| Version Number | Release Date | Comments |
|---|---|---|
| V1.0 | 2016/10/24 | Initial draft |
| V1.1 | 2017/01/16 | Modify pin definition and increase temperature curve |
| V1.2 | 2017/05/16 | Modify the pin |
| V1.3 | 2017/10/18 | Increase the SDIO_SET pin |
| V1.4 | 2018/01/20 | Increase the limit temperature of pass furnace |
| V1.5 | 2018/03/05 | Modify reference design and dimensions |
| V1.6 | 2018/08/21 | Refer to the design SDIO to add network logo |
| V1.7 | 2018/08/31 | Add echo cancellation reference circuit |
| V1.8 | 2018/09/26 | Update reference design |
| V1.9 | 2019/01/17 | Increase the power on time sequence |
| V2.0 | 2019/06/05 | Modification temperature |
| V2.1 | 2019/07/25 | Update reference design |
| V2.2 | 2019/08/02 | Update Bluetooth version and features |
| V2.3 | 2019/08/20 | Cancel reference design、Increase packing methods and performance parameters |

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# Contents

1. Introduction ..... 4
2. Block Diagram ..... 4
3. Features ..... 4
3.1 WIFI Features ..... 4
3.2 Bluetooth Features ..... 5
3.2.1 Bluetooth 4.0 Features ..... 6
3.2.2 Bluetooth 4.2 Features ..... 6
3.2.3 Bluetooth Low Energy ..... 6
3.2.4 Bluetooth 5.0 ..... 6
3.3Standards Compliance ..... 7
4. Specification ..... 7
5. Pin Diagram and Description ..... 8
5.1 PIN diagram ..... 8
5.2 Pin Description ..... 9
5.3 PCB Layout Footprint ..... 11
5.4 Module Package ..... 11
6. External LPO_CLK Signal Requirement ..... 12
7. Echo cancellation principle ..... 12
8. Power-Up Sequence and Timing ..... 12
8.1 Sequencing of Reset and Regulator Control Signals ..... 12
8.2 Power on sequence for WLAN ON and BT ON ..... 13
8.3 Power OFF Sequence for WLAN OFF and BT OFF ..... 13
8.4 Power On Sequence for WLAN On and BT OFF ..... 13
8.5 Power On Sequence for WLAN OFF and BT On ..... 14
9. UART Interface ..... 14
10. SDIO Pin Description ..... 15
10.1 Signal Connections to SDIO Host ..... 16
10.2 SDIO Default Mode Timing Diagram ..... 16
10.3 SDIO High Speed Mode Timing Diagram ..... 17
10.4 SDIO Bus Timing Specifications in SDR Modes ..... 17
10.5 SDIO Bus Timing Specifications in DDR50 Mode ..... 20
11. PCM Interface ..... 21
12. Electrical Feature ..... 25
12.1 Recommended Operating Rating ..... 25
12.2 Recommended Operating Conditions ..... 26
13. Recommended Reflow Profile ..... 26
14. PCB Layout Recommendation ..... 26
14.1 Antenna ..... 26
15.0 HCI UART Lines Layout Guideline ..... 26
14.3 PCM Lines Layout Guideline ..... 27
14.4 Power Trace Lines Layout Guideline ..... 27
14.5 Ground Lines Layout Guideline ..... 27
15. Module Part Number Description ..... 27
16. Ordering Information ..... 27
17. Packaging Information ..... 27
17.1 Net Weight ..... 27
17.2 Package ..... 27
17.3 Storage Requirements ..... 28
17.4 Humidity Sensitive Characteristic ..... 28

# 1. Introduction

In IEEE 802.11ac mode, the WLAN operation supports rates of MCS0–MCS9 (up to 256 QAM) in 20 MHz, 40 MHz, and 80 MHz channels for data rates of up to 433.3 Mbps. All rates specified in the IEEE 802.11a/b/g/n are supported. Included on-chip are 2.4 GHz and 5 GHz transmit amplifiers and receive low-noise amplifiers. Optional external PAs and LNAs are also supported.

The WLAN section supports the following host interface options: an SDIO v3.0 interface that can operate in 4b or 1b mode, a high-speed 4-wire UART, and a PCIe Gen1 (3.0 compliant) interface. The Bluetooth section supports a high-speed 4-wire UART interface.

Using advanced design techniques and process technology to reduce active and idle power, theGOC-BA440 is designed to address the needs of mobile devices that require minimal power consumption and compact size. It includes a power management unit which simplifies the system power topology and allows for direct operation from a mobile platform battery while maximizing battery life.

The GOC-BA440 implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. In addition, coexistence support for external radios (such as LTE cellular and GPS) is provided via an external interface. As a result, enhanced overall quality for simultaneous voice, video, and data transmission on a handheld system is achieved.

# 2. Block Diagram

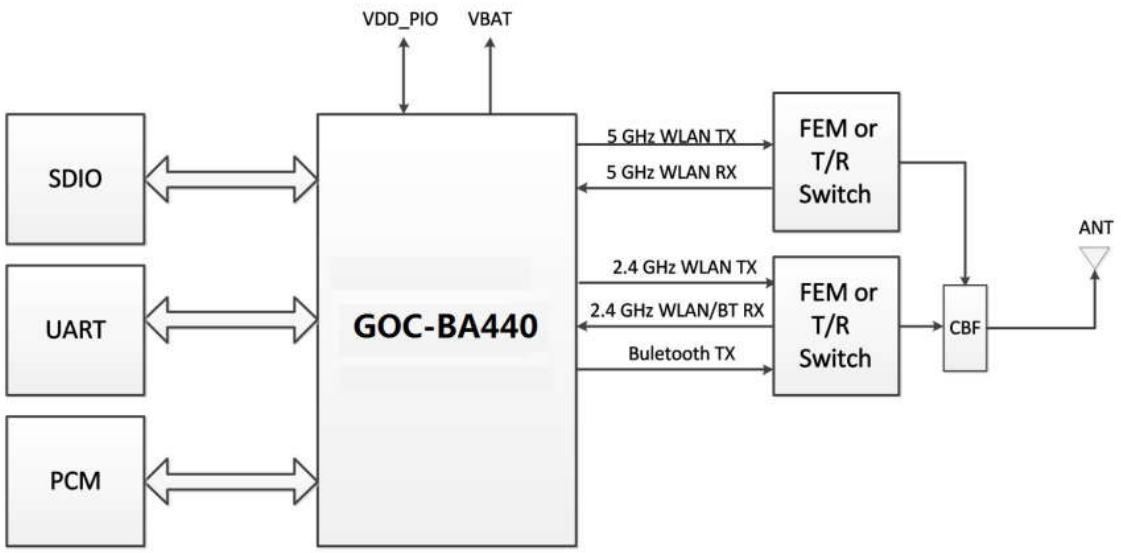


Figure 1: GOC-BA440 system Block Diagram

# 3.Features

## 3.1 WIFI Features

- IEEE 802.11ac compliant.
- Support for TurboQAM® (MCS0–MCS8 86 Mbps and MCS0–MCS9 96 Mbps) HT20, 20 MHz channel bandwidth.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI(256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- Supports explicit IEEE 802.11ac transmit beamforming.

- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Support for optional front-end modules (FEM) with external PAs and LNAs.
- Supports optional integrated T/R switch for 2.4 GHz band.
- Supports RF front-end architecture with a single dual-band antenna shared between Bluetooth and WLAN for lowest system cost.
- Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN. Internal fractional-n PLL allows support for a wide range of reference clock frequencies.
- Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE or GPS.
- Supports standard SDIO v3.0 (including DDR50 mode at 50 MHz and SDR104 mode at 208 MHz,4-bit and 1-bit) interfaces.
- Backward compatible with SDIO v2.0 host interfaces.
- PCIe mode complies with PCI Express base specification revision 3.0 compliant Gen1 interface for ×1 lane and power management base specification.
- Integrated ARMCR4 processor with tightly coupled memory for complete WLAN subsystem functionality and minimizing the need to wake-up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the ability to field upgrade with future features. On-chip memory includes 800 KB SRAM and 704 KB ROM.
- OneDriver™ software architecture for easy migration from existing embedded WLAN and Bluetooth devices as well as future devices.

## 3.2 Bluetooth Features

Primary GOC-BA440 Bluetooth features include:

- Bluetooth 5,0 complaint and qualified
- Fully supports Bluetooth Core Specification version 4.2 + EDR features:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Extended synchronous connections (eSCO)—voice connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)
  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Data packet length extension
  - Link supervision timeout (LST)
  - Secure connections
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 4.2 + HS packet types
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Cypress fast connect (TBFC)
- Narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode

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- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see Host Controller Power Management)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard sniff
  - Deep-sleep modes and software regulator shutdown
- Supports a low-power crystal, which can be used during power save mode for better timing accuracy.

### 3.2.1 Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode Bluetooth Low Energy (BT and BLE operation)
- Extended Inquiry Response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption Pause Resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure Simple Pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link Supervision Time Out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.
- Complies with Bluetooth Core Specification Version 5.0+2.1+BLE with provisions for supporting future specifications.

### 3.2.2 Bluetooth 4.2 Features

The BBC supports all Bluetooth 4.2 features, with the following benefits:

- Dual-mode classic Bluetooth and classic low energy (BT and BLE) operation
- Low-energy physical layer
- Low-energy link layer
- Enhancements to HCI for low energy
- Low-energy direct test mode
- 128 AES-CCM secure connection for both BT and BLE
- LE Data Packet Length Extension
- LE Secure Connections

Note: The CYW43455 is compatible with the Bluetooth Low Energy operating mode, which provides a dramatic reduction in the power consumption of the Bluetooth radio and baseband. The primary application for this mode is to provide support for low data rate devices, such as sensors and remote controls.

### 3.2.3 Bluetooth Low Energy

supports the Bluetooth Low Energy operating mode.

### 3.2.4 Bluetooth 5.0

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GOC-BA440 is qualified for and supports the mandatory features of the Bluetooth 5.0 specification.

### 3.3Standards Compliance

TheGOC-BA440 supports the following standards:

- Bluetooth 2.1 + EDR
- Bluetooth 3.0
- Bluetooth 4.2 (Bluetooth Low Energy)
- Bluetooth 5.0 compliant
- IEEE 802.11ac single-stream mandatory and optional requirements for 20, 40, and 80 MHz channels
- IEEE 802.11n (Handheld Device Class, Section 11)
- IEEE 802.11a
- IEEE 802.11b
- IEEE 802.11g
- IEEE 802.11d
- IEEE 802.11h
- IEEE 802.11i
- Security:
  - WEP
  - WPA Personal
  - WPA2 Personal
  - WMM
  - WMM-PS (U-APSD)
  - WMM-SA
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
  - CKIP (software support)
- Proprietary protocols:
  - CCXv2
  - CCXv3
  - CCXv4
  - CCXv5
  - WFAEC
- IEEE 802.15.2 Coexistence Compliance (on-silicon solution compliant with IEEE 3-wire requirements)

The GOC-BA440 supports the following future drafts/standards:

- IEEE 802.11r (fast roaming between APs)
- IEEE 802.11w (secure management frames)
- IEEE 802.11 Extensions:
  - IEEE 802.11e QoS Enhancements (as per the WMM specification is already supported)
  - IEEE 802.11h 5 GHz Extensions
  - IEEE 802.11i MAC Enhancements
  - IEEE 802.11k Radio Resource Measurement

## 4.Specification

| Feature | Description |
|---|---|
| Model Name | GOC-BA440 |
| Bluetooth | |

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| | |
|---|---|
| Bluetooth Standard | Bluetooth V5.0+2.1+BLE |
| Frequency Band | 2402MHz~2480MHz |
| Interface | UART/PCM/I2S |
| WIFI | |
| Frequency Band | 2.4GHz/5GHz |
| Interface | SDIO2.0/SDIO3.0 |
| Size | 17mm*17mm*2.0mm |
| Operating Temperature | -30℃~+85℃ |
| Storage Temperature | -40℃~+125℃ |
| VBAT | 3.3V |
| VDD_PIO | 1.8V~3.3V |
| Standby current | 25mA |
| Working current | 350mA |
| Max current | <700mA |
| Humidity | Operating Humidity 60% to 85% Non-Condensing |

Table 1: Specifications

# 5. Pin Diagram and Description

## 5.1 PIN diagram

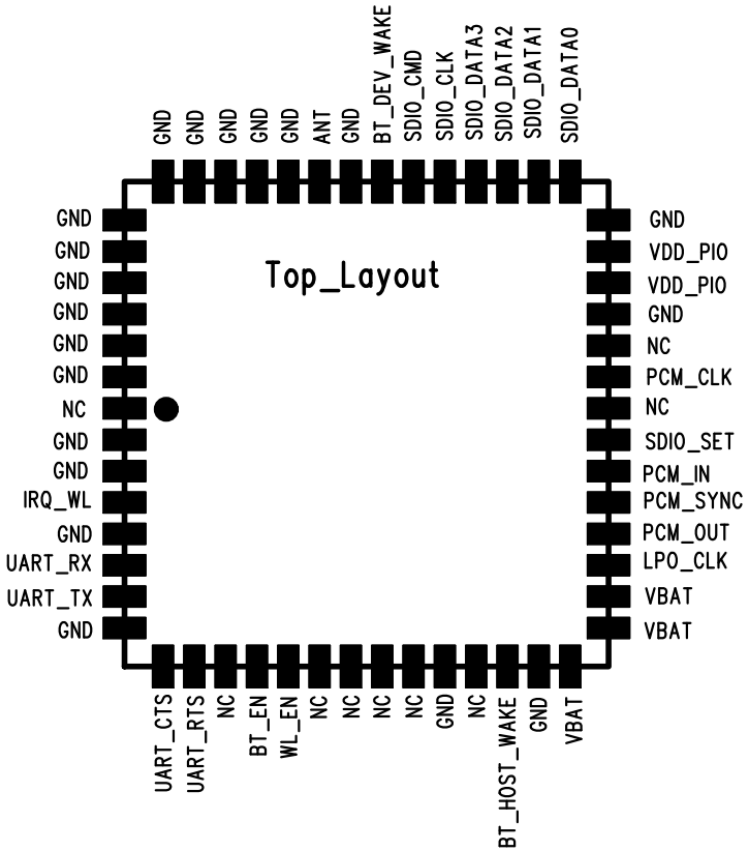


Figure2: GOC-BA440 pin

## 5.2 Pin Description

| Pin | Pin Name | **Type** | Description |
|---|---|---|---|
| 1 | NC | NC | NC |
| 2 | GND | Ground | Ground |
| 3 | GND | Ground | Ground |
| 4 | IRQ_WL | - | SDIO available, interrupt out. |
| 5 | GND | Ground | Ground |
| 6 | UART_RX | Input | BT UART Data Input |
| 7 | UART_TX | Output | BT UART Data Output |
| 8 | GND | Ground | Ground |
| 9 | UART_CTS | Input | UART CTS |
| 10 | UART_RTS | Output | UART RTS |
| 11 | NC | NC | NC |
| 12 | BT_EN | Input | BT enable high |
| 13 | WL_EN | Input | WL enable high |
| 14 | NC | NC | NC |
| 15 | NC | NC | NC |
| 16 | NC | NC | NC |
| 17 | NC | NC | NC |
| 18 | GND | Ground | Ground |
| 19 | NC | NC | NC |
| 20 | BT_HOST_WAKE | Input/Output | Bluetooth device to wake-up HOST(Reserved) |
| 21 | GND | Ground | Ground |
| 22 | VBAT | POWER | 3.3V Supply Voltage |
| 23 | VBAT | POWER | 3.3V Supply Voltage |
| 24 | VBAT | POWER | 3.3V Supply Voltage |
| 25 | LPO_CLK | Input | Slow clock. 32.768k |
| 26 | PCM_OUT | Output | PCM data Out |
| 27 | PCM_SYNC | Input/Output | PCM Synchronization control |
| 28 | PCM_IN | Input | PCM data Input |
| 29 | SDIO_SET | Input | SDIO mode selection pin |
| 30 | NC | NC | NC |
| 31 | PCM_CLK | Input/Output | PCM Clock |

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| | | | |
|---|---|---|---|
| 32 | NC | NC | NC |
| 33 | GND | Ground | Ground |
| 34 | VDD_PIO | POWER | 1.8V~3.3VSupply Voltage |
| 35 | VDD_PIO | POWER | 1.8V~3.3V Supply Voltage |
| 36 | GND | Ground | Ground |
| 37 | SDIO_DATA0 | Input/Output | SDIO Data Line 0 |
| 38 | SDIO_DATA1 | Input/Output | SDIO Data Line1 |
| 39 | SDIO_DATA2 | Input/Output | SDIO Data Line 2 |
| 40 | SDIO_DATA3 | Input/Output | SDIO Data Line 3 |
| 41 | SDIO_CLK | Input | SDIO Clock Input |
| 42 | SDIO_CMD | Input/Output | SDIO Command |
| 43 | BT_DEV_WAKE | Input/Output | HOST wake-up Bluetooth device(Reserved) |
| 44 | GND | Ground | Ground |
| 45 | ANT | RF | WLAN(2.4G/5G)Antenna(Reserved) |
| 46 | GND | Ground | Ground |
| 47 | GND | Ground | Ground |
| 48 | GND | Ground | Ground |
| 49 | GND | Ground | Ground |
| 50 | GND | Ground | Ground |
| 51 | GND | Ground | Ground |
| 52 | GND | Ground | Ground |
| 53 | GND | Ground | Ground |
| 54 | GND | Ground | Ground |
| 55 | GND | Ground | Ground |
| 56 | GND | Ground | Ground |

Table2:Pin Description

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## 5.3 PCB Layout Footprint

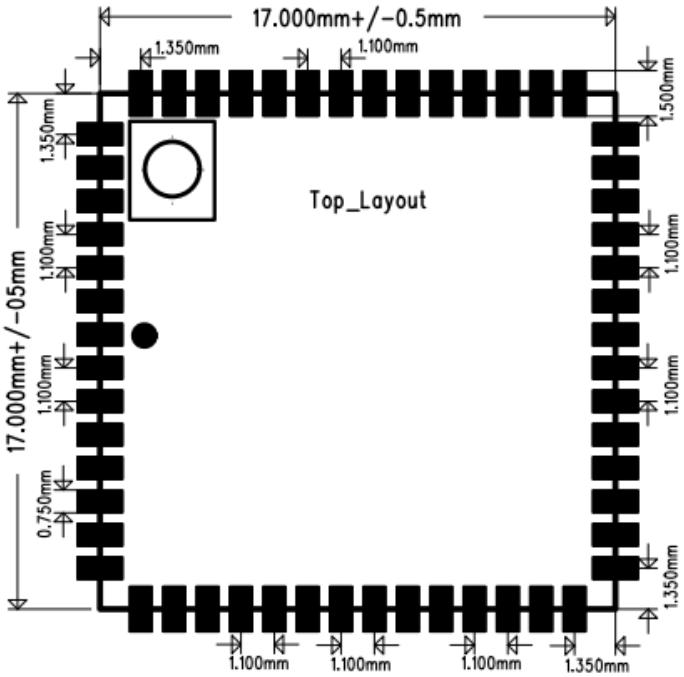



Figure3:PCB Layout Footprint

## 5.4 Module Package

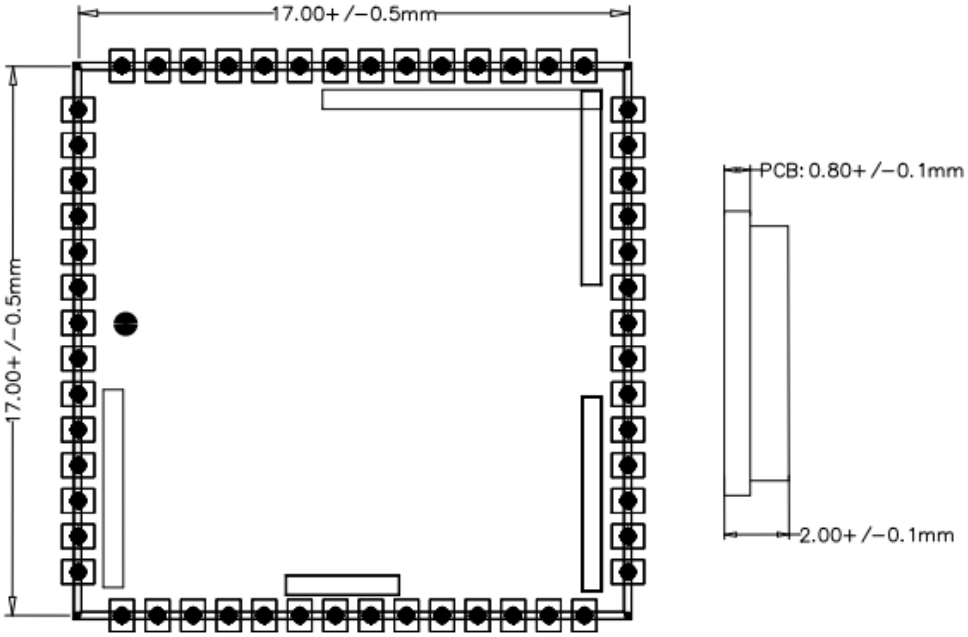



Figure4:Module Package

# 6. External LPO_CLK Signal Requirement

| Parameter | LPO Clock | Units |
|---|---|---|
| Nominal input frequency | 32.768 | kHz |
| Frequency accuracy | ±200 | ppm |
| Duty cycle | 30–70 | % |
| Input signal amplitude | 200–3300 | mV, p-p |
| Signal type | Square wave or sine wave | – |
| Input impedancel[a] | >100k | Ω |
| | <5 | pF |
| Clock jitter | <10,000 | ppm |

a:When power is applied or switched off.

Table 3: External LPO_CLK Signal Requirement

# 7.Echo cancellation principle

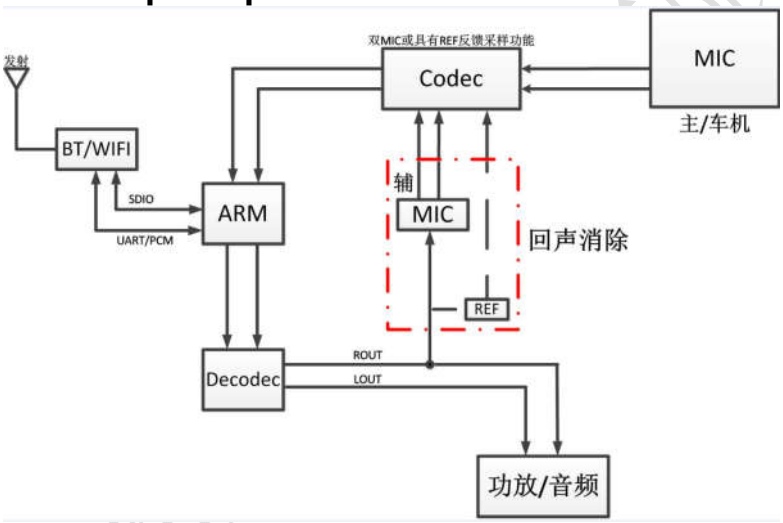



Figure5: Sound processing flow chart

The left picture is a schematic diagram of the echo cancellation principle. After Decodec decoding of the left and right channel sound, after data sampling and master MIC data comparison, echo cancellation can be processed. The right picture is a reference example, which can be designed according to the actual plan. Flying echo cancellation design, priority to use the echo cancellation design of IFLYTEK.

# 8.Power-Up Sequence and Timing

## 8.1 Sequencing of Reset and Regulator Control Signals

The GOC-BA440 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

NOTE:

1)The module has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating PCIe accesses.

2)VBAT should not rise 10% – 90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## 8.2 Power on sequence for WLAN ON and BT ON

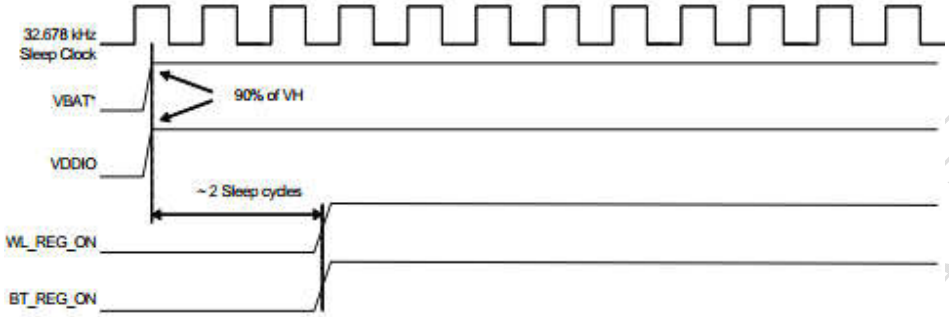



Figure 6: WLAN = ON, Bluetooth = ON

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## 8.3 Power OFF Sequence for WLAN OFF and BT OFF

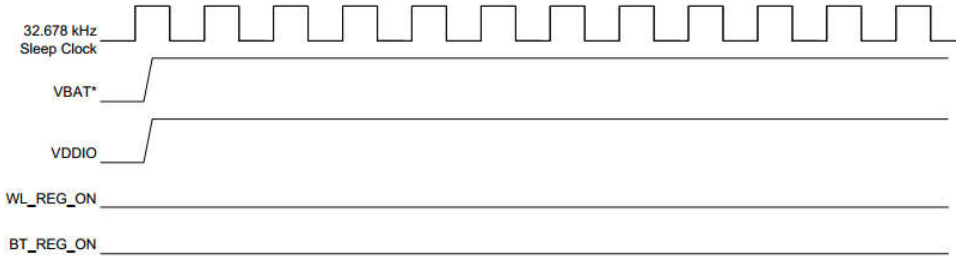



Figure 7: WLAN = OFF, Bluetooth = OFF

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## 8.4 Power On Sequence for WLAN On and BT OFF

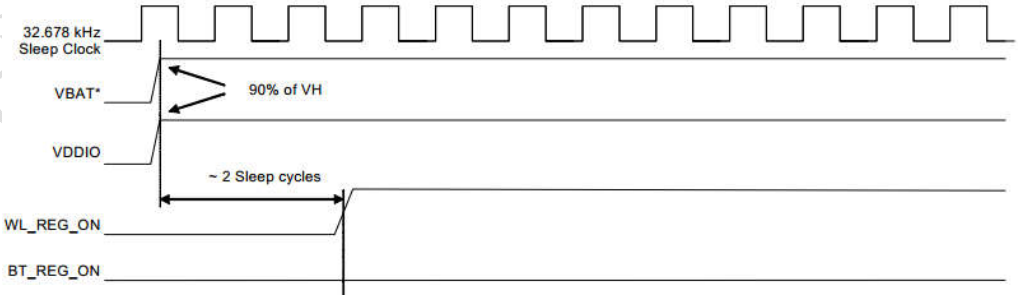



Figure 8: WLAN = ON, Bluetooth = OFF

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

### 8.5 Power On Sequence for WLAN OFF and BT On

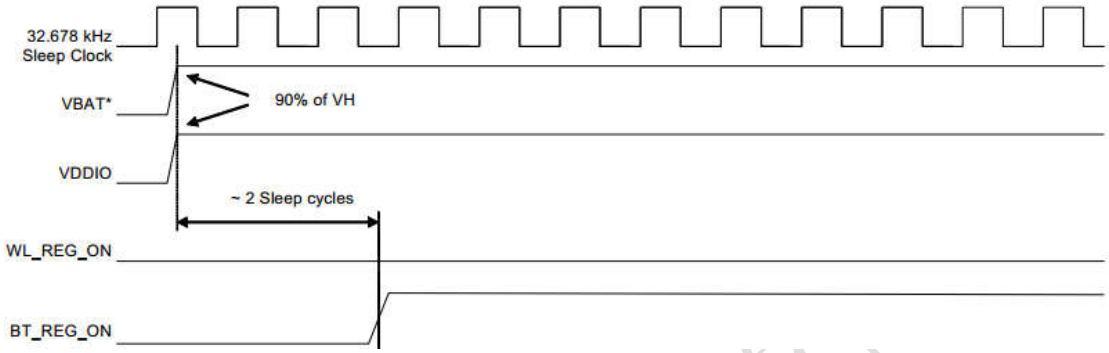



Figure 9: WLAN = OFF, Bluetooth = ON

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

## 9. UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

The GOC-BA440 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The GOC-BA440 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

| Desired Rate | Actual Rate | Error (%) |
|---|---|---|
| 4000000 | 4000000 | 0.00 |
| 3692000 | 3692308 | 0.01 |
| 3000000 | 3000000 | 0.00 |
| 2000000 | 2000000 | 0.00 |
| 1500000 | 1500000 | 0.00 |
| 1444444 | 1454544 | 0.70 |
| 921600 | 923077 | 0.16 |
| 460800 | 461538 | 0.16 |
| 230400 | 230796 | 0.17 |
| 115200 | 115385 | 0.16 |
| 57600 | 57692 | 0.16 |
| 38400 | 38400 | 0.00 |
| 28800 | 28846 | 0.16 |
| 19200 | 19200 | 0.00 |
| 14400 | 14423 | 0.16 |
| 9600 | 9600 | 0.00 |

Table4: Example of Common Baud Rates

## 10.SDIO Pin Description

All three package options of the WLAN section provide support for SDIO version 3.0 including the new UHS-I modes:

- DS: Default speed up to 25MHz (3.3V signaling).
- HS: High speed up to 50MH (1.8V signaling).
- SDR12: SDR up to 25MHz (1.8V signaling).
- SDR25: SDR up to 50MHz (1.8V signaling).
- SDR50: SDR up to 100MHz (1.8V signaling).
- SDR104: SDR up to 208MHz (1.8V signaling).
- DDR50: DDR up to 50MHz (1.8V signaling).

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by SDIO interface. The ability to force control of gated clocks from within the device is also provided.

The following three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B) .

SDIO Pin Description:

| SD 4-Bit Mode | |
|---|---|
| DATA0 | Data Line 0 |
| DATA1 | Data Line 1 or interrupt |
| DATA2 | Data Line 2 or Read Wait |
| DATA3 | Data Line 3 |
| CLK | Clock |
| CMD | Command Line |

## 10.1 Signal Connections to SDIO Host

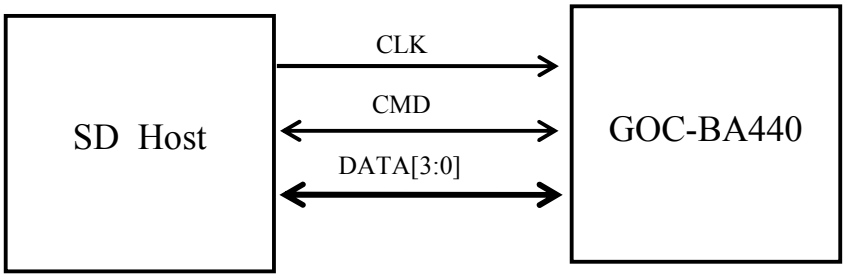
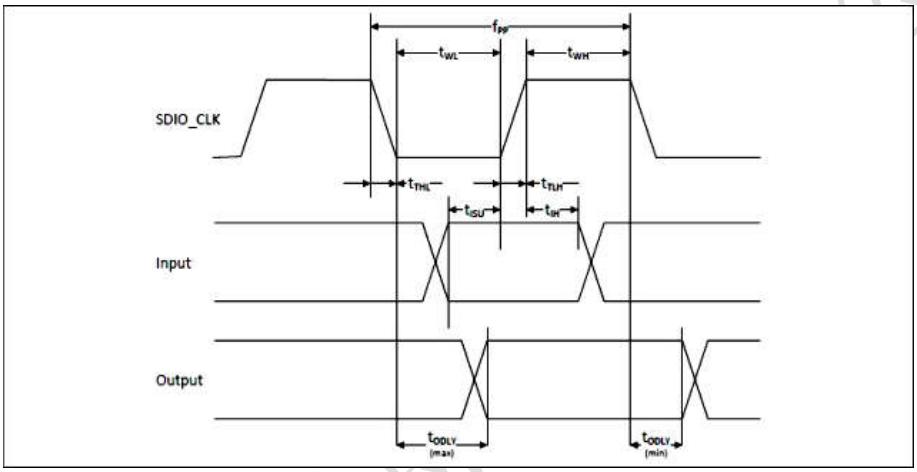



Figure 10: Signal Connections to SDIO Host

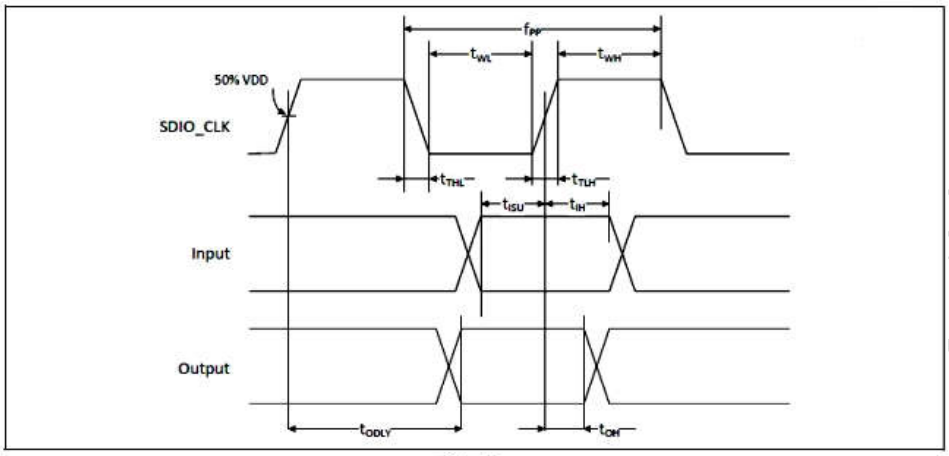
## 10.2SDIO Default Mode Timing Diagram




| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| ***SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])*** | | | | | |
| Frequency – Data Transfer mode | fPP | 0 | – | 25 | MHz |
| Frequency – Identification mode | fOD | 0 | – | 400 | kHz |
| Clock low time | tWL | 10 | – | – | ns |
| Clock high time | tWH | 10 | – | – | ns |
| Clock rise time | tTLH | – | – | 10 | ns |
| Clock low time | tTHL | – | – | 10 | ns |
| ***Inputs: CMD, DAT (referenced to CLK)*** | | | | | |
| Input setup time | tISU | 5 | – | – | ns |
| Input hold time | tIH | 5 | – | – | ns |
| ***Outputs: CMD, DAT (referenced to CLK)*** | | | | | |
| Output delay time – Data Transfer mode | tODLY | 0 | – | 14 | ns |
| Output delay time – Identification mode | tODLY | 0 | – | 50 | ns |

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

## 10.3 SDIO High Speed Mode Timing Diagram

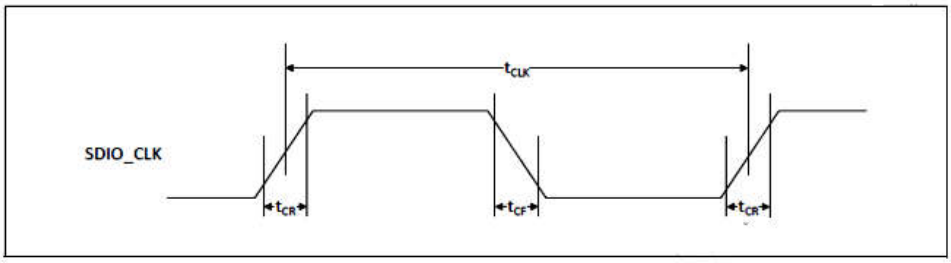



| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| ***SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])*** | | | | | |
| Frequency – Data Transfer Mode | fPP | 0 | – | 50 | MHz |
| Frequency – Identification Mode | fOD | 0 | – | 400 | kHz |
| Clock low time | tWL | 7 | – | – | ns |
| Clock high time | tWH | 7 | – | – | ns |
| Clock rise time | tTLH | – | – | 3 | ns |
| Clock low time | tTHL | – | – | 3 | ns |
| ***Inputs: CMD, DAT (referenced to CLK)*** | | | | | |
| Input setup Time | tISU | 6 | – | – | ns |
| Input hold Time | tIH | 2 | – | – | ns |
| ***Outputs: CMD, DAT (referenced to CLK)*** | | | | | |
| Output delay time – Data Transfer Mode | tODLY | – | – | 14 | ns |
| Output hold time | tOH | 2.5 | – | – | ns |
| Total system capacitance (each line) | CL | – | – | 40 | pF |

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

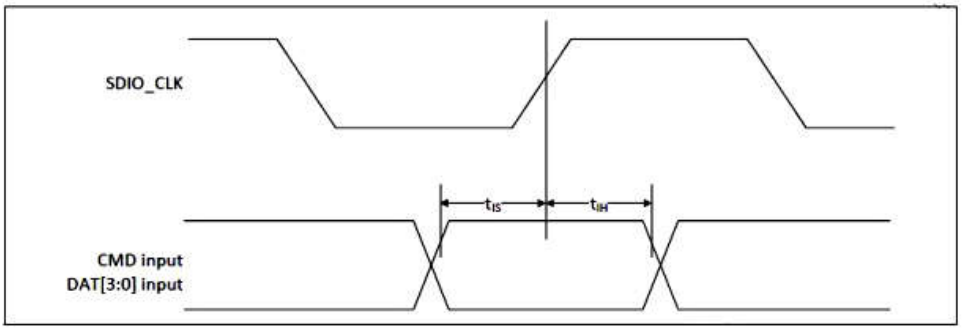
## 10.4 SDIO Bus Timing Specifications in SDR Modes

**Clock timing (SDR Modes)**



| Parameter | Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|---|
| – | $t_{CLK}$ | 40 | – | ns | SDR12 mode |
| | | 20 | – | ns | SDR25 mode |
| | | 10 | – | ns | SDR50 mode |
| | | 4.8 | – | ns | SDR104 mode |
| – | $t_{CR}$, $t_{CF}$ | – | $0.2 \times t_{CLK}$ | ns | $t_{CR}$, $t_{CF}$ < 2.00 ns (max) @100 MHz, $C_{CARD}$ = 10 pF<br>$t_{CR}$, $t_{CF}$ < 0.96 ns (max) @208 MHz, $C_{CARD}$ = 10 pF |
| Clock duty | – | 30 | 70 | % | – |

**Card Input timing (SDR Modes)**




| Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|
| ***SDR104 Mode*** | | | | |
| $t_{IS}$ | 1.70[a] | – | ns | $C_{CARD}$ = 10 pF, VCT = 0.975V |
| $t_{IH}$ | 0.80 | – | ns | $C_{CARD}$ = 5 pF, VCT = 0.975V |
| ***SDR50 Mode*** | | | | |
| $t_{IS}$ | 3.00 | – | ns | $C_{CARD}$ = 10 pF, VCT = 0.975V |
| $t_{IH}$ | 0.80 | – | ns | $C_{CARD}$ = 5 pF, VCT = 0.975V |

a. SDIO 3.0 specification value is 1.40 ns.

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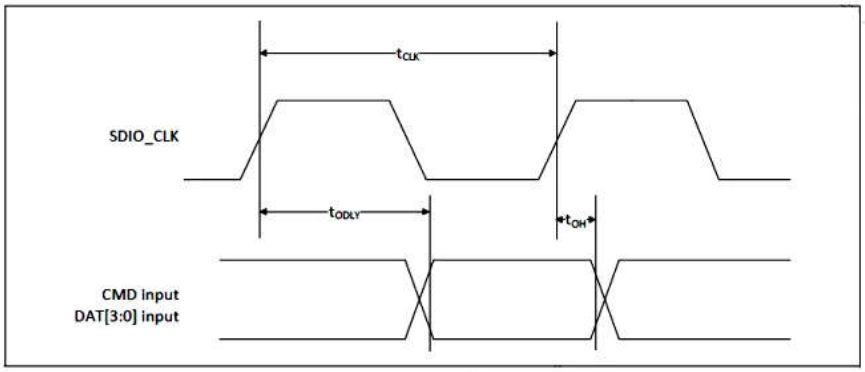
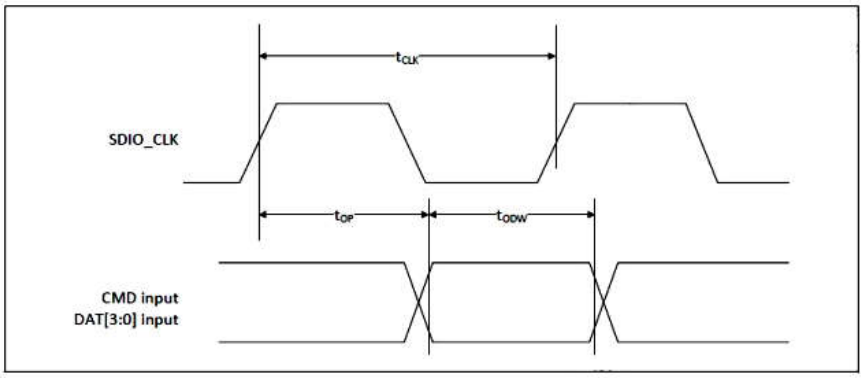
**Card output timing (SDR Modes up to 100MHz)**




| Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|
| $t_{ODLY}$ | – | 7.85[a] | ns | $t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50 |
| $t_{ODLY}$ | – | 14.0 | ns | $t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25 |
| $t_{OH}$ | 1.5 | – | ns | Hold time at the $t_{ODLY}$ (min) $C_L = 15$ pF |

a. SDIO 3.0 specification value is 7.5 ns.

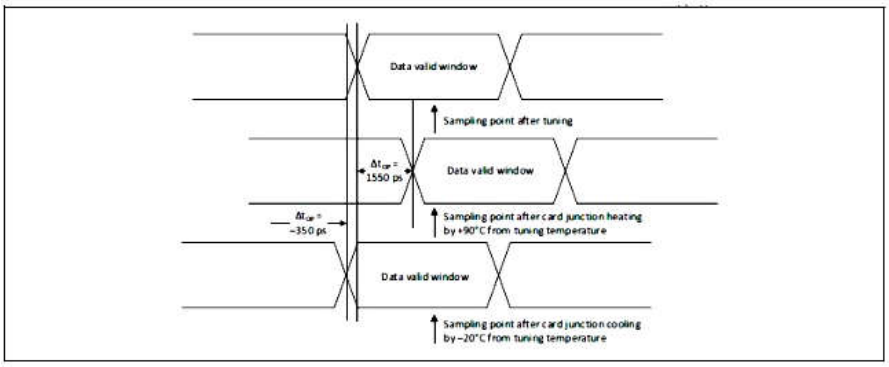
**Card output timing (SDR Modes 100MHz to 208MHz)**



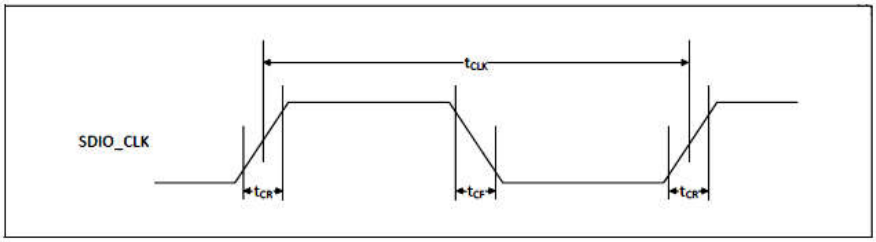

| Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|
| $t_{OP}$ | 0 | 2 | UI | Card output phase |
| $\Delta t_{OP}$ | −350 | +1550 | ps | Delay variation due to temp change after tuning |
| $t_{ODW}$ | 0.60 | – | UI | $t_{ODW}$=2.88 ns @208 MHz |

- $\Delta t_{OP}$ = +1550 ps for junction temperature of $\Delta t_{OP}$ = 90 degrees during operation
- $\Delta t_{OP}$ = −350 ps for junction temperature of $\Delta t_{OP}$ = −20 degrees during operation
- $\Delta t_{OP}$ = +2600 ps for junction temperature of $\Delta t_{OP}$ = −20 to +125 degrees during operation

**Δ*tOP* Consideration for Variable Data Window (SDR 104 Mode)**

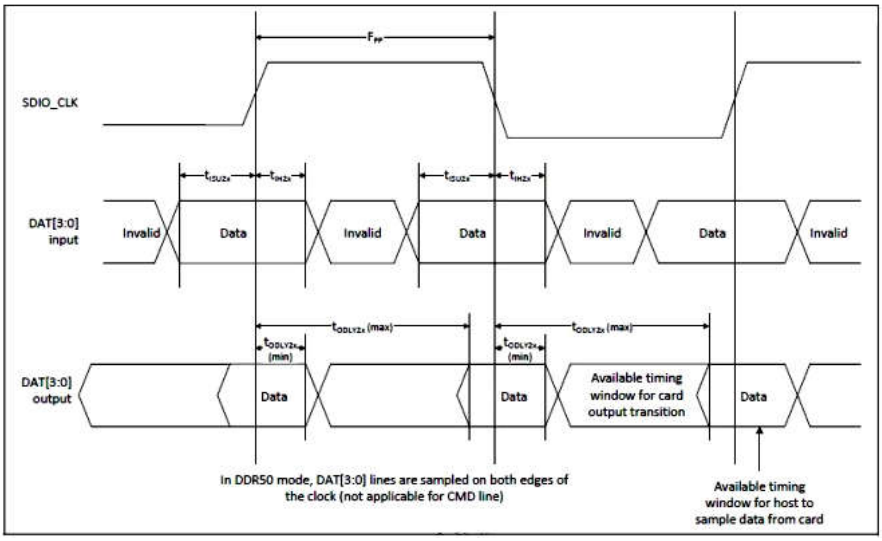



## 10.5SDIO Bus Timing Specifications in DDR50 Mode




| *Parameter* | *Symbol* | *Minimum* | *Maximum* | *Unit* | *Comments* |
|---|---|---|---|---|---|
| – | $t_{CLK}$ | 20 | – | ns | DDR50 mode |
| – | $t_{CR}$,$t_{CF}$ | – | 0.2 × tCLK | ns | $t_{CR}$, $t_{CF}$ < 4.00 ns (max) @50 MHz, $C_{CARD}$ = 10 pF |
| Clock duty | – | 45 | 55 | % | – |

**Data Timing**



| Parameter | Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|---|
| ***Input CMD*** | | | | | |
| Input setup time | $t_{ISU}$ | 6 | – | ns | $C_{CARD}$ < 10pF (1 Card) |
| Input hold time | $t_{IH}$ | 0.8 | – | ns | $C_{CARD}$ < 10pF (1 Card) |
| ***Output CMD*** | | | | | |
| Output delay time | $t_{ODLY}$ | – | 13.7 | ns | $C_{CARD}$ < 30pF (1 Card) |
| Output hold time | $t_{OH}$ | 1.5 | – | ns | $C_{CARD}$ < 15pF (1 Card) |
| ***Input DAT*** | | | | | |
| Input setup time | $t_{ISU2x}$ | 3 | – | ns | $C_{CARD}$ < 10pF (1 Card) |
| Input hold time | $t_{IH2x}$ | 0.8 | – | ns | $C_{CARD}$ < 10pF (1 Card) |
| ***Output DAT*** | | | | | |
| Output delay time | $t_{ODLY2x}$ | – | 7.85[a] | ns | $C_{CARD}$ < 25pF (1 Card) |
| Output hold time | $t_{ODLY2x}$ | 1.5 | – | ns | $C_{CARD}$ < 15pF (1 Card) |

a. SDIO 3.0 specification value is 7.0 ns.

# 11. PCM Interface

The PCM Interface on the GOC-BA440 can connect to linear PCM Codec devices in master or slave mode. In master mode,the GOC-BA440 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the GOC-BA440.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

## Slot Mapping

The GOC-BA440 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

## Frame Synchronization

The GOC-BA440 supports both short- and long-frame synchronization in both master and slave modes. In shortframe synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

## Data Formatting

The GOC-BA440 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the GOC-BA440 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2’s complement data, left justified, and clocked MSB first.

## PCM Interface Timing

### Short Frame Sync, Master Mode

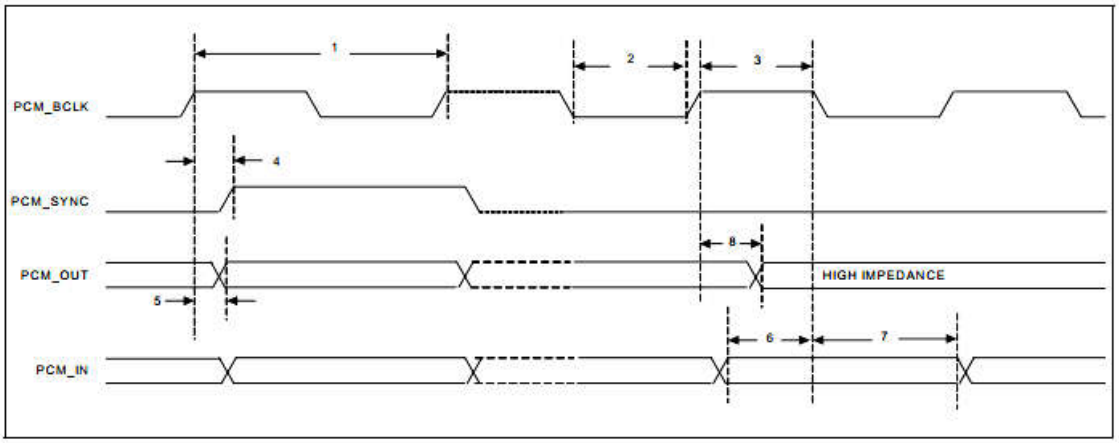



Figure 11: PCM Timing Diagram (Short Frame Sync, Master Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | - | - | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | - | - | ns |
| 3 | PCM bit clock HIGH | 41 | - | - | ns |
| 4 | PCM_SYNC delay | 0 | - | 25 | ns |
| 5 | PCM_OUT delay | 0 | - | 25 | ns |
| 6 | PCM_IN setup | 8 | - | - | ns |
| 7 | PCM_IN hold | 8 | - | - | ns |
| 8 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | - | 25 | ns |

Table4:PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

### Short Frame Sync, Slave Mode

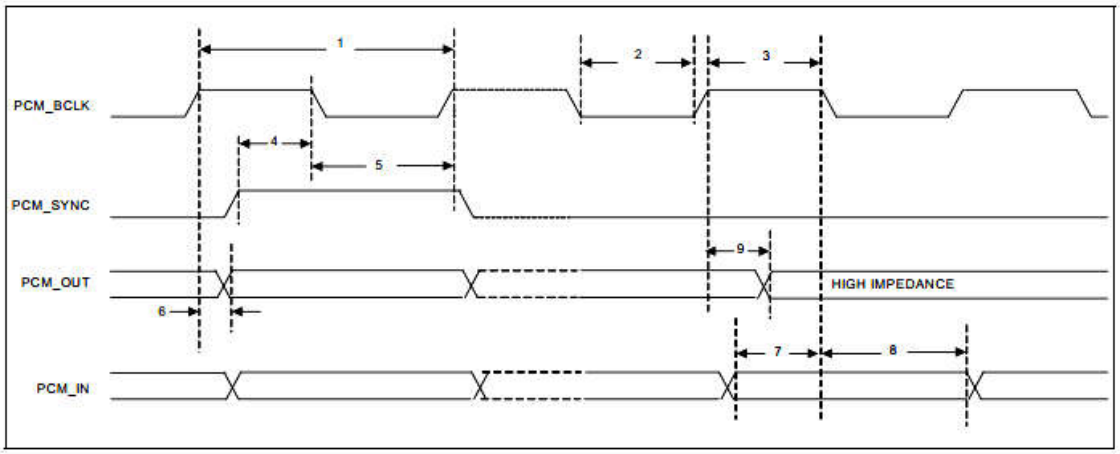



Figure12: PCM Timing Diagram (Short Frame Sync, Slave Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | - | - | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | - | - | ns |
| 3 | PCM bit clock HIGH | 41 | - | - | ns |
| 4 | PCM_SYNC setup | 8 | - | - | ns |
| 5 | PCM_SYNC hold | 8 | - | - | ns |
| 6 | PCM_OUT delay | 0 | - | 25 | ns |
| 7 | PCM_IN setup | 8 | - | - | ns |
| 8 | PCM_IN hold | 8 | - | - | ns |
| 9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | - | 25 | ns |

Table 5: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

### Long Frame Sync, Master Mode

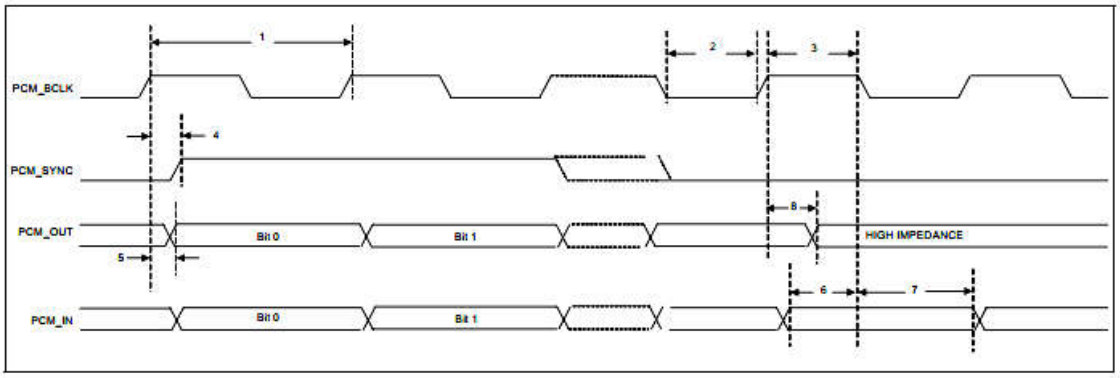



Figure 13: PCM Timing Diagram (Long Frame Sync, Master Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | - | - | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | - | - | ns |
| 3 | PCM bit clock HIGH | 41 | - | - | ns |
| 4 | PCM_SYNC delay | 0 | - | 25 | ns |
| 5 | PCM_OUT delay | 0 | - | 25 | ns |
| 6 | PCM_IN setup | 8 | - | - | ns |
| 7 | PCM_IN hold | 8 | - | - | ns |
| 8 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | - | 25 | ns |

Table 6: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

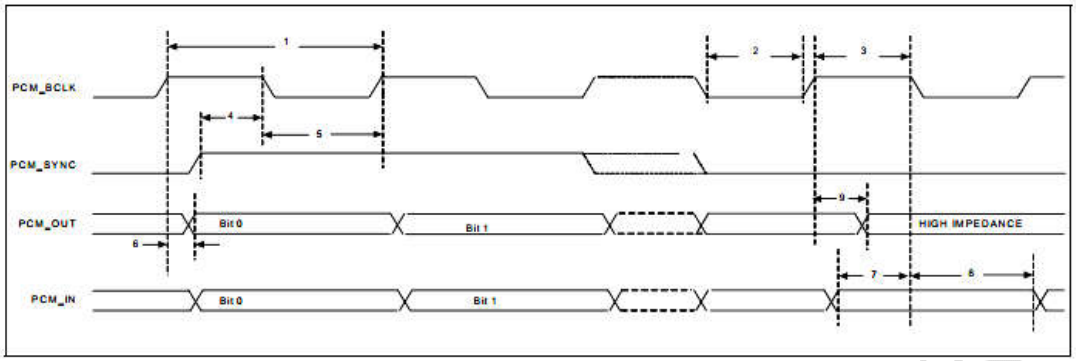



Figure 14: PCM Timing Diagram (Long Frame Sync, Slave Mode)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | - | - | 12 | MHz |
| 2 | PCM bit clock LOW | 41 | - | - | ns |
| 3 | PCM bit clock HIGH | 41 | - | - | ns |
| 4 | PCM_SYNC setup | 8 | - | - | ns |
| 5 | PCM_SYNC hold | 8 | - | - | ns |
| 6 | PCM_OUT delay | 0 | - | 25 | ns |
| 7 | PCM_IN setup | 8 | - | - | ns |
| 8 | PCM_IN hold | 8 | - | - | ns |
| 9 | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0 | - | 25 | ns |

Table 7: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

### Short Frame Sync, Burst Mode

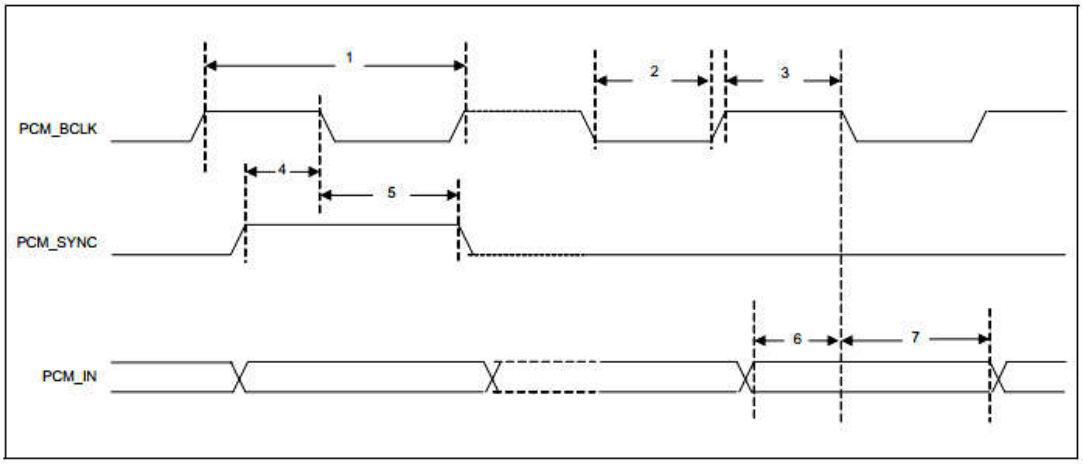



Figure 15: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | - | - | 24 | MHz |
| 2 | PCM bit clock LOW | 20.8 | - | - | ns |
| 3 | PCM bit clock HIGH | 20.8 | - | - | ns |
| 4 | PCM_SYNC setup | 8 | - | - | ns |
| 5 | PCM_SYNC hold | 8 | - | - | ns |
| 6 | PCM_OUT delay | 8 | - | - | ns |
| 7 | PCM_IN setup | 8 | - | - | ns |
| 8 | PCM_IN hold | 8 | - | - | ns |

Table 8: PCM Burst Mode (Receive Only, Short Frame Sync)

### Long Frame Sync, Burst Mode

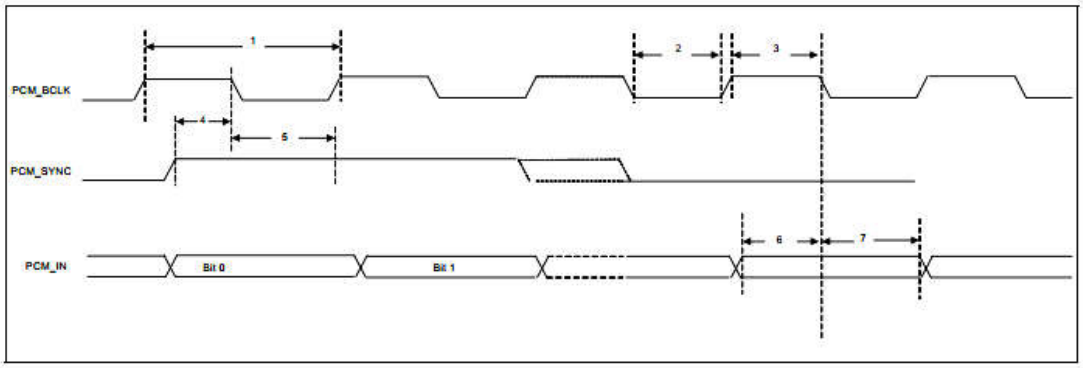



Figure 16: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

| Reference | Characteristics | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| 1 | PCM bit clock frequency | - | - | 24 | MHz |
| 2 | PCM bit clock LOW | 20.8 | - | - | ns |
| 3 | PCM bit clock HIGH | 20.8 | - | - | ns |
| 4 | PCM_SYNC setup | 8 | - | - | ns |
| 5 | PCM_SYNC hold | 8 | - | - | ns |
| 6 | PCM_OUT delay | 8 | - | - | ns |
| 7 | PCM_IN setup | 8 | - | - | ns |
| 8 | PCM_IN hold | 8 | - | - | ns |

Table 9: PCM Burst Mode (Receive Only, Long Frame Sync)

# 12.Electrical Feature

## 12.1 Recommended Operating Rating

| Rated Level | Min | Typical | Max |
|---|---|---|---|
| VBAT | 3.0V | 3.3V | 4.8V |
| VDD_PIO | 1.71V | 1.8V | 1.89V |
| | 3.16V | 3.3V | 3.46V |

Table 10: Recommended Operating Rating

### 12.2 Recommended Operating Conditions

| Operating Conditions | Min | Typical | Max |
|---|---|---|---|
| Operating Temperature | -30°C | / | +85°C |
| Storage Temperature | -40°C | / | +125°C |

*The module is functional across this range of voltages. However, optimal RF performance specified in the data sheet is guaranteed only for 3.2V <VBAT < 4.8V and -30°C to +75°C.

Table 11: Recommended Operating Conditions

## 13.Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ≦260℃ 10s

Number of Times : 2 times

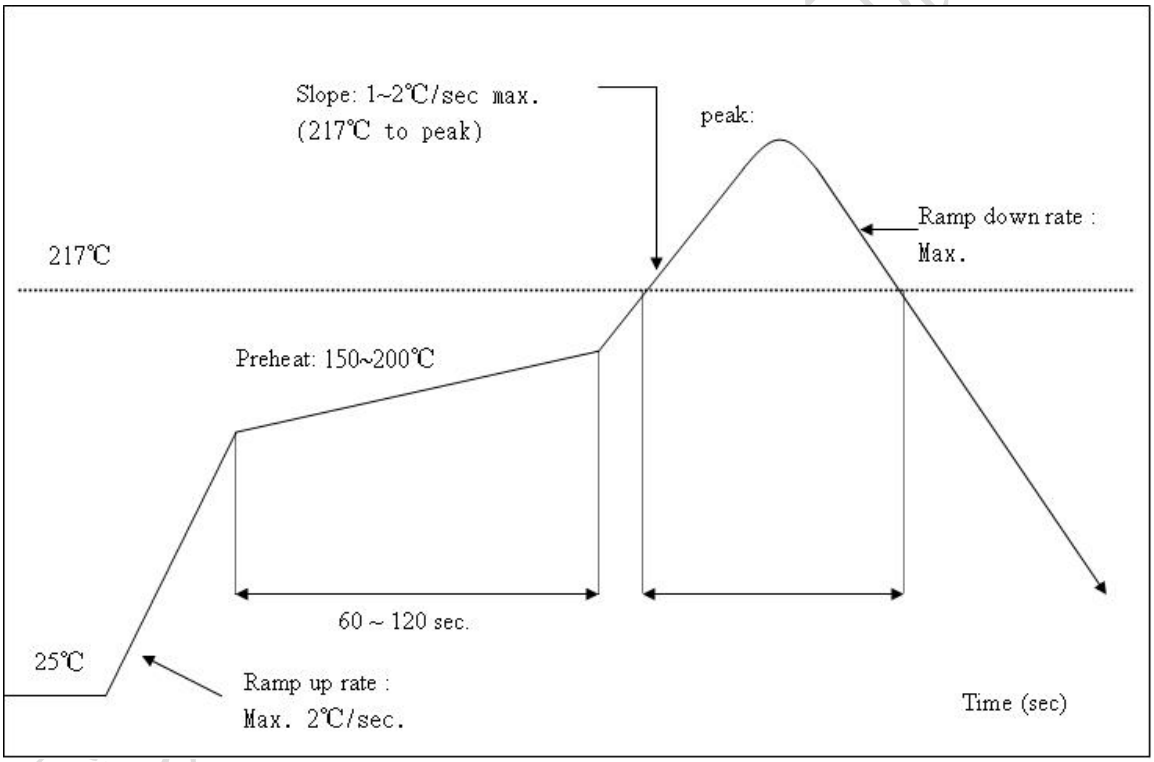



Figure17: Solder Reflow Profile

## 14.PCB Layout Recommendation

### 14.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above (or under) the RF antenna trace should be free from other traces.

### 15.0 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as

these lines drive 4 ~ 8mA.
UART_RX UART_TX UART_CTS UART_RTS
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

### 14.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA.
PCM_SYNC PCM_CLK PCM_OUT PCM_IN
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

### 14.4 Power Trace Lines Layout Guideline

VBAT Trace Width: 30mil
VDD_PIO Trace Width: 25mil

### 14.5 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.
Add Ground Through Holes to GOC-BA440 Module Ground Pads.
Decoupling Capacitors close to GOC-BA440 Module Power and Ground Pads.

## 15. Module Part Number Description

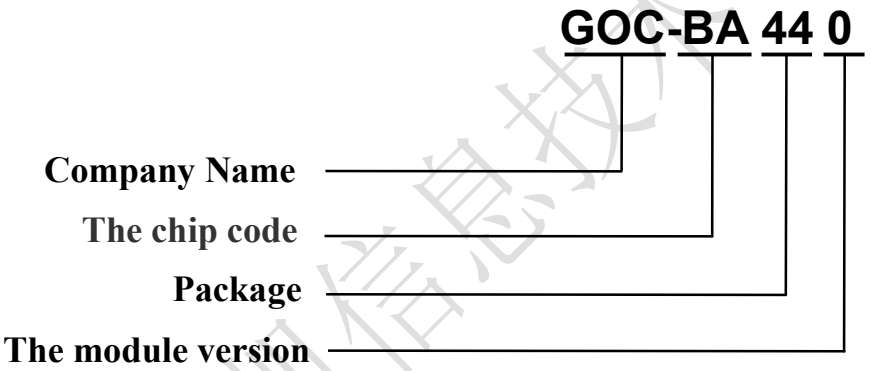



Figure18: Ordering information

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to *www.goodocom.com* or contact the GOODOCOM Sales Office nearest to you.

## 16. Ordering Information

| Part Number | Description | Remark |
|---|---|---|
| GOC-BA440 | Dual-band 2.4 GHz and 5 GHz<br>WLAN+ BT 5.0 + FMRX | |

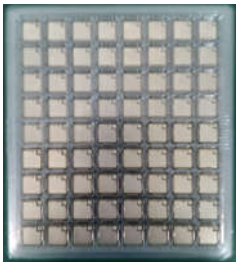
Table 12: Ordering information

## 17. Packaging Information

### 17.1 Net Weight

The module net weight: 1.3g±0.1g

### 17.2 Package



72pcs module in one tray 2000pcs modules into one pack 4000pcs

Modules One Box Carton size:270mm*275mm*220mm

Tray size:225mm*205mm*7mm

## 17.3 Storage Requirements

1）Temperature: 22~28°C；

2 ）Humidity: <70%（ RH）；

Vacuum packed and sealed in good condition to ensure 12 months of welding.

## 17.4 Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28°C and humidity<60%(RH).

3） Handling, storage, and processing should follow IPC/JEDECJ-STD-033

**Federal Communication Commission Statement (FCC, U.S.)**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

**FCC Caution:**
Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

**IMPORTANT NOTES**

**Co-location warning:**
This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

**OEM integration instructions:**
This device is intended only for OEM integrators under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the external antenna(s) that has been originally tested and certified with this module.

As long as the conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**Validity of using the module certification:**
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

**End product labeling:**
The final end product must be labeled in a visible area with the following: “Contains Transmitter Module FCC ID: 2AWOC-GOC-BA440”.

**Information that must be placed in the end user manual:**
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

**Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01**

**2.2 List of applicable FCC rules**
FCC Part 15 Subpart C 15.247 & 15.207 & 15.209

**2.3 Specific operational use conditions**
The module is a module with WIFI 2.4G function and WiFi 5G function
and BT function
Operation Frequency:
BT/BLE: 2402-2480MHz
2.4GWiFi：2412~2462MHz
5GWiFi：
U-NII-1: 5150 MHz to 5250 MHz,
U-NII-3: 5725 MHz to 5850 MHz
Type: PCB Antenna
Gain: 2.5dBi Max.
The module can be used for mobile or applications with a maximum 2.5dBi antenna. The host manufacturer installing this module into their product must ensure that the final composit product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operaition. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

**2.4 Limited module procedures**
Not applicable. The module is a Single module and complies with the requirement of FCC Part 15.212.

**2.5 Trace antenna designs**
Not applicable. The module has its own antenna, and doesn’t need a host’s printed board microstrip trace antenna etc.

**2.6 RF exposure considerations**
The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users’ body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application. The FCC ID of the module cannot be used on the final product. In these circumstances, the host manufacturer will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization

**2.7 Antennas**
Antenna Specification are as follows:
Type: PCB Antenna
Gain: 2.5 dBi
This device is intended only for host manufacturers under the following conditions:
The transmitter module may not be co-located with any other transmitter or antenna;
The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a ‘unique’ antenna coupler.
As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**2.8 Label and compliance information**
Host product manufacturers need to provide a physical or e-label stating “Contains FCC ID: 2AWOC-GOC-BA440” with their finished product.

**2.9 Information on test modes and additional testing requirements**

Operation Frequency:
BT/BLE: 2402-2480MHz
2.4GWiFi：2412~2462MHz
5GWiFi：
U-NII-1: 5150 MHz to 5250 MHz,
U-NII-3: 5725 MHz to 5850 MHz
Type: PCB Antenna
Gain: 2.5dBi Max.

Host manufacturer must perfom test of radiated & conducted emission and spurious emission, etc according to the actual test modes for a stand-alone modular transmitter in a host, as well as for multiple simultaneously transmitting modules or other transmitters in a host product.
Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

**2.10 Additional testing, Part 15 Subpart B disclaimer**

The modular transmitter is only FCC authorized for FCC Part 15 Subpart C 15.247 & 15.207 & 15.209 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

## FCC STATEMENT :

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

**Warning:** Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and receiver.

Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/TV technician for help.

### FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.