Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM17520
Contactless Transceiver IC

Datasheet

Oct.2016

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1 Product Overview

1.1 Introduction

The FM17520 is a highly integrated transceiver IC for contactless communication at 13.56 MHz, supporting Reader/Writer mode of ISO/IEC 14443A.

The FM17520's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC14443A cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC14443A compatible cards and transponders. The digital part handles the complete ISO/IEC 14443A framing and error detection. The FM17520 supports ISO/IEC14443A cards and transponders with transfer speeds from 106kbit/s to 424kbit/s in both directions.

With the features of low voltage, low power and large operating distance, FM17520 is especially suitable for connectless Reader/Writer equipment with low power, low voltage and low cost requirements.

1.2 Features

- Supports ISO/IEC 14443 A Reader/Writer mode
- ISO14443A transfer speed communication at 106kbps, 212kbps, 424kbps, 848kbps
- Typical operating distance in Read/Write mode up to 50mm depending on the antenna size and tuning
- Supports SPI up to 10Mbps, with voltage levels according pad voltage supply
- Comfortable 64 byte send and receive FIFO-buffer
- Flexible interrupt modes
- Multiple low-power modes
  - Soft powerdown mode
  - Hard powerdown mode
  - Deep powerdown mode(typical 1uA)
- Programmable timer
- Internal oscillator to connect 27.12 MHz quartz
- Wide voltage supply: 2.2V ~ 3.6V
- Integrated CRC Co-processor
- Programmable I/O pins

1.3 Block Diagram

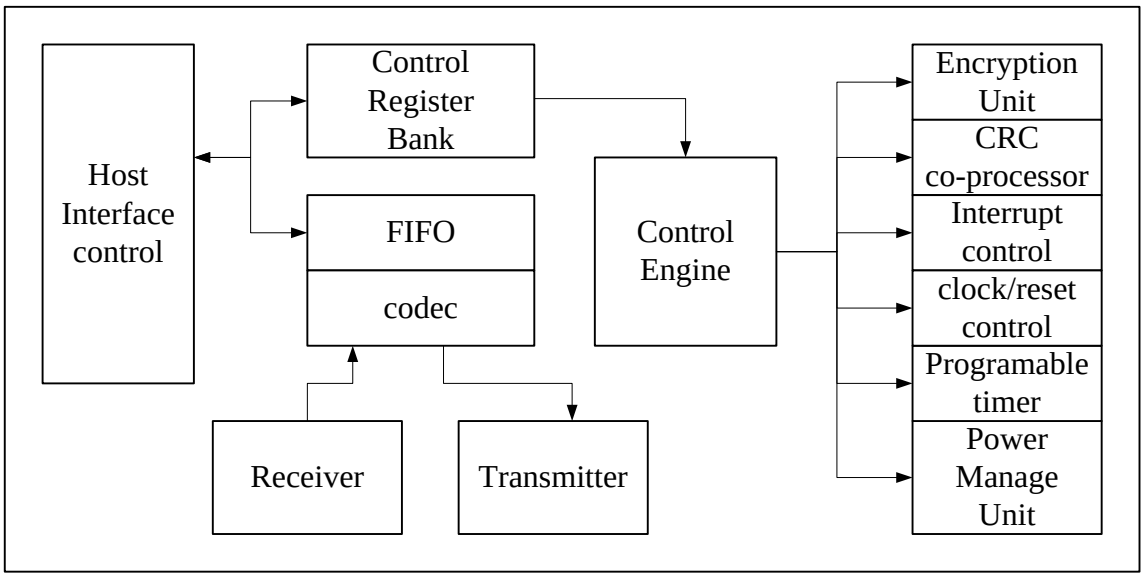


Fig1-1 FM17520 block diagram

1.4 Pinning Information

1.4.1 FM17520 Pinning Assignment

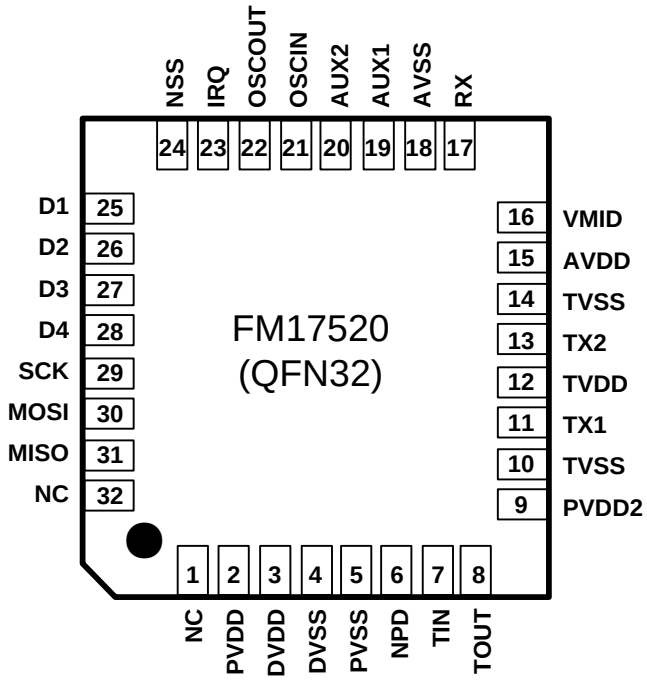


Fig1-2 FM17520 QFN32 pinning assignment (top view)

Pin Description：

Pin	Symbol	Type	Description
1	NC	-	-
2	PVDD	P	pin power supply
3	DVDD	P	chip power supply
4	DVSS	G	digital ground
5	PVSS	G	pin ground
6	NPD	I	power-down input, active low, reset chip when posedge on NPD pin
7	TIN	I	test input
8	TOUT	O	test output
9	PVDD2	P	pin power supply for TIN and TOUT pin
10	TVSS	G	transmitter output1 ground
11	TX1	O	transmitter 1 modulated 13.56MHz energy carrier output
12	TVDD	P	transmitter power supply
13	TX2	O	transmitter 2 modulated 13.56MHz energy carrier output
14	TVSS	G	transmitter output 2 ground
15	AVDD	P	analog power supply
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test
20	AUX2	O	auxiliary outputs for test
21	OSCIN	I	crystal oscillator input; also input externally generated

Pin	Symbol	Type	Description
			clock(27.12MHz)
22	OSCOUT	O	crystal oscillator output
23	IRQ	O	interrupt request output, indicates an interrupt event
24	NSS	I	SPI interface enable
25	D1	IO	test port
26	D2	IO	test port
27	D3	IO	test port
28	D4	IO	test port
29	SCK	I	SPI serial clock input
30	MOSI	I	SPI master output and slave input
31	MISO	O	SPI master input and slave output
32	NC	-	-

Tab1-1 FM17520 QFN32 pin description

2 Functional Description

2.1 General Description

FM17520 Reader IC supports ISO/IEC14443 A protocols using various transfer speeds.

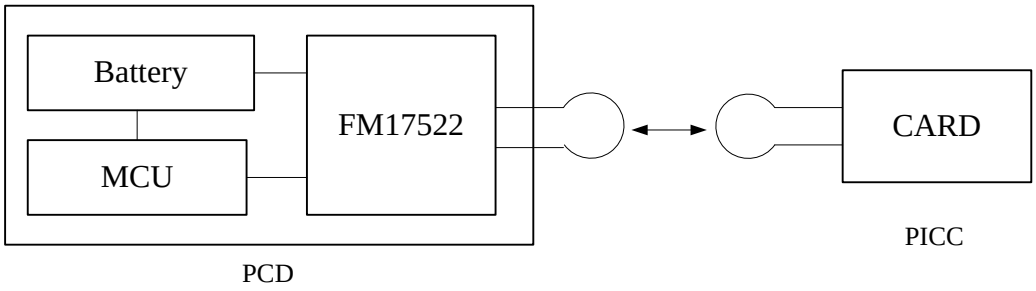


Fig2-1 FM17520 application diagram

2.2 ISO/IEC14443 A Functionality

Tab 2-1 lists the transfer speeds of ISO/IEC14443A supported by FM17520.

Communication Direction	Singal Type	Transfer Speed		
		106 kBd	212 kBd	424 kBd
Reader to Card(send data from FM17520 to a card)	reader side modulation	100%ASK	100%ASK	100%ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	(128/13.56) μ s	(64/13.56) μ s	(32/13.56) μ s
Card to Reader(FM17520 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56MHz/16	13.56MHz/16	13.56MHz/16
	bit encoding	Manchester encoding	BPSK	BPSK

Tab2-1 FM17520 ISO/IEC A communication overview

The communication between FM17520 and RFID meets ISO/IEC14443A. Fig 2-2 lists standard frames for PCD and PICC.

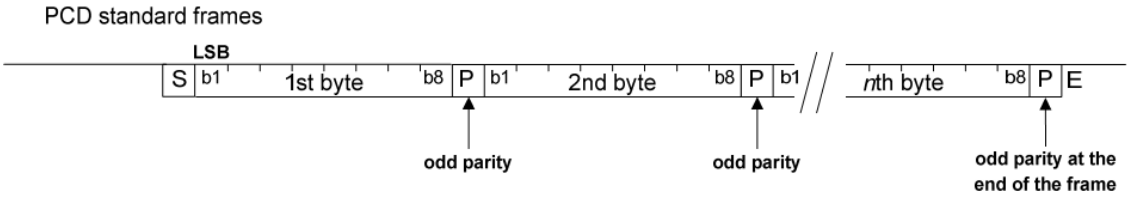


Fig2-2 PCD standard frames

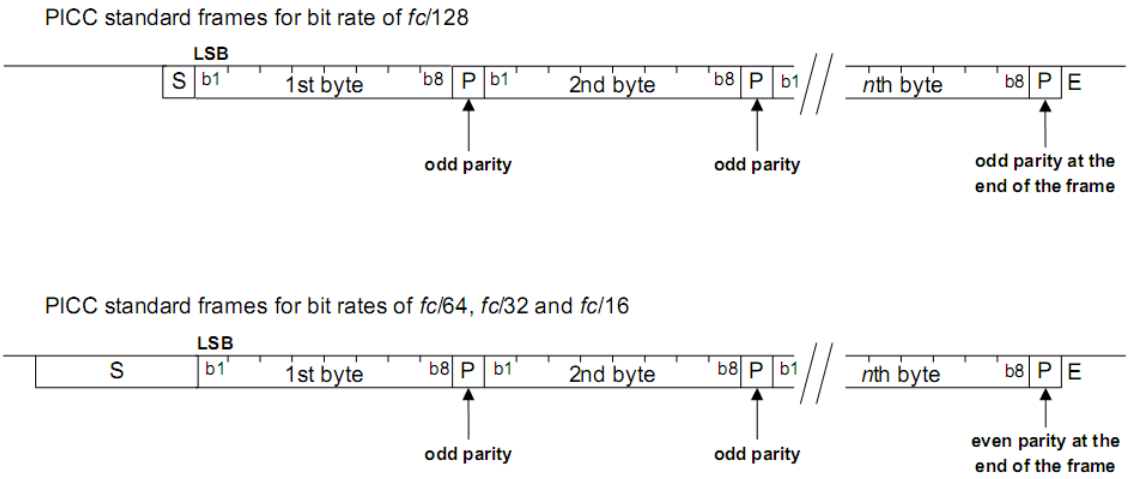


Fig2-3 PICC standard frames

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the ManualRCVReg register's ParityDisable bit.

3 FM17520 Register Set

3.1 FM17520 Registers Overview

3.1.1 Registers Overview

Page0：Command and Status

Page1：Communication

Page2：Configuration

Page3：Test

Page	Addr	Register Name	Function
0	0	RFU	Reserved for future use
	1	CommandReg	Starts and stops command execution
	2	ComIEnReg	Controls bits to enable and disable the passing of Interrupt Requests
	3	DivIEnReg	Controls bits to enable and disable the passing of Interrupt Requests
	4	ComIrqReg	Contains Interrupt Request bits
	5	DivIrqReg	Contains Interrupt Request bits
	6	ErrorReg	Error bits showing the error status of the last command executed
	7	Status1Reg	Contains status bits for communication
	8	Status2Reg	Contains status bits of the receiver and transmitter
	9	FIFODataReg	Input and output of 64 byte FIFO buffer
	A	FIFOLevelReg	Indicates the number of bytes stored in the FIFO
	B	WaterLevelReg	Defines the level for FIFO underflow and overflow warning
	C	ControlReg	Contains miscellaneous Control Registers
	D	BitFramingReg	Adjustments for bit oriented frames
	E	CollReg	Shows the bit position of the first bit collision detected on the RF-interface
	F	EXReg	Extended register(see Tab 3-2)
1	0	RFU	Reserved for future use
	1	ModeReg	Defines general modes for transmitting and receiving
	2	TxModeReg	Defines the data rate and framing during transmission
	3	RxModeReg	Defines the data rate and framing during receiving
	4	TxControlReg	Controls the logical behavior of the antenna driver pins TX1 and TX2
	5	TxASKReg	Controls the setting of the antenna drivers
	6	TxSelReg	Selects the internal sources for the antenna driver
	7	RxSelReg	Selects internal receiver settings
	8	RxThresholdReg	Selects thresholds for the bit decoder
	9	DemodReg	Defines demodulator settings
	A	RFU	Reserved for future use
	B	RFU	Reserved for future use
	C	TxReg	Defines some settings for the transmission of ISO/IEC 14443
	D	RxReg	Defines some settings for the receiving of ISO/IEC 14443

Page	Addr	Register Name	Function
	E	RFU	Reserved for future use
	F	RFU	Reserved for future use
2	0	RFU	Reserved for future use
	1	CRCResultReg	Shows the actual result of the CRC calculation
	2		
	3	RFU	Reserved for future use
	4	ModWidthReg	Controls the setting of the ModWidth
	5	RFU	Reserved for future use
	6	RFCfgReg	Configures the receiver gain
	7	GsNReg	Selects the conductance of the antenna driver pins TX1 and TX2
	8	CWGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2
	9	ModGsPReg	Selects the conductance of the antenna driver pins TX1 and TX2
	A	TModeReg	Defines settings for the internal timer
	B	TPrescalerReg	
	C	TReloadReg	Describes the 16-bit timer reload value
	D		
	E	TCounterValReg	Shows the 16-bit actual timer value
	F		
3	0	RFU	Reserved for future use
	1	TestSel1Reg	General test signal configuration
	2	TestSel2Reg	General test signal configuration and PRBS control
	3	TestPinEnReg	Enables the pin output driver on D1-D4
	4	TestPinValueReg	Defines the values for the 4-bit parallel bus when it is used as I/O bus
	5	TestBusReg	Shows the status of the internal testbus
	6	TestCtrlReg	Test control
	7	RFT	Reserved for production tests
	8	AnalogTestReg	Controls the pins AUX1 and AUX2
	9	TestDAC1Reg	Defines the test value for the TestDAC1
	A	TestDAC2Reg	Defines the test value for the TestDAC2
	B	TestADCReg	Shows the actual value of ADC I and Q
	C-F	RFT	Reserved for production tests

Tab3-1 Registers overview

Extended Registers (EXReg):

Page	Addr	Secondary Addr	Extended Register Name	Function
0	F	03	HpdCtrl	HPD/DPD mode control
		1B	UseRet	Controls data retention function in HPD mode
		1D	LVDctrl	Controls the low-voltage detection

Tab3-2 Extended registers overview

3.1.2 Register Bit Behavior

The table belowdescribles the behavior and the access conditions of registers.

Abbreviation	Behavior	Description
r/w	read and write	These bits can be written and read by the µ-Controller. Since theyare used only for control means, their content is not influenced byinternal state machines.
dy	dynamic	These bits can be written and read by the µ-Controller, and they may also be written by internalstate machines.
r	read only	These registers' value is determined by internal states only. The µ-Controller can read them only.
w	write only	These registers are write only. Reading them always returns ZERO.
RFU	-	These registers are reserved for future use.
RFT	-	These registers are reserved for production tests and shall not bechanged.

Tab3-3 Behavior of register bits and its description

3.2 Register Description

3.2.1 Page 0：Command and Status

3.2.1.1 RFU_address00h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-4 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-5 RFUReg bits description

3.2.1.2 CommandReg_address 01h

Starts and stops command execution.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RcvOff	Power Down	Command			
Access Rights	-	-	r/w	dy	dy	dy	dy	dy
Reset Value	0	0	1	0	0	0	0	0

Tab3-6 CommandReg register

Bit	Symbol	Description
7-6	-	Reserved for future use.
5	RcvOff	Set to logic 1, the analog part of the receiver is switched off.
4	PowerDown	Set to logic 1, Soft Power-down mode is entered. Set to logic 0, the FM17520 starts the wake up procedure. During this procedure, this bit still shows a 1. A 0 indicates that the FM17520 is

Bit	Symbol	Description
		ready for operations. **Remark:** The bit Power Down cannot be set, when the command SoftReset has been activated.
3-0	Command	Command register. Activates a command according to the Command Code. Reading it shows, which command is actually executed

Tab3-7 CommandReg bits description

3.2.1.3 CommIEnReg_address 02h

Control bits to enable and disable the passing of interrupt requests.

Bit	7	6	5	4	3	2	1	0
Definition	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	0	0	0	0	0	0	0

Tab3-8 CommIEnReg register

Bit	Symbol	Description
7	Irqlnv	Set to logic 1, the signal on pin IRQ is inverted with respect to bit IRq in the register Status1Reg. Set to logic 0, the signal on pin IRQ is equal to bit IRq. In combination with bit IRqPushPull in register DivIEnReg, the default value of 1 ensures, that the output level on pin IRQ is 3-state.
6	TxIEn	Allows the transmitter interrupt request (indicated by bit TxIRq) to be propagated to pin IRQ.
5	RxIEn	Allows the receiver interrupt request (indicated by bit RxIRq) to be propagated to pin IRQ.
4	IdleIEn	Allows the idle interrupt request (indicated by bit IdleIRq) to be propagated to pin IRQ.
3	HiAlertIEn	Allows the high alert interrupt request (indicated by bit HiAlertIRq) to be propagated to pin IRQ.
2	LoAlertIEn	Allows the low alert interrupt request (indicated by bit LoAlertIRq) to be propagated to pin IRQ.
1	ErrIEn	Allows the error interrupt request (indicated by bit ErrIRq) to be propagated to pin IRQ.
0	TimerIEn	Allows the timer interrupt request (indicated by bit TimerIRq) to be propagated to pin IRQ.

Tab3-9 CommIEnReg bits description

3.2.1.4 DivIEnReg_address03h

Control bits to enable and disable the passing of interrupt requests.

Bit	7	6	5	4	3	2	1	0
Definition	IRQPushPull	RFU	RFU	TinActIEn	RFU	CRCIEn	RFU	RFU
Access Rights	r/w	-	-	r/w	-	r/w	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-10 DivIEnReg register

Bit	Symbol	Description
7	IRQPushPull	Set to logic 1, the pin IRQ works as standard CMOS output pad. Set to logic 0, the pin IRQ works as open drain output pad.
6-5	-	Reserved for future use.
4	TinActIEn	Allows the TIN active interrupt request to be propagated to pin IRQ.
3	RFU	Reserved for future use.
2	CRCIEn	Allows the CRC interrupt request (indicated by bit CRCIRq) to be propagated to pin IRQ.
1-0	RFU	Reserved for future use.

Tab3-11 DivIEnReg bits description

3.2.1.5 CommIRqReg_address04h

Contain Interrupt Request bits.

Bit	7	6	5	4	3	2	1	0
Definition	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access Rights	w	dy	dy	dy	dy	dy	dy	dy
Reset Value	0	0	0	1	0	1	0	0

Tab3-12 CommIRqReg register

Bit	Symbol	Description
7	Set1	Set to logic 1, Set1 defines that the marked bits in the register CommIRqReg are set. Set to logic 0, Set1 defines, that the marked bits in the register CommIRqReg are cleared.
6	TxIRq	Set to logic 1 immediately after the lastbit of the transmitted data was sent out.
5	RxIRq	Set to logic 1 when the receiver detects the end of a valid datastream. If the bit RxNoErr in register RxModeReg is set to logic 1, bit RxIRq is only set to logic 1 when data bytes are available in the FIFO.
4	IdleIRq	Set to logic 1, when a command terminates by itself or when the CommandReg changes its value from any command to the Idle Command. If an unknown command is started, the CommandReg changes its content to the idle state and the bit IdleIRq is set. Starting the Idle Command by the μ-Controller does not set bit IdleIRq
3	HiAlertIRq	Set to logic 1, when bit HiAlert in register Status1Reg is set. In opposition to HiAlert, HiAlertIRq stores this event and can only be reset as indicated by bit Set1.
2	LoAlertIRq	Set to logic 1, when bit LoAlert in register Status1Reg is set. In opposition to LoAlert, LoAlertIRq stores this event and can only be reset as indicated by bit Set1.
1	ErrIRq	Set to logic 1 if any error bit in the Error Register is set.
0	TimerIRq	Set to logic 1 when the timer decrements the TimerValue Register to zero.

Tab3-13 CommIRqReg bits description

3.2.1.6 DivIRqReg_address05h

Contain Interrupt Request bits.

Bit	7	6	5	4	3	2	1	0
Definition	Set2	RFU	RFU	TinActIRq	RFU	CRCIRq	RFU	RFU
Access Rights	w	-	-	dy	-	dy	-	-
Reset Value	0	0	0	x	0	0	x	x

Tab3-14 DivIRqReg register

Bit	Symbol	Description
7	Set2	Set to logic 1, Set2 defines thatthe marked bits in the register DivIRqReg are set. Set to logic 0, Set2 defines, that the marked bits in the register DivIRqReg are cleared
6-5	-	Reserved for future use.
4	TinActIRq	Set to logic 1, when TIN is active.This interrupt is set when either a rising or falling signal edge is detected.
3	-	Reserved for future use.
2	CRCIRq	Set to logic 1, when the CRC command is active and all data are processed.
1-0	-	Reserved for future use.

Tab3-15 DivIRqReg bits description

3.2.1.7 ErrorReg_address06h

Error bit register showing the error status of the last command executed.

Bit	7	6	5	4	3	2	1	0
Definition	WrErr	TempErr	RFU	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access Rights	r	r	-	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Tab3-16 ErrorReg register

Bit	Symbol	Description
7	WrErr	Set to logic 1, when data is written into FIFO by the host controller during the Authent command or if data is written into FIFO by the host controller during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface.
6	TempErr	Set to logic 1, if the internal temperature sensor detects overheating. In this case, the antenna drivers are switched off automatically. Remark: excuting new command can clear all error bits except TempErr.
5	-	Reserved for future use.

Bit	Symbol	Description
4	BufferOvfl	Set to logic 1, if the host controller or a FM17520's internal state machine (e.g. receiver) tries to write datainto the FIFO-bufferalthough the FIFO-buffer is already full.
3	CollErr	Set to logic 1, if a bit-collision is detected. It is cleared automatically at receiver start-up phase. This bit is only valid during the bitwise anticollision at 106 kbit/s. During communication schemes at 212 and 424kbit/s this bit is always set to logic 1.
2	CRCErr	Set to logic 1, if bit RxCRCEn in register RxModeReg is set and the CRC calculation fails. It is cleared to 0 automatically at receiver start-up phase.
1	ParityErr	Set to logic 1, if the parity check has failed. It is cleared automatically at receiver start-up phase. Only valid for ISO/IEC 14443A communication at 106 kbit/s.
0	ProtocolErr	Set to logic 1, if one out of the following cases occur: ● Set to logic 1 if the SOF is incorrect. It is cleared automatically at receiver start-up phase. The bit is only valid for 106kbit/s in Communication mode. ● During the Authent Command, bit ProtocolErr is set to logic 1, if the number of bytes received in one data stream is incorrect.

Tab3-17 ErrorReg bits description

3.2.1.8 Status1Reg_address 07h

Contain status bits of the CRC, Interrupt and FIFO buffer.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	CRCOk	CRCReady	IRq	TRunning	RFU	HiAlert	LoAlert
Access Rights	-	r	r	r	r	-	r	r
Reset Value	0	0	1	0	0	0	0	1

Tab3-18 Status1Reg register

Bit	Symbol	Description
7	-	Reserved for future use.
6	CRCOk	Set to logic 1, if the CRC Result is zero. For data transmission and reception the bit CRCOk is undefined (use CRCErr in register ErrorReg). CRCOk indicates the status of the CRC coprocessor, during calculation the value changes to 0, when the calculation is done correctly, the value changes to 1.
5	CRCReady	Set to logic 1, when the CRC calculation has finished. This bit is only valid for the CRC coprocessor calculation using the command CalcCRC.
4	IRq	This bit shows, if any interrupt source requests attention (with respect to the setting of the interrupt enable bits, see register CommIEnReg and DivIEnReg).
3	TRunning	Set to logic 1, if the FM17520's timer unit is running. (The timer will decrement the TCounterValReg with the next timer clock.) Remark: In the gated mode the bit TRunning is set to logic 1, when the timer is enabled by the register bits. This bit is not influenced by the gated signal.
2	-	Reserved for future use.
1	HiAlert	Set to logic 1, when the numberof bytes stored in the FIFO-buffer fulfills the following equation: HiAlert = (64 – FIFOLength) ≤ WaterLevel Example： FIFOLength = 60, WaterLevel = 4 → HiAlert = 1 FIFOLength = 59, WaterLevel = 4 → HiAlert = 0

Bit	Symbol	Description
0	LoAlert	Set to logic 1, when the numberof bytes stored in the FIFO-buffer fulfills the following equation: LoAlert = FIFOLength ≤ WaterLevel Example： FIFOLength = 4, WaterLevel = 4 → LoAlert = 1 FIFOLength = 5, WaterLevel = 4 → LoAlert = 0

Tab3-19 Status1Reg bits description

3.2.1.9 Status2Reg_address 08h

Contain status bits of the Receiver, Transmitter and Data mode detector.

Bit	7	6	5	4	3	2	1	0
Definition	TempSensClear	RFU	RFU	RFU	Crypto1On	ModemState		
Access Rights	r/w	-	-	-	dy	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Tab3-20 Status2Reg register

Bit	Symbol	Description	
7	TempSensClear	Set to logic 1, this bit clears the temperature error, if the temperature is below the alarm limit of 125° C.	
6	-	Reserved for future use.	
5	-	Reserved for future use.	
4	-	Reserved for future use.	
3	Crypto1On	This bit indicates that the Crypto1 unit is switched on and therefore all data communication with the card is encrypted. This bit is only valid in Reader/Writer mode for cards. This bit can only be set to logic 1 by a successful execution of the Authent Command. This bit shall be cleared by software.	
2-0	ModemState	ModemState shows the state of the transmitter and receiver state machines.	
		Value	**Description**
		000	IDLE
		001	Wait for StartSend in register BitFramingReg
		010	TxWait: Wait until RF field is present, if the bit TxWaitRF is set to logic 1. The minimum time for TxWait is defined by the TxWaitReg register.
		011	Sending
		100	RxWait: Wait until RF field is present, if the bit RxWaitRF is set to logic 1. The minimum time for RxWait is defined by the RxWaitReg register.
		101	Wait for data
		110	Receiving

Tab3-21 Status2Reg bits description

3.2.1.10 FIFODataReg_address 09h

Input and output port of 64 byte FIFO buffer.

Bit	7	6	5	4	3	2	1	0
Definition	FIFOData							
Access Rights	dy	dy	dy	dy	dy	dy	dy	dy
Reset Value	x	x	x	x	x	x	x	x

Tab3-22 FIFODataReg register

Bit	Symbol	Description
7-0	FIFOData	Data input and output port for the internal 64 byte FIFO buffer. The FIFO buffer acts as parallel in/parallel out converter for all serial data stream in- and outputs.

Tab3-23 FIFODataReg bits description

3.2.1.11 FIFOLevelReg_address 0Ah

Indicate the number of bytes stored in the FIFO.

Bit	7	6	5	4	3	2	1	0
Definition	FlushBuffer	FIFOLevel						
Access Rights	w	r	r	r	r	r	r	r
Reset Value	0	0	0	0	0	0	0	0

Tab3-24 FIFOLevelReg register

Bit	Symbol	Description
7	FlushBuffer	Set to logic 1, this bit clears the internal FIFO buffer's read-pointer and write-pointer and the bit BufferOvfl in the register ErrReg immediately. Reading this bit will always return 0.
6-0	FIFOLevel	Indicate the number of bytes stored in the FIFO-buffer. Writing to the FIFODataReg increments, reading decrements the FIFOLevel.

Tab3-25 FIFOLevelReg bits description

3.2.1.12 WaterLevelReg_address 0Bh

Define the level for FIFO underflow and overflow warning.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	WaterLevel					
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	1	0	0	0

Tab3-26 WaterLevelReg register

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	WaterLevel	This register defines a warning level to indicate a FIFO buffer overflow or underflow. The bit HiAlert in Status1Reg is set to logic 1, if the remaining

Bit	Symbol	Description
		number of bytes in the FIFO buffer space is equal or less than the defined number of WaterLevel bytes. The bit LoAlert in Status1Reg is set to logic 1, if equal or less than WaterLevel bytes are in the FIFO.

Tab3-27 WaterLevelReg bits description

3.2.1.13 ControlReg_address 0Ch

Some control bits.

Bit	7	6	5	4	3	2	1	0
Definition	TStopNow	TStartNow	RFU	RFT	RFU	RxLastBits		
Access Rights	w	w	-	-	-	r	r	r
Reset Value	0	0	0	1	0	0	0	0

Tab3-28 ControlReg register

Bit	Symbol	Description
7	TStopNow	Set to logic 1, the timer stops immediately. Reading this bit will always return 0.
6	TStartNow	Set to logic 1 starts the timer immediately. Reading this bit will always return 0.
5	-	Reserved for future use.
4	RFT	Reserved for production tests.
3	-	Reserved for future use.
2-0	RxLastBits	Shows the number of valid bits in the last received byte. If 0, the whole byte is valid.

Tab3-29 ControlReg bits description

3.2.1.14 BitFramingReg_address 0Dh

Adjustments for bit oriented frames.

Bit	7	6	5	4	3	2	1	0
Definition	StartSend	RxAlign			RFU	TxLastBits		
Access Rights	w	r/w	r/w	r/w	-	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-30 BitFramingReg register

Bit	Symbol	Description
7	StartSend	Set to logic 1, the transmission of data starts. This bit is only valid in combination with the Transceive command.
6-4	RxAlign	Used for reception of bit oriented frames: RxAlign defines the bit position for the first bit received to be stored in the FIFO. Further received bits are stored at the following bit positions.
		Example: RxAlign = 0: the LSB of the received bit is stored at bit 0, the second received bit is stored at bit position 1. RxAlign = 1: the LSB of the received bit is stored at bit 1, the second received bit is stored at bit position 2. RxAlign = 7: the LSB of the received bit is stored at bit 7, the second received bit is stored in the following byte at bit position 0.
		This bit shall only be used for bitwise anticollision at 106 kbit/s in Communication mode. In all other modes it shall be set to logic 0.
3	-	Reserved for future use.

Bit	Symbol	Description
2-0	TxLastBits	Used for transmission of bit oriented frames: TxLastBits defines the number of bits of the last byte that shall be transmitted. A 000 indicates that all bits of the last byte shall be transmitted.

Tab3-31 BitFramingReg bits description

3.2.1.15 CollReg_address 0Eh

Define the first bit collision detected on the RF interface.

Bit	7	6	5	4	3	2	1	0
Definition	Values AfterColl	RFU	CollPos NotValid	CollPos				
Access Rights	r/w	-	R	R	R	R	R	R
Reset Value	1	0	1	x	x	x	x	x

Tab3-32 CollReg register

Bit	Symbol	Description
7	Values AfterColl	If this bit is set to logic 0, all receiving bits will be cleared after a collision. This bit shall only be used during bitwise anticollision at 106 kbit/s, otherwise it shall be set to logic 1.
6	-	Reserved for future use.
5	CollPosNotValid	Set to logic 1, if no Collision is detected or the Position of the Collision is out of the range of bits CollPos.
4-0	CollPos	These bits show the bit position of the first detected collision in a received frame, only data bits are interpreted.
		Example: 00h indicates a bit collision in the 32th bit 01h indicates a bit collision in the 1st bit 08h indicates a bit collision in the 8th bit
		These bits shall only be interpreted if bit CollPosNotValid is set to logic 0.

Tab3-33 CollReg bits description

3.2.1.16 EXReg_address 0Fh

Entrance for access extended registers.

Bit	7	6	5	4	3	2	1	0
Definition	EXmode		EXAddr					
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-34 EXReg register

Bit	Symbol	Description
7-6	EXmode	Access modes to extended registers: 01: writing mode, bit5~0 writes secondary address 10: reading mode, bit5~0 reads secondary address 11: writing mode, bit5~0 writes data 00: reading mode, bit5~0 reads data See section 4.2 ”Accessing Extended Register” for more information about access modes
5-0	EXAddr	secondary address or data of extended registers

Tab3-35 EXReg bits description

3.2.2 Page 1：Communication

3.2.2.1 RFU_address 10h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-36 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-37 RFUReg bits description

3.2.2.2 ModeReg_address 11h

Define general mode settings for transmitting and receiving.

Bit	7	6	5	4	3	2	1	0
Definition	MSBFirst	RFU	TxWaitRF	RFU	PolTin	RFT	CRCPreset	
Access Rights	r/w	-	r/w	-	r/w	-	r/w	r/w
Reset Value	0	0	1	1	1	1	1	1

Tab3-38 ModeReg register

Bit	Symbol	Description	
7	MSBFirst	Set to logic 1, the CRC coprocessor calculates the CRC with MSB first and the CRCResultMSB and the CRCResultLSB in the CRCResultReg register are bit reversed. **Remark:** During RF communication this bit is ignored.	
6	RFU	Reserved for future use.	
5	TxWaitRF	Set to logic 1 the transmitter in reader/writer mode can only be started, if an RF field is generated.	
4	RFU	Reserved for future use.	
3	PolTin	PolSigin defines the polarity of the TIN pin. Set to logic 1, the polarity of TIN pin is active high. Set to logic 0 the polarity of TIN pin is active low. **Remark:** The internal envelope signal is coded active low. **Remark:** Changing this bit will generate a TinActIRq event.	
2	RFT	Reserved for production tests.	
1-0	CRCPreset	Defines the preset value for the CRC coprocessor for the command CalCRC. **Remark:** During any communication, the preset values are selected automatically according to the definition in the bits RxMode and TxMode.	
		Value	**Description**
		00	0000
		01	6363
		10	A671
		11	FFFF

Tab3-39 ModeReg bits description

3.2.2.3 TxModeReg_address 12h

Define the data rate and framing during transmission.

Bit	7	6	5	4	3	2	1	0
Definition	TxCRCEn	TxSpeed			InvMod	RFU	RFU	RFU
Access Rights	r/w	dy	dy	dy	r/w	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-40 TxModeReg register

Bit	Symbol	Description	
7	TxCRCEn	Set to logic 1, this bit enables the CRC generation during data transmission. **Remark:** This bit shall only be set to logic 0 at 106 kbit/s.	
6-4	TxSpeed	Defines the bit rate while data transmission.	
		Value	**Description**
		000	106 kbit
		001	212 kbit
		010	424 kbit
		011	848 kbit
		100	Reserved
		101	Reserved
		110	Reserved
		111	Reserved
3	InvMod	Set to logic 1, the modulation for transmitting data is inverted.	
2-0	RFU	Reserved for future use.	

Tab3-41 TxModeReg bits description

3.2.2.4 RxModeReg_address 13h

Define the data rate and framing during reception.

Bit	7	6	5	4	3	2	1	0
Definition	RxCRCEn	RxSpeed			RxNoErr	RxMultiple	RFU	RFU
Access Rights	r/w	dy	dy	dy	r/w	r/w	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-42 RxModeReg register

Bit	Symbol	Description	
7	RxCRCEn	Set to logic 1, this bit enables the CRC calculation during reception. **Remark:** This bit shall only be set to logic 0 at 106 kbit/s.	
6-4	RxSpeed	Defines the bit rate while data transmission.	
		Value	**Description**
		000	106 kbit
		001	212 kbit
		010	424 kbit
		011	848 kbit
		100	Reserved
		101	Reserved
		110	Reserved
		111	Reserved

Bit	Symbol	Description
3	RxNoErr	If set to logic 1 a not valid received data stream (less than 4 bits received) will be ignored. The receiver will remain active.
2	RxMultiple	Set to logic 0, the receiver is deactivated after receiving a data frame. Set to logic 1, it is possible to receive more than one data frame. Having set this bit, the Receive and Transceive commands will not terminate automatically. In this case the multiple receiving can only be deactivated by writing any command (except the Receive command) to the CommandReg register or by clearing the bit by the host controller. If set to logic 1, at the end of a received data stream an error byte is added to the FIFO. The error byte is a copy of the ErrorReg register.
1-0	RFU	Reserved for future use.

Tab3-43 RxModeReg bits description

3.2.2.5 TxControlReg_address 14h

Control the antenna driver pins TX1 and TX2.

Bit	7	6	5	4	3	2	1	0
Definition	InvTx2RFOn	InvTx1RfOn	InvTx2RFOff	InvTx1RFOff	Tx2CW	RFU	Tx2RFEn	Tx1RFEn
Access Rights	r/w	r/w	r/w	r/w	r/w	-	r/w	r/w
Reset Value	1	0	0	0	0	0	0	0

Tab3-44 TxControlReg register

Bit	Symbol	Description
7	InvTx2RFOn	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is enabled.
6	InvTx1RfOn	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is enabled.
5	InvTx2RFOff	Set to logic 1, the output signal at pin TX2 will be inverted, if driver TX2 is disabled.
4	InvTx1RFOff	Set to logic 1, the output signal at pin TX1 will be inverted, if driver TX1 is disabled.
3	Tx2CW	Set to logic 1, the output signal on pin TX2 will deliver continuously the un-modulated 13.56 MHz energy carrier. Set to logic 0, Tx2CW is enabled to modulate the 13.56 MHz energy carrier.
2	RFU	Reserved for future use.
1	Tx2RFEn	Set to logic 1, the output signal on pin TX2 will deliver the 13.56 MHz energy carrier modulated by the transmission data.
0	Tx1RFEn	Set to logic 1, the output signal on pin TX1 will deliver the 13.56 MHz energy carrier modulated by the transmission data.

Tab3-45 TxControlReg bits description

3.2.2.6 TxASKReg_address 15h

Control the settings of the antenna driver.

Bit	7	6	5	4	3	2	1	0
Definiti	RFU	Force100	RFU	RFU	RFU	RFU	RFU	RFU

Bit	7	6	5	4	3	2	1	0
on		ASK						
Access Rights	-	r/w	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-46 TxASKReg register

Bit	Symbol	Description
7	RFU	Reserved for future use.
6	Force100ASK	Set to logic 1, Force100ASK forces a 100% ASK modulation independent of the setting in register ModGsPReg.
5-0	RFU	Reserved for future use.

Tab3-47 TxASKReg bits description

3.2.2.7 TxSelReg_address 16h

Select the sources for the antenna driver.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	DriverSel		TOutSel			
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	1	0	0	0	0

Tab3-48 TxSelReg register

Bit	Symbol	Description	
7-6	-	Reserved for future use.	
5-4	DriverSel	Selects the input of driver Tx1 and Tx2.	
		Value	**Description**
		00	Tristate **Remark:** In soft power down the drivers are only in Tristate mode if DriverSel is set to Tristate mode.
		01	Modulation signal (envelope) from the internal coder
		10	Modulation signal (envelope) from TIN
		11	High level **Remark:** The HIGH level depends on the setting of InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff.
3-0	TOutSel	Selects the input for the TOUT Pin.	
		Value	**Description**
		0000	Tristate
		0001	Low level
		0010	High level
		0011	TestBus signal as defined by bit TestBusBitSel in register TestSel1Reg.
		0100	Modulation signal (envelope) from the internal coder
		0101	Serial data stream to be transmitted(before Miller coding)
		0110	Reserved for future use.
		0111	Serial data stream received(after Manchester decoding)
		1000-1111	Reserved for future use.

Tab3-49 TxSelReg bits description

3.2.2.8 RxSelReg_address 17h

Select internal receiver settings.

Bit	7	6	5	4	3	2	1	0
Definition	UartSel		RxWait					
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	0	0	0	0	1	0	0

Tab3-50 RxSelReg register

Bit	Symbol	Description	
7-6	UartSel	Selects the input of the contactless UART	
		Value	**Description**
		00	Constant Low
		01	Manchester with subcarrier from pin TIN
		10	Modulation signal from the internal analog module, default
		11	NRZ coded signal without subcarrier from pin TIN which is only valid for transfer speeds above 106 kbBd
5-0	RxWait	After data transmission, the activation of the receiver is delayed for RxWait bit-clocks. During this 'frame guard time' any signal at pin RX is ignored. This parameter is ignored by the Receive command. All other commands use this parameter. The counter starts with the last modulation pulse of the transmitted data stream.	

Tab3-51 RxSelReg bits description

3.2.2.9 RxThresholdReg_address 18h

Select thresholds for the bit decoder.

Bit	7	6	5	4	3	2	1	0
Definition	MinLevel				RFU	CollLevel		
Access Rights	r/w	r/w	r/w	r/w	-	r/w	r/w	r/w
Reset Value	1	0	0	0	0	1	0	0

Tab3-52 RxThresholdReg register

Bit	Symbol	Description
7-4	MinLevel	Defines the minimum signal strength at the decoder input that shall be accepted. If the signal strength is below this level, it is not evaluated.
3	-	Reserved for future use.
2-0	CollLevel	Defines the minimum signal strength at the decoder input that has to be reached by the weaker half-bit of the Manchester-coded signal to generate a bit-collision relatively to the amplitude of the stronger half-bit.

Tab3-53 RxThresholdReg bits description

3.2.2.10 DemodReg_address 19h

Define demodulator settings.

Bit	7	6	5	4	3	2	1	0
Definition	AddIQ		FixIQ	RFU	TauRcv		TauSync	
Access Rights	r/w	r/w	r/w	-	r/w	r/w	r/w	r/w
Reset Value	0	1	0	0	1	1	0	1

Tab3-54 DemodReg register

Bit	Symbol	Description	
7-6	AddIQ	Defines the use of I and Q channel during reception. **Remark:** FixIQ has to be set to logic 0 to enable the following settings.	
		Value	**Description**
		00	Select the stronger channel
		01	Select the stronger and freeze the selected during communication
		10	combines the I and Q channel
		11	Reserved
5	FixIQ	If set to logic 1 and the bits of AddIQ are set to X0, the reception is fixed to I channel. If set to logic 1 and the bits of AddIQ are set to X1, the reception is fixed to Q channel.	
4	-	Reserved for future use.	
3-2	TauRcv	Changes the time constant of the internal during data reception. **Remark:** If set to 00, the PLL is frozen during data reception.	
1-0	TauSync	Changes the time constant of the internal PLL during burst.	

Tab3-55 DemodReg bits description

3.2.2.11 RFU_address 1A h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-56 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-57 RFUReg bits description

3.2.2.12 RFU_address 1B h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-58 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-59 RFUReg bits description

3.2.2.13 TxReg_address 1Ch

Control part of transmission parameters in ISO/IEC 14443A.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	TxWait	
Access Rights	-	-	-	-	-	-	r/w	r/w
Reset Value	0	1	1	0	0	0	1	0

Tab3-60 TxReg register

Bit	Symbol	Description
7-2	RFU	Reserved for future use.
1-0	TxWait	These bits define the additional response time. Per default 7 bits are added to the value of the register bit.

Tab3-61 TxReg bits description

3.2.2.14 RxReg_address 1D h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	ParityDisable	RFU	RFU	RFU	RFU
Access Rights	-	-	-	r/w	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-62 RxReg register

Bit	Symbol	Description
7-5	RFU	Reserved for future use.
4	Parity Disable	If this bit is set to logic 1, the generation of the Parity bit for transmission and the Parity-Check for receiving is switched off. The received Parity bit is handled as a data bit.
3-0	RFU	Reserved for future use.

Tab3-63 RxReg bits description

3.2.2.15 RFU_address 1Eh

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-64 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-65 RFUReg bits description

3.2.2.16 RFU_address 1Fh

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	1	1	1	0	1	0	1	1

Tab3-66 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-67 RFUReg bits description

3.2.3 Page 2：Configuration

3.2.3.1 RFU_address 20h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-68 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-69 RFUReg bits description

3.2.3.2 CRCResultMSBReg_address 21h

Show the actual result of the CRC calculation.
Remark: The CRC is split into two 8-bit register.
Remark: Setting the bit MSBFirst in ModeReg register reverses the bit ordering, the byte order is not changed.

Bit	7	6	5	4	3	2	1	0
Definition	CRCResultMSB							
Access Rights	r	r	r	r	r	r	r	r
Reset Value	1	1	1	1	1	1	1	1

Tab3-70 CRCResultReg register

Bit	Symbol	Description
7-0	CRCResultMSB	This register shows the actual value of the most significant byte of the CRCResultReg register. It is valid only if bit CRCReady in register Status1Reg is set to logic 1.

Tab3-71 CRCResultReg bits description

3.2.3.3 CRCResultLSBReg_address 22h

Bit	7	6	5	4	3	2	1	0
Definition	CRCResultLSB							
Access Rights	r	r	r	r	r	r	r	r
Reset Value	1	1	1	1	1	1	1	1

Tab3-72 CRCResultReg register

Bit	Symbol	Description
7-0	CRCResultLSB	This register shows the actual value of the least significant byte of the CRCResult register. It is valid only if bit CRCReady in register Status1Reg is set to logic 1.

Tab3-73 CRCResultReg bits description

3.2.3.4 RFU_address 23h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU

Bit	7	6	5	4	3	2	1	0
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-74 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-75 RFUReg bits description

3.2.3.5 ModWidthReg_address24h

Control the modulation width settings.

Bit	7	6	5	4	3	2	1	0
Definition	ModWidth							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	1	0	0	1	1	0

Tab3-76 ModWidthReg register

Bit	Symbol	Description
7-0	ModWidth	These bits define the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1)/fc. The maximum value is half the bit period.

Tab3-77 ModWidthReg bits description

3.2.3.6 RFU_address 25h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-78 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-79 RFUReg bits description

3.2.3.7 RFCfgReg_address 26h

Configure the receiver gain.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RxGain			RFU			
Access Rights	-	r/w	r/w	r/w	-	-	-	-
Reset Value	0	1	0	0	1	0	0	0

Tab3-80 RFCfgReg register

Bit	Symbol	Description	
7	RFU	Reserved for future use.	
6-4	RxGain*	This register defines the receivers signal voltage gain factor:	
		Value	**Description**

Bit	Symbol	Description	
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3-0	RFU	Reserved for future use.	

Tab3-81 RFCfgReg bits description

3.2.3.8 GsNReg_address 27h

Select the conductance for the N-driver of the antenna driver pins TX1 and TX2 when the driver is switched on.

Bit	7	6	5	4	3	2	1	0
Definition	CWGsN				ModGsN			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	1	0	0	0	1	0	0	0

Tab3-82 GsNOnReg register

Bit	Symbol	Description
7-4	CWGsN	The value of this register defines the conductance of the output N-driver during times of no modulation. This may be used to regulate the output power and subsequently current consumption and operating distance. **Remark:** The conductance value is binary weighted. **Remark:** During soft Power-down mode the highest bit is forced to 1. **Remark:** This value is only used if the driver TX1 or TX2 are switched on.
3-0	ModGsN	The value of this register defines the conductance of the output N-driver for the time of modulation. This may be used to regulate the modulation index. **Remark:** The conductance value is binary weighted. **Remark:** During soft Power-down mode the highest bit is forced to 1. **Remark:** This value is only used if the driver TX1 or Tx2 are switched on.

Tab3-83 GsNOnReg bits description

3.2.3.9 CWGsPReg_address 28h

Define the conductance of the P-driver during times of no modulation.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	CWGsP					
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	1	0	0	0	0	0

Tab3-84 CWGsPReg register

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	CWGsP	The value of this register defines the conductance of the output P-driver. This may be used to regulate the output power and subsequently current consumption and operating distance. **Remark:** The conductance value is binary weighted. **Remark:** During soft Power-down mode the highest bit is forced to 1.

Tab3-85 CWGsPReg bits description

3.2.3.10 ModGsPReg_address 29h

Define the driver P-output conductance during modulation.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	ModGsP					
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	1	0	0	0	0	0

Tab3-86 ModGsPReg register

Bit	Symbol	Description
7-6	-	Reserved for future use.
5-0	ModGsP	The value of this register defines the conductance of the output P-driver for the time of modulation. This may be used to regulate the modulation index. **Remark:** The conductance value is binary weighted. **Remark:** During soft Power-down mode the highest bit is forced to 1.

Tab3-87 ModGsPReg bits description

3.2.3.11 TModeReg，TPrescalerReg_address 2Ah

Define settings for the timer.

Remark: The Prescaler value is split into two 8-bit registers.

Bit	7	6	5	4	3	2	1	0
Definition	TAuto	TGated		TAutoRestart	TPrescaler_Hi			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-88 TModeReg register

Bit	Symbol	Description	
7	TAuto	Set to logic 1, the timer starts automatically at the end of the transmission in all communication modes at all speeds. The timer stops after the 5th bit (1 startbit, 4 databits) if the bit RxMultiple in the register RxModeReg is not set. If RxMultiple is set to logic 1, the timer never stops. In this case the timer can be stopped by setting the bit TStopNow in register ControlReg to 1. Setting to logic 0 indicates, that the timer is not influenced by the protocol.	
6-5	TGated	The internal timer is running in gated mode. **Remark:** In the gated mode, the bit TRunning is 1 when the timer is enabled by the register bits.	
		Value	**Description**
		00	Non gated mode
		01	Gated by TIN
		10	Gated by AUX1
		11	-
4	TAutoRestart	Set to logic 1, the timer automatically restarts its count-down from TReloadValue, instead of counting down to 0. Set to logic 0 the timer decrements to 0 and the bit TimerIRq is set to logic 1.	
3-0	TPrescaler_Hi	Defines higher 4 bits for TPrescaler. f_{Timer} = 13.56 MHz/(2*TPreScaler+1) Where TPreScaler = [TPrescaler_Hi：TPrescaler_Lo] (total 12 bits)	

Bit	Symbol	Description
		For detailed description, see section 9 ”Timer Unit”.

Tab3-89 TModeReg bits description

3.2.3.12 TPrescalerLoReg_address 2Bh

Bit	7	6	5	4	3	2	1	0
Definition	TPrescaler_Lo							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-90 TPrescalerReg register

Bit	Symbol	Description
7-0	TPrescaler_Lo	Defines lower 8 bits for TPrescaler. The f_{Timer} formula refers to the description of Tprescaler_Hi in TmodeReg register.

Tab3-91 TPrescalerReg bits description

3.2.3.13 TReloadHiReg_address 2Ch

Describe the 16-bit long timer reload value.

Bit	7	6	5	4	3	2	1	0
Definition	TReloadVal_Hi							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-92 TReloadHiReg register

Bit	Symbol	Description
7-0	TReloadVal_Hi	Defines the higher 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

Tab3-93 TReloadHiReg bits description

3.2.3.14 TReloadLoReg_address 2Dh

Bit	7	6	5	4	3	2	1	0
Definition	TReloadVal_Lo							
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-94 TReloadLoReg register

Bit	Symbol	Description
7-0	TReloadVal_Lo	Defines the lower 8 bits for the TReloadReg. With a start event the timer loads the TReloadVal. Changing this register affects the timer only at the next start event.

Tab3-95 TReloadLoReg bits description

3.2.3.15 TcounterValHiReg_address 2Eh

Show the current value of the timer.

Bit	7	6	5	4	3	2	1	0
Definition	TCounterVal_Hi							
Access Rights	r	r	r	r	r	r	r	r
Reset Value	x	x	x	x	x	x	x	x

Tab3-96 TCounterValHiReg register

Bit	Symbol	Description
7-0	TCounterVal_Hi	Current value of the timer, higher 8 bits.

Tab3-97 TCounterValHiReg bits description

3.2.3.16 TcounterValLoReg_address 2Fh

Bit	7	6	5	4	3	2	1	0
Definition	TCounterVal_Lo							
Access Rights	r	r	r	r	r	r	r	r
Reset Value	x	x	x	x	x	x	x	x

Tab3-98 TCounterValLoReg register

Bit	Symbol	Description
7-0	TCounterVal_Lo	Current value of the timer, lower 8 bits.

Tab3-99 TCounterValLoReg bits description

3.2.4 Page 3：Test

3.2.4.1 RFU_address 30h

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-100 RFU register

Bit	Symbol	Description
7-0	RFU	Reserved for future use.

Tab3-101 RFUReg bits description

3.2.4.2 TestSel1Reg_address 31h

General test signal configuration.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	RFU	RFU	TstBusBitSel		
Access Rights	-	-	-	-	-	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-102 TestSel1Reg register

Bit	Symbol	Description
7-3	-	Reserved for future use.
2-0	TstBusBitSel	Select the TestBus bit from the testbus to be propagated to TOUT. If AnalogSelAux2[3:0] in AnalogTestReg register is FFh, the selectable TestBus bit is propagated to AUX1 or AUX2 meanwhile.

Tab3-103 TestSel1Reg bits description

3.2.4.3 TestSel2Reg_address 32h

General test signal configuration and PRBS control.

Bit	7	6	5	4	3	2	1	0
Definition	TstBusFlip	PRBS9	PRBS15	TestBusSel				
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Bit	7	6	5	4	3	2	1	0
Reset Value	0	0	0	0	0	0	0	0

Tab3-104 TestSel2Reg register

Bit	Symbol	Description
7	TstBusFlip	If set to logic 1, the testbus is mapped to the parallel port by the following order: TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0. Refer to section 14 “Testsignals”.
6	PRBS9	Starts and enables the PRBS9 sequence according ITU-TO150. **Remark:** All relevant registers to transmit data have to be configured before entering PRBS9 mode. **Remark:** The data transmission of the defined sequence is started by the Transmit command.
5	PRBS15	Starts and enables the PRBS15 sequence according ITU-TO150. **Remark:** All relevant registers to transmit data have to be configured before entering PRBS15 mode. **Remark:** The data transmission of the defined sequence is started by the Transmit command.
4-0	TestBusSel	Selects the testbus. Refer to section 15 “Testsignals”.

Tab3-105 TestSel2Reg bits description

3.2.4.4 TestPinEnReg_address33h

Enable the pin output driver on D1-D4.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	RFU	TestPinEn				RFU
Access Rights	-	-	-	r/w	r/w	r/w	r/w	-
Reset Value	1	0	0	0	0	0	0	0

Tab3-106 TestPinEnReg register

Bit	Symbol	Description
7-5	RFU	Reserved for future use.
4-1	TestPinEn	Enables the output driver on the D1~D4 test pins. Example: Setting bit 1 to 1 enables D1 Setting bit 4 to 1 enables D4
0	RFU	Reserved for future use.

Tab3-107 TestPinEnReg bits description

3.2.4.5 TestPinValueReg_address 34h

Define the values for the 4-bit parallel port when it is used as I/O.

Bit	7	6	5	4	3	2	1	0
Definition	UseIO	RFU	RFU	TestPinValue				RFU
Access Rights	r/w	-	-	r/w	r/w	r/w	r/w	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-108 TestPinValueReg register

Bit	Symbol	Description
7	UseIO	Set to logic 1, this bit enables the I/O functionality for the 4-bit parallel port in case one of the serial interfaces is used. The input/output behavior is defined by TestPinEn in register

Bit	Symbol	Description
		TestPinEnReg. The value for the output behavior is defined in the bits TestPinVal.
6-5	RFU	Reserved for future use.
4-1	TestPinValue	Defines the value of the 4-bit parallel port, when it is used as I/O. Each output has to be enabled by the TestPinEn bits in register TestPinEnReg. **Remark:** Reading the register indicates the actual status of the pins D4~D1 if UseIO is set to logic 1. If UseIO is set to logic 0, the value of the register TestPinValueReg is read back.
0	RFU	Reserved for future use.

Tab3-109 TestPinValueReg bits description

3.2.4.6 TestBusReg_address 35h

Show the status of the internal testbus.

Bit	7	6	5	4	3	2	1	0
Definition	TestBus							
Access Rights	r	r	r	r	r	r	r	r
Reset Value	x	x	x	x	x	x	x	x

Tab3-110 TestBusReg register

Bit	Symbol	Description
7-0	TestBus	Shows the status of the internal testbus. The testbus is selected by the register TestSel2Reg. See section 15 “Testsignals”.

Tab3-111 TestBusReg bits description

3.2.4.7 TestCtrlReg_address 36h

Test control.

Bit	7	6	5	4	3	2	1	0
Definition	RFT	AmpRcv	RFU	RFU	RFT	RFT	RFT	RFT
Access Rights	-	r/w	-	-	-	-	-	-
Reset Value	0	1	0	0	0	0	0	0

Tab3-112 TestCtrlReg register

Bit	Symbol	Description
7	0	Reserved for production tests.
6	AmpRcv	If set to logic 1, the internal signal processing in the receiver chain is performed non-linear. This increases the operating distance in communication modes at 106 kbit/s. **Remark:** Due to the non linearity the effect of the bits MinLevel and CollLevel in the register RxThreshholdReg are as well non linear.
5-4	RFU	Reserved for future use.
3-0	RFT	Reserved for production tests.

Tab3-113 TestCtrlReg bits description

3.2.4.8 RFTReg_address 37h

Bit	7	6	5	4	3	2	1	0
Definition	RFT							
Access Rights	r	r	r	r	r	r	r	r
Reset Value	x	x	x	x	x	x	x	x

Tab3-114 RFTReg register

Bit	Symbol	Description
7-0	RFT	Reserved for production tests.

Tab3-115 RFTReg bits description

3.2.4.9 AnologTestReg_address 38h

Control the pins AUX1 and AUX2.

Bit	7	6	5	4	3	2	1	0
Definition	AnalogSelAux1				AnalogSelAux2			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	0	0	0	0	0	0

Tab3-116 AnologTestReg register

Bit	Symbol	Description	
7-4	AnalogSelAux1	Controls the AUX pin.	
3-0	AnalogSelAux2	**Remark:** All test signals are described in section 15 “Testsignals”.	
		Value	**Description**
		0000	Tristate
		0001	Output of TestDAC1 (AUX1), output of TestDAC2 (AUX2) [1]
		0010	Testsignal Corr1 [1]
		0011	Reserved
		0100	Testsignal MinLevel [1]
		0101	Testsignal ADC channel I [1]
		0110	Testsignal ADC channel Q [1]
		0111	Reserved
		1000	Testsignal for production test [1]
		1001	Reserved
		1010	HIGH
		1011	LOW
		1100	TxActive
		1101	RxActive
		1110	Subcarrier detected
		1111	TestBus-Bit as defined by the TstBusBitSel in register TestSel1Reg.

Tab3-117 AnologTestReg bits description

Remark[1]: current output. A 1k ohm pull-down resistance is suggested to plus with AUX pin.

3.2.4.10 TestDAC1Reg_address 39h

Define the testvalue for TestDAC1.

Bit	7	6	5	4	3	2	1	0
Definition	RFT	RFU	TestDAC1					
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	x	x	x	x	x	x

Tab3-118 TestDAC1Reg register

Bit	Symbol	Description
7	-	Reserved for production tests.
6	-	Reserved for future use.

Bit	Symbol	Description
5-0	TestDAC1	Defines the testvalue for TestDAC1. The output of the DAC1 can be switched to AUX1 by setting AnalogSelAux1 to 0001 in register AnalogTestReg.

Tab3-119 TestDAC1Reg bits description

3.2.4.11 TestDAC2Reg_address 3Ah

Define the testvalue for TestDAC2.

Bit	7	6	5	4	3	2	1	0
Definition	RFU	RFU	TestDAC2					
Access Rights	-	-	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	0	0	x	x	x	x	x	x

Tab3-120 TestDAC2Reg register

Bit	Symbol	Description
7	-	Reserved for future use.
6	-	Reserved for future use.
5-0	TestDAC2	Defines the testvalue for TestDAC2. The output of the DAC2 can be switched to AUX2 by setting AnalogSelAux2 to 0001 in register AnalogTestReg.

Tab3-121 TestDAC2Reg bits description

3.2.4.12 TestADCReg_address 3Bh

Show the actual value of ADC I and Q channel.

Bit	7	6	5	4	3	2	1	0
Definition	ADC_I				ADC_Q			
Access Rights	r	r	r	r	r	r	r	r
Reset Value	x	x	x	x	x	x	x	x

Tab3-122 TestADCReg register

Bit	Symbol	Description
7-4	ADC_I	Shows the actual value of ADC I channel.
3-0	ADC_Q	Shows the actual value of ADC Q channel.

Tab3-123 TestADCReg bits description

3.2.4.13 RFTReg_address 3Ch

Bit	7	6	5	4	3	2	1	0
Definition	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
Access Rights	-	-	-	-	-	-	-	-
Reset Value	1	1	1	1	1	1	1	1

Tab3-124 RFTReg register

Bit	Symbol	Description
7-0	-	Reserved for production tests.

Tab3-125 RFTReg bits description

3.2.4.14 RFTReg_address 3Dh

Bit	7	6	5	4	3	2	1	0
Definition	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-126 RFTReg register

Bit	Symbol	Description
7-0	-	Reserved for production tests.

Tab3-127 RFTReg bits description

3.2.4.15 RFTReg_address 3Eh

Bit	7	6	5	4	3	2	1	0
Definition	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	1	1

Tab3-128 RFTReg register

Bit	Symbol	Description
7-0	-	Reserved for production tests.

Tab3-129 RFTReg bits description

3.2.4.16 RFTReg_address 3Fh

Bit	7	6	5	4	3	2	1	0
Definition	RFT	RFT	RFT	RFT	RFT	RFT	RFT	RFT
Access Rights	-	-	-	-	-	-	-	-
Reset Value	0	0	0	0	0	0	0	0

Tab3-130 RFTReg register

Bit	Symbol	Description
7-0	-	Reserved for production tests.

Tab3-131 RFTReg bits description

3.2.5 Extended Register

FM17520 implements a set of extended registers by taking advantage of 0F address. Detailed extended registers accessing description refers to section 4.2 “Accessing Extended Register”.

3.2.5.1 HpdCtrl_address 0F/03h

Bit	7-6	5	4	3	2	1	0
Definition	ExMode	HPDEn	RFT				
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00	0	0	0	0	0	0

Tab3-132 HpdCtrl register

Bit	Symbol	Description
7-6	ExMode	Mode bits of extended registers. For details, see section 4.5 “Accessing Extended Register”. Configured according to different access requirements. The “00” is always back when reading them.

Bit	Symbol	Description
5	HPDEn	Low power mode control. Set to 0: chip enter into DPD mode combined with pin NPD=0, and register LPCDEn=0 (default value). Set to 1: chip enter into HPD mode combined with pin NPD=0, and register LPCDEn=0 (default value). (*When setting with HPDEn=0, LPCDEn=1, chip enter into LPCD mode.*)
4-0	RFT	Reserved for production tests. Please keep all zero.

Tab3-133 HpdCtrl bits description

3.2.5.2 UseRet_address 0F/1Bh

Bit	7-6	5	4	3	2	1	0
Definition	ExMode	RFU	UseRet	RFT			
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00	0	1	0	0	0	0

Tab3-134 UseRet register

Bit	Symbol	Description
4	UseRet	Set to 1, the retention of key registers will be excuted in HPD or LPCD mode. That can simplify the initialization when out of HPD or LPCD mode. Setting to 0 indicates the retention invalid.
3-0	RFT	Reserved for production tests. Please keep all zero.

Tab3-135 UseRet bits description

3.2.5.3 LVDctrl_address 0F/1Dh

Bit	7-6	5	4	3	2	1	0
Definition	ExMode	RFU	LVDIrq	LVDEff	LVDIe	LVDctrl	
Access Rights	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Reset Value	00	0	0	0	0	1	0

Tab3-136 LVDctrl register

Bit	Symbol	Description
4	LVDIrq	Set to 1, when there is a Low Voltage alarm. Cleared by writing 0.
3	LVDEff	Set to 0, Interrupt Request occurs when Low Voltage alarm. Set to 1, digit circuit resets when Low Voltage alarm.
2	LVDIe	Setting this bit enables LVDIrq. The LVDIrq is disabled by default.
1-0	LVDctrl	Low Voltage Detection control: 00：disable Low Voltage Detection 01：alert when lower than 1.9V 10：alert when lower than 2.1V(default value) 11：alert when lower than 2.4V

Tab3-137 LVDctrl bits description

Remark: Please hold default values for the other extended registers in different address. Or uncertain consequence may occur.

4 Host Interfaces

4.1 SPI Interface

A serial peripheral interface (SPI compatible) is supported by FM17520 to enable high-speed (up to 10Mbit/s) communication to the host. The FM17520 acts as a slave during SPI communication.
The SPI clock signal SCK must be generated by the master. Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge.

4.1.1 SPI Read Data

Reading data using SPI requires the byte order shown in Tab 4-1 to be used. The first byte sent defines both the mode and the address.

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n+1
MOSI	address 0	address 1	address 2	……	address n	00
MISO	X	data 0	data 1	……	data n-1	data n

Tab4-1 MOSI and MISO byte order

4.1.2 SPI Write Data

Writing data using SPI requires the byte order shown in Tab 4-2 to be used. The first byte sent defines both the mode and the address.

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n+1
MOSI	address 0	data 0	data 1	……	data n-1	data n
MISO	X	X	X	……	X	X

Tab4-2 MOSI and MISO byte order

4.1.3 SPI Address Byte

The first byte, defining mode and address, has to meet the following format in Tab 4-3. The MSB of the first byte defines the mode used. To read data from the FM17520 the MSB is set to logic 1. To write data to the FM17520, the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is always set to logic 0.

7（MSB）	6	5	4	3	2	1	0（LSB）
1 = read 0 = write	address						0

Tab4-3 Address byte format

4.2 Accessing Extended Register

The extended registers of FM17520 shall be accessed by two stages of address. All kinds of host interfaces can access the extended registers. The primary address is always set to 0Fh. The 6-bit secondary address can be latched by writing 0x0F register as usual. Tab 4-4 lists the byte definition of extended register at 0x0F.

7（MSB）	6	5	4	3	2	1	0（LSB）
=01	Secondary address for extended register write access						
=10	Secondary address for extended register read access						
=11	Data for extended register write access						
=00	Data for extended register read access						

Tab4-4 Byte definition of extended register

4.2.1 Write Extended Register

The procedure for writing common registers of FM17520:
1. write address of target common register, and set writing mode meanwhile
2. write data to target common register

The procedure for writing an extended register is as following 4 steps:
1. write 0F address, and set writing mode(according to SPI specification)
2. write secondary address of target extended register(01b + 6-bit secondary address)
3. write 0F address, and set writing mode(according to SPI specification)
4. write data to target extended register(11b + 6-bit data)

Fig 4-1 lists the writing flow:

Fig4-1 Extended register write progress

4.2.2 Read Extended Register

The procedure for reading common registers of FM17520:
1. write address of target common register, and set reading mode meanwhile
2. read data back from target common register

The procedure for reading an extended register is as following 4 steps:
1. write 0F address, and set writing mode(according to SPI specification)
2. write secondary address of target extended register(10b + 6-bit secondary address)
3. write 0F address, and set reading mode(according to SPI specification)
4. read data back from target extended register(00b + 6-bit data)

Fig 4-2 lists the reading flow:

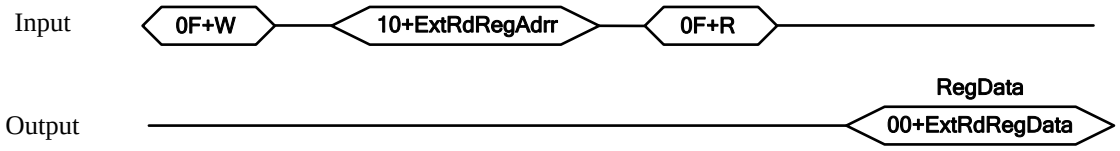


Fig4-2 Extended register read progress

5 Analog Interface And Contactless UART

5.1 General

FM17520 supports the external host online with framing and error checking of the contactless protocol requirements up to 848 kBd. It is supported thar an external circuit can be connected to the communication interface pins TIN and TOUT to modulate and demodulate the data.
The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates and processes bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.
Remarks: The size and tuning of the antenna and the power supply voltage have an important impact on the RF performance and operating distance.

5.2 TX Driver

TX1 and TX2 are both contactless RF transmitting pins. The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering. The signal on pins TX1 and TX2 can be configured using the TxControlReg register.
The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.
The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Tx1RFEn Bit	Force100ASK Bit	InvTx1RFOn Bit	InvTx1RFOff Bit	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X	X	X	X	X	X	X	not specified if RF is switched off
1	0	0	X	0	RF	pMod	nMod	100 % ASK: pin TX1pulled to logic 0,independent of theInvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

Tab5-1 Controlling signals and settings on pin TX1

Tx1RFEn Bit	Force100ASK Bit	Tx2CW Bit	InvTx2RFOn Bit	InvTx2RFOff Bit	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
0	X	X	X	X	X	X	X	X	not specified if RF is switched off
1	0	0	0	X	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X	X	RF	pCW	nCW	conductance

Tx1RF En Bit	Force100ASK Bit	Tx2 CW Bit	InvTx2 RFOn Bit	InvTx2 RFOff Bit	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
			1	X	X	RF_n	pCW	nCW	always CW forthe Tx2CW bit
	1	0	0	X	0	0	pMod	nMod	100 % ASK: pinTX2 pulledto logic 0(independent oftheInvTx2 RFOn/InvTx 2RFOff bits)
					1	RF	pCW	nCW	
			1	X	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X	X	RF	pCW	nCW	
			1	X	X	RF_n	pCW	nCW	

Tab5-2 Controlling signals and settings on pin TX2

The following abbreviations have been used in Tab 5-1 and Tab 5-2:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2.
- RF_n: inverted 13.56 MHz clock.
- GSPMos: conductance, configuration of the PMOS array.
- GSNMOS: conductance, configuration of the NMOS array.
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register.
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register.
- nCW: NMOS conductance value for continuous wave defined by the GsNRegregister's CWGsN[3:0] bits.
- nMod: NMOS conductance value for modulation defined by the GsNReg register'sModGsN[3:0] bits.
- X: do not care.

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg andGsNReg registers are used for both drivers.

5.3 Serial Data Switch

The analog front end and digital processing block of FM17520 can both connected with external signals by pins Tin and Tout. The TIN pin is capable of processing external digital signals on transfer speeds above 424 kbps. And internal signals can be output through TOUT pin. This function allows the analog front end of the FM17520 to be connected to the digital block of another device.
The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

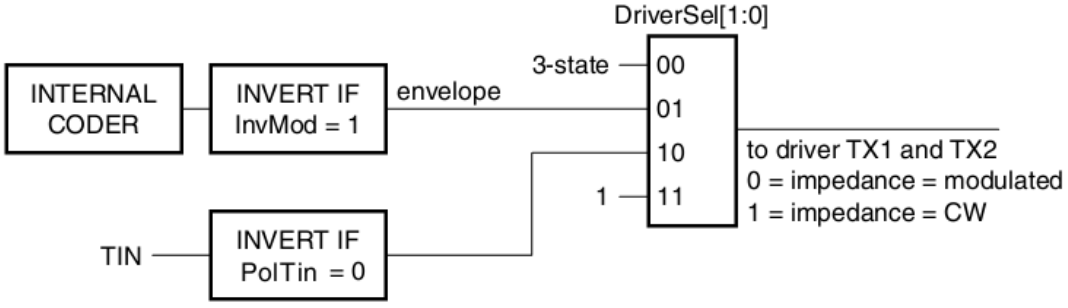


Fig5-1 Serial data switch for TX1 and TX2

6 CRC Coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16}+x^{12}+x^5+1$
- The CRCResultReg register indicates the resultof the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

Tab6-1 CRC coprocessor parameters

7 FIFO Buffer

FM17520 implements an 8*64 bit FIFO buffer.It buffers the input and output data streambetween the host and the FM17520's internal state machine. This makes it possible tomanage data streams up to 64 bytes long without the need to take timing constraints intoaccount.

7.1 Accessing FIFO Buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register.Writing to this register stores one byte in the FIFO buffer and increments the internal FIFObuffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and increments the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelRegregister.
When the microcontroller starts a command, the FM17520 can, while the command is inprogress, access the FIFO buffer according to that command. The microcontrollermustensure that there are not any unintentional FIFO buffer accesses.

7.2 Controlling FIFO Buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bitto logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorRegregister's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longeraccessible allowing the FIFO buffer to be filled with another 64 bytes.

7.3 FIFO Buffer Status Information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0].
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit.
- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit.
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bitcan only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The FM17520 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ whenStatus1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ whenStatus1Reg register's HiAlert bit changes to logic 1.

If the number of remaining bytes in FIFO buffer equals to or be less than the one defined by WaterLevel register, the HiAlert bit will be set. It is generated according to following equation:

$$HiAlert = (64 - FIFOLength) \leqslant WaterLevel$$

If the number of written bytes in FIFO buffer equals to or be less than the one defined by WaterLevel register, the LoAlert bit will be set. It is generated according to following equation:

$$LoAlert = FIFOLength \leqslant WaterLevel$$

8 Interrupt Request System

The FM17520 indicates certain events by setting the Status1Reg register's IRq bit and, ifactivated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

8.1 Interrupt Sources Overview

Tab 8-1 shows the available interrupt bits, the corresponding source and the condition for its activation.

Interrupt Flag	Interrupt Source	Trigger Action
TimerIRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

Tab8-1 Interrupt sources

The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt setby the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the statechanges from sending data to transmitting the end of the frame pattern, the transmitterunit automatically sets the interrupt bit.

The CRC coprocessor sets the DivIrqRegregister's CRCIRq bit after processing all the FIFO buffer data which is indicated byCRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the receiveddata is detected.

The ComIrqReg register's IdleIRq bit is set if a command finishes andthe Command[3:0] value in the CommandReg register changes to Idle.

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register'sHiAlert bit is set to logic 1 which means that the FIFO buffer has reached the levelindicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register'sLoAlert bit is set to logic 1 which means that the FIFO buffer has reached the levelindicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UARTduring send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

9 Timer

FM17520 implements a timer unit internally. The external host controller may use the timer to manage timing relevant tasks. The timer unit may work in one of the following modes:

- Time-out counter
- Watch-dog counter
- Stop watch
- Programmable one-shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events which will be explained in the following, but the timer itself does not influence any internal event (e.g. A time-out during data reception does not influence the reception process automatically). Furthermore, several timer-related bits are set and these bits can be used to generate an interrupt.

Timer

The timer has an input clock of 13.56 MHz (derived from the 27.12 MHz quartz). The timer consists of two stages: 1 prescaler and 1 counter.

The prescaler is a 12-bit counter. The reload value for TPrescaler can be defined between0 and 4095 in register TModeReg and TPrescalerReg.

The reload value for the counter is defined by 16 bits in a range of 0 to 65535 in the register TReloadReg.

The current value of the timer is indicated by the register TCounterValReg.

If the counter reaches 0 an interrupt will be generated automatically indicated by settingthe TimerIRq bit in the register CommonIRqReg. If enabled, this event can be indicated on
the IRQ line. The bit TimerIRq can be set and reset by the host controller. Depending on the configuration the timer will stop at 0 or restart with the value from register TReloadReg.

The status of the timer is indicated by bit TRunning in register Status1Reg.

The timer can be manually started by TStartNow in register ControlReg or manually stopped by TStopNow in register ControlReg.

Furthermore the timer can be activated automatically by setting the bit TAuto in theregister TModeReg to fulfill dedicated protocol requirements automatically.

The time delay of a timer stage is the reload value +1.

The definition of total time is:

t = ((TPrescaler*2+1)*TReload+1)/13.56MHz，

Maximum time:TPrescaler = 4095，TReloadVal = 65535

=>tmax =(2*4095+1)*65536/13.56 MHz = 39.59s

Example:

To indicate 25 us it is required to count 339 clock cycles. This means the value for TPrescaler has to be set to TPrescaler = 169. The timer has now an input clock of 25 us.The timer can count up to 65535 timeslots of each 25 μ s.

10 Power Reduction Modes

FM17520 supports three power reduction modes and can adapt to different power requirements:

- ✧ Deep Power Down mode
- ✧ Hard Power Down mode
- ✧ Soft Power Down mode

10.1 Deep Power Down

The Deep Power Down mode of FM17520 turns off all digital circuit's supply and the oscillator. All bi-directional I/O pins are set to three-state output, while all input pins are separated from internal circuit.

FM17520 will get into DPD mode when the pad NPD pulled down if bit5 of extended register at 0F/03h is 0 (default value). The device exited DPD mode automatically after the NPD turns HIGH. Then all of configuration and initialization need to be reset.

10.2 Hard Power Down

The Hard Power Down mode of FM17520 turns off the oscillator and the supply of most digital circuit. All bi-directional I/O pins are set to three-state output. All input pins are separated from internal circuit.

FM17520 will get into HPD mode when the pad NPD pulled down if bit5 of extended register at 0F/03h is 1. FM17520 provides data retention for key registers under HPD mode. And when exit from HPD mode, FM17520 will resume all these key registers automatically. For details of retention registers, see section 10.2.1 "Data Retention in HPD Mode".

When exit HPD mode, re-initialization is necessary, if the data retention function is disabled (set bit4 of UseRet register 0F/1Bh to 0).

10.2.1 Data Retention in HPD Mode

The 25-byte data of internal buffer related to Mem command will keep unchanged under HPD mode, no matter the data retention function is enabled or not.

The key registers FM17520 provides in data retention function :

Register	Address	Retention bit	
CommIEnReg	02h	7	IRqInv
		6	TxIEn
		5	RxIEn
		4	IdleIEn
		3	HiAlertIEn
		2	LoAlertIEn
		1	ErrIEn
		0	TimerIEn
DivIEnReg	03h	7	IRQPushPull
		4	TinActIEn
		2	CRCIEn
CollReg	0Eh	7	ValuesAfterColl
TxModeReg	12h	7	TxCRCEn
		3	InvMod
RxModeReg	13h	7	RxCRCEn
		3	RxNoErr
		2	RxMuliple

Register	Address	Retention bit	
TxASKReg	15h	6	Force100ASK
RxSelReg	17h	5:0	RxWait
RxThresholdReg	18h	7:4	MinLevel
		2:0	CollLevel
DemodReg	19h	7:6	AddIQ
		5	FixIQ
		3:2	TauRcv
		1:0	TauSync
ModWidthReg	24h	7:0	ModWidth
RFCfgReg	26h	6:4	RxGain[2:0]
GsNReg	27h	7:4	CWGsN
		3:0	ModGSN
CWGsPReg	28h	5:0	CWGsP
ModGsPReg	29h	5:0	ModGsP[5:0]
TModeReg	2Ah	7	TAuto
		6:5	Tgated
		4	TAutoRestart
		3:0	Tprescaler_Hi
TPrescalerLoReg	2Bh	7:0	TPrescaler_Lo
TreloadValHiReg	2Ch	7:0	TReloadVal_Hi
TReloadValLoReg	2Dh	7:0	TReloadVal_Lo

Tab10-1 List of retention registers in HPD mode

10.3 Soft Power Down

FM17520 enters Soft Power-down mode immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input and output pins do not change their state during SPD mode. Meanwhile, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediatelly clear it. It is cleared automatically by the FM17520 when Soft Power-down mode is exited.

10.4 Transmitter Off Mode

In Transmitter Off mode, FM17520 switchs off the internal antenna drivers thereby, turning off the RF field. The Transmitter Off mode is entered by setting the TxControlReg register's Tx1RFEn bit and Tx2RFEn bit to logic 0.

11 Low Voltage Detection

FM17520 could detect supply's voltage and alarm when its voltage is low enough. The monitoring voltage can be configured by setting the LVDctrl register. As default, interrupt and alarm will occur when AVDD voltage is once lower than the monitoring one. The LVDctrl register can also be configured as low voltage reset mode. But that mode will limit the minimum operating voltage.

12 Oscillator Circuitry

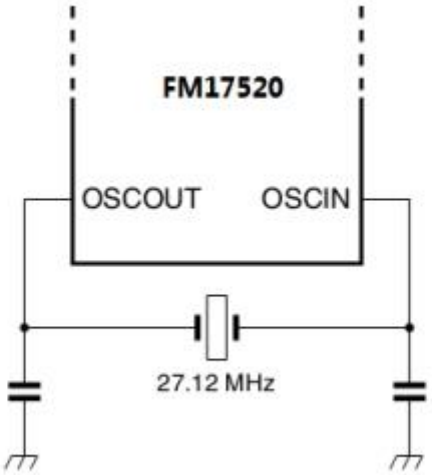


Fig12-1 Quartz crystal connection

The FM17520's clock provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

13 Reset And Oscillator Start-Up Time

13.1 Reset Timing Requirements

The reset signal is filtered bya spike filter before it enters thedigital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset,the signal must be LOW for at least 100 ns.

13.2 Oscillator Start-Up Time

If the FM17520 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the FM17520 depends on the oscillatoruesd and is shown in Fig 13-1.

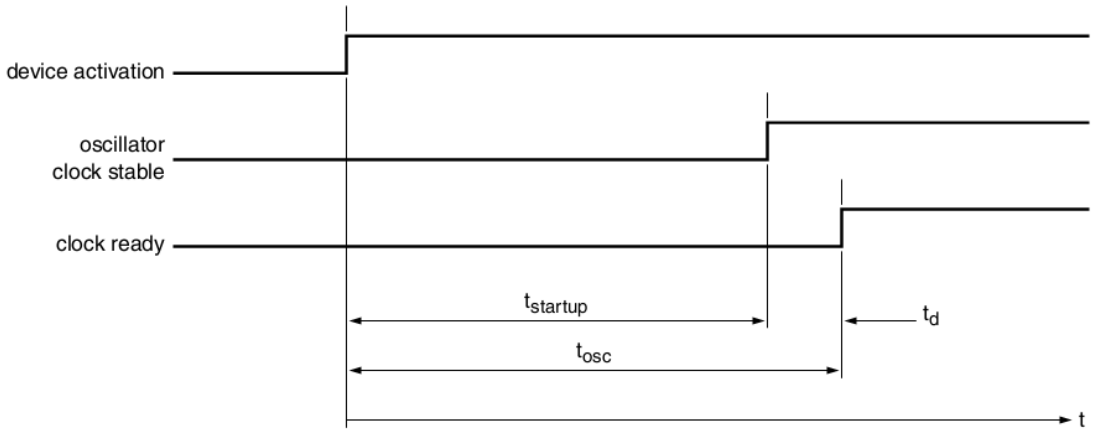


Fig13-1 Oscillator start-up time

The time（tstartup） is the start-up time of the crystal oscillator circuit. The crystal oscillator start-uptime is defined by the crystal.

The time（td） is the internal delay time of the FM17520 when the clock signal is stable before the FM17520 can be addressed.

The delay time is：

td = 1024/(27.12MHz) = 37.76 μ s

The time（tOSC） is the sum of td and tstartup.

14 Command Set

14.1 General Description

The FM17520 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code to the CommandReg register.
Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

14.2 General Behavior

- Each command that needs a data bit stream(or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts procession only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

14.3 FM17520 Command Overview

Command	Command Code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
-	1101	reserved for future use
Authent	1110	performs the M1 standard authentication as a reader
SoftReset	1111	resets FM17520

Tab14-1 Command overview

14.3.1 IDLE

Place the FM17520 in Idle mode. The Idle command also terminates itself.

14.3.2 Mem

Transfer 25 bytes from the FIFO buffer to the internal buffer.
To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.
During a hard power-down, the 25 bytes in the internal buffer remain unchanged and are lost when in DPD mode or the power supply is removed from the FM17520.
This command automatically terminates when finished and the Idle command becomes active.

14.3.3 Generate RandomID

This command generates a 10-byte random number and then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the FM17520 returns to Idle mode.

14.3.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.
The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded into the CRC coprocessor when the command starts.
This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

14.3.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Beforetransmitting the FIFO buffer content, all relevant registers must be set for datatransmission.
This command automatically terminates when the FIFO buffer is empty. It can beterminated by another command written to the CommandReg register.

14.3.6 NoCmdChange

This command does not influence any running command in the CommandReg register. Itcan be used to manipulate any bit except the CommandReg register Command[3:0] bits,for example, the RcvOff bit or the PowerDown bit.

14.3.7 Receive

The FM17520 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.
This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.
Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

14.3.8 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.
Each transmit process must be started by setting the BitFramingReg register's StartSendbit to logic 1. This command must be cleared by writing any command to the CommandReg register.
Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

14.3.9 Authent

This command manages M1 authentication to enable a secure communication to any M1 Mini, M1 1K and M1 4K card. The following data is written to theFIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes are written into the FIFO.
Remark: When the Authent command is active, all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.
This command automatically terminates when the M1 card is authenticated and theStatus2Reg register's Crypto1On bit is set to logic 1.
This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, theTimerIRq bit can be used as the termination criteria. During authentication processing, theRxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination ofthe Authent command, either after processing the protocol or writing Idle to the CommandReg register.
If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set tologic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

14.3.10 SoftReset

This command performs a reset of the FM17520. The 25-bytes configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

15 Testsignals

15.1 Testbus

The testbus is implemented for production test purposes. The following configuration can be used to improve the design of a system using the FM17520. The testbus allows to route internal signals to the digital interface. The testbus signals are selected by accessing TestBusSel in register TestSel2Reg.

Pins	D6	D5	D4	D3	D2	D1
Testsignal	sdata	scoll	svalid	sover	RCV_reset	RFU

Tab15-1 Testsignal routing (TestSel2Reg = 07h)

Pins	Testsignal	Description
D6	sdata	shows the actual received data stream
D5	scoll	shows if in the actual bit a collision has been detected (106 kbit/s only)
D4	svalid	shows if sdata and scoll are valid
D3	sover	shows that the receiver has detected a stop condition (ISO/IEC 14443A mode only)
D2	RCV_reset	shows if the receiver is reset
D1	RFU	-

Tab15-2 Testsignals description

Pins	D6	D5	D4	D3	D2	D1
Testsignal	clkstable	clk27/8	RFU	RFU	clk27	RFU

Tab15-3 Testsignal routing (TestSel2Reg = 0Dh)

Pins	Testsignal	Description
D6	clkstable	shows if the oscillator delivers a stable signal
D5	clk27/8	shows the output signal of the oscillator divided by 8
D4	RFU	-
D3	RFU	-
D2	clk27	shows the output signal of the oscillator
D1	RFU	-

Tab15-4 Testsignals description

Pins	D6	D5	D4	D3	D2	D1
Testsignal	RFU	TRunning	RFU	RFU	RFU	RFU

Tab15-5 Testsignal routing (TestSel2Reg = 19h)

Pins	Testsignal	Description
D6	RFU	-
D5	TRunning	TRunning stops 1 clock cycle after TimerIRQ is raised
D4	RFU	-
D3	RFU	-
D2	RFU	-
D1	RFU	-

Tab15-6 Testsignals description

15.2 Testsignals at pin AUX1/AUX2

SelTest	Description for AUX1/AUX2
0000	Tristate
0001	DAC: register TestDAC 1/2
0010	DAC: testsignal corr1
0011	RFU
0100	DAC: testsignal MinLevel
0101	DAC: ADC_I
0110	DAC: ADC_Q
0111	RFU
1000	RFU
1001	RFU
1010	High
1011	Low
1100	TxActive
1101	RxActive
1110	Subcarrier detected
1111	TstBusBit

Tab15-7 Testsignals description

Each signal can be switched to pin AUX1 or AUX2 by setting SelAux1 or SelAux2 in the register AnalogTestReg.

Remark: The DAC has a current output, it is recommended to use a 1 k ohm pull-down resistance at pins AUX1/AUX2.

15.3 PRBS

Enables the PRBS9 or PRBS15 sequence according to ITU-TO150. To start the transmission of the defined data stream the Transmit command has to be activated. The preamble/Sync byte/start bit/parity bit are generated automatically depending on the selected mode.

Remark: All relevant register to transmit data have to be configured before entering PRBS mode according ITU-TO150.

16 Typical Application Diagram

The figure below shows a typical application diagram based on FM17520.

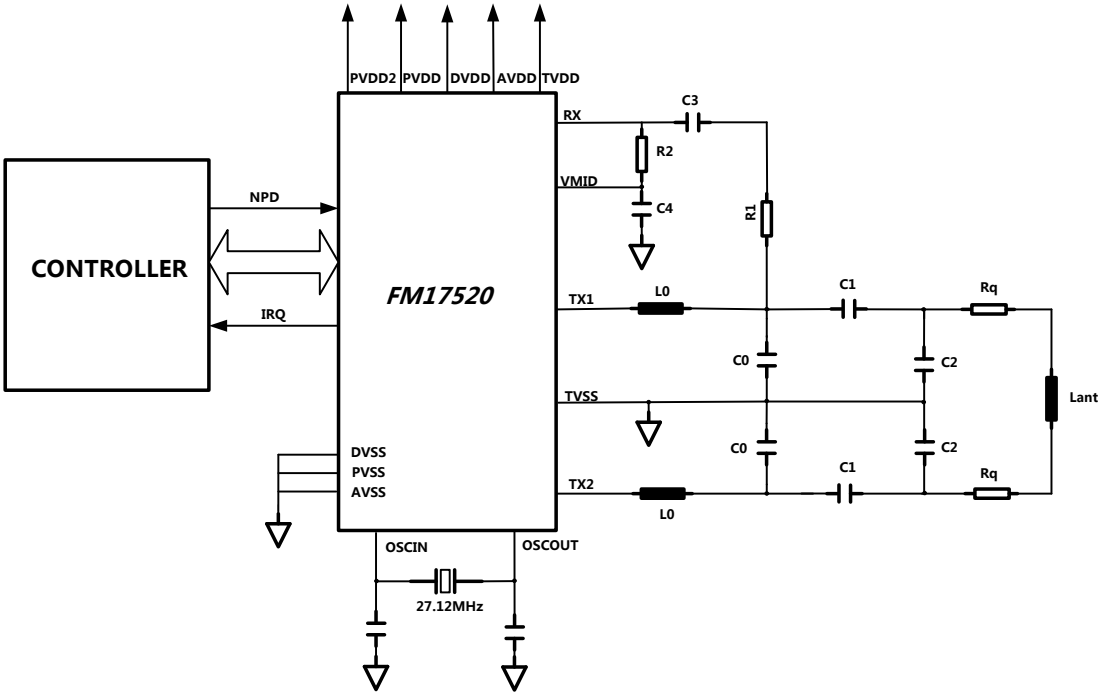


Fig16-1 Typical application diagram

17 Characteristics

17.1 Limiting Values

Parameter	Min	Max	Unit
Storage temperature	-40	+85	°C
AVDD, DVDD, TVDD,PVDD,PVDD2	-0.5	4.0	V
ESD（HMB）		2	KV
ESD（CDM）		500	V

Tab17-1 FM17520 limiting values

***Remark:** Any conditions beyond the limiting values will bring permanent damage to the device.

17.2 Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AVDD	analog supply	$V_{PVDD} \leqslant V_{AVDD}=V_{DVDD} \leqslant V_{TVDD}$	2.2	3.0	3.6	V
DVDD[1]	digital supply	$V_{PVDD} \leqslant V_{AVDD}=V_{DVDD} \leqslant V_{TVDD}$	2.2	3.0	3.6	V
TVDD[2]	transmitter supply	$V_{PVDD} \leqslant V_{AVDD}=V_{DVDD} \leqslant V_{TVDD}$	2.2	3.0	3.6	V
PVDD[3]	pin supply	$V_{PVDD} \leqslant V_{AVDD}=V_{DVDD} \leqslant V_{TVDD}$	1.62		3.6	V
PVDD2[4]	test pin supply		1.62		3.6	V
I_{DPD}	Deep power-down current	AVDD=DVDD=TVDD=PVDD=3V; NPD=0, get into DPD mode		1	10	uA
I_{HPD}	Hard power-down current (register retention)	AVDD=DVDD=TVDD=PVDD=3V; NPD=0, get into HPD mode		2	12	uA
I_{SPD}	Soft power-down current	AVDD=DVDD=TVDD=PVDD=3V; get ino SPD mode		35	60	uA
I_{AVDD}	operating current	AVDD=3V; enable receiver(RcvOff bit=0)		10	13	mA
		AVDD=3V; disable receiver(RcvOff bit=1)		6	8	mA
I_{TVDD}[5]	RF operating current	transmitting carrier wave continuously; V_{TVDD} =3.0V		60	100	mA
T_A	ambient temperature		-40		+85	°C

Tab17-2 Recommended operating conditions for FM17520

[1] AVDD must be equal to DVDD .
[2] TVDD must be the same or higher voltage than AVDD.
[3] PVDDmust always be the same or lower voltage thanAVDD.
[4] PVDD2 should be the same voltage to PVDD as a proposal.
[5] I_{TVDD}depends on TVDD voltage and the configured parameter of antenna network. The I_{TVDD}can be controlledsmaller than 100mA, or even larger to get a longer RF operating distance, by configuring different antenna network based on different application requirements.
[6] I_{DPD}/I_{HPD}/I_{SPD} are currents consumed by the whole chip in corresponding modes.

17.2.1 SPI AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WL}	pulse width LOW	line SCK	50			ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WH}	pulse width HIGH	line SCK	50		25	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI	25			ns
$t_{SU(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK	25			ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO			25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time		0			ns
t_{NHNL}	NSS high before communication		50			ns

Tab17-3 SPI AC characteristics

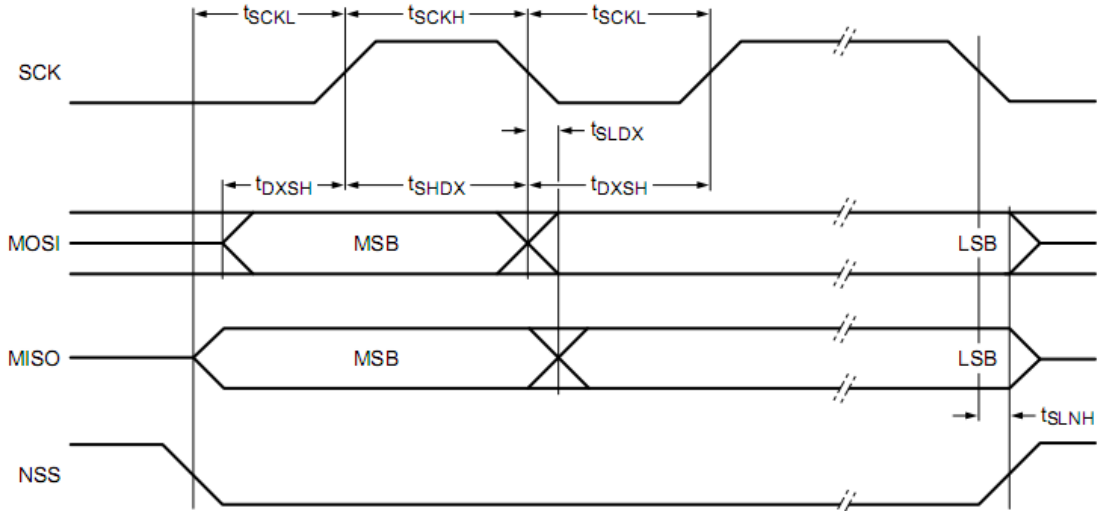


Fig17-1 Timing diagram for SPI

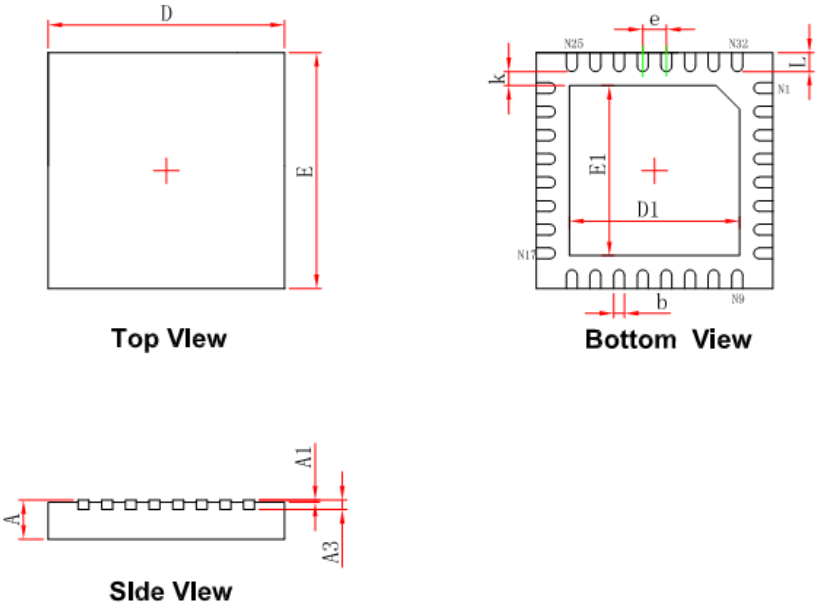
Remark: The signal NSS must be LOW to be able to send several bytes in one data stream.To send more than one data stream, the NSS must be set HIGH between the data streams.

18 Ordering Information

Device Number	Package	Wrap	Operating Environment
FM17520-QNA-A-G	QFN32	Tray	Industrial Temperature (-40℃ ~ +85℃)

19 Package Information

19.1 QFN32 Package Outline



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

Fig19-1 FM17520 QFN32 Package Outline

Revision History

Rev	Release Date	Pages	Chapters/Tables/Figures	Modifications
1.0	Oct.2016	69		Initial Release.

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FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The device has been evaluated to meet general RF exposure requirement. The device can be used in portable exposure condition without restriction.

If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains Transmitter Module FCC ID:2AWVZ-JL500N Or ContainsFCC ID: 2AWVZ-JL500N”

When the module is installed inside another device, the user manual of the host must contain below warning statements;

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference.

(2) This device must accept any interference received, including interference that may cause undesired operation.

2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.

Any company of the host device which install this modular with limit modular approval should perform the test of radiated emissionand spurious emission according to FCC part 15C : 15.247 and 15.209 requirement,Only if the test result comply with FCC part 15C : 15.247 and 15.209 requirement，then the host can be sold legally.