

# **Maverick 220**

# **EDM-XDLTEG**

**Data sheet**

## Document information

This document defines the module reference design and its air and hardware interfaces for customer applications. It can help customers quickly understand the hardware interface specifications, electrical characteristics, mechanical specifications, and other related information of the EDM-XDLTEG module reference design. With the assistance of this document, coupled with application manuals and user guides, customers can quickly apply the EDM-XDLTEG module reference design to wireless applications.

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# Table of contents

## 内容

|                                            |    |
|--------------------------------------------|----|
| <b>Data sheet</b>                          | 1  |
| Document information                       | 2  |
| Table of contents                          | 3  |
| 1. Functional description                  | 5  |
| 1.1. Overview                              | 5  |
| 1.2. Product features                      | 5  |
| 1.3. Functional block diagram              | 9  |
| 2. Interfaces                              | 10 |
| 2.1 Pin assignment                         | 10 |
| 2.2 Pin description                        | 11 |
| 2.3 Power supply design                    | 18 |
| 2.4 Power supply reference circuit         | 18 |
| 2.5 Power on/off                           | 20 |
| 2.6 Reset module                           | 21 |
| 2.7 Serial port                            | 22 |
| 2.8 SPI interface                          | 27 |
| 2.9 USIM interface                         | 28 |
| 2.10 ADC interface                         | 29 |
| 2.11 Network status indicator              | 30 |
| 2.12 Module status indicator               | 31 |
| 3. Antenna interface                       | 32 |
| 3.1 Pin definition                         | 32 |
| 3.2 Operating frequency                    | 33 |
| 3.3 RF antenna reference circuit           | 34 |
| 3.4 RF signal cable layout reference guide | 35 |
| 3.5 Antenna requirements                   | 37 |
| 3.6 RF output power                        | 37 |
| 3.7 RF receive sensitivity                 | 40 |
| 4. Electrical performance and reliability  | 42 |
| 4.1 Operating and storage temperature      | 42 |
| 4.2 Static protection                      | 43 |
| 5. Mechanical dimensions                   | 44 |
| 5.1 Module mechanical size                 | 44 |
| 5.2 Module top view / bottom view          | 46 |
| 6 FCC statement                            | 47 |
| 6.1 Radiation exposure statement           | 47 |
| 6.2 End product labeling                   | 48 |
| 6.3 Manual information to the end user     | 48 |
| Appendix A Terminology abbreviations       | 49 |
| Revision history                           | 52 |
| Contact                                    | 52 |

# 1. Functional description

## 1.1. Overview

EDM-XDLTEG is an LTE-M/NB-IoT module that supports the ISM Band, Band103, Band 106 and Band 107, which have been standardized by 3GPP for LTE-M/NB-IoT. These bands are utilized in various industries, including energy, electric and gas utilities, transportation, and others.

The module's compact size (26.5 mm \* 26.5 mm \* 2.3 mm), LCC package, and wide power supply range make it easily embeddable and compatible with a wide range of applications.

EDM-XDLTEG is a high-performance LTE Cat M/NB1 module with ultra-low power consumption compliant with 3GPP release 13. It supports a wide range of IP-based protocols, including UDP, TCP, CoAP, LwM2M, MQTT, TLS, DTLS, SNTP and HTTP. EDM-XDLTEG is a power-optimized product that delivers 10+ years of device's battery life.

EDM-XDLTEG, with its advanced feature set is recommended for developing new long-range, low-power IoT applications, as well as for migrating from other legacy cellular or unlicensed technologies, for industries such as utilities, smart grids, AML, transportation, and others.

## 1.2. Product features

The EDM-XDLTEG module reference design is a high-performance, low-power NB-IoT series module. Through the NB-IoT radio communication protocol (3GPP Release 13), the EDM-XDLTEG module can establish communication with the network operator's infrastructure equipment.

The frequency bands supported by the EDM-XDLTEG module are displayed in the table below.

| Duplex mode | Band    | Frequency band |              |
|-------------|---------|----------------|--------------|
|             |         | Downlink (MHz) | Uplink (MHz) |
| HD-FDD      | 106     | 936.5~939.5    | 896.5~900.5  |
| HD-FDD      | ISM-FDD | 925~928        | 902~915      |

Table 1: Frequency bands supported by the module

The table below describes the main characteristics of the EDM-XDLTEG module in detail.

| Description           | Value                                                  |
|-----------------------|--------------------------------------------------------|
| Physical properties   | 26.5 mm * 26.5 mm * 2.3 mm (1.04 * 1.04 * 0.09 inches) |
| Application processor | Cortex R4<br>Cache: 32KB                               |
| Working voltage       | 3.5 – 4.1 V, typical voltage: 3.8 V                    |

| Description              | Value                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Baseline Standard        | 3GPP Release 13, HD-FDD/FDD & TDD                                                                                                                                                                                                                                                                                                                                                                                                      |
| UE category              | CAT-M1 and CAT-NB1                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Bandwidth                | 1.4 MHz (CAT-M1), 200KHz (CAT-NB1)                                                                                                                                                                                                                                                                                                                                                                                                     |
| Modulation               | Uplink : QPSK/16QAM (CAT-M1), BPSK/QPSK (CAT-NB1)<br>Downlink : QPSK/16QAM (CAT-M1), QPSK (CATNB1)                                                                                                                                                                                                                                                                                                                                     |
| Application interface    | <ul style="list-style-type: none"> <li>✓ Standard SIM interface, support 3.0V/1.8V, support hot-swapping function</li> <li>✓ USB 2.0 (high-speed)</li> <li>✓ Hardware reset interface</li> <li>✓ UART serial interface</li> <li>✓ PCM &amp; I2C interface</li> <li>✓ Power interface</li> <li>✓ Network status indication interface</li> <li>✓ GPIO interface</li> <li>✓ ADC</li> <li>✓ GPIO</li> <li>✓ SPI</li> <li>✓ SDIO</li> </ul> |
| Operating frequency band | B106/ISM-FDD                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Satellite positioning    | GPS, QZSS, DGPS(RTCM) and A-GPS                                                                                                                                                                                                                                                                                                                                                                                                        |
| GNSS Interface           | GNSS antenna interface                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Operating temperature    | Normal operating temperature -30°C to +85°C (-22°F to +185°F)                                                                                                                                                                                                                                                                                                                                                                          |
| AT command               | Supports standard AT Command (3GPP TS 27.007.27.005)                                                                                                                                                                                                                                                                                                                                                                                   |

Table 2: Main characteristics of the EDM-XDLTEG module

#### NOTICE!

- The EDM-XDLTEG module is recommended to operate within a temperature range of -30°C to +75°C. It is advisable for the application terminal to implement temperature control measures in harsh environments. Additionally, certain RF performance parameters may exceed their limits under extreme temperatures. Therefore, it is recommended to store the module within a specified temperature range.

- When the temperature falls within the range of  $-40^{\circ}\text{C}$  to  $-30^{\circ}\text{C}$  or  $+75^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , some RF specifications of the EDM-XDLTEG module may not comply with 3GPP standards.

### 1.3. Functional block diagram

The following figure is a functional block diagram illustrating the main functions of the design:

- RF part
- Baseband part
- Power management
- Peripheral interface



- PSM
- Power supply
- RESET
- CHIP\_ENB
- WAKE\_UP
- Serial port
- SPI interface
- USIM interface
- ADC interface<sup>1</sup>

v.1.0

- Network Status Indicator<sup>2</sup>
- Antenna interface

## 2.1 Pin assignment

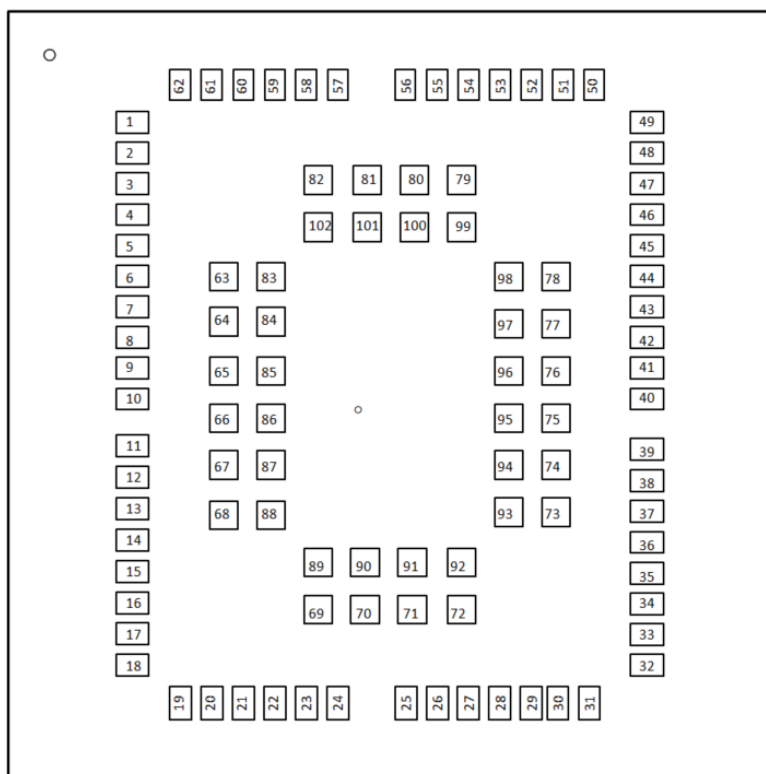


Figure 2: Pin assignment diagram<sup>3</sup>

## 2.2 Pin description

The following table describes the pin definitions of the EDM-XDLTEG module in detail.

| Type | Description              |
|------|--------------------------|
| IO   | Two-way input and output |
| DI   | Digital input            |
| DO   | Digital output           |
| PI   | Power input              |
| PO   | Power output             |

<sup>2</sup>Under development

<sup>3</sup>Leave all reserved pins open

| Type | Description   |
|------|---------------|
| AI   | Analog input  |
| AO   | Analog output |

Table 3: I/O parameter definitions

| Power supply |                                                        |     |                              |                                                 |
|--------------|--------------------------------------------------------|-----|------------------------------|-------------------------------------------------|
| Pin name     | Pin number                                             | I/O | Description                  | Remarks                                         |
| VBAT_BB      | 32, 33                                                 | PI  | Baseband power supply        | V max = 4.1 V<br>V min = 3.5 V<br>V typ = 3.8 V |
| VBAT_RF      | 52, 53                                                 | PI  | Radio frequency power supply | V max = 4.1 V<br>V min = 3.5 V<br>V typ = 3.8 V |
| VDD_EXT      | 29                                                     | PO  | 1.8 V output power supply    | V typ = 1.8 V                                   |
| GND          | 3,31,48,50,54,55,58,59,61,62,67-74,79-82,89-91,100-102 | GND | Ground                       |                                                 |

| Power on/off interface |            |     |                                                                                  |                                                          |
|------------------------|------------|-----|----------------------------------------------------------------------------------|----------------------------------------------------------|
| Pin name               | Pin number | I/O | Description                                                                      | Remarks                                                  |
| PWRKEY                 | 15         | DI  | Power on/off signal from Microprocessor, internal pull low to AGND. Active-high. | V <sub>IL</sub> max = 0.5V<br>V <sub>IH</sub> min = 1.4V |

| Reset interface |            |     |             |         |
|-----------------|------------|-----|-------------|---------|
| Pin name        | Pin number | I/O | Description | Remarks |

### Reset interface

|         |    |    |                 |                                                          |
|---------|----|----|-----------------|----------------------------------------------------------|
| RESET_N | 17 | DI | Power-on-Resets | V <sub>IL</sub> max = 0.6V<br>V <sub>IH</sub> min = 1.2V |
|---------|----|----|-----------------|----------------------------------------------------------|

### USB interface

| Pin name | Pin number | I/O | Description               | Remarks |
|----------|------------|-----|---------------------------|---------|
| USB_VBUS | 8          | PI  | USB VBUS                  |         |
| USB_DP   | 9          | IO  | USB differential signal + |         |
| USB_DM   | 10         | IO  | USB differential signal - |         |

### UART interface

| Pin name  | Pin number | I/O | Description          | Remarks              |
|-----------|------------|-----|----------------------|----------------------|
| UART0_RXD | 34         | DI  | Data reception       | 1.8 V voltage domain |
| UART0_TXD | 35         | DO  | Data transmission    | 1.8 V voltage domain |
| UART0_CTS | 36         | DO  | UART clear to send   | 1.8 V voltage domain |
| UART0_RTS | 37         | DI  | UART request to send | 1.8 V voltage domain |

### UART interface for Debug serial port

| Pin name  | Pin number | I/O | Description       | Remarks              |
|-----------|------------|-----|-------------------|----------------------|
| UART1_TXD | 27         | DO  | Data transmission | 1.8 V voltage domain |
| UART1_RXD | 28         | DI  | Data reception    | 1.8 V voltage domain |

### UART interface for Debug serial port

|           |    |    |                   |                      |
|-----------|----|----|-------------------|----------------------|
| UART2_TXD | 23 | DO | Data transmission | 1.8 V voltage domain |
| UART2_RXD | 22 | DI | Data reception    | 1.8 V voltage domain |

### USIM interface

| Pin name  | Pin number | I/O | Description            | Remarks   |
|-----------|------------|-----|------------------------|-----------|
| USIM_VDD  | 43         | PO  | USIM card power supply | 1.8V / 3V |
| USIM_RST  | 44         | DO  | USIM card reset        |           |
| USIM_DATA | 45         | IO  | USIM card data         |           |
| USIM_CLK  | 46         | DO  | USIM card clock        |           |

### GPIO interface

| Pin name | Pin number | I/O | Description                 | Remarks              |
|----------|------------|-----|-----------------------------|----------------------|
| GPIO1    | 11         | IO  | General input / output port | 1.8 V voltage domain |
| GPIO2    | 12         | IO  | General input / output port | 1.8 V voltage domain |
| GPIO3    | 13         | IO  | General input / output port | 1.8 V voltage domain |

### GPIO interface

|       |    |    |                             |                      |
|-------|----|----|-----------------------------|----------------------|
| GPIO4 | 14 | IO | General input / output port | 1.8 V voltage domain |
| GPIO5 | 25 | IO | General input / output port | 1.8 V voltage domain |
| GPIO6 | 26 | IO | General input / output port | 1.8 V voltage domain |
| GPIO7 | 64 | IO | General input / output port | 1.8 V voltage domain |
| GPIO8 | 65 | IO | General input / output port | 1.8 V voltage domain |

### Network Indication interface

| Pin name  | Pin number | I/O | Description               | Remarks              |
|-----------|------------|-----|---------------------------|----------------------|
| NETLIGHT  | 21         | DO  | Network status indication | 1.8 V voltage domain |
| W_DISABLE | 18         | I   | FLIGHT MODE               | 1.8 V voltage domain |

### Module status interface

| Pin name | Pin number | I/O | Description                       | Remarks              |
|----------|------------|-----|-----------------------------------|----------------------|
| STATUS   | 20         | DO  | Module power on status indication | 1.8 V voltage domain |

### PCM interface

| Pin name | Pin number | I/O | Description         | Remarks |
|----------|------------|-----|---------------------|---------|
| PMC_CLK  | 4          | DI  | PCM bit clock pulse |         |

### PCM interface

|          |   |    |                            |  |
|----------|---|----|----------------------------|--|
| PCM_SYNC | 5 | DI | PCM Frame sync clock pulse |  |
| PCM_IN   | 6 | DI | PCM data input             |  |
| PCM_OUT  | 7 | DO | PCM data output            |  |

### I2C interface

| Pin name | Pin number | I/O | Description             | Remarks              |
|----------|------------|-----|-------------------------|----------------------|
| I2C_SCL  | 40         | IO  | I2C serial clock        | 1.8 V voltage domain |
| I2C_SDA  | 41         | IO  | I2C serial address/data | 1.8 V voltage domain |

### ADC interface

| Pin name | Pin number | I/O | Description                             | Remarks |
|----------|------------|-----|-----------------------------------------|---------|
| ADC1     | 2          | AI  | Analog to digital converter interface 1 |         |
| ADC0     | 24         | AI  | Analog to digital converter interface 0 |         |

### CAN interface

| Pin name | Pin number | I/O | Description       | Remarks |
|----------|------------|-----|-------------------|---------|
| 83       | CAN_TX     |     | CAN Transmitter   |         |
| 84       | CAN_RX     |     | CAN Receiver      |         |
| 85       | CAN_CTRL1  |     | CAN Control pin 1 |         |

### CAN interface

|    |           |  |                   |  |
|----|-----------|--|-------------------|--|
| 86 | CAN_CTRL0 |  | CAN Control pin 0 |  |
|----|-----------|--|-------------------|--|

### SPI interface

| Pin name | Pin number | I/O | Description               | Remarks |
|----------|------------|-----|---------------------------|---------|
| 94       | SPI_MISO   | DI  | Master input slave output |         |
| 95       | SPI_MOSI   | DI  | Master output slave input |         |
| 96       | SPI_SCLK   | DO  | Clock                     |         |
| 97       | SPI_SS     | DO  | Slave select              |         |

### SDIO interface

| Pin name | Pin number | I/O | Description              | Remarks |
|----------|------------|-----|--------------------------|---------|
| 78       | SDH_D0     | IO  | SD card SDIO bus DATA0   |         |
| 77       | SDH_D1     | IO  | SD card SDIO bus DATA1   |         |
| 76       | SDH_D2     | IO  | SD card SDIO bus DATA2   |         |
| 57       | SDH_D3     | IO  | SD card SDIO bus DATA3   |         |
| 56       | SDH_CMD    | IO  | SD card SDIO bus command |         |
| 51       | SDH_CLK    | IO  | SD card SDIO bus clock   |         |

| PWM_OUT interface |            |     |                               |         |
|-------------------|------------|-----|-------------------------------|---------|
| Pin name          | Pin number | I/O | Description                   | Remarks |
| PWM_OUT           | 66         | O   | Pulse Width Modulation signal |         |

| GPS interface |            |     |                         |         |
|---------------|------------|-----|-------------------------|---------|
| Pin name      | Pin number | I/O | Description             | Remarks |
| GNSS_VRT C    | 98         | PI  | Backup voltage for GNSS |         |
| GNSS_1PPS     | 99         | O   | One pulse per second    |         |

| Antenna interface |            |     |                                      |                              |
|-------------------|------------|-----|--------------------------------------|------------------------------|
| Pin name          | Pin number | I/O | Description                          | Remarks                      |
| ANT_MAIN          | 60         | IO  | Main set antenna interface for LTE-M | 50Ω characteristic impedance |
| ANT_GNSS          | 49         | AI  | GNSS antenna interface               | 50Ω characteristic impedance |

Table 4: Pin description

## 2.3 Power supply design

EDM-XDLTEG has two VBAT pins for connecting an external power supply. The following table describes the module's VBAT pin and its ground pin.

| Power supply |                                                                       |     |                              |                                                 |
|--------------|-----------------------------------------------------------------------|-----|------------------------------|-------------------------------------------------|
| Pin name     | Pin number                                                            | I/O | Description                  | Remarks                                         |
| VBAT_BB      | 32, 33                                                                | PI  | Baseband power supply        | V max = 4.1 V<br>V min = 3.5 V<br>V typ = 3.8 V |
| VBAT_RF      | 52, 53                                                                | PI  | Radio frequency power supply | V max = 4.1 V<br>V min = 3.5 V<br>V typ = 3.8 V |
| GND          | 3,31,48,50,54,<br>55,58,59,61,62<br>, 67-74, 79-82,<br>89-91, 100-102 | GND | Ground                       |                                                 |

Table 5: Power pin

## 2.4 Power supply reference circuit

A module's power supply design is critical for its performance. EDM-XDLTEG can use an DC-DC with an output current capability of 2A as a power supply. In order to ensure better power supply performance, it is recommended to connect a low ESR ( $ESR = 0.7 \Omega$ ) 220  $\mu$ F tantalum capacitor in parallel near the VBAT input of the module, as well as 10pF, 100pF, 0.1uF and 22uF filter capacitors. At the same time, it is recommended to add a TVS tube close to the VBAT input to improve the surge voltage withstand capability of the module. In principle, the longer the VBAT trace is, the wider the trace width should be. The reference circuit of the VBAT input terminal is shown in the figure below.

For better understanding, refer the circuits given below. The users can choose one of the following circuits or design one on their own.

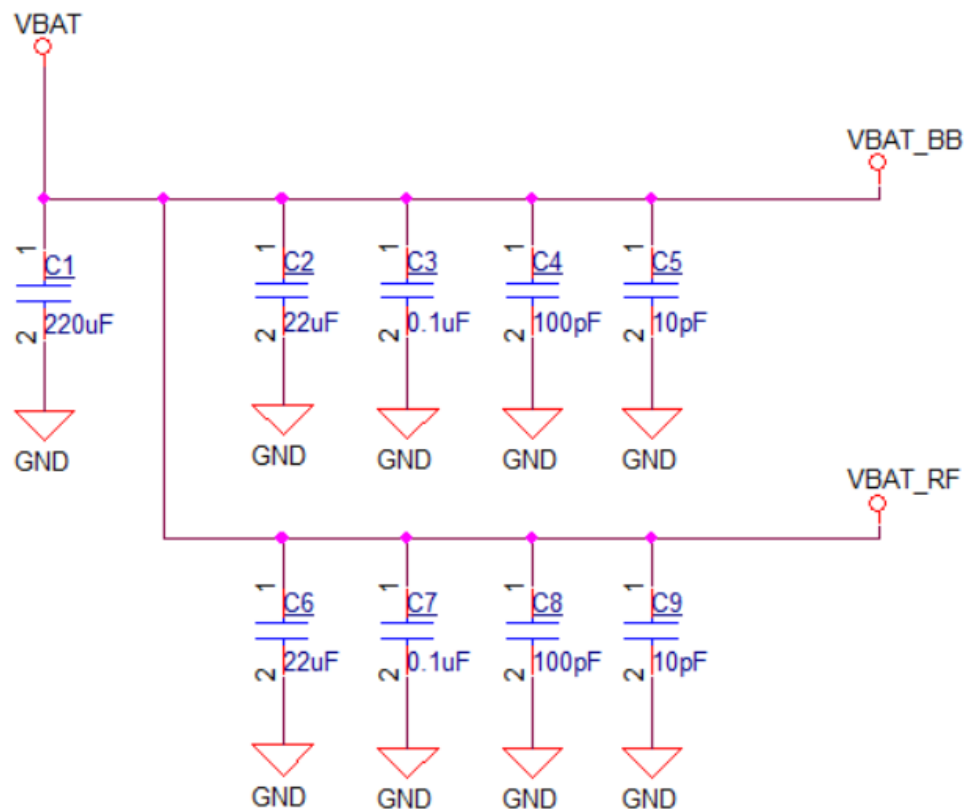
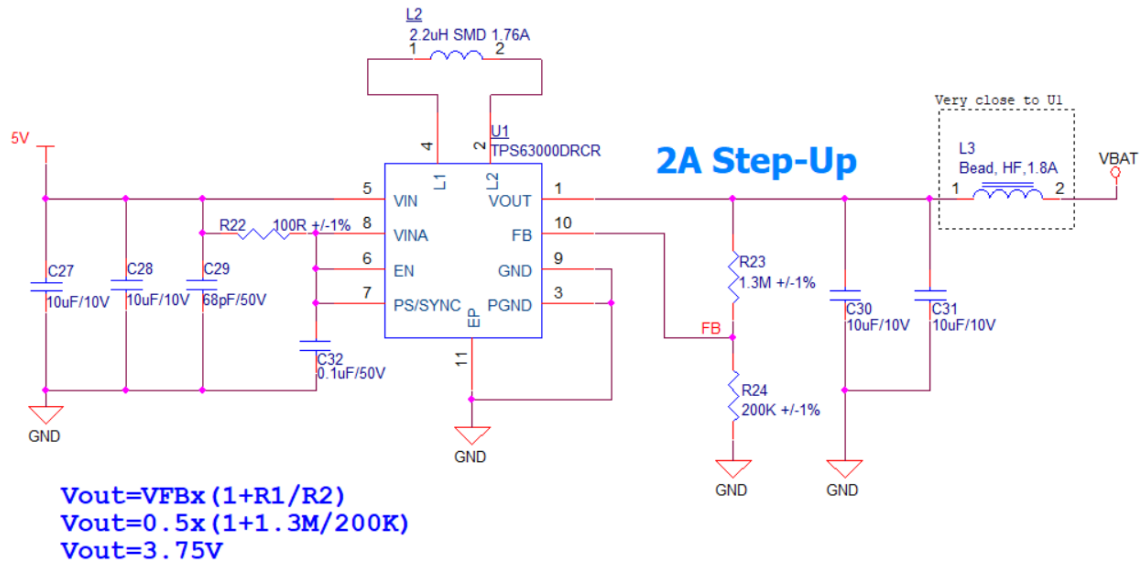


Figure 3: VBAT\_BB and VBAT\_RF input reference circuit

## 2.5 Power on/off

When the module is powered off, it can be powered on by pulling down PWRKEY for a minimum of 500 ms.

| Power on/off interface |            |     |                                                                                  |                                                            |
|------------------------|------------|-----|----------------------------------------------------------------------------------|------------------------------------------------------------|
| Pin name               | Pin number | I/O | Description                                                                      | Remarks                                                    |
| PWRKEY                 | 15         | DI  | Power on/off signal from Microprocessor, internal pull low to AGND. Active-high. | $V_{IL} \text{ max} = 0.5V$<br>$V_{IH} \text{ min} = 1.4V$ |

Table 6: PWRKEY pin

It is recommended to use an open-collector drive circuit to control the PWRKEY pin. The reference circuit is as follows.

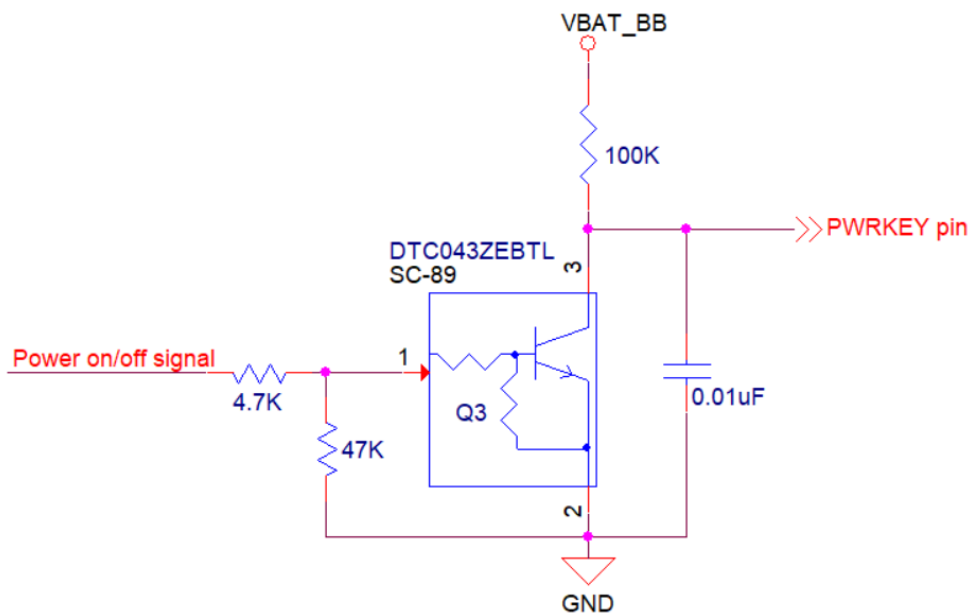


Figure 4: Open collector drive boot reference circuit

Another way to control PWRKEY is directly through a push-button switch, with a transient voltage suppressor (TVS) tube placed near the button for electrostatic discharge (ESD) protection. The reference circuit is shown in the figure below.

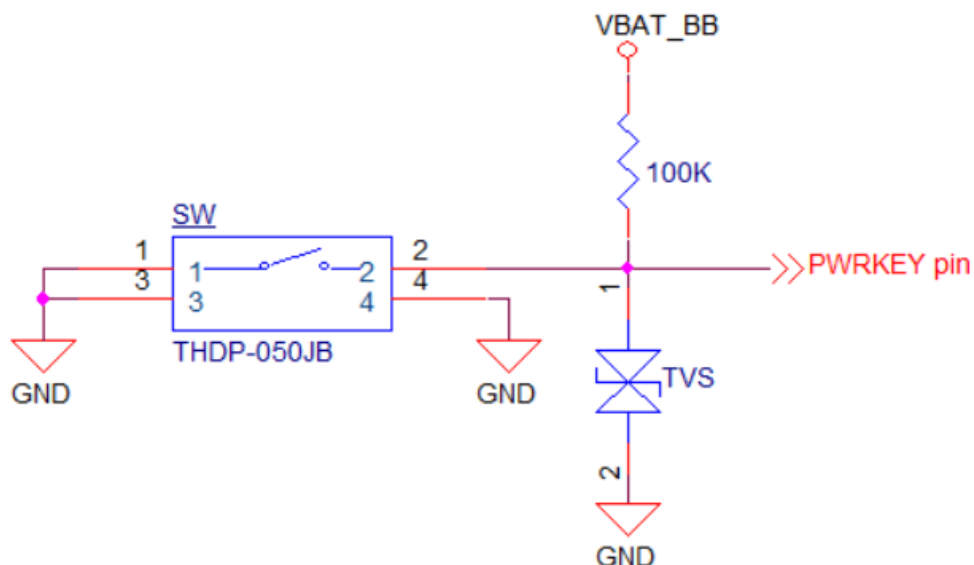


Figure 5:Button power-on reference circuit

## 2.6 Reset module

The module can be reset by pulling down the RESET pin for at least 100ms.

| Reset interface |            |     |                             |                                                            |
|-----------------|------------|-----|-----------------------------|------------------------------------------------------------|
| Pin name        | Pin number | I/O | Description                 | Remarks                                                    |
| RESET_N         | 17         | DI  | Power-on-Resets. Active low | $V_{IL} \text{ max} = 0.6V$<br>$V_{IH} \text{ min} = 1.2V$ |

Table 7: Reset pin

The hardware reset reference circuit is shown in the figure below. It is recommended to use an open-collector drive circuit to control the RESET pin.

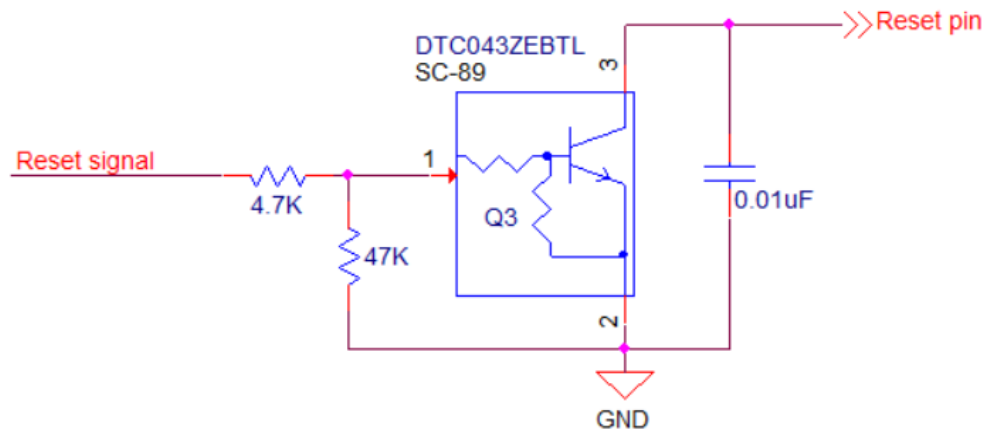


Figure 6: Open collector drive reference reset circuit

The RESET pin can also be controlled using a key.

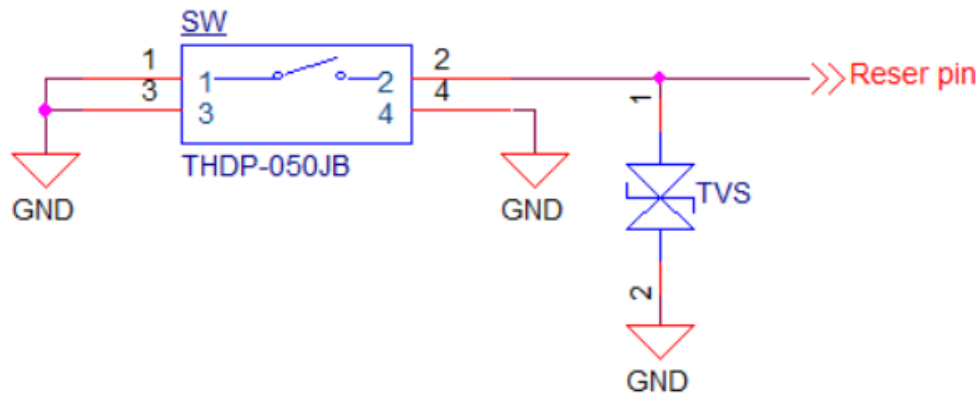


Figure 7: Button reset reference circuit

## 2.7 Serial port

The module has three serial ports: main serial port, debugging serial port and auxiliary serial port. The module operates as DCE (Data Communication Equipment) and is connected in the traditional DCE-DTE (Data Terminal Equipment) way.

Main serial port:

The serial level is 1.8V. The module's serial port baud rate can be set to 4800 to 921600bps baud rate, the default is 115200bps.

- UART1\_TXD: Send data to the RXD end of the DTE device.
- UART1\_RXD: Receive data from the TXD end of the DTE device.

Debug serial port:

- UART1\_TXD: Send data to the serial port of DTE.
- UART1\_RXD: Receive data from the serial port of DTE.

Auxiliary serial port:

- UART2\_TXD: Send data to the serial port of DTE.
- UART2\_RXD: Receive data from the serial port of DTE.

| UART interface |            |     |                      |                      |
|----------------|------------|-----|----------------------|----------------------|
| Pin name       | Pin number | I/O | Description          | Remarks              |
| UART0_RXD      | 34         | DI  | Data reception       | 1.8 V voltage domain |
| UART0_TXD      | 35         | DO  | Data transmission    | 1.8 V voltage domain |
| UART0_CTS      | 36         | DO  | UART clear to send   | 1.8 V voltage domain |
| UART0_RTS      | 37         | DI  | UART request to send | 1.8 V voltage domain |

| UART interface for Debug serial port |            |     |                   |                      |
|--------------------------------------|------------|-----|-------------------|----------------------|
| Pin name                             | Pin number | I/O | Description       | Remarks              |
| UART1_TXD                            | 27         | DO  | Data transmission | 1.8 V voltage domain |
| UART1_RXD                            | 28         | DI  | Data reception    | 1.8 V voltage domain |
| UART2_TXD                            | 23         | DO  | Data transmission | 1.8 V voltage domain |
| UART2_RXD                            | 22         | DI  | Data reception    | 1.8 V voltage domain |

Table 8: Serial port pin definition

The main serial port can be used for AT command transmission, data transmission and Interact with peripheral data..

After the module is turned on, it is in the adaptive serial transmission rate mode by default (the default is 115,200 bps serial transmission rate self-adjusting synchronization); the MCU needs to continuously send AT commands to the module for serial transmission rate synchronization, and if an "OK" is returned, it means the synchronization is successful; Following hibernation, the module will directly use the serial transmission rate that had been successfully synchronized after power-on, without needing to resynchronize.

The figure below shows a schematic diagram of the connection between a DCE and a DTE for the main serial port.

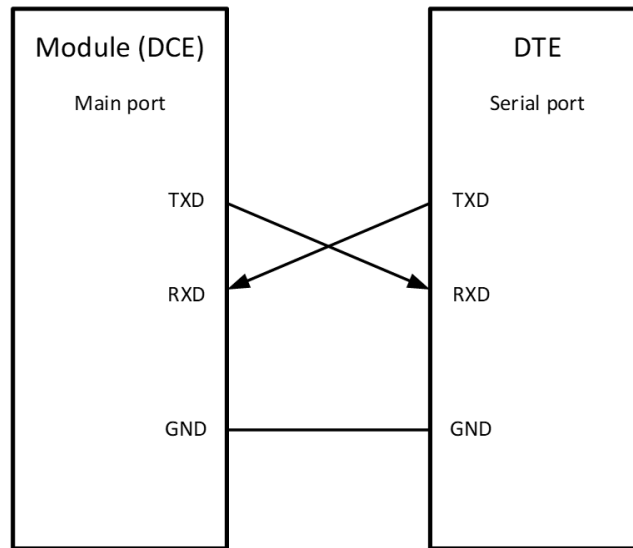


Figure 8: Schematic diagram of the main serial port's connection mode

With the debugging tool, customers can view the underlying log information through the debugging serial port for software debugging; its default serial transfer rate is 115,200 bps.

The figure below shows a schematic diagram of the connection between a DCE and a DTE for the debugging serial port.

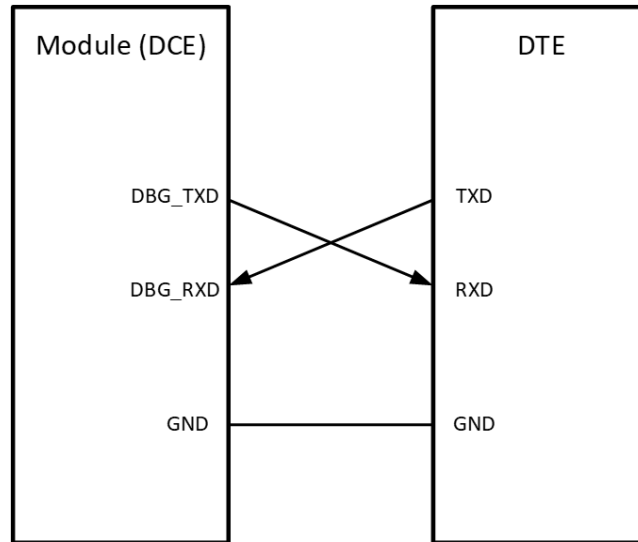


Figure 9: Schematic diagram of the debugging serial port's connection mode

With the debugging tool, customers can view the underlying log information through the auxiliary serial port for software debugging. Its default serial transfer rate is 115,200 bps. The schematic diagram of the connection between a DCE and a DTE is as follows.

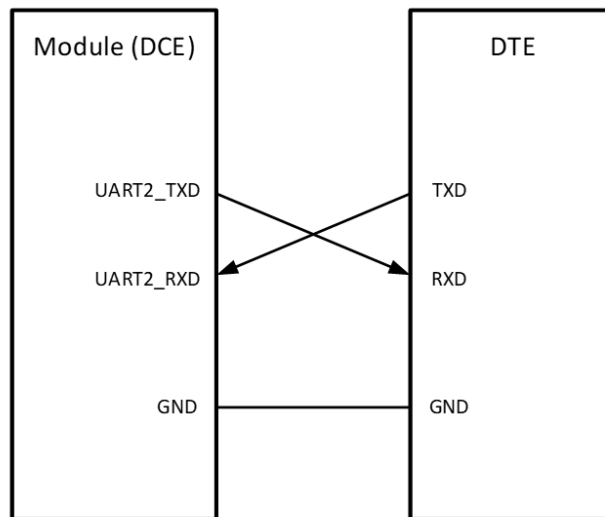


Figure 10: Schematic diagram of the auxiliary serial port's connection mode

The voltage domain of the serial port of this module is 1.8 V. If the voltage domain of the customer application system is 3.3 V, a level converter must be included in the serial connection between the module and the customer application system. The following figure provides a reference circuit design using a level conversion chip.



## 2.8 SPI interface

EDM-XDLTEG provides an SPI interface (the module acting as the host), and the following table lists the pin definitions of the SPI interface.

| SPI interface |            |     |                           |         |
|---------------|------------|-----|---------------------------|---------|
| Pin name      | Pin number | I/O | Description               | Remarks |
| 94            | SPI_MISO   | DI  | Master input slave output |         |
| 95            | SPI_MOSI   | DI  | Master output slave input |         |
| 96            | SPI_SCLK   | DO  | Clock                     |         |
| 97            | SPI_SS     | DO  | Slave select              |         |

Table 9: SPI interface pin definition

The SPI interface voltage domain of this module is 1.8 V. If the system voltage domain of the slave device is 3.3 V, a level shifter needs to be added between the module and the slave device; it is recommended to use a level shifter that supports the SPI data rate. A reference circuit is shown in the figure below.

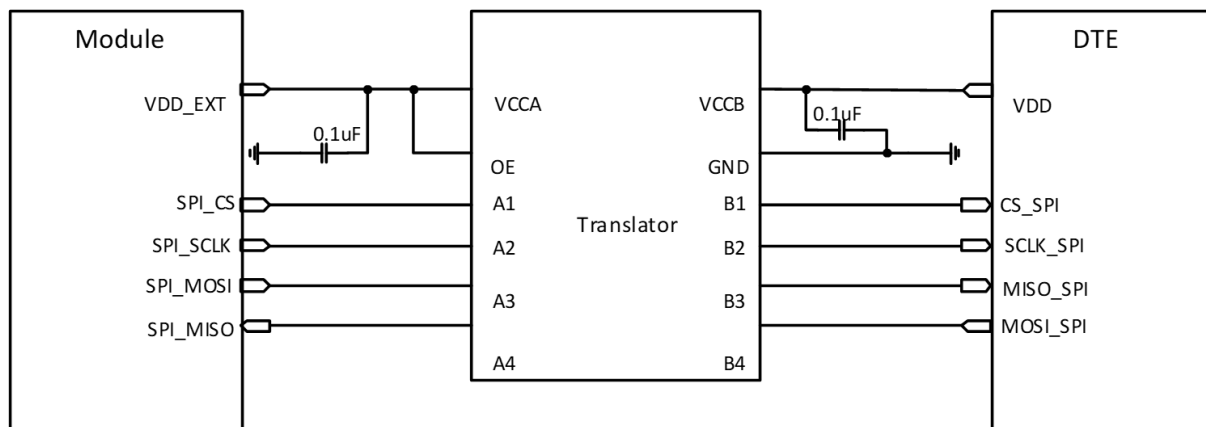


Figure 13: SPI interface level shifting reference circuit

## 2.9 USIM interface

The USIM interface of the EDM-XDLTEG module complies with the ISO/IEC 7816-3 specification and supports 1.8 V / 3.0 V external USIM cards, powered by the power supply inside the module.

| USIM interface |            |     |                        |           |
|----------------|------------|-----|------------------------|-----------|
| Pin name       | Pin number | I/O | Description            | Remarks   |
| USIM_VDD       | 43         | PO  | USIM card power supply | 1.8V / 3V |
| USIM_RST       | 44         | DO  | USIM card reset        |           |
| USIM_DATA      | 45         | IO  | USIM card data         |           |
| USIM_CLK       | 46         | DO  | USIM card clock        |           |

Table 10: USIM interface pin definition

The figure below is the reference design of the 7-pin external USIM card holder.

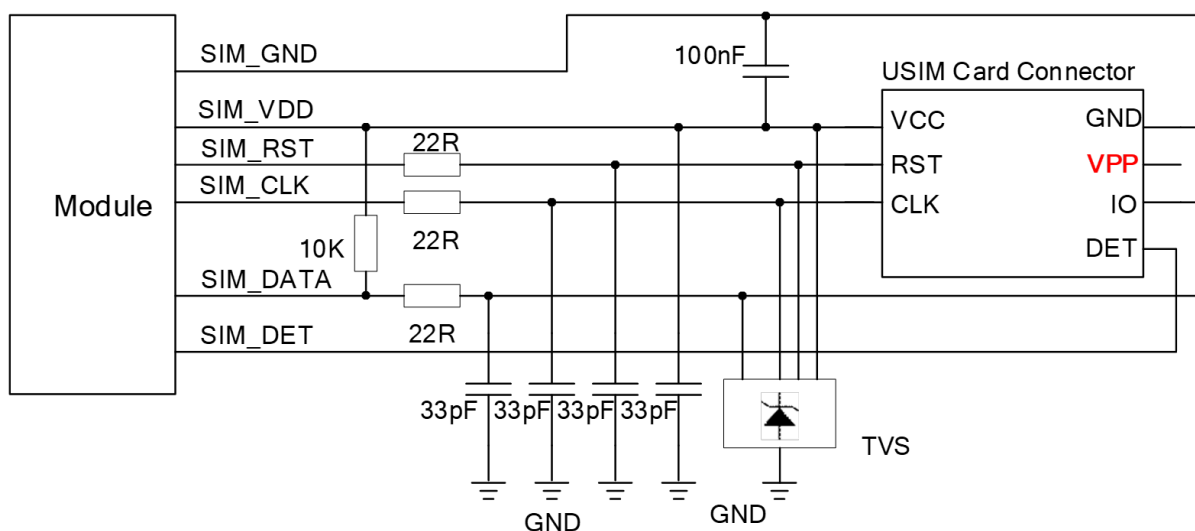


Figure 14: 7-pin external USIM card holder reference circuit diagram

In the circuit design of the USIM interface, it is recommended to follow the design principles described below in order to ensure good performance of the external USIM card and prevent it from being damaged.

- The external USIM card holder should be placed close to the module, and the length of the signal cable should not exceed 200 mm to ensure optimal performance.
- The external USIM card socket signal cable should be routed away from both the RF trace and the VBAT power cable.
- The ground of the external USIM card socket and the SIM\_GND wiring of the module should be short and thick, ensuring a wiring width of not less than 0.5 mm to ensure the same potential. The decoupling capacitor of SIM\_VDD should not exceed 1 uF, and should be placed close to the external USIM card socket.
- To prevent interference between the SIM\_CLK and SIM\_DATA signals, their wiring should not be too close, and a ground shield should be placed between them. Furthermore, the SIM\_RST signal should also be provided with a ground shield.
- To ensure optimal ESD protection performance, it is recommended to add a TVS tube to the pin of the external USIM card holder, where the parasitic capacitance should not exceed 50 pF. The ESD protection device should be placed as close as possible to the external USIM card socket, and the signal routing should run from the socket to the device, then to the module. A 22-ohm resistor should be connected in series between the module and the external USIM card to suppress stray EMI and bolster ESD protection. To further improve performance, peripheral components of the external USIM card should be placed as close as possible to the external USIM card holder.
- Connect 33 pF capacitors in parallel to the SIM\_DATA, SIM\_VDD, SIM\_CLK, and SIM\_RST lines to filter out radio-frequency interference.

## 2.10 ADC interface

The module provides a 10-bit analog-to-digital conversion input interface to measure the voltage value. The A/D interface operates in both Active and Idle modes.

| ADC interface |            |     |                                         |         |
|---------------|------------|-----|-----------------------------------------|---------|
| Pin name      | Pin number | I/O | Description                             | Remarks |
| ADC1          | 2          | AI  | Analog to digital converter interface 1 |         |
| ADC0          | 24         | AI  | Analog to digital converter interface 0 |         |

Table 11: ADC interface pin definition

The following is the ADC peripheral reference design circuit. The detection voltage is connected either in series with  $0\ \Omega$  or directly to the ADC pin, with a filter capacitor connected in parallel near the module.

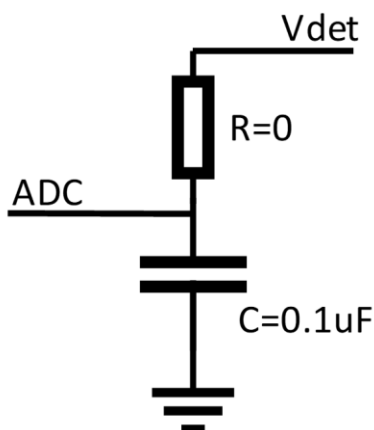


Figure 15: ADC peripheral reference circuit<sup>5</sup>

## 2.11 Network status indicator

The NETLIGHT signal can be used to indicate the network status of the module. The connection reference circuit of the network status indicator is shown in the figure below.

| Network Indication interface |            |     |                           |                      |
|------------------------------|------------|-----|---------------------------|----------------------|
| Pin name                     | Pin number | I/O | Description               | Remarks              |
| NETLIGHT                     | 21         | DO  | Network status indication | 1.8 V voltage domain |

Table 12: NETLIGHT pin definition

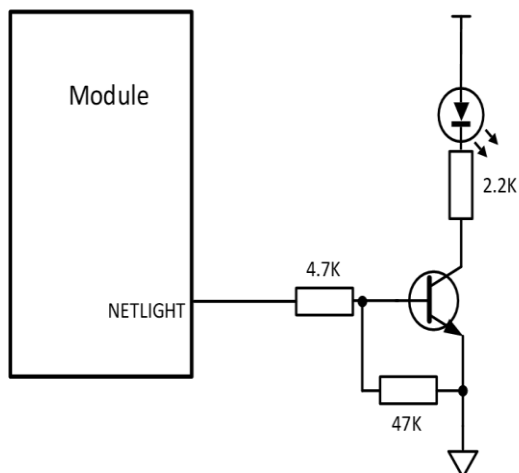


Figure 16: Network status indication reference circuit

## 2.12 Module status indicator

The STATUS signal can be used to indicate the module status. The connection reference circuit of the module status indicator is shown in the figure below.

| Module status interface |            |     |                                   |                      |
|-------------------------|------------|-----|-----------------------------------|----------------------|
| Pin name                | Pin number | I/O | Description                       | Remarks              |
| STATUS                  | 20         | DO  | Module power on status indication | 1.8 V voltage domain |

Table 13: STATUS pin definition

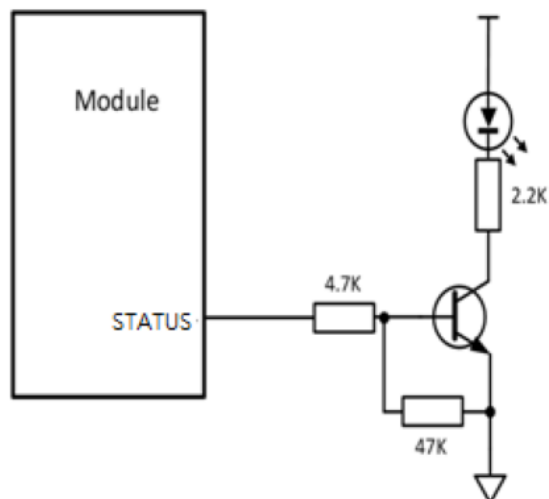


Figure 17: Module status indication reference circuit

## 3. Antenna interface

Pin 35 is the RF antenna interface of the module. The impedance of the RF antenna port is 50  $\Omega$ .

### 3.1 Pin definition

| Antenna interface |            |     |                                      |                                      |
|-------------------|------------|-----|--------------------------------------|--------------------------------------|
| Pin name          | Pin number | I/O | Description                          | Remarks                              |
| ANT_MAIN          | 60         | IO  | Main set antenna interface for LTE-M | 50 $\Omega$ characteristic impedance |
| ANT_GNSS          | 49         | AI  | GNSS antenna interface               | 50 $\Omega$ characteristic impedance |

Table 14: RF antenna pin definition

### 3.2 Operating frequency

| Duplex mode | Band    | Frequency band |              |
|-------------|---------|----------------|--------------|
|             |         | Downlink (MHz) | Uplink (MHz) |
| HD-FDD      | 8       | 925~960        | 880~915      |
| HD-FDD      | 106     | 935~940        | 896~901      |
| HD-FDD      | ISM-FDD | 915~928        | 880~915      |

Table 15: Module operating frequency

### 3.3 RF antenna reference circuit

It is recommended to reserve a  $\pi$ -type matching circuit in the peripheral circuit design of the antenna interface in order to better adjust the radio frequency performance. The components of the  $\pi$ -type matching circuit should be placed as close to the antenna as possible and selected according to the actual situation. By default, C1 and C2 are omitted and only a 0 ohm resistor is attached to R1.

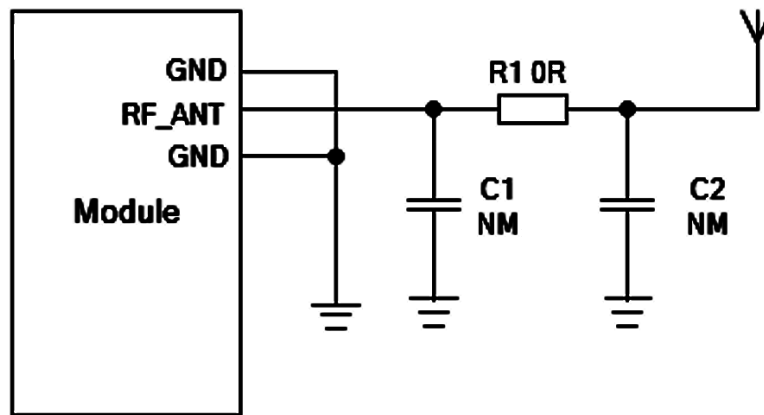


Figure 18: RF antenna reference circuit

The EDM-XDLTEG module provides an RF pad interface for connecting an external antenna, with ground pads on either side for improved grounding performance.

### 3.4 RF signal cable layout reference guide

For the user PCB, the characteristic impedance of all RF signal lines should be controlled to 50  $\Omega$ . In general, the impedance of an RF signal line is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S), and the height of the reference ground plane (H). The control of PCB characteristic impedance is usually accomplished through two methods: microstrip line and coplanar waveguide. To illustrate the design principle, the following

figures show the structural design of the microstrip line and the coplanar waveguide when the impedance line is controlled to  $50\ \Omega$ .

- The complete structure of the microstrip line.

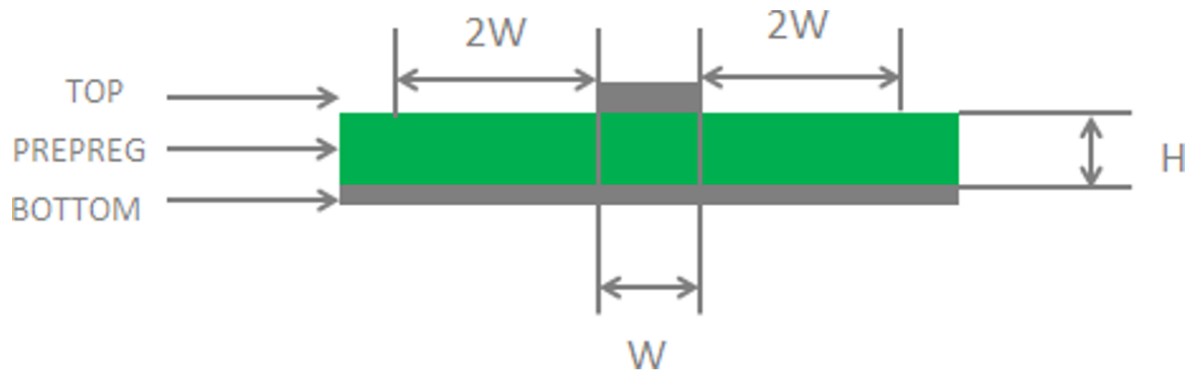


Figure 19: Two-layer PCB board microstrip line structure

- Complete structure of coplanar waveguide.

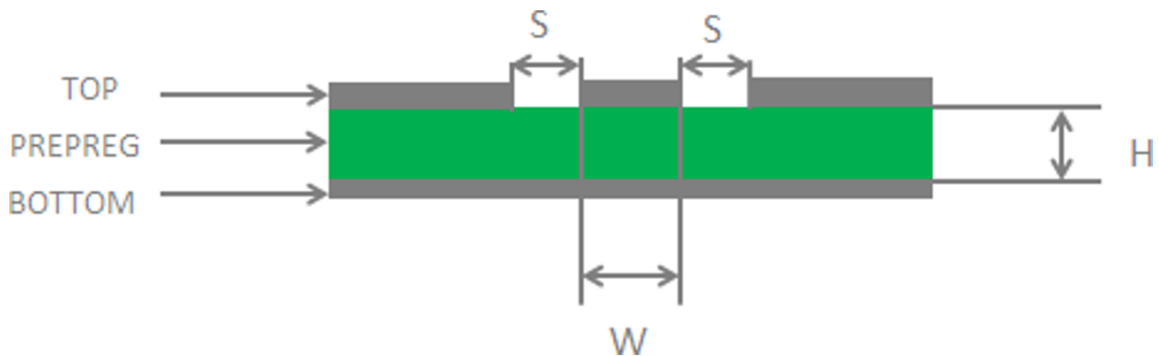


Figure 20: Two-layer PCB coplanar waveguide structure

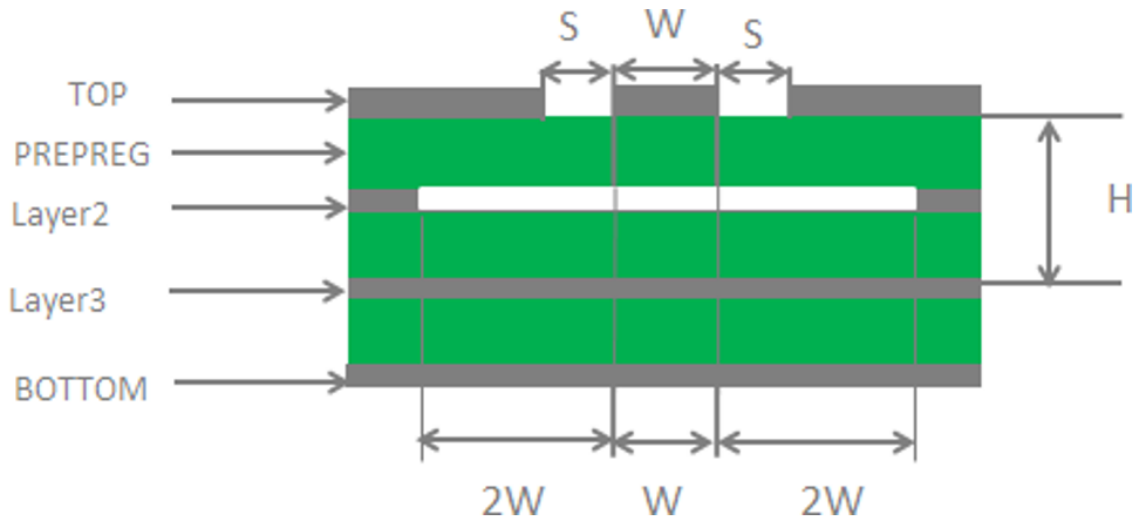


Figure 21: Four-layer PCB coplanar waveguide structure (the reference ground is the third layer)

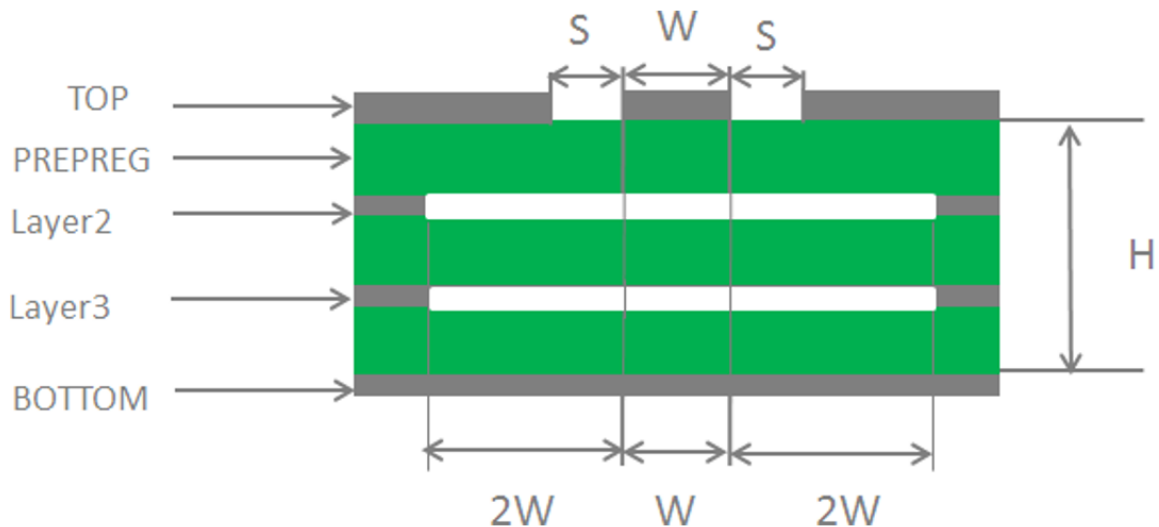


Figure 22: Four-layer PCB coplanar waveguide structure (the reference ground is the fourth layer)

To ensure good performance and reliability of the RF signal in the circuit design of the RF antenna interface, the following design principles are recommended:

- The impedance simulation calculation tool should be used to precisely control the 50Ω impedance on the RF signal line.
- The GND pin adjacent to the RF pin should not be used as a thermal pad, but should be fully in contact with the ground plane.
- The distance between the RF pin and the RF connector should be kept as short as possible; additionally, right-angle routing should be avoided, with a recommended routing angle of 135 degrees.
- Care should be taken when constructing the package of the connecting device, and a certain distance should be maintained between the signal pin and the ground.

- The reference ground plane of the RF signal line should be complete; adding a certain number of ground holes around the signal line and the reference ground can improve the RF performance; the distance between the ground hole and the signal line should be at least twice the line width ( $2*W$ ).

### 3.5 Antenna requirements

The table below lists the requirements for LTE-M and NB-IoT antennas.

| Parameter                    | Requirement                                                                                                                                                |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Frequency                    | B1/B2/B3/B4/B5/B6/B8/B9/B10/B12/B13/B14/B17/<br>B18/B19/B20/B25/B26/B27/B28/B33/B35/B36/B39/<br>B44/B54/B65/B66/B68/B70/B71/B85/B103/B106/<br>B111/ISM-FDD |
| Insertion loss               | <1dB                                                                                                                                                       |
| VSWR                         | $\leq 2$                                                                                                                                                   |
| Efficiency                   | > 30%                                                                                                                                                      |
| Maximum input power (W)      | 50                                                                                                                                                         |
| Input Impedance ( $\Omega$ ) | 50                                                                                                                                                         |

Table 16: Antenna parameter requirements

### 3.6 RF output power

| Frequency band | Maximum value     | Minimum value |
|----------------|-------------------|---------------|
| 1              | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 2              | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 3              | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 4              | 23 dBm $\pm$ 2 dB | < -20dBm      |

| Frequency band | Maximum value     | Minimum value |
|----------------|-------------------|---------------|
| 5              | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 6              | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 8              | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 9              | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 10             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 12             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 13             | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 14             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 17             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 18             | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 19             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 20             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 25             | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 26             | 28 dBm $\pm$ 2 dB | < -20dBm      |
| 27             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 28             | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 33             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 35             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 36             | 23dBm $\pm$ 2 dB  | < -20dBm      |

| Frequency band | Maximum value     | Minimum value |
|----------------|-------------------|---------------|
| 39             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 44             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 54             | 28dBm $\pm$ 2 dB  | < -20dBm      |
| 65             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 66             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 68             | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 70             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 71             | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 85             | 23dBm $\pm$ 2 dB  | < -20dBm      |
| 103            | 23 dBm $\pm$ 2 dB | < -20dBm      |
| 106            | 28 dBm $\pm$ 2 dB | < -20dBm      |
| 111            | 28dBm $\pm$ 2 dB  | < -20dBm      |
| ISM-FDD        | 28 dBm $\pm$ 2 dB | < -20dBm      |

Table 17: RF conducted power

### 3.7 RF receive sensitivity

| Frequency band | Conducted reception sensitivity |
|----------------|---------------------------------|
| 1              | -103 dBm                        |
| 2              | -104 dBm                        |
| 3              | -105.5 dBm                      |
| 4              | -103 dBm                        |
| 5              | -105 dBm                        |
| 6              | -105 dBm                        |
| 8              | -106 dBm                        |
| 9              | -105.5 dBm                      |
| 10             | -103 dBm                        |
| 12             | -104.5 dBm                      |
| 13             | -105 dBm                        |
| 14             | -105 dBm                        |
| 17             | -105 dBm                        |
| 18             | -104.5 dBm                      |
| 19             | -105 dBm                        |
| 20             | -103.5 dBm                      |
| 25             | -104 dBm                        |
| 26             | -105 dBm                        |

| Frequency band | Conducted reception sensitivity |
|----------------|---------------------------------|
| 27             | -104.5 dBm                      |
| 28             | -105 dBm                        |
| 33             | -106 dBm                        |
| 35             | -106 dBm                        |
| 36             | -104.5 dBm                      |
| 39             | -106 dBm                        |
| 44             | -105 dBm                        |
| 54             | -104 dBm                        |
| 65             | -103 dBm                        |
| 66             | -103 dBm                        |
| 68             | -103 dBm                        |
| 70             | -103.5 dBm                      |
| 71             | -106 dBm                        |
| 85             | -105 dBm                        |
| 106            | -106 dBm                        |
| 111            | -105 dBm                        |
| ISM-FDD        | -106 dBm                        |

Table 18: RF retransmission sensitivity

## 4. Electrical performance and reliability

### 4.1 Operating and storage temperature

The table below shows the module operating and storage temperature range.

| Parameter                                   | Minimum value | Typical value | Maximum value | Unit |
|---------------------------------------------|---------------|---------------|---------------|------|
| Normal operating temperature <sup>6</sup>   | -30           | +25           | +85           | °C   |
| Extended operating temperature <sup>7</sup> | -30           | +25           | +85           | °C   |
| Storage temperature                         | -40           | +25           | +100          | °C   |

Table 19: Operating and storage temperature range

<sup>6</sup>When the module works in this temperature range, the relevant performance of the module meets the requirements of the 3GPP standard.

<sup>7</sup>When the module works within this temperature range, it can still maintain a normal working state, with functions such as SMS and data transmission, and there will be no irreparable faults; the radio frequency spectrum and network are largely unaffected. However, the values of individual indicators such as output power may exceed the scope of 3GPP standards. When the temperature returns to the normal operating temperature range, the indicators of the module will still meet the 3GPP standard.

## 4.2 Static protection

Due to the static electricity generated by the human body and the charged friction between microelectronics, static electricity may be discharged to the module through various channels in the application process, causing certain damage to the module. Thus, ESD protection should be paid attention to throughout the research and development, production assembly and testing, especially during product design. Anti-static protection should be added at the interface of circuit design and points that are susceptible to damage or influence by electrostatic discharge; additionally, anti-static gloves should be worn during production. Friction between microelectronics, static electricity can be discharged to the module through various channels, which may cause certain damage, thus emphasizing the need for ESD protection. During the process of research and development, production assembly, and testing, especially in product design, ESD protection measures should be taken. For example, anti-static protection should be added to the interface of circuit design and points that are susceptible to damage or influence by electrostatic discharge; furthermore, anti-static gloves should be worn during production.

The following table shows the ESD withstand voltage of the module pins.

| Test point        | Contact discharge | Air discharge | Unit |
|-------------------|-------------------|---------------|------|
| VBAT, GND         | ±5                | ±10           | kV   |
| Antenna interface | ±5                | ±10           | kV   |
| Other interfaces  | ±0.5              | ±1            | kV   |

Table 20: ESD Performance Parameters (Temperature: 25 °C, Humidity: 45 %)

## 5. Mechanical dimensions

This chapter describes the mechanical dimensions of the module, all of which are in millimeters. For those dimensions without specified tolerances, the tolerance is ±0.05mm.

## 5.1 Module mechanical size

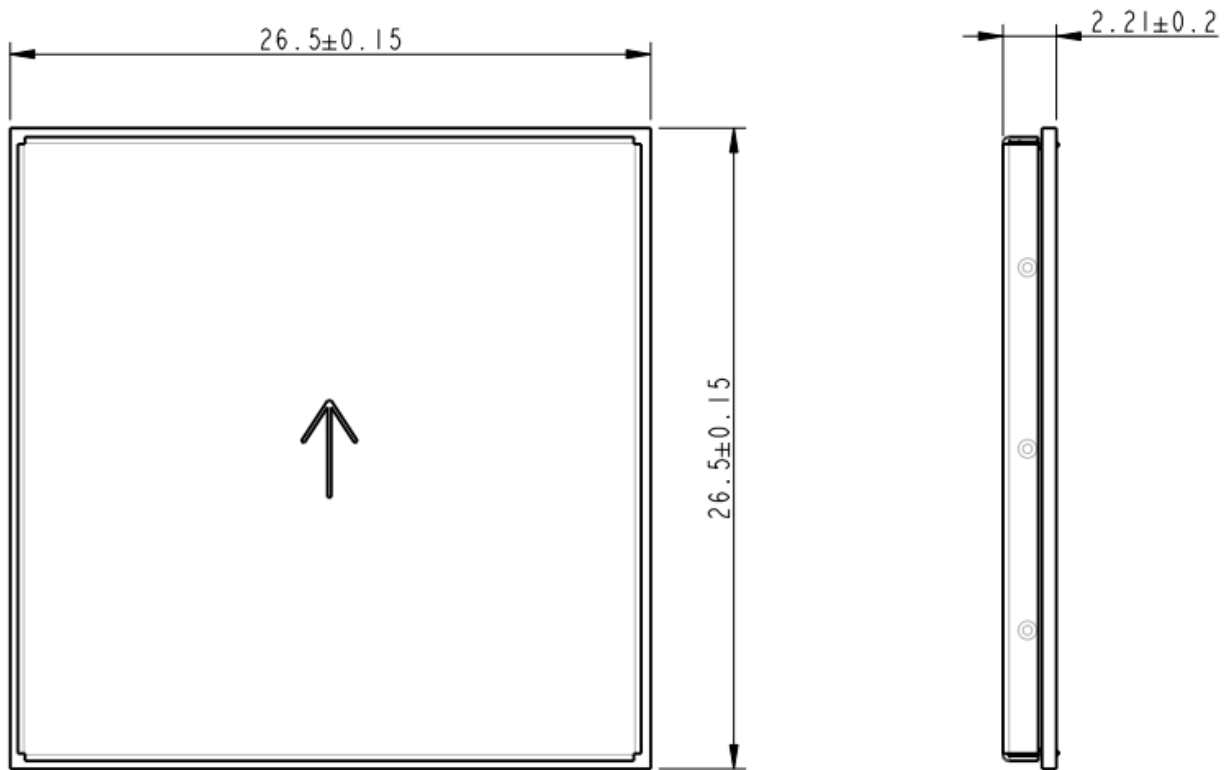


Figure 23: Top and side dimension drawing (unit: mm)

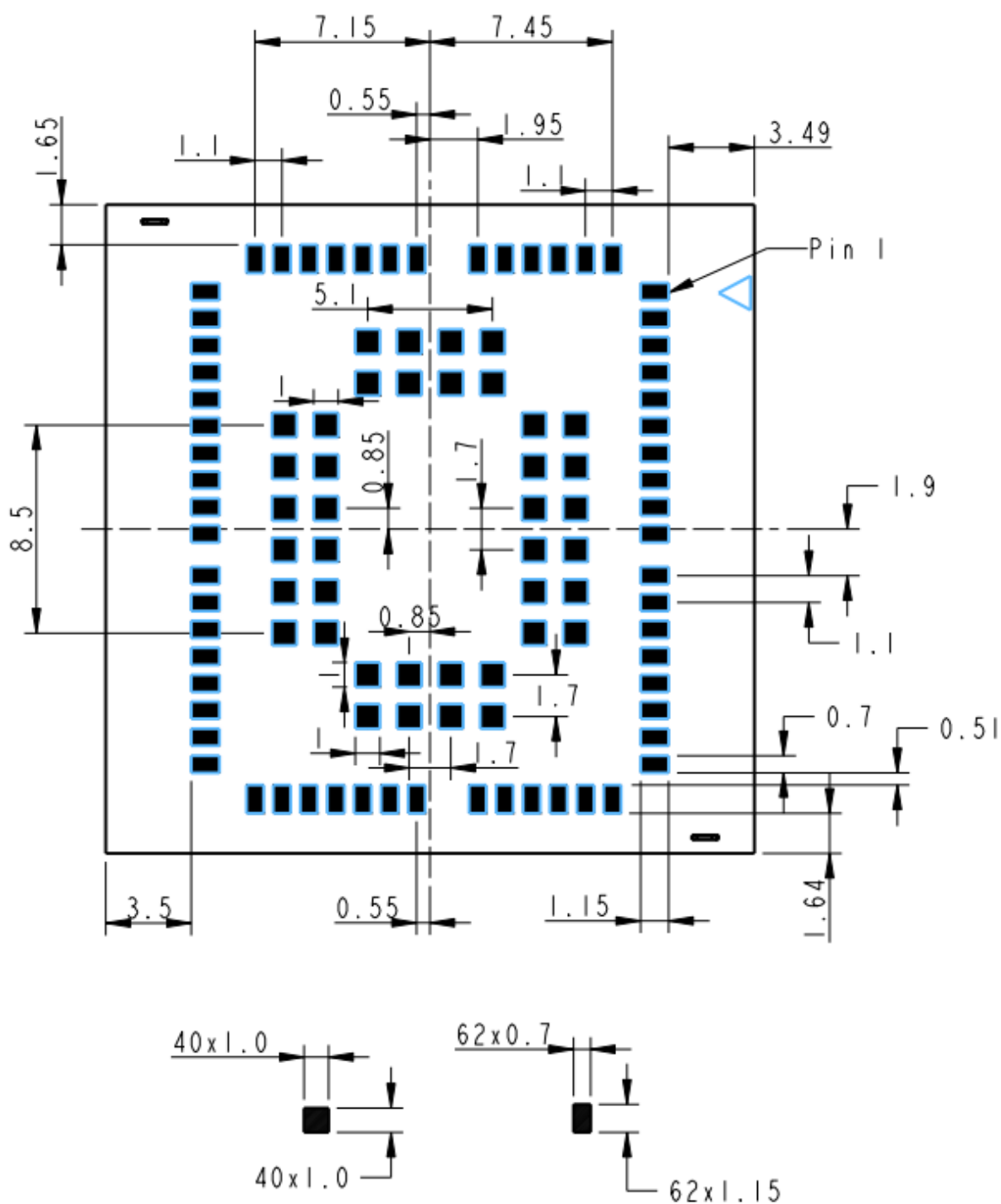


Figure 24: Module bottom view dimensions (bottom view)

## 5.2 Module top view / bottom view



Figure 25: Module top view<sup>8</sup>

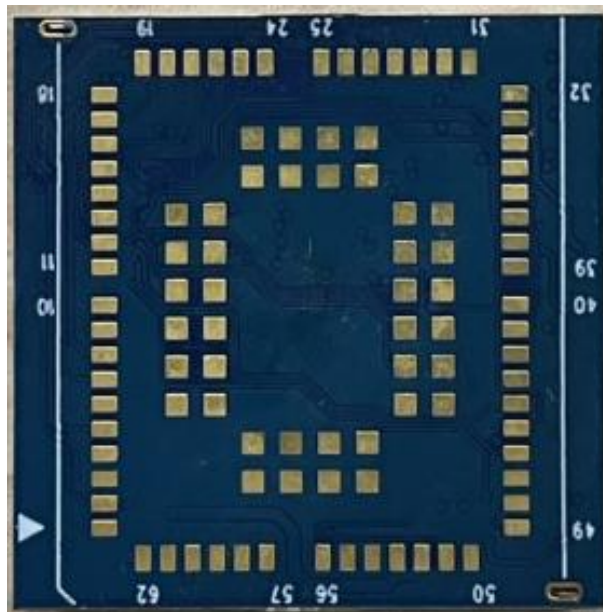


Figure 26: Module Bottom View

<sup>8</sup>It is the design rendering of the Maverick 220 module

## 6 FCC statement

FCC Statement: This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

### 6.1 Radiation exposure statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 65 cm between the radiator and your body.

This device is intended only for OEM integrators under the following conditions:

The antenna must be installed such that 46 cm is maintained between the antenna and users, and the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

The exposure standard for wireless device employs a unit of measurement known as the Specific Absorption Rate, or SAR. The SAR limit set by the FCC is 1.6W/kg. Tests for SAR are conducted using standard operating positions (10mm) accepted by the FCC with the device transmitting at its highest certified power level in all tested frequency bands.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

**IMPORTANT NOTE:** In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

## 6.2 End product labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID:2AXTDEDMXNLTEG”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

## 6.3 Manual information to the end user

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

## Appendix A Terminology abbreviations

| Abbreviation        | Description                                                       |
|---------------------|-------------------------------------------------------------------|
| ADC                 | Analog-to-Digital Converter                                       |
| CoAP                | Constrained Application Protocol                                  |
| DCE                 | Data Communications Equipment (typically module)                  |
| DTE                 | Data Terminal Equipment (typically computer, external controller) |
| DTLS                | Datagram Transport Layer Security                                 |
| EMI                 | Electromagnetic Interference                                      |
| ESD                 | Electrostatic Discharge                                           |
| FTP                 | File Transfer Protocol                                            |
| HD-FDD              | Half-Duplex Frequency Division Duplexing                          |
| HTTP                | Hyper Text Transfer Protocol                                      |
| HTTPS               | Hyper Text Transfer Protocol over Secure Socket Layer             |
| I/O                 | Input/Output                                                      |
| kbps                | Kilo Bits Per Second                                              |
| LED                 | Light Emitting Diode                                              |
| Li-MnO <sub>2</sub> | Lithium-manganese Dioxide                                         |
| Li-2S               | Lithium Sulfur                                                    |
| LTE                 | Long Term Evolution                                               |
| LwM2M               | Lightweight M2M                                                   |

| Abbreviation | Description                                   |
|--------------|-----------------------------------------------|
| MQTT         | Message Queuing Telemetry Transport           |
| NB-IoT       | Narrow Band- Internet of Things               |
| PCB          | Printed Circuit Board                         |
| PDU          | Protocol Data Unit                            |
| PPP          | Point-to-Point Protocol                       |
| PSM          | Power Saving Mode                             |
| RF           | Radio Frequency                               |
| RTC          | Real Time Clock                               |
| RXD          | Receive Data                                  |
| SMS          | Short Message Service                         |
| SSL          | Secure Sockets Layer                          |
| TCP          | Transmission Control Protocol                 |
| TE           | Terminal Equipment                            |
| TXD          | Transmitting Data                             |
| UART         | Universal Asynchronous Receiver & Transmitter |
| UDP          | User Datagram Protocol                        |
| URC          | Unsolicited Result Code                       |
| USIM         | (Universal) Subscriber Identification Module  |
| VSWR         | Voltage Standing Wave Ratio                   |

| Abbreviation        | Description                             |
|---------------------|-----------------------------------------|
| V max               | Maximum Voltage Value                   |
| V norm              | Normal Voltage Value                    |
| V min               | Minimum Voltage Value                   |
| V <sub>IH</sub> max | Maximum Input High Level Voltage Value  |
| V <sub>IH</sub> min | Minimum Input High Level Voltage Value  |
| V <sub>IL</sub> max | Maximum Input Low Level Voltage Value   |
| V <sub>IL</sub> min | Minimum Input Low Level Voltage Value   |
| V <sub>I</sub> max  | Absolute Maximum Input Voltage Value    |
| V <sub>I</sub> norm | Absolute Normal Input Voltage Value     |
| V <sub>I</sub> min  | Absolute Minimum Input Voltage Value    |
| V <sub>OH</sub> max | Maximum Output High Level Voltage Value |
| V <sub>OH</sub> min | Minimum Output High Level Voltage Value |
| V <sub>OL</sub> max | Maximum Output Low Level Voltage Value  |
| V <sub>OL</sub> min | Minimum Output Low Level Voltage Value  |

## Revision history

| Revision | Date      | Description     |
|----------|-----------|-----------------|
| 1.0      | July 2025 | Initial release |

## Contact

For further support and contact information, visit us at [www.ubiik.com](http://www.ubiik.com)  
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