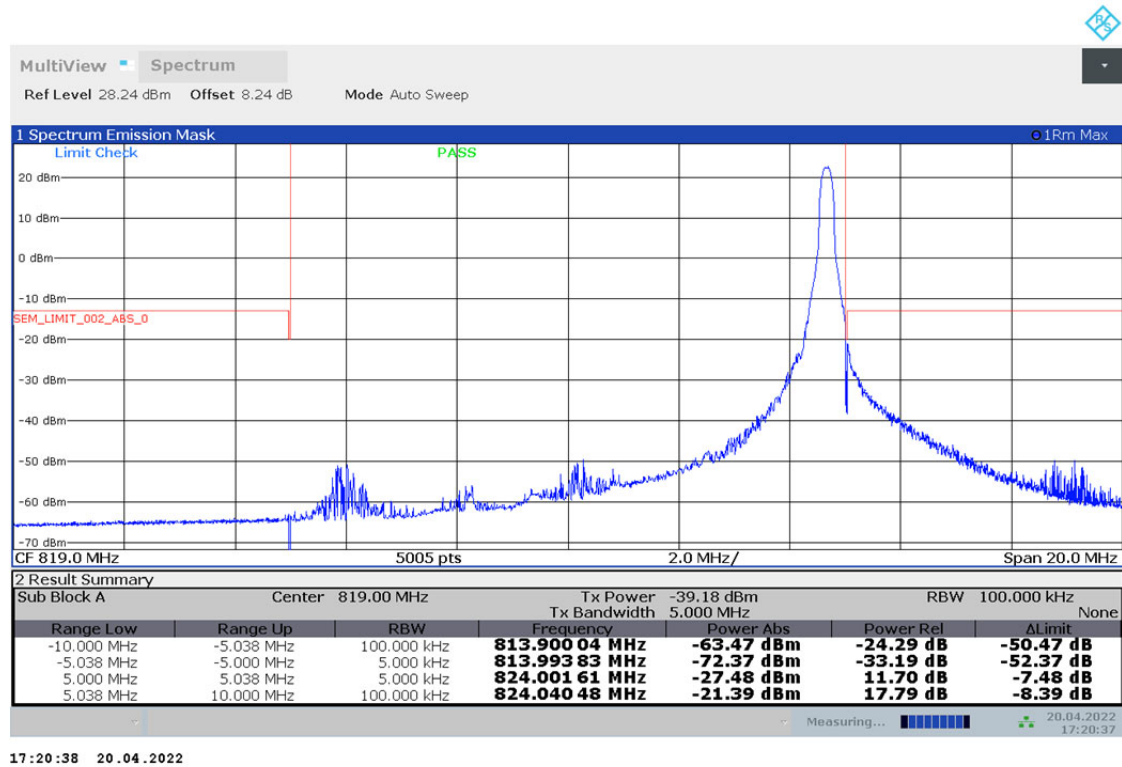
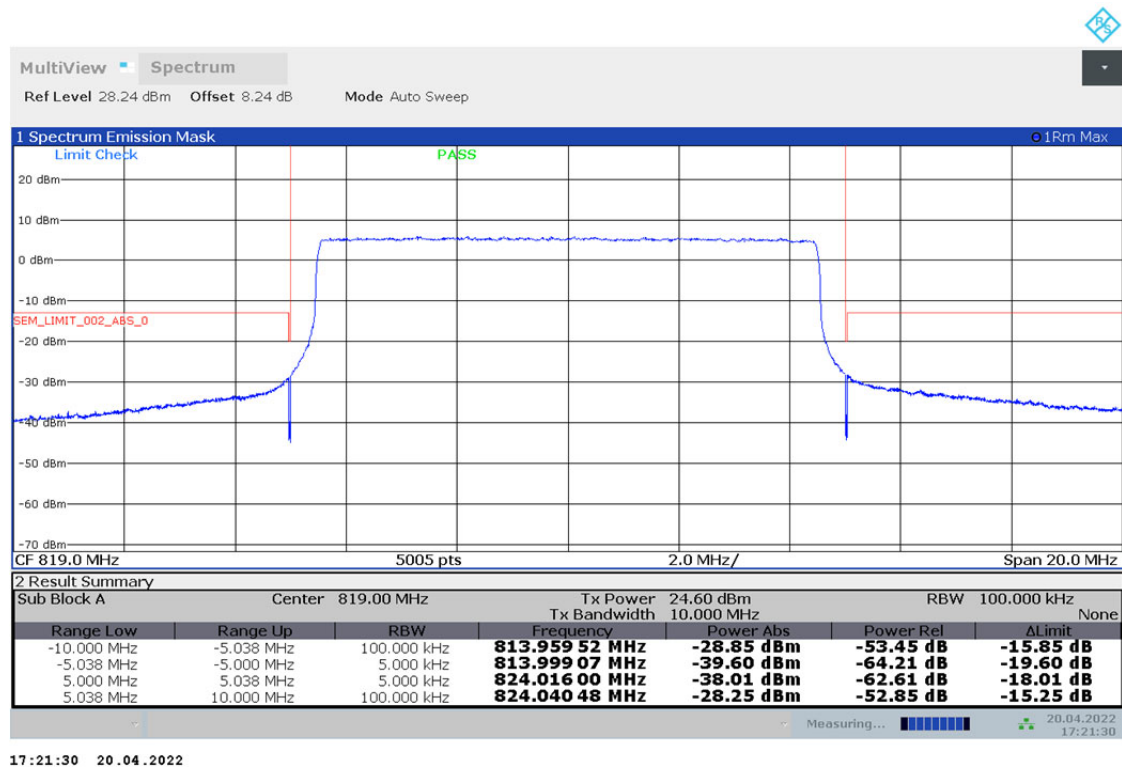


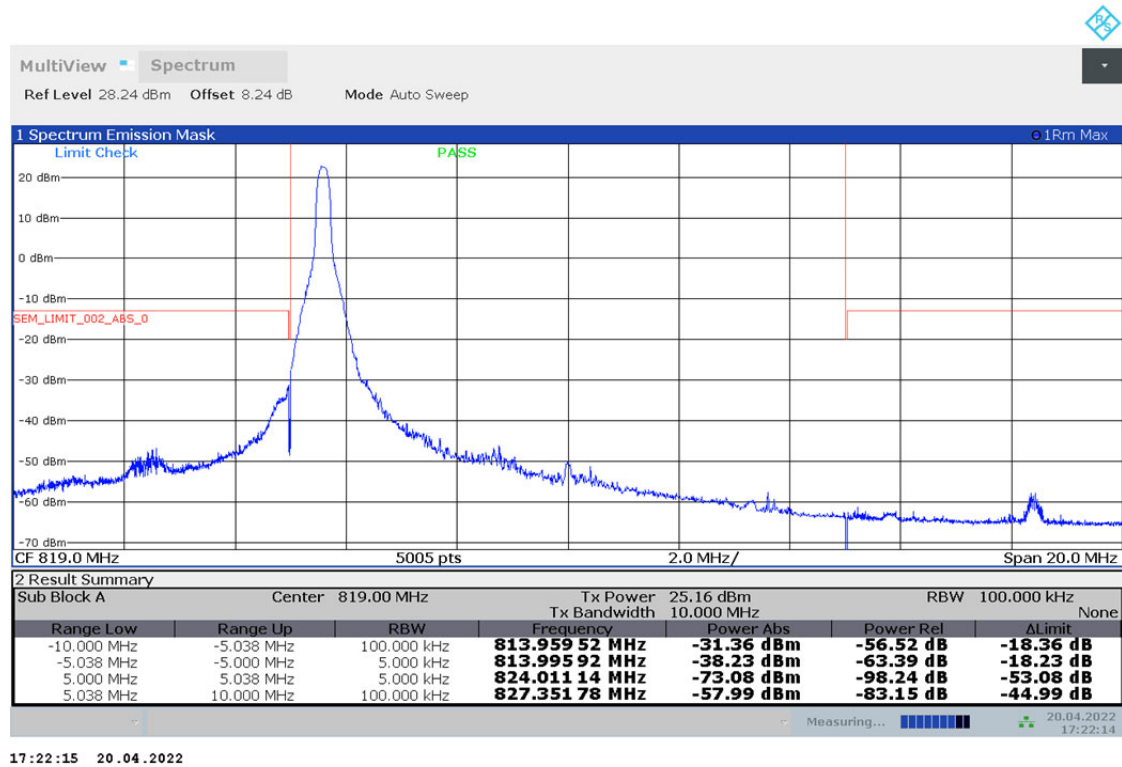
5.2.12 TM1_5MHz_HCH_RB1#24



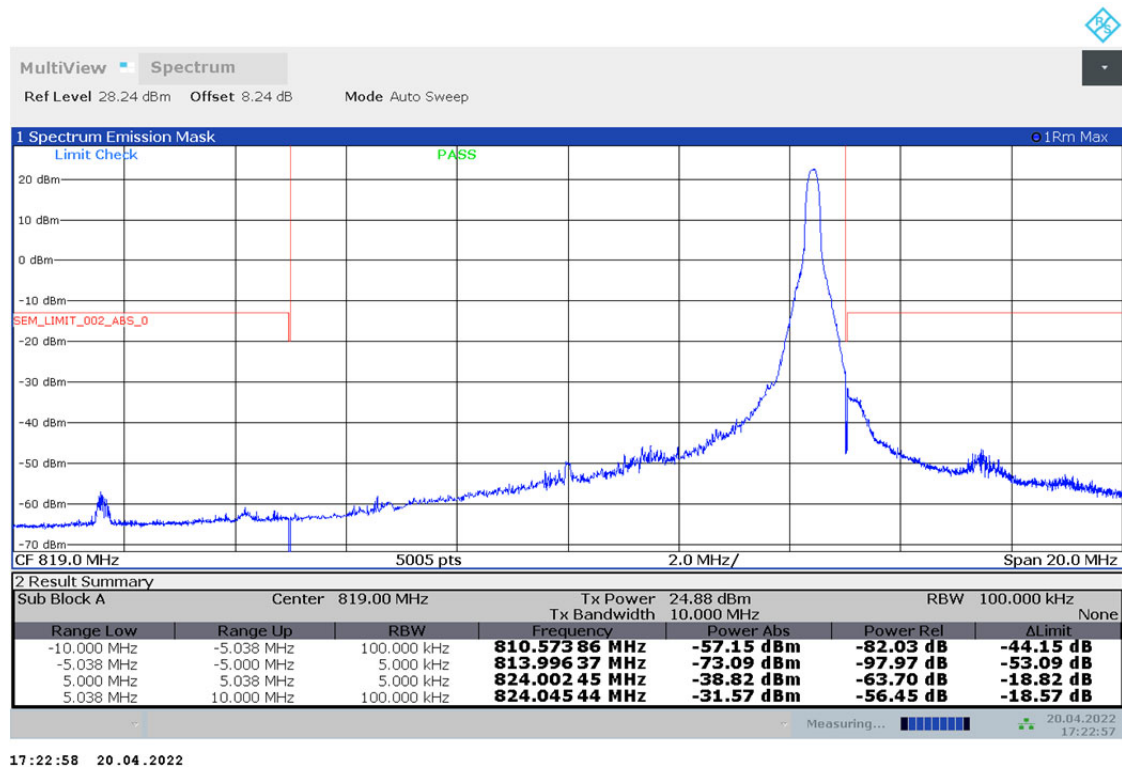
5.2.13 TM1_10MHz_LCH_RB50#0



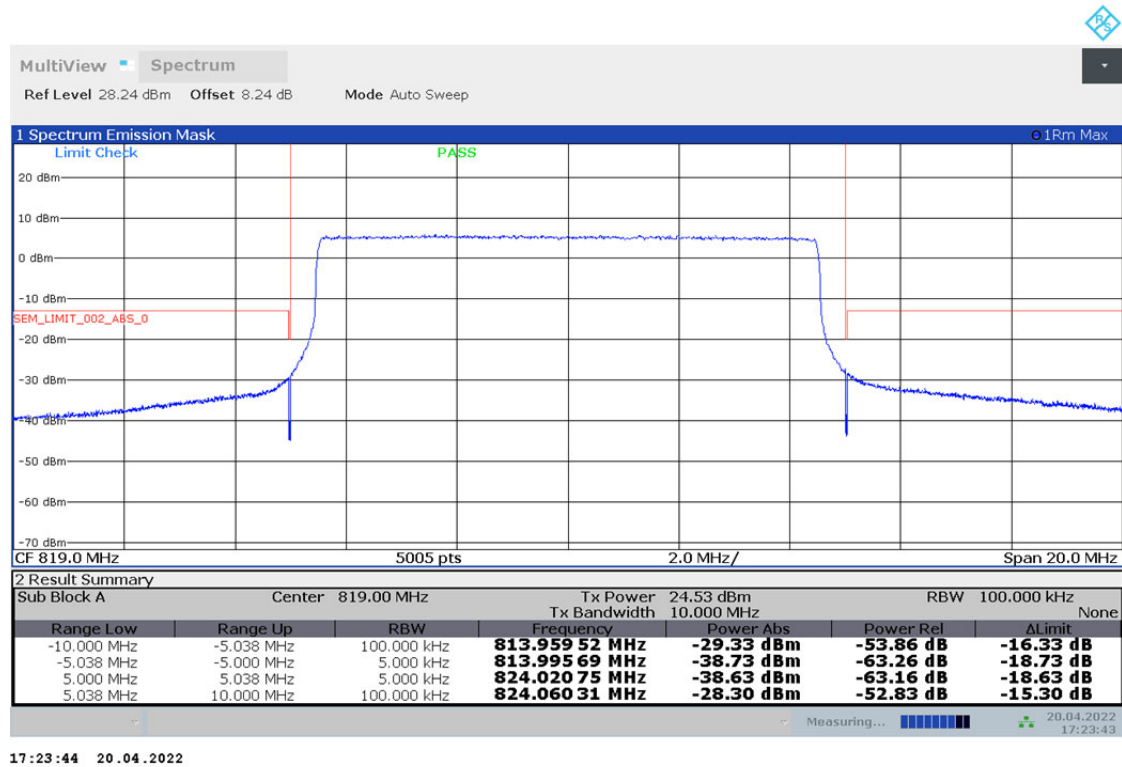
5.2.14 TM1_10MHz_LCH_RB1#0



5.2.15 TM1_10MHz_LCH_RB1#49

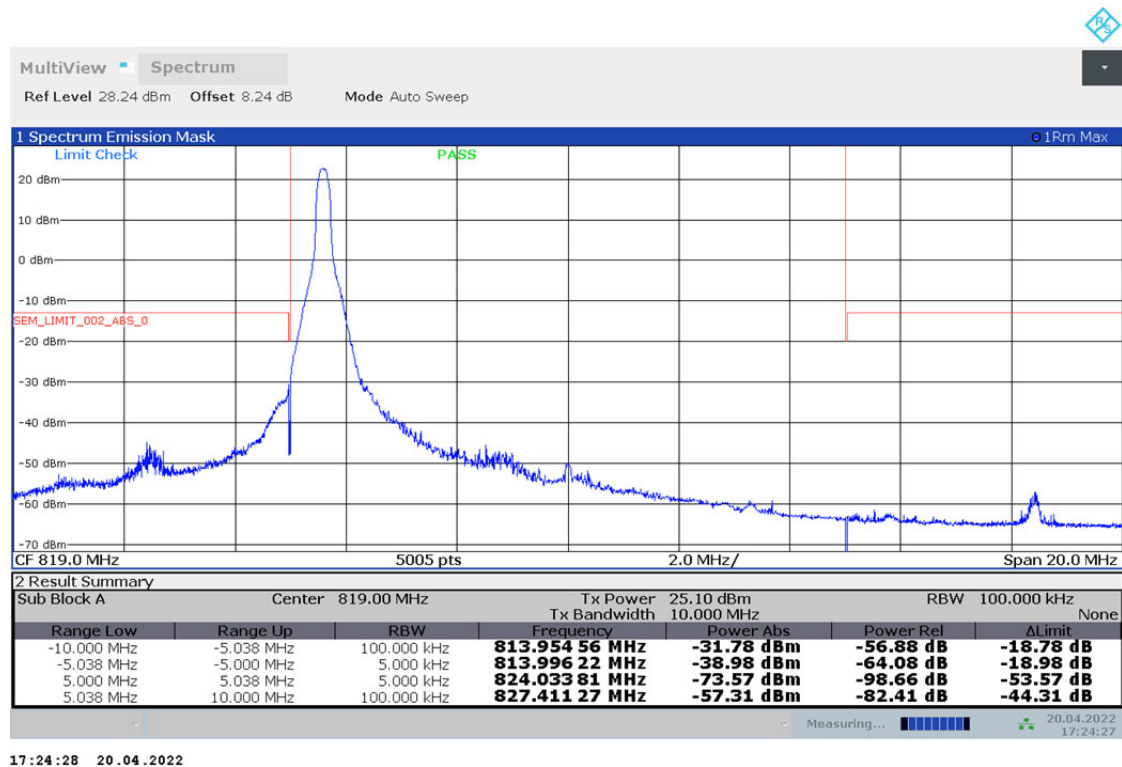


5.2.16 TM1_10MHz_HCH_RB50#0



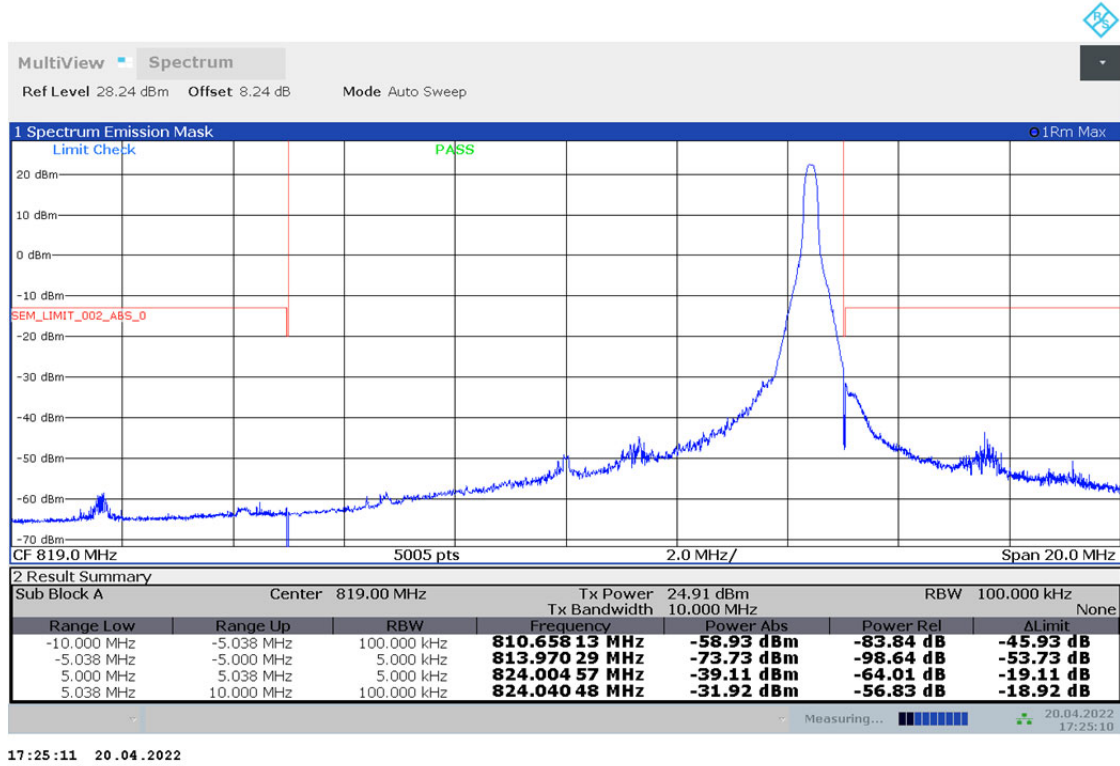
17:23:44 20.04.2022

5.2.17 TM1_10MHz_HCH_RB1#0

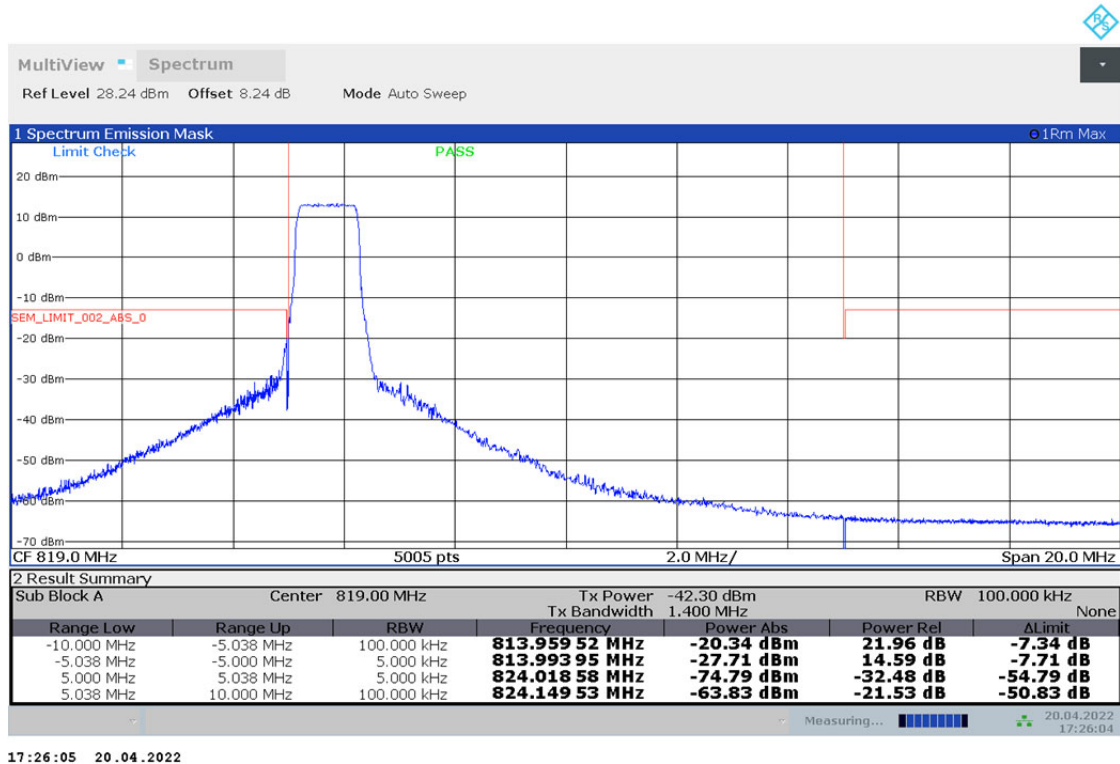


17:24:28 20.04.2022

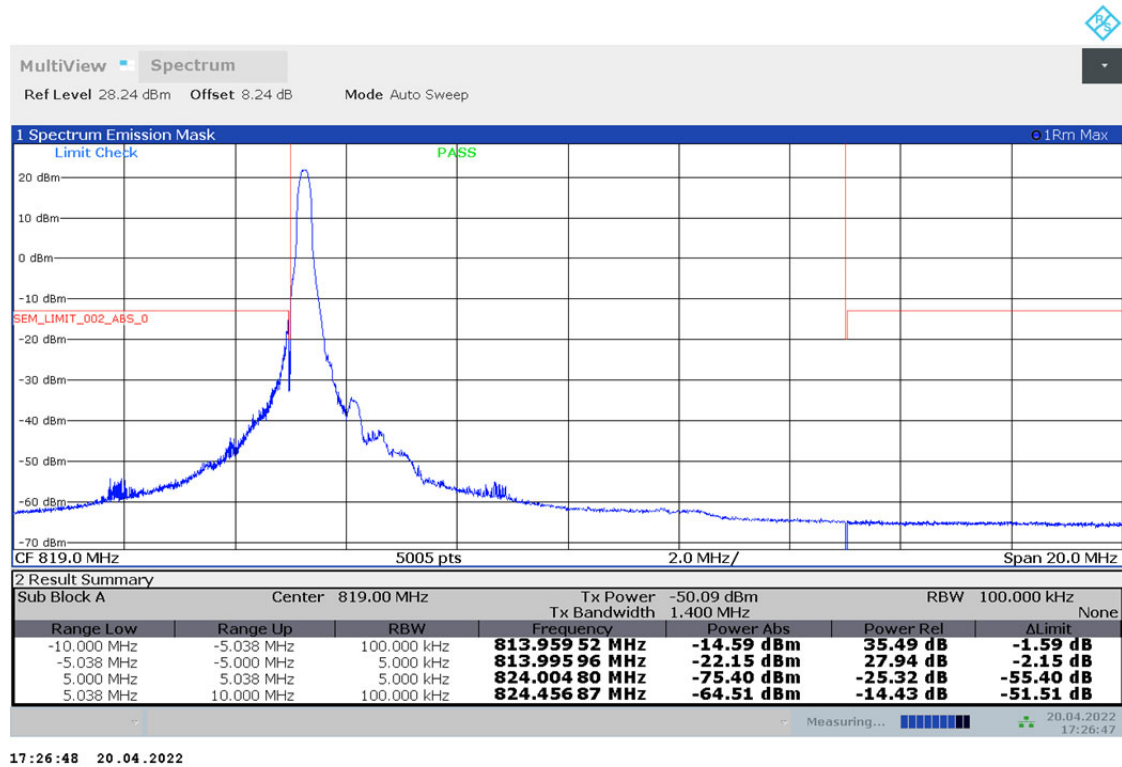
5.2.18 TM1_10MHz_HCH_RB1#49



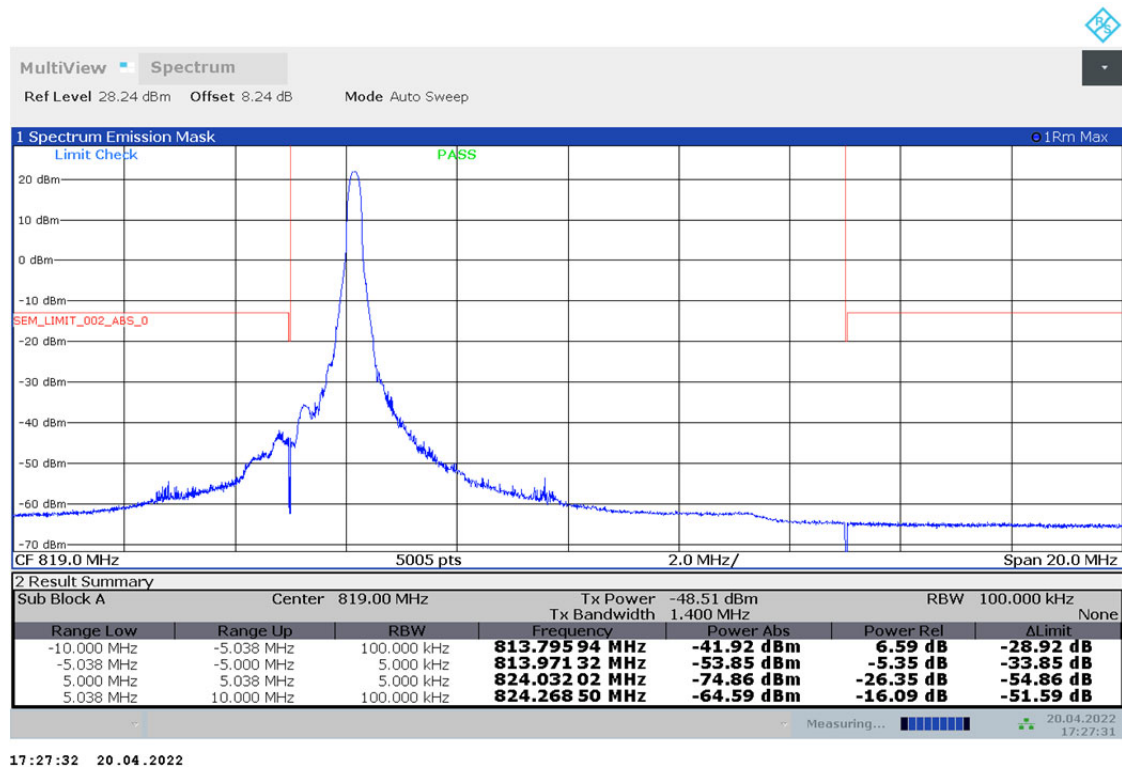
5.2.19 TM2_1.4MHz_LCH_RB6#0



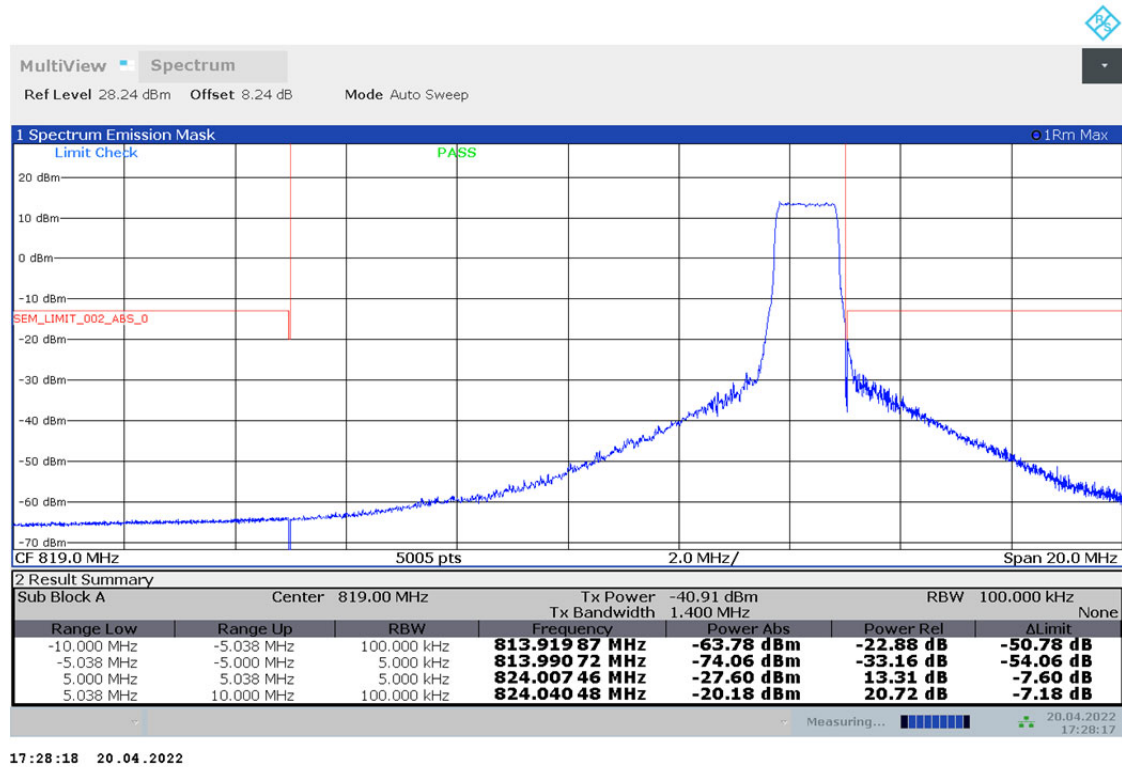
5.2.20 TM2_1.4MHz_LCH_RB1#0



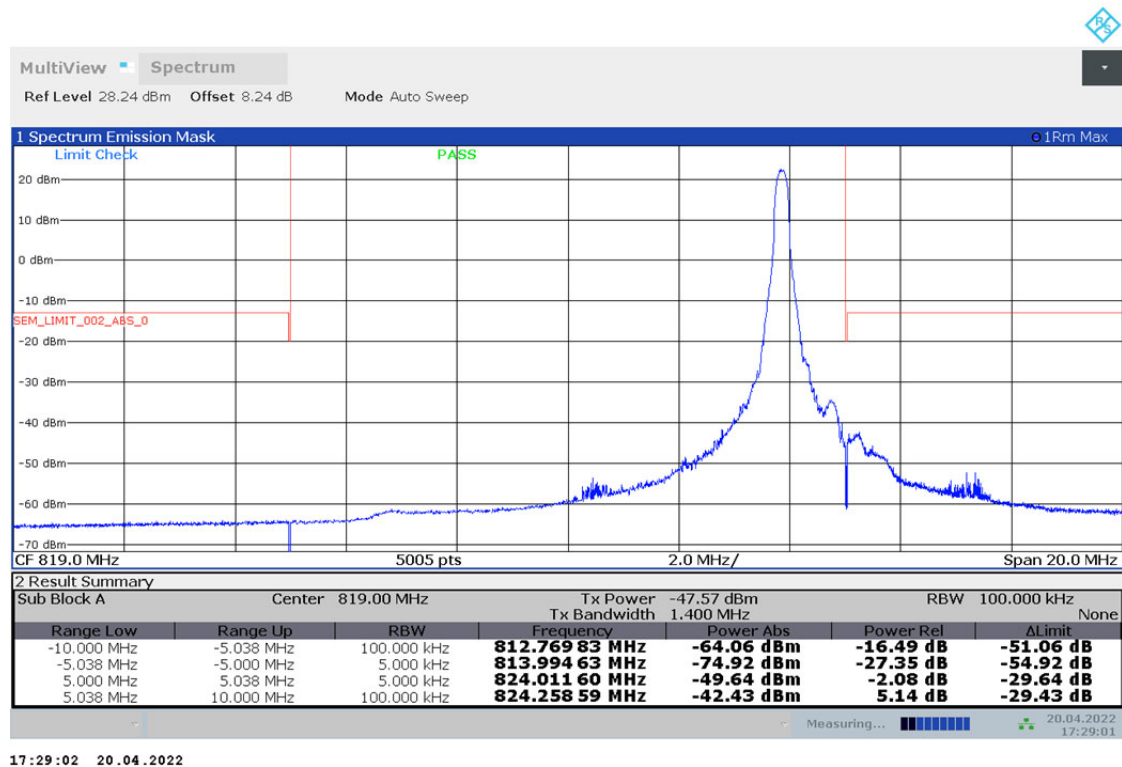
5.2.21 TM2_1.4MHz_LCH_RB1#5



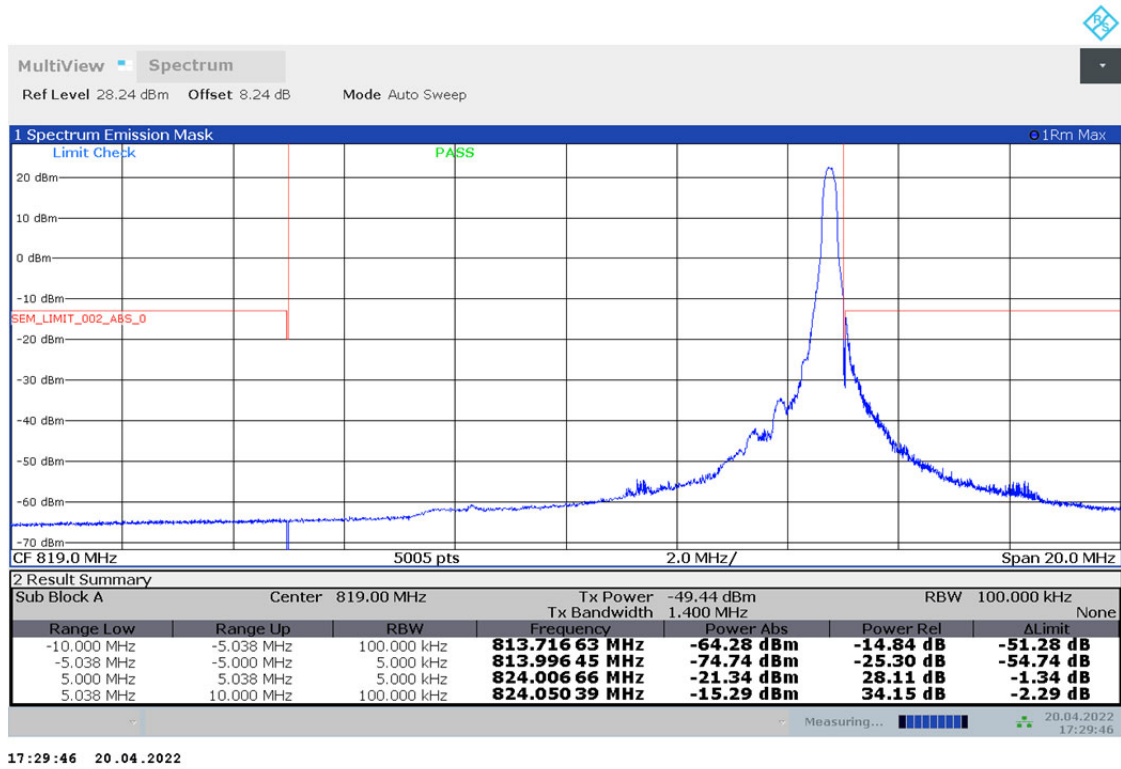
5.2.22 TM2_1.4MHz_HCH_RB6#0



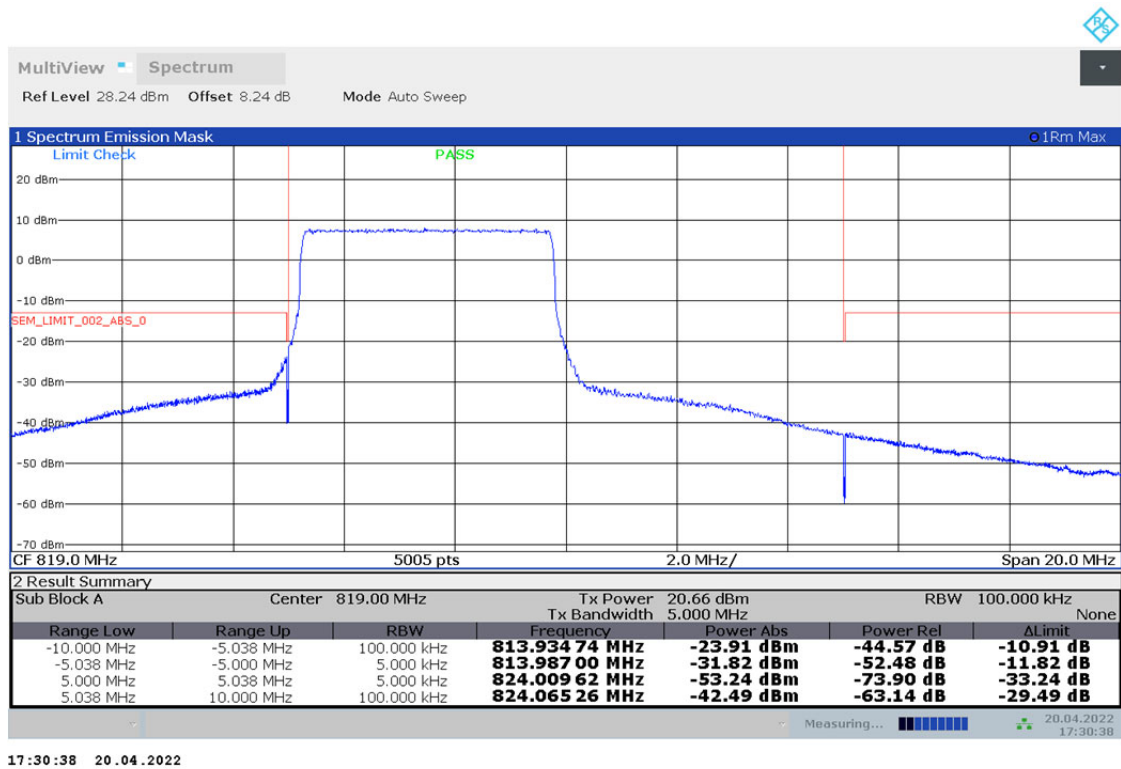
5.2.23 TM2_1.4MHz_HCH_RB1#0



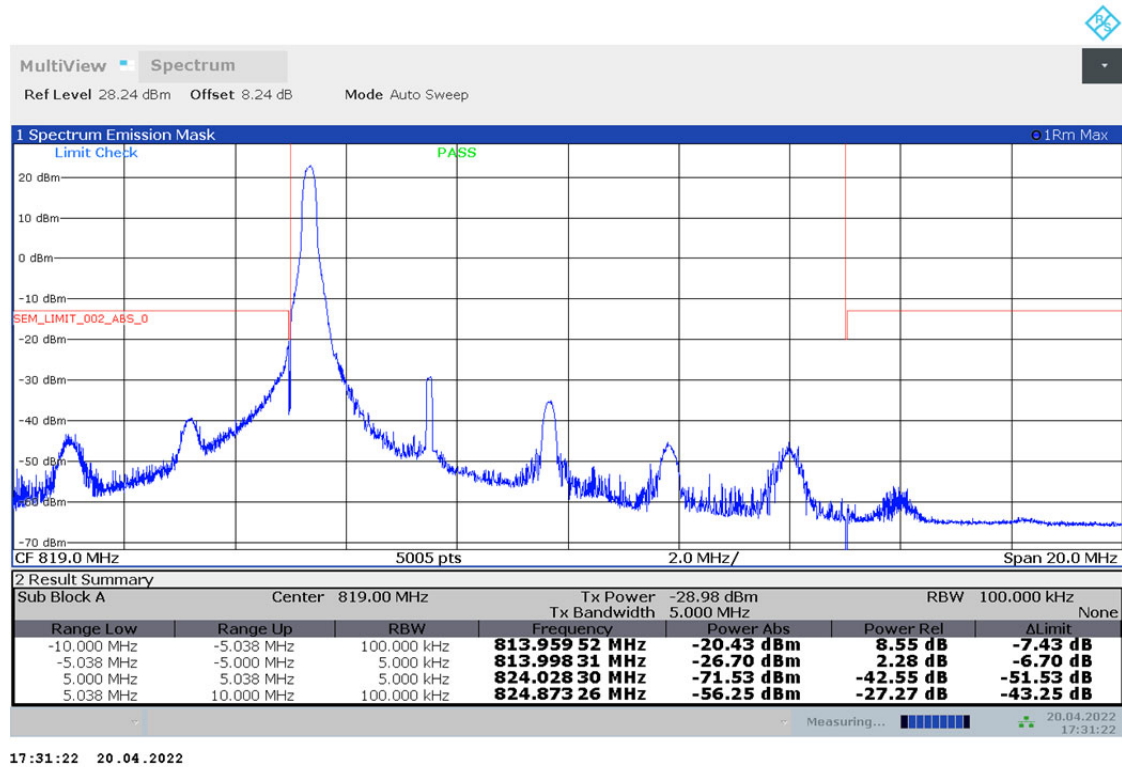
5.2.24 TM2_1.4MHz_HCH_RB1#5



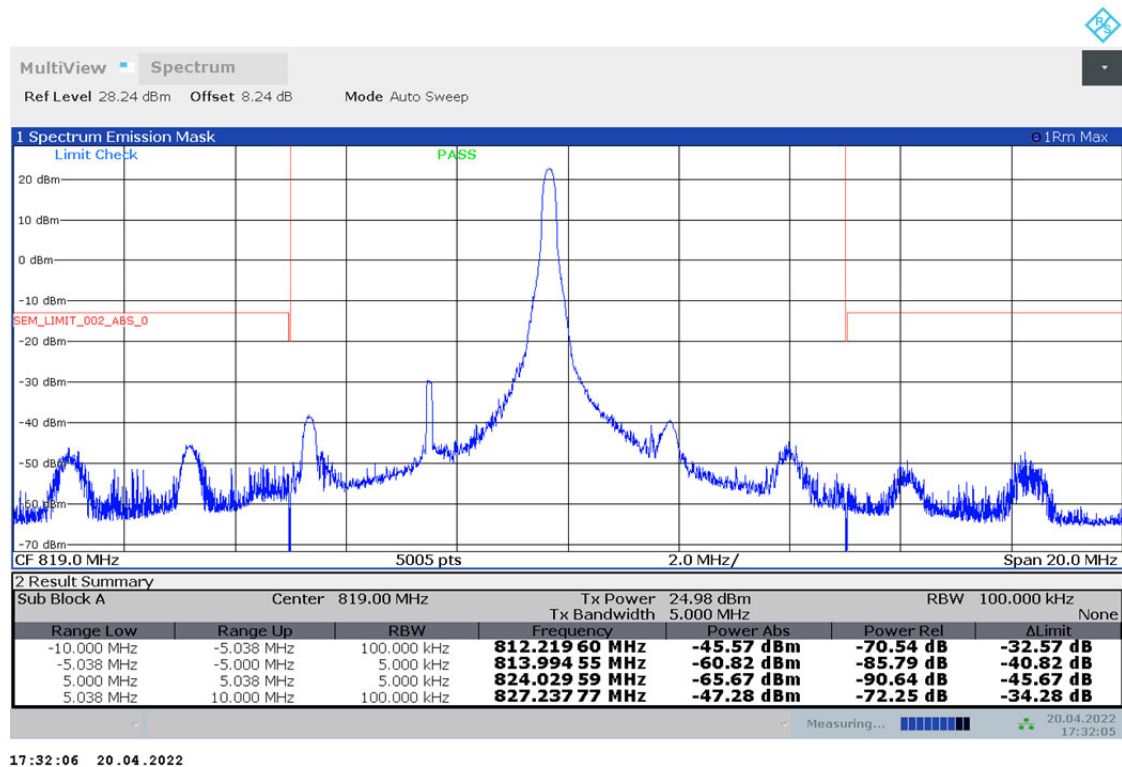
5.2.25 TM2_5MHz_LCH_RB25#0



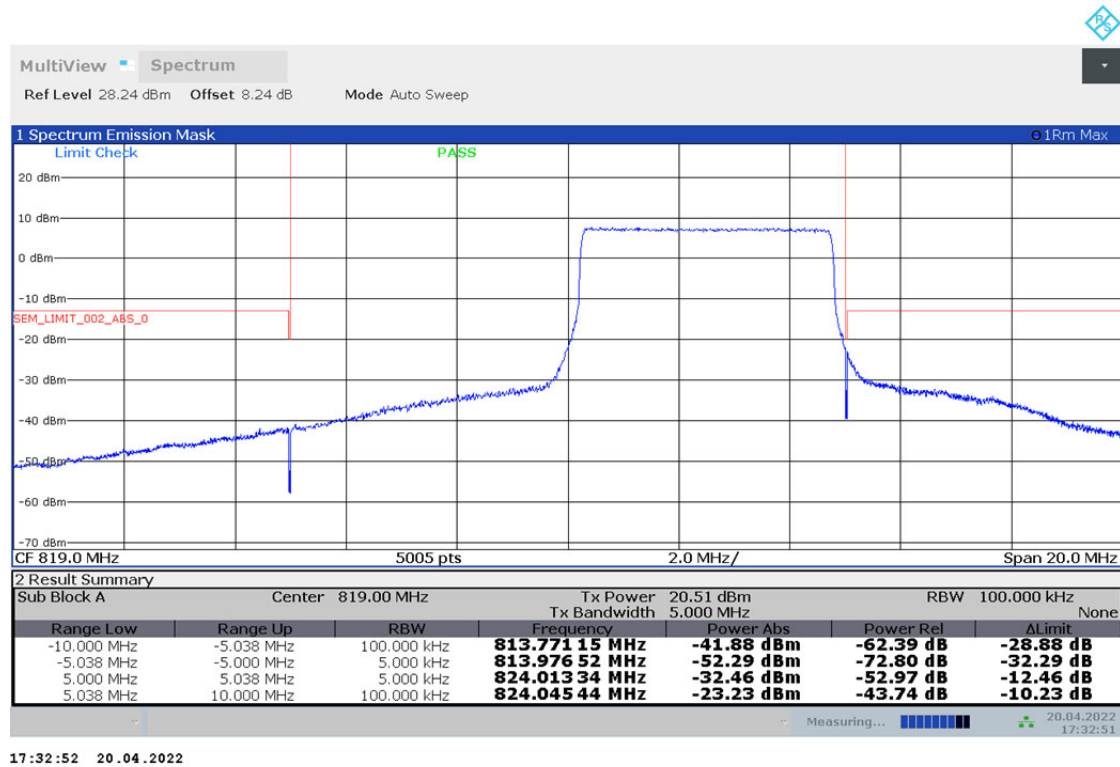
5.2.26 TM2_5MHz_LCH_RB1#0



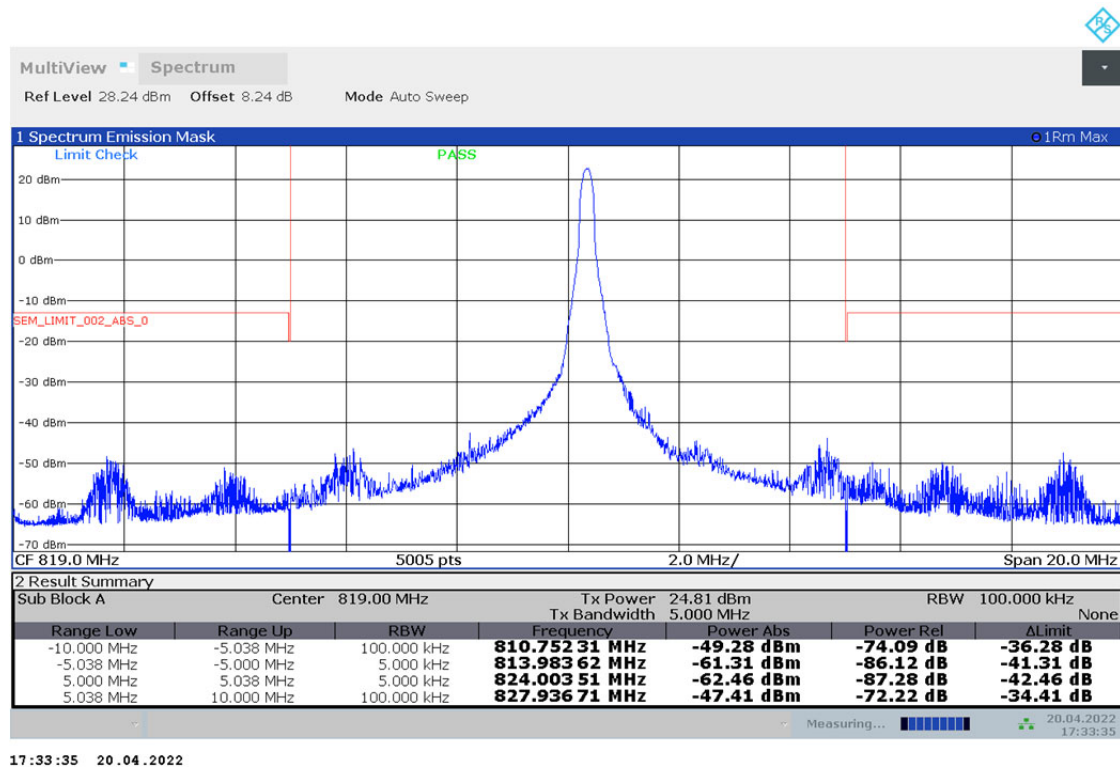
5.2.27 TM2_5MHz_LCH_RB1#24



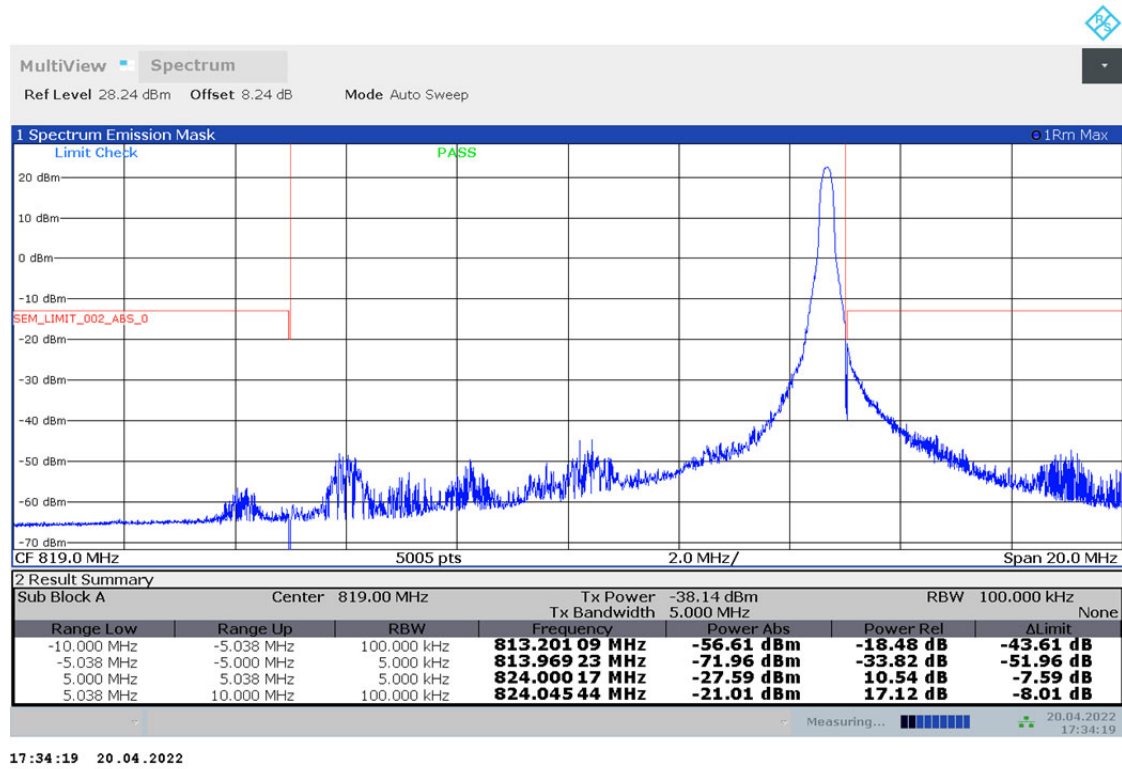
5.2.28 TM2_5MHz_HCH_RB25#0



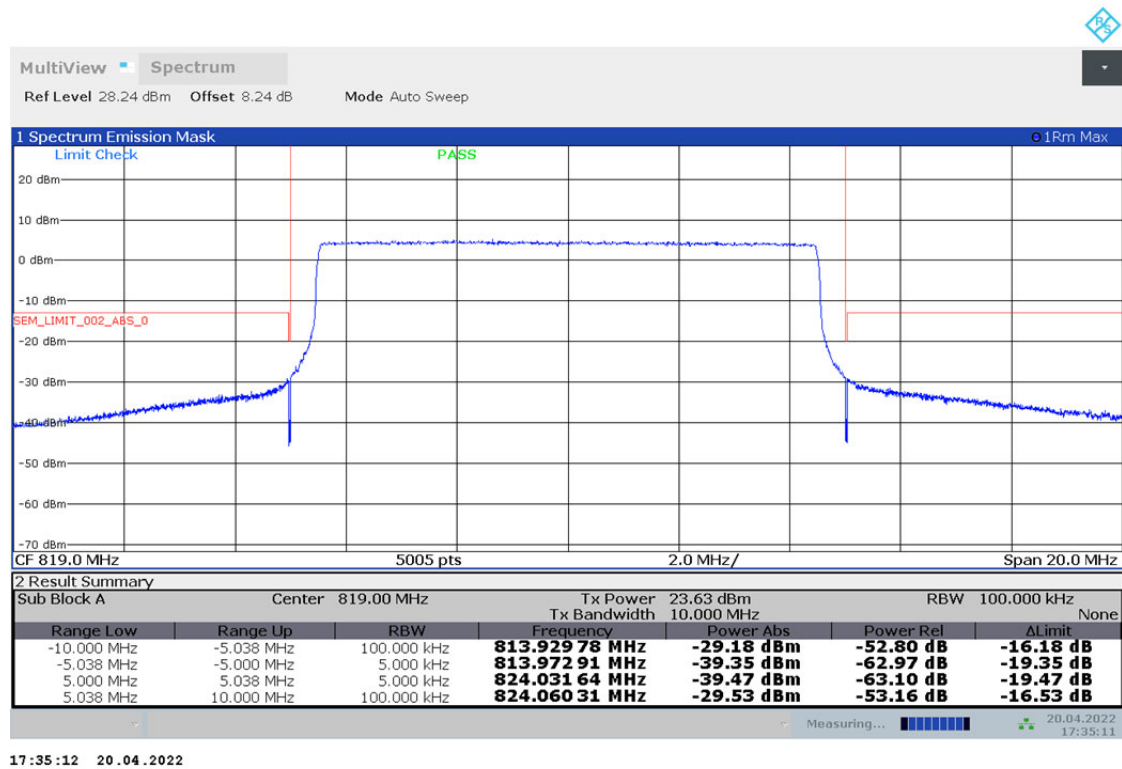
5.2.29 TM2_5MHz_HCH_RB1#0



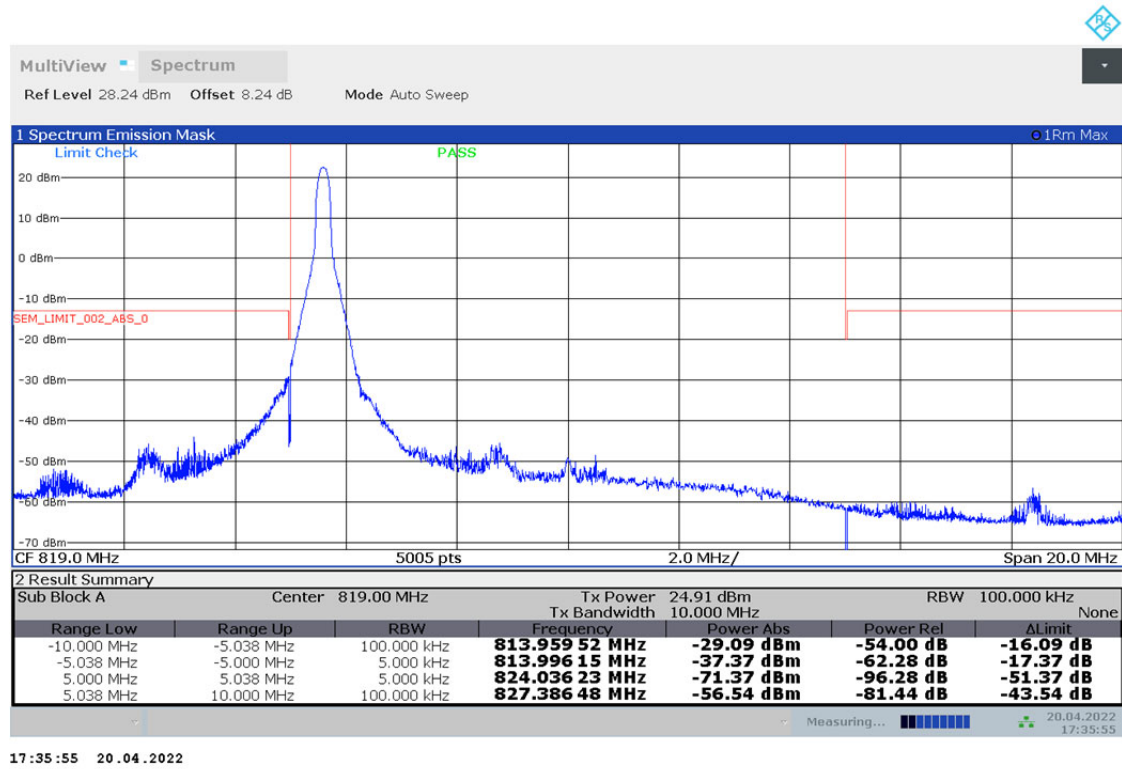
5.2.30 TM2_5MHz_HCH_RB1#24



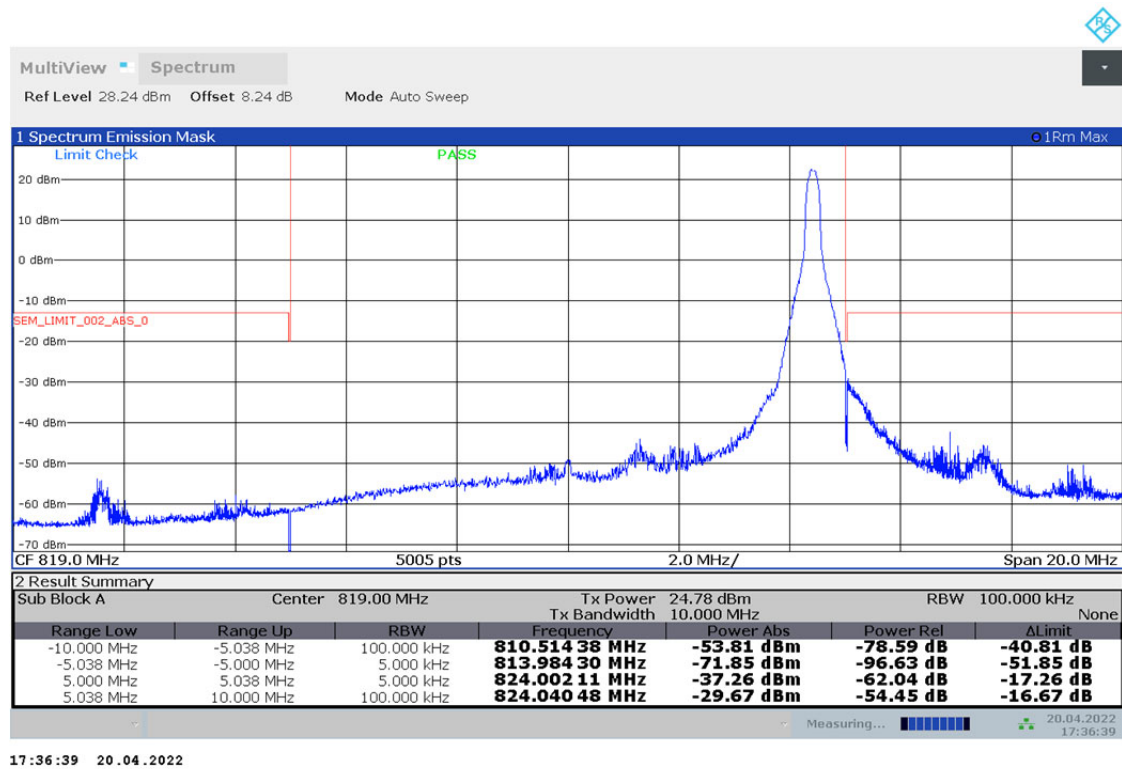
5.2.31 TM2_10MHz_LCH_RB50#0



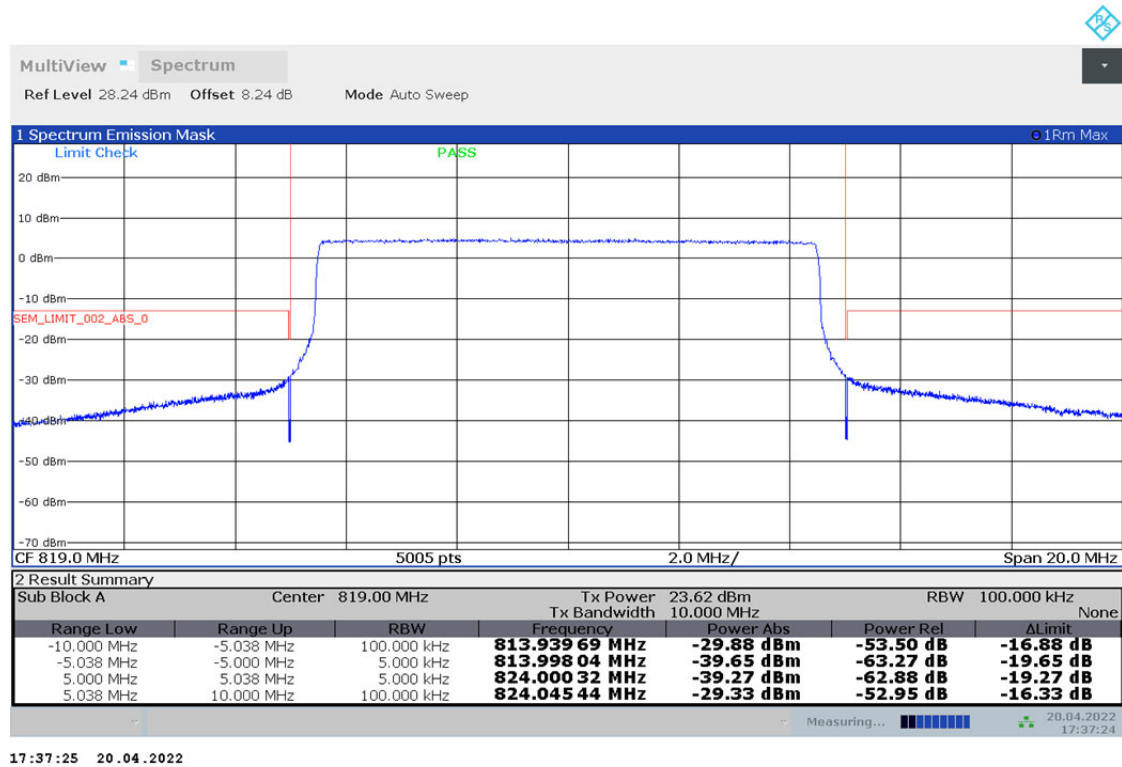
5.2.32 TM2_10MHz_LCH_RB1#0



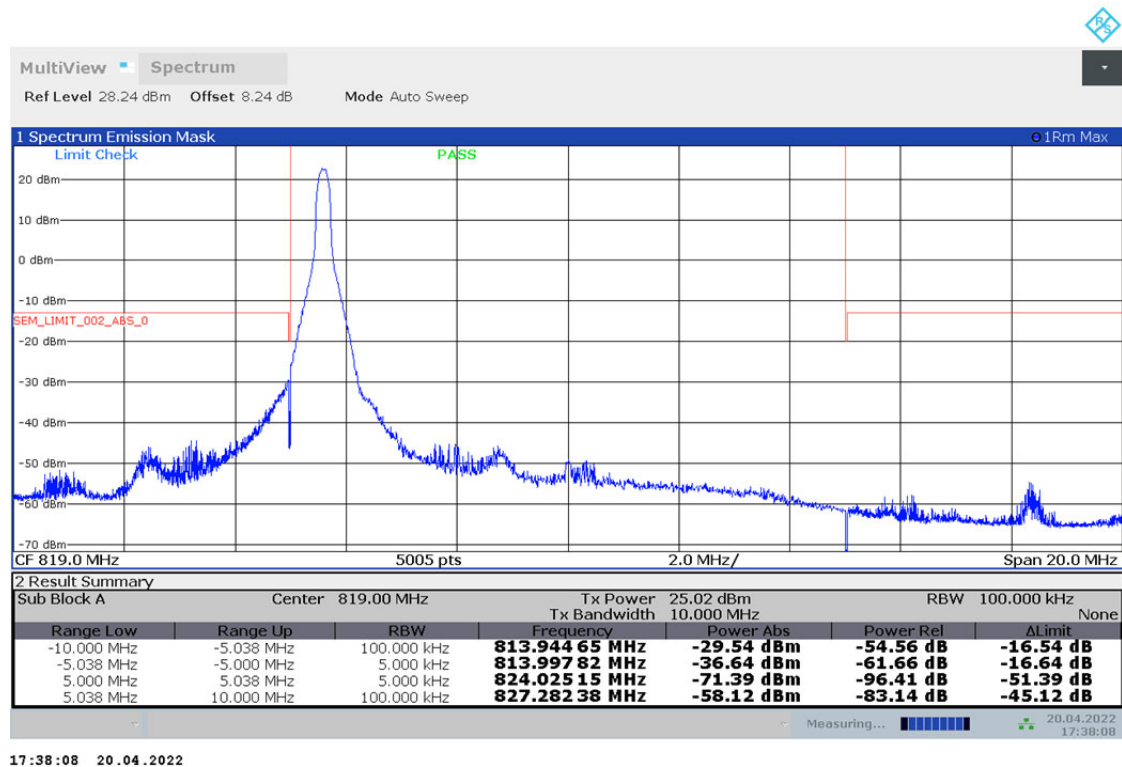
5.2.33 TM2_10MHz_LCH_RB1#49



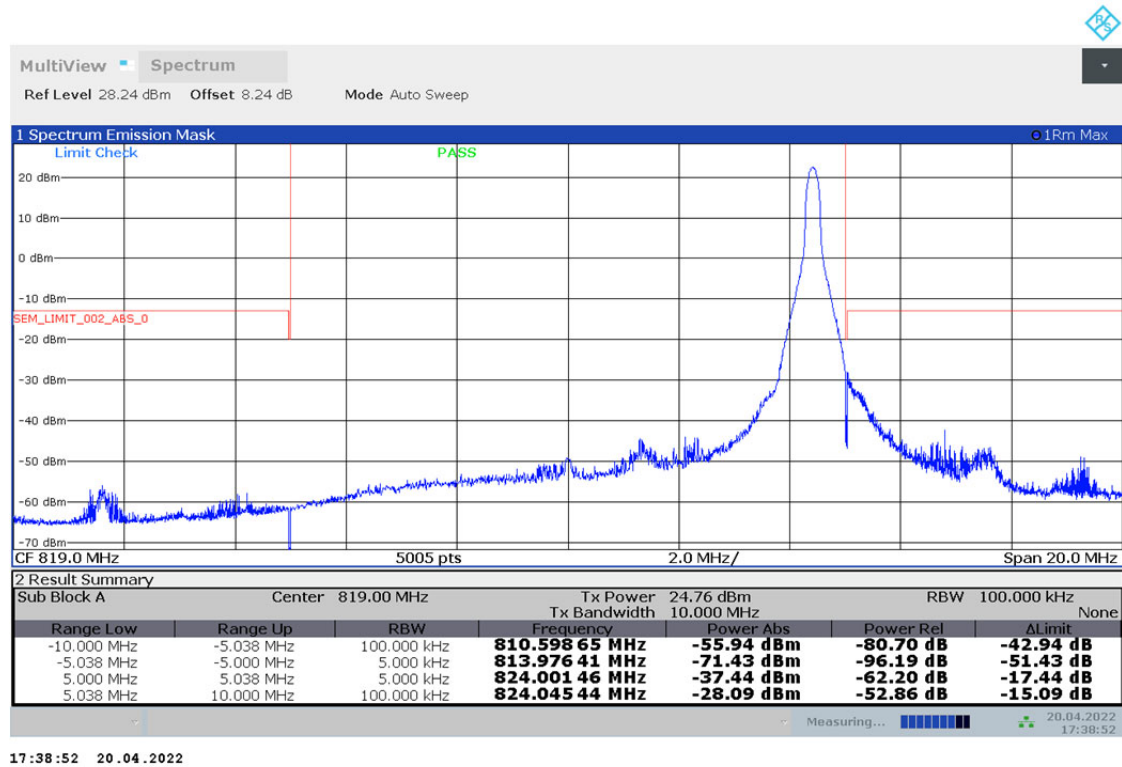
5.2.34 TM2_10MHz_HCH_RB50#0



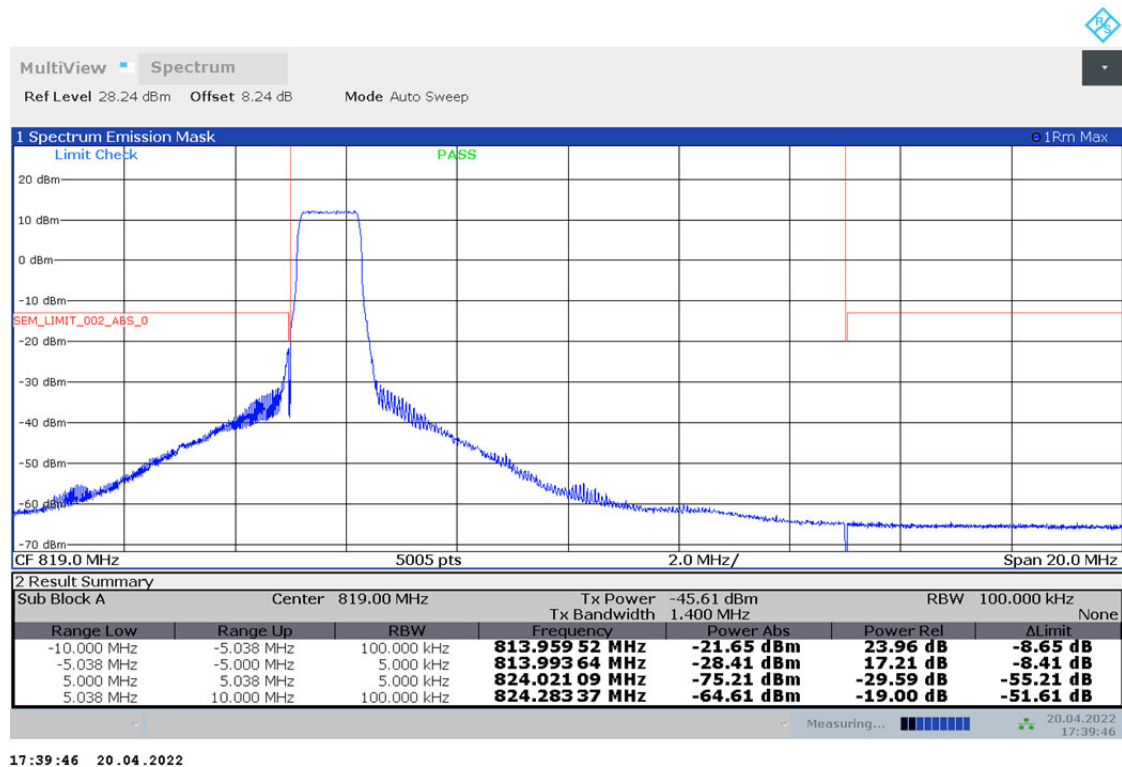
5.2.35 TM2_10MHz_HCH_RB1#0



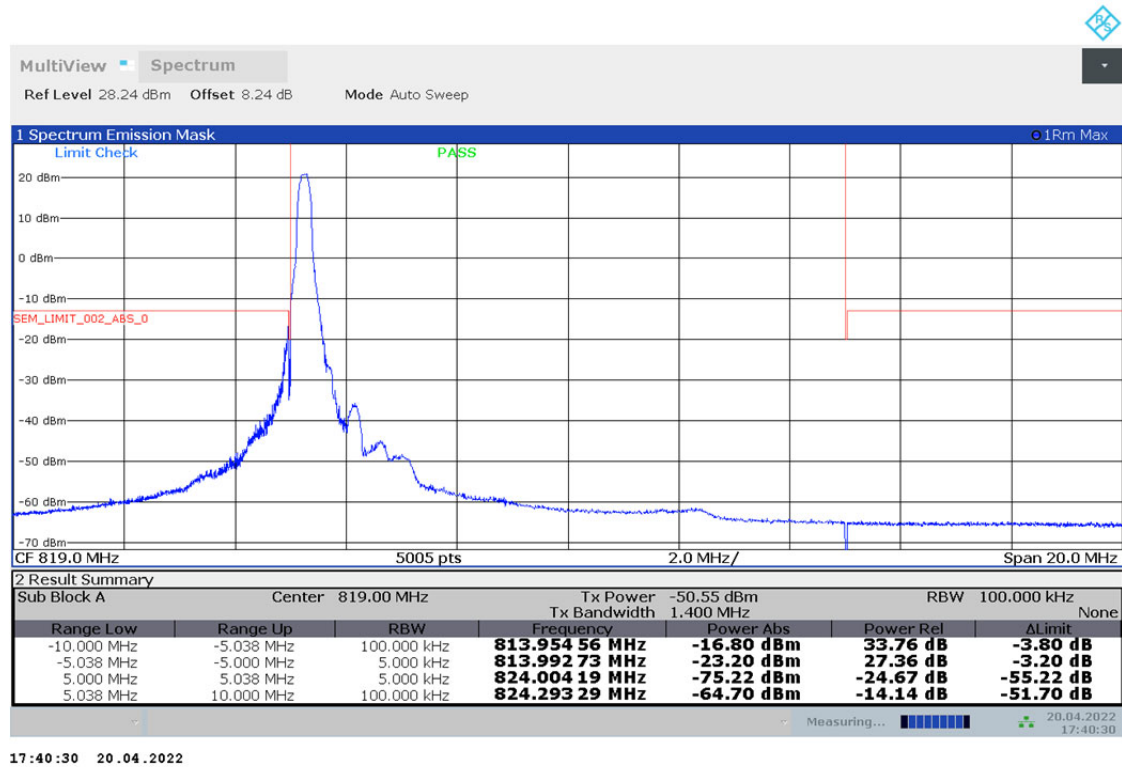
5.2.36 TM2_10MHz_HCH_RB1#49



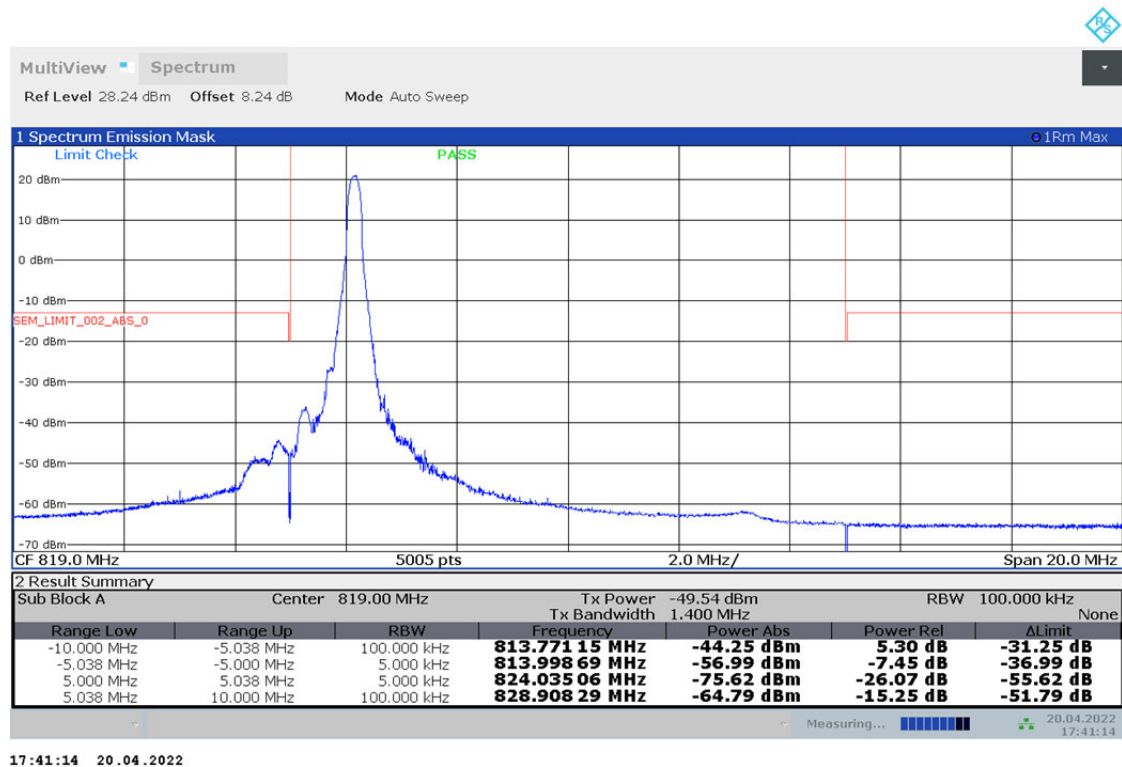
5.2.37 TM3_1.4MHz_LCH_RB6#0



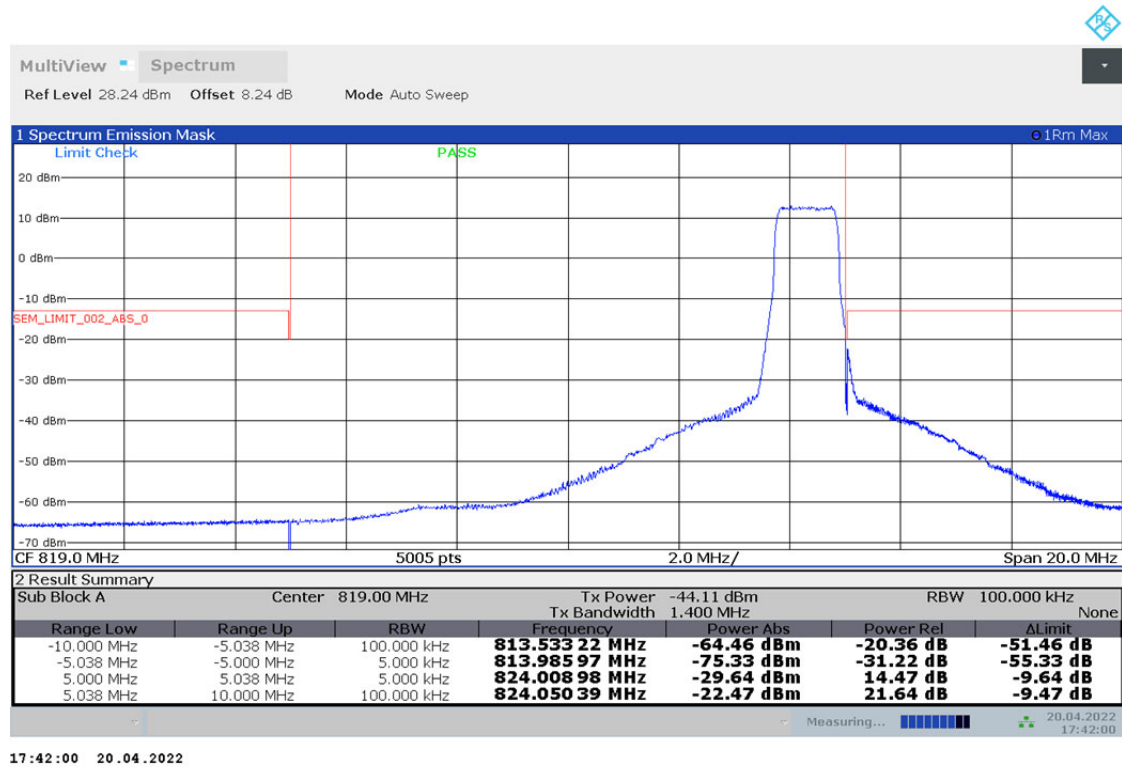
5.2.38 TM3_1.4MHz_LCH_RB1#0



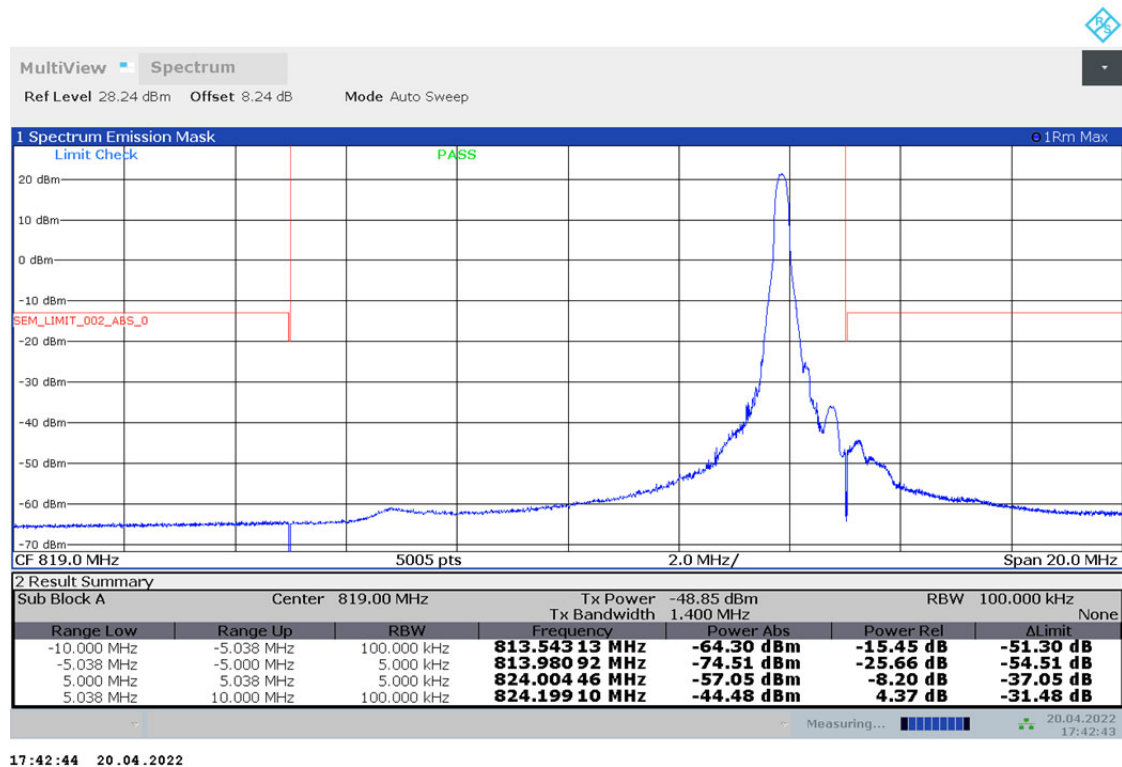
5.2.39 TM3_1.4MHz_LCH_RB1#5



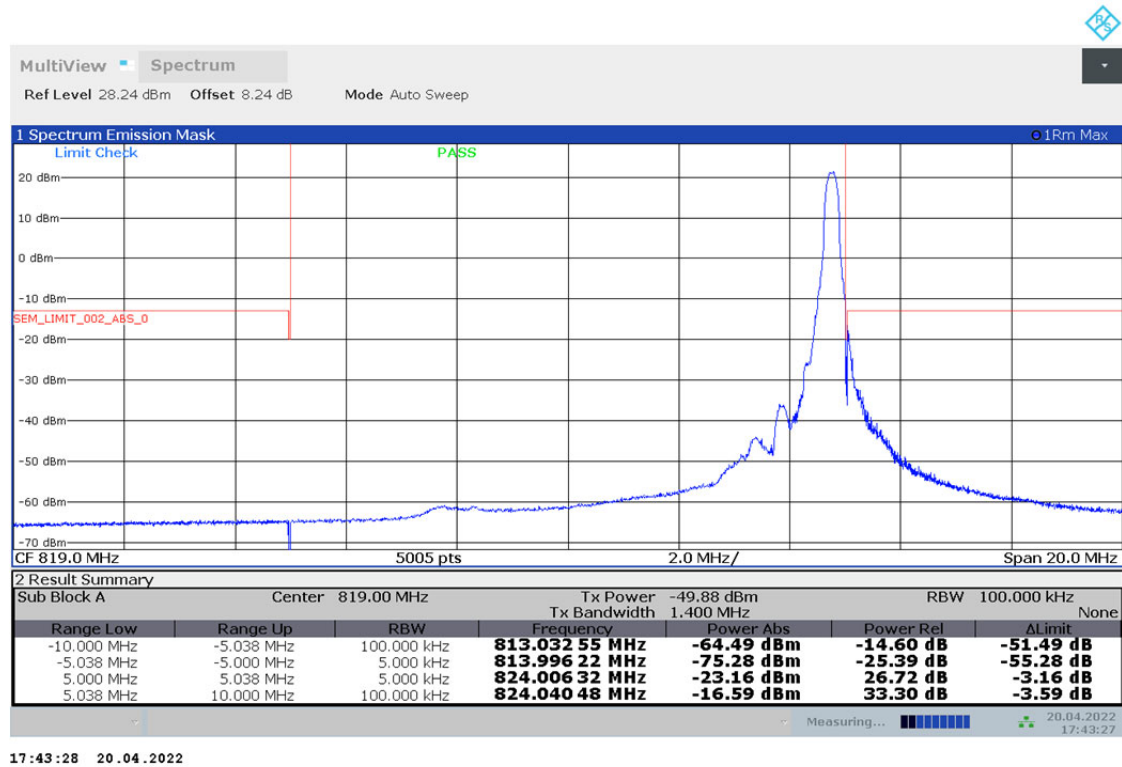
5.2.40 TM3_1.4MHz_HCH_RB6#0



5.2.41 TM3_1.4MHz_HCH_RB1#0

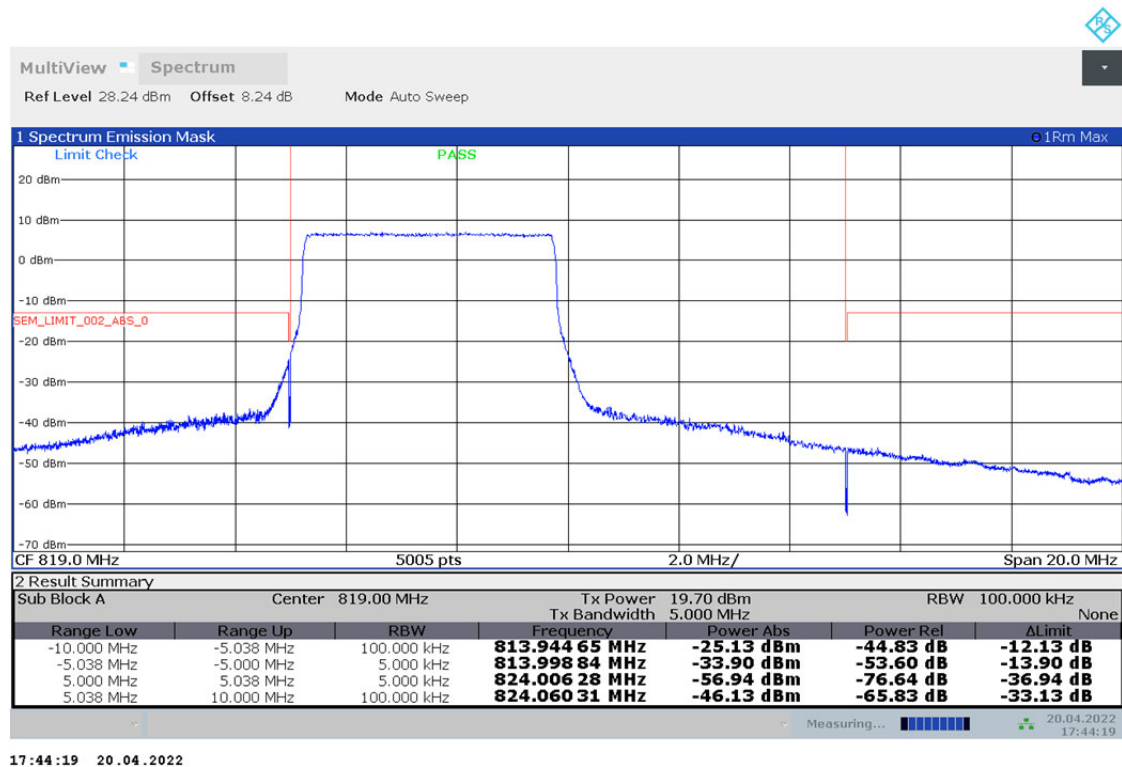


5.2.42 TM3_1.4MHz_HCH_RB1#5



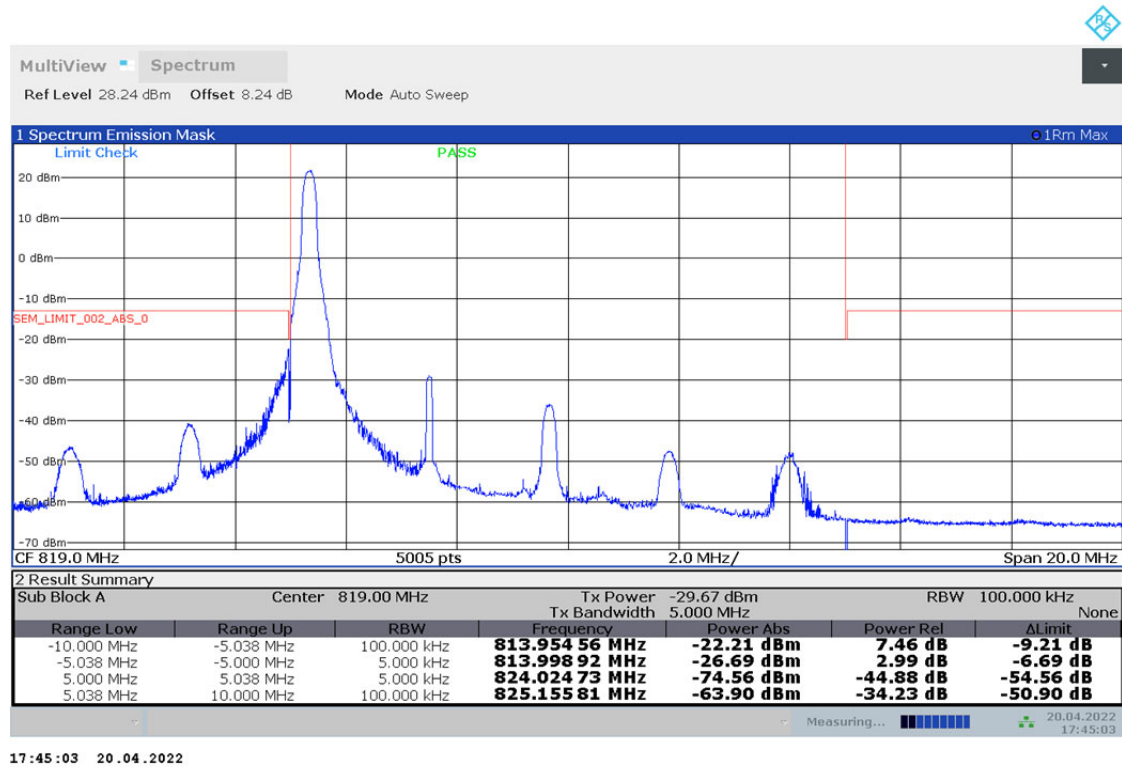
17:43:28 20.04.2022

5.2.43 TM3_5MHz_LCH_RB25#0

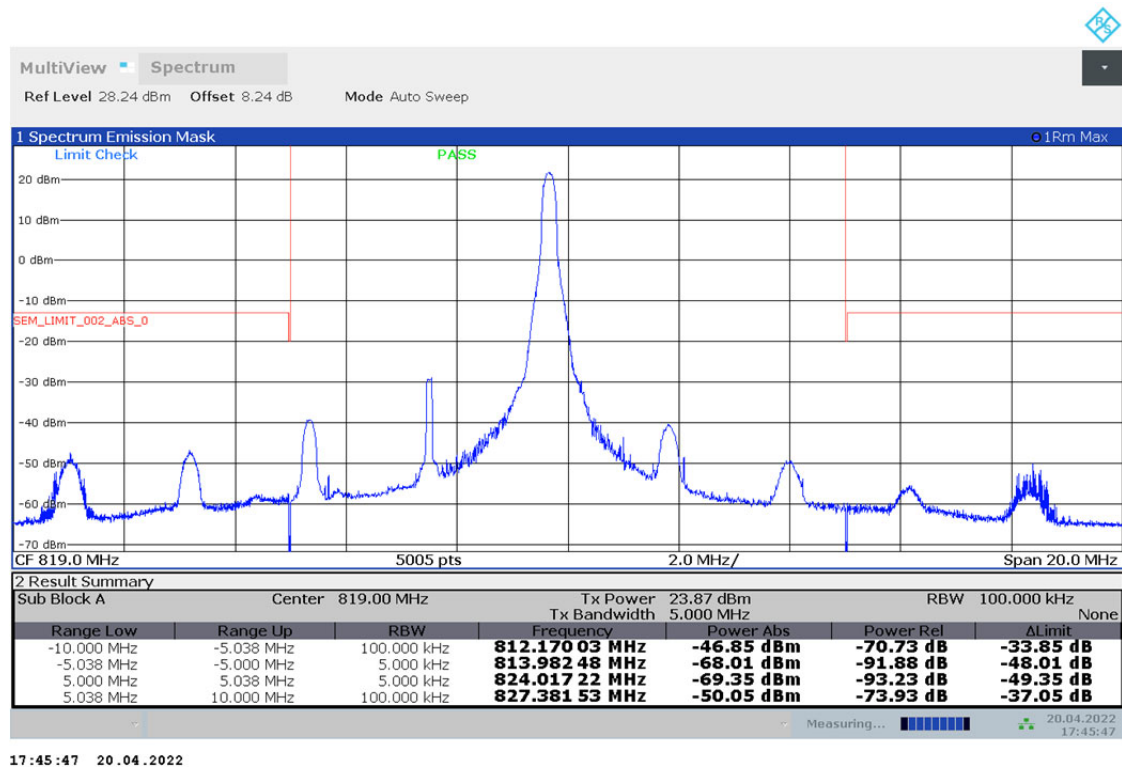


17:44:19 20.04.2022

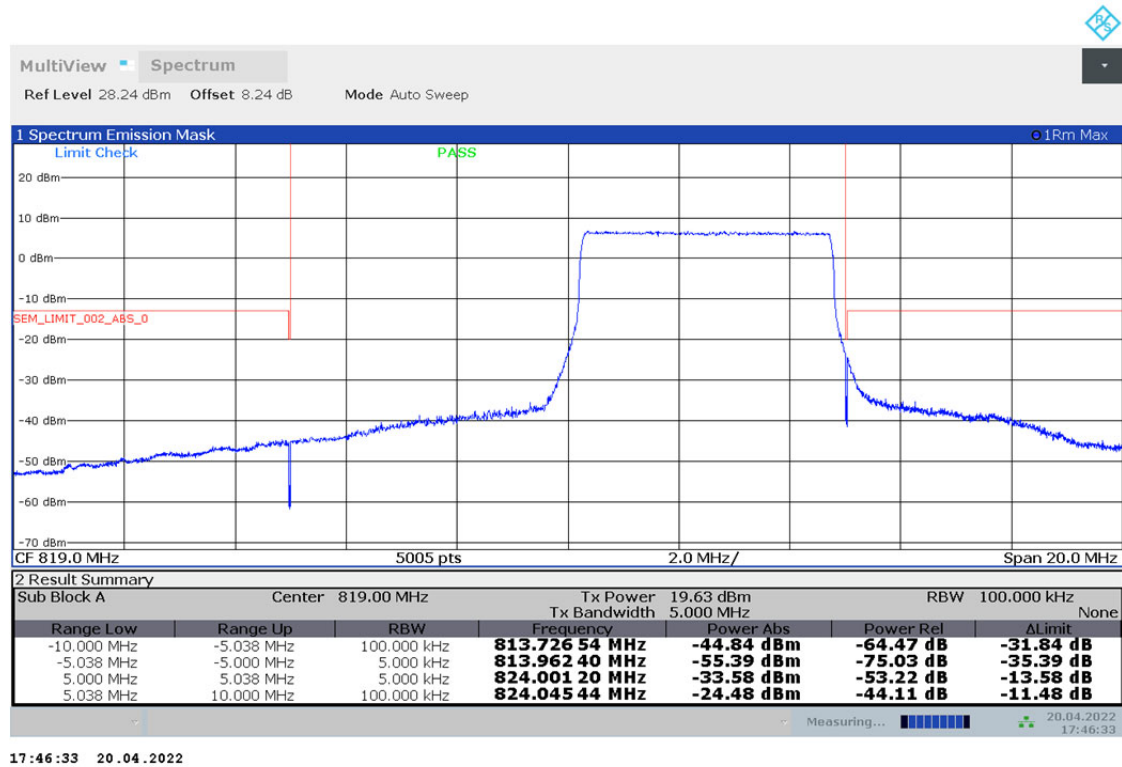
5.2.44 TM3_5MHz_LCH_RB1#0



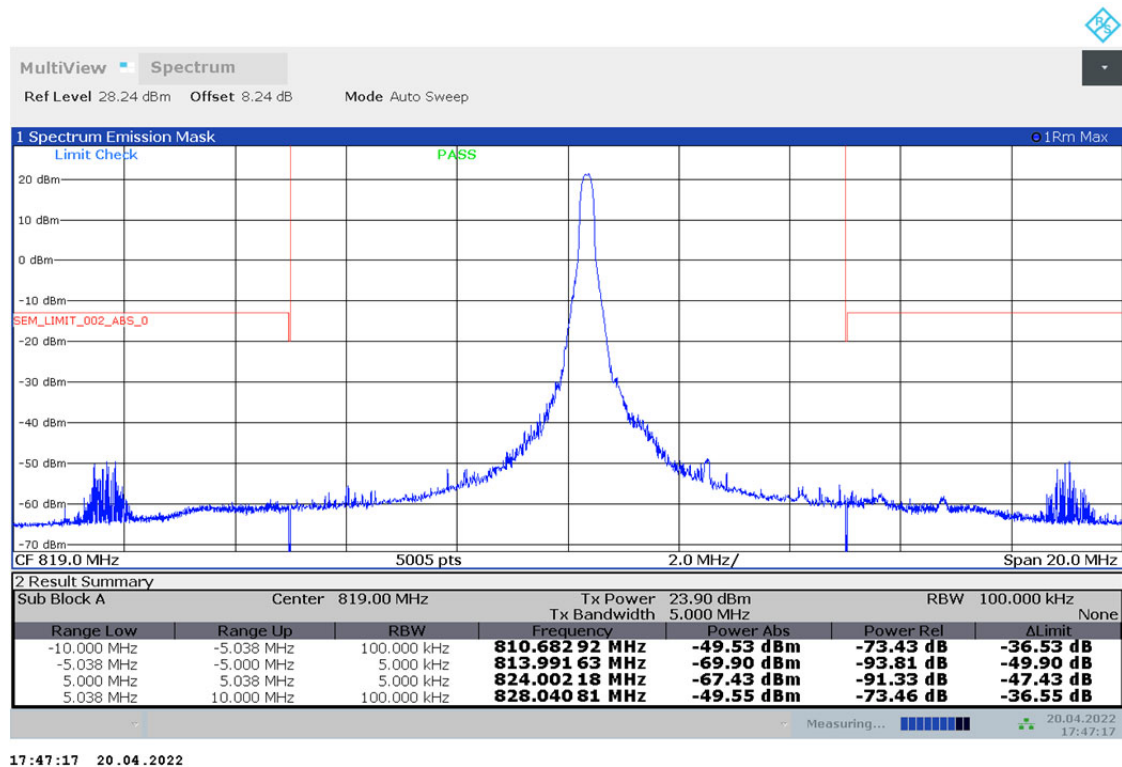
5.2.45 TM3_5MHz_LCH_RB1#24



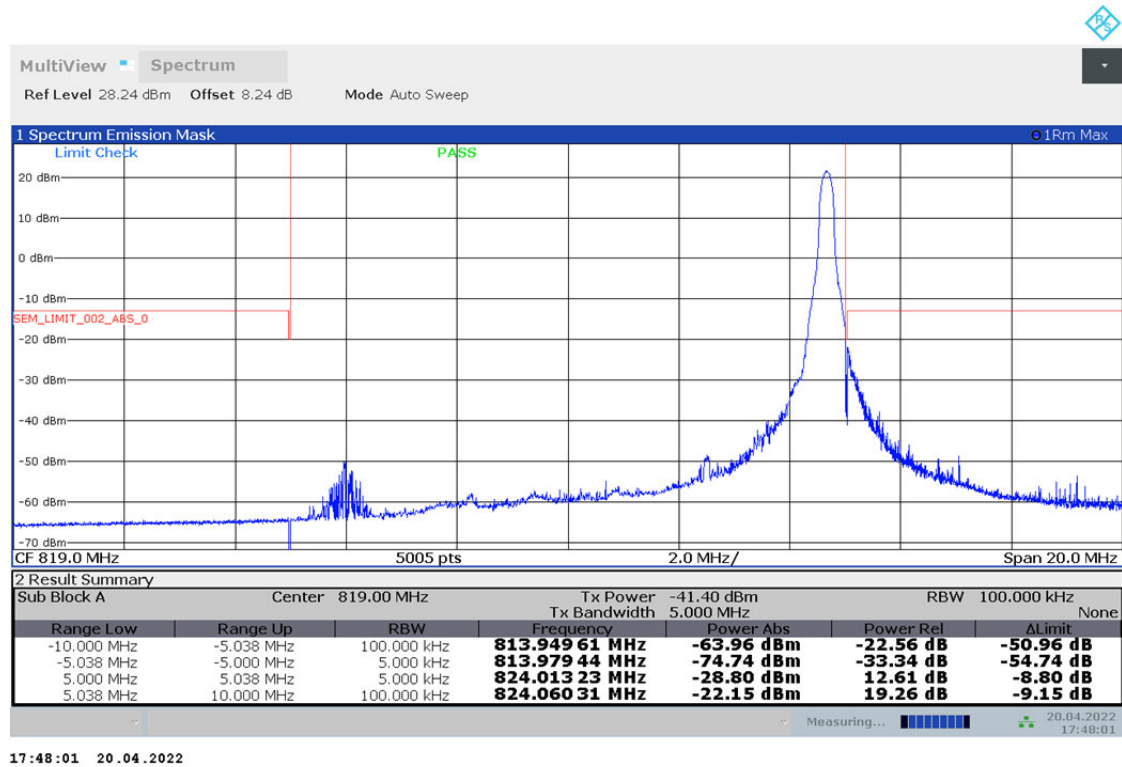
5.2.46 TM3_5MHz_HCH_RB25#0



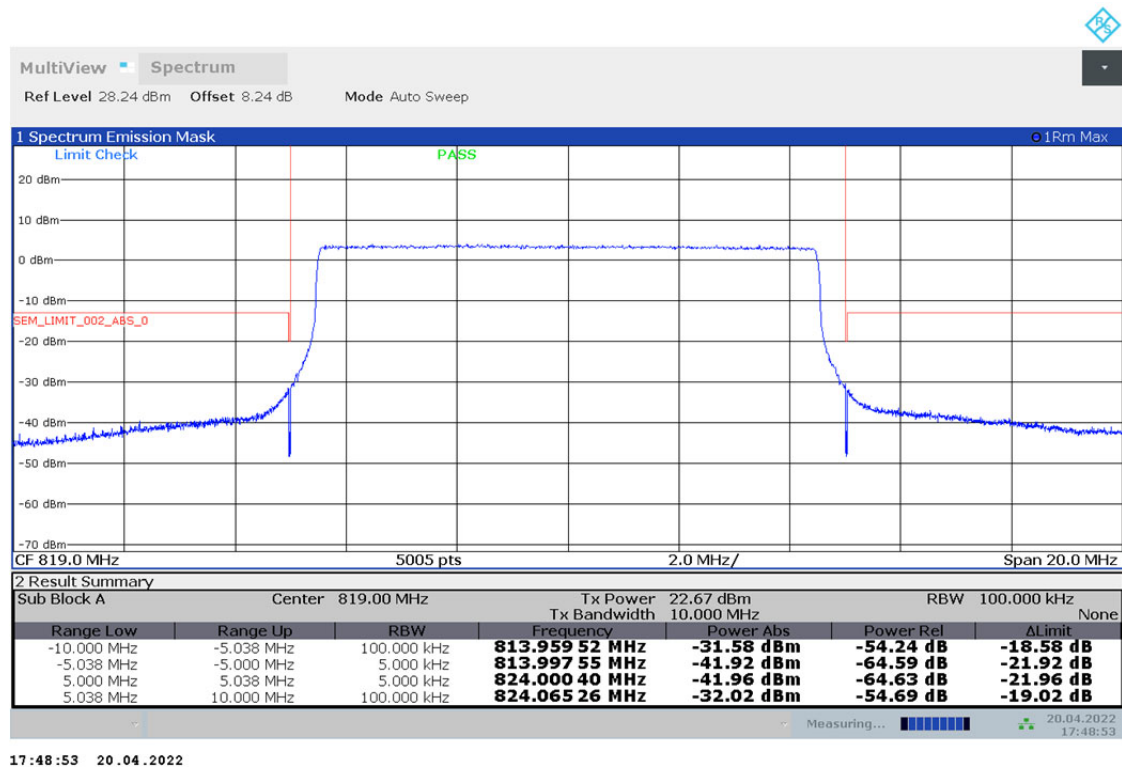
5.2.47 TM3_5MHz_HCH_RB1#0



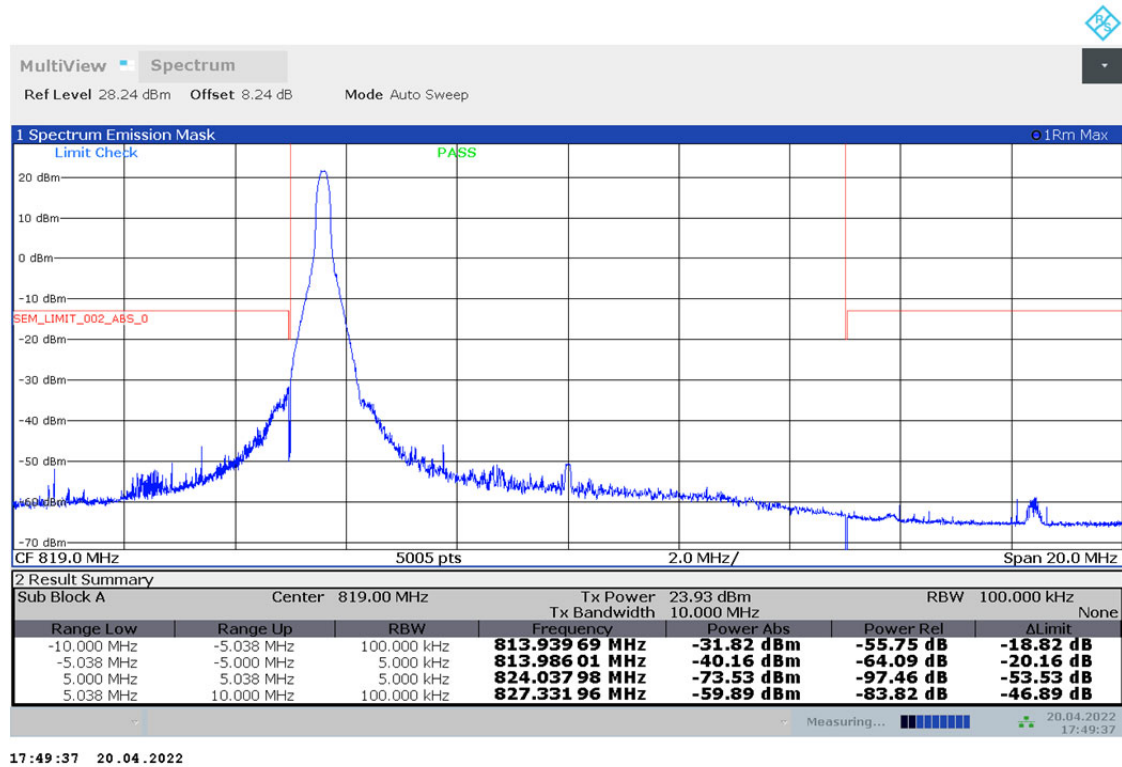
5.2.48 TM3_5MHz_HCH_RB1#24



5.2.49 TM3_10MHz_LCH_RB50#0



5.2.50 TM3_10MHz_LCH_RB1#0



5.2.51 TM3_10MHz_LCH_RB1#49

